Allwinner DE3.0 Specification

Revision 1.0

Jan.23, 2018

Revision History

Revision	Date	Description
1.0	Jan. 23,2018	Initial Release Version

Glossary

The glossary is intended to cover the acronyms used in the document.

Term	Definition
R	Read only/non-Write
R/W	Read/Write
RC	Read-Clear/non-Write
RS	Read-Set/non-Write
RC/W	Read-Clear/Write
RS/W	Read-Set/Write
R/WAC	Read/Write-Automatic-Clear，Clear the bit automatically when the operation of complete.Writing 0 has no effect.
R/WC	Read/Write-Clear
R/WS	Read/Write-Set
RC/WS	Read-Clear/Write-Set
RS/WC	Read-Set/Write-Clear
R/W1C	Read/Write 1 to Clear, Write 0 has non-effect
R/W1S	Read/Write 1 to Set, Write 0 has non-effect
R/W1T	Read/Write 1 to Flip, Write 0 has non-effect
R/W0C	Read/Write 0 to Clear, Write 1 has non-effect
R/W0S	Read/Write 0 to Set, Write 1 has non-effect
R/W0T	Read/Write 0 to Flip, Write 1 has non-effect
RC/W1S	Read-Clear/Write 1 to Set, Write 0 has non-effect
RS/W1C	Read-Set/Write 1 to Clear, Write 0 has non-effect
RC/W0S	Read-Clear/Write 0 to Set, Write 1 has non-effect
RS/W0C	Read-Set/Write 0 to Clear, Write 1 has non-effect
W	Write only/non-Read
WC	Write-Clear/non-Read
WS	Write-Set/non-Read
W1	After reset, Write at the first time, non-Write after the first time/Read
WO1	After reset, Write at the first time, non-Write after the first time/non-Read

Contents

Figures

Tables

1 .A63 Display_Engine_Top

1.1 Overview

The Display Engine(DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the *LCD* interface, The DE support four overlay windows to blending, and support image post-processing in the video channel. The display system block diagram show as the Figure1-1.

Features:

- Support output size up to 2560x1440
- Support four alpha blending channels for main display, two channels for aux display.
- Support four overlay layers in each channel, and has a independent scaler.
- Support potter-duff compatible blending operation.
- Support AFBC1.0
- Support hardware accelerator for distortion, chromatic correction and asynchronous time warp for virtual reality.
- Support input format semi-planar of YUV422/YUV420/YUV411 and planar of YUV422/YUV420/ YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565.
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- Support SmartColor3.0 for excellent display experience.
  - Adaptive detail/edge enhancement.
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify.
  - Content adaptive backlight control.
- Support write back and rotation for high efficient dual display and miracast.

1.2 Block Diagram

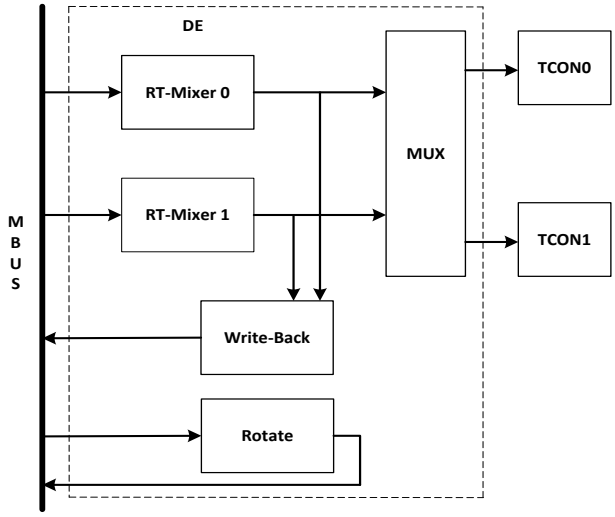


Figure 1-1. Display Top Level Diagram

Figure 1-2, 1-3, 1-4, 1-5, 1-6 shows the block diagram of RT-Mixer0, RT-Mixer1, VEP, DEP.

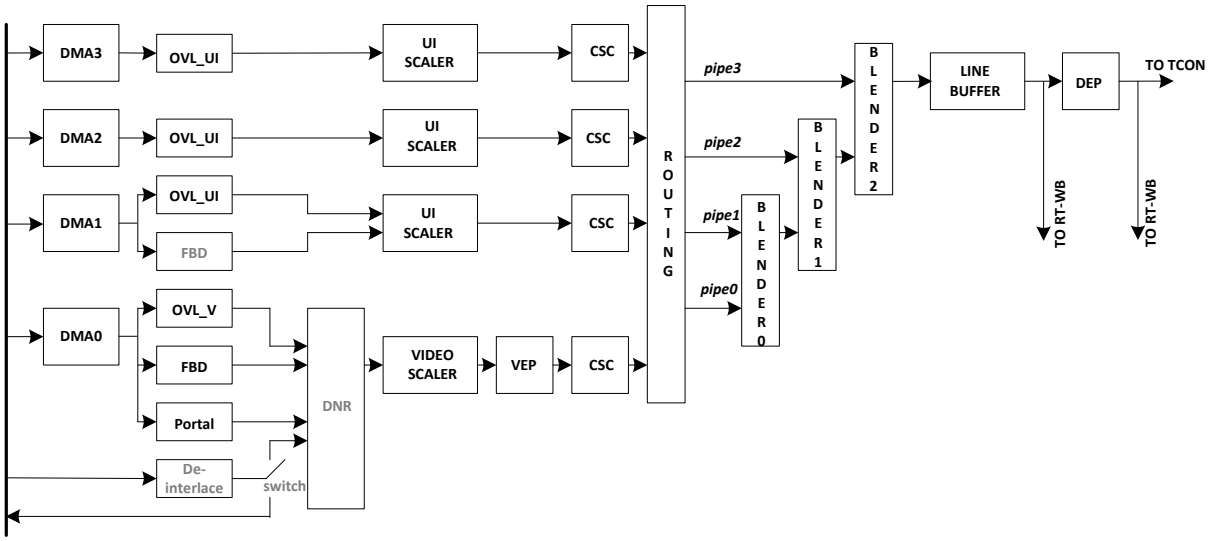


Figure 1-2. RT-MIXER0 Block Diagram

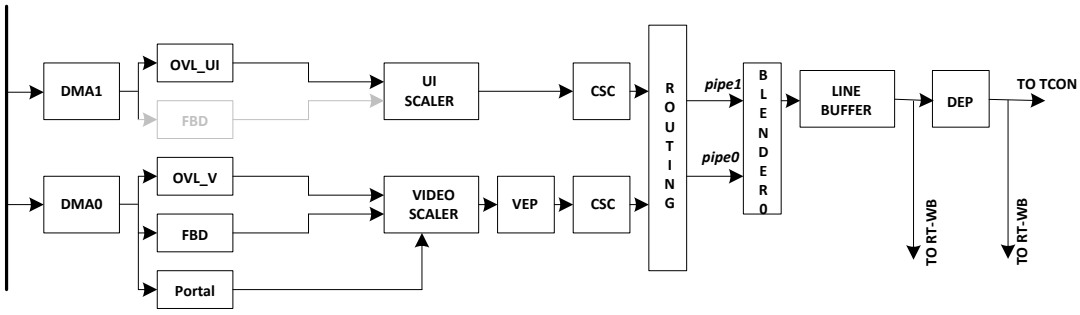
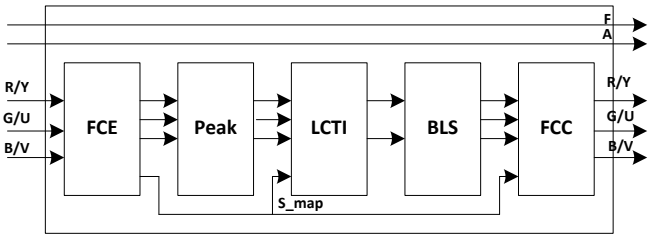


Figure 1-3. RT-MIXER1 Block Diagram



DE300

Figure 1-4. VEP Block Diagram

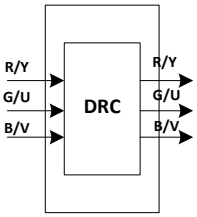


Figure 1-5. DEP Block Diagram

1.3 Operations and Functional Descriptions

1.3.1 System Configure and Requirement

The following table describes the configuration of ***DE***.

Table 1-1. DE Configuration(DE300)

IC Type	DE 版本	量产 IC 速度	Module	4K	Channel	UI Overlay	Video Overlay	UI Scaler	Video Scaler	DI-Online	FBD	Portal	DNS	VEP	DEP	Rot
A63	DE300	600MHz	RTMX0	N	CH0	N	Y	N	Y	N	Y	Y	N	Y	Y	Y
				N	CH1	Y	N	Y	N	N	N		N	N		
				N	CH2	Y	N	Y	N	N	N		N	N		
				N	CH3	Y	N	Y	N	N	N		N	N		
			RTMX1	N	CH0	N	Y	N	Y	N	Y	Y	N	N	N	
				N	CH1	Y	N	Y	N	N	N		N	N		

1.3.2 DE3.0 Configure and Requirement

The following table describes the configuration.

Table 1-2. DE Memory and Speed Requirements

Module Name	Base Address	Memory Range
Display System	0x01000000	64K
RT-WB	0x01010000	64K
Rotate	0x01020000	64K
RT-Mixer0	0x01100000	1M
RT-Mixer1	0x01200000	1M

Table 1-3. RT-Mixer Address and Memory Requirements

		Module Name	Base Address	Memory Range
RT-Mix0	***RTMX***	rtd	0x01100000	2K
		apb	0x01100800	2K
		ovl0	0x01101000	2K
		ovl1	0x01101800	2K
		ovl2	0x01102000	2K
		ovl3	0x01102800	2K
		portal	0x01105000	2K
		dma	0x01108000	32K
	Scaler	SCALER0	0x01120000	32K
		SCALER1	0x01128000	32K
		SCALER2	0x01130000	32K
		SCALER3	0x01138000	32K
	VEP0	FCE	0x01170000	2K
		Peak	0x01170800	2K
		LCTI	0x01171000	2K
		BLS	0x01171800	2K
		FCC	0x01172000	2K
		VEP_TOP	0x01177000	4K
	VEP1		0x01178000~0x0117ffff	32K
	DNS	DNS	0x01180000	32K
	DEP	DRC	0x011a0000	32K
		Line buffer	0x011c0000	32K
RT-Mix1			0x01200000~	

Note: The method of configuring RT-Mix1 address space is same as RT-Mix0.

Video Channel support alpha function:

a). Considering scalability and alpha channel consumes the line buffer, Add the alpha output at each CSC output.

b). Add the global alpha enable and value configuration register at CSC of each channel. (Please refer to DE RTMIXER Specification), The register function is not controlled by the CSC enable bit.

c). When the channel is UI, the value of overlay alpha is transmitted to CSC, and then the alpha enable bit of CSC is closed, the alpha value from the CSC front unit is in used. When the channel is video, the alpha value of the front channel is not transmitted, the alpha enable bit of front channel is opened, and the global alpha value of CSC is in used.

1.3.3 Clock Sources

Display Engine controller get two different clocks, Users can select one of them to make DE Clock Source. The following table describes the clock sources for DE. Users can see ***Clock Controller Unit(CCU)*** in chapter3 for clock setting, configuration and gating information.

Table 1-4. DE Clock Sources

Clock Sources	Description
PLL_DE	PLL_DE,default value is 600MHz for DE.
PLL_PERIPH0(2x)	Peripheral Clock0 source, divide to about 600MHz for DE.

1.4 DE Register List

Module Name	Base Address
DE	0x01000000

Register Name	Offset	Description
DE_SCLK_GATE	0x00	DE SCLK Gating Register
DE_HCLK_GATE	0x04	DE HCLK Gating Register
DE_AHB_RESET	0x08	DE AHB Reset Register
DE_SCLK_DIV	0x0C	DE SCLK Division Register
DE2TCON_MUX	0x10	DE MUX Register
DE_CMD	0x14	DE CMD Register
/	0x18	/
DE_BIST_CTL	0x1C	DE Bist Control Register
DE_IP_CFG	0x24	DE IP Configure Register

1.5 DE Register Description

1.5.1 DE SCLK Gating Register(Default Value: 0x0000_0000)

Offset: 0x00	Register Name: DE_SCLK_GATE

Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	ROT_SCLK_GATE 0: clock gate 1: clock pass
2	R/W	0x0	WB_SCLK_GATE 0: clock gate 1: clock pass
1	R/W	0x0	CORE1_SCLK_GATE 0: clock gate 1: clock pass
0	R/W	0x0	CORE0_SCLK_GATE 0: clock gate 1: clock pass

1.5.2 DE HCLK Gating Register(Default Value: 0x0000_0000)

Offset: 0x04			Register Name: DE_HCLK_GATE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ROT_HCLK_GATE 0: clock gate 1: clock pass
2	R/W	0x0	WB_HCLK_GATE 0: clock gate 1: clock pass
1	R/W	0x0	CORE1_HCLK_GATE 0: clock gate 1: clock pass
0	R/W	0x0	CORE0_HCLK_GATE 0: clock gate 1: clock pass

1.5.3 DE AHB Reset Register(Default Value: 0x0000_0000)

Offset: 0x08			Register Name: DE_AHB_RESET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ROT_AHB_RESET 0: reset on 1: reset off
2	R/W	0x0	WB_AHB_RESET 0: reset on 1: reset off
1	R/W	0x0	CORE1_AHB_RESET

			0: reset on 1: reset off
0	R/W	0x0	CORE0_AHB_RESET 0: reset on 1: reset off

1.5.4 DE SCLK Division Register(Default Value: 0x0000_0000)

Offset: 0x0C			Register Name: DE_SCLK_DIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	ROT_SCLK_DIV
11:8	R/W	0x0	WB_SCLK_DIV
7:4	R/W	0x0	CORE1_SCLK_DIV
3:0	R/W	0x0	CORE0_SCLK_DIV

1.5.5 DE MUX Register(Default Value: 0x0000_0000)

Offset: 0x10			Register Name: DE2TCON_MUX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DE2TCON_MUX 0: MIXER0->TCON0; MIXER1->TCON1 1: MIXER0->TCON1; MIXER1->TCON0

1.5.6 DE CMD Register(Default Value: 0x0000_0000)

Offset: 0x14			Register Name: DE_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	Reserved
19:16	R/W	0x0	RT_WB_CMD_CTL
15:8	/	/	/
7:4	R/W	0x0	CORE1_CMD_CTL
3:0	R/W	0x0	CORE0_CMD_CTL

注：向 dram 发命令数约 N+2

1.5.7 DE Bist Control Register(Default Value: 0x0000_0000)

Offset: 0x1C			Register Name: DE_BIST_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	BIST_EN 0: disable 1: enable

7:0	R/W	0x0	BIST_SEL

1.5.8 DE IP Configure Register(Default Value: 0x0920_1923)

Offset: 0x0024			Register Name: DE_IP_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R	0x0	RTD1_DI_NO
29:27	R	0x1	RTD1_UI_NO
26:24	R	0x1	RTD1_VIDEO_NO
23:21	R	0x1	RTD1_FBD_NO
20:19	R	0x0	RTD1_DNS_NO
18:17	R	0x0	RTD1_VEP_NO
16	R	0x0	RTD1_DEP_NO
15:14	R	0x0	RTD0_DI_NO
1311	R	0x3	RTD0_UI_NO
10:8	R	0x1	RTD0_VIDEO_NO
7:5	R	0x1	RTD0_FBD_NO
4:3	R	0x0	RTD0_DNS_NO
2:1	R	0x1	RTD0_VEP_NO
0	R	0x1	RTD0_DEP_NO

2 .H6 Display_Engine_Top

2.1 Overview

The Display Engine(DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the *LCD* interface, The DE support four overlay windows to blending, and support image post-processing in the video channel. The display system block diagram show as the Figure1-1.

Features:

- Support output size up to 4096x4096
- Support four alpha blending channels for main display, two channels for aux display.
- Support four overlay layers in each channel, and has a independent scaler.
- Support potter-duff compatible blending operation.
- Support AFBC buffer in main display.
- Support input format semi-planar of YUV422/YUV420/YUV411/P010/P210 and planar of YUV422/YUV420/ YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565.
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- Support 10-bit processing path for HDR video.
- Support HDR2SDR and HLG2HDR conversion for HDR video and SDR2HDR conversion for SDR UI.
- Support SmartColor3.0 for excellent display experience.
  - Adaptive detail/edge enhancement.
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify.
  - Adaptive de-noising with image quality assessment and block detector function.
- Support write back for high efficient dual display and miracast.

2.2 Block Diagram

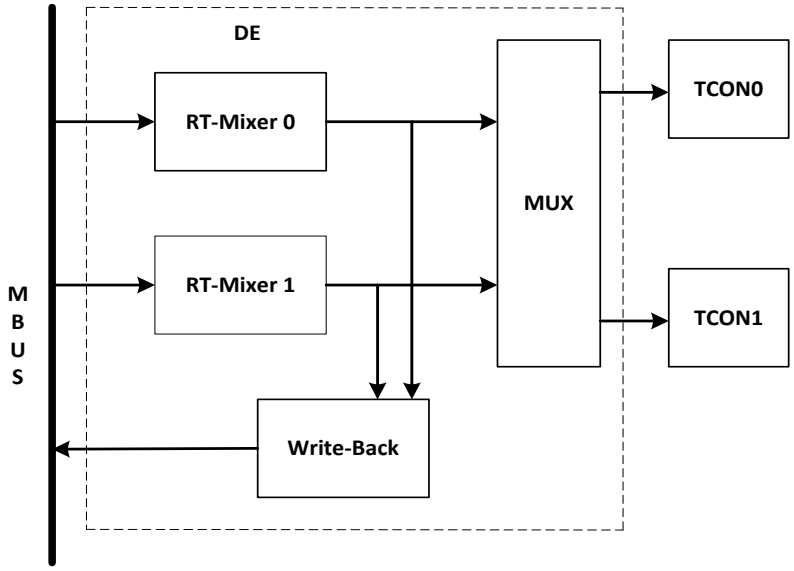


Figure 2-1.DE System Block Diagram

Figure 1-2, 1-3, 1-4, 1-5, 1-6 shows the block diagram of RT-Mixer0, RT-Mixer1, VEP, DEP.

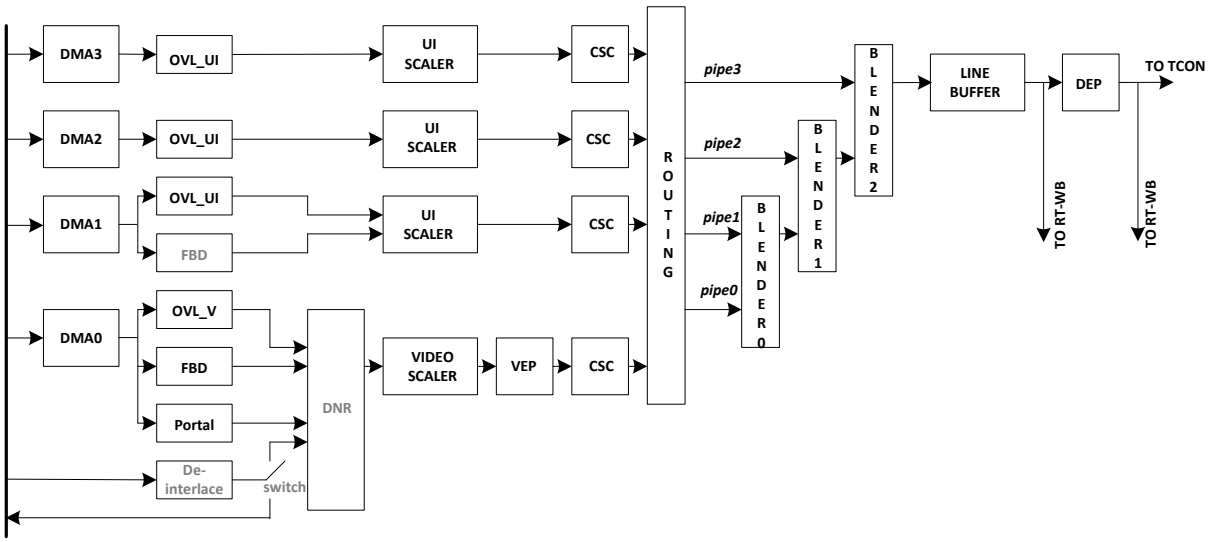


Figure 2-2. RT-MIXER0 Block Diagram

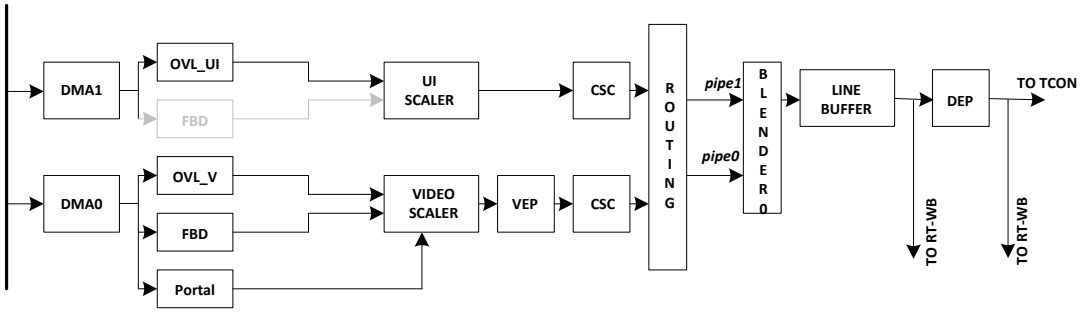
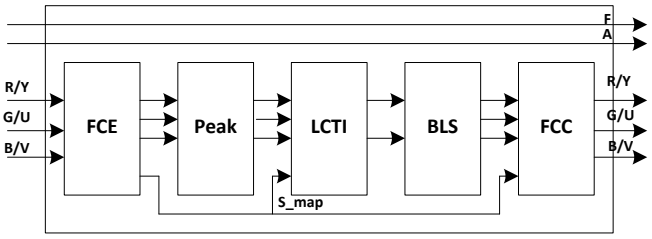


Figure 2-3. RT-MIXER1 Block Diagram



DE300

Figure 2-4. VEP Block Diagram

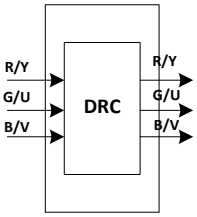


Figure 2-5. DEP Block Diagram

2.3 Operations and Functional Descriptions

2.3.1 System Configure and Requirement

The following table describes the configuration of ***DE***.

Table 2-1. DE Configuration(DE300)

IC Type	DE 版本	量产 IC 速度	Module	4K	Channel	UI Overlay	Video Overlay	UI Scaler	Video Scaler	DI-Online	FBD	DNS	VEP	CDC	DEP	FMT	ROT
H6	DE300	600MHz	RTMX0	Y	CH0	N	Y	N	Y	Y	Y	Y	Y	Y	N	Y	N
				N	CH1	Y	N	Y	N	N	N	N	N	Y			
				N	CH2	Y	N	Y	N	N	N	N	N	N			
				N	CH3	Y	N	Y	N	N	N	N	N	N			
			RTMX1	N	CH0	N	Y	N	Y	N	N	N	N	N	N	N	
				N	CH1	Y	N	Y	N	N	N	N	N	N			

2.3.2 DE3.0 Configure and Requirement

The following table describes the configuration.

Table 2-2. DE Memory and Speed Requirements

Module Name	Base Address	Memory Range
Display System	0x01000000	64K
RT-WB	0x01010000	64K
Rotate	0x01020000	64K
RT-Mixer0	0x01100000	1M
RT-Mixer1	0x01200000	1M

Table 2-3. RT-Mixer Address and Memory Requirements

		Module Name	Base Address	Memory Range
RT-Mix0	***RTMX***	rtd	0x01100000	2K
		apb	0x01100800	2K
		ovl0	0x01101000	2K
		ovl1	0x01101800	2K
		ovl2	0x01102000	2K
		ovl3	0x01102800	2K
		dma	0x01108000	32K
	Scaler	SCALER0	0x01120000	32K
		SCALER1	0x01128000	32K
		SCALER2	0x01130000	32K
		SCALER3	0x01138000	32K
	VEP	FCE	0x01170000	2K
		Peak	0x01170800	2K
		LCTI	0x01171000	2K
		BLS	0x01171800	2K
		FCC	0x01172000	2K
		VEP_TOP	0x01177000	4K
	VEP1		0x01178000~0x0117ffff	32K
	DNS	DNS	0x01180000	32K
	DEP	DRC	0x011a0000	32K
	FMT		0x011a8000	32K
		Line buffer	0x011c0000	32K
	CDC	CDC0	0x011d0000	32K
		CDC1	0x011d8000	32K

RT-Mix1			0x01200000~	

Note: The method of configuring RT-Mix1 address space is same as RT-Mix0.

Video Channel support alpha function:

a). Considering scalability and alpha channel consumes the line buffer, Add the alpha output at each CSC output.

b). Add the global alpha enable and value configuration register at CSC of each channel. (Please refer to DE RTMIXER Specification), The register function is not controlled by the CSC enable bit.

c). When the channel is UI, the value of overlay alpha is transmitted to CSC, and then the alpha enable bit of CSC is closed, the alpha value from the CSC front unit is in used. When the channel is video, the alpha value of the front channel is not transmitted, the alpha enable bit of front channel is opened, and the global alpha value of CSC is in used.

2.3.3 Clock Sources

Display Engine controller get two different clocks, Users can select one of them to make DE Clock Source. The following table describes the clock sources for DE. Users can see ***Clock Controller Unit(CCU)*** in chapter3 for clock setting, configuration and gating information.

Table 2-4. DE Clock Sources

Clock Sources	Description
PLL_DE	PLL_DE,default value is 600MHz for DE.
PLL_PERIPH0(2x)	Peripheral Clock0 source, divide to about 600MHz for DE.

2.4 DE Register List

Module Name	Base Address
DE	0x01000000

Register Name	Offset	Description
DE_SCLK_GATE	0x00	DE SCLK Gating Register
DE_HCLK_GATE	0x04	DE HCLK Gating Register
DE_AHB_RESET	0x08	DE AHB Reset Register
DE_SCLK_DIV	0x0C	DE SCLK Division Register
DE2TCON_MUX	0x10	DE MUX Register
DE_CMD	0x14	DE CMD Register
/	0x18	/
DE_BIST_CTL	0x1C	DE Bist Control Register
DE_IP_CFG	0x24	DE IP Configure Register

2.5 DE Register Description

2.5.1 DE SCLK Gating Register(Default Value: 0x0000_0000)

Offset: 0x00			Register Name: DE_SCLK_GATE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ROT_SCLK_GATE 0: clock gate 1: clock pass
2	R/W	0x0	WB_SCLK_GATE 0: clock gate 1: clock pass
1	R/W	0x0	CORE1_SCLK_GATE 0: clock gate 1: clock pass
0	R/W	0x0	CORE0_SCLK_GATE 0: clock gate 1: clock pass

2.5.2 DE HCLK Gating Register(Default Value: 0x0000_0000)

Offset: 0x04			Register Name: DE_HCLK_GATE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ROT_HCLK_GATE 0: clock gate 1: clock pass
2	R/W	0x0	WB_HCLK_GATE 0: clock gate 1: clock pass
1	R/W	0x0	CORE1_HCLK_GATE 0: clock gate 1: clock pass
0	R/W	0x0	CORE0_HCLK_GATE 0: clock gate 1: clock pass

2.5.3 DE AHB Reset Register(Default Value: 0x0000_0000)

Offset: 0x08			Register Name: DE_AHB_RESET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3	R/W	0x0	ROT_AHB_RESET 0: reset on 1: reset off
2	R/W	0x0	WB_AHB_RESET 0: reset on 1: reset off
1	R/W	0x0	CORE1_AHB_RESET 0: reset on 1: reset off
0	R/W	0x0	CORE0_AHB_RESET 0: reset on 1: reset off

2.5.4 DE SCLK Division Register(Default Value: 0x0000_0000)

Offset: 0x0C			Register Name: DE_SCLK_DIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	ROT_SCLK_DIV
11:8	R/W	0x0	WB_SCLK_DIV
7:4	R/W	0x0	CORE1_SCLK_DIV
3:0	R/W	0x0	CORE0_SCLK_DIV

2.5.5 DE MUX Register(Default Value: 0x0000_0000)

Offset: 0x10			Register Name: DE2TCON_MUX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DE2TCON_MUX 0: MIXER0->TCON0; MIXER1->TCON1 1: MIXER0->TCON1; MIXER1->TCON0

2.5.6 DE CMD Register(Default Value: 0x0000_0000)

Offset: 0x14			Register Name: DE_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	Reserved
19:16	R/W	0x0	RT_WB_CMD_CTL
15:8	/	/	/
7:4	R/W	0x0	CORE1_CMD_CTL
3:0	R/W	0x0	CORE0_CMD_CTL

Note: The number of commands transmitted to dram are about N+2.

2.5.7 DE Bist Control Register(Default Value: 0x0000_0000)

Offset: 0x1C			Register Name: DE_BIST_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	BIST_EN 0: disable 1: enable
7:0	R/W	0x0	BIST_SEL

2.5.8 DE IP Configure Register(Default Value: 0x0920_1923)

Offset: 0x0024			Register Name: DE_IP_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R	0x0	RTD1_DI_NO
29:27	R	0x1	RTD1_UI_NO
26:24	R	0x1	RTD1_VIDEO_NO
23:21	R	0x1	RTD1_FBD_NO
20:19	R	0x0	RTD1_DNS_NO
18:17	R	0x0	RTD1_VEP_NO
16	R	0x0	RTD1_DEP_NO
15:14	R	0x0	RTD0_DI_NO
1311	R	0x3	RTD0_UI_NO
10:8	R	0x1	RTD0_VIDEO_NO
7:5	R	0x1	RTD0_FBD_NO
4:3	R	0x0	RTD0_DNS_NO
2:1	R	0x1	RTD0_VEP_NO
0	R	0x1	RTD0_DEP_NO

3 .Sub_Module_Specification

3.1 DE BLS Specification

3.1.1 BLS Overview

Blue Level Stretch (BLS) module contains two parts: CSC stage (if input data stream is RGB format) and Blue Gain Stage. CSC module converts the pixels between RGB and YUV, if not implemented in a YUV data stream.
Then gain stage will find gain coefficient from LUT according to different Y and U/V values, then multiply U and V with gain.
The BLS module including following feature:

- Maximum input frame size: 4096×2160
- Performance: 300M pixels/second.
- Update register settings when VSYNC comes.

3.1.2 BLS Block Diagram

Figure 3-1 shows the data flow of BLS module. If RGB stream is input, CSC stage ahead and behind the Blue gain stage must be enabled.

Internal RGB/YUV data path are all 10bit. When connected to 8bit data path, RGB inputs are padded with 2b'00 at the LSB, while RGB outputs are truncated with higher 8 MSB.

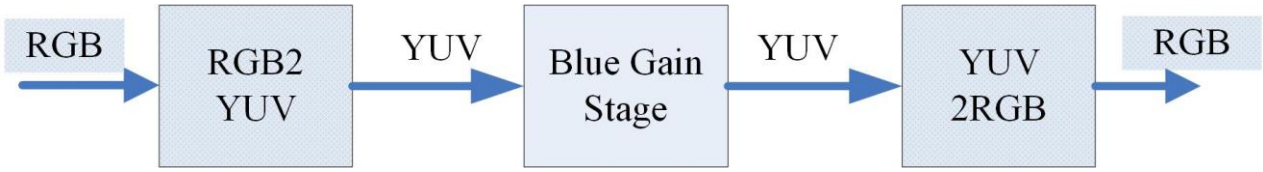


Figure 3-1. BLS module data flow

3.1.3 BLS Algorithm Descriptions

Here introduce the CSC and gain stage.

3.1.3.1 CSC stage

Normally use the BT709 standard for conversion. Using Fixed coefficients for hardware implementation. And 10bit YUV data is keep between two CSC stage.

RGB_10bit 2YUV_10bit

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \left(\begin{bmatrix} C00 & C01 & C02 \\ C10 & C11 & C12 \\ C20 & C21 & C22 \end{bmatrix} \times \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} C03 \\ C13 \\ C23 \end{bmatrix} \right) >> 10$$

$$\begin{bmatrix} C00 & C01 & C02 \\ C10 & C11 & C12 \\ C20 & C21 & C22 \end{bmatrix} = \begin{bmatrix} 218 & 732 & 74 \\ -118 & -394 & 512 \\ 512 & -465 & -47 \end{bmatrix}, \begin{bmatrix} C03 \\ C13 \\ C23 \end{bmatrix} = \begin{bmatrix} 0x800 \\ 0x80800 \\ 0x80800 \end{bmatrix}$$

YUV_10bit2RGB_ 10bit

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \left(\begin{bmatrix} C00 & C01 & C02 \\ C10 & C11 & C12 \\ C20 & C21 & C22 \end{bmatrix} \times \begin{bmatrix} Y \\ U \\ V \end{bmatrix} + \begin{bmatrix} C03 \\ C13 \\ C23 \end{bmatrix} \right) >> 10$$

$$\begin{bmatrix} C00 & C01 & C02 \\ C10 & C11 & C12 \\ C20 & C21 & C22 \end{bmatrix} = \begin{bmatrix} 1024 & 0 & 1613 \\ 1024 & -191 & -479 \\ 1024 & 1901 & 0 \end{bmatrix}, \begin{bmatrix} C03 \\ C13 \\ C23 \end{bmatrix} = \begin{bmatrix} -827802 \\ 345457 \\ -975127 \end{bmatrix}$$

3.1.4 Module Register list

Module Name	Base Address
BLS	0x00500000

Register name	Offset	Description
BLS_CTRL_REG	0x00	BLS module control register
BLS_SIZE_REG	0x04	BLS size register
BLS_WIN0_REG	0x08	BLS window setting register0
BLS_WIN1_REG	0x0C	BLS window setting register1
BLS_ATTLUT_REG	0x10+N*0x4	BLS attenuation LUT register, +N*0x4 (N = 0,1,2,3)
BLS_POS_REG	0x20	BLS blue zone position register
BLS_GAINLUT_REG	0x30+N*0x4	BLS GainLUT access register, +N*0x4, Total 16byte, 16*8bit (N = 0,1,2,3)

3.1.5 BLS register description

3.1.5.1 BLS_CTRL_REG (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: BLS_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	/	/	/
5	R/W	0x0	**OUTPUT_CSC_EN** 0: Disable 1: Enable
4	R/W	0x0	**INPUT_CSC_EN**

			0: Disable 1: Enable
3:2	/	/	/
1	R/W	0x0	**WIN_EN** Output window function enable 0: disable 1: enable
0	R/W	0x0	**EN** BLS Module enable 0: Disable 1: Enable

3.1.5.2 BLS_SIZE_REG (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: BLS_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	Reserved
27:16	R/W	0x0	**HEIGHT** The real height = The value of these bits add 1
15:12	/	/	/
11:0	R/W	0x0	**WIDTH** The real width = The value of these bits add 1

3.1.5.3 BLS_WIN0_REG (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: BLS_WIN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**WIN_TOP** Window Top position Top position is the left-top y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0	**WIN_LEFT** Window Left position Left position is left-top x coordinate of display window in pixels

3.1.5.4 BLS_WIN1_REG (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: BLS_WIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**WIN_BOT** Window Bottom position Bottom position is right-bottom y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0	**WIN_RIGHT**

			Window Right position Right position is right-bottom x coordinate of display window in pixels

3.1.5.5 BLS_ATTLUT_REG (Default Value: 0xFFFF_FFFF)

Offset: 0x0010+N*0x4(N = 0~3)			Register Name: BLS_ATTLUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0xF	**K7** The K_{ATTEN} value of Y>>5=N*8+7, if Y is 10bit
27:24	R/W	0xF	**K6** The K_{ATTEN} value of Y>>5=N*8+6
23:20	R/W	0xF	**K5** The K_{ATTEN} value of Y>>5=N*8+5
19:16	R/W	0xF	**K4** The K_{ATTEN} value of Y>>5=N*8+4
15:12	R/W	0xF	**K3** The K_{ATTEN} value of Y>>5=N*8+3
11:8	R/W	0xF	**K2** The K_{ATTEN} value of Y>>5=N*8+2
7:4	R/W	0xF	**K1** The K_{ATTEN} value of Y>>5=N*8+1
3:0	R/W	0xF	**K0** The K_{ATTEN} value of Y>>5=N*8

BLS_ATTLUT_REG + N*4, N=0~3

ATTLUT size is 32*4bits, and implemented as register. Updated when VSYNC occur.

3.1.5.6 BLS_POS_REG (Default Value: 0x0056_0076)

Offset: 0x0020			Register Name: BLS_POS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x56	**V_OFFSET** Blue zone offset of V, default 86
15:8	/	/	/
7:0	R/W	0x76	**U_OFFSET** Blue zone offset of U, default 118

3.1.5.7 BLS_GAINLUT_REG (Default Value: 0x0000_0000)

Offset: 0x0030+N*0x4(N = 0~3)			Register Name: BLS_GAINLUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	GAIN**3** The value of GAIN_LUT(N*4+3)
23:16	R/W	0x0	GAIN**2** The value of GAIN_LUT(N*4+2)
15:8	R/W	0x0	GAIN**1**

			The value of GAIN_LUT(N*4+1)
7:0	R/W	0x0	GAIN**0** The value of GAIN_LUT(N*4)

BLS_GAIN_LUT + N*4, N=0~3

GAIN_LUT size is 16*7bits, and implemented as register. Updated when VSYNC occur.

3.2 DE CDC Specification

3.2.1 Overview

The Color space and Dynamic range conversion (CDC) is a DE module which provides color space conversion between BT2020/BT709, and dynamic range conversion between SDR/ST2084/HLG.

Feature:

- Interface: 10bit per channel in both input and output
- Support 17×17×17 3D-LUT
- Support input and output color space conversion

Configuration in H6 system:

Table 3-1. CDC Configuration in H6 system

Configuration parameter	Descriptions	CDC in VEP of RTD0	CDC in Channel1 of RTD0
SUPPORT_INPUT_CSC	Support input CSC	YES	NO
SUPPORT_INPUT_CSC	Support output CSC	YES	NO

3.2.2 CDC Block Diagram

The CDC comprises with:
Input and ouput color space conversion: The modules convert color space between RGB and YCbCr.
3D-LUT: The module provides color space conversion and dynamic range conversion.
Register: The controller for AHB accessing.

Figure 3-2 shows a block diagram of the CDC.

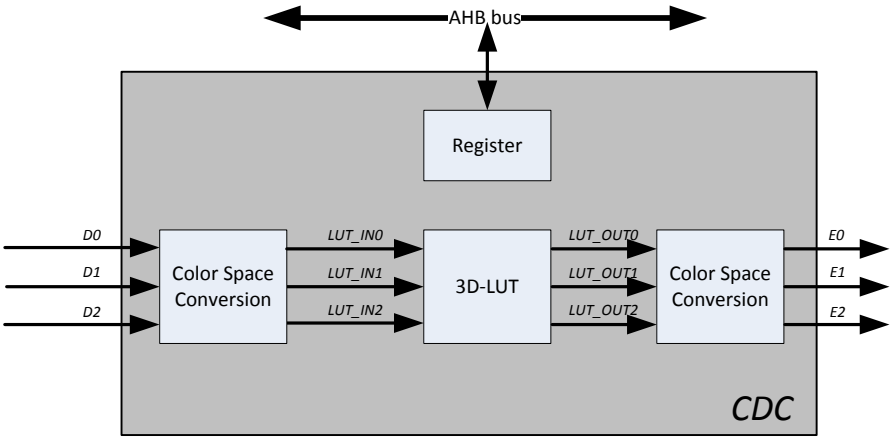


Figure 3-2. CDC Block Diagram

3.2.3 CDC Register List

Module Name	Base Address
CDC	0x011d0000

Register Name	Offset	Description
CDC_CTRL_REG	0x0000	CDC Module Control Register
CDC_UPDATE_REG	0x0004	CDC Update Register
INCSC_D0_REG	0x0014	Input CSC Constant D0 Register
INCSC_D1_REG	0x0018	Input CSC Constant D1 Register
INCSC_D2_REG	0x001C	Input CSC Constant D2 Register
INCSC_C00_REG	0x0020	Input CSC Coefficient 00 Register
INCSC_C01_REG	0x0024	Input CSC Coefficient 01 Register
INCSC_C02_REG	0x0028	Input CSC Coefficient 02 Register
INCSC_C03_REG	0x002C	Input CSC Constant 03 Register
INCSC_C10_REG	0x0030	Input CSC Coefficient 10 Register
INCSC_C11_REG	0x0034	Input CSC Coefficient 11 Register
INCSC_C12_REG	0x0038	Input CSC Coefficient 12 Register
INCSC_C13_REG	0x003C	Input CSC Constant 13 Register
INCSC_C20_REG	0x0040	Input CSC Coefficient 20 Register
INCSC_C21_REG	0x0044	Input CSC Coefficient 21 Register
INCSC_C22_REG	0x0048	Input CSC Coefficient 22 Register
INCSC_C23_REG	0x004C	Input CSC Constant 23 Register
OUTCSC_D0_REG	0x0054	Output CSC Constant D0 Register
OUTCSC_D1_REG	0x0058	Output CSC Constant D1 Register
OUTCSC_D2_REG	0x005C	Output CSC Constant D2 Register
OUTCSC_C00_REG	0x0060	Output CSC Coefficient 00 Register
OUTCSC_C01_REG	0x0064	Output CSC Coefficient 01 Register
OUTCSC_C02_REG	0x0068	Output CSC Coefficient 02 Register
OUTCSC_C03_REG	0x006C	Output CSC Constant 03 Register
OUTCSC_C10_REG	0x0070	Output CSC Coefficient 10 Register
OUTCSC_C11_REG	0x0074	Output CSC Coefficient 11 Register
OUTCSC_C12_REG	0x0078	Output CSC Coefficient 12 Register
OUTCSC_C13_REG	0x007C	Output CSC Constant 13 Register
OUTCSC_C20_REG	0x0080	Output CSC Coefficient 20 Register
OUTCSC_C21_REG	0x0084	Output CSC Coefficient 21 Register
OUTCSC_C22_REG	0x0088	Output CSC Coefficient 22 Register
OUTCSC_C23_REG	0x008C	Output CSC Constant 23 Register
LUT0_COEF_REG	0x1000 + N*4	LUT0 Coefficient Register N
LUT1_COEF_REG	0x1C00 + N*4	LUT1 Coefficient Register N
LUT2_COEF_REG	0x2800 + N*4	LUT2 Coefficient Register N
LUT3_COEF_REG	0x3400 + N*4	LUT3 Coefficient Register N
LUT4_COEF_REG	0x4000 + N*4	LUT4 Coefficient Register N
LUT5_COEF_REG	0x4C00 + N*4	LUT5 Coefficient Register N
LUT6_COEF_REG	0x5800 + N*4	LUT6 Coefficient Register N
LUT7_COEF_REG	0x6400 + N*4	LUT7 Coefficient Register N

Note: All registers are double-buffered, except COEF_SWITCH_EN

3.2.4 CDC Register Description

3.2.4.1 CDC Module Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CDC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EN Module function enable 1: Disable 1: Enable Note: When set this bit to zero, the clock of CDC module will be closed.

3.2.4.2 CDC Update Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: CDC_UPDATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	COEF_SWITCH_EN Coefficients RAM switch 0: DONOT switch 1: Switch RAM use REG_RDY **Note:** **1. When LCD SYNC go low and COEF_SWITCH_EN is 1, coefficient RAM will switch to the latest updated RAM if REG_RDY is 1, and then the bit will also be self-cleared if switch action successes.** 2. **This bit can set to 1 or 0 by AHB before LCD SYNC comes.**

3.2.4.3 Input CSC constant D0 register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: INCSC_D0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	D0 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.4 Input CSC constant D1 register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: INCSC_D1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	D1 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.5 Input CSC constant D2 register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: INCSC_D2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	D2 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.6 Input CSC coefficient 00 register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: INCSC_C00_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C00 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.7 Input CSC coefficient 01 register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: INCSC_C01_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C01 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.8 Input CSC coefficient 02 register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: INCSC_C02_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C02 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.9 Input CSC constant 03 register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: INCSC_C03_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C03 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.10 Input CSC coefficient 10 register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: INCSC_C10_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C10 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.11 Input CSC coefficient 11 register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: INCSC_C11_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C11 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.12 Input CSC coefficient 12 register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: INCSC_C12_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C12 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.13 Input CSC constant 13 register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: INCSC_C13_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C13 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.14 Input CSC coefficient 20 register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: INCSC_C20_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C20 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.15 Input CSC coefficient 21 register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: INCSC_C21_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C21 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.16 Input CSC coefficient 22 register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: INCSC_C22_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C22 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.17 Input CSC constant 23 register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: INCSC_C23_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C23 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.18 Output CSC constant D0 register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: OUTCSC_D0_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	D0 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.19 Output CSC constant D1 register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: OUTCSC_D1_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	D1 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.20 Output CSC constant D2 register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: OUTCSC_D2_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	D2 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.21 Output CSC coefficient 00 register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: OUTCSC_C00_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C00 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.22 Output CSC coefficient 01 register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: OUTCSC_C01_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C01 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.23 Output CSC coefficient 02 register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: OUTCSC_C02_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C02 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.24 Output CSC constant 03 register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: OUTCSC_C03_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C03 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.25 Output CSC coefficient 10 register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: OUTCSC_C10_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C10 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.26 Output CSC coefficient 11 register (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: OUTCSC_C11_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C11 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.27 Output CSC coefficient 12 register (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: OUTCSC_C12_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C12 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.28 Output CSC constant 13 register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: OUTCSC_C13_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C13 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.29 Output CSC coefficient 20 register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: OUTCSC_C20_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C20 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.30 Output CSC coefficient 21 register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: OUTCSC_C21_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C21 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.31 Output CSC coefficient 22 register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: OUTCSC_C22_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C22 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.2.4.32 Output CSC constant 23 register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: OUTCSC_C23_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C23 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.2.4.33 LUT0 coefficient register N (N=0:728)

Offset: 0x1000 + N*4			Register Name: LUT0_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.34 LUT1 coefficient register N (N=0:647)

Offset: 0x1C00 + N*4			Register Name: LUT1_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.35 LUT2 coefficient register N (N=0:647)

Offset: 0x2800 + N*4			Register Name: LUT2_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.36 LUT3 coefficient register N (N=0:575)

Offset: 0x3400 + N*4			Register Name: LUT3_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.37 LUT4 coefficient register N (N=0:647)

Offset: 0x4000 + N*4			Register Name: LUT4_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.38 LUT5 coefficient register N (N=0:575)

Offset: 0x4C00 + N*4			Register Name: LUT5_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.39 LUT6 coefficient register N (N=0:575)

Offset: 0x5800 + N*4			Register Name: LUT6_COEF_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.2.4.40 LUT7 coefficient register N (N=0:511)

Offset: 0x6400 + N*4			Register Name: LUT7_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:0	R/W	UDF	COEF Value of R component = COEF[29:20]; value of G component = COEF[19:10]; value of B component = COEF[9:0].

3.3 DE DNS Specification

3.3.1 Overview

The Denoise(DNS) is a compression artifacts eliminating module.

Feature:

- Adaptive denoising with Image Quality Assessment and Block detector function
- Deblock
- Suppress sawtooth edge
- Denoising strength variable
- Support for yuv420/422 input(not support yuv422 interleave format), size of 16*16~4096*N
- Eliminating for luma

3.3.2 DNS Block Diagram

The DNS comprises with: Edge detection, PCA, Adaptive filter.

Edge detection calculates the edge strength for each pixel, and counter for strength histogram.

PCA calculates the edge direction for a 5x5 window.

Adaptive filter decide the filter parameter for this window according to the edge direction strength.

Figure3-3 shows a block diagram of the DNS.

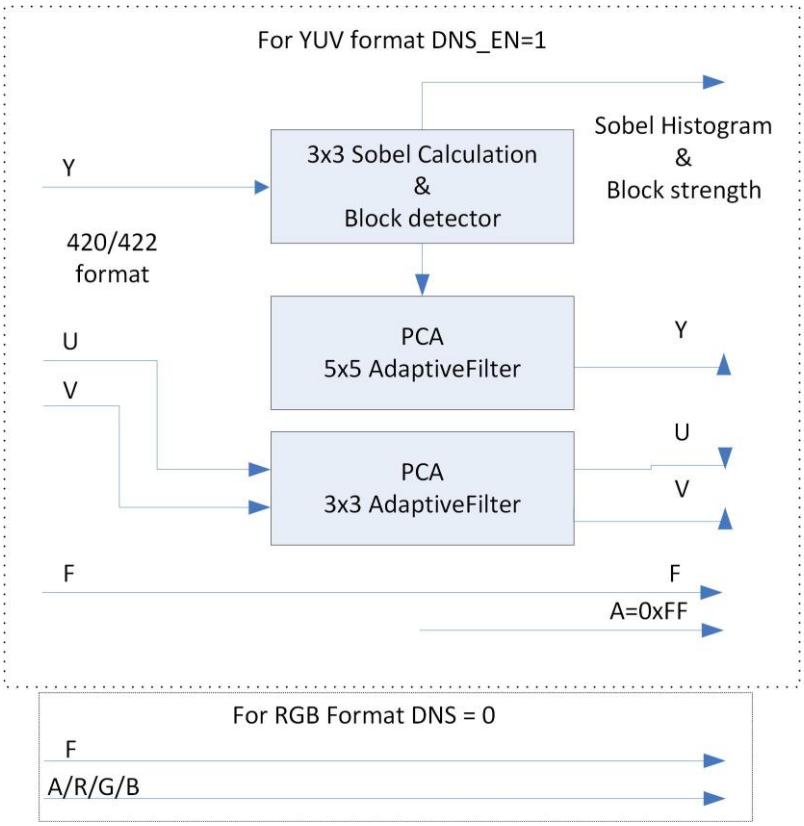


Figure 3-3. DNS Block Diagram

3.3.3 DNS Register List

Module Name	Base Address
DNS	0x01180000

Register Name	Offset	Description
DNS_CTL	0x00	DNS module control register
DNS_SIZE	0x04	DNS size register
DNS_WIN0	0x08	DNS ROI window0 setting register
DNS_WIN1	0x0C	DNS ROI window1 setting register
DNS_LFT_PARA0	0x10	DNS LumFilter Parameter0 Register
DNS_LFT_PARA1	0x14	DNS LumFilter Parameter1 Register
DNS_LFT_PARA2	0x18	DNS LumFilter Parameter2 Register
DNS_LFT_PARA3	0x1C	DNS LumFilter Parameter3 Register
	0x20~0xFC	Reserved
IQA_CTL	0x100	IQA Control Register
IQA_SUM	0x104	IQA Sum Register
IQA_STA0	0x108	IQA Statistic0 Register
IQA_STA1	0x10C	IQA Statistic1 Register
IQA_STA2	0x110	IQA Statistic2 Register
IQA_STA3	0x114	IQA Statistic3 Register
IQA_STA4	0x118	IQA Statistic4 Register
IQA_STA5	0x11C	IQA Statistic5 Register
IQA_STA6	0x120	IQA Statistic6 Register
IQA_STA7	0x124	IQA Statistic7 Register
IQA_STA8	0x128	IQA Statistic8 Register
IQA_STA9	0x12C	IQA Statistic9 Register
IQA_STA10	0x130	IQA Statistic10 Register
IQA_STA11	0x134	IQA Statistic11 Register
IQA_STA12	0x138	IQA Statistic12 Register
IQA_BLKDT_PARA0	0x13C	IQA Block Detector Para0 Register
IQA_BLKDT_SUM	0x140	IQA Block Detector Sum Register
IQA_BLKDT_NUM	0x144	IQA Block Detector Number Register

3.3.4 DNS Register Description

3.3.4.1 DNS Module Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DNS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	**WIN_EN** ROI(Region of interest) window function enable, bypass the pixel outside the window defined by **DNS_WIN0 & DNS_WIN1, sobel histogram function counter for every pixel and not related to this window.** 0: disable

			1: enable
30:2	/	/	/
1	R/W	0x0	**WINSZ_SEL** DNS luma filter size select 0: Normal 5x5 1: Small 3x3 When **WINSZ_SEL**==1, block effect detect function is disable
0	R/W	0x0	**EN** DNS Module luma denoise function enable 0: Disable 1: Enable

3.3.4.2 DNS Size Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DNS_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**HEIGHT** The real height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** The real width = The value of these bits add 1

3.3.4.3 DNS ROI Window0 Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: DNS_WIN0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**WIN_TOP** Window Top position Top position is the left-top y coordinate of display window in pixels
15:13	/	/	/
12:0	R/W	0x0	**WIN_LEFT** Window Left position Left position is left-top x coordinate of display window in pixels

3.3.4.4 DNS ROI Window1 Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: DNS_WIN1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**WIN_BOT** Window Bottom position Bottom position is right-bottom y coordinate of display window in pixels
15:13	/	/	/
12:0	R/W	0x0	**WIN_RIGHT**

			Window Right position Right position is right-bottom x coordinate of display window in pixels

3.3.4.5 DNS LumFilter Parameter0 Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DNS_LFT_PARA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LDIR_RSIG_GAIN2** DNS edge range sigma gain2 0~255 for luma
23:16	R/W	0x0	**LSIG3** DNS luma filter sig3 parameter 0~255
15:8	R/W	0x0	**LSIG2** DNS luma filter sig2 parameter 0~255
7:3	/	/	/
2:0	R/W	0x0	**LSIG** DNS luma filter sig parameter 0~7

3.3.4.6 DNS LumFilter Parameter1 Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: DNS_LFT_PARA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LDIR_THRHIGH** DNS edge high threshold for luma
23:16	R/W	0x0	**LDIR_THRLOW** DNS edge low threshold for luma
15:8	R/W	0x0	**LDIR_RSIG_GAIN** DNS edge range sigma gain 0~255 for luma
7:0	R/W	0x0	**LDIR_CEN** DNS edge center 0~255 for luma

3.3.4.7 DNS LumFilter Parameter2 Register(Default Value: 0x7700_0000)

Offset: 0x0018			Register Name: DNS_LFT_PARA2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x7	**LBH** Block height=LBH+1, normally 7
27:24	R/W	0x7	**LBW** Block width=LBW+1, normally 7
23:20	R/W	0x0	**LBXST** Block x start offset
19:16	R/W	0x0	**LBYST** Block y start offset
15:8	R/W	0x0	**LBGAIN** Block gain
7:1	/	/	**/**
0	R/W	0x0	**LBBEN**

			Block boundary setting enable 0: disable 1: enable

3.3.4.8 DNS LumFilter Parameter3 Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DNS_LFT_PARA3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**LSIG_CEN** DNS luma filter sig parameter for dir center 0~255

3.3.4.9 IQA Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: IQA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R	0x0	**MAX** Max edge value detected in one frame.
15:1	/	/	/
0	R/W	0x0	**/**

3.3.4.10 IQA Sum Register(Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IQA_SUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**SUM** Sum of the edge statistic.

3.3.4.11 IQA Statistic0 Register(Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IQA_STA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA0** Hist of the sob lv0.

3.3.4.12 IQA Statistic1 Register(Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: IQA_STA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA1** Hist of the sob lv1.

3.3.4.13 IQA Statistic2 Register(Default Value: 0x0000_0000)

Offset: 0x0110	Register Name: IQA_STA2

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	**STA2** Hist of the sob lv2.

3.3.4.14 IQA Statistic3 Register(Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IQA_STA3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA3** Hist of the sob lv3.

3.3.4.15 IQA Statistic4 Register(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IQA_STA4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA4** Hist of the sob lv4.

3.3.4.16 IQA Statistic5 Register(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IQA_STA5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA5** Hist of the sob lv5.

3.3.4.17 IQA Statistic6 Register(Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IQA_STA6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA6** Hist of the sob lv6.

3.3.4.18 IQA Statistic7 Register(Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IQA_STA7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA7** Hist of the sob lv7.

3.3.4.19 IQA Statistic8 Register(Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IQA_STA8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**STA8** Hist of the sob lv8.

3.3.4.20 IQA Statistic9 Register(Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: IQA_STA9
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	**STA9** Hist of the sob lv9.

3.3.4.21 IQA Statistic10 Register(Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IQA_STA10
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	**STA10** Hist of the sob lv10.

3.3.4.22 IQA Statistic11 Register(Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IQA_STA11
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	**STA11** Hist of the sob lv11.

3.3.4.23 IQA Statistic12 Register(Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: IQA_STA12
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	**STA12** Hist of the sob lv12.

3.3.4.24 IQA Block Detector Para0 Register(Default Value: 0x0000_c810)

Offset: 0x013C			Register Name: IQA_BLKDT_PARA0
Bit	Read/Write	Default/Hex	Description
31:16	/	/	**/**
15:8	R/W	0xc8	**DT_THRHIGH** Block detector threshold high.
7:0	R/W	0x10	**DT_THRLOW** Block detector threshold low.

3.3.4.25 IQA Block Detector Sum Register(Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: IQA_BLKDT_SUM
Bit	Read/Write	Default/Hex	Description
31:27	/	/	**/**
26:0	R	0x0	**DT_BLKSUM** Block detected sum.

Block detect function only work in 5x5 mode

3.3.4.26 IQA Block Detector Block Number Register(Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: IQA_BLKDT_NUM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R	0x0	**DT_BLKNUM** Block detected number.

3.4 DE DRC Specification

3.4.1 Overview

The dynamic range controller (DRC) is a post-processing module which adjusts the image mapping curve according to the histogram frame by frame. The control function can be defined by the software driver according to the application. A typical application is Content-based backlight control.

Feature:

- Support data format with 8-bit per channel
- Support 2048*2048 input/output
- Support HISTOGRAM and DRC in HSV color space

3.4.2 DRC Block Diagram

Figure 3-4 show the data flow of DRC module. It contains some parts list followed:

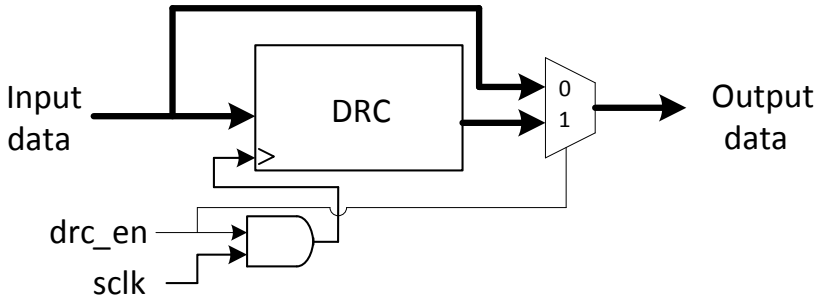


Figure 3-4. DRC Block Diagram

3.4.3 Register List

Module Name	Base Address
DRC	0x011A0000

Register Name	Offset	Description
GNECTL_REG	0x0000	Module general control register
DRC_SIZE_REG	0x0004	DRC size setting register
DRC_CTL_REG	0x0010	DRC control register
DRC_SET_REG	0x0018	DRC setting register
DRC_WP0_REG	0x001C	DRC window position register0
DRC_WP1_REG	0x0020	DRC window position register1
LH_CTL_REG	0x0030	Luminance histogram control register
LH_THR0_REG	0x0034	Luminance histogram threshold setting register0
LH_THR1_REG	0x0038	Luminance histogram threshold setting register1

LH_SLUMN_REG	0x0040 + N*4(N=0 ~ 7)	Luminance histogram statistics luminance recording register
LH_SCNTN_REG	0x0060 + N*4(N=0 ~ 7)	Luminance histogram statistics counter recording register
CSC_C00_REG	0x00C0	CSC coefficient 00 register
CSC_C01_REG	0x00C4	CSC coefficient 01 register
CSC_C02_REG	0x00C8	CSC coefficient 02 register
CSC_C03_REG	0x00CC	CSC constant 03 register
CSC_C10_REG	0x00D0	CSC coefficient 10 register
CSC_C11_REG	0x00D4	CSC coefficient 11 register
CSC_C12_REG	0x00D8	CSC coefficient 12 register
CSC_C13_REG	0x00DC	CSC constant 13 register
CSC_C20_REG	0x00E0	CSC coefficient 20 register
CSC_C21_REG	0x00E4	CSC coefficient 21 register
CSC_C22_REG	0x00E8	CSC coefficient 22 register
CSC_C23_REG	0x00EC	CSC constant 23 register
DRC_SPACOFF_REGN	0x0F0 + N*4(N=0,1,2)	DRC spatial coefficient registers
DRC_INTCOFF_REGN	0x100 + N*4(N=0 ~ 63)	DRC intensity coefficient registers
DRC_LGCOFF_REGN	0x200 + N*4(N=0 ~ 127)	DRC Luminance gain coefficient registers

3.4.4 Register Description

3.4.4.1 General control register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: GNECTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	BIST_EN BIST enable 0x0: disable 0x1: enable
30:10	/	/	/
09:08	R/W	0x0	MOD Work mode selection. If bit 0 of the register is set ZERO, the following setting will be ignored. 0x0: reserved 0x1: reserved 0x2: DRC mode 0x3: reserved
07:05	/	/	/
04	R/W	0x0	COEF_SWITCH_EN 0x0: DONOT switch 0x1: Switch RAM use external RDY_EN Note: When LCD SYNC negative edge comes and COEF_SWITCH_EN is 1, DRC_LGCOFF_REGN will switch to the latest updated RAM if external RDY_EN equal to 1, and then the bit will also be self-cleared if switch action successes.

03:02	/	/	/
01	R/W	0x0	Reserved Note: Must set to 0.
00	R/W	0x0	DRC_EN DRC module enable 0x0: disabled 0x1: enable **Note: When module disable, the input data will be bypassed to output, and the clock of calculation circuit will be gated automatically.**

3.4.4.2 DRC size setting register (Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: DRC_SIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	DRC_HEIGHT Display height The real display height = The value of these bits + 1. Note: Must set to 7~2047 when module enable.
15:13	/	/	/
12:00	R/W	0x0	DRC_WIDTH Display width The real display width = The value of these bits + 1.

3.4.4.3 DRC control register (Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: DRC_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
09	R/W	0x0	HSV_MODE_EN Enable Using component V calculated from three source components to process Luma Histogram and DRC. 0x0: disable 0x1: enable **Note: Must set to 1.**
08	R/W	0x0	DRC_WIN_EN Output window function enable 0x0: disable 0x1: enable
07:01	/	/	/
00	R/W	0x0	DRC_DB_EN DRC double buffer function enable control 0x0: disable 0x1: enable

3.4.4.4 DRC setting register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: DRC_SET_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	DRC_LGC_ABSLUMPERVAL Abs luminance percent value
7:2	/	/	/
1	R/W	0x0	DRC_ADJUST_EN DRC adjust enable 0x0: disable 0x1: enable
0	R/W	0x0	DRC_LGC_ABSLUMSHF Abs luminance shift bits 0x0: shift 8bits 0x1: shift 9bits

3.4.4.5 DRC window position 0 register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DRC_WP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	DRC_WIN_TOP Window Top position Top position is the left-top y coordinate of display window in pixels.
15:12	/	/	/
11:00	R/W	0x0	DRC_WIN_LEFT Window Left position Left position is left-top x coordinate of display window in pixels.

3.4.4.6 DRC window position 1 register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: DRC_WP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	DRC_WIN_BOT Window Bottom position Bottom position is the right-bottom y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0x0	DRC_WIN_RIGHT Window Right position Right position is the right-bottom x coordinate of display window in pixels

3.4.4.7 Luminance histogram control register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: LH_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	LH_MOD 0: Current frame case 1: Average case
0	R/W	0x0	LH_REC_CLR If the bit is set, the all of the luminance statistics recording registers will be clear, and the bit will self-clear when the recording registers is clear done.

3.4.4.8 Luminance histogram threshold setting 0 register (Default Value: 0x8060_4020)

Offset: 0x0034			Register Name: LH_THR0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x80	LH_THRES_VAL4 Step4 threshold value
23:16	R/W	0x60	LH_THRES_VAL3 Step3 threshold value
15:08	R/W	0x40	LH_THRES_VAL2 Step2 threshold value
07:00	R/W	0x20	LH_THRES_VAL1 Step1 threshold value

3.4.4.9 Luminance histogram threshold setting 1 register (Default Value: 0x00E0_C0A0)

Offset: 0x0038			Register Name: LH_THR1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xE0	LH_THRES_VAL7 Step7 threshold value
15:08	R/W	0xC0	LH_THRES_VAL6 Step6 threshold value
07:00	R/W	0xA0	LH_THRES_VAL5 Step5 threshold value

Note: When setting LHT_REG0 and LHT_REG1, make sure that THRES_VAL1<THRES_VAL2<…<THRES_VAL7.

3.4.4.10 Luminance histogram statistics lum recording register N (N = 0~7) (Default Value: 0x0000_0000)

Offset: 0x0040 + N*4			Register Name: LH_SLUM_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0x0	LH_LUM_DATA Luminance statistics data

3.4.4.11 Luminance histogram statistics counter recording register N (N = 0~7) (Default Value: 0x0000_0000)

Offset: 0x0060 + N*4			Register Name: LH_SCNT_REGN
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:00	R/W	0x0	LH_CNT_DATA Luminance statistics data

3.4.4.12 CSC coefficient 00 register (Default Value: 0x0000_04A7)

Offset: 0x00C0			Register Name: CSC_C00_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x04A7	C00 Note: must set to 0x0400.

3.4.4.13 CSC coefficient 01 register (Default Value: 0x0000_1E6F)

Offset: 0x00C4			Register Name: CSC_C01_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x1E6F	C01 Note: must set to 0x0000.

3.4.4.14 CSC coefficient 02 register (Default Value: 0x0000_1CBF)

Offset: 0x00C8			Register Name: CSC_C02_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x1CBF	C02 Note: must set to 0x0000.

3.4.4.15 CSC constant 03 register (Default Value: 0x0000_0877)

Offset: 0x00CC			Register Name: CSC_C03_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0877	C03 Note: must set to 0x0000.

3.4.4.16 CSC coefficient 10 register (Default Value: 0x0000_04A7)

Offset: 0x00D0			Register Name: CSC_C10_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

12:0	R/W	0x04A7	C10 Note: must set to 0x0000.

3.4.4.17 CSC coefficient 11 register (Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: CSC_C11_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0000	C11 Note: must set to 0x0400.

3.4.4.18 CSC coefficient 12 register (Default Value: 0x0000_0662)

Offset: 0x00D8			Register Name: CSC_C12_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0662	C12 Note: must set to 0x0000.

3.4.4.19 CSC constant 13 register (Default Value: 0x0000_3211)

Offset: 0x00DC			Register Name: CSC_C13_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x3211	C13 Note: must set to 0x0000.

3.4.4.20 CSC coefficient 20 register (Default Value: 0x0000_04A7)

Offset: 0x00E0			Register Name: CSC_C20_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x04A7	C20 **Note: must set to 0x0000.**

3.4.4.21 CSC coefficient 21 register (Default Value: 0x0000_0812)

Offset: 0x00E4			Register Name: CSC_C21_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0812	C21 **Note: must set to 0x0000.**

3.4.4.22 CSC coefficient 22 register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: CSC_C22_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0000	C22 **Note: must set to 0x0400.**

3.4.4.23 CSC constant 23 register (Default Value: 0x0000_2EB1)

Offset: 0x00EC			Register Name: CSC_C23_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x2EB1	C23 **Note: must set to 0x0000.**

3.4.4.24 DRC spatial coefficient register N (N=0~2) (Default Value: 0x0000_0000)

Offset: 0x00F0 + N*4			Register Name: DRC_SPACOFF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	SPA_COEF2 8 bits unsigned spatial coefficient data
15:08	R/W	0x0	SPA_COEF1 8 bits unsigned spatial coefficient data
07:00	R/W	0x0	SPA_COEF0 8 bits unsigned spatial coefficient data

3.4.4.25 DRC intensity coefficient register N (N=0~63) (Default Value: 0x0000_0000)

Offset: 0x0100 + N*4			Register Name: DRC_INTCOFF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	INT_COEF3 8 bits unsigned intensity coefficient data
23:16	R/W	0x0	INT_COEF2 8 bits unsigned intensity coefficient data
15:08	R/W	0x0	INT_COEF1 8 bits unsigned intensity coefficient data
07:00	R/W	0x0	INT_COEF0 8 bits unsigned intensity coefficient data

3.4.4.26 DRC luminance gain coefficient register N (N=0~127)

Offset: 0x0200 + N*4			Register Name: DRC_LGCOFF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	UDF	LGC_COEF1

			16bits luminance gain coefficient, unsigned data The high 5 bits is the integer part The low 11 bits is the decimal part
15:00	R/W	UDF	LGC_COEF0 16bits luminance gain coefficient, unsigned data The high 5 bits is the integer part The low 11 bits is the decimal part

Note: Double-buffered registers. When SYNC negative edge comes and COEF_SWITCH_EN is 1, coefficient RAM will switch to the latest updated RAM if external RDY_EN equal to 1.

3.5 DE FCC Specification

3.5.1 Overview

Fancy color curvature (FCC) is to adjust fancy colors so that a better vivid vision effect can be achieved. The FCC has the following features

Feature:

- Support window clipping up to 4096x4096 pixels
- Support local adjustment for hue/ saturation in HSV space
- Support red/green/blue/cyan/magenta/yellow areas modifying in adjustment mode

3.5.2 Register List

Module Name	Offset Address
FCC	0x00072000

Register Name	Offset	Description
FCC_CTL_REG	0x000	FCC Control Register
FCC_INPUT_SIZE_REG	0x004	FCC Input Size Register
FCC_OUTPUT_WIN0_REG	0x008	FCC Output Window0 Register
FCC_OUTPUT_WIN1_REG	0x00c	FCC Output Window1 Register
FCC_HUE_RANGE_REG	0x010 + N*0x4(N=0~5)	FCC Hue Range Register
/	0x028~0x02c	reserved
FCC_HUE_GAIN_REG	0x030 + N*0x4(N=0~5)	FCC Hue Range Register
FCC_SAT_GAIN_REG	0x048	FCC Hue Gain Register
FCC_COLOR_GAIN_REG	0x04c	FCC Color Gain Register
FCC_LUT_CTL_REG	0x050	FCC LUT Control Register
FCC_LIGHT_CTL_REG	0x054	FCC Light Control Register
/	0x058~0x05c	reserved
FCC_CSC0_COEFF00_REG	0x060	FCC CSC0 COEFF00 Register
FCC_CSC0_COEFF01_REG	0x064	FCC CSC0 COEFF01 Register
FCC_CSC0_COEFF02_REG	0x068	FCC CSC0 COEFF02 Register
FCC_CSC0_CONST0_REG	0x06c	FCC CSC0 CONST0 Register
FCC_CSC0_COEFF10_REG	0x070	FCC CSC0 COEFF10 Register
FCC_CSC0_COEFF11_REG	0x074	FCC CSC0 COEFF11 Register
FCC_CSC0_COEFF12_REG	0x078	FCC CSC0 COEFF12 Register
FCC_CSC0_CONST1_REG	0x07c	FCC CSC0 CONST1 Register
FCC_CSC0_COEFF20_REG	0x080	FCC CSC0 COEFF20 Register
FCC_CSC0_COEFF21_REG	0x084	FCC CSC0 COEFF21 Register
FCC_CSC0_COEFF22_REG	0x088	FCC CSC0 COEFF22 Register
FCC_CSC0_CONST2_REG	0x08c	FCC CSC0 CONST2 Register
FCC_CSC0_DIFF0_REG	0x090	FCC CSC0 DIFF0 Register

FCC_CSC0_DIFF0_REG	0x094	FCC CSC0 DIFF0 Register
FCC_CSC0_DIFF0_REG	0x098	FCC CSC0 DIFF0 Register
/	0x09c	/
FCC_CSC1_COEFF00_REG	0x0a0	FCC CSC1 COEFF00 Register
FCC_CSC1_COEFF01_REG	0x0a4	FCC CSC1 COEFF01 Register
FCC_CSC1_COEFF02_REG	0x0a8	FCC CSC1 COEFF02 Register
FCC_CSC1_CONST0_REG	0x0ac	FCC CSC1 CONST0 Register
FCC_CSC1_COEFF10_REG	0x0b0	FCC CSC1 COEFF10 Register
FCC_CSC1_COEFF11_REG	0x0b4	FCC CSC1 COEFF11 Register
FCC_CSC1_COEFF12_REG	0x0b8	FCC CSC1 COEFF12 Register
FCC_CSC1_CONST1_REG	0x0bc	FCC CSC1 CONST1 Register
FCC_CSC1_COEFF20_REG	0x0c0	FCC CSC1 COEFF20 Register
FCC_CSC1_COEFF21_REG	0x0c4	FCC CSC1 COEFF21 Register
FCC_CSC1_COEFF22_REG	0x0c8	FCC CSC1 COEFF22 Register
FCC_CSC1_CONST2_REG	0x0cc	FCC CSC1 CONST2 Register
FCC_CSC1_DIFF0_REG	0x0d0	FCC CSC1 DIFF0 Register
FCC_CSC1_DIFF0_REG	0x0d4	FCC CSC1 DIFF0 Register
FCC_CSC1_DIFF0_REG	0x0d8	FCC CSC1 DIFF0 Register
/	0x0dc~0x0fc	reserved
FCC_SAT_LUT_REG	0x100 + N*0x4(N=0~255)	FCC Saturation Gain Lookup Table Register

3.5.3 Register Description

3.5.3.1 FCC Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: FCC_CTL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**WIN_EN** Output window function enable 0: disable 1: enable
7	/	/	/
6	R/W	0x0	**Light_EN** Light protect enable 0: disable 1: enable
5	R/W	0x0	**Sat_EN** Saturate protect enable 0: disable 1: enable
4	R/W	0x0	**Skin_EN** Skin protect enable 0: disable 1: enable

3:1	/	/	/
0	R/W	0x0	**Enable** Enable control 0:disable 1:enable If the bit is disabled, the input data will by-pass to next module.

3.5.3.2 FCC Input Size Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: FCC_INPUT_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HEIGHT Processing height The real display height = The value of these bits + 1.
15:13	/	/	/
12:0	R/W	0x0	WIDTH Processing width The real display width = The value of these bits + 1.

3.5.3.3 FCC Output Window0 Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: FCC_OUTPUT_WIN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**WIN_TOP** Window Top position Top position is the left-top y coordinate of display window in pixels
15:13	/	/	/
12:0	R/W	0x0	**WIN_LEFT** Window Left position Left position is left-top x coordinate of display window in pixels

3.5.3.4 FCC Output Window1 Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: FCC_OUTPUT_WIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**WIN_BOT** Window Bottom position Bottom position is right-bottom y coordinate of display window in pixels
15:12	/	/	/
12:0	R/W	0x0	**WIN_RIGHT** Window Right position Right position is right-bottom x coordinate of display window in pixels

3.5.3.5 FCC Hue Range Register(Default Value: 0x0000_0000)

Offset: 0x0010+N*0x0004(N=0~5)			Register Name: FCC_HUE_RANGE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	HMAX the max value of hue
15:12	/	/	/
11:0	R/W	0x0	HMIN the min value of hue

3.5.3.6 FCC Hue Gain Register(Default Value: 0x0000_0000)

Offset: 0x0030+N*0x0004(N=0~5)			Register Name: FCC_HUE_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x0	HGAIN the local gain of hue(Hgain),this data represent the two's complement Range: -511~511
15:9	/	/	/
8:0	R/W	0x0	SGAIN the local gain of Saturation (Sgain),this data represent the two's complement. Range: -511~511

3.5.3.7 FCC Saturation Gain Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: FCC_SAT_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R/W	0x0	SGAIN the gain of Saturation (Sgain),this data represent the two's complement. Range: -511~511

3.5.3.8 FCC Color Gain Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: FCC_COLOR_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	SKR Range: 0~15
7:4	R/W	0x0	SKG Range: 0~15
3:0	R/W	0x0	SKB Range: 0~15

3.5.3.9 FCC LUT Control Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: FCC_LUT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	LUT_ACCESS_SWITCH 0: AHB access 1: Module access Note: When module access, LUT registers can't access through AHB bus. When AHB access, LUT will return the input address for data output.

3.5.3.10 FCC Light Control Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: FCC_LIGHT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x0	LIGHT_TH1 The light protect threshold Range: 0~512
15:9	/	/	/
8:0	R/W	0x0	LIGHT_TH0 The light protect threshold Range: 0~512

3.5.3.11 FCC CSC0 COEFF00 Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: FCC_CSC0_COEFF00_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C00 The value equals to coefficient*2^{17}

3.5.3.12 FCC CSC0 COEFF01 Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: FCC_CSC0_COEFF01_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C01 The value equals to coefficient*2^{17}

3.5.3.13 FCC CSC0 COEFF02 Register(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: FCC_CSC0_COEFF02_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/

19:0	R/W	0x0	C02 The value equals to coefficient*2^{17}

3.5.3.14 FCC CSC0 CONST0 Register(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: FCC_CSC0_CONST0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C03

3.5.3.15 FCC CSC0 COEFF10 Register(Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: FCC_CSC0_COEFF10_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C10 The value equals to coefficient*2^{17}

3.5.3.16 FCC CSC0 COEFF11 Register(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: FCC_CSC0_COEFF11_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C11 The value equals to coefficient*2^{17}

3.5.3.17 FCC CSC0 COEFF12 Register(Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: FCC_CSC0_COEFF12_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C12 The value equals to coefficient*2^{17}

3.5.3.18 FCC CSC0 CONST1 Register(Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: FCC_CSC0_CONST1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C13 the C13 represent the two’s complement

3.5.3.19 FCC CSC0 COEFF20 Register(Default Value: 0x0000_0000)

Offset: 0x0080	Register Name: FCC_CSC0_COEFF20_REG

Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C20 The value equals to coefficient*2^{17}

3.5.3.20 FCC CSC0 COEFF21 Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: FCC_CSC0_COEFF21_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C21 The value equals to coefficient*2^{17}

3.5.3.21 FCC CSC0 COEFF22 Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: FCC_CSC0_COEFF22_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C22 The value equals to coefficient*2^{17}

3.5.3.22 FCC CSC0 CONST2 Register(Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: FCC_CSC0_CONST2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C23 the C23 represent the two’s complement

3.5.3.23 FCC CSC0 DIFF0 Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: FCC_CSC0_DIFF0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C30

3.5.3.24 FCC CSC0 DIFF1 Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: FCC_CSC0_DIFF1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C31

3.5.3.25 FCC CSC0 DIFF2 Register(Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: FCC_CSC0_DIFF2_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C32

3.5.3.26 FCC CSC1 COEFF00 Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: FCC_CSC1_COEFF00_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C00 The value equals to coefficient*2^{17}

3.5.3.27 FCC CSC1 COEFF01 Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: FCC_CSC1_COEFF01_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C01 The value equals to coefficient*2^{17}

3.5.3.28 FCC CSC1 COEFF02 Register(Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: FCC_CSC1_COEFF02_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C02 The value equals to coefficient*2^{17}

3.5.3.29 FCC CSC1 CONST0 Register(Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: FCC_CSC1_CONST0_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C03

3.5.3.30 FCC CSC1 COEFF10 Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: FCC_CSC1_COEFF10_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C10 The value equals to coefficient*2^{17}

3.5.3.31 FCC CSC1 COEFF11 Register(Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: FCC_CSC1_COEFF11_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C11 The value equals to coefficient*2^{17}

3.5.3.32 FCC CSC1 COEFF12 Register(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: FCC_CSC1_COEFF12_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C12 The value equals to coefficient*2^{17}

3.5.3.33 FCC CSC1 CONST1 Register(Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: FCC_CSC1_CONST1_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:0	R/W	0x0	C13 the C13 represent the two's complement

3.5.3.34 FCC CSC1 COEFF20 Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: FCC_CSC1_COEFF20_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C20 The value equals to coefficient*2^{17}

3.5.3.35 FCC CSC1 COEFF21 Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: FCC_CSC1_COEFF21_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C21 The value equals to coefficient*2^{17}

3.5.3.36 FCC CSC1 COEFF22 Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: FCC_CSC1_COEFF22_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	C22

			The value equals to coefficient*2^{17}

3.5.3.37 FCC CSC1 CONST2 Register(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: FCC_CSC1_CONST2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C23 the C23 represent the two's complement

3.5.3.38 FCC CSC1 DIFF0 Register(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: FCC_CSC1_DIFF0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C30

3.5.3.39 FCC CSC1 DIFF1 Register(Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: FCC_CSC1_DIFF1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C31

3.5.3.40 FCC CSC1 DIFF2 Register(Default Value: 0x0000_0000)

Offset: 0x00D8			Register Name: FCC_CSC1_DIFF2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C32

3.5.3.41 FCC Saturation Gain Lookup Table Register(Default Value: 0x0000_0000)

Offset: 0x0100+N*0x04(N=0~255)			Register Name: FCC_SAT_LUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	UDF	LUT1 (N*2+1) level LUT
15:10	/	/	/
9:0	R/W	UDF	LUT0 (N*2) level LUT

Note: This register is not double buffer.

3.6 DE FCE Specification

3.6.1 Overview

The Fresh and Contrast Enhancement (FCE) is a post-processing module which includes contrast enhancement, fresh tone detection and correction.

Feature:

- Support data format with 10-bit per channel
- Support maximum input frame size 4096×2160

3.6.2 FCE Block Diagram

Figure 3-5 show the data flow of FCE module. It contains some parts list followed:

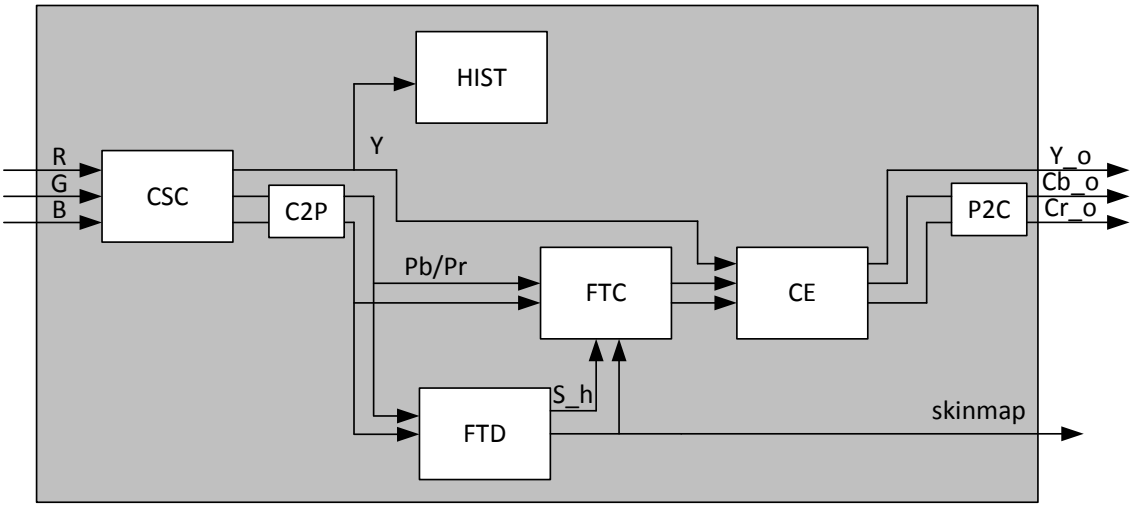


Figure 3-5. FCE data flow

3.6.3 Register List

Module Name	Offset Address
FCE	0x01170000

Register Name	Offset	Description
GCTRL_REG	0x000	Control register
FCE_SIZE_REG	0x004	Size setting register
FCE_WIN0_REG	0x008	Window setting 0 register
FCE_WIN1_REG	0x00C	Window setting 1 register
HIST_SUM_REG	0x020	Histogram sum register
HIST_STATUS_REG	0x024	Histogram status register

CE_STATUS_REG	0x028	CE LUT status register
CE_CC_REG	0x02C	CE chroma compensation function setting register
FTC_GAIN_REG	0x030	FTC gain setting register
FTD_HUE_THR_REG	0x034	FTD hue threshold setting register
FTD_CHROMA_THR_REG	0x038	FTD chroma threshold setting register
FTD_SLP_REG	0x03C	FTD slop setting register
CSC_ENABLE_REG	0x040	CSC enable setting register
CSC_D0_REG	0x044	CSC Constant D0 Register
CSC_D1_REG	0x048	CSC Constant D1 Register
CSC_D2_REG	0x04C	CSC Constant D2 Register
CSC_C00_REG	0x050	CSC Coefficient 00 Register
CSC_C01_REG	0x054	CSC Coefficient 01 Register
CSC_C02_REG	0x058	CSC Coefficient 02 Register
CSC_C03_REG	0x05C	CSC Constant 03 Register
CSC_C10_REG	0x060	CSC Coefficient 10 Register
CSC_C11_REG	0x064	CSC Coefficient 11 Register
CSC_C12_REG	0x068	CSC Coefficient 12 Register
CSC_C13_REG	0x06C	CSC Constant 13 Register
CSC_C20_REG	0x070	CSC Coefficient 20 Register
CSC_C21_REG	0x074	CSC Coefficient 21 Register
CSC_C22_REG	0x078	CSC Coefficient 22 Register
CSC_C23_REG	0x07C	CSC Constant 23 Register
CE_LUT_REGN	0x200+N*4	CE LUT register N (N=0:127)
HIST_CNT_REGN	0x400+N*4	Histogram count register N (N=0:255)

3.6.4 Register Description

3.6.4.1 Control register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: GCTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	WINDOW_EN CE/FTC window function enable 0x0:Disable 0x1:Enable Note: When window function enable, only the area inside the window will be processed. HIST and FTD function will be not effected by window function. **Note: double-buffered register.**
30:19	/	/	/
18	R/W	0x0	FTC_EN FTC function enable 0x0: Disable 0x1: Enable **Note: double-buffered register.**

17	R/W	0x0	CE_EN CE function enable 0x0: Disable 0x1: Enable **Note: double-buffered register.**
16	R/W	0x0	HIST_EN Histogram function enable 0x0: Disable 0x1: Enable **Note: double-buffered register.**
15:1	/	/	/
0	R/W	0x0	EN FCE module enable 0x0: Disable 0x1: Enable **Note: When module disable, the clock of the calculation circuit will be gated automatically.**

3.6.4.2 Size setting register (Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: FCE_SIZE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	HEIGHT Input height The actual height is register value + 1
15:12	/	/	/
11:0	R/W	0x0	WIDTH Input width The actual width is register value + 1

3.6.4.3 WIndow setting 0 register (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: FCE_WIN0_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	WIN_TOP Window Top position Top position is the left-top y coordinate of display window in pixels
15:12	/	/	/
11:0	R/W	0x0	WIN_LEFT Window Left position Left position is left-top x coordinate of display window in pixels

3.6.4.4 Window setting 1 register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: FCE_WIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	WIN_BOT Window Bottom position Bottom position is right-bottom y coordinate of display window in pixels
15:12	/	/	/
11:0	R/W	0x0	WIN_RIGHT Window Right position Right position is right-bottom x coordinate of display window in pixels

3.6.4.5 Histogram sum register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HIST_SUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SUM Pixel level sum Note: Register will clear when reset module. And double-buffered register refresh when pixel counter equal to WIDTH × HEIGHT.

3.6.4.6 Histogram status register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HIST_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R	0x0	HIST_NUM Histogram pixel number counter
7:2	/	/	/
1	R/W	0x0	BIST_EN BIST enable 0x0: Disable 0x1: Enable
0	R	0x0	HIST_CNT_VALID 0x0: AHB access not valid 0x1: AHB access valid **Note: This bit switch to 0 when HIST_CNT_REG are updated.**

3.6.4.7 CE LUT status register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CELUT_ACCESS_SWITCH 0x0: Module access 0x1: AHB access

			Note: When module access, CELUT registers can't access through AHB bus. When AHB access, CELUT will return the input address for data output.

3.6.4.8 CE chroma compensation function setting register (Default Value: 0x0000_0000)

Offset: 0x002C			**Register Name: CE_CC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CHROMA_COMPENSATION_EN 0x0: Disable 0x1: Enable

3.6.4.9 FTC gain setting register (Default Value: 0x0000_0000)

Offset: 0x0030			**Register Name: FTC_GAIN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	FTC_H_GAIN_R FTC gain value for Red
15:8	/	/	/
7:0	R/W	0x0	FTC_H_GAIN_Y FTC gain value for Yellow

3.6.4.10 FTD hue threshold setting register (Default Value: 0x0096_005A)

Offset: 0x0034			**Register Name: FTD_HUE_THR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x96	FTD_HUE_HIGH_THR FTD Skin hue high threshold **Note: must be set between 0x78~0xB4.**
15:9	/	/	/
8:0	R/W	0x5A	FTD_HUE_LOW_THR FTD Skin hue low threshold **Note: must be set between 0x3C~0x78.**

3.6.4.11 FTD chroma threshold setting register (Default Value: 0x0028_000A)

Offset: 0x0038			**Register Name: FTD_CHROMA_THR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x28	FTD_CHR_HIGH_THR FTD Skin chroma high threshold **Note: must be set between 0x14~0xB5.**

15:8	/	/	/
7:0	R/W	0x0A	FTD_CHR_LOW_THR FTD Skin chroma low threshold **Note: must be set between 0x0~0x14.**

3.6.4.12 FTD slop setting register (Default Value: 0x0404_0604)

Offset: 0x003C			Register Name: FTD_SLP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x4	FTD_CHR_HIGH_SLP FTD Skin chroma high slope
23:20	/	/	/
19:16	R/W	0x4	FTD_CHR_LOW_SLP FTD Skin chroma low slope
15:12	/	/	/
11:8	R/W	0x6	FTD_HUE_HIGH_SLP FTD Skin hue high slope
7:4	/	/	/
3:0	R/W	0x4	FTD_HUE_LOW_SLP FTD Skin hue low slope

3.6.4.13 CSC enable setting register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: CSC_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CSC_EN CSC enable 0x0: Disable 0x1: Enable

3.6.4.14 CSC constant D0 register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CSC_D0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	D0 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.6.4.15 CSC constant D1 register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CSC_D1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:10	/	/	/
9:0	R/W	0x0	D1 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.6.4.16 CSC constant D2 register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: CSC_D2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	D2 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.6.4.17 CSC coefficient 00 register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CSC_C00_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C00 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.18 CSC coefficient 01 register (Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CSC_C01_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C01 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.19 CSC coefficient 02 register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CSC_C02_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C02 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.20 CSC constant 03 register (Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: CSC_C03_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:10	/	/	/
9:0	R/W	0x0	C03 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.6.4.21 CSC coefficient 10 register (Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: CSC_C10_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C10 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.22 CSC coefficient 11 register (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: CSC_C11_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C11 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.23 CSC coefficient 12 register (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: CSC_C12_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C12 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.24 CSC constant 13 register (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: CSC_C13_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C13 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.6.4.25 CSC coefficient 20 register (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: CSC_C20_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:20	/	/	/
19:0	R/W	0x0	C20 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.26 CSC coefficient 21 register (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: CSC_C21_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C21 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.27 CSC coefficient 22 register (Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: CSC_C22_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	C22 The register value equals to constant*2^{CoBit} with 1-bit signed, 2-bit integer and CoBit-bit fraction. Valid value ranges from -0x7FFFF ~ 0x7FFFF.

3.6.4.28 CSC constant 23 register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: CSC_C23_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	C23 The register value equals to constant with 0-bit signed, 10-bit integer and 0-bit fraction.

3.6.4.29 CE LUT register N (N=0:127)

Offset: 0x0200 + N*0x4			Register Name: CE_LUT_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	UDF	/
25:16	R/W	UDF	CELUT1 (N*2+1) level LUT
15:10	/	UDF	/
9:0	R/W	UDF	CELUT0 (N*2) level LUT

Note: Registers can access in burst mode.

3.6.4.30 Histogram count register N (N=0:255)

Offset: 0x0400 + N*0x4			Register Name: HIST_CNT_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	UDF	HIST Bin N counter. **Note:** **1.Registers switch to AHB bus access mode when HIST_CNT_VALID = 1. When HIST_CNT_VALID = 0, accessing registers will return 0x00000000.** **2.Registers will be clear to zero when LCD SYNC positive edge comes.** **3.Registers can access in burst mode.**

3.7 DE FMT Specification

3.7.1 Overview

The formatter (FMT) is a DE module which provides YUV444 to YUV422/YUV420 conversion, format re-mapping and color depth conversion.

Feature:

- Interface: 10bit pre channel in both input and output
- Support input width up to *MAXWIDTH* pixels
- Support YUV444 to YUV420/ YUV444 to YUV422 conversion and format re-mapping
- Support color depth conversion from 10bit to 8bit

Configuration in H6 system:

Table 1-1. FMT configuration in H6 system

Configuration parameter	Descriptions	Platform
MAXWIDTH	Support maximum pixel per line	4096
SUPPORT_444TO420	Support YUV444 to YUV420 or not	YES

3.7.2 FMT Block Diagram

The FMT comprises with:
Swap: The module swaps Cb and Cr.
YUV444_formatter: The module re-maps channel data.
YUV422_formatter: The module converts YUV444 to YUV422 and re-maps channel data.
YUV420_formatter: The module converts YUV444 to YUV420 and re-maps channel data.
Color depth conversion: The module converts data color depth from 10bit to 8bit for all channels.
Register: The controller for AHB accessing.

Figure 3-6 shows a block diagram of the FMT.

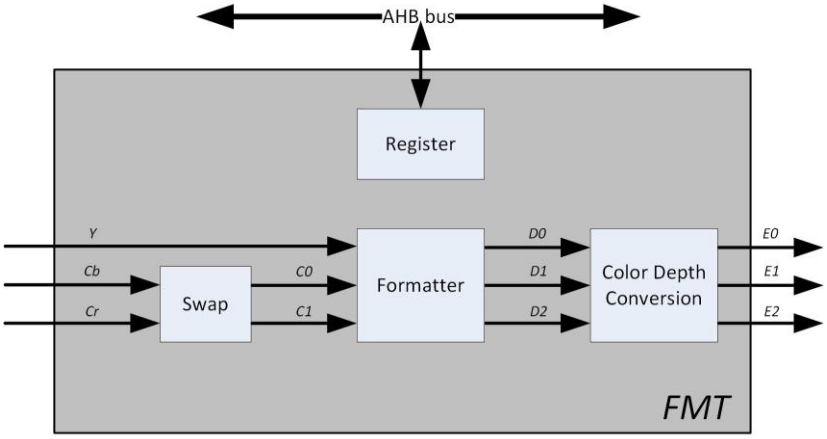


Figure 3-6. FMT Block Diagram

3.7.3 FMT Register List

Module Name	Offset Address
FMT	0x011A8000

Register Name	Offset	Description
FMT_CTRL_REG	0x0000	FMT Module Control Register
FMT_SIZE_REG	0x0004	FMT Size Setting Register
FMT_SWAP_REG	0x0008	FMT Swap Setting Register
FMT_BITDEPTH_REG	0x000C	FMT Color Depth Conversion Setting Register
FMT_FORMAT_REG	0x0010	FMT Formatter Setting Register
FMT_COEF_REG	0x0014	FMT Coefficient Setting Register
FMT_FUNC_VERSION_REG	0x0018	FMT Function Version Register

Note: All registers are single-buffered.

3.7.4 FMT Register Description

3.7.4.1 FMT Module Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: FMT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	BIST_EN BIST test enable 0: Disable 1: Enable
30:1	/	/	/
0	R/W	0x0	EN Module function enable 1: Disable 1: Enable Note: When set this bit to zero, the clock of FMT module will be closed.

3.7.4.2 FMT Size Setting Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: FMT_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HEIGHT Input pixel height. The actual height is the register value + 1. Note: The actual height must be 2 lines aligned.
15:13	/	/	/
12:0	R/W	0x0	WIDTH

			Input pixel width. The actual width is the register value + 1. **Note: The actual width must be 2 pixels aligned.**

3.7.4.3 FMT Swap Setting Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: FMT_SWAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	SWAP_EN Swap Cb and Cr component enable 0: Disable 1: Enable

3.7.4.4 FMT Color Depth Conversion Setting Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: FMT_BITDEPTH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	OUT_BITDEPTH Output color depth selection 0: 8-bit 1: 10-bit

3.7.4.5 FMT Formatter Setting Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: FMT_FORMAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	PIXEL_FORMAT_TYPE 0: Type0 1: Type1 others: Reserved **Note: Detail description in Table 1-2.**
15:2	/	/	/
1:0	R/W	0x0	COLOR_SPACE 0: YUV444 1: YUV422 2: YUV420 3: Reserved

3.7.4.6 FMT Coefficient Setting Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: FMT_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/

25:24	R/W	0x0	C1_V_COEF_SEL 0: V_Type0 1: V_Type1 2: V_Type2 3: Reserved
23:19	/	/	/
18:16	R/W	0x0	C1_H_COEF_SEL 0: H_Type0 1: H_Type1 2: H_Type2 3: H_Type3 4: H_Type4 5: H_Type5 6: H_Type6 7: H_Type7
15:10	/	/	/
9:8	R/W	0x0	C0_V_COEF_SEL 0: V_Type0 1: V_Type1 2: V_Type2 3: Reserved
7:3	/	/	/
2:0	R/W	0x0	C0_H_COEF_SEL 0: H_Type0 1: H_Type1 2: H_Type2 3: H_Type3 4: H_Type4 5: H_Type5 6: H_Type6 7: H_Type7

3.7.4.7 FMT Function Version Register (Default Value: 0x0000_0005)

Offset: 0x0018			**Register Name: FMT_FUNC_VERSION_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R	0x1	MAXWIDTH Support maximum pixel per line 0: 2048 1: 4096 2: Reserved
1	/	/	/
0	R	0x1	SUPPORT_444TO420 Support YUV444 to YUV420 or not 0: Not support

			1: Support

3.8 DE UIS Specification

3.8.1 UIS Overview

The UI Scale(UIS) provides RGB format image resizing function for display engine. It receives data from overlay module, performs the image resizing function, and outputs to routing modules.

The UIS can receive ARGB8888 data format, and then converts to a required size ARGB8888 image for display. Horizontal and vertical direction scaling are implemented independently.

Feature:

- Support ARGB data format with 8-bit per channel
- Support output size from 8×4 to 4096×4096
- Support input size from 8×4 to W_RGB×W_RGB for YUV444/ARGB format
- Support 1/16× to 32× resize ratio
- Support M-phase 4-tap horizontal anti-alias filter, M-phase 2 vertical linear filter for A/R(Y)/G(U)/B(V) channel scale-up and scale-down

Table 3-2. UIS programmable parameters table

Parameter name	Default	Possible value	Description
M	16	16	Phase number
W_RGB	2048	1280/2048/4096 etc	R/G/B channel line buffer length (ARGB/YUV444 format)
FRAC	18	18	Phase adder fraction part bit width

3.8.2 UIS Block Diagram

Figure 3-7 shows the block diagram of General Scaler Unit. It is a stream-to-stream module. The input interface which contains F/A/R/G/B five channels, receives data together from up-stream module. The A/R/G/B channels have the same resizing paths with the same scaling method. And the F channel is a 1-bit data channel that scales using the nearest neighborhood method which data represents the valid data flag generated by overlay module. After resizing, five channel FARGB data outputs in pixel mode to down-stream module. It contains some parts and their function list followed:

Control logic: state machine control, registers operation, VPHASE selection.

Resizing: five channels line buffer control, horizontal resize, vertical resize.

Figure 3-7 shows a block diagram of the UIS.

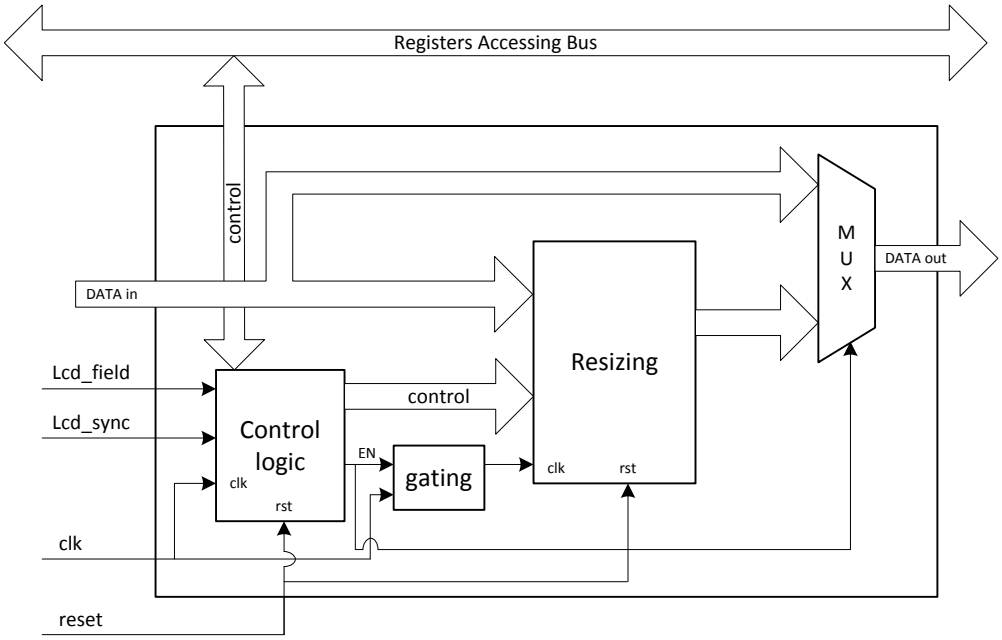


Figure 3-7. UIS Block Diagram

3.8.3 UIS Register List

Register Name	Offset	Description
UIS_CTRL_REG	0x0000	UIS Module Control Register
UIS_STATUS_REG	0x0008	UIS Status Register
UIS_FIELD_CTRL_REG	0x000C	UIS Field Control Register
UIS_OUTSIZE_REG	0x0040	UIS Output Size Register
UIS_INSIZE_REG	0x0080	UIS Input Size Register
UIS_HSTEP_REG	0x0088	UIS Horizontal Step Register
UIS_VSTEP_REG	0x008C	UIS Vertical Step Register
UIS_HPHASE_REG	0x0090	UIS Horizontal Initial Phase Register
UIS_VPHASE0_REG	0x0098	UIS Vertical Initial Phase 0 Register
UIS_VPHASE1_REG	0x009C	UIS Vertical Initial Phase 1 Register
UIS_HCOEF_REGN	0x0200+N*4	UIS Horizontal Filter Coefficient Register N (N=0:15)

Note: All registers except some bits in **UIS_CTRL_REG**, **UIS_FIELD_CTRL_REG**, **UIS_STATUS_REG** are double-buffered and refreshed by **REG_RDY**.

3.8.4 UIS Register Description

3.8.4.1 UIS Function Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UIS_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/WAC	0x0	COEF_SWITCH_RDY Coefficients RAM switch 0x0: DONOT switch

			0x1: Switch RAM use **REG_RDY** **Note: When LCD SYNC go low and COEF_SWITCH_RDY is 1, coefficient RAM will switch to the latest updated RAM if REG_RDY is 1, and then the bit will also be self-cleared if switch action successes.**
3:1	/	/	/
0	R/W	0x0	EN UIS enable 0x0: Disable 0x1: Enable **Note: When module disabled, the core clock to the core circuit will be gated, and the input data will be bypassed to down-stream module.**

Note: Only bit EN is double-buffered.

3.8.4.2 UIS Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: UIS_STATUS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R	0x0	LINE_CNT Output line number
15:5	/	/	/
4	R	0x0	BUSY Core circuit status 0x0: idle (finish, module disable, waiting for **LCD SYNC** negative edge) 0x1: busy (core circuit calculating)
3:0	/	/	/

Note: Whole WORD is non-double-buffered.

3.8.4.3 UIS Field Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: UIS_FIELD_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	LCD_SYNC_REVERSE Reverse LCD SYNC 0x0: DONOT reverse 0x1: Reverse
4	R/W	0x0	LCD_FILED_REVERSE Reverse LCD FILED 0x0: DONOT reverse 0x1: Reverse
3:1	/	/	/
0	R/W	0x0	FIELD_SEL_VPHASE_EN Vertical initial phase switch control 0x0: Vertical initial phase fix to phase0 0x1: Switch Vertical initial phase by LCD FIELD (Switch to phase0 when LCD

			FILED is 1, and switch to phase1 when LCD FIELD is 0)

Note: Only bit FIELD_SEL_VPHASE_EN is double-buffered.

3.8.4.4 UIS Output Size Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: UIS_OUT_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output width The actual width is register value + 1

3.8.4.5 UIS Input Size Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UIS_INSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input width The actual width is register value + 1

3.8.4.6 UIS Horizontal Step Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: UIS_HSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:20	R/W	0x0	HSTEP_INT The integer part of horizontal scale ratio Note: valid range from 0~16.
19:2	R/W	0x0	HSTEP_FRAC The fraction part of horizontal scale ratio
1:0	/	/	/

3.8.4.7 UIS Vertical Step Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: UIS_VSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/

24:20	R/W	0x0	VSTEP_INT The integer part of vertical scale ratio Note: valid range from 0~16.
19:2	R/W	0x0	VSTEP_FRAC The fraction part of vertical scale ratio
1:0	/	/	/

3.8.4.8 UIS Horizontal Initial Phase Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: UIS_HPHASE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	HPHASE_INT The integer part of horizontal initial phase Note: must set 0xF or 0x0.
19:2	R/W	0x0	HPHASE_FRAC The fraction part of horizontal initial phase
1:0	/	/	/

Note : HPHASE is a register with 1-bit signed, 3-bit integer and 18-bit fraction. Valid value ranges from -0x3FFFF ~ 0x3FFFF.

3.8.4.9 UIS Vertical Initial Phase 0 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: UIS_VPHASE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	VPHASE0_INT The integer part of vertical initial phase0 Note: must set 0xF or 0x0.
19:2	R/W	0x0	VPHASE0_FRAC The fraction part of vertical initial phase0
1:0	/	/	/

Note: VPHASE0 is a register with 1-bit signed, 3-bit integer and 18-bit fraction. Valid value ranges from -0x3FFFF ~ 0x3FFFF.

3.8.4.10 UIS Vertical Initial Phase 1 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: UIS_VPHASE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	VPHASE1_INT The integer part of vertical initial phase1 **Note:** must set 0xF or 0x0.
19:2	R/W	0x0	VPHASE1_FRAC The fraction part of vertical initial phase1
1:0	/	/	/

Note: VPHASE1 is a register with 1-bit signed, 3-bit integer and 18-bit fraction. Valid value ranges from -0x3FFFF ~ 0x3FFFF.

3.8.4.11 UIS Horizontal Filter Coefficient Register N (N=0:(M-1))

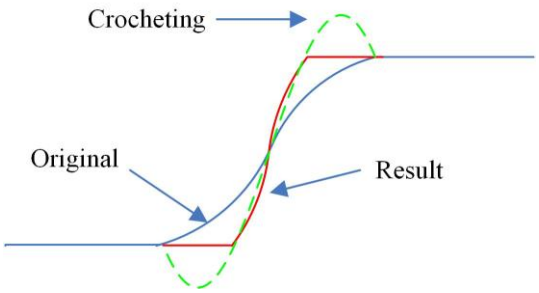
Offset: 0x0200 + N*4			Register Name: UIS_HCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	COEF3
23:16	R/W	UDF	COEF2
15:8	R/W	UDF	COEF1
7:0	R/W	UDF	COEF0

3.9 DE LCTI Specification

3.9.1 LCTI Overview

Chrominance transient improvement (CTI) is a method to enhance the image quality . The method of the chrominance signal transition bands were detected, when the chrominance signal transition, so that the signal transition zone is narrow, steep edge, so as to improve the clarity of the image, the image is more clear and bright.

This algorithm uses the one-dimensional stacking hook signal method commonly used, through a hook signal superimposed on the input signal, the signal edge becomes steeper, and then calculate the signal of a window within the scope of the maximum and minimum values, will limit the signal after superposition in the minimum and maximum range, to get the final results. Sketch of the algorithm is as follows:



3.9.2 Register List

Module Name	Base Address
LCTI	0x01171000

Register name	Offset	Description
LTI_EN	0x000	Global control register
LTI_SIZE	0x00C	LTI size register
LTI_FIR_COFF0	0x010	LTI FIR filter coefficient register0
LTI_FIR_COFF1	0x014	LTI FIR filter coefficient register1
LTI_FIR_COFF2	0x018	LTI FIR filter coefficient register2
LTI_FIR_GAIN	0x01C	LTI FIR filter gain register
LTI_COR_TH	0x020	LTI coring threshold register
LTI_DIFF_CTL	0x024	LTI scaling coefficient/offset of frist derivation
LTI_EDGE_GAIN	0x028	LTI edge gain
LTI_OS_CON	0x02C	LTI coring/clipping threshold of Y shoot value
LTI_WIN_EXPANSION	0x030	LTI window range control register
LTI_EDGE_LEVEL_TH	0x034	LTI edge level threshold in edge-adaptive filtering
LTI_WIN0_REG	0x038	LTI window setting register0
LTI_WIN1_REG	0x03c	LTI window setting register1

CTI_EN	0x100	CTI Global control register
CTI_SIZE	0x10C	CTI size register
CTI_FIR_COFF0	0x110	CTI FIR filter coefficient register0
CTI_FIR_COFF1	0x114	CTI FIR filter coefficient register1
CTI_FIR_COFF2	0x118	CTI FIR filter coefficient register2
CTI_FIR_GAIN	0x11C	CTI FIR filter gain register
CTI_COR_TH	0x120	CTI coring threshold register
CTI_DIFF_CTL	0x124	CTI scaling coefficient/offset of frist derivation
CTI_EDGE_GAIN	0x128	CTI edge gain
CTI_OS_CON	0x12C	CTI coring/clipping threshold of UV shoot value
CTI_WIN_EXPANSION	0x130	CTI window range control register
CTI_EDGE_LEVEL_TH	0x134	CTI edge level threshold in edge-adaptive filtering
CTI_WIN0_REG	0x138	CTI window setting register0
CTI_WIN1_REG	0x13c	CTI window setting register1
CTI_CLMPRT_REG	0x140	CTI climbing protection register

3.9.3 Register Description

3.9.3.1 Global control register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LTI_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	Reserved
24	R/W	0x0	**WIN_EN** 0: disable 1: enable
23:17	/	/	/
16	R/W	0x0	**NONLINEAR_LIMIT_EN** 0: disable 1: enable
15:9	/	/	/
8	R/W	0x0	**SEL** 0: select window range 1: select first differ
7:1	/	/	/
0	R/W	0x0	**LTI_EN** 0: LTI close 1: LTI open

3.9.3.2 LTI size register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: LTI_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	Reserved

27:16	R/W	0x0	**HEIGHT** The real height = The value of these bits add 1
15:12	/	/	/
11:0	R/W	0x0	**WIDTH** The real width = The value of these bits add 1

3.9.3.3 LTI FIR filter coefficient register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LTI_FIR_COFF0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**C1** FIR filter coefficient C1 Note: in two's complement. Range: -127~+127
15:8	/	/	/
7:0	R/W	0x0	**C0** FIR filter coefficient C0 Note: in two's complement. Range: -127~+127

3.9.3.4 LTI FIR filter coefficient register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: LTI_FIR_COFF1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**C3** FIR filter coefficient C3 Note: in two's complement. Range: -127~+127
15:8	/	/	/
7:0	R/W	0x0	**C2** FIR filter coefficient C2 Note: in two's complement. Range: -127~+127

3.9.3.5 LTI FIR filter coefficient register2 (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: LTI_FIR_COFF2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**C7** FIR filter coefficient C7 Note: in two's complement. Range: -127~+127
23:16	R/W	0x0	**C6** FIR filter coefficient C6

			Note: in two's complement. Range: -127~+127
15:8	R/W	0x0	**C5** FIR filter coefficient C5 Note: in two's complement. Range: -127~+127
7:0	R/W	0x0	**C4** FIR filter coefficient C4 Note: in two's complement. Range: -127~+127

3.9.3.6 LTI FIR filter gain register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: LTI_FIR_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	**FIR FILTER GAIN**

3.9.3.7 LTI coring threshold register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: LTI_COR_TH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	**LTI_COR_TH** Coring threshold

3.9.3.8 LTI differ filter control register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: LTI_DIFF_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	**DIFF_SLOPE** Differ gain slope control
15:8	/	/	/
7:0	R/W	0x0	**DIFF_OFFSET** Differ gain offset control

3.9.3.9 LTI adjustable gain parameter register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: LTI_EDGE_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**LTI_SKMG_EN** Skinmap control gain enable
7:5	/	/	/
4:0	R/W	0x0	**LTI_EDGE_GAIN**

			Edge adjustable gain parameter

3.9.3.10 LTI The overshoot of control register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: LTI_OS_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	**PEAK_LIMIT** Shifting bit for nonlinear limit
27:24	/	/	/
23:16	R/W	0x0	**CLIP_Y** Clipping threshold of Y shoot value
15:8	/	/	/
7:0	R/W	0x0	**CORE_X** Coring threshold of Y shoot value

3.9.3.11 LTI window range expansion register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: LTI_WIN_EXPANSION
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	**CMP_WIN_SEL** Compare window radius select. Change this for different scale ratio. (0~2)
7:0	R/W	0x0	**LTI_WIN_EXPANSION** Window expansion size

3.9.3.12 LTI edge strength threshold register (Default Value: 0x0000_0000)

Offset: 00x034			Register Name: LTI_EDGE_ELVEL_TH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**LTI_EDGE_ELVEL_TH** Edge level threshold in edge-adaptive filtering

3.9.3.13 LTI_WIN0_REG (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: LTI_WIN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
27:16	R/W	0X0	**WIN_TOP** Window Top position
15:12	/	/	/
11:0	R/W	0x0	**WIN_LEFT** Window Left position

3.9.3.14 LTI_WIN1_REG (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LTI_WIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
27:16	R/W	0X0	**WIN_BOT** Window bottom position
15:12	/	/	/
11:0	R/W	0x0	**WIN_RIGHT** Window right position

3.9.3.15 Global control register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: CTI_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	Reserved
24	R/W	0x0	**WIN_EN** 0: disable 1: enable
23:17	/	/	/
16	R/W	0x0	**NONLINEAR_LIMIT_EN** 0: disable 1: enable
15:9	/	/	/
8	R/W	0x0	**SEL** 0: select window range 1: select first differ
7:1	/	/	/
0	R/W	0x0	**CTI_EN** 0: CTI close 1: CTI open

3.9.3.16 CTI size register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: CTI_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	Reserved
28:16	R/W	0x0	**HEIGHT** The real height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** The real width = The value of these bits add 1

3.9.3.17 CTI FIR filter coefficient register0 (Default Value: 0x0000_0000)

Offset: 0x0110	Register Name: CTI_FIR_COFF0

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	**C1** FIR filter coefficient C1 Note: in two's complement. Range: -127~+127
15:8	/	/	/
7:0	R/W	0x0	**C0** FIR filter coefficient C0 Note: in two's complement. Range: -127~+127

3.9.3.18 CTI FIR filter coefficient register1 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: CTI_FIR_COFF1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**C3** FIR filter coefficient C3 Note: in two's complement. Range: -127~+127
15:8	/	/	/
7:0	R/W	0x0	**C2** FIR filter coefficient C2 Note: in two's complement. Range: -127~+127

3.9.3.19 CTI FIR filter coefficient register2 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: CTI_FIR_COFF2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**C7** FIR filter coefficient C7 Note: in two’s complement. Range: -127~+127
23:16	R/W	0x0	**C6** FIR filter coefficient C6 Note: in two’s complement. Range: -127~+127
15:8	R/W	0x0	**C5** FIR filter coefficient C5 Note: in two’s complement. Range: -127~+127
7:0	R/W	0x0	**C4** FIR filter coefficient C4 Note: in two's complement.

			Range: -127~+127

3.9.3.20 TI FIR filter gain register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: CTI_FIR_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	**FIR FILTER GAIN**

3.9.3.21 CTI coring threshold register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: CTI_COR_TH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	**CTI_COR_TH** Coring threshold

3.9.3.22 CTI differ filter control register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: CTI_DIFF_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	**DIFF_SLOPE** Differ gain slope control
15:8	/	/	/
7:0	R/W	0x0	**DIFF_OFFSET** Differ gain offset control

3.9.3.23 CTI adjustable gain parameter register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: CTI_EDGE_GAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**CTI_SKMG_EN** Skinmap control gain
7:5	/	/	/
4:0	R/W	0x0	**CTI_EDGE_GAIN** Edge adjustable gain parameter

3.9.3.24 CTI The overshoot of control register (Default Value: 0x0000_0000)

Offset: 0x012c			Register Name: CTI_OS_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	**PEAK_LIMIT**

			Shifting bit for nonlinear limit
27:24	/	/	/
23:16	R/W	0x0	**CLIP_UV** Clipping threshold of UV shoot value
15:8	/	/	/
7:0	R/W	0x0	**CORE_X** Coring threshold of UV shoot value

3.9.3.25 CTI window range expansion register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: CTI_WIN_EXPANSION
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	**CMP_WIN_SEL** Compare window radius select. Change this for different scale ratio. (0~2)
7:0	R/W	0x0	**CTI_WIN_EXPANSION** Window expansion size

3.9.3.26 CTI edge strength threshold register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: CTI_EDGE_ELVEL_TH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**CTI_EDGE_ELVEL_TH** Edge level threshold in edge-adaptive filtering

3.9.3.27 CTI_WIN0_REG (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: CTI_WIN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
27:16	R/W	0X0	**WIN_TOP** Window Top position
15:12	/	/	/
11:0	R/W	0x0	**WIN_LEFT** Window Left position

3.9.3.28 CTI_WIN1_REG (Default Value: 0x0000_0000)

Offset: 0x013c			Register Name: CTI_WIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
27:16	R/W	0X0	**WIN_BOT** Window bottom position
15:12	/	/	/

11:0	R/W	0x0	**WIN_RIGHT** Window right position

3.9.3.29 CTI_CLMPRT_REG (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: CTI_CLMPRT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	/	/	/
11:8	R/W	0x0	**CLM_LMT** Climbing limit
7:0	R/W	0x0	**CLM_THR** Climbing detect threshold

3.10 DE Luma Peaking Specification

3.10.1 Overview

The Luma Peaking module enhances mid-high frequence of luma channel in images. The chroma channels will bypass.

The Luma Peaking module including following feature:

- Maximum input frame size: 4096×2160.
- Data width: 8bit /10bit(hardware programmable) per channel.
- Interface: Stream-to-stream pixel interface.

Table 3-3. RTL programmable paaarameeeters table

Parameter name	Default	Possible value	Description
CSTM_FILTER_EXIST	1	0/1	Custom filter exist in this module.

3.10.2 Luma Peaking Block Diagram

Figure 3-8 shows the block diagram of luma peaking module. It is a stream-to-stream module with uniform input and output interface. It contains some parts and their function list followed:

- Control logic: Status machine control, registers operation.
- Peaking calculation unit: luma peaking, chroma bypassing.
- MUX: select processed data or input data (input data pass-through works without clock)

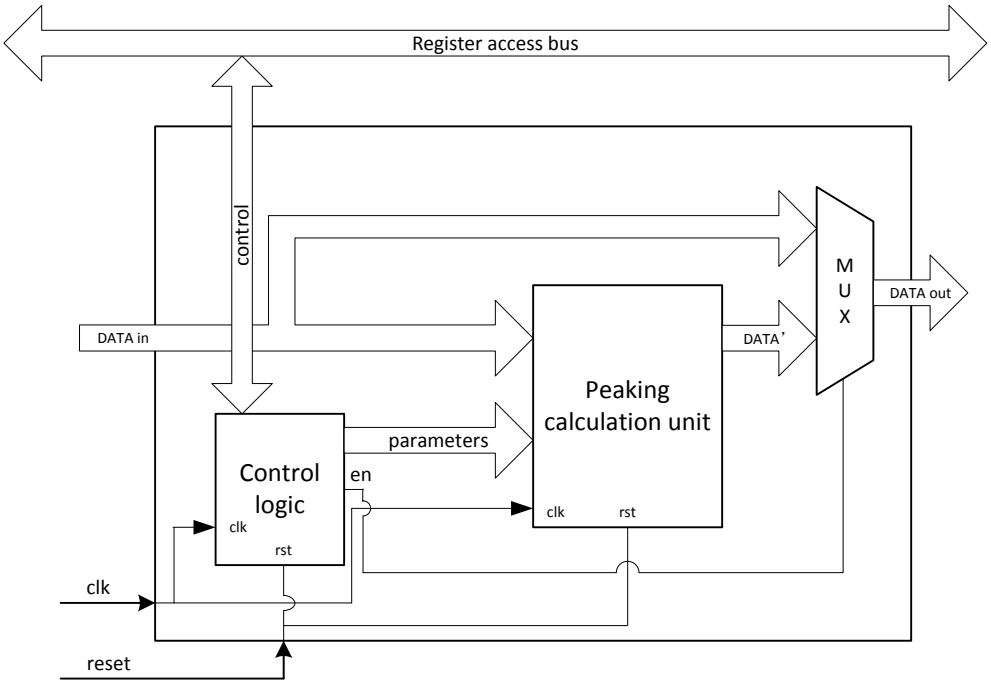


Figure 3-8. Luma peaking module block diagram

3.10.3 Register list

Module Name	Base Address
PEAKING	0x01170800

Register Name	Offset	Description
LP_CTRL_REG	0x000	LP module control register
LP_SIZE_REG	0x004	LP size setting register
LP_WIN0_REG	0x008	LP window setting register0
LP_WIN1_REG	0x00C	LP window setting register1
LP_FILTER_REG	0x010	LP filter setting register
LP_CSTM_FILTER0_REG	0x014	LP custom filter setting register0
LP_CSTM_FILTER1_REG	0x018	LP custom filter setting register1
LP_CSTM_FILTER2_REG	0x01C	LP custom filter setting register2
LP_GAIN_REG	0x020	LP gain setting register
LP_GAINCTRL_REG	0x024	LP gain control setting register
LP_SHOOTCTRL_REG	0x028	LP shoot control setting register
LP_CORING_REG	0x02C	LP coring setting register

3.10.4 Register Description

3.10.4.1 LP_CTRL_REG (Default Value: 0x0000_0000)

Offset: 0x0000			Register name: LP_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**WIN_EN** Output window function enable 0: disable 1: enable
7:1	/	/	/
0	R/W	0x0	**EN** LP Module enable 0: Disable 1: Enable

3.10.4.2 LP_SIZE_REG (Default Value: 0x0000_0000)

Offset: 0x0004			Register name: LP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**HEIGHT** Processing height The real display height = The value of these bits + 1.

15:12	/	/	/
11:00	R/W	0	**WIDTH** Processing width The real display width = The value of these bits + 1.

3.10.4.3 LP_WIN0_REG (Default Value: 0x0000_0000)

Offset: 0x0008			Register name: LP_WIN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**WIN_TOP** Window Top position Top position is the left-top y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0	**WIN_LEFT** Window Left position Left position is left-top x coordinate of display window in pixels

3.10.4.4 LP_WIN1_REG (Default Value: 0x0000_0000)

Offset: 0x000C			Register name: LP_WIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0	**WIN_BOT** Window Bottom position Bottom position is right-bottom y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0	**WIN_RIGHT** Window Right position Right position is right-bottom x coordinate of display window in pixels

3.10.4.5 LP_FILTER_REG (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LP_FILTER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	**FILTER_SEL** Filter selection: 0: Default filter. 1: Custom filter.
30:22	/	/	/
21:16	R/W	0x0	**HP_RATIO** Default high-pass filter ratio Note: in two's complement.
15:14	/	/	/
13:8	R/W	0x0	**BP0_RATIO**

			Default band-pass filter0 ratio Note: in two's complement.
7:6	/	/	/
5:0	R/W	0x0	**BP1_RATIO** Default band-pass filter1 ratio Note: in two's complement.

3.10.4.6 LP_CSTM_FILTER0_REG (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: LP_CSTM_FILTER0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x0	**C1** Custom filter coefficient C1. Note: in two's complement. Range: -255~+255
15:9	/	/	/
8:0	R/W	0x0	**C0** Custom filter coefficient C0. Note: in two's complement. Range: -255~+255

3.10.4.7 LP_CSTM_FILTER1_REG (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: LP_CSTM_FILTER1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x0	**C3** Custom filter coefficient C3. Note: in two's complement. Range: -255~+255
15:9	/	/	/
8:0	R/W	0x0	**C2** Custom filter coefficient C2. Note: in two's complement. Range: -255~+255

3.10.4.8 LP_CSTM_FILTER2_REG (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: LP_CSTM_FILTER2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R/W	0x0	**C4** Custom filter coefficient C4. Note: in two's complement.

			Range: -255~+255

3.10.4.9 LP_GAIN_REG(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: LP_GAIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**GAIN** Peaking gain setting.

3.10.4.10 LP_GAINCTRL_REG (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: LP_GAINCTRL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	**DIF_UP** Gain control: limitation threshold. Note: use low 8bits for 8bit data width.
15:8	/	/	/
4:0	R/W	0x0	**BETA** Gain control: large gain limitation.

3.10.4.11 LP_SHOOTCTRL_REG (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: LP_SHOOTCTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	**NEG_GAIN** Undershoot gain control.

3.10.4.12 LP_CORING_REG (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: LP_CORING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**CORTHR** Coring threshold. Note: use low 8bits for 8bit data width.

3.11 DE RT-MIXER Specification

3.11.1 Overview

The RT-mixer Core consist of dma, overlay, scaler and blender block. It supports 4 layers overlay in one pipe, and its result can scaler up or down to blender in the next processing. There's the feature description as follows:

- Support output size up to 4096x4096
- Support four alpha blending channels for main display, two channels for aux display.
- Support four overlay layers in each channel, and has an independent scaler.
- Support potter-duff compatible blending operation.
- Support AFBC buffer in main display.
- Support input format Semi-planar YUV422/YUV420/YUV411 and Planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565.
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- Support SmartColor3.0 for excellent display experience.
  - Adaptive detail/edge enhancement.
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify.
  - Adaptive de-noising with image quality assessment and block detector function.
  - Content adaptive backlight control.
- Support write back and rotation for high efficient dual display and miracast.

3.11.2 Block Diagram

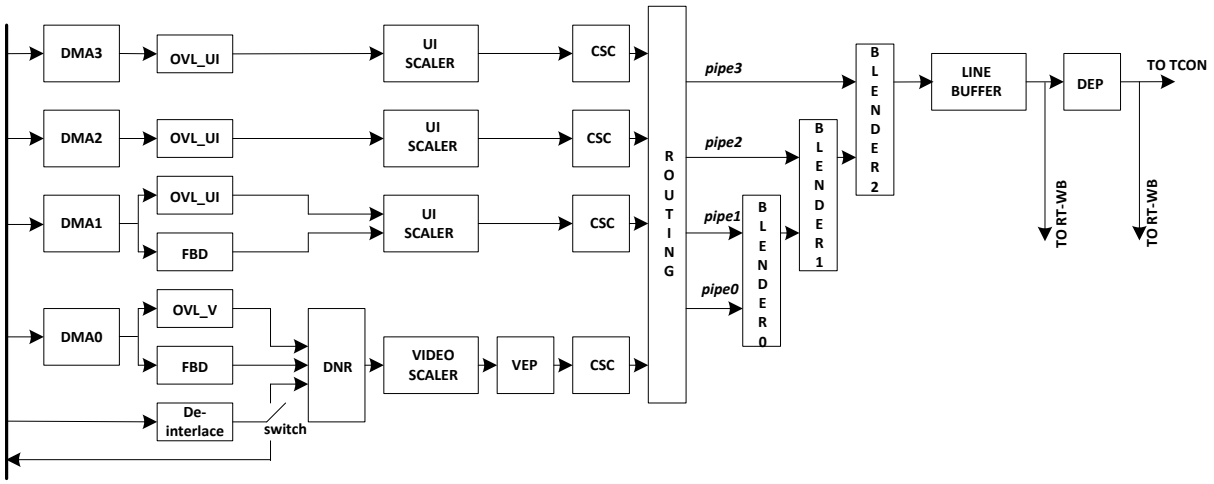


Figure 3-9. RT-Mixer General Diagram

3.11.3 DE RT-Mixer Description

3.11.3.1 Input Data Memory Layout

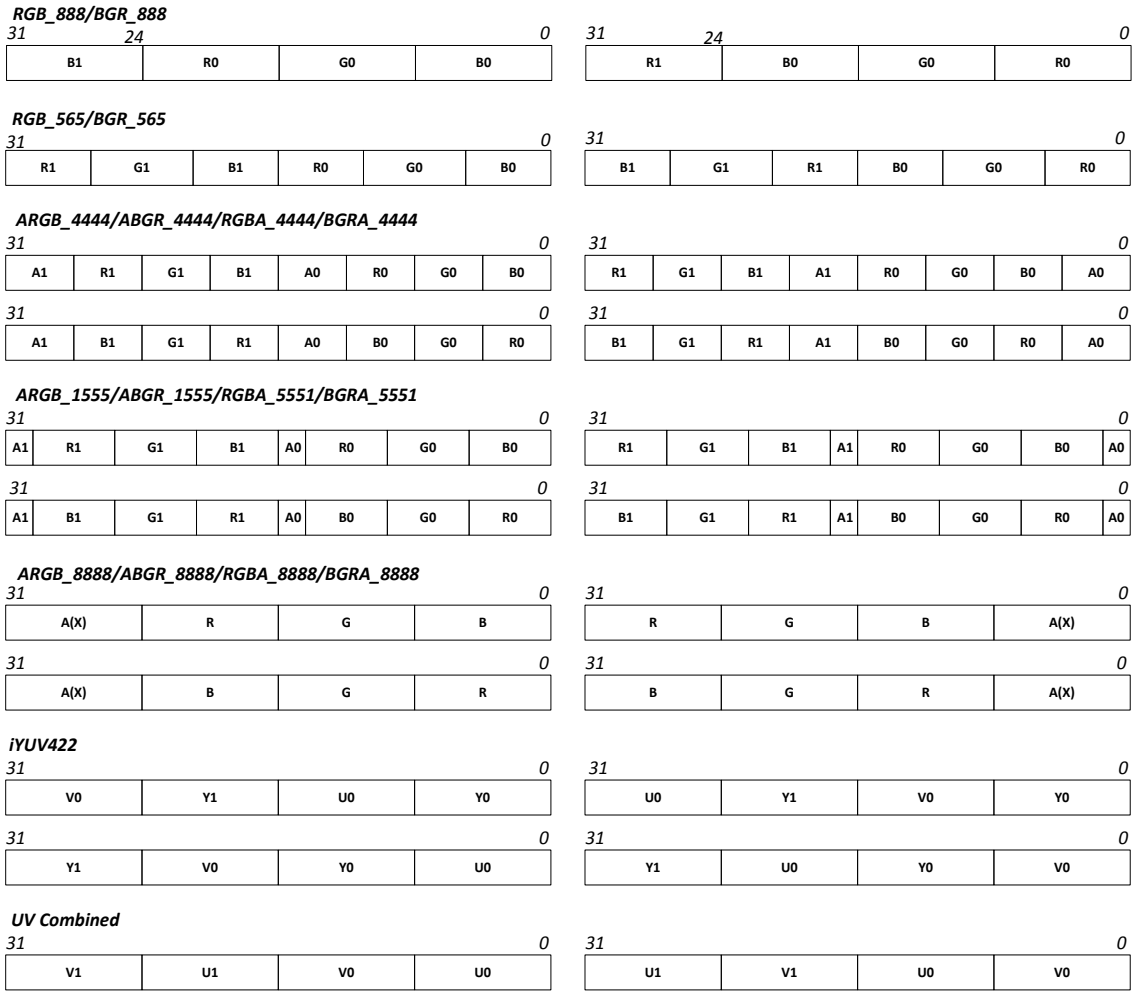


Figure 3-10. Input data pixel sequence

3.11.3.2 Overlay

Figure 3-11 is the overlay processing include layer memory data access and overlay relationship, the detail as following.

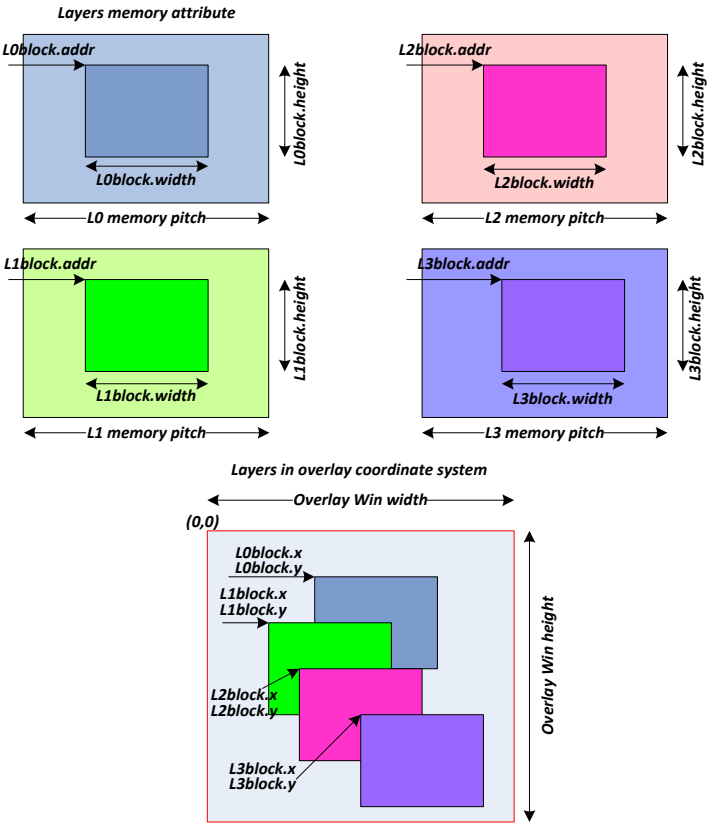


Figure 3-11. Layers memory access and overlay processing

Note: the layer priority is layer3>layer2>layer1>layer0

3.11.3.3 Routing

Routing: The routing connects N channels and N input of blending together. Any channel can connect to any pipe. Programmer should make sure every pipe should connect one different channel only.

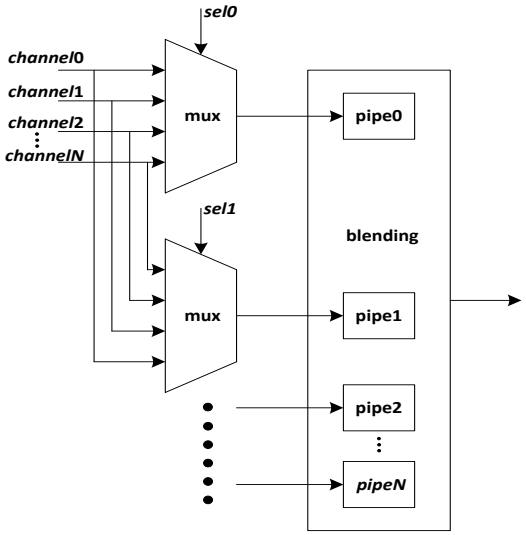


Figure 3-12. N Channel select pipe route processing

3.11.3.4 Blender

Blender input data storing:

The following diagram is about overlay data remapping in the blender pipe.

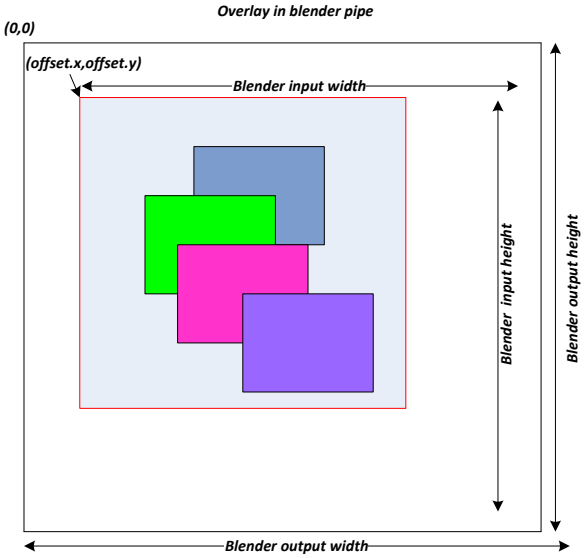


Figure 3-13. Pipe memory access diagram

Alpha blending:

Alpha blending is a convex combination of two colors allowing for transparency effects in computer graphics. The value of alpha in the color code ranges from 0.0 to 1.0, where 0.0 represents a fully transparent color, and 1.0 represents a fully opaque color.

In the display engine:

If setting the alpha register value (ARV) = 0B xxxxxxxx (8 bit value)

Then the alpha value (AV) = ARV/256; when ARV == 255, AV = 1.

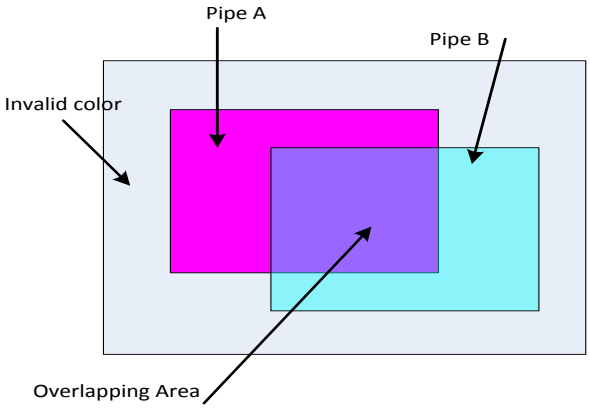


Figure 3-14. alpha blending processing

Color key:

In display engine, the process of color key will be done in Alpha Blender block. When the color match one pipe, another pipe color will pass, otherwise, in the non-match area color key will be same as normal alpha blending process. Figure 3-15a) is the sketch map and Figure 1-8 is the processing diagram.

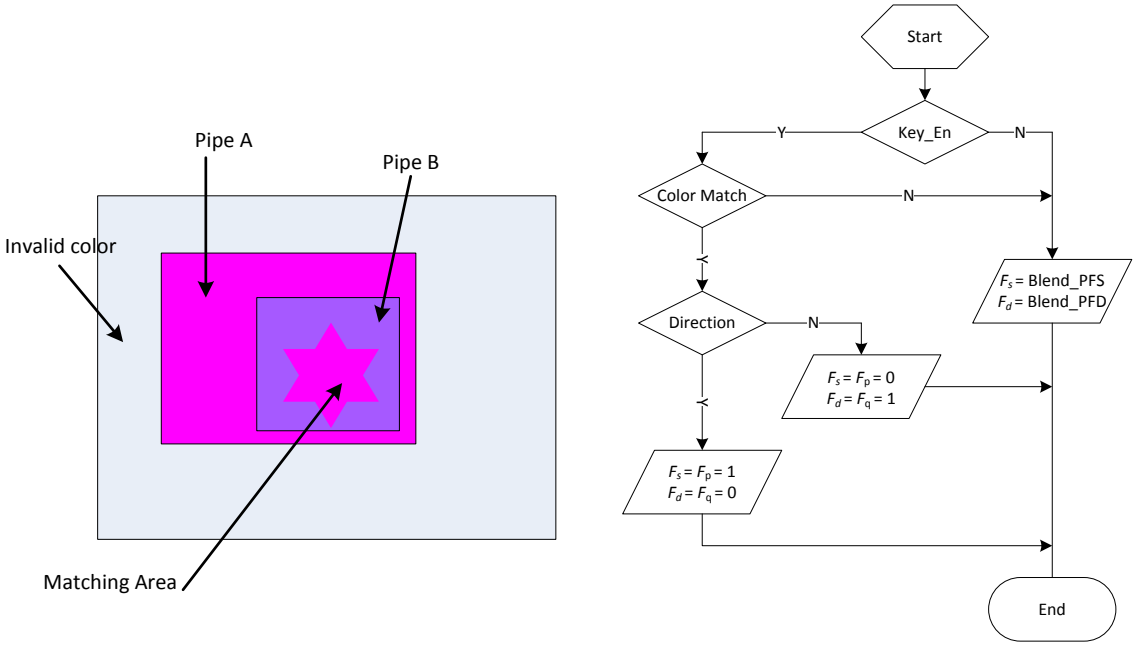


Figure 3-15. a) Color Key Diagram b) Color Key Processing

3.11.3.5 Interface

There are some restriction as follow:

- When the field signal from lcd is high, using the top field address, otherwise changing to the bottom field address.
- When lcd sync is high the module should reset, if the sync is changing from high to low, the module should start.

3.11.4 Memory Mapping List

		Module Name	Base Address	Memory Range
RT-Mix0	***RTMX***	rtd	0x01100000	2K
		apb	0x01100800	2K
		ovl0	0x01101000	2K
		ovl1	0x01101800	2K
		ovl2	0x01102000	2K
		ovl3	0x01102800	2K
		ovl4	0x01103000	2K
		ovl5	0x01103800	2K
		ovl6	0x01104000	2K
		ovl7	0x01104800	2K
		dma	0x01108000	32K
	Scaler	SCALER0	0x01120000	32K
		SCALER1	0x01128000	32K
		SCALER2	0x01130000	32K
		SCALER3	0x01138000	32K
		SCALER4	0x01140000	32K
		SCALER5	0x01148000	32K

		SCALER6	0x01150000	32K
		SCALER7	0x01158000	32K
	VEP	FCE	0x01170000	2K
		Peak	0x01170800	2K
		CTI	0x01171000	2K
		BLS	0x01171800	2K
		FCC	0x01172000	2K
		VEP_TOP	0x01177000	4K
	VEP1		0x01178000~0x0117ffff	32K
	DNR	DNR	0x01180000	32K
	DEP	DRC	0x011a0000	32K
		Line buffer	0x011c0000	32K
RT-Mix1			0x01200000~	

Note: The method of configuring RT-Mix1 address space is same as RT-Mix0.

3.11.5 Register List

Register name	Offset	Description
GLB_CTL	0x000	Global control register
GLB_STS	0x004	Global status register
GLB_DBUFFER	0x008	Global double buffer control register
GLB_SIZE	0x00C	Global size register
GLB_DI_CTL	0x010	Global de-interlace control register
OVL_V_ATTCTL	0x000 + N*0x30	OVL_V attribute control register(N=0,1,2,3)
OVL_V_MBSIZE	0x004 + N*0x30	OVL_V memory block size register(N=0,1,2,3)
OVL_V_COOR	0x008 + N*0x30	OVL_V memory block coordinate register(N=0,1,2,3)
OVL_V_PITCH0	0x00C + N*0x30	OVL_V memory pitch register0(N=0,1,2,3)
OVL_V_PITCH1	0x010 + N*0x30	OVL_V memory pitch register1(N=0,1,2,3)
OVL_V_PITCH2	0x014 + N*0x30	OVL_V memory pitch register2(N=0,1,2,3)
OVL_V_TOP_LADD0	0x018 + N*0x30	OVL_V top field memory block low address register0(N=0,1,2,3)
OVL_V_TOP_LADD1	0x01C + N*0x30	OVL_V top field memory block low address register1(N=0,1,2,3)
OVL_V_TOP_LADD2	0x020 + N*0x30	OVL_V top field memory block low address register2(N=0,1,2,3)
OVL_V_BOT_LADD0	0x024 + N*0x30	OVL_V bottom field memory block low address register0(N=0,1,2,3)
OVL_V_BOT_LADD1	0x028 + N*0x30	OVL_V bottom field memory block low address register1(N=0,1,2,3)
OVL_V_BOT_LADD2	0x02C + N*0x30	OVL_V bottom field memory block low address register2(N=0,1,2,3)
OVL_V_FILL_COLOR	0x0C0 + N*0x4	OVL_V fill color register(N=0,1,2,3)

OVL_V_TOP_HADD0	0x0D0	OVL_V top field memory block high address register0
OVL_V_TOP_HADD1	0x0D4	OVL_V top field memory block high address register1
OVL_V_TOP_HADD2	0x0D8	OVL_V top field memory block high address register2
OVL_V_BOT_HADD0	0x0DC	OVL_V bottom field memory block high address register0
OVL_V_BOT_HADD1	0x0E0	OVL_V bottom field memory block high address register1
OVL_V_BOT_HADD2	0x0E4	OVL_V bottom field memory block high address register2
OVL_V_SIZE	0x0E8	OVL_V overlay window size register
OVL_V_HDS_CTL0	0x0F0	OVL_V horizontal down sample control register0
OVL_V_HDS_CTL1	0x0F4	OVL_V horizontal down sample control register1
OVL_V_VDS_CTL0	0x0F8	OVL_V vertical down sample control register0
OVL_V_VDS_CTL1	0x0FC	OVL_V vertical down sample control register1
/	0x100~0x2FC	/
FBD_V_CTL	0x300	OVL_V FBD control register
FBD_V_STA	0x304	OVL_V FBD status register
FBD_V_SIZE	0x308	OVL_V FBD image size register
FBD_V_BLOCK_SIZE	0x30C	OVL_V FBD block size register
FBD_V_SRC_CROP	0x310	OVL_V FBD source crop register
FBD_V_OVL_CROP	0x314	OVL_V FBD overlay crop register
FBD_V_FMT	0x318	OVL_V FBD input format register
/	0x31C	/
FBD_V_HD_LADDR	0x320	OVL_V FBD header low address register
FBD_V_HD_HADDR	0x324	OVL_V FBD header high address register
FBD_V_PL_LADDR	0x328	OVL_V FBD payload low address register
FBD_V_PL_HADDR	0x32C	OVL_V FBD payload high address register
FBD_V_OVL_SIZE	0x330	OVL_V FBD overlay window size register
FBD_V_COOR	0x334	OVL_V FBD memory block coordinate register
FBD_V_BGC	0x338	OVL_V FBD memory block coordinate register
FBD_V_FC	0x33C	OVL_V FBD overlay window size register
OVL_V_FBD_DBG0	0x340	OVL_V FBD dbg0 register
OVL_V_FBD_DBG1	0x344	OVL_V FBD dbg1 register
OVL_V_FBD_DBG2	0x348	OVL_V FBD dbg2 register
OVL_V_FBD_DBG3	0x34C	OVL_V FBD dbg3 register
/	0x350~0x37C	/
OVL_V_FBD_BIST_STATUS	0x380	OVL_V FBD bist register
OVL_V_FBD_BIST_START_ADDR	0x384	OVL_V FBD bist start address register
OVL_V_FBD_BIST_START_ADDR	0x388	OVL_V FBD bist end address register
OVL_V_FBD_BIST_MARK	0x38C	OVL_V FBD bist data mark register
OVL_UI_ATTCTL	0x000 + N*0x20	OVL_UI attribute control register(N=0,1,2,3)
OVL_UI_MBSIZE	0x004 + N*0x20	OVL_UI memory block size register(N=0,1,2,3)
OVL_UI_COOR	0x008 + N*0x20	OVL_UI memory block coordinate register(N=0,1,2,3)
OVL_UI_PITCH	0x00C + N*0x20	OVL_UI memory pitch register(N=0,1,2,3)
OVL_UI_TOP_LADD	0x010 + N*0x20	OVL_UI top field memory block low address register(N=0,1,2,3)
OVL_UI_BOT_LADD	0x014 + N*0x20	OVL_UI bottom field memory block low address register(N=0,1,2,3)

OVL_UI_FILL_COLOR	0x018 + N*0x20	OVL_UI fill color register(N=0,1,2,3)
OVL_UI_TOP_HADD	0x080	OVL_UI top field memory block high address register
OVL_UI_BOT_HADD	0x084	OVL_UI bottom field memory block high address register
OVL_UI_SIZE	0x088	OVL_UI overlay window size register
/	0x8C~0xEC	/
OVL_UI_HDS_CTL	0x0F0	OVL_UI horizontal down sample control register
/	0x0F4	/
OVL_UI_VDS_CTL	0x0F8	OVL_UI vertical down sample control register
/	0xFC~0x2FC	/
FBD_UI_CTL	0x300	OVL_UI FBD control register
FBD_UI_STA	0x304	OVL_UI FBD status register
FBD_UI_SIZE	0x308	OVL_UI FBD image size register
FBD_UI_BLOCK_SIZE	0x30C	OVL_UI FBD block size register
FBD_UI_SRC_CROP	0x310	OVL_UI FBD source crop register
FBD_UI_OVL_CROP	0x314	OVL_UI FBD overlay crop register
FBD_UI_FMT	0x318	OVL_UI FBD input format register
/	0x31C	/
FBD_UI_HD_LADDR	0x320	OVL_UI FBD header low address register
FBD_UI_HD_HADDR	0x324	OVL_UI FBD header high address register
FBD_UI_PL_LADDR	0x328	OVL_UI FBD payload low address register
FBD_UI_PL_HADDR	0x32C	OVL_UI FBD payload high address register
FBD_UI_OVL_SIZE	0x330	OVL_UI FBD overlay window size register
FBD_UI_COOR	0x334	OVL_UI FBD memory block coordinate register
FBD_UI_BGC	0x338	OVL_UI FBD memory block coordinate register
FBD_UI_FC	0x33C	OVL_UI FBD overlay window size register
OVL_UI_FBD_DBG0	0x340	OVL_UI FBD dbg0 register
OVL_UI_FBD_DBG1	0x344	OVL_UI FBD dbg1 register
OVL_UI_FBD_DBG2	0x348	OVL_UI FBD dbg2 register
OVL_UI_FBD_DBG3	0x34C	OVL_UI FBD dbg3 register
/	0x350~0x37C	/
OVL_UI_FBD_BIST_STATUS	0x380	OVL_UI FBD bist register
OVL_UI_FBD_BIST_START_ADDR	0x384	OVL_UI FBD bist start address register
OVL_UI_FBD_BIST_START_ADDR	0x388	OVL_UI FBD bist end address register
OVL_UI_FBD_BIST_MARK	0x38C	OVL_UI FBD bist data mark register
BLD_ENABLE_CTL	0x000	BLD enable color control register
BLD_FILL_COLOR	0x004 + N*0x14	BLD fill color register(N=0,1,2,3,4)
BLD_CH_ISIZE	0x008 + N*0x14	BLD input memory size register(N=0,1,2,3,4)
BLD_CH_OFFSET	0x00C + N*0x14	BLD input memory offset register(N=0,1,2,3,4)
BLD_CH_RTCTL	0x080	BLD routing control register
BLD_PREMUL_CTL	0x084	BLD pre-multiply control register
BLD_BK_COLOR	0x088	BLD background color register
BLD_SIZE	0x08C	BLD output size setting register
BLD_CTL0	0x090	BLD control register0
BLD_CTL1	0x094	BLD control register1

BLD_CTL2	0x098	BLD control register2
BLD_CTL3	0x09C	BLD control register3
BLD_KEY_CTL	0x0B0	BLD color key control register
BLD_KEY_CON	0x0B4	BLD color key configuration register
BLD_KEY_MAX0	0x0C0	BLD color key max register0
BLD_KEY_MAX1	0x0C4	BLD color key max register1
BLD_KEY_MAX2	0x0C8	BLD color key max register2
BLD_KEY_MAX3	0x0CC	BLD color key max register3
BLD_KEY_MIN0	0x0E0	BLD color key min register0
BLD_KEY_MIN1	0x0E4	BLD color key min register1
BLD_KEY_MIN2	0x0E8	BLD color key min register2
BLD_KEY_MIN3	0x0EC	BLD color key min register3
BLD_OUT_COLOR	0x0FC	BLD output color control register
BLD_CSC_CTL	0x100	BLD color space control register
BLD_CSC0_COEFF00	0x110	BLD csc0 coeff0 register0
BLD_CSC0_COEFF01	0x114	BLD csc0 coeff0 register1
BLD_CSC0_COEFF02	0x118	BLD csc0 coeff0 register2
BLD_CSC0_CONST0	0x11C	BLD csc0 const0 register
BLD_CSC0_COEFF10	0x120	BLD csc0 coeff1 register0
BLD_CSC0_COEFF11	0x124	BLD csc0 coeff1 register1
BLD_CSC0_COEFF12	0x128	BLD csc0 coeff1 register2
BLD_CSC0_CONST1	0x12C	BLD csc0 const1 register
BLD_CSC0_COEFF20	0x130	BLD csc0 coeff2 register0
BLD_CSC0_COEFF21	0x134	BLD csc0 coeff2 register1
BLD_CSC0_COEFF22	0x138	BLD csc0 coeff2 register2
BLD_CSC0_CONST2	0x13C	BLD csc0 const2 register
BLD_CSC1_COEFF00	0x140	BLD csc0 coeff0 register0
BLD_CSC1_COEFF01	0x144	BLD csc0 coeff0 register1
BLD_CSC1_COEFF02	0x148	BLD csc0 coeff0 register2
BLD_CSC1_CONST0	0x14C	BLD csc1 const0 register
BLD_CSC1_COEFF10	0x150	BLD csc0 coeff1 register0
BLD_CSC1_COEFF11	0x154	BLD csc0 coeff1 register1
BLD_CSC1_COEFF12	0x158	BLD csc0 coeff1 register2
BLD_CSC1_CONST1	0x15C	BLD csc1 const1 register
BLD_CSC1_COEFF20	0x160	BLD csc0 coeff2 register0
BLD_CSC1_COEFF21	0x164	BLD csc0 coeff2 register1
BLD_CSC1_COEFF22	0x168	BLD csc0 coeff2 register2
BLD_CSC1_CONST2	0x16C	BLD csc1 const2 register
BLD_CSC2_COEFF00	0x170	BLD csc2 coeff0 register0
BLD_CSC2_COEFF01	0x174	BLD csc2 coeff0 register1
BLD_CSC2_COEFF02	0x178	BLD csc2 coeff0 register2
BLD_CSC2_CONST0	0x17C	BLD csc2 const0 register
BLD_CSC2_COEFF10	0x180	BLD csc2 coeff1 register0
BLD_CSC2_COEFF11	0x184	BLD csc2 coeff1 register1
BLD_CSC2_COEFF12	0x188	BLD csc2 coeff1 register2

BLD_CSC2_CONST1	0x18C	BLD csc2 const1 register
BLD_CSC2_COEFF20	0x190	BLD csc2 coeff2 register0
BLD_CSC2_COEFF21	0x194	BLD csc2 coeff2 register1
BLD_CSC2_COEFF22	0x198	BLD csc2 coeff2 register2
BLD_CSC2_CONST2	0x19C	BLD csc2 const2 register
BLD_CSC3_COEFF00	0x1A0	BLD csc3 coeff0 register0
BLD_CSC3_COEFF01	0x1A4	BLD csc3 coeff0 register1
BLD_CSC3_COEFF02	0x1A8	BLD csc3 coeff0 register2
BLD_CSC3_CONST0	0x1AC	BLD csc3 const0 register
BLD_CSC3_COEFF10	0x1B0	BLD csc3 coeff1 register0
BLD_CSC3_COEFF11	0x1B4	BLD csc3 coeff1 register1
BLD_CSC3_COEFF12	0x1B8	BLD csc3 coeff1 register2
BLD_CSC3_CONST1	0x1BC	BLD csc3 const1 register
BLD_CSC3_COEFF20	0x1C0	BLD csc3 coeff2 register0
BLD_CSC3_COEFF21	0x1C4	BLD csc3 coeff2 register1
BLD_CSC3_COEFF22	0x1C8	BLD csc3 coeff2 register2
BLD_CSC3_CONST2	0x1CC	BLD csc3 const2 register
/	0x1D0~0x1EC	/
BLD_CSC0_APHA	0x1F0	BLD csc0 alpha register
BLD_CSC1_APHA	0x1F4	BLD csc1 alpha register
BLD_CSC2_APHA	0x1F8	BLD csc2 alpha register
BLD_CSC3_APHA	0x1FC	BLD csc3 alpha register

3.11.6 GLB Register Description

Note: all registers in GLB are not double buffer.

3.11.6.1 Global control register

3.11.6.2 Global control register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: GLB_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	**OUT_DATA_WB** Output data for **RT-WB** 0x0:**RT-WB** fetch data after **DEP** port 0x1:**RT-WB** fetch data before **DEP** port Other: Reserved
11:10	/	/	/
9	R/W	0x0	lcd flied in reverse
8	R/W	0x0	lcd sync in reverse
7:6	/	/	/
5	R/W1C	0x0	**ERROR_IRQ_EN** Hardware error IRQ enable 0x0:disable

			0x1:enable
4	R/W1C	0x0	**FINISH_IRQ_EN** Mission finish IRQ enable 0x0:disable 0x1:enable
3:1	/	/	/
0	R/W	0x0	**EN** RT enable/disable 0x0: disable 0x1: enable

3.11.6.3 Global status register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name:GLB_STS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R	0x0	**EVEN_ODD** 0x0: even field 0x1: odd field This bit is the flag for output data in interlace mode
7:6	/	/	/
5	R	0x0	**ERROR** Hardware error status
4	R	0x0	**BUSY** Module working status 0x0:idle 0x1:running busy
3:2	/	/	/
1	R/W	0x0	**ERROR_IRQ** Hardware error IRQ It will be set when hardware error occur, and cleared by writing 1.
0	R/W	0x0	**FINISH_IRQ** Mission finish IRQ It will be set when 1 frame operation accomplished, and cleared by writing 1.

3.11.6.4 Global double buffer control register(Default Value: 0x0000_0000)

Offset: 0x0008			**Register Name: GLB_DBUFFER**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	**DOUBLE_BUFFER_RDY** 0x0: no change 0x1: register value be ready for update Note:This bit is self-cleared by writing 1 after update.

3.11.6.5 Global size register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: GLB_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**HEIGHT** Height The Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** Width The Width = The value of these bits add 1

3.11.6.6 Global de-interlace control register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GLB_DI_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DI_CTL 0x0: DI disable 0x1: DI enable Note: if DI enable, VSU use DI data, otherwise use overlay data. This bits is double buffer.

3.11.6.7 Global auto-clock-gate control register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GLB_AUTO_CLOCK_GATE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	AUTO_CLOCK_GATE 0x0: Disable 0x1: Enable Note: if AUTO_CLOCK_GATE = 1, core clock of RTD module will be gated before LCD fetch data in each frame.

3.11.7 OVL_V Register Description

Note: all registers in OVL_V are double buffer.

3.11.7.1 OVL_V attribute control register(Default Value: 0x0000_0000)

Offset: 0x0000+N*0x30(N=0,1,2,3)			Register Name: OVL_V_ATTCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY_GLBALPHA** Globe alpha value Alpha value is used for this layer

23	R/W	0x0	**LAY0_TOP_BOTTOM_ADDR_EN** 0x0: disable 0x1: enable When this bit is disable the layer address use top field address in both top and bottom field, otherwise use the top and bottom field address separate in top and bottom field.
22	/	/	/
21:20	R/W	0x0	**LAY_BRUST_LENGTH** 0x0: brust4 0x1: brust8 0x2: brust16 0x3: brust32
19:18	/	/	/
17:16	R/W	0x0	**LAY_PREMUL_CTL** Layer input pre-multiply alpha control 0x0: Input layer data is non-pre-multiply data and it needn't to unify pre-multiply data. 0x1: Input layer data is non-pre-multiply data and it need to unify pre-multiply data. 0x2: pre-multiply input layer Other: Reserved
15	R/W	0x0	**Video_UI_SEL** Video Overlay or UI Overlay Select 0x0: Video Overlay(using **Video Overlay Layer Input data format**) 0x1: UI Overlay(using **UI Overlay Layer Input data format**)
14:13	/	/	/
12:8	R/W	0x0	**LAY_FBFMT** **UI Overlay Layer Input data format** 0x00: ARGB_8888 0x01: ABGR_8888 0x02: RGBA_8888 0x03: BGRA_8888 0x04: XRGB_8888 0x05: XBGR_8888 0x06: RGBX_8888 0x07: BGRX_8888 0x08: RGB_888 0x09: BGR_888 0x0A: RGB_565 0x0B: BGR_565 0x0C: ARGB_4444 0x0D: ABGR_4444 0x0E: RGBA_4444 0x0F: BGRA_4444 0x10: ARGB_1555 0x11: ABGR_1555

			0x12: RGBA_5551 0x13: BGRA_5551 0x14: A2R10G10B10 0x15: A2B10G10R10 0x16: R10G10B10A2 0x17: B10G10R10A2 Other: Reserved **Video Overlay Layer Input data format** 0x00: Interleaved YUV422(V0Y1U0Y0) 0x01: Interleaved YUV422(Y1V0Y0U0) 0x02: Interleaved YUV422(U0Y1V0Y0) 0x03: Interleaved YUV422(Y1U0Y0V0) 0x04: Planar YUV422 UV combined(V1U1V0U0) 0x05: Planar YUV422 UV combined(U1V1U0V0) 0x06: Planar YUV422 0x07: Reserved 0x08: Planar YUV420 UV combined(V1U1V0U0-NV12) 0x09: Planar YUV420 UV combined(U1V1U0V0) 0x0A: Planar YUV420(YV12) 0x0B: Reserved 0x0C: Planar YUV411 UV combined(V1U1V0U0) 0x0D: Planar YUV411 UV combined(U1V1U0V0) 0x0E: Planar YUV411 0x0F: Reserved 0x10: YVU10_420_2PLANE(P010) 0x11: YUV10_420_2PLANE(P010) 0x12: YVU10_422_2PLANE(P210) 0x13: YUV10_422_2PLANE(P210) 0x14: YVU10_444_1PLANE 0x15: YUV10_444_1PLANE Other: Reserved All video layers must be the same format, programmer should confirm it.
7:5	/	/	/
4	R/W	0x0	**LAY_FILLCOLOR_EN** 0x0: disable 0x1:enable When the layer fill-color is enabled, the layer data will use the fill-color.
3	/	/	/
2:1	R/W	0x0	**LAY_ALPHA_MODE** Layer input alpha mode 0x0:Ignore Input alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 0x1:Globe alpha enable Ignore pixel alpha value Input alpha value = globe alpha value

			0x2: Globe alpha mix pixel alpha Input alpha value = globe alpha value * pixels alpha value 0x3:Reserved
0	R/W	0x0	**LAY0_EN** Layer0 enable/disable 0x0: disabled 0x1: enabled

Note: the layer priority is layer3>layer2>layer1>layer0

3.11.7.2 OVL_V memory block size register(Default Value: 0x0000_0000)

Offset: 0x0004+N*0x30(N=0,1,2,3)			Register Name: OVL_V_MBSIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**LAY_HEIGHT** Layer Height The Layer Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**LAY_WIDTH** Layer Width The Layer Width = The value of these bits add 1

3.11.7.3 OVL_V memory block coordinate register(Default Value: 0x0000_0000)

Offset: 0x0008+N*0x30(N=0,1,2,3)			Register Name: OVL_V_COOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	**LAY_YCOOR** Y coordinate Y is the left-top y coordinate of layer on overlay window in pixels
15:0	R/W	0x0	**LAY_XCOOR** X coordinate X is left-top x coordinate of the layer on overlay window in pixels

Setting the layer0-layer3 the coordinate (left-top) on overlay window control information

3.11.7.4 OVL_V memory pitch register0(Default Value: 0x0000_0000)

Offset: 0x000C+N*0x30(N=0,1,2,3)			Register Name: OVL_V_PITCH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAY_PITCH** Layer memory pitch in bytes

Note: The setting of this register is Y channel.

3.11.7.5 OVL_V memory pitch register1(Default Value: 0x0000_0000)

Offset: 0x0010+N*0x30(N=0,1,2,3)			Register Name: OVL_V_PITCH1
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	**LAY_PITCH** Layer memory pitch in bytes

Note: The setting of this register is U/UV channel.

3.11.7.6 OVL_V memory pitch register2(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x30(N=0,1,2,3)			Register Name: OVL_V_PITCH2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAY_PITCH** Layer memory pitch in bytes

Note: The setting of this register is V channel.

3.11.7.7 OVL_V top field memory block low address register0(Default Value: 0x0000_0000)

Offset: 0x0018+N*0x30(N=0,1,2,3)			Register Name:OVL_V_TOP_LADD0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

Note: The setting of this register is Y channel address.

3.11.7.8 OVL_V top field memory block low address register1(Default Value: 0x0000_0000)

Offset: 0x001C+N*0x30(N=0,1,2,3)			Register Name:OVL_V_TOP_LADD1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

Note: The setting of this register is U/UV channel address.

3.11.7.9 OVL_V top field memory block low address register2(Default Value: 0x0000_0000)

Offset: 0x0020+N*0x30(N=0,1,2,3)			Register Name:OVL_V_TOP_LADD2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

Note: The setting of this register is V channel address.

3.11.7.10 OVL_V bottom field memory block low address register0(Default Value: 0x0000_0000)

Offset: 0x0024+N*0x30(N=0,1,2,3)			Register Name:OVL_V_BOT_LADD0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

Note: The setting of this register is Y channel address.

3.11.7.11 OVL_V bottom field memory block low address register1(Default Value: 0x0000_0000)

Offset: 0x0028+N*0x30(N=0,1,2,3)			Register Name:OVL_V_BOT_LADD1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

Note: The setting of this register is U/UV channel address.

3.11.7.12 OVL_V bottom field memory block low address register2(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x30(N=0,1,2,3)			Register Name:OVL_V_BOT_LADD2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

Note: The setting of this register is V channel address.

3.11.7.13 OVL_V fill color register(Default Value: 0x0000_0000)

Offset: 0x00C0+N*0x4(N=0,1,2,3)			Register Name:OVL_V_FILL_COLOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**Alpha** Alpha fill color value
23:16	R/W	0x0	**Y/R** Y/Red fill color value
15:8	R/W	0x0	**U/G** U/Green fill color value
7:0	R/W	0x0	**V/B** V/Blue fill color value

3.11.7.14 OVL_V top field memory block high address register0(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name:OVL_V_TOP_HADD0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1

			Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

Note: The setting of this register is Y channel address.

3.11.7.15 OVL_V top field memory block high address register1(Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name:OVL_V_TOP_HADD1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

Note: The setting of this register is U/UV channel address.

3.11.7.16 OVL_V top field memory block high address register2(Default Value: 0x0000_0000)

Offset: 0x00D8			Register Name:OVL_V_TOP_HADD2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

Note: The setting of this register is V channel address.

3.11.7.17 OVL_V bottom field memory block high address register0(Default Value: 0x0000_0000)

Offset: 0x00DC			Register Name:OVL_V_BOT_HADD0
Bit	**Read/Write**	**Default/Hex**	**Description**

31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

Note: The setting of this register is Y channel address.

3.11.7.18 OVL_V bottom field memory block high address register1(Default Value: 0x0000_0000)

Offset: 0x00E0			**Register Name:OVL_V_BOT_HADD1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

Note: The setting of this register is U/UV channel address.

3.11.7.19 OVL_V bottom field memory block high address register2(Default Value: 0x0000_0000)

Offset: 0x00E4			**Register Name:OVL_V_BOT_HADD2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD**

			Layer0 Layer Memory Block Address in bytes

Note: The setting of this register is V channel address.

3.11.7.20 OVL_V overlay window size register(Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name:OVL_V_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**HEIGHT** Overlay Height The Overlay Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** Overlay Width The Overlay Width = The value of these bits add 1

when all the layers are disable the overlay has no output data, and by pass.

3.11.7.21 OVL_V horizontal down sampling control register0(Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name:OVL_V_HDS_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x0	**N** The step size for overlay data fetch. Note: Refer to "Figure 1-6 Video overlay data fetch rule"
15:14	/	/	/
13:0	R/W	0x0	**M** The counter threshold for fetch data Note: Refer to "Figure 1-6 Video overlay data fetch rule"

The setting of this register is Y channel.

3.11.7.22 OVL_V horizontal down sampling control register1(Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name:OVL_V_HDS_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x0	**N** The step size for overlay data fetch. Note: Refer to "Figure 1-6 Video overlay data fetch rule"
15:14	/	/	/
13:0	R/W	0x0	**M** The counter threshold for fetch data Note: Refer to "Figure 1-6 Video overlay data fetch rule"

The setting of this register is UV channel.

3.11.7.23 OVL_V vertical down sampling control register0(Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name:OVL_V_VDS_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x0	**N** The step size for overlay data fetch. Note: Refer to "Figure 1-6 Video overlay data fetch rule"
15:14	/	/	/
13:0	R/W	0x0	**M** The counter threshold for fetch data Note: Refer to "Figure1-6 Video overlay data fetch rule"

The setting of this register is Y channel.

3.11.7.24 OVL_V vertical down sampling control register1(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name:OVL_V_VDS_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x0	**N** The step size for overlay data fetch. Note: Refer to "Figure1-6 Video overlay data fetch rule"
15:14	/	/	/
13:0	R/W	0x0	**M** The counter threshold for fetch data Note: Refer to "Figure 1-6 Video overlay data fetch rule"

The setting of this register is UV channel.

3.11.7.25 OVL_V FBD control register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name:FBD_V_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**GLB_A** Global alpha value
23:5	/	/	**/**
4	R/W	0x0	**CLK_GATE** 0x0: disable 0x1: enable
3:2	R/W	0x0	**LAY_ALPHA_MODE** Layer input alpha mode 0x0:Ignore Input alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 0x1:Globe alpha enable Ignore pixel alpha value Input alpha value = globe alpha value

			0x2: Globe alpha mix pixel alpha Input alpha value = globe alpha value * pixels alpha value 0x3:Reserved
1	R/W	0x0	**FBD_FCEN** 0x0: disable 0x1: enable, fill the layer area with data defined by register **OVL_FBD_FC**. And **STOP** decoding data from DRAM.
0	R/W	0x0	**FBD_EN** 0x0: disable 0x1: enable Note: If frame buffer decoder enable, channel data from FBD input, otherwise from normal overlay. FBD decoder will load all configurations to hardware and start decoding data when VSYNC signal comes. Change 1 to 0 will stop decoding after current frame finish.

FBD registers start +0x300 offset to each channel base, control the first layer input for each channel.

3.11.7.26 OVL_V FBD status register(Default Value: 0x0000_0000)

Offset: 0x0304			**Register Name:FBD_V_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	**XXX_ERR** Error Write 1 to clear this bit. 0x0: no error 0x1: error
1	R/W1C	0x0	**DEC_ERR** Any error will pause current decoding. Write 1 to clear this bit. 0x0: no error 0x1: error occurs when decoding one frame.
0	R	0x0	**FLAG** 0x0: Idle 0x1: decoding

3.11.7.27 OVL_V FBD image size register(Default Value: 0x0000_0000)

Offset: 0x0308			**Register Name:FBD_V_SIZE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	**HEIGHT** Compressed image height in units of pixels – 1
15:12	/	/	/
11:0	R/W	0x0	**WIDTH** Compressed image width in units of pixels – 1

FBD_SIZE is the real size after the layer crop from sourc image.

3.11.7.28 OVL_V FBD block size register(Default Value: 0x0000_0000)

Offset: 0x030C			Register Name:FBD_V_BLOCK_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	**BLOCK HEIGHT** The vertical mb size in units of 16 pixels
15:10	/	/	/
9:0	R/W	0x0	**BLOCK WIDTH** The horizontal mb size in units of 16 pixels

3.11.7.29 OVL_V FBD source crop register(Default Value: 0x0000_0000)

Offset: 0x0310			Register Name:FBD_V_SRC_CROP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	**TOP_CROP** How many pixels to crop to the top of the source compressed image. 0~15, normally 0.
15:4	/	/	/
3:0	R/W	0x0	**LEFT_CROP** How many pixels to crop to the left of the source compressed image. 0~15, normally 0.

3.11.7.30 OVL_V FBD layer crop register(Default Value: 0x0000_0000)

Offset: 0x0314			Register Name:FBD_V_LAY_CROP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	**LAY_CROP_TOP** The top crop position of the decoded image
15:12	/	/	/
11:0	R/W	0x0	**LAY_CROP_LEFT** The left crop position of the decoded image

This register will control the block start position for layer crop function.

The block coordinates starts to decode is [(LAY_CROP_TOP+CROP_TOP)/16, (LAY_CROP_LEFT + CROP_TOP)/16].

The block inner start coordinates is [(LAY_CROP_TOP+CROP_TOP)%16, (LAY_CROP_LEFT + CROP_TOP)%16].

3.11.7.31 OVL_V FBD input format register(Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: FBD_V_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	**SBS1** Sub-block size 0~2: 1byte~3byte

17:16	R/W	0x0	**SBS0** Sub-block size 0~2: 1byte~3byte
15:8	/	/	/
7	R/W	0x0	**YUV_TRAN** Yuv transform enable 0x0: no transform 0x1: transform enabled for rgb format
6:0	R/W	0x0	**INFMT** FBD input format Used for internal overlay, not for decoding 0x02: RGBA_8888 0x08: RGB_888 0x0A: RGB_565 0x0E: RGBA_4444 0x12: RGBA_5551 0x16: R10G10B10A2 0x26: Planar YUV422 0x2A: Planar YUV420(YV12) 0x30: YVU10_420_2PLANE(P010) 0x32: YVU10_422_2PLANE(P210) others: reserved

3.11.7.32 OVL_V FBD header low address register(Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: FBD_V_HD_LADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**HD_LADDR** FBD header Start Address in byte

3.11.7.33 OVL_V FBD header high address register(Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: FBD_V_HD_HADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**HD_HADDR** FBD header Start Address in byte

3.11.7.34 OVL_V FBD overlay size register(Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: OVL_V_FBD_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**OVL_HEIGHT** The OVL Height = The value of these bits add 1
15:13	/	/	/

12:0	R/W	0x0	**OVL_WIDTH** The OVL Width = The value of these bits add 1

3.11.7.35 OVL_V FBD overlay coordinate register(Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: OVL_V_FBD_COOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**OVL_YCOOR** Y coordinate Y is the left-top y coordinate of layer on overlay window in pixels
15:13	/	/	/
12:0	R/W	0x0	**OVL_XCOOR** X coordinate X is left-top x coordinate of the layer on overlay window in pixels

Setting the coordinate (left-top) on overlay window control information

3.11.7.36 OVL_V FBD overlay BGC register(Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: OVL_V_FBD_BGC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_BGC** FBD overlay background color Data format is AP0P1P2, P0/1/2 corresponding to Y/U/V or R/G/B channel data in 8bit

Set the pixel value in the area outside the FB and inside the overlay.

3.11.7.37 OVL_V FBD overlay FC register(Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: OVL_V_FBD_FC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_FC** When FBD_FCEN=1, fill the FB area with FBD_FC data. Data format is AP0P1P2, P0/1/2 corresponding to Y/U/V or R/G/B channel data in 8bit

3.11.7.38 OVL_V FBD dbg0 register(Default Value: 0x0000_0000)

Offset: 0x0340			Register Name:OVL_V_FBD_DBG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**FBD_DBG** **Ch0 counter**

3.11.7.39 OVL_V FBD dbg1 register(Default Value: 0x0000_0000)

Offset: 0x0344	Register Name:OVL_V_FBD_DBG1

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	**FBD_DBG** **Ch1 counter**

3.11.7.40 OVL_V FBD dbg2 register(Default Value: 0x0000_0000)

Offset: 0x0348			Register Name:OVL_V_FBD_DBG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**FBD_DBG** **Ch2 counter**

3.11.7.41 OVL_V FBD dbg3 register(Default Value: 0x0000_0000)

Offset: 0x034C			Register Name:OVL_V_FBD_DBG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	**FBD_DBG** Block counter

OVL_FBD_DBG0~3 register only for debug use.

3.11.7.42 OVL_V FBD bist register(Default Value: 0x0000_0000)

Offset: 0x0380			Register Name:OVL_V_FBD_BIST_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	**BIST_ERR_STA.** BIST Error Status.
14:12	R	0x0	**BIST_ERR_PAT.** BIST Error Pattern.
11:10	R	0x0	**BIST_ERR_CYC.** BIST Error Cycle.
9	R	0x1	**BIST_STOP.** BIST Stop. 0: running 1: stop
8	R	0x0	**BIST_BUSY.** BIST Busy. 0: idle, 1: busy.
7:5	R/W	0x0	**BIST_REG_SEL.** BIST Register Select.
4	R/W	0x0	**BIST_ADDR_MODE_SEL.** BIST Address Mode Select.
3:1	R/W	0x0	**BIST_WDATA_PAT.** BIST Write Data Pattern. 000: 0x00000000 001: 0x55555555 010: 0x33333333 011: 0x0F0F0F0F

			100: 0x00FF00FF 101: 0x0000FFFF Others: reserved.
0	R/W	0x0	**BIST_EN** BIST Enable. A positive edge will trigger the BIST to start.

3.11.7.43 OVL_V FBD bist start address register(Default Value: 0x0000_0000)

Offset: 0x0384			Register Name:OVL_V_FBD_BIST_START_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**BIST_START_ADDR.** BIST Start Address. It is 4 bytes aligned.

3.11.7.44 OVL_V FBD bist end address register(Default Value: 0x0000_0000)

Offset: 0x0388			Register Name:OVL_V_FBD_BIST_END_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**BIST_END_ADDR.** BIST End Address. It is 4 bytes aligned.

3.11.7.45 OVL_V FBD bist mark register(Default Value: 0x0000_0000)

Offset: 0x038C			Register Name:OVL_V_FBD_BIST_MARK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**BIST_DATA_MASK.** BIST Data Mask. 0: unmask 1: mask.

For different bist space
0~800: mask=low 24bit
4000~4200: mask=low 26bit
8000~10000: mask=low 20bit
10000~18000: mask=low18bit

0~7ff: mask=ff000000
4000~41ff: mask=fc000000
8000~ffff: mask=fff00000
10000~17fff: mask=fffc0000

3.11.8 OVL_UI Register Description

Note: all registers in OVL_UI are double buffer.

3.11.8.1 OVL_UI attribute control register(Default Value: 0x0000_0000)

Offset: 0x0000+N*0x20(N=0,1,2,3)			Register Name: OVL_UI_ATTCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY_GLBALPHA** Globe alpha value Alpha value is used for this layer
23	R/W	0x0	**TOP_BOTTOM_ADDR_EN** 0x0: disable 0x1: enable When this bit is disable the layer address use top field address in both top and bottom field, otherwise use the top and bottom field address separate in top and bottom field.
22	/	/	/
21:20	R/W	0x0	**LAY_BRUST_LENGTH** 0x0: brust4 0x1: brust8 0x2: brust16 0x3: brust32
19:18	/	/	/
17:16	R/W	0x0	**LAY_PREMUL_CTL** Layer input pre-multiply alpha control 0x0: Input layer data is non-pre-multiply data and it needn't to unify pre-multiply data. 0x1: Input layer data is non-pre-multiply data and it need to unify pre-multiply data. 0x2: pre-multiply input layer Other: Reserved
15:13	/	/	/
12:8	R/W	0x0	**LAY_FBFMT** Input data format 0x00: ARGB_8888 0x01: ABGR_8888 0x02: RGBA_8888 0x03: BGRA_8888 0x04: XRGB_8888 0x05: XBGR_8888 0x06: RGBX_8888 0x07: BGRX_8888 0x08: RGB_888 0x09: BGR_888 0x0A: RGB_565 0x0B: BGR_565 0x0C: ARGB_4444 0x0D: ABGR_4444 0x0E: RGBA_4444 0x0F: BGRA_4444

			0x10: ARGB_1555 0x11: ABGR_1555 0x12: RGBA_5551 0x13: BGRA_5551 Other: Reserved
7:5	/	/	/
4	R/W	0x0	**LAY_FILLCOLOR_EN** 0x0: disable 0x1:enable When the layer fill-color is enabled, the layer data will use the fill-color.
3	/	/	/
2:1	R/W	0x0	**LAY_ALPHA_MODE** Layer input alpha mode 0x0:Ignore Input alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 0x1:Globe alpha enable Ignore pixel alpha value Input alpha value = globe alpha value 0x2: Globe alpha mix pixel alpha Input alpha value = globe alpha value * pixels alpha value others:Reserved
0	R/W	0x0	**LAY_EN** Layer enable/disable 0x0: disabled 0x1: enabled

Note: the layer priority is layer3>layer2>layer1>layer0

3.11.8.2 OVL_UI memory block size register(Default Value: 0x0000_0000)

Offset: 0x0004+N*0x20(N=0,1,2,3)			**Register Name: OVL_UI_MBSIZE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**LAY_HEIGHT** Layer Height The Layer Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**LAY_WIDTH** Layer Width The Layer Width = The value of these bits add 1

3.11.8.3 OVL_UI memory block coordinate register(Default Value: 0x0000_0000)

Offset: 0x0008+N*0x20(N=0,1,2,3)			**Register Name: OVL_UI_COOR**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0x0	**LAY_YCOOR** Y coordinate Y is the left-top y coordinate of layer on overlay window in pixels
15:0	R/W	0x0	**LAY_XCOOR** X coordinate X is left-top x coordinate of the layer on overlay window in pixels

Setting the layer0-layer3 the coordinate (left-top) on overlay window control information

3.11.8.4 OVL_UI memory pitch register(Default Value: 0x0000_0000)

Offset: 0x000C+N*0x20(N=0,1,2,3)			Register Name: OVL_UI_PITCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAY_PITCH** Layer memory pitch in bytes

3.11.8.5 OVL_UI top field memory block low address register(Default Value: 0x0000_0000)

Offset: 0x0010+N*0x20(N=0,1,2,3)			Register Name: OVL_UI_TOP_LADD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

3.11.8.6 OVL_UI bottom field memory block low address register(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x20(N=0,1,2,3)			Register Name: OVL_UI_BOT_LADD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**LAYMB_LADD** Memory Block Start Address Layer Memory Block Address in bytes

3.11.8.7 OVL_UI fill color register(Default Value: 0x0000_0000)

Offset: 0x0018+N*0x20(N=0,1,2,3)			Register Name: OVL_UI_FILL_COLOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**Alpha** Alpha fill color value
23:16	R/W	0x0	**RED** Red fill color value
15:8	R/W	0x0	**GREEN** Green fill color value
7:0	R/W	0x0	**BLUE** Blue fill color value

3.11.8.8 OVL_UI top field memory block high address register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: OVL_UI_TOP_HADD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

3.11.8.9 OVL_UI bottom field memory block high address register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: OVL_UI_BOT_HADD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**LAY3MB_HADD** Layer3 Layer Memory Block Address in bytes
23:16	R/W	0x0	**LAY2MB_HADD** Layer2 Layer Memory Block Address in bytes
15:8	R/W	0x0	**LAY1MB_HADD** Layer1 Layer Memory Block Address in bytes
7:0	R/W	0x0	**LAY0MB_HADD** Layer0 Layer Memory Block Address in bytes

3.11.8.10 OVL_UI overlay window size register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: OVL_UI_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**HEIGHT** Overlay Height The Overlay Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** Overlay Width The Overlay Width = The value of these bits add 1

When all the layers are disable the overlay has no output data, and by pass.

3.11.8.11 OVL_UI horizontal down sampling control register(Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: OVL_UI_HDS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x0	**N** The step size for overlay data fetch. Note: Refer to "Figure 6 Video overlay data fetch rule"
15:14	/	/	/
13:0	R/W	0x0	**M** The counter threshold for fetch data Note: Refer to "Figure 6 Video overlay data fetch rule"

3.11.8.12 OVL_UI vertical down sampling control register(Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: OVL_UI_VDS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x0	**N** The step size for overlay data fetch. Note: Refer to "Figure 6 Video overlay data fetch rule"
15:14	/	/	/
13:0	R/W	0x0	**M** The counter threshold for fetch data Note: Refer to "Figure 6 Video overlay data fetch rule"

3.11.8.13 OVL_UI FBD control register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name:FBD_UI_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**GLB_A** Global alpha value
23:4	/	/	/
3:2	R/W	0x0	**LAY_ALPHA_MODE** Layer input alpha mode 0x0:Ignore Input alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 0x1:Globe alpha enable Ignore pixel alpha value Input alpha value = globe alpha value 0x2: Globe alpha mix pixel alpha Input alpha value = globe alpha value * pixels alpha value

			others:Reserved
1	R/W	0x0	**FBD_FCEN** 0x0: disable 0x1: enable, fill the layer area with data defined by register **OVL_FBD_FC**. And **STOP** decoding data from DRAM.
0	R/W	0x0	**FBD_EN** 0x0: disable 0x1: enable Note: If frame buffer decoder enable, channel data from FBD input, otherwise from normal overlay. FBD decoder will load all configurations to hardware and start decoding data when VSYNC signal comes. Change 1 to 0 will stop decoding after current frame finish.

FBD registers start +0x300 offset to each channel base, control the first layer input for each channel.

3.11.8.14 OVL_UI FBD status register(Default Value: 0x0000_0000)

Offset: 0x0304			**Register Name: FBD_UI_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	**XXX_ERR** Error Write 1 to clear this bit. 0x0: no error 0x1: error
1	R/W1C	0x0	**DEC_ERR** Any error will pause current decoding. Write 1 to clear this bit. 0x0: no error 0x1: error occurs when decoding one frame.
0	R	0x0	**FLAG** 0x0: Idle 0x1: decoding

3.11.8.15 OVL_UI FBD image size register(Default Value: 0x0000_0000)

Offset: 0x0308			**Register Name: FBD_UI_SIZE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	**HEIGHT** Compressed image height in units of pixels – 1
15:12	/	/	/
11:0	R/W	0x0	**WIDTH** Compressed image width in units of pixels – 1

FBD_SIZE is the real size after the layer crop from source image

3.11.8.16 OVL_UI FBD block size register(Default Value: 0x0000_0000)

Offset: 0x030C			Register Name: FBD_UI_BLOCK_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	**BLOCK HEIGHT** The vertical mb size in units of 16 pixels
15:10	/	/	/
9:0	R/W	0x0	**BLOCK WIDTH** The horizontal mb size in units of 16 pixels

3.11.8.17 OVL_UI FBD source crop register(Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: FBD_UI_SRC_CROP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	**TOP_CROP** How many pixels to crop to the top of the source compressed image. 0~15, normally 0.
15:4	/	/	/
3:0	R/W	0x0	**LEFT_CROP** How many pixels to crop to the left of the source compressed image. 0~15, normally 0.

3.11.8.18 OVL_UI FBD layer crop register(Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: FBD_UI_LAY_CROP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	**LAY_CROP_TOP** The top crop position of the decoded image
15:12	/	/	/
11:0	R/W	0x0	**LAY_CROP_LEFT** The left crop position of the decoded image

This register will control the block start position for layer crop function.

The block coordinates starts to decode is [(LAY_CROP_TOP+CROP_TOP)/16, (LAY_CROP_LEFT + CROP_TOP)/16].

The block inner start coordinates is [(LAY_CROP_TOP+CROP_TOP)%16, (LAY_CROP_LEFT + CROP_TOP)%16].

3.11.8.19 OVL_UI FBD input format register(Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: FBD_UI_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	**SBS1** Sub-block size 0~2: 1byte~3byte
17:16	R/W	0x0	**SBS0**

			Sub-block size 0~2: 1byte~3byte
15:8	/	/	/
7	R/W	0x0	**YUV_TRAN** Yuv transform enable 0x0: no transform 0x1: transform enabled for rgb format
6:0	R/W	0x0	**INFMT** FBD input format Used for internal overlay, not for decoding 0x02: RGBA_8888 0x08: RGB_888 0x0A: RGB_565 0x0E: RGBA_4444 0x12: RGBA_5551 0x16: R10G10B10A2 0x26: Planar YUV422 0x2A: Planar YUV420(YV12) 0x30: YVU10_420_2PLANE(P010) 0x32: YVU10_422_2PLANE(P210) others: reserved

3.11.8.20 OVL_UI FBD header low address register(Default Value: 0x0000_0000)

Offset: 0x0320			**Register Name: FBD_UI_HD_LADDR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**HD_LADDR** FBD header Start Address in byte

3.11.8.21 OVL_UI FBD header high address register(Default Value: 0x0000_0000)

Offset: 0x0324			**Register Name: FBD_UI_HD_HADDR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	**HD_HADDR** FBD header Start Address in byte

3.11.8.22 OVL_UI FBD overlay size register(Default Value: 0x0000_0000)

Offset: 0x0330			**Register Name: OVL_UI_FBD_SIZE**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**OVL_HEIGHT** The OVL Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**OVL_WIDTH**

			The OVL Width = The value of these bits add 1

3.11.8.23 OVL_UI FBD overlay coordinate register(Default Value: 0x0000_0000)

Offset: 0x0334			Register Name: OVL_UI_FBD_COOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**OVL_YCOOR** Y coordinate Y is the left-top y coordinate of layer on overlay window in pixels
15:13	/	/	/
12:0	R/W	0x0	**OVL_XCOOR** X coordinate X is left-top x coordinate of the layer on overlay window in pixels

Setting the coordinate (left-top) on overlay window control information

3.11.8.24 OVL_UI FBD overlay BGC register(Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: OVL_UI_FBD_BGC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_BGC** FBD overlay background color Data format is AP0P1P2, P0/1/2 corresponding to Y/U/V or R/G/B channel data in 8bit

Set the pixel value in the area outside the FB and inside the overlay.

3.11.8.25 OVL_UI FBD overlay FC register(Default Value: 0x0000_0000)

Offset: 0x033C			Register Name: OVL_UI_FBD_FC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_FC** When FBD_FCEN=1, fill the FB area with FBD_FC data. Data format is AP0P1P2, P0/1/2 corresponding to Y/U/V or R/G/B channel data in 8bit

3.11.8.26 OVL_UI FBD dbg0 register(Default Value: 0x0000_0000)

Offset: 0x0340			Register Name:OVL_UI_FBD_DBG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_DBG** **Ch0 counter**

3.11.8.27 OVL_UI FBD dbg1 register(Default Value: 0x0000_0000)

Offset: 0x0344			Register Name:OVL_UI_FBD_DBG1
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	**FBD_DBG** **Ch1 counter**

3.11.8.28 OVL_UI FBD dbg2 register(Default Value: 0x0000_0000)

Offset: 0x0348			**Register Name:OVL_UI_FBD_DBG2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_DBG** **Ch2 counter**

3.11.8.29 OVL_UI FBD dbg3 register(Default Value: 0x0000_0000)

Offset: 0x034C			**Register Name:OVL_UI_FBD_DBG3**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**FBD_DBG** Block counter

OVL_FBD_DBG0~3 register only for debug use.

3.11.8.30 OVL_UI FBD bist register(Default Value: 0x0000_0000)

Offset: 0x0380			**Register Name:OVL_UI_FBD_BIST_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	**BIST_ERR_STA.** BIST Error Status.
14:12	R	0x0	**BIST_ERR_PAT.** BIST Error Pattern.
11:10	R	0x0	**BIST_ERR_CYC.** BIST Error Cycle.
9	R	0x1	**BIST_STOP.** BIST Stop. 0: running 1: stop
8	R	0x0	**BIST_BUSY.** BIST Busy. 0: idle, 1: busy.
7:5	R/W	0x0	**BIST_REG_SEL.** BIST Register Select.
4	R/W	0x0	**BIST_ADDR_MODE_SEL.** BIST Address Mode Select.
3:1	R/W	0x0	**BIST_WDATA_PAT.** BIST Write Data Pattern. 000: 0x00000000 001: 0x55555555 010: 0x33333333 011: 0x0F0F0F0F 100: 0x00FF00FF

			101: 0x0000FFFF Others: reserved.
0	R/W	0x0	**BIST_EN** BIST Enable. A positive edge will trigger the BIST to start.

3.11.8.31 OVL_UI FBD bist start address register(Default Value: 0x0000_0000)

Offset: 0x0384			Register Name:OVL_UI_FBD_BIST_START_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**BIST_START_ADDR.** BIST Start Address. It is 4 bytes aligned.

3.11.8.32 OVL_UI FBD bist end address register(Default Value: 0x0000_0000)

Offset: 0x0388			Register Name:OVL_UI_FBD_BIST_END_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**BIST_END_ADDR.** BIST End Address. It is 4 bytes aligned.

3.11.8.33 OVL_UI FBD bist mark register(Default Value: 0x0000_0000)

Offset: 0x038C			Register Name:OVL_UI_FBD_BIST_MARK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**BIST_DATA_MASK.** BIST Data Mask. 0: unmask 1: mask.

Channel2~4 register definition is same as OVL_UI's register definition.

3.11.9 BLD Register Description

Note: all registers in BLD are double buffer.

3.11.9.1 BLD enable color control register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: BLD_EN_COLOR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	**P4_EN** Pipe4 enable/disable 0x0: disabled 0x1: enabled
11	R/W	0x0	**P3_EN** Pipe3 enable/disable 0x0: disabled

			0x1: enabled
10	R/W	0x0	**P2_EN** Pipe2 enable/disable 0x0: disabled 0x1: enabled
9	R/W	0x0	**P1_EN** Pipe1 enable/disable 0x0: disabled 0x1: enabled
8	R/W	0x0	**P0_EN** Pipe0 enable/disable 0x0: disabled 0x1: enabled
7:5	/	/	/
4	R/W	0x0	**P4_FCEN** Pipe4 fill color enable/disable 0x0: disabled 0x1: enabled
3	R/W	0x0	**P3_FCEN** Pipe3 fill color enable/disable 0x0: disabled 0x1: enabled
2	R/W	0x0	**P2_FCEN** Pipe2 fill color enable/disable 0x0: disabled 0x1: enabled
1	R/W	0x0	**P1_FCEN** Pipe1 fill color enable/disable 0x0: disabled 0x1: enabled
0	R/W	0x0	**P0_FCEN** Pipe0 fill color enable/disable 0x0: disabled 0x1: enabled

3.11.9.2 BLD fill color register(Default Value: 0x0000_0000)

Offset: 0x0004+N*0x10(N=0,1,2,3,4)			**Register Name: BLD_FILL_COLOR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	**Alpha** Alpha fill color value
23:16	R/W	0x0	**RED** Red fill color value
15:8	R/W	0x0	**GREEN** Green fill color value
7:0	R/W	0x0	**BLUE**

			Blue fill color value

3.11.9.3 BLD input memory size register(Default Value: 0x0000_0000)

Offset: 0x0008+N*0x10(N=0,1,2,3,4)			Register Name: BLD_CH_ISIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**HEIGHT** Pipe input memory height The input height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** Pipe input memory width The input width = The value of these bits add 1

3.11.9.4 BLD input memory offset register(Default Value: 0x0000_0000)

Offset: 0x000C+N*0x10(N=0,1,2,3,4)			Register Name: BLD_CH_OFFSET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	**YCOOR** Y coordinate Y is the left-top y coordinate of the pipe on blender memory window in pixels
15:0	R/W	0x0	**XCOOR** X coordinate X is the left-top x coordinate of the pipe on blender memory window in pixels

3.11.9.5 BLD routing control register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: BLD_CH_RTCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x3	**P3_RTCTL** Pipe3 select channel control 0x0:from channel0 0x1:from channel1 0x2:from channel2 0x3:from channel3 others: reserved
11:8	R/W	0x2	**P2_RTCTL** Pipe2 select channel control 0x0:from channel0 0x1:from channel1 0x2:from channel2 0x3:from channel3

			others: reserved
7:4	R/W	0x1	**P1_RTCTL** Pipe1 select channel control 0x0:from channel0 0x1:from channel1 0x2:from channel2 0x3:from channel3 others: reserved
3:0	R/W	0x0	**P0_RTCTL** Pipe0 select channel control 0x0:from channel0 0x1:from channel1 0x2:from channel2 0x3:from channel3 others: reserved

Note: Setting 2 or more channels in the same pipe is illegal, programmer should confirm it.

3.11.9.6 BLD pre-multiply control register(Default Value: 0x0000_0000)

Offset: 0x0084			**Register Name: BLD_PREMUL_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	**P3_ALPHA_MODE** Pipe3 input alpha mode 0x0:all alpha data is no-pre-multiply alpha 0x1:all alpha data is pre-multiply alpha
2	R/W	0x0	**P2_ALPHA_MODE** Pipe2 input alpha mode 0x0:all alpha data is no-pre-multiply alpha 0x1:all alpha data is pre-multiply alpha
1	R/W	0x0	**P1_ALPHA_MODE** Pipe1 input alpha mode 0x0:all alpha data is no-pre-multiply alpha 0x1:all alpha data is pre-multiply alpha
0	R/W	0x0	**P0_ALPHA_MODE** Pipe0 input alpha mode 0x0:all alpha data is no-pre-multiply alpha 0x1:all alpha data is pre-multiply alpha

3.11.9.7 BLD background color register(Default Value: 0x0000_0000)

Offset: 0x0088			**Register Name: BLD_BK_COLOR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**RED** Red background color value

15:8	R/W	0x0	**GREEN** Green background color value
7:0	R/W	0x0	**BLUE** Blue background color value

3.11.9.8 BLD output size setting register(Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: BLD_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**BLD_HEIGHT** Blender height The real blender height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	**BLD_WIDTH** Blender width The real blender width = The value of these bits add 1

3.11.9.9 BLD control register0(Default Value: 0x0301_0301)

Offset: 0x0090			Register Name: BLD_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	**BLEND_AFD** Specifies the coefficient that used in destination alpha data Q_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved
23:20	/	/	/
19:16	R/W	0x1	**BLEND_AFS** Specifies the coefficient that used in source alpha data Q_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved
15:12	/	/	/
11:8	R/W	0x3	**BLEND_PFD** Specifies the coefficient that used in destination pixel data F_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved

7:4	/	/	/
3:0	R/W	0x1	**BLEND_PFS** Specifies the coefficient that used in source pixel data F_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved

3.11.9.10 BLD control register1(Default Value: 0x0301_0301)

Offset: 0x0094			Register Name: BLD_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	**BLEND_AFD** Specifies the coefficient that used in destination alpha data Q_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved
23:20	/	/	/
19:16	R/W	0x1	**BLEND_AFS** Specifies the coefficient that used in source alpha data Q_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved
15:12	/	/	/
11:8	R/W	0x3	**BLEND_PFD** Specifies the coefficient that used in destination pixel data F_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved
7:4	/	/	/
3:0	R/W	0x1	**BLEND_PFS** Specifies the coefficient that used in source pixel data F_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved

3.11.9.11 BLD control register2(Default Value: 0x0301_0301)

Offset: 0x0098			Register Name: BLD_CTL2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	**BLEND_AFD** Specifies the coefficient that used in destination alpha data Q_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved
23:20	/	/	/
19:16	R/W	0x1	**BLEND_AFS** Specifies the coefficient that used in source alpha data Q_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved
15:12	/	/	/
11:8	R/W	0x3	**BLEND_PFD** Specifies the coefficient that used in destination pixel data F_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved
7:4	/	/	**/**
3:0	R/W	0x1	**BLEND_PFS** Specifies the coefficient that used in source pixel data F_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved

3.11.9.12 BLD control register3(Default Value: 0x0301_0301)

Offset: 0x009C			Register Name: BLD_CTL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	**BLEND_AFD** Specifies the coefficient that used in destination alpha data Q_d. 0x0: 0 0x1: 1

			0x2: A_s 0x3: 1-A_s others: Reserved
23:20	/	/	/
19:16	R/W	0x1	**BLEND_AFS** Specifies the coefficient that used in source alpha data Q_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved
15:12	/	/	/
11:8	R/W	0x3	**BLEND_PFD** Specifies the coefficient that used in destination pixel data F_d. 0x0: 0 0x1: 1 0x2: A_s 0x3: 1-A_s others: Reserved
7:4	/	/	**/**
3:0	R/W	0x1	**BLEND_PFS** Specifies the coefficient that used in source pixel data F_s. 0x0: 0 0x1: 1 0x2: A_d 0x3: 1-A_d others: Reserved

3.11.9.13 BLD color key control register(Default Value: 0x0000_0000)

Offset: 0x00B0			**Register Name: BLD_KEY_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	
14:13	R/W	0x0	**KEY3_MATCH_DIR** In Alpha Blender3 0x0: when the pixel value matches destination image, it displays the pixel form source image. 0x1: when the pixel value matches source image, it displays the pixel form destination image. others: Reserved
12	R/W	0x0	**KEY3_EN** Enable color key 0x0: disabled color key 0x1: enable color key in Alpha Blender3.
11	/	/	/
10:9	R/W	0x0	**KEY2_MATCH_DIR**

			In Alpha Blender2 0x0: when the pixel value matches destination image, it displays the pixel form source image. 0x1: when the pixel value matches source image, it displays the pixel form destination image. others: Reserved
8	R/W	0x0	**KEY2_EN** Enable color key 0x0: disabled color key 0x1: enable color key in Alpha Blender2.
7	/	/	
6:5	R/W	0x0	**KEY1_MATCH_DIR** In Alpha Blender1 0x0: when the pixel value matches destination image, it displays the pixel form source image. 0x1: when the pixel value matches source image, it displays the pixel form destination image. others: Reserved
4	R/W	0x0	**KEY1_EN** Enable color key 0x0: disabled color key 0x1: enable color key in Alpha Blender1.
3	/	/	
2:1	R/W	0x0	**KEY0_MATCH_DIR** In Alpha Blender0 0x0: when the pixel value matches destination image, it displays the pixel form source image. 0x1: when the pixel value matches source image, it displays the pixel form destination image. others: Reserved
0	R/W	0x0	**KEY0_EN** Enable color key 0x0: disabled color key 0x1: enable color key in Alpha Blender0.

3.11.9.14 BLD color key configuration register(Default Value: 0x0000_0000)

Offset: 0x00B4			**Register Name: BLD_KEY_CON**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	**KEY3R_MATCH** Red Match Rule 0x0: match if (Color Min=<Color<=Color Max) the red condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the red condition is true, else the condition is false.

25	R/W	0x0	**KEY3G_MATCH** Green Match Rule 0x0: match if (Color Min=<Color<=Color Max) the green condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the green condition is true, else the condition is false.
24	R/W	0x0	**KEY3B_MATCH** Blue Match Rule 0x0: match if (Color Min=<Color<=Color Max) the blue condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the blue condition is true, else the condition is false.
23:19	/	/	/
18	R/W	0x0	**KEY2R_MATCH** Red Match Rule 0x0: match if (Color Min=<Color<=Color Max) the red condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the red condition is true, else the condition is false.
17	R/W	0x0	**KEY2G_MATCH** Green Match Rule 0x0: match if (Color Min=<Color<=Color Max) the green condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the green condition is true, else the condition is false.
16	R/W	0x0	**KEY2B_MATCH** Blue Match Rule 0x0: match if (Color Min=<Color<=Color Max) the blue condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the blue condition is true, else the condition is false.
15:11	/	/	/
10	R/W	0x0	**KEY1R_MATCH** Red Match Rule 0x0: match if (Color Min=<Color<=Color Max) the red condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the red condition is true, else the condition is false.
9	R/W	0x0	**KEY1G_MATCH** Green Match Rule 0x0: match if (Color Min=<Color<=Color Max) the green condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the green condition is true, else the condition is false.
8	R/W	0x0	**KEY1B_MATCH** Blue Match Rule

			0x0: match if (Color Min=<Color<=Color Max) the blue condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the blue condition is true, else the condition is false.
7:3	/	/	/
2	R/W	0x0	**KEY0R_MATCH** Red Match Rule 0x0: match if (Color Min=<Color<=Color Max) the red condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the red condition is true, else the condition is false.
1	R/W	0x0	**KEY0G_MATCH** Green Match Rule 0x0: match if (Color Min=<Color<=Color Max) the green condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the green condition is true, else the condition is false.
0	R/W	0x0	**KEY0B_MATCH** Blue Match Rule 0x0: match if (Color Min=<Color<=Color Max) the blue condition is true, else the condition is false. 0x1: match if (Color>Color Max or Color<Color Min) the blue condition is true, else the condition is false.

Note: when R/G/B channel condition is true the color pass through otherwise is false.

3.11.9.15 BLD color key max register0(Default Value: 0x0000_0000)

Offset: 0x00C0			**Register Name: BLD_KEY_MAX0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MAX_R** Red Red color key max
15:8	R/W	0x0	**MAX_G** Green Green color key max
7:0	R/W	0x0	**MAX_B** Blue Blue color key max

3.11.9.16 BLD color key max register1(Default Value: 0x0000_0000)

Offset: 0x00C4			**Register Name: BLD_KEY_MAX1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MAX_R**

			Red Red color key max
15:8	R/W	0x0	**MAX_G** Green Green color key max
7:0	R/W	0x0	**MAX_B** Blue Blue color key max

3.11.9.17 BLD color key max register2(Default Value: 0x0000_0000)

Offset: 0x00C8			**Register Name: BLD_KEY_MAX2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MAX_R** Red Red color key max
15:8	R/W	0x0	**MAX_G** Green Green color key max
7:0	R/W	0x0	**MAX_B** Blue Blue color key max

3.11.9.18 BLD color key max register3(Default Value: 0x0000_0000)

Offset: 0x00CC			**Register Name: BLD_KEY_MAX3**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MAX_R** Red Red color key max
15:8	R/W	0x0	**MAX_G** Green Green color key max
7:0	R/W	0x0	**MAX_B** Blue Blue color key max

3.11.9.19 BLD color key min register0(Default Value: 0x0000_0000)

Offset: 0x00E0			**Register Name: BLD_KEY_MIN0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MIN_R** Red

			Red color key min
15:8	R/W	0x0	**MIN_G** Green Green color key min
7:0	R/W	0x0	**MIN_B** Blue Blue color key min

3.11.9.20 BLD color key min register1(Default Value: 0x0000_0000)

Offset: 0x00E4			**Register Name: BLD_KEY_MIN1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MIN_R** Red Red color key min
15:8	R/W	0x0	**MIN_G** Green Green color key min
7:0	R/W	0x0	**MIN_B** Blue Blue color key min

3.11.9.21 BLD color key min register2(Default Value: 0x0000_0000)

Offset: 0x00E8			**Register Name: BLD_KEY_MIN2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MIN_R** Red Red color key min
15:8	R/W	0x0	**MIN_G** Green Green color key min
7:0	R/W	0x0	**MIN_B** Blue Blue color key min

3.11.9.22 BLD color key min register3(Default Value: 0x0000_0000)

Offset: 0x00EC			**Register Name: BLD_KEY_MIN3**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	**MIN_R** Red Red color key min

15:8	R/W	0x0	**MIN_G** Green Green color key min
7:0	R/W	0x0	**MIN_B** Blue Blue color key min

3.11.9.23 BLD output color control register(Default Value: 0x0000_0000)

Offset: 0x00FC			**Register Name: BLD_OUT_COLOR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	**ITLMOD_EN** Output interlace mode enable 0x0:disable 0x1:enable When output interlace mode software programmer should confirm the blender output height is even.
0	R/W	0x0	**PREMUL_EN** Output color control 0x0: output normal data(A ' will be A_{abcde} ') 0x1: output pre-multiply data(A ' = 1)

3.11.9.24 BLD color space control register(Default Value: 0x0000_0000)

Offset: 0x0100			**Register Name: BLD_CSC_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**ALPHA_MODE** Alpha blending mode depending on the output format 0x0: alpha blending in **RGB** color space. 0x1: alpha blending in **YUV** color space.
7:4	/	/	/
3	R/W	0x0	**CSC3_EN** Enable channel3 color space transform 0x0:disable 0x1:enable
2	R/W	0x0	**CSC2_EN** Enable channel2 color space transform 0x0:disable 0x1:enable
1	R/W	0x0	**CSC1_EN** Enable channel1 color space transform 0x0:disable 0x1:enable
0	R/W	0x0	**CSC0_EN**

			Enable channel0 color space transform 0x0:disable 0x1:enable

3.11.9.25 BLD csc0 coeff0 register0(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: BLD_CSC0_COEFF00
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.26 BLD csc0 coeff0 register1(Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: BLD_CSC0_COEFF01
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.27 BLD csc0 coeff0 register2(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: BLD_CSC0_COEFF02
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.28 BLD csc0 const0 register(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: BLD_CSC0_CONST0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.29 BLD csc0 coeff1 register0(Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: BLD_CSC0_COEFF10
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.30 BLD csc0 coeff1 register1(Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: BLD_CSC0_COEFF11
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.31 BLD csc0 coeff1 register2(Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: BLD_CSC0_COEFF12
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.32 BLD csc0 const1 register(Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: BLD_CSC0_CONST1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.33 BLD csc0 coeff2 register0(Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: BLD_CSC0_COEFF20
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.34 BLD csc0 coeff2 register1(Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: BLD_CSC0_COEFF21
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.35 BLD csc0 coeff2 register2(Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: BLD_CSC0_COEFF22
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.36 BLD csc0 const2 register(Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: BLD_CSC0_CONST2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.37 BLD csc1 coeff0 register0(Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: BLD_CSC1_COEFF00
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.38 BLD csc1 coeff0 register1(Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: BLD_CSC1_COEFF01
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.39 BLD csc1 coeff0 register2(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: BLD_CSC1_COEFF02
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.40 BLD csc1 const0 register(Default Value: 0x0000_0000)

Offset: 0x014C	Register Name: BLD_CSC1_CONST0

Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.41 BLD csc1 coeff1 register0(Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: BLD_CSC1_COEFF10
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.42 BLD csc1 coeff1 register1(Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: BLD_CSC1_COEFF11
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.43 BLD csc1 coeff1 register2(Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: BLD_CSC1_COEFF12
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.44 BLD csc1 const1 register(Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: BLD_CSC1_CONST1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.45 BLD csc1 coeff2 register0(Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: BLD_CSC1_COEFF20
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.46 BLD csc1 coeff2 register1(Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: BLD_CSC1_COEFF21
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.47 BLD csc1 coeff2 register2(Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: BLD_CSC1_COEFF22
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.48 BLD csc1 const2 register(Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: BLD_CSC1_CONST2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.49 BLD csc2 coeff0 register0(Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: BLD_CSC2_COEFF00
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.50 BLD csc2 coeff0 register1(Default Value: 0x0000_0000)

Offset: 0x0174	Register Name: BLD_CSC2_COEFF01

Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.51 BLD csc2 coeff0 register2(Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: BLD_CSC2_COEFF02
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.52 BLD csc2 const0 register(Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: BLD_CSC2_CONST0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.53 BLD csc2 coeff1 register0(Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: BLD_CSC2_COEFF10
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.54 BLD csc2 coeff1 register1(Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: BLD_CSC2_COEFF11
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.55 BLD csc2 coeff1 register2(Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: BLD_CSC2_COEFF12
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/

19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.56 BLD csc2 const1 register(Default Value: 0x0000_0000)

Offset: 0x018C			Register Name: BLD_CSC2_CONST1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.57 BLD csc2 coeff2 register0(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: BLD_CSC2_COEFF20
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.58 BLD csc2 coeff2 register1(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: BLD_CSC2_COEFF21
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.59 BLD csc2 coeff2 register2(Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: BLD_CSC2_COEFF22
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.60 BLD csc2 const2 register(Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: BLD_CSC2_CONST2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement

15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.61 BLD csc3 coeff0 register0(Default Value: 0x0000_0000)

Offset: 0x01A0			Register Name: BLD_CSC3_COEFF00
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.62 BLD csc3 coeff0 register1(Default Value: 0x0000_0000)

Offset: 0x01A4			Register Name: BLD_CSC3_COEFF01
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.63 BLD csc3 coeff0 register2(Default Value: 0x0000_0000)

Offset: 0x01A8			Register Name: BLD_CSC3_COEFF02
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.64 BLD csc3 const0 register(Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: BLD_CSC3_CONST0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.65 BLD csc3 coeff1 register0(Default Value: 0x0000_0000)

Offset: 0x01B0			Register Name: BLD_CSC3_COEFF10
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF**

			The value equals to coefficient*2^{17}

3.11.9.66 BLD csc3 coeff1 register1(Default Value: 0x0000_0000)

Offset: 0x01B4			Register Name: BLD_CSC3_COEFF11
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.67 BLD csc3 coeff1 register2(Default Value: 0x0000_0000)

Offset: 0x01B8			Register Name: BLD_CSC3_COEFF12
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.68 BLD csc3 const1 register(Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: BLD_CSC3_CONST1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.69 BLD csc3 coeff2 register0(Default Value: 0x0000_0000)

Offset: 0x01C0			Register Name: BLD_CSC3_COEFF20
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.70 BLD csc3 coeff2 register1(Default Value: 0x0000_0000)

Offset: 0x01C4			Register Name: BLD_CSC3_COEFF21
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.71 BLD csc3 coeff2 register2(Default Value: 0x0000_0000)

Offset: 0x01C8			Register Name: BLD_CSC3_COEFF22
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	**COEFF** The value equals to coefficient*2^{17}

3.11.9.72 BLD csc3 const2 register(Default Value: 0x0000_0000)

Offset: 0x01CC			Register Name: BLD_CSC3_CONST2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:16	R/W	0x0	**D0** the *D0* represent the two's complement
15:11	/	/	/
10:0	R/W	0x0	**C03** the *C03* represent the two's complement

3.11.9.73 BLD csc0 alpha register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: BLD_CSC0_APHA
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	**ALPHA_EN** 0x0:disable 0x1:enable
7:0	R/W	0x0	**ALPHA** the alpha value for csc0, if the alpha enable using this value, otherwise using the channel0's alpha.

3.11.9.74 BLD csc1 alpha register(Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: BLD_CSC1_APHA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**ALPHA_EN** 0x0:disable 0x1:enable
7:0	R/W	0x0	**ALPHA** the alpha value for csc1, if the alpha enable using this value, otherwise using the channel1's alpha.

3.11.9.75 BLD csc2 alpha register(Default Value: 0x0000_0000)

Offset: 0x01F8	Register Name: BLD_CSC2_APHA

Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	**ALPHA_EN** 0x0:disable 0x1:enable
7:0	R/W	0x0	**ALPHA** the alpha value for csc2, if the alpha enable using this value, otherwise using the channel2's alpha.

3.11.9.76 BLD csc3 alpha register(Default Value: 0x0000_0000)

Offset: 0x01FC			Register Name: BLD_CSC3_APHA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	**ALPHA_EN** 0x0:disable 0x1:enable
7:0	R/W	0x0	**ALPHA** the alpha value for csc3, if the alpha enable using this value, otherwise using the channel3's alpha.

3.12 DE RT-WB Controller Specification

3.12.1 Overview

The Real-time write-back controller (RT-WB) provides data capture function for display engine. It captures data from RT-mixer module, performs the image resizing function, and then write-back to SDRAM.

The RT-WB can receive RGB888 or YUV444 data format, and then converts to YV12/NV12/NV21 or interleaved RGB888/pRGB888/pBGR888 for write-back. Horizontal and vertical direction scaling-down are implemented independently.

The RT-WB features:

- Support RGB888 and YUV444 input data format
- Support input size from 8×4 to 4096×4096
- Support output size from 8×4 to **W**×4096 (**W** is RTL programmable)
- Support fine down scaling ratio from 1× to 1/2×, and the anti-aliasing filter is 16-phase 4-tap in horizontal , 16-phase 2-tap filter in vertical.
- Support coarse down scaling.

Table 3-4. RTL programmable parameters table

Parameter name	Default	Possible value	Description
W	2048	1280/2048/4096	3 channels line buffer length
FINE_SCALE_EXIST	1	1/0	Define fine scaler exist or not.
PORT_NUM	4	2/4/8	Input port number
M	16	16	Phase number
FRAC	18	18	Phase adder fraction part bit width

3.12.2 Block Diagram

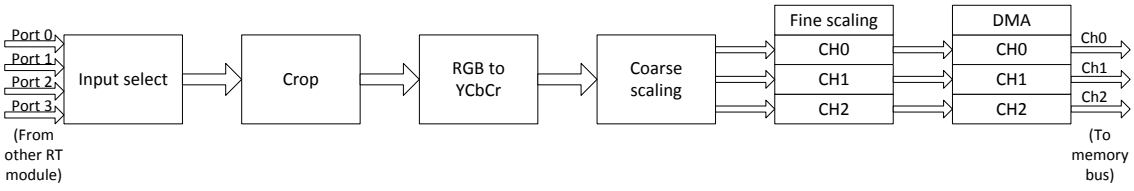


Figure 3-16. RT-WB Block Diagram

3.12.3 Operations and Function Descriptions

3.12.3.1 Write-back flow

The main flow when new frame starts description in Figure 5-8.

The new frame starts with a positive edge of *START*, which is a input from RT-TOP. RT-WB module will check signals like BUSY, OVERFLOW, FINISH to determine the last frame is success to write-back or not. If BUSY is still 1, TIME_OUT will be set, and users will know that the last frame did not write-back successfully. The OVERFLOW is also a error status signal. It represents the module is too slow to write-back all the data to memory bus in last frame. These two errors will

cause a local reset action to clear the whole scaler and some parts in DMA circuit.

A write-back address switch circuit can select the next write-back address automatically. The detail switch function description in Figure 5-9.

After local reset action or address switch, the circuit will check the WB_START is set or not. When WB_START is 1, the write-back function will be activated and this frame will be processed.

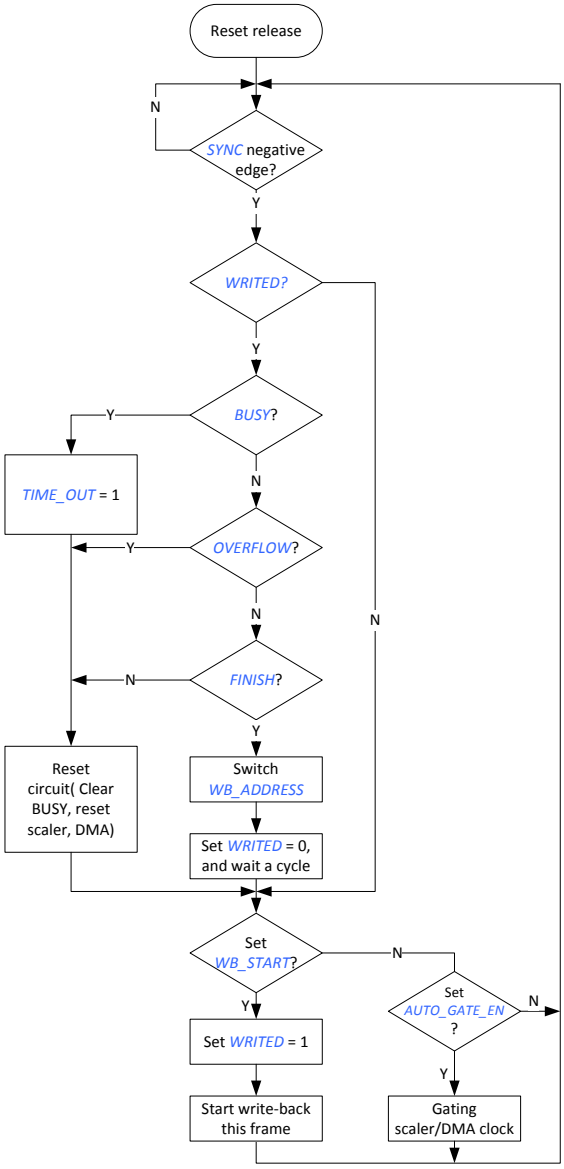


Figure 3-17. The main control flow of RT-WB

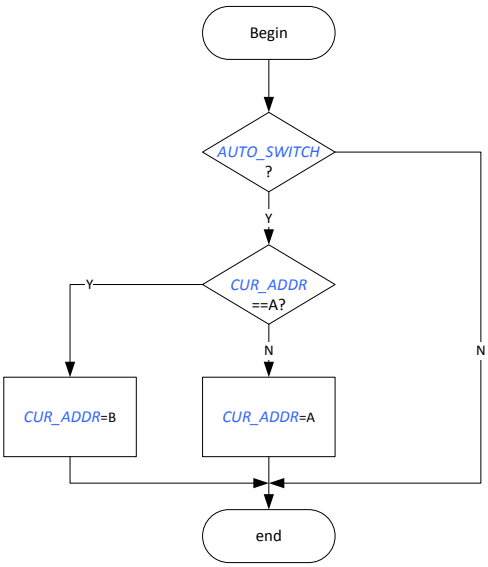


Figure 3-18. Write-back address switch function

3.12.3.2 Key signal and key register

Signal	Type	Description	Note
BUSY	Read only register	Scaler or DMA busy status	Becomes 1 when WB_START takes effect, becomes 0 when FIFO overflowed,write-back time-out or write-back finished, or local reset, or global reset.
WB_START	R/W register	Write-back enable register	Set 1 to start a new frame write-back, becomes 0 when write-back started, or global reset.
SYNC	Input signal	New frame start signal from RT TOP module	Negative edge of SYNC represents a new display frame.
OVERFLOW	R/W register	FIFO overflowed flag	Becomes 1 when FIFO overflowed (write-back too slow), becomes 0 when write 1 to it, or global reset.
FINISH	R/W register	Write-back successful finish flag	Becomes 1 when write-back finished successfully, becomes 0 when write 1 to it, or global reset.
TIME_OUT	R/W register	Write-back time out flag	When SYNC negative edge comes, write-back has not finished yet , this bit will set 1. Becomes 0 when write 1 to it, or global reset.
WRITED	Internal signal	One frame has been written-back	Becomes 1 when WB_START takes effect, becomes 0 when next SYNC negative edge comes, or global reset.
IRQ	R/W register	Write-back end flag	When WRITED negative edge comes, IRQ becomes 1, becomes 0 when write 1 to it, or global reset.
INTR	Output signal	Interrupt signal to GIC module	INTR = *IRQ* & *INT_EN*
GLOBAL RESET	Input signal	Global reset from RT TOP module	Clear the whole scaler circuit, some parts of DMA circuit, and status register/WB_START.

AUTO SWITCH	R/W register	Write-back address automatic switch enable	Set 1 to enable function, set 0 to disable.
CUR_ADDRx (x=0,1,2)	Internal register	Channel x current write back start address	
AUTO_GATE_EN	R/W register	Enable automatic gating clock.	Set 1 to enable function, set 0 to disable. If AUTO_GATE_EN==1, when module idle, the clock to scaler and DMA will be gated. And when a write-back frame starts, the clock gate will be released.
CLK_GATE	R/W register	Clock gate of scaler and DMA module	If AUTO_GATE_EN==0, set 1 to release clock, set 0 to gating clock. No use when AUTO_GATE_EN==1.

3.12.4 RT-WB Register List

Module Name	Base Address
RT-WB	0x011A0000

Register name	Offset	Description
WB_GCTRL_REG	0x000	Module general control register
WB_SIZE_REG	0x004	Input size register
WB_CROP_COORD_REG	0x008	Cropping coordinate register
WB_CROP_SIZE_REG	0x00c	Cropping size register
WB_A_CH0_ADDR_REG	0x010	Write-back Group A channel 0 address register
WB_A_CH1_ADDR_REG	0x014	Write-back Group A channel 1 address register
WB_A_CH2_ADDR_REG	0x018	Write-back Group A channel 2 address register
WB_A_HIGH_ADDR_REG	0x01c	Write-back Group A address high bit register
WB_B_CH0_ADDR_REG	0x020	Write-back Group B channel 0 address register
WB_B_CH1_ADDR_REG	0x024	Write-back Group B channel 1 address register
WB_B_CH2_ADDR_REG	0x028	Write-back Group B channel 2 address register
WB_B_HIGH_ADDR_REG	0x02c	Write-back Group B address high bit register
WB_CH0_PITCH_REG	0x030	Write-back channel 0 pitch register
WB_CH12_PITCH_REG	0x034	Write-back channel 1/2 pitch register
WB_ADDR_SWITCH_REG	0x040	Write-back address switch setting register
WB_FORMAT_REG	0x044	Output format register
WB_INT_REG	0x048	Interrupt control register
WB_STATUS_REG	0x04c	Module status register
WB_BYPASS_REG	0x054	Bypass control register
WB_CS_HORZ_REG	0x070	Coarse scaling horizontal setting register
WB_CS_VERT_REG	0x074	Coarse scaling vertical setting register
WB_FS_INSIZE_REG	0x080	Fine scaling input size register
WB_FS_OUTSIZE_REG	0x084	Fine scaling output size register

WB_FS_HSTEP_REG	0x088	Fine scaling horizontal step register
WB_FS_VSTEP_REG	0x08C	Fine scaling vertical step register
WB_DEBUG_REG	0x0FC	Debug register
WB_CH0_HCOEF_REGN	0x200 + N*4	Channel 0 horizontal coefficient register N (N = 0,1,2,...,15)
WB_CH1_HCOEF_REGN	0x280 + N*4	Channel 1/2 horizontal coefficient register N (N = 0,1,2,...,15)

Note: None of these registers is double-buffer.

3.12.5 RT-WB Register Description

3.12.5.1 WB_GCTRL_REG (Default Value: 0x0000_0000)

Offset: 0x0000			Register name: WB_GCTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	**BIST_EN** Enable BIST mode 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	**CLK_GATE** Clock gate of scaler and DMA module 0: Gate 1: Release
28	R/W	0x0	**AUTO_GATE_EN** Enable automatic clock gating 0: Disable 1: Enable
27:18	/	/	/
17:16	R/W	0x0	**IN_PORT_SEL** Input port selection 0: port 0 1: port 1 2: port 2 3: port 3
15:5	/	/	/
4	R/W	0x0	**SOFT_RESET** Reset the whole scaler and DMA. 0:Reset release. 1:Reset hold.
3:1	/	/	/
0	R/W	0x0	**WB_START** Start write-back process. 0: Do nothing.

			1: Start.

3.12.5.2 WB_SIZE_REG (Default Value: 0x0000_0000)

Offset: 0x0004			Register name: WB_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**HEIGHT** Input height The real input height = The value of these bits + 1.
15:13	/	/	/
12:0	R/W	0x0	**WIDTH** Input width The real input width = The value of these bits + 1.

3.12.5.3 WB_CROP_COORD_REG (Default Value: 0x0000_0000)

Offset: 0x0008			Register name: WB_CROP_COORD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**CROP_TOP** Cropping top position Top position is the left-top y coordinate of input window in pixels
15:13	/	/	/
12:0	R/W	0x0	**CROP_LEFT** Cropping left position Left position is left-top x coordinate of input window in pixels

3.12.5.4 WB_CROP_SIZE_REG (Default Value: 0x0000_0000)

Offset: 0x0000C			Register name: WB_CROP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**CROP_HEIGHT** Cropping region height The real cropping region height = the value of these bits + 1.
15:13	/	/	/
12:0	R/W	0x0	**CROP_WIDTH** Cropping region width The real cropping region width = the value of these bits + 1.

3.12.5.5 WB_A_CH0_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x0010			Register name: WB_A_CH0_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**ADDR**

			Note: In BYTE. When output format is RGB, **ADDR** must 4 bytes aligning.

3.12.5.6 WB_A_CH1_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x0014			Register name: WB_A_CH1_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**ADDR** Note: In BYTE.

3.12.5.7 WB_A_CH2_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x0018			Register name: WB_A_CH2_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0	**ADDR** Note: In BYTE.

3.12.5.8 WB_A_HIGH_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x001C			Register name: WB_A_HIGH_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	**/**
23:16	R/W	0x0	**CH2_H_ADDR**
15:8	R/W	0x0	**CH1_H_ADDR**
7:0	R/W	0x0	**CH0_H_ADDR**

3.12.5.9 WB_B_CH0_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x0020			Register name: WB_B_CH0_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:00	R/W	0x0	**ADDR** Note: In BYTE. When output format is RGB, **ADDR** must 4 bytes aligning.

3.12.5.10 WB_B_CH1_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x0024			Register name: WB_B_CH1_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**ADDR** Note: In BYTE.

3.12.5.11 WB_B_CH2_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x0028			Register name: WB_B_CH2_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**ADDR**

			Note: In BYTE.

3.12.5.12 WB_B_HIGH_ADDR_REG (Default Value: 0x0000_0000)

Offset: 0x002C			Register name: WB_B_HIGH_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	**/**
23:16	R/W	0x0	**CH2_H_ADDR**
15:8	R/W	0x0	**CH1_H_ADDR**
7:0	R/W	0x0	**CH0_H_ADDR**

3.12.5.13 WB_CH0_PITCH_REG (Default Value: 0x0000_0000)

Offset: 0x0030			Register name: WB_CH0_PITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**PITCH** Write-back channel 0 pitch in BYTE.

3.12.5.14 WB_CH12_PITCH_REG (Default Value: 0x0000_0000)

Offset: 0x0034			Register name: WBC_CH12_PITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	**PITCH** Write-back channel 1/2 pitch in BYTE.

3.12.5.15 WB_ADDR_SWITCH_REG (Default Value: 0x0000_0000)

Offset: 0x0040			Register name: WB_ADDR_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	R/W	0x0	**MANUAL_GROUP** When **AUTO_SWITCH** is 0, set this bit will switch the group. 0: Group A 1: Group B
19:17	/	/	/
16	R/W	0x0	**AUTO_SWITCH** Write-back address automatic switch enable 0: Disable 1: Enable
15:01	/	/	/
0	R	0x0	**CUR_GROUP** When **AUTO_SWITCH** is 1, this bit will show the index of group using. 0: Group A 1: Group B

3.12.5.16 WB_FORMAT_REG (Default Value: 0x0000_0000)

Offset: 0x0044			Register name: WB_FORMAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:05	/	/	/
4	R/W	0x0	**OUTBIT** 0: 8bit output 1:10bit output If OUTBIT==0, WB module only input the high 8bit for each data bus; If OUTBIT==1, WB module input 10bit for write back and only write back in one format as X2P10P10P10 in 32bit(without crop/scale or csc functions); And bit[3:0] will be no use in this condition
03:0	R/W	0x0	**FORMAT** Output format selection 0000: RGB888 (R in high address) 0001: BGR888 (B in high address) 0010: Reserved 0011: Reserved 0100: pRGB888(pad equal to 0xff)(p in high address) 0101: pBGR888(pad equal to 0xff)(p in high address) 0110: BGRp888(pad equal to 0xff)(B in high address) 0111: RGBp888(pad equal to 0xff)(R in high address) 1000:Planar YUV420 1001:Reserved 1010:Reserved 1011:Reserved 1100:Planar YUV420 UV combined (V1U1V0U0, V1 in high address) 1101:Planar YUV420 UV combined (U1V1U0V0, U1 in high address) 1110:Reserved 1111:Reserved

3.12.5.17 WB_INT_REG (Default Value: 0x0000_0000)

Offset: 0x0048			Register name: WB_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	**INT_EN** Write-back interrupt enable 0: Disable 1: Enable

3.12.5.18 WB_STATUS_REG (Default Value: 0x0000_0000)

Offset: 0x004C			Register name: WB_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:09	/	/	/

8	R	0x0	**BUSY** Write-back process status 0: write-back end or write-back disable 1: write-back in process
7	/	/	/
6	R/W1C	0x0	**TIME_OUT** Write-back TIME_OUT error flag 0: No error 1: Error
5	R/W1C	0x0	**OVERFLOW** Write-back FIFO overflow error flag 0: No error 1: Error
4	R/W1C	0x0	**FINISH** Write-back process finish flag 0: write-back not finish or fail 1: write-back finished successfully
3:1	/	/	/
0	R/W1C	0x0	**IRQ** Write-back process end flag 0: write-back not end 1: write-back end

3.12.5.19 WB_BYPASS_REG (Default Value: 0x0000_0000)

Offset: 0x0054			**Register Name: WB_BYPASS_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	**FS_EN** Enable Fine Scaling function 0: Bypass Fine scaling 1: Enable Fine scaling
1	R/W	0x0	**CS_EN** Enable Coarse Scaling function 0: Bypass Coarse scaling 1: Enable Coarse scaling
0	R/W	0x0	**CSC_EN** Enable RGB to YPbPr color space conversion 0: Bypass CSC 1: Enable CSC

3.12.5.20 WB_CS_HORZ_REG (Default Value: 0x0000_0000)

Offset: 0x0070			**Register Name: WB_CS_HORZ_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

28:16	R/W	0x0	**N**
15:13	/	/	/
12:0	R/W	0x0	**M**

3.12.5.21 WB_CS_VERT_REG (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: WB_CS_VERT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**N**
15:13	/	/	/
12:0	R/W	0x0	**M**

3.12.5.22 WB_FS_INSIZE_REG (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: WB_FS_INSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**IN_HEIGHT** Channel 0 input height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	**IN_WIDTH** Channel 0 input width The actual width is register value + 1

3.12.5.23 WB_FS_OUTSIZE_REG (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: WB_FS_OUTSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	**OUT_HEIGHT** Channel 0 output height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	**OUT_WIDTH** Channel 0 output width The actual width is register value + 1

3.12.5.24 WB_FS_HSTEP_REG (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: WB_FS_HSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

2			
21:20	R/W	0x0	**HSTEP_INT** The integer part of channel 0 horizontal scale ratio
19:2	R/W	0x0	**HSTEP_FRAC** The fraction part of channel 0 horizontal scale ratio
1:0	/	/	/

3.12.5.25 WB_FS_VSTEP_REG (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: WB_FS_VSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	**VSTEP_INT** The integer part of channel 0 vertical scale ratio
19:2	R/W	0x0	**VSTEP_FRAC** The fraction part of channel 0 vertical scale ratio
1:0	/	/	/

3.12.5.26 WB_DEBUG_REG (Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: WB_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R	0x0	**INPUT_LINE_CNT** Input line counter

3.12.5.27 WB_CH0_HCOEF_REGN (Default Value: 0x0000_0000)

Offset: 0x0200 + N*0x4 (N = 0~15)			Register Name: WB_CH0_HCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	W	UDF	**COEF3** The most right hand-side pixel coefficient
23:16	W	UDF	**COEF2** The right hand-side pixel coefficient
15:8	W	UDF	**COEF1** The left hand-side pixel coefficient
7:0	W	UDF	**COEF0** The most left hand-side pixel coefficient

Note: This coefficients are signed. The coefficient value equals to coefficient*2^6. N represents the phase.

3.12.5.28 WB_CH1_HCOEF_REGN(Default Value: 0x0000_0000)

Offset: 0x0280 + N*0x4 (N = 0~15)			Register Name: WB_CH1_HCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	W	UDF	**COEF3**

			The most right hand-side pixel coefficient
23:16	W	UDF	**COEF2** The right hand-side pixel coefficient
15:8	W	UDF	**COEF1** The left hand-side pixel coefficient
7:0	W	UDF	**COEF0** The most left hand-side pixel coefficient

Note: This coefficients are signed. The coefficient value equals to coefficient*2^6. N represents the phase.

3.13 DE VSU Specification

3.13.1 Overview

The Video Scaler Unit (VSU) provides YUV/ARGB format image resizing function for display engine. It receives data from De-noise module, performs the image resizing function, and outputs to video post-processing modules.

The VSU can receive YUV/ARGB data format, and then converts to YUV444/ARGB for display. Horizontal and vertical direction scaling are implemented independently.

Feature:

- Support YUV420/YUV422/YUV411/YUV444/ARGB data format with 10-bit per channel.
- Support output size from 8×4 to 4096×4096.
- Support input size from 8×4 to W_RGB×W_RGB for YUV444/ARGB format, and support input size from 8×4 to W_YUV×W_YUV for YUV420/YUV422/YUV411 format.
- Support 1/16× to 32× resize ratio
- Support M-phase 8-tap horizontal anti-alias filter, M-phase 4 vertical anti-alias filter for A/R(Y)/G(U)/B(V) channel scale-up and scale-down
- Support edge-direction filtering for Y channel scale-up in YUV420/YUV422/YUV411 format with better picture quality(edge-direction mode support size up to W_YUV_ED×W_YUV_ED, and only be enabled when scale-up in both horizontal and vertical direction)
- Support edge-direction 2-D sharpness enhancement for edge-direction filtering mode
- Point-to-point display size up to W_YUV pixels/line for YUV420/YUV422/YUV411 format

Table 3-5. RTL programmable parameters table

Parameter name	Default	Possible value	Description
M	32	16/32	Phase number
W_YUV	4096	1280/2048/4096 etc	Y channel line buffer length, U/V channel should divide by 2 (YUV420/YUV422/YUV411 format)
W_RGB	2048	1280/2048/4096 etc	R/G/B channel line buffer length (ARGB/YUV444 format)
W_YUV_ED	2048	1280/2048/4096 etc	Y channel line buffer length in ed-scaler mode, U/V channel should divide by 2 (YUV420/YUV422/YUV411 format)
FRAC	19	18/19	Phase adder fraction part bit width
VCLIP	6	0~6 integer	Vertical filtering right shift bit width in normal scale mode

3.13.2 VSU Block Diagram

Figure 3-19 shows the block diagram of Video Scaler Unit. It is a stream-to-stream module. The input interface which contains independent F/A/Y(R)/U(G)/V(B) channel, receives data separately from up-stream module. The five channels also have independent resizing path for U/V format conversion. Together with the Y channel, the F channel is a 1-bit data channel that scales using the nearest neighborhood method which data represents the valid data flag generated

by overlay module. After resizing to F-A-Y-U-V(or F-A-R-G-B) data outputs in pixel mode to down-stream module. It contains some parts and their function list followed:

Control logic: status machine control, registers operation, VPHASE selection.

Resizing: four independent channels line buffer control, horizontal resize, vertical resize.

Figure 3-19 shows a block diagram of the VSU.

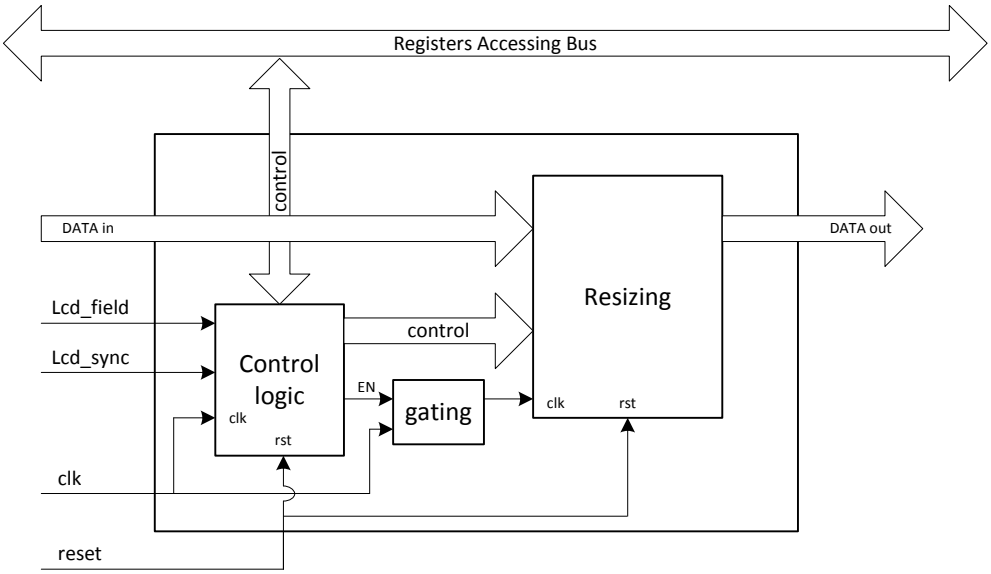


Figure 3-19. VSU block diagram

3.13.3 Video Scaler Register List

Register Name	Offset	Description
VSU_CTRL_REG	0x0000	VSU Module Control Register
VSU_STATUS_REG	0x0008	VSU Status Register
VSU_FIELD_CTRL_REG	0x000C	VSU Field Control Register
VSU_SCALE_MODE_REG	0x0010	VSU Scale Mode Setting Register
VSU_DIRECTION_THR_REG	0x0020	VSU Direction Detection Threshold Register
VSU_EDGE_THR_REG	0x0024	VSU Edge Detection Setting Register
VSU_EDSCALER_CTRL_REG	0x0028	VSU Edge-Direction Scaler Control Register
VSU_ANGLE_THR_REG	0x002C	VSU Angle Reliability Setting Register
VSU_SHARP_EN_REG	0x0030	VSU Sharpness Control Enable Register
VSU_SHARP_CORING_REG	0x0034	VSU Sharpness Control Coring Setting Register
VSU_SHARP_GAIN0_REG	0x0038	VSU Sharpness Control Gain Setting 0 Register
VSU_SHARP_GAIN1_REG	0x003C	VSU Sharpness Control Gain Setting 1 Register
VSU_OUT_SIZE_REG	0x0040	VSU Output Size Register
VSU_GLOBAL_ALPHA_REG	0x0044	VSU Output Global Alpha Register
VSU_Y_SIZE_REG	0x0080	VSU Y Channel Size Register
VSU_Y_HSTEP_REG	0x0088	VSU Y Channel Horizontal Step Register
VSU_Y_VSTEP_REG	0x008C	VSU Y Channel Vertical Step Register
VSU_Y_HPHASE_REG	0x0090	VSU Y Channel Horizontal Initial Phase Register
VSU_Y_VPHASE0_REG	0x0098	VSU Y Channel Vertical Initial Phase 0 Register

VSU_Y_VPHASE1_REG	0x009C	VSU Y Channel Vertical Initial Phase 1 Register
VSU_C_SIZE_REG	0x00C0	VSU C Channel Size Register
VSU_C_HSTEP_REG	0x00C8	VSU C Channel Horizontal Step Register
VSU_C_VSTEP_REG	0x00CC	VSU C Channel Vertical Step Register
VSU_C_HPHASE_REG	0x00D0	VSU C Channel Horizontal Initial Phase Register
VSU_C_VPHASE0_REG	0x00D8	VSU C Channel Vertical Initial Phase 0 Register
VSU_C_VPHASE1_REG	0x00DC	VSU C Channel Vertical Initial Phase 1 Register
VSU_Y_HCOEF0_REGN	0x200+N*4	VSU Y Channel Horizontal Filter Coefficient0 Register N (N=0:(M-1))
VSU_Y_HCOEF1_REGN	0x300+N*4	VSU Y Channel Horizontal Filter Coefficient1 Register N (N=0:(M-1))
VSU_Y_VCOEF_REGN	0x400+N*4	VSU Y Channel Vertical Filter Coefficient Register N (N=0:(M-1))
VSU_C_HCOEF0_REGN	0x600+N*4	VSU C Channel Horizontal Filter Coefficient0 Register N (N=0:(M-1))
VSU_C_HCOEF1_REGN	0x700+N*4	VSU C Channel Horizontal Filter Coefficient1 Register N (N=0:(M-1))
VSU_C_VCOEF_REGN	0x800+N*4	VSU C Channel Vertical Filter Coefficient Register N (N=0:(M-1))

3.13.4 Video Scaler Register Description

3.13.4.1 VSU Module Control Register (Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: VSU_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	BIST_EN BIST enable 0x0: Disable 0x1: Enable
30	R/W	0x0	CORE_RST Core circuit reset 0x0: Do noting 0x1: reset core circuit
29:5	/	/	/
4	R/WAC	0x0	COEF_SWITCH_EN Coefficients RAM switch 0x0: DONOT switch 0x1: Switch RAM use REG_RDY Note: When LCD SYNC go low and COEF_SWITCH_EN is 1, coefficient RAM will switch to the latest updated RAM if REG_RDY is 1, and then the bit will also be self-cleared if switch action successes.
3:1	/	/	/
0	R/W	0x0	EN Video Scaler Unit enable 0x0: Disable

			0x1: Enable Note: When module disabled, the core clock to the core circuit will be gated.

3.13.4.2 VSU Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: VSU_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R	0x0	LINE_CNT Output line number
15:5	/	/	/
4	R	0x0	BUSY Core circuit status 0x0: idle (finish, module disable, waiting for LCD SYNC negative edge) 0x1: busy (core circuit calculating)
3:0	/	/	/

3.13.4.3 VSU Field Control Register (Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: VSU_FIELD_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	LCD_SYNC_REVERSE Reverse LCD SYNC 0x0: DONOT reverse 0x1: Reverse
4	R/W	0x0	LCD_FILED_REVERSE Reverse LCD FILED 0x0: DONOT reverse 0x1: Reverse
3:1	/	/	/
0	R/W	0x0	FIELD_SEL_VPHASE_EN Vertical initial phase switch control 0x0: Vertical initial phase fix to phase0 0x1: Switch Vertical initial phase by LCD FIELD (Switch to phase0 when LCD FILED is 1, and switch to phase1 when LCD FIELD is 0)

3.13.4.4 VSU Scale Mode Setting Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: VSU_SCALE_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	SCALE_MODE FIFO number and filter type for different scale mode

			0x0:UI mode (for ARGB/YUV444 format) 0x1:Video normal mode (for YUV420/YUV422/YUV411 format. Input size limit to W_YUVxW_YUV) 0x2: Video ed-scale mode (for YUV420/YUV422/YUV411 format, Input size limit to W_YUV_EDxW_YUV_ED. Only support when scale-up in both horizontal and vertical direction)

3.13.4.5 VSU Direction Detection Threshold Register (Default Value: 0x0000_FF01)

Offset: 0x0020			Register Name: VSU_DIRECTION_THR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	SUB_ZERO_DIR_THR Threshold of zero gradient in sub-window
23:16	R/W	0x0	ZERO_DIR_THR Threshold of zero gradient
15:8	R/W	0xFF	HORZ_DIR_THR Threshold of horizontal direction detection
7:0	R/W	0x1	VERT_DIR_THR Threshold of vertical direction detection

3.13.4.6 VSU Edge Detection Setting Register (Default Value: 0x0008_0000)

Offset: 0x0024			Register Name: VSU_EDGE_THR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x8	EDGESHIFT Right shift bit width of edge strength
15:8	/	/	/
7:0	R/W	0x0	EDGEOFFSET Offset of edge strength

3.13.4.7 VSU Edge-Direction Scaler Control Register (Default Value: 0x0000_0001)

Offset: 0x0028			Register Name: VSU_EDSCALER_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	LOCALCLAMP Clamp output result to source range 0x0: Disable 0x1: Enable

3.13.4.8 VSU Angle Reliability Setting Register (Default Value: 0x0002_0000)

Offset: 0x002C			Register Name: VSU_ANGLE_THR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/

19:16	R/W	0x2	ANGLESHIFT Right shift bit width of angle reliability
15:8	/	/	/
7:0	R/W	0x0	ANGLEOFFSET Offset of angle reliability

3.13.4.9 VSU Sharpness Enhancement Enable Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: VSU_SHARP_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	SHARP_EN Sharpness enhancement enable 0x0: Disable 0x1: Enable Note: Sharpness enhancement is only valid when SCALE_MODE is video ed-scale mode.

3.13.4.10 VSU Sharpness Enhancement Coring Setting Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: VSU_SHARP_CORING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	CORTH Coring threshold

3.13.4.11 VSU Sharpness Enhancement Gain Setting 0 Register (Default Value: 0x0320_0078)

Offset: 0x0038			Register Name: VSU_SHARP_GAIN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x320	DIPTHR1 Dynamic gain control threshold1
15:10	/	/	/
9:0	R/W	0x78	DIPTHR0 Dynamic gain control threshold0

3.13.4.12 VSU Sharpness Enhancement Gain Setting 1 Register (Default Value: 0x0108_0019)

Offset: 0x003C			Register Name: VSU_SHARP_GAIN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x1	BETA Sharpness suppress for large shoot
23:21	/	/	/

20:16	R/W	0x8	NEGGAIN Sharpness gain for undershoot
15:8	/	/	/
7:0	R/W	0x19	GAIN Sharpness gain

3.13.4.13 VSU Output Size Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: VSU_OUT_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output width The actual width is register value + 1

3.13.4.14 VSU Output Global Alpha Register (Default Value: 0x0000_00FF)

Offset: 0x0044			Register Name: VSU_GLOBAL_ALPHA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xFF	GLOBAL_ALPHA Output global alpha value for **SCALE_MODE** is Video Normal Mode or Video Ed-scale Mode. It will be ignored when **SCALE_MODE** is UI Mode.

3.13.4.15 VSU Y Channel Size Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: VSU_Y_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	Y_HEIGHT Y channel input height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	Y_WIDTH Y channel input width The actual width is register value + 1

3.13.4.16 VSU Y Channel Horizontal Step Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: VSU_Y_HSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	Y_HSTEP_INT The integer part of Y channel horizontal scale ratio
19:1	R/W	0x0	Y_HSTEP_FRAC The fraction part of Y channel horizontal scale ratio
0	/	/	/

3.13.4.17 VSU Y Channel Vertical Step Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: VSU_Y_VSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	Y_VSTEP_INT The integer part of Y channel vertical scale ratio
19:1	R/W	0x0	Y_VSTEP_FRAC The fraction part of Y channel vertical scale ratio
0	/	/	/

3.13.4.18 VSU Y Channel Horizontal Initial Phase Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: VSU_Y_HPHASE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	Y_HPHASE_INT The integer part of Y channel horizontal initial phase
19:1	R/W	0x0	Y_HPHASE_FRAC The fraction part of Y channel horizontal initial phase
0	/	/	/

Note : Y_HPHASE is a register with 1-bit signed, 3-bit integer and 19-bit fraction. Valid value ranges from -0x3FFFFF ~ 0x3FFFFF.

3.13.4.19 VSU Y Channel Vertical Initial Phase 0 Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: VSU_Y_VPHASE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	Y_VPHASE0_INT The integer part of Y channel vertical initial phase0
19:1	R/W	0x0	Y_VPHASE0_FRAC The fraction part of Y channel vertical initial phase0
0	/	/	/

Note : Y_VPHASE0 is a register with 1-bit signed, 3-bit integer and 19-bit fraction. Valid value ranges from -0x3FFFFF ~

0x3FFFFF.

3.13.4.20 VSU Y Channel Vertical Initial Phase 1 Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: VSU_Y_VPHASE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	Y_VPHASE1_INT The integer part of Y channel vertical initial phase1
19:1	R/W	0x0	Y_VPHASE1_FRAC The fraction part of Y channel vertical initial phase1
0	/	/	/

Note : Y_VPHASE1 is a register with 1-bit signed, 3-bit integer and 19-bit fraction. Valid value ranges from -0x3FFFFF ~ 0x3FFFFF.

3.13.4.21 VSU C Channel Size Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: VSU_C_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	C_HEIGHT C channel input height The actual height is register value + 1
15:13	/	/	/
12:0	R/W	0x0	C_WIDTH C channel input width The actual width is register value + 1

3.13.4.22 VSU C Channel Horizontal Step Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: VSU_C_HSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	C_HSTEP_INT The integer part of C channel horizontal scale ratio
19:1	R/W	0x0	C_HSTEP_FRAC The fraction part of C channel horizontal scale ratio
0	/	/	/

3.13.4.23 VSU C Channel Vertical Step Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: VSU_C_VSTEP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

23:20	R/W	0x0	C_VSTEP_INT The integer part of C channel vertical scale ratio
19:1	R/W	0x0	C_VSTEP_FRAC The fraction part of C channel vertical scale ratio
0	/	/	/

3.13.4.24 VSU C Channel Horizontal Initial Phase Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: VSU_C_HPHASE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	C_HPHASE_INT The integer part of C channel horizontal initial phase
19:1	R/W	0x0	C_HPHASE_FRAC The fraction part of C channel horizontal initial phase
0	/	/	/

Note : C_HPHASE is a register with 1-bit signed, 3-bit integer and 19-bit fraction. Valid value ranges from -0x3FFFFF ~ 0x3FFFFF.

3.13.4.25 VSU C Channel Vertical Initial Phase 0 Register (Default Value: 0x0000_0000)

Offset: 0x00D8			Register Name: VSU_C_VPHASE0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	C_VPHASE0_INT The integer part of C channel vertical initial phase0
19:1	R/W	0x0	C_VPHASE0_FRAC The fraction part of C channel vertical initial phase0
0	/	/	/

Note : C_VPHASE0 is a register with 1-bit signed, 3-bit integer and 19-bit fraction. Valid value ranges from -0x3FFFFF ~ 0x3FFFFF.

3.13.4.26 VSU C Channel Vertical Initial Phase 1 Register (Default Value: 0x0000_0000)

Offset: 0x00DC			Register Name: VSU_C_VPHASE1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	C_VPHASE1_INT The integer part of C channel vertical initial phase1
19:1	R/W	0x0	C_VPHASE1_FRAC The fraction part of C channel vertical initial phase1
0	/	/	/

Note : C_VPHASE1 is a register with 1-bit signed, 3-bit integer and 19-bit fraction. Valid value ranges from -0x3FFFFF ~ 0x3FFFFF.

3.13.4.27 Y Channel Horizontal Filter Coefficient 0 Register N (N=0:(M-1))

Offset: 0x0200 + N*4			Register Name: VSU_Y_HCOEF0_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	COEF3
23:16	R/W	UDF	COEF2
15:8	R/W	UDF	COEF1
7:0	R/W	UDF	COEF0

3.13.4.28 Y Channel Horizontal Filter Coefficient 1 Register N (N=0:(M-1))

Offset: 0x0300 + N*4			Register Name: VSU_Y_HCOEF1_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	COEF7
23:16	R/W	UDF	COEF6
15:8	R/W	UDF	COEF5
7:0	R/W	UDF	COEF4

3.13.4.29 Y Channel Vertical Filter Coefficient Register N (N=0:(M-1))

Offset: 0x0400 + N*4			Register Name: VSU_Y_VCOEF_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	COEF3
23:16	R/W	UDF	COEF2
15:8	R/W	UDF	COEF1
7:0	R/W	UDF	COEF0

3.13.4.30 C Channel Horizontal Filter Coefficient 0 Register N (N=0:(M-1))

Offset: 0x0600 + N*4			Register Name: VSU_C_HCOEF0_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	COEF3
23:16	R/W	UDF	COEF2
15:8	R/W	UDF	COEF1
7:0	R/W	UDF	COEF0

3.13.4.31 C Channel Horizontal Filter Coefficient 1 Register N (N=0:(M-1))

Offset: 0x0700 + N*4			Register Name: VSU_C_HCOEF1_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	COEF7
23:16	R/W	UDF	COEF6
15:8	R/W	UDF	COEF5
7:0	R/W	UDF	COEF4

3.13.4.32 C Channel Vertical Filter Coefficient Register N (N=0:(M-1))

Offset: 0x0800 + N*4			Register Name: VSU_C_VCOEF_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	COEF3
23:16	R/W	UDF	COEF2
15:8	R/W	UDF	COEF1
7:0	R/W	UDF	COEF0