Features

Processor

- Octa-core ARM Cortex™-A55, up to 1.8 GHz
- RISC-V CPU, up to 200 MHz
- HiFi4 Audio DSP
- ARM G57 MC1 GPU
- Up to 2 TOPS NPU

Memory

- 32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X interface, supporting maximum capacity of 4 GB
- 4 chip select lines for LPDDR3, LPDDR4, and LPDDR4X (especially the 64-bit LPDDR3, LPDDR4, and LPDDR4X)
- SD3.0/eMMC5.1 interface

Video Engine

- H.265 MP and VP9 decoder up to 4K@60fps
- H.264 BL/MP/HP decoder up to 4K@30fps
- H.264 BP/MP/HP encoder up to 4K@25fps
- MJPEG encoder up to 4K@15fps, JPEG encoder up to 8K x 8K resolution

Video Output

- Two dual-link LVDS interfaces, up to 1080p@60fps
- Two RGB interfaces with DE/SYNC mode, up to 1080p@60fps
- eDP 1.3, up to 2.5K@60fps and 4K@30fps
- 4+4-lane MIPI-DSI output interface up to 2.5K@60fps and 4K@45fps
- HDMI2.0 TX interface, supporting HDCP1.4

Video Input

- 8/10/12/16-bit parallel CSI, supporting BT.656 up to 4*720P@30fps and BT.1120 up to 4*1080P@30fps
- 4+4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI CSI, up to 2.0 Gbit/s per lane in HS transmission, compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.1
- Maximum video capture resolution of 8M@30fps for MIPI CSI

Audio

- 2 DACs and 3 ADCs
- 3 x audio outputs: LINEOUTLP/N, LINEOUTRP/N, HPOUTL/R
- 3 x audio inputs: MICIN1P/N, MICIN2P/N, MICIN3P/N
- 4x I2S/PCM external interfaces: I2S0, I2S1, I2S2, and I2S3
- Maximum 8 digital PDM microphones (DMIC)
- One OWA RX and one OWA TX, compliance with S/PDIF interface

External Peripherals

- 1 x USB2.0 Host, 1 x USB2.0 DRD, 1 x USB3.1 DRD&PCIe2.1 Combo
- 2 x GMAC (10/100/1000 Mbps port with RGMII and RMII interfaces)
- 2 x CIR RX, 1 x CIR TX, 9 x TWI, 4 x SPI, 10 x UART, 2 x CAN
- 30-ch PWM, 24-ch GPADC, 2-ch LRADC
- SDIO 3.0, LEDC, SPIF (Octal I/O)

Security System

- AES, DES, 3DES, and SM4 encryption and decryption algorithms
- MD5, SHA, and HMAC tamper proofing
- RSA, ECC signature and verification algorithms

Package

- HS-FCBGA 664balls
- 17 mm x 17 mm body size
- Maximum 1.844 mm height
- 0.5 mm ball pitch
- 0.3 mm ball size

Revision History

Revision	Date	Author	Description
0.90	November 16, 2023	AWA1896	Initial Release Version
0.91	July 24, 2024	AWA1896	**Chapter 3 Features** 1. Update the input formats and output formats of G2D in section 3.6.3. 2. Remove BMODE and timeout in section 3.9.2. **Chapter 6 Electrical Characteristics** 1. Update the maximum values of VDD-CPUB, VDD-CPUL, VDD-CPUS, VDD-DNR, VDD-GPU, VDD-SYS, VDD-VE, VDD09-PCIE, and VDD09-USB in Table 6-1 Absolute Maximum Ratings. 2. Add VDD09-HDMI in Table 6-1 Absolute Maximum Ratings. 3. Update the T5 timing requirement in Figure 6-46 Power-on Timing. 4. Update the typical voltages of VDD-DNR and VDD-SYS in Figure 6-46 and Figure 6-47. **Chapter 7 Temperature and Thermal Characteristics** Update package thermal parameters in Table 7-3.

Contents

Figures

Tables

About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the T527 series. For details about register descriptions of each module, see the *T527_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics

- Sales personnel for electronic parts and components

Revision Number Definition

Revision 0.90-0.9x

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
⚠ WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
⚠ CAUTION	A caution means that damage to equipment is possible.

Symbol	Description
☐ NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

1 Overview

T527 series features high-performance octa-core Cortex™-A55 AI platform SoCs for the electronic commercial, industrial, and automotive fields. The chip family integrates octa-core Cortex™-A55 CPU, a HiFi4 DSP, 2 TOPS NPU, G57 MC1 GPU, 32-bit DDR3/ DDR3L/ DDR4/ LPDDR3/ LPDDR4/ LPDDR4X DRAM, high-speed interfaces (PCIe2.1 and USB3.1), automotive interface (CAN), multi video output interfaces (2*RGB/2*Dual-LVDS/2*MIPI-DSI/HDMI/eDP), and video input interfaces (MIPI CSI). The chip family supports 4K@60fps H.265 decoder, 4K@30fps H.264 decoder, 4K@25fps H.264 encoder, DI, and AWonder system, which provides users with smooth experience and professional AI visual effect. T527 series can be used in Content sharing and self-service interactive terminals, Smart manufacturing, and other electronic commercial and industrial devices.

2 Ordering Information

T527 series contains the following devices:

Table 2-1 Device Summary

Orderable Device	NPU	Package
T527M02X0DCH	Support	17 mm x 17 mm, FCBGA 664 balls
T527M00X0DCH	Not Support	17 mm x 17 mm, FCBGA 664 balls

📖 NOTE

- The terms T527 and T527 Series are used in the following document to refer to the all devices listed in Table 2-1.

- If you need to use 4K@60fps H.265 decoder, additional design is required. For detailed description, please refer to *T527_Hardware_Design_Guide*, *T527-DEMO-AXP717B-LPDDR4-32X1*, and *Linux_Decoder_Development_Manual*.

3 Features

3.1 CPU Architecture

- Octa-core ARM Cortex™-A55 in a DynamIQ big. LITTLE configuration, up to 1.8 GHz

  - 32 KB L1 I-cache and 32 KB L1 D-cache per A55 core

  - Optional 64KB L2 cache per　LITTLE　core

  - Optional 128KB L2 cache per　big　core

- RISC-V CPU, up to 200 MHz

  - 16 KB I-cache and 16 KB D-cache

  - RV32IMAFC instructions

3.2 NPU Architecture

- 2 TOPS NPU

- Embedded 512KB internal buffer

- Supports deep learning frameworks: TensorFlow, Caffe, TFLite, Pytorch, Onnx NN, and so on

3.3 GPU Architecture

- ARM G57 MC1 GPU

- Supports OpenGL ES 3.2/2.0/1.1, Vulkan1.1/1.2/1.3, and OpenCL2.2

- Anti-aliasing algorithm

- High memory bandwidth and low power consumption in 3D graphics processing

3.4 DSP Architecture

- HiFi4 Audio DSP

  - 32 KB I-cache + 32 KB D-cache

3.5 Memory Subsystem

3.5.1 Boot ROM (BROM)

- On-chip memory

- Supports system boot from the following devices:

  - SD Card

  - eMMC

  - RAW NAND Flash

  - SPI NOR Flash (Quad Mode and Single Mode)

  - SPI NAND Flash

- Supports mandatory upgrade process through USB or SD card

- Supports GPADC0 pin and eFuse module to select the boot media type

- Supports normal booting and secure booting

- Secure BROM loads only certified firmware

- Secure BROM ensures that the secure boot is a trusted environment

3.5.2   RAW NAND Flash

- Up to 80-bit ECC per 1024 bytes

- Supports 1K/2K/4K/8K/16K/32K bytes page size

- Up to 8-bit data bus width

- Supports SLC/MLC flash and EF-NAND

- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0, and Toggle DDR2.0 RAW NAND FLASH

3.5.3   SDRAM

- 32-bit DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X interface

- Memory capacity up to 4GB

- 4 chip select lines for LPDDR3, LPDDR4, and LPDDR4X (especially the 64-bit LPDDR3, LPDDR4, and LPDDR4X)

- Clock frequency up to 1066 MHz for DDR3, DDR3L, and LPDDR3

- Clock frequency up to 1200 MHz for DDR4, LPDDR4, and LPDDR4x

3.5.4   SMHC

- Three SD/MMC host controller (SMHC) interfaces

  - SMHC0, compliant with the protocol Secure Digital Memory (SD3.0)

  - SMHC1, compliant with the protocol Secure Digital I/O (SDIO3.0)

  - SMHC2, compliant with the protocol Multimedia Card (eMMC5.1)

- The SMHC0 and the SMHC1 support the following:

  - 1-bit or 4-bit data width

  - Maximum performance:

    - ➢ SDR mode 200 MHz@1.8 V IO pad

    - ➢ DDR mode 50 MHz@1.8 V IO pad

    - ➢ SDR mode 50 MHz@3.3 V IO pad

- The SMHC2 supports the following:

  - 1-bit, 4-bit, or 8-bit data width

  - Supports HS400 mode and HS200 mode

  - Maximum performance

    - ➢ SDR mode 200 MHz@1.8V IO pad

    - ➢ DDR mode 50 MHz@1.8V IO pad

    - ➢ SDR mode 50 MHz@3.3V IO pad

    - ➢ DDR mode 50 MHz@3.3V IO pad

- Support block size of 1 to 65535 bytes

- Support hardware CRC generation and error detection

3.6 Video and Graphics

3.6.1 Display Engine (DE)

- Output size up to 4096 x 2048

- Supports seven alpha blending channels for main display and two display outputs

- Supports four overlay layers in each channel, and has an independent scaler

- Supports potter-duff compatible blending operation

- Supports AFBC buffer decoder

- Supports vertical keystone correction

- Input format

  - Semi-planar of YUV422/YUV420/YUV411/P010/P210

  - Planar of YUV422/YUV420/ YUV411

  - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565

- Output format: 8-bit or 10-bit YUV444/YUV422/YUV420/RGB444

- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data

- 10-bit processing path for HDR video

- AWonder1.0 for excellent display experience

  - Adaptive de-noising for compression noise or mosquito noise with yuv420/422 input

  - Adaptive super resolution scaler

  - Adaptive local dynamic contrast enhancement

  - Adaptive detail/edge enhancement

  - Adaptive color enhancement (blue-stretch, green-stretch, and fresh tone correction) and skin tone protection

  - Hue gain, saturation gain, and value gain controller

  - Fully programmable color matrix

  - Dynamic gamma

- Supports write back for high efficient dual display and miracast

- Supports register configuration queue for register update function

3.6.2   De-interlacer (DI)

- Only off-line processing mode

- Video resolution from 32x32 to 2048x1280 pixel

- Input data format: 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined

- Output data format

  - 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined for DIT

  - YV12/planar YUV422 for TNR

- Weave/pixel-motion-adaptive de-interlace method

- Temporal noise reduction

- Film mode detection with video-on-film detection

- Performance

  - Module clock 120MHz for 1080P@60Hz YUV420 with all functions enable

  - Module clock 150MHz for 1080P@60Hz YUV422 with all functions enable

3.6.3   Graphic 2D (G2D)

- Maximum resolution: 2560x2560

- The input formats supporting rotation function are as follows:

  - YUV422 (packed, semi-planar and planar format)

  - YUV420 (semi-planar and planar format)

- P010, P210, P410, and Y8

- A2R10G10B10, A2B10G10R10, R10G10B10A2, and B10G10R10A2

- ARGB8888, RGBA8888, XRGB8888, RGBX8888, RGB888, RGB565, ARGB4444, RGBA4444, ARGB1555, and RGBA5551

- ABGR8888, BGRA8888, XBGR8888, BGRX8888, BGR888, BGR565, ABGR4444, BGRA4444, ABGR1555, and BGRA5551

- Multiple rotation types

  - Horizontal flip and vertical flip

  - 0, 90, 180, or 270 degrees   rotation in clockwise direction

3.6.4　Video Engine

3.6.4.1　Video Decoding

- Supports ITU-T H.265 Main/Main10, level 6.1

  - Maximum video resolution:8192x4320

  - Maximum decoding rate: 3840x2160@60fps

- Supports VP9 Profile0/ Profile2, level 6.1

  - Maximum video resolution: 8192 x 4320

  - Maximum decoding rate: 3840x2160@60fps

- Supports ITU-T H.264 Base/Main/High Profile@Level 4.2

  - Maximum video resolution: 3840 x 2160

  - Maximum decoding rate: 3840x2160@30fps

3.6.4.2　Video Encoding

- H.264 BP/MP/HP encoding

  - Supports 4K@25fps@8bits

  - Maximum resolution: 4096 x 4096 (16 megapixels)

  - Supports I/P frame type

  - Supports CBR, VBR and FIXEDQP modes

  - Supports region of interest(ROI) encoding, a maximum of eight ROIs

- JPEG baseline encoding

  - JPEG encoder supports 4K@15fps

  - JPEG encoder supports YUV420, YUV422 and YUV444 format

- MJPEG baseline encoding up to 4K@15fps

3.7 Video Output

3.7.1 eDP1.3

- Up to 2.5K@60fps and 4K@30fps
- 1-lane, 2-lane, or 4-lane transmission, up to 2.7 Gbit/s per lane
- Video formats: RGB, YCbCr4:4:4, and YCbCr4:2:2
- Color depth: 8-bit and 10-bit per channel
- Supports I2S interface
  - Supports mono sound, stereo sound, and 7.1 surround sound
  - Maximum sampling rate: 192 KHz
- Full link training
- Hot plug detection
- AUX channel
  - Maximum working frequency: 1MHz
  - Adopts Manchester-II encoding
- Clock spread spectrum
- Programmable voltage swing and pre-emphasis
- Embedded ESD

3.7.2 MIPI DSI

- Compliance with MIPI DSI V1.02
- Up to 1.2 Gbit/s for each lane
- Supports 4-lane MIPI DSI, up to 1280 x 720@60fps and 1920 x 1200@60fps
- Supports 4+4-lane MIPI DSI, up to 2560 x 1600@60fps and 4096 x 2160@45fps
- Supports non-burst mode with sync pulse/sync event, burst mode, and command mode
- Pixel format: RGB888, RGB666, RGB666 loosely packed and RGB565
- Supports continuous and non-continuous lane clock modes
- Generic commands support bidirectional communication in LP through data lane 0
- Supports low power data transmission
- Supports ULPS and escape modes
- Supports hardware checksum

3.7.3   TCON LCD

- Three TCON LCD controllers: TONC_LCD0, TCON_LCD1, and TCON_LCD2.

- TCON_LCD0 supports the following:

    - Supports RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps

    - Supports serial RGB/dummy RGB interface, up to 800 x 480@60fps

    - Supports LVDS interface with dual link, up to 1920 x 1080@60fps

    - Supports LVDS interface with single link, up to 1366 x 768@60fps

    - Dither function for RGB888, RGB666, and RGB565

    - Supports i8080 interface, up to 800 x 480@60fps

    - Supports BT656 interface for NTSC and PAL

    - Supports MIPI DSI interface with dual link, up to 2560x1600@60fps, 3840x2160@45fps and 4096x2160@45fps

    - Supports MIPI DSI interface with single link, up to 1920x1200@60fps

- TCON_LCD1 supports MIPI DSI interface with single link, up to 1920x1200@60fps

- TCON_LCD2 supports the following:

    - Supports RGB interface with DE/SYNC mode, up to 1280x720@60fps

    - Supports serial RGB/dummy RGB interface, up to 800x480@60fps

    - Supports i8080 interface, up to 800x480@60fps

    - Supports BT656 interface for NTSC and PAL

    - Supports RGB888, RGB666 and RGB565 with dither function

    - Supports LVDS interface with dual link, up to 1920x1080@60fps

    - Supports LVDS interface with single link, up to 1366x768@60fps

3.7.4   TCON TV

- Two TCON TV controllers: TCON_TV0 for HDMI 2.0b and TCON_TV1 for eDP1.3

- Up to 4K@60Hz

- Output format:

    - 8-bit or 10-bit pixel depth

    - HV

3.7.5   HDMI

- One HDMI2.0 TX interface, supporting HDCP1.4

- Up to 4K@60fps for 2D display and up to 4K@30fps for 3D display

- Supports several data formats including RGB888, YUV444, YUV422, and YUV420

- Supports I2S, 192KHz sampling rate, 8 sound channels

- Supports up to 3840x2160@60 10bit input, 3 Data lanes, 6 Gbit/s per lane for YUV422

- Supports DDC/CEC, 5 V tolerant voltage

- Supports 3840x2160, 1920x1080, and 1280x720 resolution

3.8 Video Input

3.8.1 ISP

- Supports one individual image signal processor(ISP), with maximum resolution of 3264x4224 in online mode

- Maximum frame rate of 8M@30fps 2F-WDR

- Supports off-line mode

- Supports WDR spilt, 2F-WDR line-based stitch, dynamic range compression (DRC), tone mapping, digital gain, gamma correction, defect pixel correction (DPC), cross talk correction (CTC), and chromatic aberration correction (CAC)

- Supports 2D/3D noise reduction, bayer interpolation, sharpen, white balance, and color enhancement

- Adjustable 3A functions: automatic white balance (AWB), automatic exposure (AE), and automatic focus (AF)

- Supports anti-flick detection statistics, and histogram statistics

3.8.2 VIPP

- Four VIPP YUV422 or YUV420 outputs

- Maximum resolution of 3264x4224

- Each VIPP has one sub-VIPP in online mode

- Each VIPP has maximum four sub-VIPPs for time division multiplexing in offline mode

- Each Sub-VIPP supports the following:

  - Crop

  - 1 to 1/16 scaling for height and width

  - 16 ORLs

- Supports graphics mirror and flip

3.8.3 MIPI CSI

- 8M@30fps RAW12 2F-WDR, size up to 3264(H) x 2448(V)

- 4+4-lane, 4+2+2-lane, or 2+2+2+2-lane MIPI Interface

    - MIPI CSI2 V1.1

    - MIPI DPHY V1.1

    - 2.0 Gbit/s per lane

- Crop function

- Frame-rate decreasing via software

- 6 DMA controllers for 6 video stream storage

    - Conversion of interlaced input to progressive output (anti-aliasing and noise reduction are not supported)

    - Data conversion supports: YUV422 to YUV420, YUV422 to YUV400, YUV420 to YUV400

    - Horizontal and vertical flip

3.8.4   Parallel CSI

- 16-bit digital camera interface

- Supports 8/10/12/16-bit width

- Supports BT.656, BT.601, BT.1120 interface

- Dual Data Rate (DDR) sample mode with pixel clock up to 148.5MHz

- Supports ITU-R BT.656 up to 4*720P@30fps

- Supports ITU-R BT.1120 up to 4*1080P@30fps

3.9   System Peripherals

3.9.1   Clock Controller Unit (CCU)

- 11 PLLs

- One on-chip RC oscillator

- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator

- Supports clock configuration and clock generation for corresponding modules

- Supports software-controlled clock gating and software-controlled reset for corresponding modules

3.9.2   DMAC

- Two 16-ch DMAs

- Provides 53 peripheral DMA requests for data reading and 53 peripheral DMA requests for data writing

- Transferring data with linked list

- Flexible data width: 8 bits, 16 bits, or 32 bits

- Programmable DMA burst length

- DRQ response includes waiting mode and handshake mode

- Supports non-aligned transform for memory devices

- DMA channels that support the following

  - Pausing DMA

  - I/O speed mode

3.9.3 I/O Memory Management Unit (IOMMU)

- Supports virtual address to physical address mapping by hardware implementation

- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI parallel address mapping

- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI bypass function independently

- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI pre-fetch independently

- Supports ISP, CSI, VE_MBUS0, VE_MBUS1, G2D, DE, and DI interrupt handing mechanism independently

- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)

- Supports TLB Fully cleared and Partially disabled

- Supports trigger PTW behavior when TLB miss

- Supports checking the permission

3.9.4 Message Box (MSGBOX)

- Supports communication between two CPUs through one way channels. Each CPU has one MSGBOX and can only read or write in one communication

  - CPUX_MSGBOX: CPUS/RISC-V/DSP write; ARM CPU read

  - CPUS_MSGBOX: ARM CPU/RISC-V/DSP write; CPUS read

  - DSP_MSGBOX: ARM CPU/RISC-V/CPUS write; DSP read

  - RISCV_MSGBOX: ARM CPU/CPUS/DSP write; RISC-V read

- The channel between two CPU has 4 channels, and the FIFO depth of a channel is 8 x 32 bits

- Supports interrupts

3.9.5 Power Reset Clock Management (PRCM)

- Two PRCMs: STBY_PRCM and MCU_PRCM

- 1 PLL

- Bus gating, bus reset, and module clock configuration

- RAM configure Control for STBY_PRCM

3.9.6   RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second

- External connect a 32.768 kHz low-frequency oscillator for count clock

- Timer frequency is 1 kHz

- Configurable initial value by software anytime

- Supports fanout function of internal 32K clock

- Supports timing alarm, and generates interrupt and wakeup the external devices

- 8 general purpose registers for storing power-off information in AON domain

3.9.7   Spinlock

- Supports 32 lock units

- Two kinds of lock status: locked and unlocked

- Lock time of the processor is predictable (less than 200 cycles)

3.9.8   Thermal Sensor Controller (THS)

- Two THS controllers
  - THS0, including THS0_0
  - THS1, including THS1_0, THS1_1, THS1_2, and THS1_3
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.9.9   Timer

- Configurable counting clock: 32KHz, 24MHz, 16MHz, or 200MHz

- Programmable 56-bit down timer

- Two working modes: periodic mode and single count mode

- Generates an interrupt when the count is decreased to 0

3.9.10   Watchdog Timer (WDT)

- Supports 12 initial values

- Supports the generation of timeout interrupts

- Supports the generation of reset signals

- Supports Watchdog Restart

3.10 Audio Subsystem

3.10.1 Audio Codec

- Two audio digital-to-analog converter (DAC) channels

    - 16-bit and 20-bit sample resolution

    - 8 kHz to 192 kHz DAC sample rate

    - 100 ± 2 dB SNR@A-weight, -85 ± 3 dB THD+N

- Three audio outputs

    - One stereo headphone output: HPOUTL/R

    - Two differential lineout output: LINEOUTLP/N and LINEOUTRP/N

- Three audio analog-to-digital converter (ADC) channels

    - 16-bit and 20-bit sample resolution

    - 8 kHz to 48 kHz ADC sample rate

    - 95 ± 3 dB SNR@A-weight, -80 ± 3 dB THD+N

- Three differential microphone inputs: MICIN1P/1N, MICIN2P/2N, and MICIN3P/3N (for echo reduction)

- Two low-noise analog microphone bias outputs: MBIAS and HBIAS

- Supports Dynamic Range Controller adjusting the DAC playback and ADC recording

- One 128x20-bits FIFO for DAC data transmit, one 128x20-bits FIFO for ADC data receive

- Programmable FIFO thresholds

- Supports interrupts and DMA

- Internal ALDO output for AVCC

3.10.2 I2S/PCM

- Four I2S/PCM external interfaces (I2S0, I2S1, I2S2, and I2S3) for connecting external power amplifier and MIC ADC

- Compliant with standard Philips Inter-IC sound (I2S) bus specification

    - Left-justified, Right-justified, PCM mode, and Time Division Multiplexing (TDM) format

    - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)

- FIFOs for transmitting and receiving data

    - Programmable FIFO thresholds

    - 128 depth x 32-bit width TXFIFO and 64 depth x 32-bit width RXFIFO

- Supports multiple function clocks

    - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and Peripheral I2S/PCM satisfy Timing Parameters)

    - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode

- Supports TX/RX DMA slave interface

- Supports multiple application scenarios

    - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8-bit to 32-bit

    - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width   24.576 MHz)

    - 8-bit u-law and 8-bit A-law companded sample

- Supports master/slave mode

3.10.3   DMIC

- Supports maximum 8 digital PDM microphones

- Supports sample rate from 8 kHz to 48 kHz

3.10.4   One Wire Audio (OWA)

- One OWA TX and One OWA RX

- Compliance with S/PDIF interface

- IEC-60958 and IEC-61937 transmitter and receiver functionality

- IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits

- TXFIFO and RXFIFO

    - One 128×24bits TXFIFO and one 64×24bits RXFIFO for audio data transfer

    - Programmable FIFO thresholds

- Supports TX/RX DMA slave interface

- Multiple function clock

    - Separate clock for OWA TX and OWA RX

    - The clock of TX function includes 24.576 MHz and 22.5792 MHz

    - The clock of RX function includes 24.576*8 MHz

- Supports Hardware Parity On TX/RX

    - Hardware Parity generation on the transmitter

- Hardware Parity checking on the receiver

- Supports channel status capture on the receiver

- Supports channel sample rate capture on the receiver

- Supports insertion detection for the receiver

- Supports channel status insertion for the transmitter

3.11 Security System

3.11.1   Crypto Engine (CE)

- Symmetrical algorithm:

  - AES symmetrical algorithm

    ➢ Key size: 128/192/256 bits

    ➢ CFB mode includes: CFB1, CFB8, CFB64, and CFB128

    ➢ CTR mode includes: CTR16, CTR32, CTR64, and CTR128

    ➢ Supports ECB, CBC, CTS, OFB, CBC-MAC, and GCM modes

  - DES symmetrical algorithm

    ➢ CTR mode, includes: CTR16, CTR32, and CTR64

    ➢ Supports ECB, CBC, and CBC-MAC mode

  - Supports 3DES

  - SM4 symmetrical algorithm supports ECB and CBC mode

- Hash algorithms

  - Support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3

  - Support HMAC-SHA1, HMAC-SHA256

- Random bit generator algorithms

  - Support PRNG, 175 bits seed width, and output with multiple of 5 words

  - Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words

- Public key algorithms

  - Support RSA public key algorithms: 512/1024/2048/3072/4096-bit width

  - Support ECC public key algorithms: 160/224/256/384/521-bit width

  - Support SM2 algorithms

3.11.2   Security ID (SID)

- 4 Kbits eFuse

- Supports secure and non-secure world in eFuse

- The register configuration of SID is always in non-secure world

- Backup eFuse information by using SID_SRAM

- One-time programming

- Selecting double-bit check by parameter definition

- Data scrambling

- Reading and writing protection

3.11.3   Secure Memory Control (SMC)

- The SMC is always secure, only secure CPUX can access the SMC

- Sets secure area of DRAM

- Supports Master and address protection

- Sets secure property that Master accesses to DRAM

- Sets DRM area

- Maximum 16 regions and Master has access to each region

3.11.4   Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC

- Sets secure property of peripherals

3.12 External Peripherals

3.12.1   CIR Receiver (CIR_RX)

- Two CIR_RX interfaces

- Full physical layer implementation

- Supports NEC format infra data

- Supports CIR for remote control

- 64x8 bits FIFO for data buffer

- Sample clock up to 1 MHz

3.12.2   CIR Transmitter (CIR_TX)

- One CIR_TX interface

- Full physical layer implementation

- Arbitrary wave generator

- Configurable carrier frequency

- Handshake mode and waiting mode of DMA

- 128 bytes FIFO for data buffer

- Supports Interrupts and DMA

3.12.3   GMAC

- One GMAC interface (GMAC0) for connecting to external Ethernet PHY

- 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces

- Compliant with the IEEE 802.3-2002 standard

- Supports both full-duplex and half-duplex operations

- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB

- Supports a variety of flexible address filtering modes

- Separate 32-bit status returned for transmission and reception packets

- Optimization for packet-oriented DMA transfers with frame delimiters

    - Supports linked-list descriptor list structure

    - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 2 KB of data

    - Comprehensive status reporting for normal operation and transfers with errors

- 2 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets

- Programmable interrupt options for different operational conditions

- Provides the management data input/output (MDIO) interface for PHY device configuration and management with configurable clock frequencies

3.12.4   GMAC200

- One GMAC interface (GMAC1) for connecting to external Ethernet PHY

- Compliant with the IEEE 802.3-2015 standard

- Supports 10/100/1000 Mbit/s data transfer rates

- Supports RMII/RGMII PHY interface

- AMBA4 AXI master interface with 64bit data transfer

- Supports both full-duplex and half-duplex operation

- Full-duplex flow control

- IEEE 1588-2008 for precision networked clock synchronization, support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008

- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB

- Source Address field and VLAN insertion or replacement, Double VLAN

- Transmit TCP/IP Checksum Offload

- Supports a variety of flexible address filtering modes (include Hash filter function)

- Optimization for packet-oriented DMA transfers with frame delimiters

  - Supports linked-list descriptor list structure

  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention: each descriptor can transfer up to 32 KB of data

  - Comprehensive status reporting for normal operation and transfers with errors

- Supports 4KB TXFIFO for transmission packets and 8KB RXFIFO for reception packets

- Supports 16 Descriptors Descriptor Pre-fetch cache for TXDMA and RX DMA

- Programmable interrupt options for different operational conditions

- Supports MDIO Interface for PHY device configuration and management

- Configurable big-endian and little-endian mode for Transmit and Receive paths

- Supports statistics on the received and transmitted packets

- Split Header Support

3.12.5   General Purpose ADC (GPADC)

- Two 12-ch SAR ADCs

- 64 FIFO depth of data register

- 12-bit sampling resolution and 10-bit precision

- Power reference voltage: VCC-ADC, analog input voltage range: 0 to 1.8V

- Maximum sampling frequency up to 1 MHz

- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

3.12.6   LEDC

- Configurable LED output high/low level width

- Configurable LED reset time

- LEDC data supports DMA configuration mode and CPU configuration mode

- Maximum 1024 LEDs serial connect

- Configurable interval time between data packets and frame data

- Configurable RGB display mode

3.12.7   Low Rate ADC (LRADC)

- 2-ch LRADC input

- 6-bit resolution

- Sampling rate up to 2 kHz

- Supports hold key and general key

- Supports normal, continue and single work mode

- Power supply voltage:1.8V, power reference voltage:1.35V

3.12.8   USB2.0 DRD

- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY

- Complies with USB2.0 Specification

- Supports static host operation:

  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0

  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a

  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)

  - Supports only 1 USB Root port shared between EHCI and OHCI

- Supports static device operation:

  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)

  - Supports bi-directional endpoint0 (EP0) for Control transfer

  - Up to 10 user-configurable endpoints (EP1 IN/OUT, EP2 IN/OUT, EP3 IN/OUT, EP4 IN/OUT, EP5 IN/OUT) for Bulk transfer, Isochronous transfer and Interrupt transfer

  - Up to (8 KB + 64 Bytes) FIFO for all EPs (including EP0)

  - Supports interface to an external Normal DMA controller for every EP

- Supports an internal DMA controller for data transfer with memory

- Supports High-Bandwidth Isochronous & Interrupt transfers

- Automated splitting/combining of packets for Bulk transfers

- Includes automatic PING capabilities

- Soft connect/disconnect function

- Hardware handles all data transfer

- Power optimization and power management capabilities

- Device and host controller share an 8K SRAM and a physical PHY

3.12.9   USB2.0 HOST

- One USB 2.0 HOST (USB1), with integrated USB 2.0 analog PHY

- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device

- Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0

- Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a

- Supports only 1 USB Root port shared between EHCI and OHCI

- An internal DMA Controller for data transfer with memory

- Supports the UTMI+ Level 3 interface and 8-bit bidirectional data buses

- Industry-standard AMBA High-Performance Bus (AHB), fully compliant with the AMBA Specification, Revision 2.0.

- 32-bit Little Endian AMBA AHB Slave Bus for Register Access

- 32-bit Little Endian AMBA AHB Master Bus for Memory Access

3.12.10   PCIe2.1&USB3.1 System

PCIe2.1&USB3.1 system contains 1 PCIe2.1&USB3.1 combo PHY, 1 PCIe2.1 controller and 1 USB3.1 DRD controller.

3.12.10.1   PCIe2.1

- Compliance to PCI Express Base Specification, Revision 2.1

- Supports Gen1(2.5 Gbit/s), Gen2 (5.0 Gbit/s) speed

- Supports 62.5MHz/125 MHz operation on PIPE interface for Gen1/Gen2, respectively

- Constant 32-bit PIPE width for Gen1/Gen2 modes

- Supports Root Complex (RC) mode

- Supports 1 lane link width

- Eight Traffic Classes (TC)

- Maximum payload size of 1K bytes

- 8 inbound and 8 outbound address translation regions

- 4 write/read channels for embedded DMA

- Maximum number of non-posted outstanding transactions: 32

- Supports Active State Power Management (ASPM)

- Supports Advanced Error Reporting (AER)

- Supports MSI interrupt

3.12.10.2   USB3.1 DRD

📖 **NOTE**

USB2.0 PHY and USB3.1 PHY share the same controller. They cannot be used simultaneously.

- One USB 2.0 UTMI+ PHY (USB2)

- One USB3.1 PIPE PHY (USB3)

- USB3.1 DRD Device mode supports the following:

  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY

  - High-Speed (HS, 480 Mbit/s) and Full-Speed (FS, 12-Mbit/s) for USB2.0 PHY

- USB3.1 DRD HOST mode supports the following:

  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY

  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) for USB2.0 PHY

- Supports Device or Host operation at a time

- AXI interface for DMA operation

- Reading and writing access to Control and Status Registers (CSRs) through AHB Slave interface

- Up to 10 Endpoints, including control Endpoint 0 in Device mode:

  - 5 IN Endpoints: User EP1 IN, EP2 IN, EP3 IN, EP4 IN, Control EP0 IN

  - 5 OUT Endpoints: User EP1 OUT, EP2 OUT, EP3 OUT, EP4 OUT, Control EP0 OUT

- Simultaneous IN and OUT transfer in Super-Speed mode

- Dual-port interfaces for TX data buffering, RX data prefetching, descriptor caching, and register caching

- Three RAMs: Rx data FIFO RAM, TX data FIFO RAM, and descriptor/register Cache RAM

- Hardware handles all data transfer

- Implements both static and dynamic power reduction techniques at multiple levels

3.12.11   PWM

- Up to 30 PWM channels and 4 PWM controllers

    - PWM0-[15:0] for PWM0 controller

    - PWM1- [3:0] for PWM1 controller

    - S-PWM0-[1:0] for S_PWM0 controller

    - MCU-PWM0-[7:0] for MCU_PWM0 controller

- Maximum 16 independent PWM channels for PWM controller

    - Supports PWM continuous mode output

    - Supports PWM pulse mode output, and the pulse number is configurable

    - Output frequency range:

        ➢ 0 to 24 MHz (when the clock source is DCXO24M)

        ➢ 0 to 100 MHz (when the clock source is APB1 clock)

    - Various duty-cycle: 0% to 100%

    - Minimum resolution: 1/65536

- Maximum 8 complementary pairs output for PWM controller

    - The pairing methods are as follows. The components are PWM output signals.

        ➢ Maximum 8 pairs for PWM0:

        PWM0-0 + PWM0-1, PWM0-2 + PWM0-3, PWM0-4 + PWM0-5, PWM0-6 + PWM0-7, PWM0-8 + PWM0-9, PWM0-10 + PWM0-11, PWM0-12 + PWM0-13, PWM0-14 + PWM0-15

        ➢ Maximum 2 pairs for PWM1:

        PWM1-0+PWM1-1, PWM1-2+PWM1-3

        ➢ Maximum 1 pair for S_PWM0:

        S-PWM0-0+ S-PWM0-1

        ➢ Maximum 4 pairs for MCU_PWM0:

        MCU-PWM0-0+ MCU-PWM0-1, MCU-PWM0-2+ MCU-PWM0-3, MCU-PWM0-4+ MCU-PWM0-5, MCU-PWM0-6+ MCU-PWM0-7

    - Supports dead-zone generator, and the dead-zone time is configurable

- Maximum 4 group of PWM channel output for controlling stepping motors

    - Supports any plural channels to form a group, and output the same duty-cycle pulse

    - In group mode, the relative phase of the output waveform for each channel is configurable

- Maximum 16 channels capture input

  - Supports rising edge detection and falling edge detection for input waveform pulse

  - Supports pulse-width measurement for input waveform pulse

3.12.12 SPI and SPI_DBI

- Up to 4 SPI controllers

  - SPI0, SPI2, and S_SPI0, supporting SPI mode

  - SPI1, supporting SPI mode and display bus interface (DBI) mode

SPI mode

- Multiple SPI modes:

  - Master mode and slave mode for standard SPI

  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI

  - Master mode for Quad-Output/Quad-Input SPI

  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits

- Maximum clock frequency: 100MHz

- TX/RX DMA slave interface

- 8-bit wide and 64-entry FIFO for both transmitting and receiving data

- Supports mode0, mode1, mode2, and mode3

- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

DBI mode

- DBI Type C 3 Line/4 Line Interface Mode

- 2 Data Lane Interface Mode

- RGB111/444/565/666/888 video format

- Maximum resolution of RGB666 240 x 320@30Hz with single data lane

- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane

- Tearing effect

- Software flexible control video frame rate

3.12.13 SPI Flash Controller (SPIFC)

- Supports multiple SPI modes

  - Standard SPI

  - Dual-Input/Dual-Output SPI and Dual-I/O SPI

- Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI

- Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI

- 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits

- Supports STR mode and DTR mode, and DTR mode supports DQS signal

- High Speed Clock Frequency

  - 150MHz for STR Mode

  - 100MHz for DTR Mode

- Software Write Protection

  - Write protection for all/portion of memory via software

  - Top/Bottom Block protection

- Programmable delay between transactions

- Support Mode0, Mode1, Mode2 and Mode3

- Support control signal configuration

  - Up to four chip selects to support multiple peripherals

  - Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

3.12.14 Two Wire Interface (TWI)

- Up to 9 TWI controllers

  - TWI0, TWI1, TWI2, TWI3, TWI4, and TWI5

  - S_TWI0, S_TWI1, and S_TWI2

- Compliant with I2C bus standard

- 7-bit and 10-bit device addressing modes

- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)

- Supports general call and start byte

- Master mode supports the following:

  - Bus arbitration in the case of multiple master devices

  - Clock synchronization and bit and byte waiting

  - Packet transmission and DMA

- Slave mode supports Interrupt on address detection

3.12.15 UART

- Up to 10 UART controllers
  - UART0, UART1, UART2, UART3, UART4, UART5, UART6, and UART7
  - S_UART0 and S_UART1
- Compatible with industry-standard 16450/16550 UARTs
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes for UART0, S_UART0, and S_UART1
  - Each of them is 128 bytes for UART1, UART2, UART3, UART4, UART5, UART6, and UART7
- The working reference clock is from the APB bus clock
  - Speed up to 10 Mbit/s with 160 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 5 Mbit/s with 80 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 3.75 Mbit/s with 60 MHz APB clock (excluding S_UART0 and S_UART1)
  - Speed up to 1.5 Mbit/s with 24 MHz APB clock
- 5 to 8 data bits for RS-232 format, or 9 bits RS-485 format
- 1, 1.5 or 2 stop bits
- Programmable parity (even, odd, or no parity)
- Supports TX/RX DMA slave controller interface
- Supports software/hardware flow control
- Supports IrDA-compatible slow infrared (SIR) format
- Supports auto-flow by using CTS & RTS (excluding UART0, S_UART0, and S_UART1)

3.13 Package

HS-FCBGA 664balls, 17 mm x 17 mm size, 1.844 mm height (maximum), 0.5 mm ball pitch, 0.3 mm ball size

4   Block Diagram

The following figure shows the system block diagram of the T527.

Figure 4-1 T527 System Block Diagram

| HiFi4 DSP |
| RISC-V 200 MHz |
| NPU 2 TOPS(1) |
| G57 MC01 |

ARM Cortex™-A55 x 4

| L1 I-Cache 32 KB | L1 D-Cache 32 KB |
| L2 Cache 64 KB |

ARM Cortex™-A55 x 4

| L1 I-Cache 32 KB | L1 D-Cache 32 KB |
| L2 Cache 128 KB |

L3 Cache 1 MB

Connectivity

- CAN x 2
- USB2.0 HOST
- USB2.0 DRD
- USB3.1 DRD & PCIe2.1
- SDIO3.0
- SPI x4 (Supports SPI Nand/Nor Flash)
- TWI x 9
- UART x 10
- 10M/100M/1000M GMAC x 2
- GPADC (24-ch)
- LRADC (2-ch)
- PWM (30-ch)
- LEDC
- CIR TX x 1
- CIR RX x 2
- SPIF (Octal I/O)

Video Input
- 8/10/12/16-bit Parallel CSI
- MIPI CSI (4+4-lane/4+2+2-lane/2+2+2-lane)

Video Output
- HDMI2.0 TX
- 4+4-lane MIPI DSI
- RGB x 2
- LVDS x 4
- eDP1.3

Audio
- Audio Codec
- I2S/PCM x 4
- DMIC
- OWA IN/OUT

Display Engine
- DE
- DI
- G2D

Video Engine
- Video Decoding 4K@60fps H.265 4K@30fps H.264
- Video Encoding 4K@25fps H.264

Memory
- 32 bits DDR3/DDR3L/LPDDR3/ DDR4/LPDDR4/LPDDR4x
- SD3.0/eMMC5.1
- RAW NAND Flash

Internal System
- CCU
- GIC/CLIC
- DMA
- Thermal Sensor
- Timer
- Watchdog Timer
- IOMMU

Security System
- Crypto Engine
- Security ID
- Trustzone
- Secure Boot

(1) Some modules shown in this block diagram are not offered on all devices, please refer to Table 2-1 Device Summary for details.

The following figure shows the typical application of the T527.

Figure 4-2 Typical Application
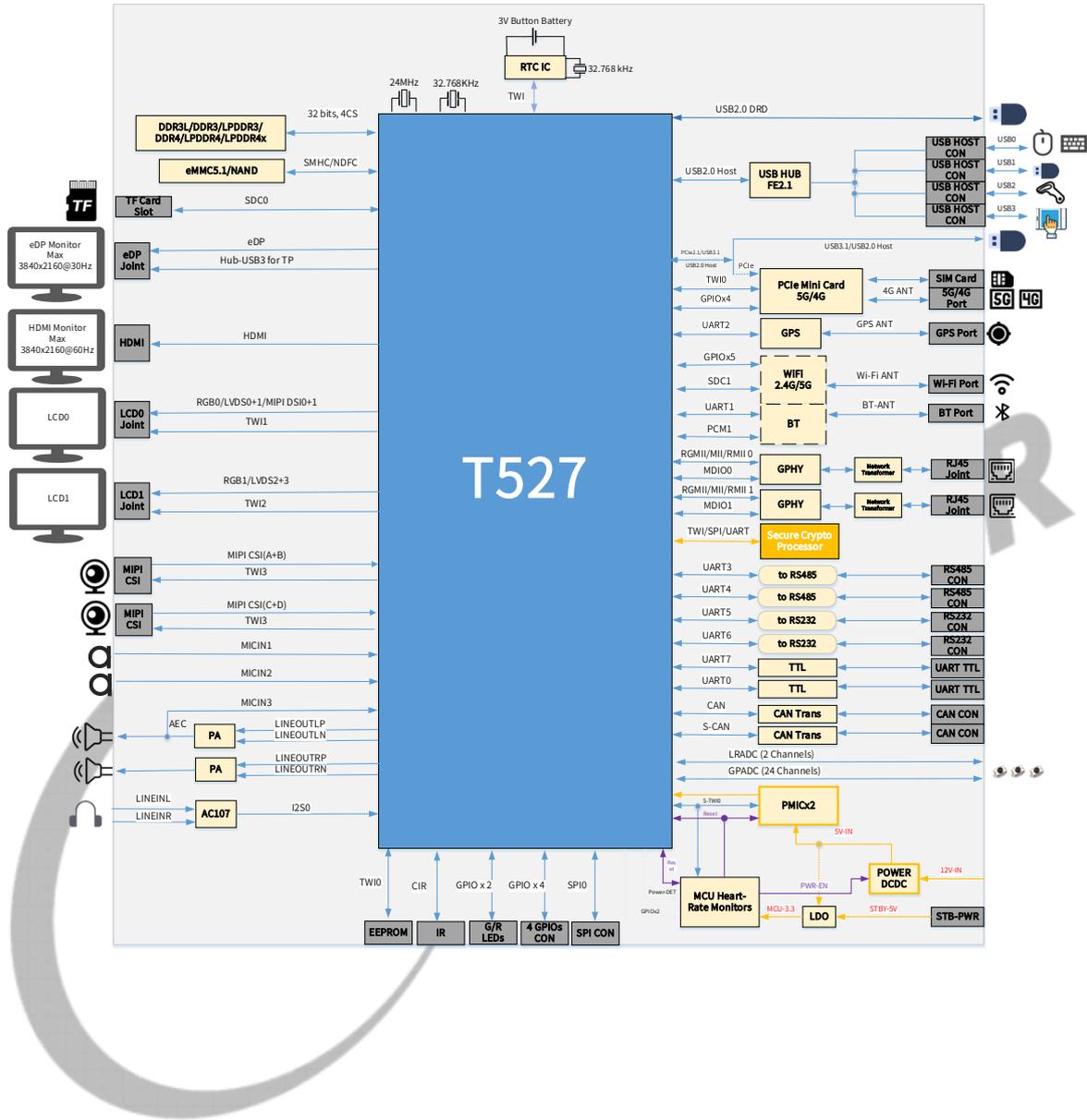
5 Pin Description

5.1 Pin Quantity

The following table lists the pin quantity of the T527.

Table 5-1 T527 Pin Quantity

Pin Type	Quantity
I/O	377
Power	71
DDR power	13
Ground	196
NC	7
Total	664

5.2 Pin Characteristics

The following tables list the characteristics of the T527 pins from the following seven aspects.

[1] **Ball#**: Package ball numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

   NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

   I (Input),

   O (Output),

   I/O (Input/Output),

   OD (Open-Drain),

   A (Analog),

   AI (Analog Input),

   AO (Analog Output),

   P (Power),

   G (Ground)

   N/A (Not Applicable)

[4] Ball Reset State: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] Default Buffer Strength: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] I/O Power Supply: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

5.2.1　SDRAM

Table 5-2 SDRAM Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AK33	SA0	O	VCC-DRAM/VCC-DRAML
AG30	SA1	O	VCC-DRAM/VCC-DRAML
AJ33	SA2	O	VCC-DRAM/VCC-DRAML
AL27	SA3	O	VCC-DRAM/VCC-DRAML
AH25	SA4	O	VCC-DRAM/VCC-DRAML
AK27	SA5	O	VCC-DRAM/VCC-DRAML
AN27	SA6	O	VCC-DRAM/VCC-DRAML
AM33	SA7	O	VCC-DRAM/VCC-DRAML
AL25	SA8	O	VCC-DRAM/VCC-DRAML
AJ31	SA9	O	VCC-DRAM/VCC-DRAML
AG29	SA10	O	VCC-DRAM/VCC-DRAML
AJ32	SA11	O	VCC-DRAM/VCC-DRAML

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AL31	SA12	O	VCC-DRAM/VCC-DRAML
AK29	SA13	O	VCC-DRAM/VCC-DRAML
AM28	SA14	O	VCC-DRAM/VCC-DRAML
AN29	SA15	O	VCC-DRAM/VCC-DRAML
AJ27	SA16	O	VCC-DRAM/VCC-DRAML
AJ30	SA17	O	VCC-DRAM/VCC-DRAML
AL29	SACT	O	VCC-DRAM/VCC-DRAML
AK25	SBA0	O	VCC-DRAM/VCC-DRAML
AJ25	SBA1	O	VCC-DRAM/VCC-DRAML
AN26	SBG0	O	VCC-DRAM/VCC-DRAML
AM27	SBG1	O	VCC-DRAM/VCC-DRAML
AM31	SCKE0	O	VCC-DRAM/VCC-DRAML
AM30	SCKP	O	VCC-DRAM/VCC-DRAML
AN30	SCKN	O	VCC-DRAM/VCC-DRAML
AN32	SCS0	O	VCC-DRAM/VCC-DRAML
AM32	SCS1	O	VCC-DRAM/VCC-DRAML
AE28	SDQ0	I/O	VCC-DRAM/VCC-DRAML
AE27	SDQ1	I/O	VCC-DRAM/VCC-DRAML
AG32	SDQ2	I/O	VCC-DRAM/VCC-DRAML
AH33	SDQ3	I/O	VCC-DRAM/VCC-DRAML
AE30	SDQ4	I/O	VCC-DRAM/VCC-DRAML
AD32	SDQ5	I/O	VCC-DRAM/VCC-DRAML
AE31	SDQ6	I/O	VCC-DRAM/VCC-DRAML
AD33	SDQ7	I/O	VCC-DRAM/VCC-DRAML
AC27	SDQ8	I/O	VCC-DRAM/VCC-DRAML
AC28	SDQ9	I/O	VCC-DRAM/VCC-DRAML
AC30	SDQ10	I/O	VCC-DRAM/VCC-DRAML
AC31	SDQ11	I/O	VCC-DRAM/VCC-DRAML
AA33	SDQ12	I/O	VCC-DRAM/VCC-DRAML
AA31	SDQ13	I/O	VCC-DRAM/VCC-DRAML
AA28	SDQ14	I/O	VCC-DRAM/VCC-DRAML
AA27	SDQ15	I/O	VCC-DRAM/VCC-DRAML
AM25	SDQ16	I/O	VCC-DRAM/VCC-DRAML

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AN25	SDQ17	I/O	VCC-DRAM/VCC-DRAML
AH23	SDQ18	I/O	VCC-DRAM/VCC-DRAML
AK23	SDQ19	I/O	VCC-DRAM/VCC-DRAML
AL23	SDQ20	I/O	VCC-DRAM/VCC-DRAML
AM22	SDQ21	I/O	VCC-DRAM/VCC-DRAML
AN21	SDQ22	I/O	VCC-DRAM/VCC-DRAML
AG21	SDQ23	I/O	VCC-DRAM/VCC-DRAML
AG19	SDQ24	I/O	VCC-DRAM/VCC-DRAML
AH19	SDQ25	I/O	VCC-DRAM/VCC-DRAML
AK19	SDQ26	I/O	VCC-DRAM/VCC-DRAML
AL19	SDQ27	I/O	VCC-DRAM/VCC-DRAML
AM21	SDQ28	I/O	VCC-DRAM/VCC-DRAML
AL21	SDQ29	I/O	VCC-DRAM/VCC-DRAML
AK21	SDQ30	I/O	VCC-DRAM/VCC-DRAML
AH21	SDQ31	I/O	VCC-DRAM/VCC-DRAML
AE33	SDQM0	I/O	VCC-DRAM/VCC-DRAML
AC32	SDQM1	I/O	VCC-DRAM/VCC-DRAML
AM24	SDQM2	I/O	VCC-DRAM/VCC-DRAML
AN20	SDQM3	I/O	VCC-DRAM/VCC-DRAML
AF32	SDQS0P	I/O	VCC-DRAM/VCC-DRAML
AF33	SDQS0N	I/O	VCC-DRAM/VCC-DRAML
AB32	SDQS1P	I/O	VCC-DRAM/VCC-DRAML
AB33	SDQS1N	I/O	VCC-DRAM/VCC-DRAML
AM23	SDQS2P	I/O	VCC-DRAM/VCC-DRAML
AN23	SDQS2N	I/O	VCC-DRAM/VCC-DRAML
AM19	SDQS3P	I/O	VCC-DRAM/VCC-DRAML
AN19	SDQS3N	I/O	VCC-DRAM/VCC-DRAML
AL32	SODT0	O	VCC-DRAM/VCC-DRAML
AL33	SODT1	O	VCC-DRAM/VCC-DRAML
AG23	SRST	O	VCC-DRAM/VCC-DRAML
AA29	SZQ	AI	VCC-DRAM/VCC-DRAML
W23, W24, W25, Y24, AA24, AB24, AC24	VCC-DRAM	P	N/A

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AC17, AC18, AC19, AC20, AC22	VCC-DRAML	P	N/A
AD25	VDD18-DRAM	P	N/A

5.2.2 System

Table 5-3 System Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	I/O Power Supply[6]
F16	FEL	I	PU	PU	VCC-IO
G16	JTAG-SEL	I	PU	PU	VCC-IO
AM10	NMI	I/O, OD	N/A	N/A	VCC-RTC
AJ11	RESET	I/O, OD	N/A	N/A	VCC-RTC

5.2.3 RTC&PLL

Table 5-4 RTC&PLL Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AL11	X32KFOUT	AO, OD	VCC-PM
AM12	X32KIN	AI	VCC-RTC
AM11	X32KOUT	AO	VCC-RTC
AE13	VCC-RTC	P	N/A
AG15	VCC-PLL	P	N/A

5.2.4 DCXO

Table 5-5 DCXO Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AM13	DXIN	AI	VCC-DCXO
AN13	DXOUT	AO	VCC-DCXO
AM14	REFCLK-OUT	AO	VCC-DCXO
AK13	WREQIN	I	VCC-PG
AD15	VCC-DCXO	P	N/A

5.2.5 USB2.0 DRD

Table 5-6 USB2.0 DRD Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
A24	USB0-DP	A I/O	VCC33-USB
B24	USB0-DM	A I/O	VCC33-USB
G22	USB0-REXT	AO	VCC33-USB

5.2.6 USB2.0 Host

Table 5-7 USB2.0 Host Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
D24	USB1-DP	A I/O	VCC33-USB
E24	USB1-DM	A I/O	VCC33-USB
G24	USB1-REXT	AO	VCC33-USB
K19	VCC33-USB	P	N/A
J19	VCC33-18-USB	P	N/A
L18	VDD09-USB	P	N/A

5.2.7 PCIe2.1&USB3.1 DRD

Table 5-8 PCIe2.1&USB3.1 DRD Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
D22	USB2-DP	A I/O	VCC33-USB-2
E22	USB2-DM	A I/O	VCC33-USB-2
G20	USB2-REXT	AO	VCC33-USB-2
B21	PCIE-REF-CLKP	A I/O	VCC18-PCIE
C21	PCIE-REF-CLKN	A I/O	VCC18-PCIE
E20	PCIE-REXT	AO	VCC18-PCIE
B23	PCIE-RX0-DP/USB3-RXP	AI	VCC18-PCIE
C23	PCIE-RX0-DN/USB3-RXN	AI	VCC18-PCIE
A22	PCIE-TX0-DP/USB3-TXP	AO	VCC18-PCIE
B22	PCIE-TX0-DN/USB3-TXN	AO	VCC18-PCIE
L17	VCC33-USB-2	P	N/A
J18	VCC33-18-USB-2	P	N/A
J15	VCC18-PCIE	P	N/A

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
J16	VDD09-PCIE	P	N/A

5.2.8   eDP1.3

Table 5-9 eDP1.3 Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
C32	EDP-AUXP	A I/O	VCC18-EDP
C33	EDP-AUXN	A I/O	VCC18-EDP
C29	EDP-HPD	AI	VCC18-EDP
F28	EDP-REXT	AO	VCC18-EDP
A29	EDP-TX0P	AO	VCC18-EDP
B29	EDP-TX0N	AO	VCC18-EDP
A30	EDP-TX1P	AO	VCC18-EDP
B30	EDP-TX1N	AO	VCC18-EDP
A31	EDP-TX2P	AO	VCC18-EDP
B31	EDP-TX2N	AO	VCC18-EDP
B32	EDP-TX3P	AO	VCC18-EDP
B33	EDP-TX3N	AO	VCC18-EDP
L22	VCC18-EDP	P	N/A
M22	VDD09-EDP	P	N/A

5.2.9   HDMI

Table 5-10 HDMI Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
E28	HCEC	I/O	VCC18-HDMI
D28	HHPD	I/O	VCC18-HDMI
F26	HREXT	I/O	VCC18-HDMI
D26	HSCL	O	VCC18-HDMI
E26	HSDA	I/O	VCC18-HDMI
B27	HTX0P	AO	VCC18-HDMI
C27	HTX0N	AO	VCC18-HDMI
A26	HTX1P	AO	VCC18-HDMI
B26	HTX1N	AO	VCC18-HDMI

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
B25	HTX2P	AO	VCC18-HDMI
C25	HTX2N	AO	VCC18-HDMI
A28	HTXCP	AO	VCC18-HDMI
B28	HTXCN	AO	VCC18-HDMI
M21	VCC18-HDMI	P	N/A
L21	VDD09-HDMI	P	N/A

5.2.10 Audio Codec

Table 5-11 Audio Codec Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AD2	MICIN1P	AI	AVCC
AD1	MICIN1N	AI	AVCC
AE2	MICIN2P	AI	AVCC
AE1	MICIN2N	AI	AVCC
AF2	MICIN3P	AI	AVCC
AF1	MICIN3N	AI	AVCC
AG2	LINEOUTLP	AO	AVCC
AG1	LINEOUTLN	AO	AVCC
AH2	LINEOUTRP	AO	AVCC
AH1	LINEOUTRN	AO	AVCC
AL2	HPOUTL	AO	CPVIN
AM2	HPOUTR	AO	CPVIN
AM1	HPOUTFB	AI	CPVIN
AJ1	MIC-DET	AI	AVCC
AJ2	HP-DET	AI	AVCC
AL1	HBIAS	AO	VDD33
AK1	MBIAS	AO	VDD33
AG5	VRA1	AO	AVCC
AG4	VRA2	AO	AVCC
AC7	VRP	P	N/A
AJ3	CPVDD	P	N/A
AK2	CPVEE	P	N/A

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AJ5	CPVIN	P	N/A
AB9	AVCC	P	N/A
AE7	ALDO-OUT	P	N/A
AC9	VDD33	P	N/A
AJ4	VEE	P	N/A
AE3	AGND	G	N/A

5.2.11　GPADC

Table 5-12 GPADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
W1	GPADC0	AI	VCC-ADC
W2	GPADC1	AI	VCC-ADC
W3	GPADC2	AI	VCC-ADC
W4	GPADC3	AI	VCC-ADC
W5	GPADC4	AI	VCC-ADC
W6	GPADC5	AI	VCC-ADC
Y2	GPADC6	AI	VCC-ADC
Y3	GPADC7	AI	VCC-ADC
AA1	GPADC8	AI	VCC-ADC
AA2	GPADC9	AI	VCC-ADC
AA3	GPADC10	AI	VCC-ADC
AA4	GPADC11	AI	VCC-ADC
AA5	GPADC12	AI	VCC-ADC
AA6	GPADC13	AI	VCC-ADC
AB2	GPADC14	AI	VCC-ADC
AB3	GPADC15	AI	VCC-ADC
AC2	GPADC16	AI	VCC-ADC
AC3	GPADC17	AI	VCC-ADC
AC4	GPADC18	AI	VCC-ADC
AC5	GPADC19	AI	VCC-ADC
AC6	GPADC20	AI	VCC-ADC
AE4	GPADC21	AI	VCC-ADC

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
AE5	GPADC22	AI	VCC-ADC
AE6	GPADC23	AI	VCC-ADC
Y9	VCM-ADC	A I/O	VCC-ADC
Y10	VREFN-ADC	P	N/A
AA9	VREFP-ADC	P	N/A
W7	VCC-ADC	P	N/A
AA7	GND-ADC	G	N/A

5.2.12   LRADC

Table 5-13 LRADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	I/O Power Supply[4]
V3	LRADC0	AI	VCC-ADC
V2	LRADC1	AI	VCC-ADC

5.2.13   Power

Table 5-14 Power Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]
L15	VCC-IO	P
R26	VCC-EFUSE	P
AC15	VDD-CPUS	P
T19, T21, T22, U18, U19, U21, U22	VDD-CPUB	P
W19, W21, Y19, Y21	VDD-CPUL	P
R15, R17, R18	VDD-SYS	P
N21, P21, P22	VDD-DE	P
N13, P13	VDD-VE	P
T11, T13, U12, U13	VDD-GPU	P
Y12, Y13, AA12, AA13	VDD-DNR	P
R22	VDD-CPUBFB	P
AA19	VDD-CPULFB	P
P18	VDD-SYSFB	P
AB13	VDD-DNRFB	P

5.2.14 GPIO Groups

5.2.14.1 Port B

Table 5-15 Port B Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
N28	PB0	I/O	Z	PU/PD	4 mA	VCC-IO
N29	PB1	I/O	Z	PU/PD	4 mA	VCC-IO
M31	PB2	I/O	Z	PU/PD	4 mA	VCC-IO
M32	PB3	I/O	Z	PU/PD	4 mA	VCC-IO
N31	PB4	I/O	Z	PU/PD	4 mA	VCC-IO
N32	PB5	I/O	Z	PU/PD	4 mA	VCC-IO
N33	PB6	I/O	Z	PU/PD	4 mA	VCC-IO
P31	PB7	I/O	Z	PU/PD	4 mA	VCC-IO
P32	PB8	I/O	Z	PU/PD	4 mA	VCC-IO
R28	PB9	I/O	Z	PU/PD	4 mA	VCC-IO
R29	PB10	I/O	Z	PU/PD	4 mA	VCC-IO
R30	PB11	I/O	Z	PU/PD	4 mA	VCC-IO
R31	PB12	I/O	Z	PU/PD	4 mA	VCC-IO
R32	PB13	I/O	Z	PU/PD	4 mA	VCC-IO
R33	PB14	I/O	Z	PU/PD	4 mA	VCC-IO

5.2.14.2 Port C

Table 5-16 Port C Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
W28	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
Y31	PC1	I/O	Z	PU/PD	4 mA	VCC-PC
U30	PC2	I/O	Z	PU/PD	4 mA	VCC-PC
U29	PC3	I/O	Z	PU	4 mA	VCC-PC
U28	PC4	I/O	Z	PU	4 mA	VCC-PC
Y32	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
W33	PC6	I/O	Z	PU	4 mA	VCC-PC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
W29	PC7	I/O	Z	PU	4 mA	VCC-PC
W32	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
W31	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
V32	PC10	I/O	Z	PU/PD	4 mA	VCC-PC
V31	PC11	I/O	Z	PU/PD	4 mA	VCC-PC
U33	PC12	I/O	Z	PU/PD	4 mA	VCC-PC
U32	PC13	I/O	Z	PU/PD	4 mA	VCC-PC
U31	PC14	I/O	Z	PU/PD	4 mA	VCC-PC
T32	PC15	I/O	Z	PU/PD	4 mA	VCC-PC
T31	PC16	I/O	Z	PU/PD	4 mA	VCC-PC
U26	VCC-PC	P	N/A	N/A	N/A	N/A

5.2.14.3 Port D

Table 5-17 Port D Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
D32	PD0	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
D33	PD1	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
E30	PD2	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
E31	PD3	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
E32	PD4	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
E33	PD5	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
F32	PD6	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
F33	PD7	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
G30	PD8	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
G31	PD9	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
G32	PD10	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
G33	PD11	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
H31	PD12	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
H32	PD13	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
J29	PD14	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
J30	PD15	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
J32	PD16	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
J33	PD17	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
K31	PD18	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
K32	PD19	I/O	Z	PU/PD	4 mA	VCC-PD/VCC-LVDS0
L28	PD20	I/O	Z	PU/PD	4 mA	VCC-PD
L29	PD21	I/O	Z	PU/PD	4 mA	VCC-PD
L31	PD22	I/O	Z	PU/PD	4 mA	VCC-PD
L32	PD23	I/O	Z	PU/PD	4 mA	VCC-PD
L26	VCC-PD	P	N/A	N/A	N/A	N/A
N24	VCC-LVDS0	P	N/A	N/A	N/A	N/A

5.2.14.4   Port E

Table 5-18 Port E Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	I/O Power Supply[7]
E6	PE0	I/O	Z	PU/PD	4 mA	VCC-PE
C4	PE1	I/O	Z	PU/PD	4 mA	VCC-PE
E5	PE2	I/O	Z	PU/PD	4 mA	VCC-PE
E4	PE3	I/O	Z	PU/PD	4 mA	VCC-PE
C3	PE4	I/O	Z	PU/PD	4 mA	VCC-PE
B3	PE5	I/O	Z	PU/PD	4 mA	VCC-PE
A3	PE6	I/O	Z	PU/PD	4 mA	VCC-PE
A2	PE7	I/O	Z	PU/PD	4 mA	VCC-PE
B2	PE8	I/O	Z	PU/PD	4 mA	VCC-PE
B1	PE9	I/O	Z	PU/PD	4 mA	VCC-PE
C2	PE10	I/O	Z	PU/PD	4 mA	VCC-PE
J7	PE11	I/O	Z	PU/PD	4 mA	VCC-PE
C1	PE12	I/O	Z	PU/PD	4 mA	VCC-PE
G6	PE13	I/O	Z	PU/PD	4 mA	VCC-PE
L7	PE14	I/O	Z	PU/PD	4 mA	VCC-PE

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	I/O Power Supply[7]
N7	PE15	I/O	Z	PU/PD	4 mA	VCC-PE
L9	VCC-PE	P	N/A	N/A	N/A	N/A

5.2.14.5　Port F

Table 5-19 Port F Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B20	PF0	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI
A20	PF1	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI
C19	PF2	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI
B19	PF3	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI
B18	PF4	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI
A18	PF5	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI
D20	PF6	I/O	Z	PU/PD	4 mA	VCC-IO/VCC-MCSI

📖 NOTE

I/Os in Port F are supplied by VCC-IO when using 3.3 V voltage and are supplied by VCC-MCSI when using 1.8 V voltage.

5.2.14.6　Port G

Table 5-20 Port G Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
R1	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
R2	PG1	I/O	Z	PU	4 mA	VCC-PG
P3	PG2	I/O	Z	PU	4 mA	VCC-PG
P2	PG3	I/O	Z	PU	4 mA	VCC-PG
T3	PG4	I/O	Z	PU	4 mA	VCC-PG
T2	PG5	I/O	Z	PU	4 mA	VCC-PG

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
R6	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
R5	PG7	I/O	Z	PU/PD	4 mA	VCC-PG
R4	PG8	I/O	Z	PU/PD	4 mA	VCC-PG
U6	PG9	I/O	Z	PU/PD	4 mA	VCC-PG
U5	PG10	I/O	Z	PU/PD	4 mA	VCC-PG
U4	PG11	I/O	Z	PU/PD	4 mA	VCC-PG
U3	PG12	I/O	Z	PU/PD	4 mA	VCC-PG
U2	PG13	I/O	Z	PU/PD	4 mA	VCC-PG
U1	PG14	I/O	Z	PU/PD	4 mA	VCC-PG
T9	VCC-PG	P	N/A	N/A	N/A	N/A

5.2.14.7　Port H

Table 5-21 Port H Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
F18	PH0	I/O	Z	PU/PD	4 mA	VCC-IO
E18	PH1	I/O	Z	PU/PD	4 mA	VCC-IO
D18	PH2	I/O	Z	PU/PD	4 mA	VCC-IO
C17	PH3	I/O	Z	PU/PD	4 mA	VCC-IO
B17	PH4	I/O	Z	PU/PD	4 mA	VCC-IO
E16	PH5	I/O	Z	PU/PD	4 mA	VCC-IO
G12	PH6	I/O	Z	PU/PD	4 mA	VCC-IO
F14	PH7	I/O	Z	PU/PD	4 mA	VCC-IO
D16	PH8	I/O	Z	PU/PD	4 mA	VCC-IO
C16	PH9	I/O	Z	PU/PD	4 mA	VCC-IO
B16	PH10	I/O	Z	PU/PD	4 mA	VCC-IO
A16	PH11	I/O	Z	PU/PD	4 mA	VCC-IO
C15	PH12	I/O	Z	PU/PD	4 mA	VCC-IO
B15	PH13	I/O	Z	PU/PD	4 mA	VCC-IO
E14	PH14	I/O	Z	PU/PD	4 mA	VCC-IO
D14	PH15	I/O	Z	PU/PD	4 mA	VCC-IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B14	PH16	I/O	Z	PU/PD	4 mA	VCC-IO
B13	PH17	I/O	Z	PU/PD	4 mA	VCC-IO
A14	PH18	I/O	Z	PU/PD	4 mA	VCC-IO
C13	PH19	I/O	Z	PU/PD	4 mA	VCC-IO

5.2.14.8   Port I

Table 5-22 Port I Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AH13	PI0	I/O	Z	PU/PD	4 mA	VCC-PI
AG13	PI1	I/O	Z	PU/PD	4 mA	VCC-PI
AL15	PI2	I/O	Z	PU/PD	4 mA	VCC-PI
AN15	PI3	I/O	Z	PU/PD	4 mA	VCC-PI
AM15	PI4	I/O	Z	PU/PD	4 mA	VCC-PI
AJ15	PI5	I/O	Z	PU/PD	4 mA	VCC-PI
AK15	PI6	I/O	Z	PU/PD	4 mA	VCC-PI
AH15	PI7	I/O	Z	PU/PD	4 mA	VCC-PI
AL16	PI8	I/O	Z	PU/PD	4 mA	VCC-PI
AM16	PI9	I/O	Z	PU/PD	4 mA	VCC-PI
AN17	PI10	I/O	Z	PU/PD	4 mA	VCC-PI
AM17	PI11	I/O	Z	PU/PD	4 mA	VCC-PI
AL17	PI12	I/O	Z	PU/PD	4 mA	VCC-PI
AK17	PI13	I/O	Z	PU/PD	4 mA	VCC-PI
AM18	PI14	I/O	Z	PU/PD	4 mA	VCC-PI
AH17	PI15	I/O	Z	PU/PD	4 mA	VCC-PI
AJ17	PI16	I/O	Z	PU/PD	4 mA	VCC-PI
AE16	VCC-PI	P	N/A	N/A	N/A	N/A

5.2.14.9 Port J

Table 5-23 Port J Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
D1	PJ0	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
D2	PJ1	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
E1	PJ2	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
E2	PJ3	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
F1	PJ4	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
F2	PJ5	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
G1	PJ6	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
G2	PJ7	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
H2	PJ8	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
H3	PJ9	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
G4	PJ10	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
G5	PJ11	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
J4	PJ12	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
J5	PJ13	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
L4	PJ14	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
L5	PJ15	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
J1	PJ16	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
J2	PJ17	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
N4	PJ18	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
N5	PJ19	I/O	Z	PU/PD	4 mA	VCC-PJ/VCC-LVDS1
K3	PJ20	I/O	Z	PU/PD	4 mA	VCC-PJ
K2	PJ21	I/O	Z	PU/PD	4 mA	VCC-PJ
L2	PJ22	I/O	Z	PU/PD	4 mA	VCC-PJ
L1	PJ23	I/O	Z	PU/PD	4 mA	VCC-PJ
M3	PJ24	I/O	Z	PU/PD	4 mA	VCC-PJ
M2	PJ25	I/O	Z	PU/PD	4 mA	VCC-PJ
N2	PJ26	I/O	Z	PU/PD	4 mA	VCC-PJ
N1	PJ27	I/O	Z	PU/PD	4 mA	VCC-PJ
P9	VCC-PJ	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
N9	VCC-LVDS1	P	N/A	N/A	N/A	N/A

5.2.14.10　Port K

Table 5-24 Port K Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
A12	PK0	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B12	PK1	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B11	PK2	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
C11	PK3	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A10	PK4	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B10	PK5	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
E12	PK6	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
D12	PK7	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
E10	PK8	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
D10	PK9	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
E8	PK10	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
D8	PK11	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B9	PK12	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
C9	PK13	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A8	PK14	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B8	PK15	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B7	PK16	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
C7	PK17	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A6	PK18	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B6	PK19	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A5	PK20	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B5	PK21	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
A4	PK22	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
B4	PK23	I/O	Z	PU/PD	4 mA	VCC-PK/VCC-MCSI
M10	VCC-PK	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
K13	VCC-MCSI	P	N/A	N/A	N/A	N/A

5.2.14.11 Port L

Table 5-25 Port L Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AN6	PL0	I/O	Z	PU	4 mA	VCC-PL
AN5	PL1	I/O	Z	PU	4 mA	VCC-PL
AN7	PL2	I/O	Z	PU/PD	4 mA	VCC-PL
AM6	PL3	I/O	Z	PU/PD	4 mA	VCC-PL
AM7	PL4	I/O	Z	PU/PD	4 mA	VCC-PL
AL7	PL5	I/O	Z	PU/PD	4 mA	VCC-PL
AN8	PL6	I/O	Z	PU/PD	4 mA	VCC-PL
AM8	PL7	I/O	Z	PU/PD	4 mA	VCC-PL
AN9	PL8	I/O	Z	PU/PD	4 mA	VCC-PL
AM9	PL9	I/O	Z	PU/PD	4 mA	VCC-PL
AK9	PL10	I/O	Z	PU/PD	4 mA	VCC-PL
AJ9	PL11	I/O	Z	PU/PD	4 mA	VCC-PL
AK7	PL12	I/O	Z	PU/PD	4 mA	VCC-PL
AJ7	PL13	I/O	Z	PU/PD	4 mA	VCC-PL
AE11	VCC-PL	P	N/A	N/A	N/A	N/A

5.2.14.12 Port M

Table 5-26 Port M Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	I/O Power Supply[7]
AN3	PM0	I/O	Z	PU/PD	4 mA	VCC-PM
AN2	PM1	I/O	Z	PU/PD	4 mA	VCC-PM
AM4	PM2	I/O	Z	PU/PD	4 mA	VCC-PM
AM3	PM3	I/O	Z	PU/PD	4 mA	VCC-PM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	I/O Power Supply[7]
AN4	PM4	I/O	Z	PU/PD	4 mA	VCC-PM
AL5	PM5	I/O	Z	PU/PD	4 mA	VCC-PM
AG9	VCC-PM	P	N/A	N/A	N/A	N/A

5.2.15   Ground

Table 5-27 Ground Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]
A32, A33, C22, C24, C26, C28, C30, C31, E29, F22, F24, G26, G28, H24, J17, J21, J22, J23, J26, K15, K16, K21, K22, K24, K25, L16, L19, L24, M16, M18, M19	AVSS	G
A1, C6, C8, C10, C12, C14, C18, C20, D6, E3, F6, F8, F10, F12, G3, G8, G10, G14, G18, G29, J3, J6, J9, J10, J12, J13, J28, J31, K9, K10, K11, K12, K26, L3, L6, L10, L12, L13, L27, L30, L33, M13, N3, N6, N10, N12, N15, N18, N19, N22, N26, N27, N30, P11, P16, P19, P24, R3, R7, R11, R13, R19, R24, R27, T15, T16, T18, T24, U7, U14, U16, U25, U27, V18, V19, W12, W13, W15, W16, W22, W27, W30, Y15, Y18, Y22, Y23, Y26, AA15, AA16, AA18, AA21, AA22, AA26, AA30, AA32, AB10, AB11, AB12, AB14, AB15, AB17, AC1, AC26, AC29, AC33, AD9, AD11, AD13, AD14, AD20, AD21, AD22, AE9, AE12, AE14, AE18, AE19, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AE29, AE32, AG3, AG6, AG7, AG11, AG25, AG28, AG31, AG33, AH7, AH9, AH27, AH32, AJ13, AJ19, AJ21, AJ23, AK5, AK11, AK32, AL3, AL9, AL12, AL13, AL14, AM5, AM20, AM26, AM29, AN1, AN10, AN11, AN18, AN22, AN24, AN28, AN31, AN33	GND	G

5.2.16   Others

Ball#[1]	Pin Name[2]
AH11, AG17, F20, W9, W10, U8, U10	NC

5.3 GPIO Multiplex Function

The following tables provide a description of the T527 GPIO multiplex function.

📖 NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function7 to Function13 are reserved.

5.3.1 Port B

Table 5-28 Port B Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PB0	I/O	UART2-TX	SPI2-CS0	JTAG-MS	LCD0-D0	PWM0-6	PB-EINT0
PB1	I/O	UART2-RX	SPI2-CLK	JTAG-CK	LCD0-D1	PWM0-7	PB-EINT1
PB2	I/O	UART2-RTS	SPI2-MOSI	JTAG-DO	LCD0-D8	CAN-TX0	PB-EINT2
PB3	I/O	UART2-CTS	SPI2-MISO	JTAG-DI	LCD0-D9	CAN-RX0	PB-EINT3
PB4	I/O	TWI1-SCK	I2S0-MCLK[1]		PWM0-8	HDMI-SCL	PB-EINT4
PB5	I/O	TWI1-SDA	I2S0-BCLK[1]		PWM0-9	HDMI-SDA	PB-EINT5
PB6	I/O		I2S0-LRCK[1]		PWM0-10	HDMI-CEC	PB-EINT6
PB7	I/O	OWA-IN	I2S0-DOUT0[1]	I2S0-DIN1[1]	LCD0-D16	PWM0-11	PB-EINT7
PB8	I/O	OWA-OUT	I2S0-DIN0[1]	I2S0-DOUT1[1]	LCD0-D17	PWM0-0	PB-EINT8
PB9	I/O	UART0-TX	TWI0-SCK		I2S0-DIN2[1]	I2S0-DOUT2[1]	PB-EINT9
PB10	I/O	UART0-RX	TWI0-SDA	PWM0-1	I2S0-DIN3[1]	I2S0-DOUT3[1]	PB-EINT10
PB11	I/O	TWI5-SCK	UART7-RTS	SPI1-CS0	PWM0-2		PB-EINT11
PB12	I/O	TWI5-SDA	UART7-CTS	SPI1-CLK	PWM0-3		PB-EINT12
PB13	I/O	TWI4-SCK	UART7-TX	SPI1-MOSI	PWM0-4		PB-EINT13
PB14	I/O	TWI4-SDA	UART7-RX	SPI1-MISO	PWM0-5		PB-EINT14

(1) I2S0 signals and S-I2S0 signals cannot be connected simultaneously.

5.3.2 Port C

Table 5-29 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PC0	I/O	NAND-WE	SDC2-DS				PC-EINT0
PC1	I/O	NAND-ALE	SDC2-RST				PC-EINT1
PC2	I/O	NAND-CLE		SPI0-MOSI	SPIF-MOSI		PC-EINT2
PC3	I/O	NAND-CE1		SPI0-CS0	SPIF-CS0		PC-EINT3
PC4	I/O	NAND-CE0		SPI0-MISO	SPIF-MISO		PC-EINT4
PC5	I/O	NAND-RE	SDC2-CLK				PC-EINT5
PC6	I/O	NAND-RB0	SDC2-CMD				PC-EINT6
PC7	I/O	NAND-RB1		SPI0-CS1	SPIF-DQS		PC-EINT7
PC8	I/O	NAND-DQ7	SDC2-D3		SPIF-D7		PC-EINT8
PC9	I/O	NAND-DQ6	SDC2-D4		SPIF-D6		PC-EINT9
PC10	I/O	NAND-DQ5	SDC2-D0		SPIF-D5		PC-EINT10
PC11	I/O	NAND-DQ4	SDC2-D5		SPIF-D4		PC-EINT11
PC12	I/O	NAND-DQS		SPI0-CLK	SPIF-CLK		PC-EINT12
PC13	I/O	NAND-DQ3	SDC2-D1				PC-EINT13
PC14	I/O	NAND-DQ2	SDC2-D6				PC-EINT14
PC15	I/O	NAND-DQ1	SDC2-D2	SPI0-WP	SPIF-WP		PC-EINT15
PC16	I/O	NAND-DQ0	SDC2-D7	SPI0-HOLD	SPIF-HOLD		PC-EINT16

5.3.3 Port D

Table 5-30 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PD0	I/O	LCD0-D2	LVDS0-D0P	DSI0-D0P	PWM0-0		PD-EINT0
PD1	I/O	LCD0-D3	LVDS0-D0N	DSI0-D0N	PWM0-1		PD-EINT1
PD2	I/O	LCD0-D4	LVDS0-D1P	DSI0-D1P	PWM0-2		PD-EINT2
PD3	I/O	LCD0-D5	LVDS0-D1N	DSI0-D1N	PWM0-3		PD-EINT3
PD4	I/O	LCD0-D6	LVDS0-D2P	DSI0-CKP	PWM0-4		PD-EINT4
PD5	I/O	LCD0-D7	LVDS0-D2N	DSI0-CKN	PWM0-5		PD-EINT5
PD6	I/O	LCD0-D10	LVDS0-CKP	DSI0-D2P	PWM0-6		PD-EINT6
PD7	I/O	LCD0-D11	LVDS0-CKN	DSI0-D2N	PWM0-7		PD-EINT7
PD8	I/O	LCD0-D12	LVDS0-D3P	DSI0-D3P	PWM0-8		PD-EINT8
PD9	I/O	LCD0-D13	LVDS0-D3N	DSI0-D3N	PWM0-9		PD-EINT9
PD10	I/O	LCD0-D14	LVDS1-D0P	DSI1-D0P	PWM0-10	SPI1-CS0/DBI-CSX	PD-EINT10
PD11	I/O	LCD0-D15	LVDS1-D0N	DSI1-D0N	PWM0-11	SPI1-CLK/DBI-SCLK	PD-EINT11
PD12	I/O	LCD0-D18	LVDS1-D1P	DSI1-D1P	PWM0-12	SPI1-MOSI/DBI-SDO	PD-EINT12
PD13	I/O	LCD0-D19	LVDS1-D1N	DSI1-D1N	PWM0-13	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PD-EINT13
PD14	I/O	LCD0-D20	LVDS1-D2P	DSI1-CKP	PWM0-14	UART3-TX	PD-EINT14
PD15	I/O	LCD0-D21	LVDS1-D2N	DSI1-CKN	PWM0-15	UART3-RX	PD-EINT15
PD16	I/O	LCD0-D22	LVDS1-CKP	DSI1-D2P	PWM1-0	UART3-RTS	PD-EINT16
PD17	I/O	LCD0-D23	LVDS1-CKN	DSI1-D2N	PWM1-1	UART3-CTS	PD-EINT17
PD18	I/O	LCD0-CLK	LVDS1-D3P	DSI1-D3P	PWM1-2	UART4-TX	PD-EINT18
PD19	I/O	LCD0-DE	LVDS1-D3N	DSI1-D3N	PWM1-3	UART4-RX	PD-EINT19
PD20	I/O	LCD0-HSYNC	PWM0-2	UART2-TX	UART7-RTS	UART4-RTS	PD-EINT20
PD21	I/O	LCD0-VSYNC	PWM0-3	UART2-RX	UART7-CTS	UART4-CTS	PD-EINT21
PD22	I/O	PWM0-1	SPI1-HOLD/DBI-DCX/DBI-WRX	UART2-RTS	UART7-TX	TWI0-SCK	PD-EINT22
PD23	I/O	PWM0-0	SPI1-WP/DBI-TE	UART2-CTS	UART7-RX	TWI0-SDA	PD-EINT23

5.3.4 Port E

Table 5-31 Port E Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PE0	I/O	MCSI0-MCLK					PE-EINT0
PE1	I/O	TWI2-SCK	UART4-TX				PE-EINT1
PE2	I/O	TWI2-SDA	UART4-RX				PE-EINT2
PE3	I/O	TWI3-SCK	UART4-RTS				PE-EINT3
PE4	I/O	TWI3-SDA	UART4-CTS				PE-EINT4
PE5	I/O	MCSI1-MCLK		I2S2-MCLK(1)	LEDC		PE-EINT5
PE6	I/O			I2S2-BCLK[1]	LCD0-TRIG	NCSI-D8	PE-EINT6
PE7	I/O			I2S2-LRCK(1)	LCD1-TRIG	NCSI-D9	PE-EINT7
PE8	I/O			I2S2-DOUT0(1)	LCD2-TRIG	NCSI-D10	PE-EINT8
PE9	I/O			I2S2-DIN0(1)		NCSI-D11	PE-EINT9
PE10	I/O	MCSI3-MCLK	PWM0-3			NCSI-D12	PE-EINT10
PE11	I/O	TWI1-SCK	UART5-RTS	SPI2-CS0	UART6-TX	NCSI-D13	PE-EINT11
PE12	I/O	TWI1-SDA	UART5-CTS	SPI2-CLK	UART6-RX	NCSI-D14	PE-EINT12
PE13	I/O	TWI4-SCK	UART5-TX	SPI2-MOSI	UART6-RTS	CSI0-XVS-FSYNC	PE-EINT13
PE14	I/O	TWI4-SDA	UART5-RX	SPI2-MISO	UART6-CTS	CSI1-XVS-FSYNC	PE-EINT14
PE15	I/O	MCSI2-MCLK	PWM0-2			NCSI-D15	PE-EINT15

(1) If I2S2 needs to be used, please ensure that the peripheral device connected to I2S2 signals will not be used with HDMI/eDP interface simultaneously. If you have more questions, please contact Allwinner FAE.

5.3.5 Port F

Table 5-32 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PF0	I/O	SDC0-D1	JTAG-MS		I2S3-DIN0	I2S3-DOUT1	PF-EINT0
PF1	I/O	SDC0-D0	JTAG-DI		I2S3-DOUT0	I2S3-DIN1	PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX		I2S3-DIN2	I2S3-DOUT2	PF-EINT2
PF3	I/O	SDC0-CMD	JTAG-DO		I2S3-LRCK		PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX		I2S3-DIN3	I2S3-DOUT3	PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK		I2S3-BCLK		PF-EINT5
PF6	I/O				I2S3-MCLK		PF-EINT6

5.3.6 Port G

Table 5-33 Port G Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PG0	I/O	SDC1-CLK					PG-EINT0
PG1	I/O	SDC1-CMD					PG-EINT1
PG2	I/O	SDC1-D0	PCIE0-PERSTN				PG-EINT2
PG3	I/O	SDC1-D1	PCIE0-WAKEN				PG-EINT3
PG4	I/O	SDC1-D2	PCIE0-CLKREQN				PG-EINT4
PG5	I/O	SDC1-D3					PG-EINT5
PG6	I/O	UART1-TX					PG-EINT6
PG7	I/O	UART1-RX					PG-EINT7
PG8	I/O	UART1-RTS					PG-EINT8
PG9	I/O	UART1-CTS					PG-EINT9
PG10	I/O		I2S1-MCLK				PG-EINT10
PG11	I/O		I2S1-BCLK				PG-EINT11
PG12	I/O		I2S1-LRCK				PG-EINT12
PG13	I/O		I2S1-DOUT0	I2S1-DIN1			PG-EINT13
PG14	I/O		I2S1-DIN0	I2S1-DOUT1			PG-EINT14

5.3.7 Port H

Table 5-34 Port H Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PH0	I/O	TWI0-SCK			RGMII0-RXD1/RMII0-RXD1		PH-EINT0
PH1	I/O	TWI0-SDA			RGMII0-RXD0/RMII0-RXD0		PH-EINT1
PH2	I/O	TWI1-SCK		I2S2-DIN3[1]	RGMII0-RXCTL/RMII0-CRS-DV	I2S2-DOUT3[1]	PH-EINT2
PH3	I/O	TWI1-SDA	IR-TX	I2S2-DIN2[1]	RGMII0-CLKIN/RMII0-RXER	I2S2-DOUT2[1]	PH-EINT3
PH4	I/O	UART3-TX	SPI1-CS0		RGMII0-TXD1/RMII0-TXD1		PH-EINT4
PH5	I/O	UART3-RX	SPI1-CLK	LEDC	RGMII0-TXD0/RMII0-TXD0		PH-EINT5
PH6	I/O	UART3-RTS	SPI1-MOSI	OWA-IN	RGMII0-TXCK/RMII0-TXCK		PH-EINT6
PH7	I/O	UART3-CTS	SPI1-MISO	OWA-OUT	RGMII0-TXCTL/RMII0-TXEN		PH-EINT7
PH8	I/O	DMIC-CLK[2]	SPI2-CS0	I2S2-MCLK[1]	I2S2-DIN2[1]		PH-EINT8
PH9	I/O	DMIC-DATA0[2]	SPI2-CLK	I2S2-BCLK[1]	RGMII0-MDC		PH-EINT9
PH10	I/O	DMIC-DATA1[2]	SPI2-MOSI	I2S2-LRCK[1]	RGMII0-MDIO		PH-EINT10
PH11	I/O	DMIC-DATA2[2]	SPI2-MISO	I2S2-DOUT0[1]	I2S2-DIN1[1]	PCIE0-PERSTN	PH-EINT11
PH12	I/O	DMIC-DATA3[2]	TWI3-SCK	I2S2-DIN0[1]	I2S2-DOUT1[1]	PCIE0-WAKEN	PH-EINT12
PH13	I/O		TWI3-SDA	I2S3-MCLK	RGMII0-EPHY-25M		PH-EINT13

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PH14	I/O			I2S3-BCLK	RGMII0-RXD3/RMII0-NULL		PH-EINT14
PH15	I/O			I2S3-LRCK	RGMII0-RXD2/RMII0-NULL		PH-EINT15
PH16	I/O		I2S3-DOUT0	I2S3-DIN1	RGMII0-RXCK/RMII0-NULL	CLK-FANOUT0	PH-EINT16
PH17	I/O		I2S3-DOUT1	I2S3-DIN0	RGMII0-TXD3/RMII0-NULL		PH-EINT17
PH18	I/O	IR-TX	I2S3-DOUT2	I2S3-DIN2	RGMII0-TXD2/RMII0-NULL		PH-EINT18
PH19	I/O	IR-RX	I2S3-DOUT3	I2S3-DIN3	LEDC	PCIE0-CLKREQN	PH-EINT19

(1) If I2S2 needs to be used, please ensure that the peripheral device connected to I2S2 signals will not be used with HDMI/eDP interface simultaneously. If you have more questions, please contact Allwinner FAE.

(2) DMIC signals and S-DMIC signals cannot be connected simultaneously.

5.3.8　Port I

Table 5-35 Port I Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PI0	I/O	TWI4-SCK	UART4-TX	PWM0-1	I2S2-DIN3[1]	I2S2-DOUT3[1]	PI-EINT0
PI1	I/O	TWI4-SDA	UART4-RX	PWM0-2	I2S2-DIN2[1]	I2S2-DOUT2[1]	PI-EINT1
PI2	I/O	UART5-TX	SPI1-CS0	PWM0-3	I2S2-BCLK[1]		PI-EINT2
PI3	I/O	UART5-RX	SPI1-CLK	PWM0-4	I2S2-LRCK[1]		PI-EINT3
PI4	I/O	UART5-RTS	SPI1-MOSI	PWM0-5	I2S2-DOUT0[1]	I2S2-DIN1[1]	PI-EINT4
PI5	I/O	UART5-CTS	SPI1-MISO	PWM0-6	I2S2-DIN0[1]	I2S2-DOUT1[1]	PI-EINT5
PI6	I/O	UART6-TX	UART4-RTS	PWM0-7	SPI2-CS0		PI-EINT6
PI7	I/O	UART6-RX	UART4-CTS	PWM0-8	SPI2-CLK		PI-EINT7
PI8	I/O	TWI5-SCK	IR-RX	PWM0-9	SPI2-MOSI		PI-EINT8
PI9	I/O	TWI5-SDA	DMIC-DATA2[2]	PWM0-10			PI-EINT9
PI10	I/O	OWA-OUT	DMIC-DATA1[2]	PWM0-11	I2S2-MCLK[1]		PI-EINT10
PI11	I/O	UART3-TX	DMIC-DATA0[2]	PWM0-12			PI-EINT11
PI12	I/O	UART3-RX		PWM0-13	SPI2-MISO		PI-EINT12
PI13	I/O	UART6-CTS	DMIC-DATA3[2]	PWM0-14	I2S2-MCLK[1]		PI-EINT13
PI14	I/O	UART6-RTS	DMIC-CLK[2]	PWM0-15			PI-EINT14
PI15	I/O	UART3-RTS	TWI2-SCK	PWM1-0	CAN-TX0		PI-EINT15
PI16	I/O	UART3-CTS	TWI2-SDA	PWM1-1	CAN-RX0		PI-EINT16

(1) If I2S2 needs to be used, please ensure that the peripheral device connected to I2S2 signals will not be used with HDMI/eDP interface simultaneously. If you have more questions, please contact Allwinner FAE.

(2) DMIC signals and S-DMIC signals cannot be connected simultaneously.

5.3.9　Port J

Table 5-36 Port J Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PJ0	I/O	LCD1-D0	LVDS2-D0P		RGMII1-RXD1/RMII1-RXD1		PJ-EINT0
PJ1	I/O	LCD1-D1	LVDS2-D0N		RGMII1-RXD0/RMII1-RXD0		PJ-EINT1
PJ2	I/O	LCD1-D2	LVDS2-D1P		RGMII1-RXCTL/RMII1-CRS-DV		PJ-EINT2
PJ3	I/O	LCD1-D3	LVDS2-D1N		RGMII1-CLKIN/RMII1-RXER		PJ-EINT3
PJ4	I/O	LCD1-D4	LVDS2-D2P		RGMII1-TXD1/RMII1-TXD1		PJ-EINT4
PJ5	I/O	LCD1-D5	LVDS2-D2N		RGMII1-TXD0/RMII1-TXD0		PJ-EINT5
PJ6	I/O	LCD1-D6	LVDS2-CKP		RGMII1-TXCK/RMII1-TXCK		PJ-EINT6
PJ7	I/O	LCD1-D7	LVDS2-CKN		RGMII1-TXCTL/RMII1-TXEN		PJ-EINT7
PJ8	I/O	LCD1-D8	LVDS2-D3P		RGMII1-MDC		PJ-EINT8
PJ9	I/O	LCD1-D9	LVDS2-D3N		RGMII1-MDIO		PJ-EINT9
PJ10	I/O	LCD1-D10	LVDS3-D0P		RGMII1-EPHY-25M		PJ-EINT10
PJ11	I/O	LCD1-D11	LVDS3-D0N		RGMII1-RXD3/RMII1-NULL		PJ-EINT11
PJ12	I/O	LCD1-D12	LVDS3-D1P		RGMII1-RXD2/RMII1-NULL		PJ-EINT12

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PJ13	I/O	LCD1-D13	LVDS3-D1N		RGMII1-RXCK/RMII1-NULL		PJ-EINT13
PJ14	I/O	LCD1-D14	LVDS3-D2P		RGMII1-TXD3/RMII1-NULL		PJ-EINT14
PJ15	I/O	LCD1-D15	LVDS3-D2N		RGMII1-TXD2/RMII1-NULL		PJ-EINT15
PJ16	I/O	LCD1-D16	LVDS3-CKP				PJ-EINT16
PJ17	I/O	LCD1-D17	LVDS3-CKN				PJ-EINT17
PJ18	I/O	LCD1-D18	LVDS3-D3P				PJ-EINT18
PJ19	I/O	LCD1-D19	LVDS3-D3N				PJ-EINT19
PJ20	I/O	LCD1-D20	UART2-TX	UART3-RTS	SPI0-CS0		PJ-EINT20
PJ21	I/O	LCD1-D21	UART2-RX	UART3-CTS	SPI0-CLK		PJ-EINT21
PJ22	I/O	LCD1-D22	UART2-RTS	UART3-TX	SPI0-MOSI		PJ-EINT22
PJ23	I/O	LCD1-D23	UART2-CTS	UART3-RX	SPI0-MISO		PJ-EINT23
PJ24	I/O	LCD1-CLK	TWI4-SCK	UART4-TX	SPI0-CS1		PJ-EINT24
PJ25	I/O	LCD1-DE	TWI4-SDA	UART4-RX	SPI0-WP		PJ-EINT25
PJ26	I/O	LCD1-HSYNC	TWI5-SCK	UART4-RTS	SPI0-HOLD		PJ-EINT26
PJ27	I/O	LCD1-VSYNC	TWI5-SDA	UART4-CTS			PJ-EINT27

5.3.10　Port K

Table 5-37 Port K Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PK0	I/O	MCSIA-D0N					PK-EINT0
PK1	I/O	MCSIA-D0P					PK-EINT1
PK2	I/O	MCSIA-D1N					PK-EINT2
PK3	I/O	MCSIA-D1P					PK-EINT3
PK4	I/O	MCSIA-CKN	TWI2-SCK				PK-EINT4
PK5	I/O	MCSIA-CKP	TWI2-SDA				PK-EINT5
PK6	I/O	MCSIB-D0N					PK-EINT6
PK7	I/O	MCSIB-D0P					PK-EINT7
PK8	I/O	MCSIB-D1N					PK-EINT8
PK9	I/O	MCSIB-D1P					PK-EINT9
PK10	I/O	MCSIB-CKN	TWI3-SCK				PK-EINT10
PK11	I/O	MCSIB-CKP	TWI3-SDA				PK-EINT11
PK12	I/O	MCSIC-D0N	UART7-TX	TWI4-SCK	NCSI-PCLK		PK-EINT12
PK13	I/O	MCSIC-D0P	UART7-RX	TWI4-SDA	NCSI-MCLK		PK-EINT13
PK14	I/O	MCSIC-D1N	UART7-RTS	UART5-RTS	NCSI-HSYNC		PK-EINT14
PK15	I/O	MCSIC-D1P	UART7-CTS	UART5-CTS	NCSI-VSYNC		PK-EINT15
PK16	I/O	MCSIC-CKN	TWI5-SCK	UART5-TX	NCSI-D0		PK-EINT16
PK17	I/O	MCSIC-CKP	TWI5-SDA	UART5-RX	NCSI-D1		PK-EINT17
PK18	I/O	MCSID-D0N	MCSI0-MCLK	UART6-TX	NCSI-D2		PK-EINT18
PK19	I/O	MCSID-D0P	TWI2-SCK	UART6-RX	NCSI-D3		PK-EINT19
PK20	I/O	MCSID-D1N	TWI2-SDA	UART6-RTS	NCSI-D4		PK-EINT20
PK21	I/O	MCSID-D1P	MCSI1-MCLK	UART6-CTS	NCSI-D5		PK-EINT21
PK22	I/O	MCSID-CKN	TWI3-SCK	PWM0-6	NCSI-D6		PK-EINT22
PK23	I/O	MCSID-CKP	TWI3-SDA	PWM0-7	NCSI-D7		PK-EINT23

5.3.11　Port L

Table 5-38 Port L Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PL0	I/O	S-TWI0-SCK					PL-EINT0
PL1	I/O	S-TWI0-SDA					PL-EINT1

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PL2	I/O	S-UART0-TX	S-UART1-TX	MCU-PWM0-0			PL-EINT2
PL3	I/O	S-UART0-RX	S-UART1-RX	MCU-PWM0-1			PL-EINT3
PL4	I/O	S-JTAG-MS	S-CAN-TX0	MCU-PWM0-2	S-I2S0-BCLK[1]		PL-EINT4
PL5	I/O	S-JTAG-CK	S-CAN-RX0	MCU-PWM0-3	S-I2S0-LRCK[1]	S-DMIC-DATA3[2]	PL-EINT5
PL6	I/O	S-JTAG-DO	MCU-PWM0-4	S-I2S0-DIN1[1]	S-I2S0-DOUT0[1]	S-DMIC-DATA2[2]	PL-EINT6
PL7	I/O	S-JTAG-DI	MCU-PWM0-5	S-I2S0-DOUT1[1]	S-I2S0-DIN0[1]	S-DMIC-DATA1[2]	PL-EINT7
PL8	I/O	S-TWI1-SCK	S-DJTAG-MS	S-RJTAG-MS	S-I2S0-MCLK[1]	S-DMIC-DATA0[2]	PL-EINT8
PL9	I/O	S-TWI1-SDA	S-DJTAG-CK	S-RJTAG-CK	S-PWM0-1	S-DMIC-CLK[2]	PL-EINT9
PL10	I/O	S-PWM0-0	S-DJTAG-DO	S-RJTAG-DO	S-DMIC-DATA0[2]	S-SPI0-CS0	PL-EINT10
PL11	I/O	S-IR-RX	S-DJTAG-DI	S-RJTAG-DI	S-DMIC-DATA1[2]	S-SPI0-CLK	PL-EINT11
PL12	I/O	S-TWI2-SCK	MCU-PWM0-6	S-UART0-TX	S-DMIC-DATA2[2]	S-SPI0-MOSI	PL-EINT12
PL13	I/O	S-TWI2-SDA	MCU-PWM0-7	S-UART0-RX	S-DMIC-DATA3[2]	S-SPI0-MISO	PL-EINT13

(1) I2S0 signals and S-I2S0 signals cannot be connected simultaneously.

(2) DMIC signals and S-DMIC signals cannot be connected simultaneously.

5.3.12   Port M

Table 5-39 Port M Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function14
PM0	I/O	S-UART0-TX	S-UART1-TX	MCU-PWM0-0			PM-EINT0
PM1	I/O	S-UART0-RX	S-UART1-RX	MCU-PWM0-1			PM-EINT1
PM2	I/O	S-TWI1-SCK	S-RJTAG-MS	MCU-PWM0-4			PM-EINT2
PM3	I/O	S-TWI1-SDA	S-RJTAG-CK	MCU-PWM0-5			PM-EINT3
PM4	I/O	MCU-PWM0-6	S-RJTAG-DO	S-TWI2-SCK			PM-EINT4
PM5	I/O	S-IR-RX	S-RJTAG-DI	S-TWI2-SDA	MCU-PWM0-7		PM-EINT5

5.4 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name**: The name of every signal.

[2] **Description**: The detailed function description of every signal.

[3] **Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

5.4.1 Audio Codec

Table 5-40 Audio Codec Signal Description

Signal Name[1]	Description[2]	Type[3]
MICIN1P	Microphone Differential Positive Input 1	AI
MICIN1N	Microphone Differential Negative Input 1	AI
MICIN2P	Microphone Differential Positive Input 2	AI
MICIN2N	Microphone Differential Negative Input 2	AI
MICIN3P	Microphone Differential Positive Input 3	AI
MICIN3N	Microphone Differential Negative Input 3	AI
LINEOUTLP	Lineout Left Channel Positive Differential Output	AO
LINEOUTLN	Lineout Left Channel Negative Differential Output	AO
LINEOUTRP	Lineout Right Channel Positive Differential Output	AO
LINEOUTRN	Lineout Right Channel Negative Differential Output	AO
HPOUTL	Headphone Left Output	AO

Signal Name[1]	Description[2]	Type[3]
HPOUTR	Headphone Right Output	AO
HPOUTFB	Pseudo Differential Headphone Ground Reference	AI
MIC-DET	Headphone MIC detect	AI
HP-DET	Headphone Jack detect	AI
MBIAS	First bias voltage output for main microphone	AO
HBIAS	Second bias voltage output for headset microphone	AO
CPVDD	Analog power for headphone charge pump	P
CPVEE	Charge pump negative voltage output	P
CPVIN	Analog power for LDO	P
AVCC	Power Supply for Analog Part	P
ALDO-OUT	Internal LDO Output	P
VDD33	Power Supply for 3.3V Analog Part	P
VEE	Negative Voltage to Headphone	P
VRA1	Internal Reference Voltage	AO
VRA2	Internal Reference Voltage	AO
VRP	Internal Reference Voltage	AO
AGND	Analog Ground	G

5.4.2　CAN

Table 5-41 CAN Signal Description

Signal Name[1]	Description[2]	Type[3]
CAN-TX0	CAN Transmitter0	O
CAN-RX0	CAN Receiver0	I
S-CAN-TX0	CAN Transmitter0	O
S-CAN-RX0	CAN Receiver0	I

5.4.3　CIR_RX

Table 5-42 CIR_RX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-RX	Consumer Infrared Receiver	I
S-IR-RX	Consumer infrared Receiver	I

5.4.4 CIR_TX

Table 5-43 CIR_TX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-TX	Consumer Infrared Transmitter	O

5.4.5 DCXO

Table 5-44 DCXO Signal Description

Signal Name[1]	Description[2]	Type[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
WREQIN	Request signal of REFCLK_OUT	I
VCC-DCXO	Digital Compensated Crystal Oscillator Power Supply	P

5.4.6 DMIC

Table 5-45 DMIC Signal Description

Signal Name[1]	Description[2]	Type[3]
DMIC-DATA[3:0]	Digital Microphone Data Input	I
DMIC-CLK	Digital Microphone Clock Output	O
S-DMIC-DATA[3:0]	Digital Microphone Data Input	I
S-DMIC-CLK	Digital Microphone Clock Output	O

5.4.7 HDMI

Table 5-46 HDMI Signal Description

Signal Name[1]	Description[2]	Type[3]
HCEC	HDMI Consumer Electronics Control	I/O
HHPD	HDMI Hot Plug Detection Signal	I/O
HREXT	HDMI Reference Resistance	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO

Signal Name[1]	Description[2]	Type[3]
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
VCC18-HDMI	1.8V Analog Supply for IO	P
VDD09-HDMI	0.9V HDMI Digital Power Supply	P

5.4.8   eDP1.3

Table 5-47 eDP1.3 Signal Description

Signal Name[1]	Description[2]	Type[3]
EDP-AUXP	AUX channel Positive Input/Output	A I/O
EDP-AUXN	AUX channel Negative Input/Output	A I/O
EDP-HPD	Hot Plug Detection Signal	AI
EDP-REXT	eDP External Reference Resistor	AO
EDP-TX0P	eDP Positive Output of Data Channel0	AO
EDP-TX0N	eDP Negative Output of Data Channel0	AO
EDP-TX1P	eDP Positive Output of Data Channel1	AO
EDP-TX1N	eDP Negative Output of Data Channel1	AO
EDP-TX2P	eDP Positive Output of Data Channel2	AO
EDP-TX2N	eDP Negative Output of Data Channel2	AO
EDP-TX3P	eDP Positive Output of Data Channel3	AO
EDP-TX3N	eDP Negative Output of Data Channel3	AO
VCC18-EDP	1.8V Analog Supply	P
VDD09-EDP	0.9V Digital Supply	P

5.4.9   GMAC

Table 5-48 GMAC Signal Description

Signal Name[1]	Description[2]	Type[3]
RGMII0-RXD0/RMII0-RXD0	RGMII0/RMII0 Receive Data0	I
RGMII0-RXD1/RMII0-RXD1	RGMII0/RMII0 Receive Data1	I

Signal Name[1]	Description[2]	Type[3]
RGMII0-RXD2/RMII0-NULL	RGMII0 Receive Data2	I
RGMII0-RXD3/RMII0-NULL	RGMII0 Receive Data3	I
RGMII0-RXCK/ RMII0-NULL	RGMII0 Receive Clock	I
RGMII0-RXCTL/RMII0-CRS-DV	RGMII0 Receive Control/RMII0 Carrier Sense Receive Data Valid	I
RGMII0-CLKIN/RMII0-RXER	RGMII0 Transmit Clock from External/RMII0 Receive Error	I
RGMII0-TXD0/RMII0-TXD0	RGMII0/RMII0 Transmit Data0	O
RGMII0-TXD1/RMII0-TXD1	RGMII0/RMII0 Transmit Data1	O
RGMII0-TXD2/RMII0-NULL	RGMII0 Transmit Data2	O
RGMII0-TXD3/RMII0-NULL	RGMII0 Transmit Data3	O
RGMII0-TXCK/RMII0-TXCK	RGMII0/RMII0 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII0-TXCTL/RMII0-TXEN	RGMII0 Transmit Control/RMII0 Transmit Enable	O
RGMII0-MDC	RGMII0 Management Data Clock	O
RGMII0-MDIO	RGMII0 Management Data Input/ Output	I/O
RGMII0-EPHY-25M	25 MHz Output for GMAC PHY	O

5.4.10　GMAC200

Table 5-49 GMAC200 Signal Description

Signal Name[1]	Description[2]	Type[3]
RGMII1-RXD0/RMII1-RXD0	RGMII1/RMII1 Receive Data0	I
RGMII1-RXD1/RMII1-RXD1	RGMII1/RMII1 Receive Data1	I
RGMII1-RXD2/RMII1-NULL	RGMII1 Receive Data2	I
RGMII1-RXD3/RMII1-NULL	RGMII1 Receive Data3	I
RGMII1-RXCK/ RMII1-NULL	RGMII1 Receive Clock	I
RGMII1-RXCTL/RMII1-CRS-DV	RGMII1 Receive Control/RMII1 Carrier Sense Receive Data Valid	I
RGMII1-CLKIN/RMII1-RXER	RGMII1 Transmit Clock from External/RMII1 Receive Error	I
RGMII1-TXD0/RMII1-TXD0	RGMII1/RMII1 Transmit Data0	O
RGMII1-TXD1/ RMII1-TXD1	RGMII1 Transmit Data1	O

Signal Name[1]	Description[2]	Type[3]
RGMII1-TXD2/RMII1-NULL	RGMII1 Transmit Data2	O
RGMII1-TXD3/RMII1-NULL	RGMII1 Transmit Data3	O
RGMII1-TXCK/RMII1-TXCK	RGMII1/RMII1 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII1-TXCTL/RMII1-TXEN	RGMII1 Transmit Control/RMII1 Transmit Enable	O
RGMII1-MDC	RGMII1 Management Data Clock	O
RGMII1-MDIO	RGMII1 Management Data Input/ Output	I/O
RGMII1-EPHY-25M	25 MHz Output for GMAC PHY	O

5.4.11   GPADC

Table 5-50 GPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
GPADC0	General Purpose ADC Input Channel 0/ BROM Boot Select	AI
GPADC1	General Purpose ADC Input Channel 1	AI
GPADC2	General Purpose ADC Input Channel 2	AI
GPADC3	General Purpose ADC Input Channel 3	AI
GPADC4	General Purpose ADC Input Channel 4	AI
GPADC5	General Purpose ADC Input Channel 5	AI
GPADC6	General Purpose ADC Input Channel 6	AI
GPADC7	General Purpose ADC Input Channel 7	AI
GPADC8	General Purpose ADC Input Channel 8	AI
GPADC9	General Purpose ADC Input Channel 9	AI
GPADC10	General Purpose ADC Input Channel 10	AI
GPADC11	General Purpose ADC Input Channel 11	AI
GPADC12	General Purpose ADC Input Channel 12	AI
GPADC13	General Purpose ADC Input Channel 13	AI
GPADC14	General Purpose ADC Input Channel 14	AI
GPADC15	General Purpose ADC Input Channel 15	AI
GPADC16	General Purpose ADC Input Channel 16	AI
GPADC17	General Purpose ADC Input Channel 17	AI
GPADC18	General Purpose ADC Input Channel 18	AI

Signal Name[1]	Description[2]	Type[3]
GPADC19	General Purpose ADC Input Channel 19	AI
GPADC20	General Purpose ADC Input Channel 20	AI
GPADC21	General Purpose ADC Input Channel 21	AI
GPADC22	General Purpose ADC Input Channel 22	AI
GPADC23	General Purpose ADC Input Channel 23	AI
VCM-ADC	External Capacitor Connection	A I/O
VCC-ADC	Power Supply for GPADC and LRADC	P
VREFP-ADC	GPADC Reference Voltage (Positive)	P
VREFN-ADC	GPADC Reference Voltage (Negative)	P
GND-ADC	Analog Ground	G

5.4.12 LRADC

Table 5-51 LRADC Signal Description

Signal Name[1]	Description[2]	Type[3]
LRADC0	Low Rate ADC	AI
LRADC1	Low Rate ADC	AI

5.4.13 I2S/PCM

Table 5-52 I2S/PCM Signal Description

Signal Name[1]	Description[2]	Type[3]
I2S0-DOUT[3:0]	I2S0/PCM0 Serial Data Output Channel [3:0]	O
I2S0-DIN[3:0]	I2S0/PCM0 Serial Data Input Channel [3:0]	I
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S1-DOUT[1:0]	I2S1/PCM1 Serial Data Output Channel [1:0]	O
I2S1-DIN[1:0]	I2S1/PCM1 Serial Data Input Channel [1:0]	I
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM01Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S2-DOUT[3:0]	I2S2/PCM2 Serial Data Output Channel [3:0]	O
I2S2-DIN[3:0]	I2S2/PCM2 Serial Data Input Channel [3:0]	I

Signal Name[1]	Description[2]	Type[3]
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S3-DOUT[3:0]	I2S3/PCM3 Serial Data Output Channel [3:0]	O
I2S3-DIN[3:0]	I2S3/PCM3 Serial Data Input Channel [3:0]	I
I2S3-MCLK	I2S3 Master Clock	O
I2S3-LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3-BCLK	I2S3/PCM3 Bit Rate Clock	I/O
S-I2S0-DIN[1:0]	S-I2S0/PCM0 Serial Data Input Channel [1:0]	I
S-I2S0-DOUT[1:0]	S-I2S0/PCM0 Serial Data Output Channel [1:0]	O
S-I2S0-MCLK	S-I2S0 Master Clock	O
S-I2S0-LRCK	S-I2S0/PCM0 Sample Rate Clock/Sync	I/O
S-I2S0-BCLK	S-I2S0/PCM0 Bit Rate Clock	I/O

5.4.14   Interrupt

Table 5-53 Interrupt Signal Description

Signal Name[1]	Description[2]	Type[3]
PB-EINT [14:0]	Port B Interrupt	I
PC-EINT [16:0]	Port C Interrupt	I
PD-EINT [23:0]	Port D Interrupt	I
PE-EINT [15:0]	Port E Interrupt	I
PF-EINT [6:0]	Port F Interrupt	I
PG-EINT [14:0]	Port G Interrupt	I
PH-EINT [19:0]	Port H Interrupt	I
PI-EINT [16:0]	Port I Interrupt	I
PJ-EINT [27:0]	Port J Interrupt	I
PK-EINT [23:0]	Port K Interrupt	I
PL-EINT [13:0]	Port L Interrupt	I
PM-EINT [5:0]	Port M Interrupt	I

5.4.15 JTAG

Table 5-54 JTAG Signal Description

Signal Name[1]	Description[2]	Type[3]
JTAG-MS	ARM CPU JTAG Mode Selection	I
JTAG-CK	ARM CPU JTAG Clock Signal	I
JTAG-DO	ARM CPU JTAG Data Output	O
JTAG-DI	ARM CPU JTAG Data Input	I
S-JTAG-MS	CPUS JTAG Mode Selection	I
S-JTAG-CK	CPUS JTAG Clock Signal	I
S-JTAG-DO	CPUS JTAG Data Output	O
S-JTAG-DI	CPUS JTAG Data Input	I
S-DJTAG-MS	DSP JTAG Mode Select	I
S-DJTAG-CK	DSP JTAG Clock Signal	I
S-DJTAG-DO	DSP JTAG Data Output	O
S-DJTAG-DI	DSP JTAG Data Input	I
S-RJTAG-MS	RISC-V JTAG Mode Select	I
S-RJTAG-CK	RISC-V JTAG Clock Signal	I
S-RJTAG-DO	RISC-V JTAG Data Output	O
S-RJTAG-DI	RISC-V JTAG Data Input	I

5.4.16 LEDC

Table 5-55 LEDC Signal Description

Signal Name[1]	Description[2]	Type[3]
LEDC	Intelligent Control LED Signal Output	O

5.4.17 MIPI CSI

Table 5-56 MIPI CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
MCSIA-D0P	MIPI CSI Controller A Data0 Positive Signal	AI
MCSIA-D0N	MIPI CSI Controller A Data0 Negative Signal	AI
MCSIA-D1P	MIPI CSI Controller A Data1 Positive Signal	AI
MCSIA-D1N	MIPI CSI Controller A Data1 Negative Signal	AI
MCSIA-CKP	MIPI CSI Controller A Clock Positive Signal	AI

Signal Name[1]	Description[2]	Type[3]
MCSIA-CKN	MIPI CSI Controller A Clock Negative Signal	AI
MCSI0-MCLK	Master Clock for MIPI Sensor	O
MCSIB-D0P	MIPI CSI Controller B Data0 Positive Signal	AI
MCSIB-D0N	MIPI CSI Controller B Data0 Negative Signal	AI
MCSIB-D1P	MIPI CSI Controller B Data1 Positive Signal	AI
MCSIB-D1N	MIPI CSI Controller B Data1 Negative Signal	AI
MCSIB-CKP	MIPI CSI Controller B Clock Positive Signal	AI
MCSIB-CKN	MIPI CSI Controller B Clock Negative Signal	AI
MCSI1-MCLK	Master Clock for MIPI Sensor	O
MCSIC-D0P	MIPI CSI Controller C Data0 Positive Signal	AI
MCSIC-D0N	MIPI CSI Controller C Data0 Negative Signal	AI
MCSIC-D1P	MIPI CSI Controller C Data1 Positive Signal	AI
MCSIC-D1N	MIPI CSI Controller C Data1 Negative Signal	AI
MCSIC-CKP	MIPI CSI Controller C Clock Positive Signal	AI
MCSIC-CKN	MIPI CSI Controller C Clock Negative Signal	AI
MCSI2-MCLK	Master Clock for MIPI Sensor	O
MCSID-D0P	MIPI CSI Controller D Data0 Positive Signal	AI
MCSID-D0N	MIPI CSI Controller D Data0 Negative Signal	AI
MCSID-D1P	MIPI CSI Controller D Data1 Positive Signal	AI
MCSID-D1N	MIPI CSI Controller D Data1 Negative Signal	AI
MCSID-CKP	MIPI CSI Controller D Clock Positive Signal	AI
MCSID-CKN	MIPI CSI Controller D Clock Negative Signal	AI
MCSI3-MCLK	Master Clock for MIPI Sensor	O
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O
VCC-MCSI	Power Supply for MIPI CSI	P

5.4.18　MIPI DSI

Table 5-57 MIPI DSI Signal Description

Signal Name[1]	Description[2]	Type[3]
DSI0-D0P	DSI0 Differential Data0 Positive Signal	I/O
DSI0-D0N	DSI0 Differential Data0 Negative Signal	I/O
DSI0-D1P	DSI0 Differential Data1 Positive Signal	O

Signal Name[1]	Description[2]	Type[3]
DSI0-D1N	DSI0 Differential Data1 Negative Signal	O
DSI0-D2P	DSI0 Differential Data2 Positive Signal	O
DSI0-D2N	DSI0 Differential Data2 Negative Signal	O
DSI0-D3P	DSI0 Differential Data3 Positive Signal	O
DSI0-D3N	DSI0 Differential Data3 Negative Signal	O
DSI0-CKP	DSI0 Differential Clock Positive Signal	O
DSI0-CKN	DSI0 Differential Clock Negative Signal	O
DSI1-D0P	DSI1 Differential Data0 Positive Signal	I/O
DSI1-D0N	DSI1 Differential Data0 Negative Signal	I/O
DSI1-D1P	DSI1 Differential Data1 Positive Signal	O
DSI1-D1N	DSI1 Differential Data1 Negative Signal	O
DSI1-D2P	DSI1 Differential Data2 Positive Signal	O
DSI1-D2N	DSI1 Differential Data2 Negative Signal	O
DSI1-D3P	DSI1 Differential Data3 Positive Signal	O
DSI1-D3N	DSI1 Differential Data3 Negative Signal	O
DSI1-CKP	DSI1 Differential Clock Positive Signal	O
DSI1-CKN	DSI1 Differential Clock Negative Signal	O

5.4.19   OWA

Table 5-58 OWA Signal Description

Signal Name[1]	Description[2]	Type[3]
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O

5.4.20   Parallel CSI

Table 5-59 Parallel CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
NCSI-PCLK	Parallel CSI Pixel Clock	I
NCSI-MCLK	Parallel CSI Master Clock	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous	I
NCSI-D[15:0]	Parallel CSI Data Bit	I

Signal Name[1]	Description[2]	Type[3]
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC	I/O

5.4.21   PCIe2.1&USB3.1 DRD

Table 5-60 PCIe2.1&USB3.1 DRD Signal Description

Signal Name[1]	Description[2]	Type[3]
USB2-DP	USB2.0 Data Signal DP	A I/O
USB2-DM	USB2.0 Data Signal DM	A I/O
USB2-REXT	USB2.0 External Reference Resistor	AO
PCIE-REF-CLKP	PCIe2.1 Differential Signal REFCLK (Positive)	A I/O
PCIE-REF-CLKN	PCIe2.1 Differential Signal REFCLK (Negative)	A I/O
PCIE-REXT	PCIe2.1 External Reference Resistor	AO
PCIE-RX0-DP/USB3-RXP	PCIe2.1 Differential Signal of RX (Positive)/USB3.1 SuperSpeed Differential Signal of RX (Positive)	AI
PCIE-RX0-DN/USB3-RXN	PCIe2.1 Differential Signal of RX (Negative)/USB3.1 SuperSpeed Differential Signal of RX (Negative)	AI
PCIE-TX0-DP/USB3-TXP	PCIe2.1 Differential Signal of TX (Positive)/USB3.1 SuperSpeed Differential Signal of TX (Positive)	AO
PCIE-TX0-DN/USB3-TXN	PCIe2.1 Differential Signal of TX (Negative)/USB3.1 SuperSpeed Differential Signal of TX (Negative)	AO
PCIE0-PERSTN	PCIe0 Fundamental Reset	O
PCIE0-WAKEN	PCIe0 Wake Up	I
PCIE0-CLKREQN	PCIe0 Clock Request from PCIe Peripheral	I
VCC33-USB-2	3.3 V Power Supply for USB2.0 PHY	P
VCC33-18-USB-2	3.3 V Power Supply for USB2.0 PHY	P
VCC18-PCIE	1.8 V Power Supply for PCIe2.1	P
VDD09-PCIE	0.9 V Power Supply for PCIe2.1	P

5.4.22   PWM

Table 5-61 PWM Signal Description

Signal Name[1]	Description[2]	Type[3]
PWM0-[15:0]	Pulse Width Modulation Output Channel [15:0]	I/O

Signal Name[1]	Description[2]	Type[3]
PWM1-[3:0]	Pulse Width Modulation Output Channel [3:0]	I/O
S-PWM0-[1:0]	Pulse Width Modulation Output Channel [1:0]	I/O
MCU-PWM0-[7:0]	Pulse Width Modulation Output Channel [7:0]	I/O

5.4.23 RAW NAND Flash

Table 5-62 RAW NAND Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
NAND-WE	NAND Flash Write Enable	O
NAND-ALE	NAND Flash Address Latch Enable	O
NAND-CLE	NAND Flash Command latch Enable	O
NAND-CE[1:0]	NAND Flash Chip Select	O
NAND-RE	NAND Flash Read Enable	O
NAND-RB[1:0]	NAND Flash Ready/Busy Status Indicator Signal	I
NAND-DQ[7:0]	NAND Flash Data Bit	I/O
NAND-DQS	NAND Flash Data Strobe	I/O

5.4.24 RTC&PLL

Table 5-63 RTC&PLL Signal Description

Signal Name[1]	Description[2]	Type[3]
X32KFOUT	32.768 kHz clock Fanout Provides low frequency clock for external devices	AO,OD
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
PLLTEST	PLL Test Signal	AO, OD
VCC-RTC	RTC Power	P
VCC-PLL	Power Supply for System PLL	P

5.4.25 SDRAM

Table 5-64 SDRAM Signal Description

Signal Name[1]	Description[2]	Type[3]
SA[17:0]	DRAM Address Signal to the Memory Device	O
SACT	DRAM Activation Command Output	O

Signal Name[1]	Description[2]	Type[3]
SBA[1:0]	DRAM Bank Address Signal to the Memory Device	O
SBG[1:0]	DRAM Bank Group Address Signal to the Memory Device	O
SCKE0	DRAM Clock Enable Signal to the Memory Device	O
SCKP	DRAM Active-High Clock Signal to the Memory Device	O
SCKN	DRAM Active-Low Clock Signal to the Memory Device	O
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	I/O
SDQS[3:0]P	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O
SDQS[3:0]N	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SODT[1:0]	DRAM On-Die Termination Output Signal	O
SRST	DRAM Reset Signal to the Memory Device	O
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
VCC-DRAM	Power Supply for DRAM IO	P
VCC-DRAML	Power Supply for DRAM IO	P
VDD18-DRAM	DRAM 1.8V Internal PAD Power	P

5.4.26   SPI&SPI_DBI

Table 5-65 SPI&SPI_DBI Signal Description in CPUX Domain

Signal Name[1]	Description[2]	Type[3]
SPI0-CS[1:0]	SPI0 Chip Select Signal, Low Active	I/O
SPI0-CLK	SPI0 Clock Signal Provides serial interface timing.	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O

Signal Name[1]	Description[2]	Type[3]
SPI0-WP	SPI0 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI0-HOLD	SPI0 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-CS0	SPI1 Chip Select Signal, Low Active	I/O
SPI1-CLK	SPI1 Clock Signal Provides serial interface timing.	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protect, Low Active Protects the memory area against all program or erase instructions. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI1-HOLD	SPI1 Hold Signal Pauses any serial communication with the device without deselecting or resetting it. It also can be used for serial data input and output for SPI Quad Input or Quad Output mode.	I/O
SPI2-CS0	SPI2 Chip Select Signal, Low Active	I/O
SPI2-CLK	SPI2 Clock Signal Provides serial interface timing.	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
DBI-CSX	Chip Select Signal, Low Active	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O

Signal Name[1]	Description[2]	Type[3]
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
S-SPI0-CS0	S-SPI Chip Select Signal, Low Active	I/O
S-SPI0-CLK	S-SPI Clock Signal Provides serial interface timing.	I/O
S-SPI0-MOSI	S-SPI Master Data Out, Slave Data In	I/O
S-SPI0-MISO	S-SPI Master Data In, Slave Data Out	I/O

5.4.27 SPIFC

Table 5-66 SPIFC Signal Description

Signal Name	Description	Type
SPIF-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF-CLK	SPI Master Mode Clock Output	O
SPIF-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF-DQS	Data Strobe Signal	I
SPIF-D[7:4]	SPI Master Mode Data in Octal Mode.	I/O
SPIF-WP	SPI Write Protect, Low Active	I/O
SPIF-HOLD	SPI Hold Signal	I/O

5.4.28 SMHC

Table 5-67 SMHC Signal Description

Signal Name[1]	Description[2]	Type[3]
SDC0-CMD	Command Signal for SD Card	I/O, OD

Signal Name[1]	Description[2]	Type[3]
SDC0-CLK	Clock for SD Card	O
SDC0-D[3:0]	Data Input and Output for SD Card	I/O
SDC1-CMD	Command Signal for SDIO WIFI	I/O, OD
SDC1-CLK	Clock for SDIO WIFI	O
SDC1-D[3:0]	Data Input and Output for SDIO WIFI	I/O
SDC2-CMD	Command Signal for eMMC	I/O, OD
SDC2-CLK	Clock for eMMC	O
SDC2-D[8:0]	Data Input and Output for eMMC	I/O
SDC2-RST	Reset for eMMC	O
SDC2-DS	Data Strobe for eMMC	I

5.4.29 System

Table 5-68 System Signal Description

Signal Name[1]	Description[2]	Type[3]
FEL	Boot Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process. For more details, see section 2.4 BROM System in the *T527_User_Manual*.	I
JTAG-SEL	JTAG mode select The signal is used to select the port from which JTAG function outputs.	I
NMI	Non-Maskable Interrupt	I/O, OD
RESET	Reset Signal (Low Active)	I/O, OD

5.4.30 TCONLCD

Table 5-69 TCONLCD Signal Description

Signal Name[1]	Description[2]	Type[3]
LCD0-D[23:0]	LCD Data Input/Output	I/O
LCD0-CLK	LCD Clock The pixel data are synchronized by this clock	O

Signal Name[1]	Description[2]	Type[3]
LCD1-CLK	LCD Clock The pixel data are synchronized by this clock	O
LCD0-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD1-VSYNC	LCD Vertical Sync It indicates one new frame	O
LCD0-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD1-HSYNC	LCD Horizontal Sync It indicates one new scan line	O
LCD0-DE	LCD Data Output Enable	O
LCD1-DE	LCD Data Output Enable	O
LCD1-D[23:0]	LCD Data Input/Output	I/O
LCD0-TRIG	LCD Sync It is input from peripherals for sync	I
LCD1-TRIG	LCD Sync It is input from peripherals for sync	I
LCD2-TRIG	LCD Sync It is input from peripherals for sync	I
LVDS0-D[3:0]P	LVDS0 Positive Port of Data Channel [3:0]	AO
LVDS0-D[3:0]N	LVDS0 Negative Port of Data Channel [3:0]	AO
LVDS0-CKP	LVDS0 Positive Port of Clock	AO
LVDS0-CKN	LVDS0 Negative Port of Clock	AO
LVDS1-D[3:0]P	LVDS1 Positive Port of Data Channel [3:0]	AO
LVDS1-D[3:0]N	LVDS1 Negative Port of Data Channel [3:0]	AO
LVDS1-CKP	LVDS1 Positive Port of Clock	AO
LVDS1-CKN	LVDS1 Negative Port of Clock	AO
LVDS2-D[3:0]P	LVDS2 Positive Port of Data Channel [3:0]	AO
LVDS2-D[3:0]N	LVDS2 Negative Port of Data Channel [3:0]	AO
LVDS2-CKP	LVDS2 Positive Port of Clock	AO
LVDS2-CKN	LVDS2 Negative Port of Clock	AO
LVDS3-D[3:0]P	LVDS3 Positive Port of Data Channel [3:0]	AO
LVDS3-D[3:0]N	LVDS3 Negative Port of Data Channel [3:0]	AO

Signal Name[1]	Description[2]	Type[3]
LVDS3-CKP	LVDS3 Positive Port of Clock	AO
LVDS3-CKN	LVDS3 Negative Port of Clock	AO

5.4.31 TWI

Table 5-70 TWI Signal Description

Signal Name[1]	Description[2]	Type[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O
TWI4-SCK	TWI4 Serial Clock Signal	I/O
TWI4-SDA	TWI4 Serial Data Signal	I/O
TWI5-SCK	TWI5 Serial Clock Signal	I/O
TWI5-SDA	TWI5 Serial Data Signal	I/O
S-TWI0-SCK	S-TWI0 Serial Clock Signal	I/O
S-TWI0-SDA	S-TWI0 Serial Data Signal	I/O
S-TWI1-SCK	S-TWI1 Serial Clock Signal	I/O
S-TWI1-SDA	S-TWI1 Serial Data Signal	I/O
S-TWI2-SCK	S-TWI2 Serial Clock Signal	I/O
S-TWI2-SDA	S-TWI2 Serial Data Signal	I/O

5.4.32 USB2.0 DRD

Table 5-71 USB2.0 DRD Signal Description

Signal Name[1]	Description[2]	Type[3]
USB0-DP	USB2.0 Data Signal DP	A I/O
USB0-DM	USB2.0 Data Signal DM	A I/O
USB0-REXT	USB2.0 External Reference Resistor	AO

5.4.33   USB2.0 Host

Table 5-72 USB2.0 Host Signal Description

Signal Name[1]	Description[2]	Type[3]
USB1-DP	USB2.0 Data Signal DP	A I/O
USB1-DM	USB2.0 Data Signal DM	A I/O
USB1-REXT	USB2.0 External Reference Resistor	AO
VCC33-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host	P
VCC33-18-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host	P
VDD09-USB	0.9 V USB Digital Power Supply	P

5.4.34   UART

Table 5-73 UART Signal Description

Signal Name[1]	Description[2]	Type[3]
UART0-TX	UART0 Data Transmitter	O
UART0-RX	UART0 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART1-CTS	UART1 Data Clear to Send	I
UART1-RTS	UART1 Data Request to Send	O
UART2-TX	UART2 Data Transmitter	O
UART2-RX	UART2 Data Receiver	I
UART2-CTS	UART2 Data Clear to Send	I
UART2-RTS	UART2 Data Request to Send	O
UART3-TX	UART3 Data Transmitter	O
UART3-RX	UART3 Data Receiver	I
UART3-CTS	UART3 Data Clear to Send	I
UART3-RTS	UART3 Data Request to Send	O
UART4-TX	UART4 Data Transmitter	O
UART4-RX	UART4 Data Receiver	I
UART4-CTS	UART4 Data Clear to Send	I
UART4-RTS	UART4 Data Request to Send	O
UART5-TX	UART5 Data Transmitter	O
UART5-RX	UART5 Data Receiver	I

Signal Name[1]	Description[2]	Type[3]
UART5-CTS	UART5 Data Clear to Send	I
UART5-RTS	UART5 Data Request to Send	O
UART6-TX	UART6 Data Transmitter	O
UART6-RX	UART6 Data Receiver	I
UART6-CTS	UART6 Data Clear to Send	I
UART6-RTS	UART6 Data Request to Send	O
UART7-TX	UART7 Data Transmitter	O
UART7-RX	UART7 Data Receiver	I
UART7-CTS	UART7 Data Clear to Send	I
UART7-RTS	UART7 Data Request to Send	O
S-UART0-TX	S-UART0 Data Transmitter	O
S-UART0-RX	S-UART0 Data Receiver	I
S-UART1-TX	S-UART1 Data Transmitter	O
S-UART1-RX	S-UART1 Data Receiver	I
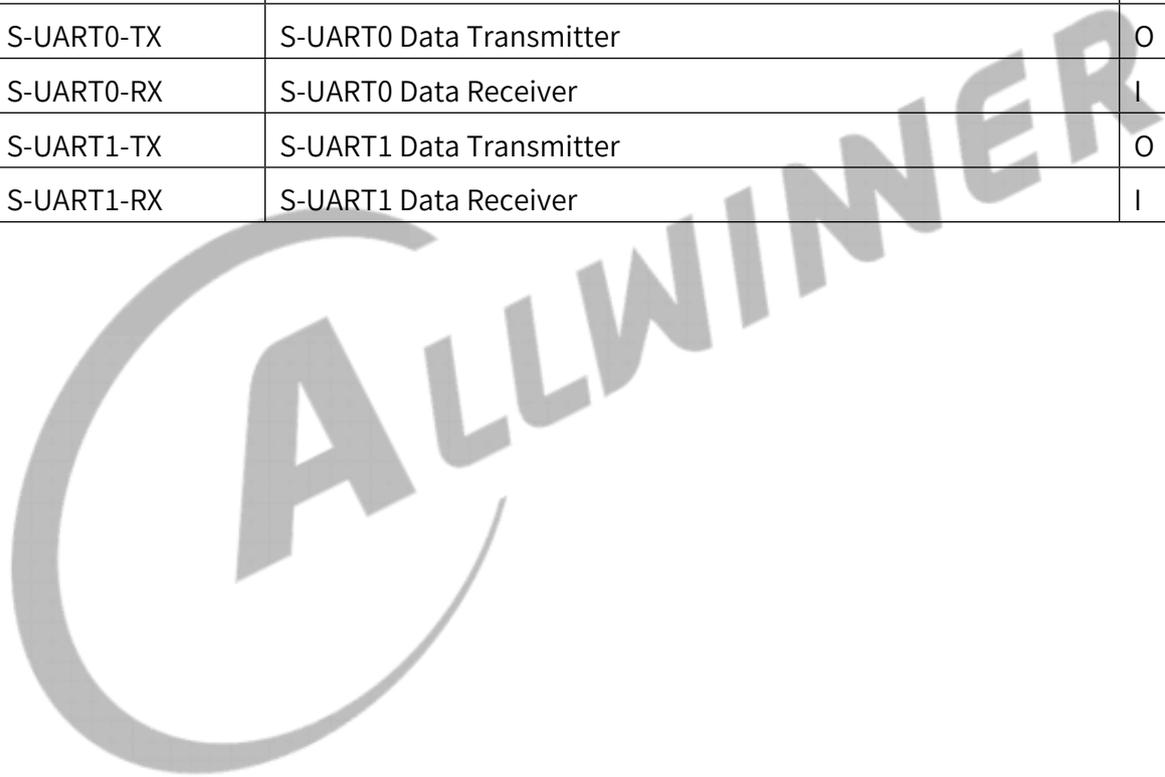
6 Electrical Characteristics

6.1 Parameter Conditions

6.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

6.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

6.1.3 Temperature Definitions

- Ambient Temperature(c) the temperature of the surrounding environment.

- Junction Temperature(c) the hottest temperature of the silicon chip inside the package.

- Absolute Maximum Junction Temperature(c) the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.

- Recommended Operating Temperature(c) the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

6.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.

⚠ **CAUTION**

Stresses beyond those listed under Table 6-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 6.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
CPVIN	Analog power for LDO	-0.3	2.16	V
VCC-ADC	Power Supply for GPADC and LRADC	-0.3	2.16	V
VCC-DCXO	Digital Compensated Crystal Oscillator Power Supply	-0.3	2.16	V
VCC-DRAM	Power Supply for DRAM IO	-0.3	1.8	V
VCC-DRAML	Power Supply for DRAM IO	-0.3	1.8	V
VCC-EFUSE	Power Supply for eFuse	-0.3	2.16	V
VCC-IO	Power Supply for 3.3 V Digital Part	-0.3	3.96	V
VCC-LVDS0	Analog Power Supply for LVDS0/1 and DSI0/1	-0.3	2.16	V
VCC-LVDS1	Analog Power Supply for LVDS2/3	-0.3	2.16	V
VCC-MCSI	Power supply for MIPI CSI	-0.3	2.16	V
VCC-PC	Digital Port C Power	-0.3	3.96	V
VCC-PD	Digital Port D Power	-0.3	3.96	V
VCC-PE	Digital Port E Power	-0.3	3.96	V
VCC-PG	Digital Port G Power	-0.3	3.96	V
VCC-PI	Digital Port I Power	-0.3	3.96	V
VCC-PJ	Digital Port J Power	-0.3	3.96	V
VCC-PK	Digital Port K Power	-0.3	3.96	V
VCC-PL	Digital Port L Power	-0.3	3.96	V
VCC-PM	Digital Port M Power	-0.3	3.96	V

Symbol	Parameter		Min[1]	Max[1]	Unit
VCC-PLL	Power Supply for System PLL		-0.3	2.16	V
VCC-RTC	RTC Power		-0.3	2.16	V
VCC18-PCIE	1.8 V Power Supply for PCIe2.1		-0.3	2.16	V
VCC18-EDP	1.8V Analog Supply		-0.3	2.16	V
VCC18-HDMI	1.8 V Power Supply for HDMI		-0.3	2.16	V
VCC33-18-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host		-0.3	3.96	V
VCC33-18-USB-2	3.3 V Power Supply for USB2.0 PHY		-0.3	3.96	V
VCC33-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host		-0.3	3.96	V
VCC33-USB-2	3.3 V Power Supply for USB2.0 PHY		-0.3	3.96	V
VDD-CPUB	Power Supply for Big Cores of ARM CPU		-0.3	1.3	V
VDD-CPUL	Power Supply for Little Cores of ARM CPU		-0.3	1.3	V
VDD-CPUS	Power Supply for CPUS		-0.3	1.3	V
VDD-DNR	Power Supply for DSP, NPU, and RISC-V		-0.3	1.3	V
VDD-GPU	Power Supply for GPU		-0.3	1.3	V
VDD-SYS	Power Supply for System		-0.3	1.3	V
VDD-DE	Power Supply for DE		-0.3	1.3	V
VDD-VE	Power Supply for VE		-0.3	1.3	V
VDD09-EDP	0.9V EDP Digital Supply		-0.3	1.3	V
VDD09-HDMI	0.9V HDMI Digital Power Supply		-0.3	1.3	V
VDD09-PCIE	0.9 V Power Supply for PCIe2.1		-0.3	1.3	V
VDD09-USB	0.9 V USB Digital Power Supply		-0.3	1.3	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
VDD33	Power Supply for 3.3V Analog Part		-0.3	3.96	V
V_{ESD}	Electrostatic Discharge[2]	Human Body Model (HBM)[3]	-2000	2000	V
		Charged Device Model (CDM)[4]	-250	250	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin[5]		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin[6]		Pass		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2017.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2018.

(5) Based on JESD78E; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

6.3   Recommended Operating Conditions

The following table describes operating conditions of the T527.

📖 **NOTE**

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVCC	Power Supply for Analog Part	1.782	1.8	1.818	V
CPVIN	Analog power for LDO	1.746	1.8	1.854	V
VCC-ADC	Power Supply for GPADC and LRADC	1.782	1.8	1.818	V
VCC-DCXO	Digital Compensated Crystal Oscillator Power Supply	1.782	1.8	1.818	V
VCC-DRAM	Power Supply for DDR3	1.425	1.5	1.575	V
	Power Supply for DDR3L	1.283	1.35	1.45	
	Power Supply for LPDDR3	1.14	1.2	1.30	
	Power Supply for DDR4	1.14	1.2	1.26	
	Power Supply for LPDDR4 and LPDDR4x	1.06	1.1	1.17	
VCC-DRAML	Power Supply for DRAM IO	0.57	0.6[1]	0.65	V
VCC-EFUSE	Power Supply for eFuse	1.62	1.8	1.98	V
VCC-IO	Power Supply for 3.3 V Digital Part	2.97	3.3	3.63	V
VCC-LVDS0	Analog Power Supply for LVDS0/1 and DSI0/1	1.71	1.8	1.89	V
VCC-LVDS1	Analog Power supply for LVDS2/3	1.71	1.8	1.89	V
VCC-MCSI	Power supply for MIPI CSI	1.71	1.8	1.89	V

Symbol	Parameter	Min	Typ	Max	Unit
VCC-PC	Digital Port C Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PD	Digital Port D Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PE	Digital Port E Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3[2]	1.98 3.63	V
VCC-PG	Digital Port G Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PI	Digital Port I Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PJ	Digital Port J Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PK	Digital Port K Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PL	Digital Port L Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PM	Digital Port M Power 1.8 V voltage 3.3 V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-RTC	RTC Power	1.62	1.8	1.98	V
VCC18-PCIE	1.8 V Power Supply for PCIe2.1	1.71	1.8	1.89	V
VCC33-18-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host	3.07	3.3	3.6	V
VCC33-18-USB-2	3.3 V Power Supply for USB2.0 PHY	3.07	3.3	3.6	V

Symbol	Parameter	Min	Typ	Max	Unit
VCC18-EDP	1.8V Analog Supply	1.71	1.8	1.89	V
VCC18-HDMI	1.8 V Power Supply for HDMI	1.71	1.8	1.89	V
VCC33-USB	3.3 V Analog Power Supply for USB2.0 DRD and USB2.0 Host	3.07	3.3	3.6	V
VCC33-USB-2	3.3 V Power Supply for USB2.0 PHY	3.07	3.3	3.6	V
VDD-CPUB	Power Supply for Big Cores of ARM CPU	0.9	-	1.2	V
VDD-CPUL	Power Supply for Little Cores of ARM CPU	0.9	-	1.2	V
VDD-CPUS	Power Supply for CPUS	0.9	-	0.99	V
VDD-DNR	Power Supply for DSP, NPU, and RISC-V	0.9	-	1.1	V
VDD-GPU	Power Supply for GPU	0.9	-	0.99	V
VDD-SYS	Power Supply for System	0.9	-	0.99	V
VDD-DE	Power Supply for DE	0.9	-	0.99	V
VDD-VE	Power Supply for VE	0.9	-	0.99	V
VDD09-EDP	0.9V Digital Supply	0.9	-	0.99	V
VDD09-PCIE	0.9 V Power Supply for PCIe2.1	0.9	-	0.99	V
VDD09-USB	0.9 V USB Digital Power Supply	0.9	-	0.99	V
VDD09-HDMI	0.9V HDMI Digital Power Supply	0.9	-	0.99	V
VDD18-DRAM	DRAM 1.8V Internal PAD Power	1.71	1.8	1.89	V
VDD33	Power Supply for 3.3V Analog Part	2.97	3.3	3.63	V

(1) VCC-DRAML is 0.6 V only when LPDDR4x is used. When DDR3/DDR3L/LPDDR3/DDR4/LPDDR4 is selected, the voltage of VCC-DRAM and VCC-DRAML are the same.

(2) VCC-PE is compatible with 2.8 V typical voltage and the recommended operating range is from 2.7 V to 3.63 V.

6.4　DC Electrical Characteristics

Table 6-3 summarizes the DC electrical characteristics of the T527. For the interfaces of GPIO function port, refer to the DC parameters in Table 6-3 unless otherwise stated.

Table 6-3 DC Electrical Characteristics[1]

(VCC-IO/VCC-PC/ VCC-PD/ VCC-PE/ VCC-PG/ VCC-PI/VCC-PJ/VCC-PK/ VCC-PL/VCC-PM)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V

Symbol	Parameter		Min	Typ	Max	Unit
R$_{PU}$	Input Pull-up Resistance	PL0, PL1	2.82	4.7	6.58	kΩ
		PC0, PC1, PC3, PC6, PC7, PF3, PF6, PG1 to PG5	9	15	21	kΩ
		Other GPIOs	60	100	140	kΩ
R$_{PD}$	Input Pull-down Resistance	PL0, PL1	2.82	4.7	6.58	kΩ
		PC0, PC1, PC3, PC6, PC7, PF3, PF6, PG1 to PG5	9	15	21	kΩ
		Other GPIOs	60	100	140	kΩ
I$_{IH}$	High-Level Input Current		-	-	10	uA
I$_{IL}$	Low-Level Input Current		-	-	10	uA
V$_{OH}$	High-Level Output Voltage		VCC-IO (b)0.3	-	VCC-IO	V
V$_{OL}$	Low-Level Output Voltage		0	-	0.2	V
I$_{OZ}$	Tri-State Output Leakage Current		-10	-	10	uA
C$_{IN}$	Input Capacitance		-	-	5	pF
C$_{OUT}$	Output Capacitance		-	-	5	pF

(1) Guaranteed by design.

All I/Os in T527 are CMOS. The following figure shows the input characteristics for standard I/Os.

Figure 6-1 Standard I/O Input Characteristics - CMOS port

CMOS standard requirement:

VIH=0.6933VDD

VIL=0.4198VDD
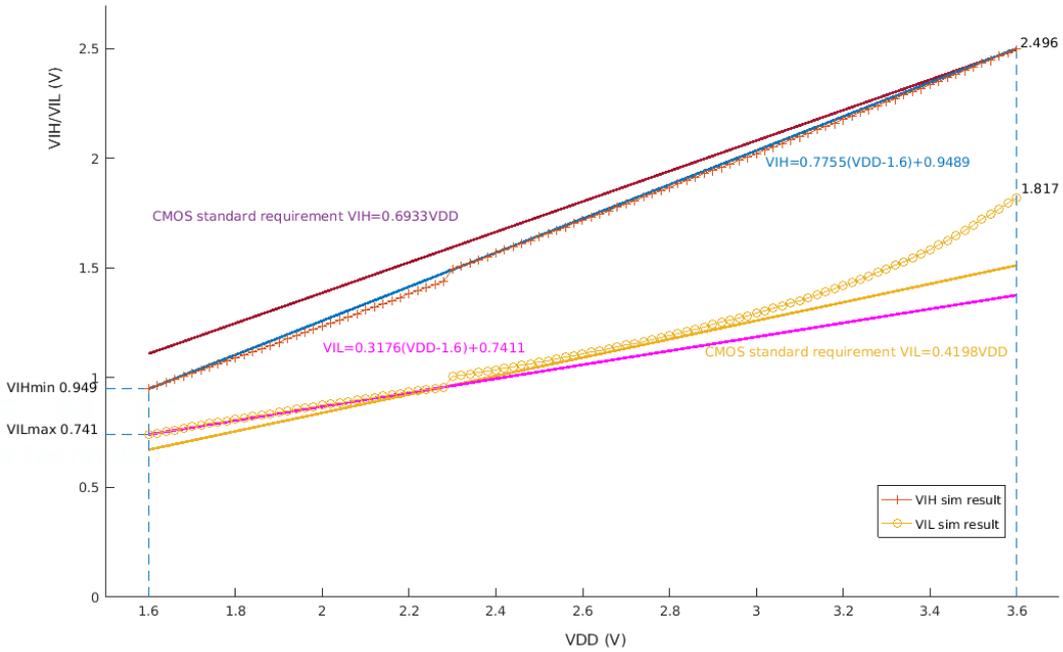
6.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 6-2 SMHC Voltage Waveform
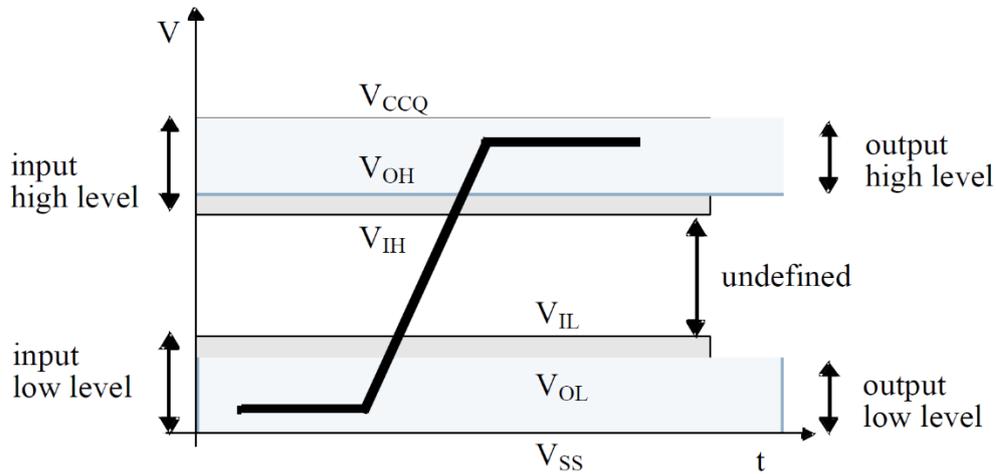
Table 6-4 shows 3.3 V SMHC electrical parameters.

Table 6-4 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} (b)0.3	-	0.25 * V_{CCQ}	V

Table 6-5 shows 1.8 V SMHC electrical parameters.

Table 6-5 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} (b)0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.65 * V_{CCQ} [1]	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} (b)0.3	-	0.35 * V_{CCQ} [2]	V
(1).0.7 * V_{CCQ} for MMC5.1 lower.					
(2).0.3 * V_{CCQ} for MMC5.1 lower.					

6.6 GPADC Electrical Characteristics

Table 6-6 lists GPADC electrical characteristics.

Table 6-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	1.8	V
Effective Precision	-	10	-	bits
Sampling Rate	-	-	1	MHz
Conversion Time	-	13	-	ADC Clock Cycles

6.7 LRADC Electrical Characteristics

Table 6-7 lists LRADC electrical characteristics.

Table 6-7 LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range			LEVELB[1]	V
Effective Precision	-	5	-	bits
Sampling Rate	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.286 V. For details, see the register description of LRADC in *T527_User_Manual*.				

6.8 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 6-8 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to HPOUTL or HPOUTR(R=10K,CPVDD=1.2V)					
	Full-scale	0 dBFS 1 kHz	-	555	-	mVrms
	SNR(A-weighted)	0 data	-	100	-	dB
	THD+N	0 dBFS 1 kHz	-	-89	-	dB
	Crosstalk	R_0dB_L_0data 1kHz L_0dB_R_0data 1kHz	-	-94	-	dB
	DAC to HPOUTL or HPOUTR(R=16Ω,CPVDD=1.2V)					
	Full-scale	0dBFS 1 kHz	-	520	-	mVrms
	SNR(A-weighted)	0data	-	100	-	dB
	THD+N (16.5mW)	Full-scale Level	-	-25	-	dB
	THD+N(10mW)	1 kHz	-	-77	-	dB
	Crosstalk	R_0dB_L_0data 1 kHz L_0dB_R_0data 1 kHz	-	-94	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	DAC to HPOUTL or HPOUTR(R=32Ω, CPVDD=1.2V)					
	Full-scale	0 dBFS 1 kHz	-	540	-	mVrms
	SNR(A-weighted)	0 data	-	100	-	dB
	THD+N (9.0mW)	0 dBFS 1 kHz	-	-83	-	dB
	Crosstalk	R_0dB_L_0data 1 kHz L_0dB_R_0data 1 kHz	-	-94	-	dB
	DAC to LINEOUTLP/N or LINEOUTRP/N(R=100K)					
	Full-scale	0 dBFS 1 kHz	-	1.08	-	Vrms
	SNR(A-weighted)	0data	-	103	-	dB
	THD+N	0 dBFS 1 kHz	-	-90	-	dB
	Crosstalk	R_0dB_L_0data 1 kHz L_0dB_R_0data 1 kHz	-	-110	-	dB
	MICIN via ADC					
	Output Level	MICP=3.3Vpp/2,MICN=3.3Vpp/2, 1 kHz, 0 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-84	-	dB
	Output Level	MICP=1.69Vpp/2,MICN=1.69Vpp/2, 1 kHz, 6 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	93	-	dB
	THD+N		-	-87	-	dB
	Output Level	MICP=0.805Vpp/2,MICN=0.805Vpp/2, 1 kHz, 12 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	93	-	dB
	THD+N		-	-82	-	dB
ADC Path	Output Level	MICP=0.4035Vpp/2,MICN=0.4035Vpp/2, 1 kHz, 18 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	91	-	dB
	THD+N		-	-83	-	dB
	Output Level	MICP=0.204Vpp/2,MICN=0.204Vpp/2, 1 kHz , 24 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	89	-	dB
	THD+N		-	-82	-	dB
	Output Level	MICP=0.1032Vpp/2,MICN=0.1032Vpp/2, 1 kHz, 30 dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	86	-	dB
	THD+N		-	-79	-	dB
	Output Level	MICP=0.0524Vpp/2,MICN=0.0524Vpp/2,	-	880	-	mFFS
	SNR(A-weighted)		-	80	-	dB

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	THD+N	1 kHz, 36 dB Gain	-	-76	-	dB

6.9 Clock Electrical Characteristics

6.9.1 Input Clock Requirements

6.9.1.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 6-9 High-speed 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
$f_{X24M-IN}$	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C [1]	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance [2]	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of T527. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.

2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 6-10 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/ (C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.

- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance (C_{pkg} + C_{PCB}) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

6.9.1.2 Low-speed Crystal/Ceramic Resonator Characteristics

The T527 contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.

The T527 also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 6-11 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{X32K-IN}$	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C [1]	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance [2]	-	1.1	-	pF

The T527 has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.

The 1.1 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

6.9.2 Output Clock Characteristics

6.9.2.1 24MHz Clock Fanout

The REFCLK-OUT signal can output 24MHz clock. The following table lists the output clock characteristics.

Table 6-12 REFCLK-OUT Output Clock Characteristics

Parameter	Specification	Unit
Input Source	24 MHz crystal	-
Nominal Output Frequency	24	MHz
Frequency Accuracy	The output frequency accuracy is related to the accuracy of external crystal.	ppm
Duty Cycle	50	%
Signal Type	Square-wave	-

6.9.2.2 32.768 kHz Clock Fanout

The X32KFOUT signal can output 32.768 kHz clock. The following table lists the output clock characteristics.

Table 6-13 X32KFOUT Output Clock Characteristics

Parameter	Specification	Unit
Input Source	24 MHz crystal or 32.768 kHz crystal	-
Nominal Output Frequency	32.768	kHz
Frequency Accuracy	The output frequency accuracy is related to the accuracy of external crystal.	ppm
Duty Cycle	50	%
Signal Type	Square-wave	-

6.10 Internal Reset Electrical Characteristics

Table 6-14 Internal Reset Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Power-on threshold voltage of VDD-SYS on which the reset signal is excited	Ta=-40① to 85①	-	700	-	mV
Reset active timeout period	Ta=-40① to 85①	-	32[1]	-	ms

(1) This indicates the time required for T527 to complete reset.

6.11 Interface Timings

6.11.1   NAND Interface Timing

Figure 6-3 Conventional Serial Access Cycle Timing (SAM0)
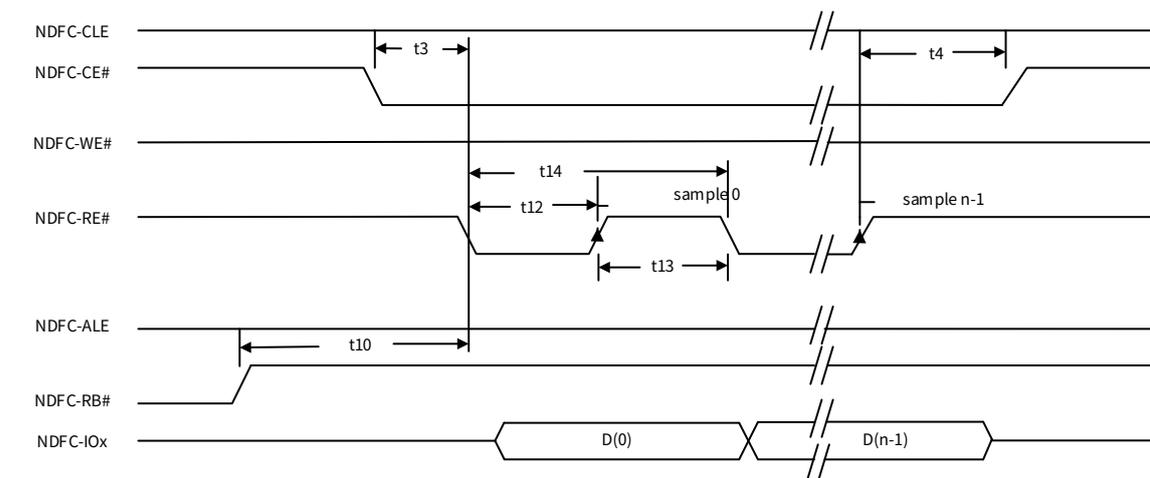
Figure 6-4 EDO Type Serial Access after Read Cycle Timing (SAM1)
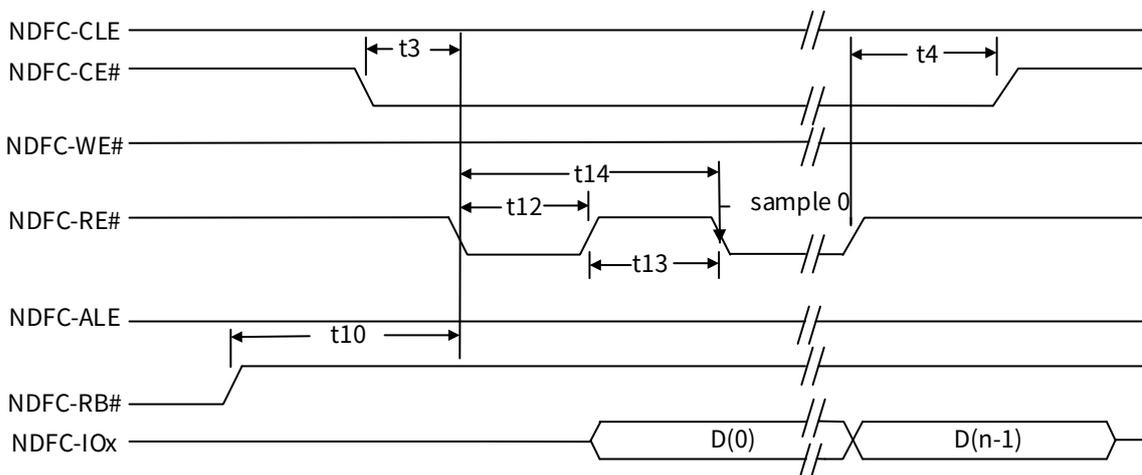
Figure 6-5 Extending EDO Type Serial Access Mode Timing (SAM2)
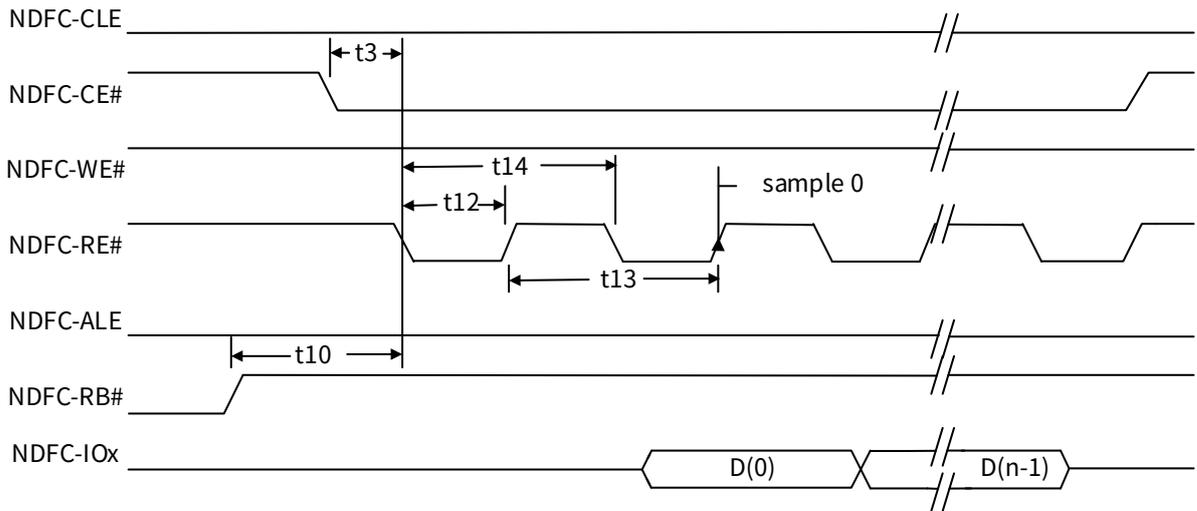
Figure 6-6 Command Latch Cycle Timing
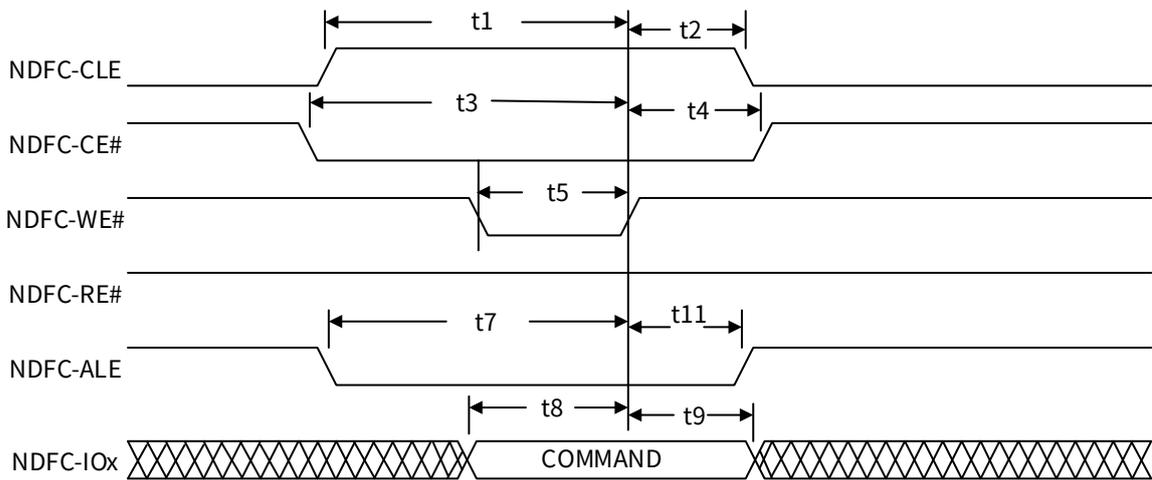
Figure 6-7 Address Latch Cycle Timing
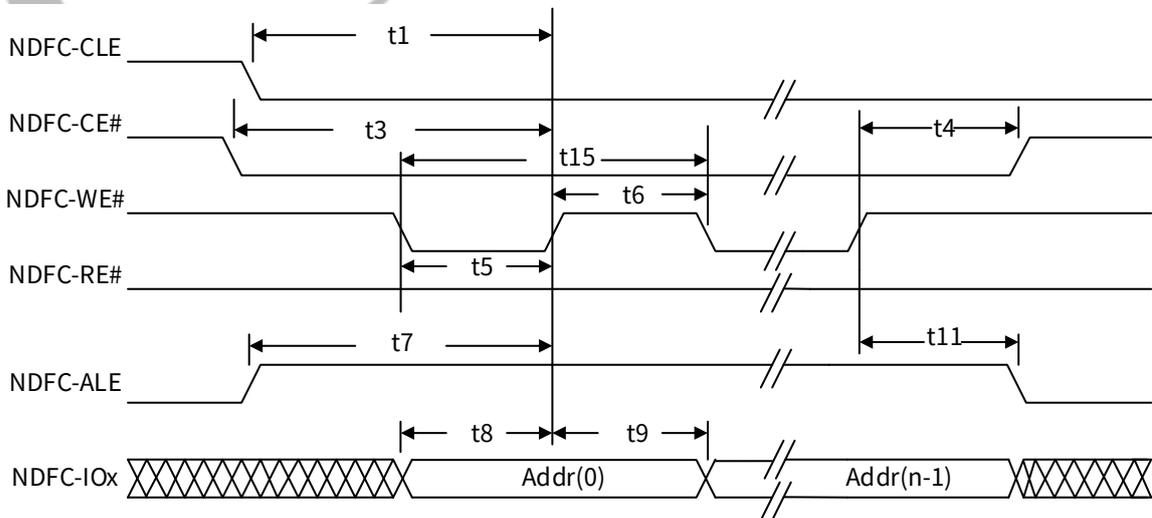
Figure 6-8 Write Data to Flash Cycle Timing
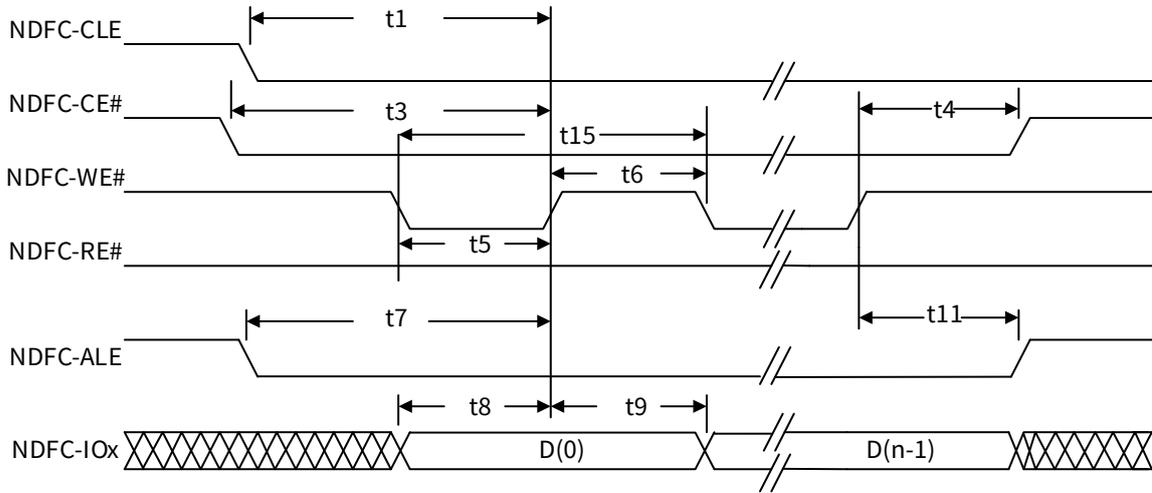
Figure 6-9 Waiting R/B# Ready Timing
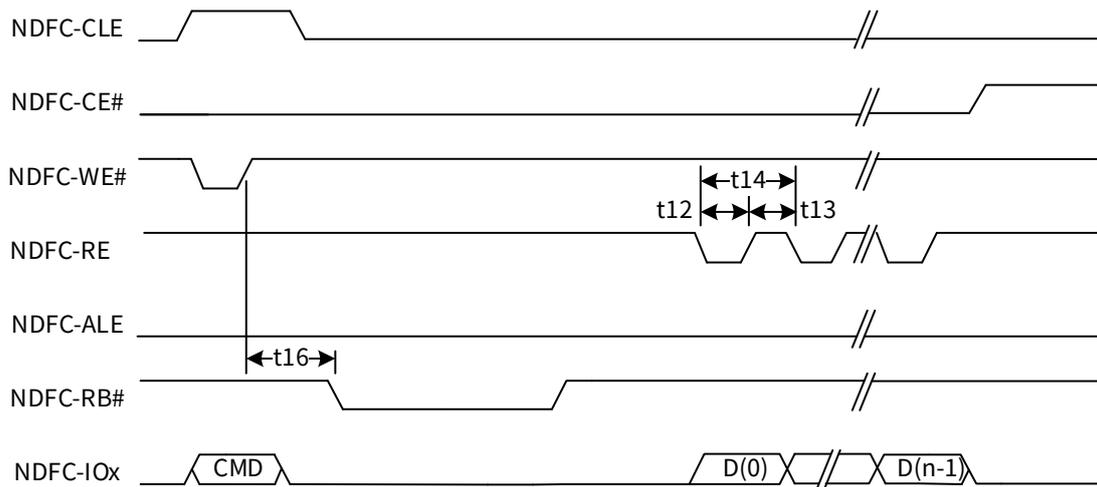
Figure 6-10 WE# High to RE# Low Timing
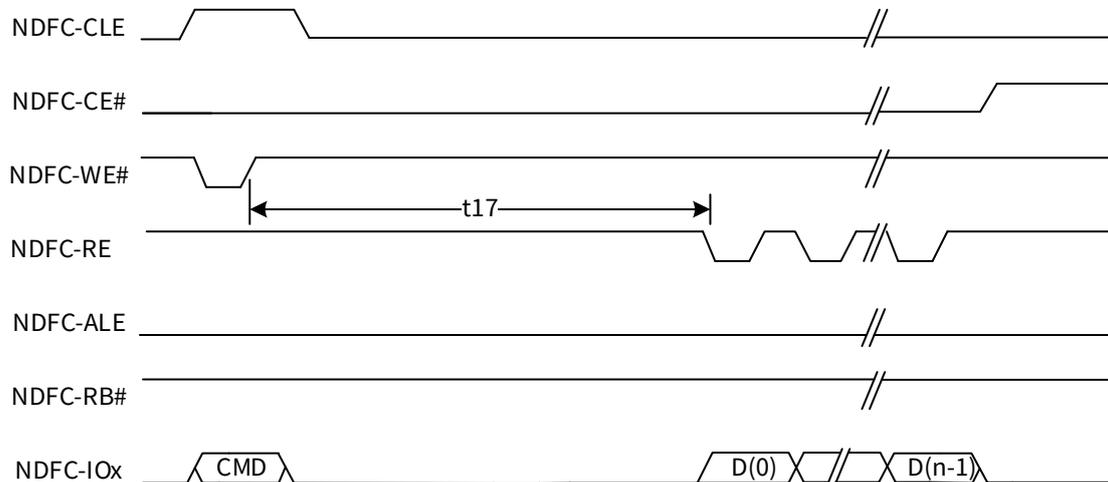
Figure 6-11 RE# High to WE# Low Timing
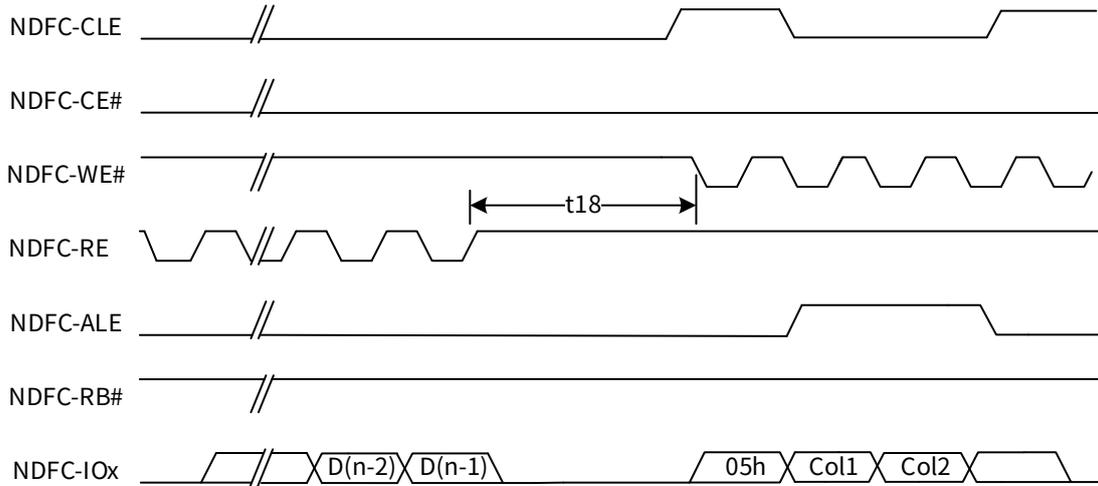
Figure 6-12 Address to Data Loading Timing
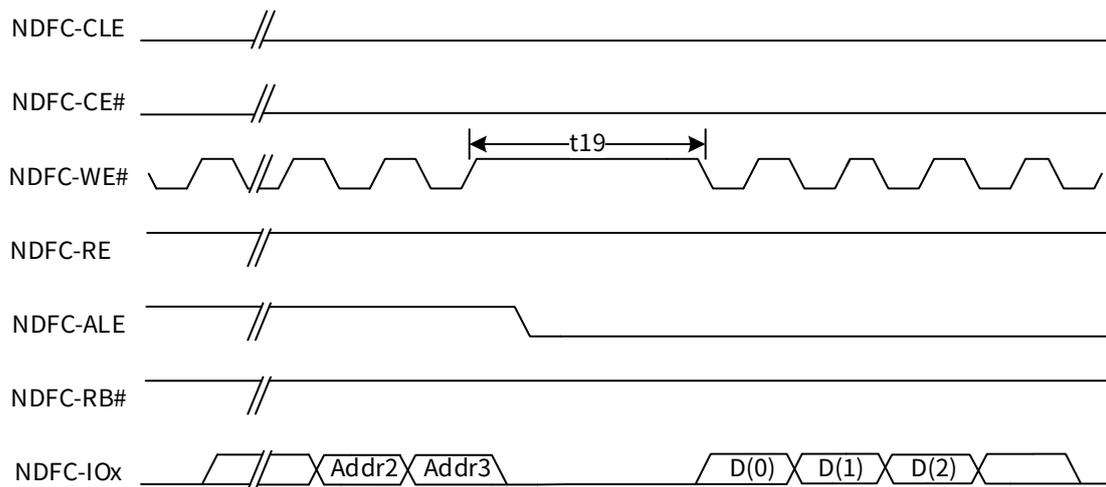
Table 6-15 NDFC Timing Constants

Parameter	Symbol	Timing	Unit
NDFC-CLE setup time	t1	2T	ns
NDFC-CLE hold time	t2	2T	ns
NDFC-CE setup time	t3	2T	ns
NDFC-CE hold time	t4	2T	ns
NDFC-WE# pulse width	t5	T[1]	ns
NDFC-WE# hold time	t6	T	ns
NDFC-ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns

Parameter	Symbol	Timing	Unit
Ready to NDFC-RE# low	t10	3T	ns
NDFC-ALE hold time	t11	2T	ns
NDFC-RE# pulse width	t12	T	ns
NDFC-RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC-WE# high to R/B# busy	t16	T_WB[2]	ns
NDFC-WE# high to NDFC-RE# low	t17	T_WHR[3]	ns
NDFC-RE# high to NDFC-WE# low	t18	T_RHW[4]	ns
Address to Data Loading time	t19	T_ADL[5]	ns
(1) T is the cycle of internal clock. (2), (3), (4), (5) This values are configurable in NAND Flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 8*2T/16*2T/24*2T/32*2T, the value of T_RHW could be 4*2T/8*2T/12*2T/20*2T, the value of T_ADL could be 0*2T/8*2T/16*2T/24*2T.			

6.11.2   SMHC Interface Timing

6.11.2.1   HS-SDR Mode

 NOTE

IO voltage is 1.8V or 3.3V.

Figure 6-13 SMHC HS-SDR Mode Output Timing Diagram
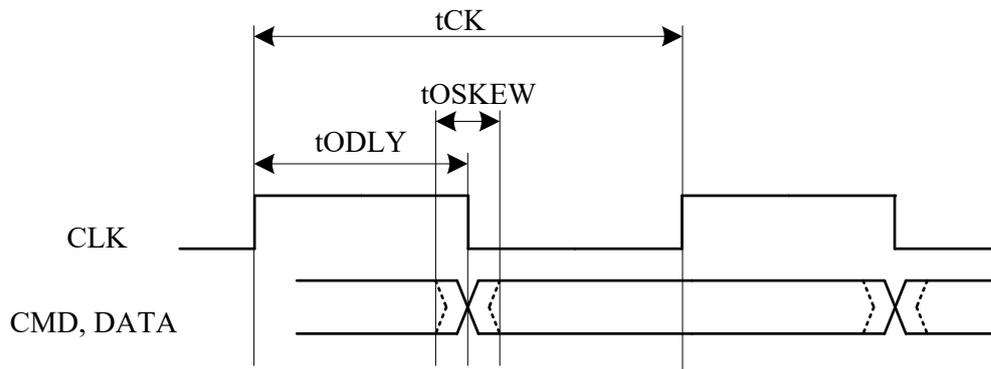
Table 6-16 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.					
(2) The driver strength level of GPIO is 2 for test.					

Figure 6-14 SMHC HS-SDR Mode Input Timing Diagram
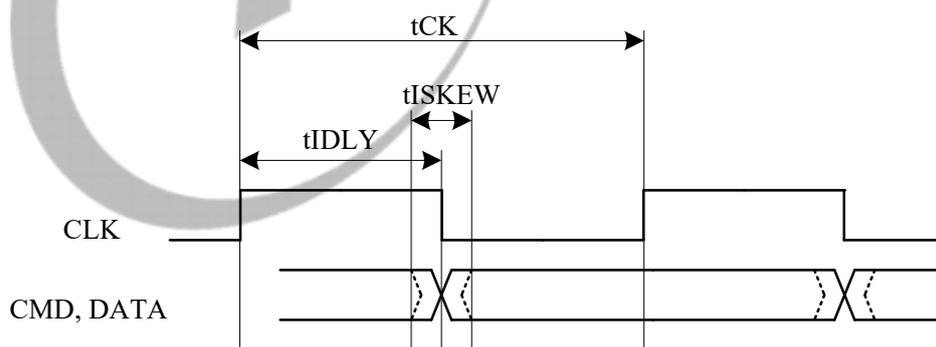
Table 6-17 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%

Parameter	Symbol	Min	Typ	Max	Unit
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

6.11.2.2   HS-DDR Mode

Figure 6-15 SMHC HS-DDR Mode Output Timing Diagram
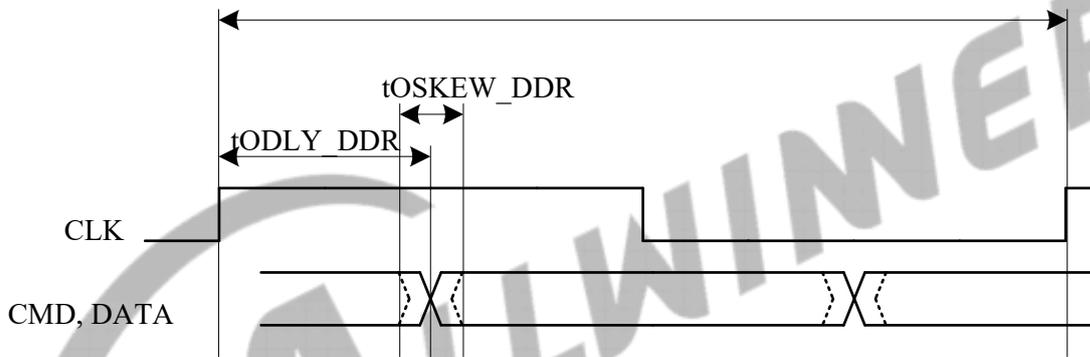
Table 6-18 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 6-16 SMHC HS-DDR Mode Input Timing Diagram
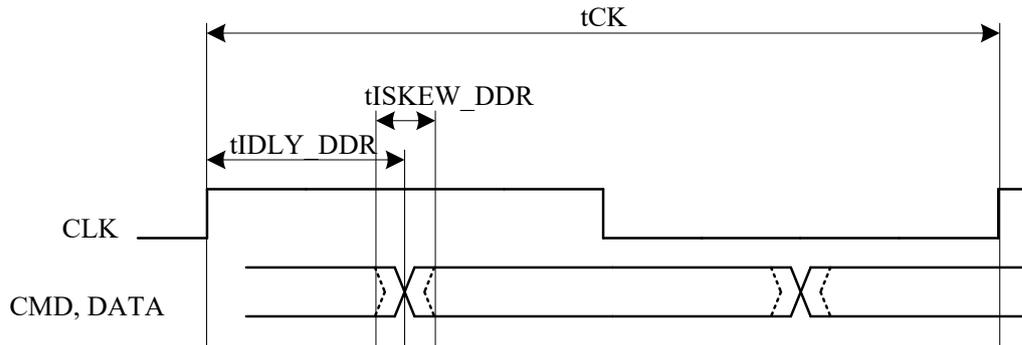
Table 6-19 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
Data input skew time in DDR mode	tISKEW-DDR	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

6.11.2.3 HS200/SDR104 Mode

Figure 6-17 SMHC HS200/SDR104 Mode Output Timing Diagram
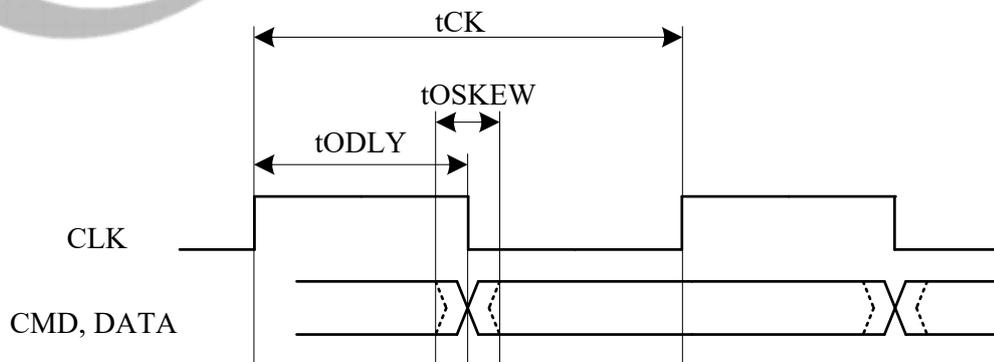
Table 6-20 SMHC HS200/SDR104 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	-	-	200	MHz
Duty Cycle	DC	45	50	55	%
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.					
(2) The driver strength level of GPIO is 3 for test.					

Figure 6-18 SMHC HS200/SDR104 Mode Input Timing Diagram
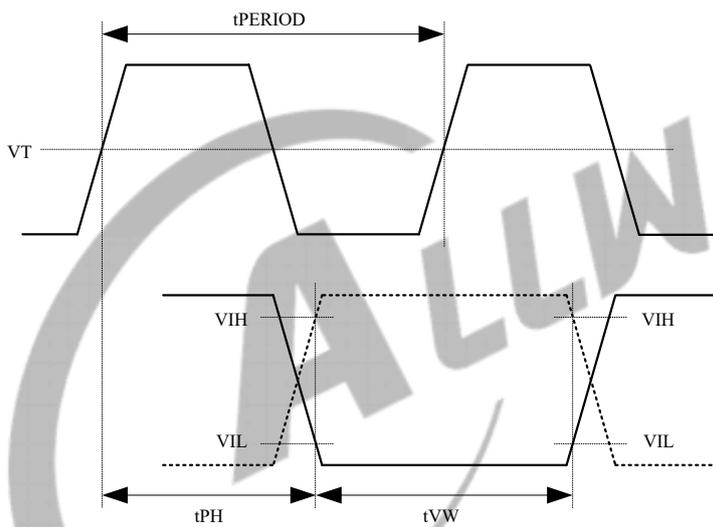
Table 6-21 SMHC HS200 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	5	-	-	ns	Max: 200MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA (referenced to CLK)						
Output delay	tPH	0	-	2	UI	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, Data valid window	tVW	0.575	-	-	UI	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test. (3) Temperature variation: -20 °C. (4) Temperature variation: 90 °C.						

6.11.2.4 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 6-19 SMHC HS400 Mode Output Timing Diagram
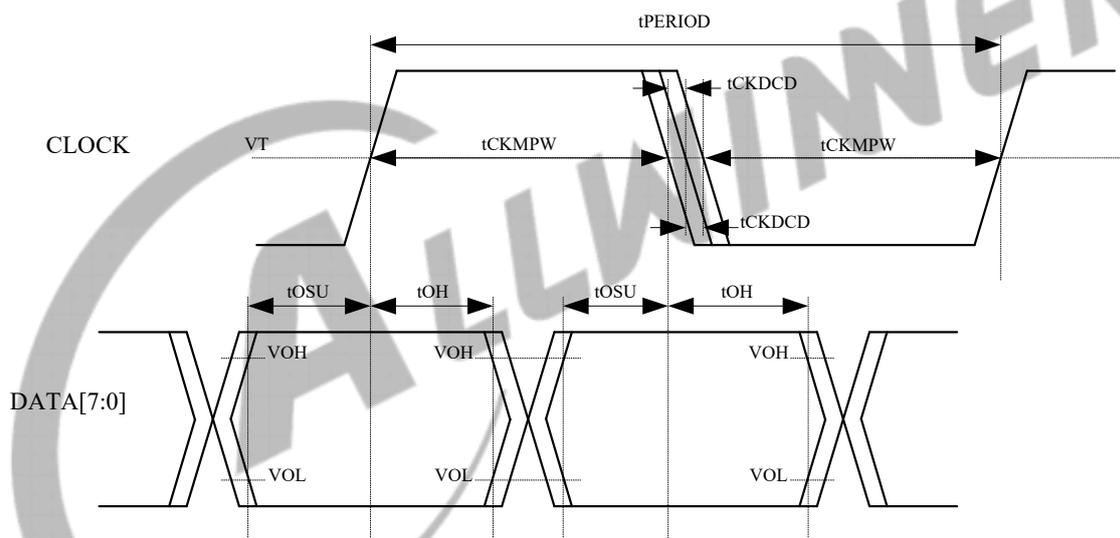
Table 6-22 SMHC HS400 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	5	-	-	ns	Max: 200MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA (referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.						
(2) The driver strength level of GPIO is 3 for test.						

Figure 6-20 SMHC HS400 Mode Input Timing Diagram
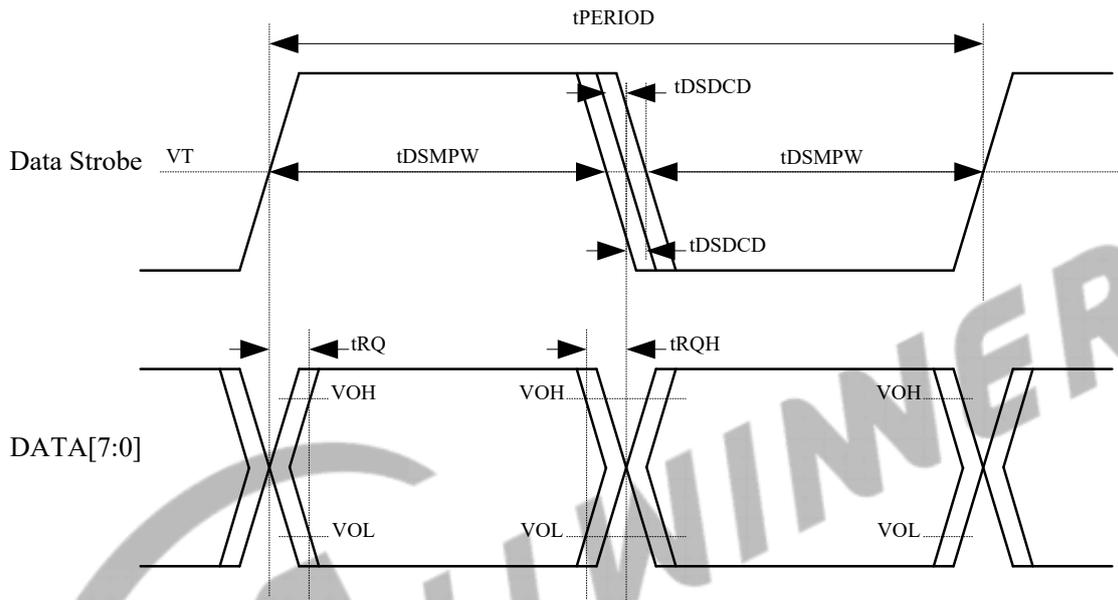
Table 6-23 SMHC HS400 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS (Data Strobe)						
DS period	tPERIOD	5	-	-	ns	Max: 200MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA (referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.						
(2) The driver strength level of GPIO is 3 for test.						

6.11.3   UART Interface Timing

Figure 6-21 UART RX Timing

Register Setting:

    Data length(DLS in LCR[1:0]) = 3 (8bit)

    Stop bit length(STOP in LCR[2]) = 1 (2bit)

    Parity enable(PEN in LCR[3]) = 1

RX   start   data   parity   stop

RX FIFO
DATA   vaild data
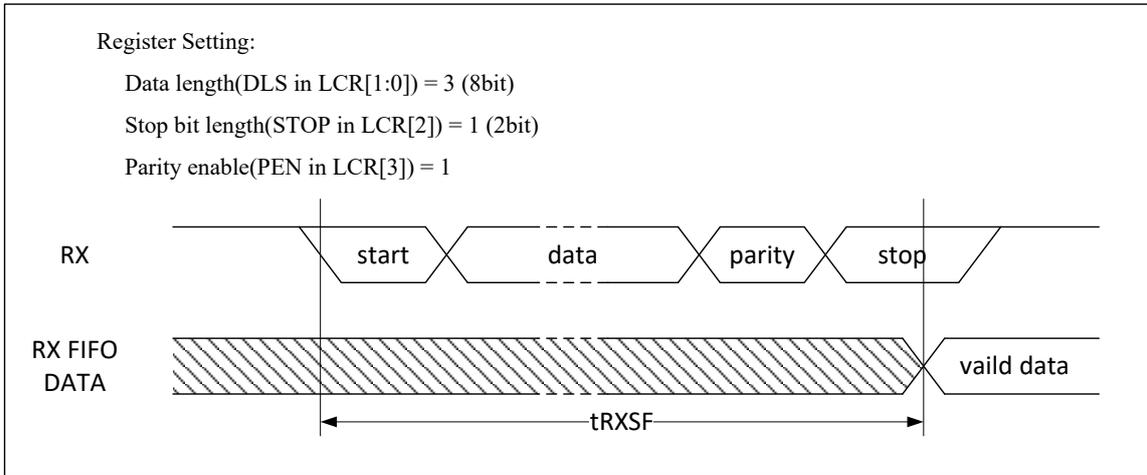
tRXSF

Figure 6-22 UART nCTS Timing

TX   start   data   parity   stop   start

nCTS

tDCTS   tACTS
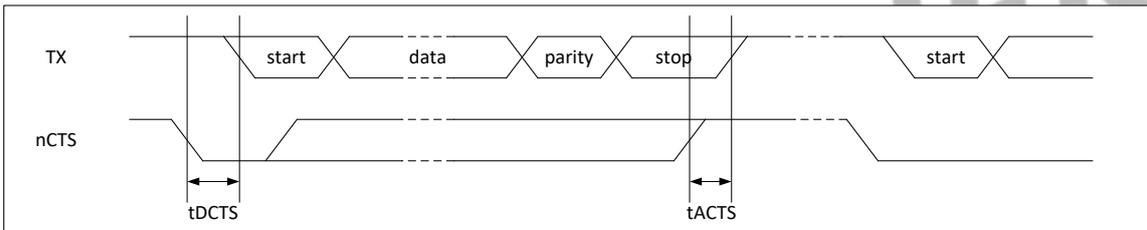
Figure 6-23 UART nRTS Timing

Register Setting:

    RTS Trigger level(RT in FCR[7:6]) = 3 (De-asserted nRTS when FIFO valid data number reach FIFO depth-2)

RX FIFO
DATA NUM   FD[1]-3   FD-2   0

nRTS

tDRTS   tARTS

Note (1): FD: FIFO Depth
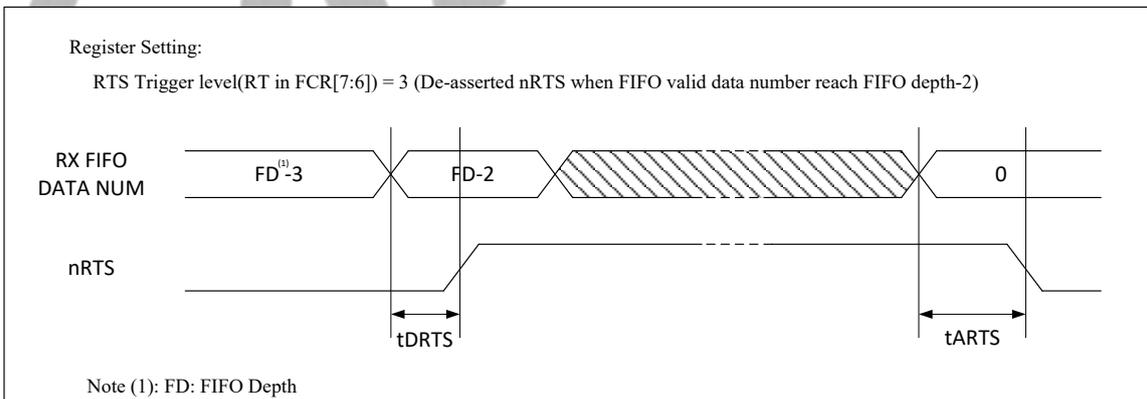
Table 6-24 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	$10.5*BRP^{(1)}$	-	$11*BRP^{(1)}$	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	$BRP^{(1)}$	ns
Step time of asserted nCTS to stop next transmission	tACTS	$BRP^{(1)}/4$	-	-	ns

Parameter	Symbol	Min	Typ	Max	Unit
Delay time of de-asserted nRTS	tDRTS	-	-	BRP[1]	ns
Delay time of asserted nRTS	tARTS	-	-	BRP[1]	ns
BRP: Baud-Rate Period.					

6.11.4   SPI Interface Timing

Figure 6-24 SPI Writing Timing
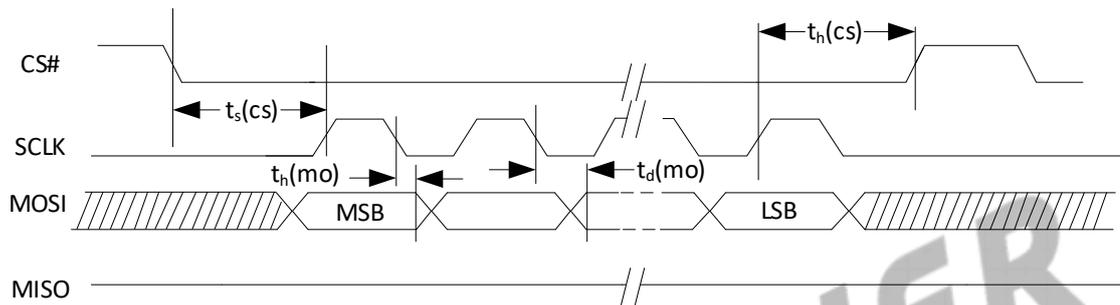
Figure 6-25 SPI Reading Timing
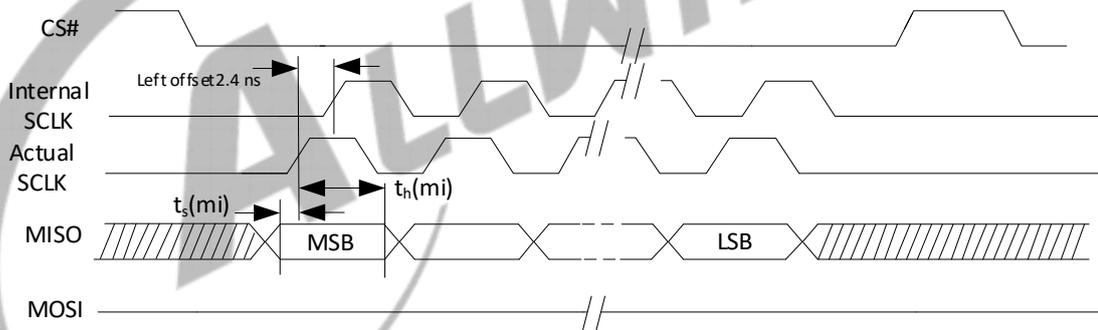
Table 6-25 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	$t_s(cs)$	-	$2T^{(1)}$	-	ns
CS# Active Hold Time	$t_h(cs)$	-	$2T^{(1)}$	-	ns
Data output Delay Time	$t_v(mo)$	-	$T^{(1)}/2-3$	-	ns
Data output Hold Time	$t_h(mo)$	-	$T^{(1)}/2-3$	-	ns
Data In Setup Time	$t_s(mi)$	0.2	-	-	ns
Data In Hold Time	$t_h(mi)$	0.2	-	-	ns
(1) T is the cycle of clock.					

6.11.5 SPI-DBI Interface Timing

Figure 6-26 DBI 3-line Serial Interface Timing
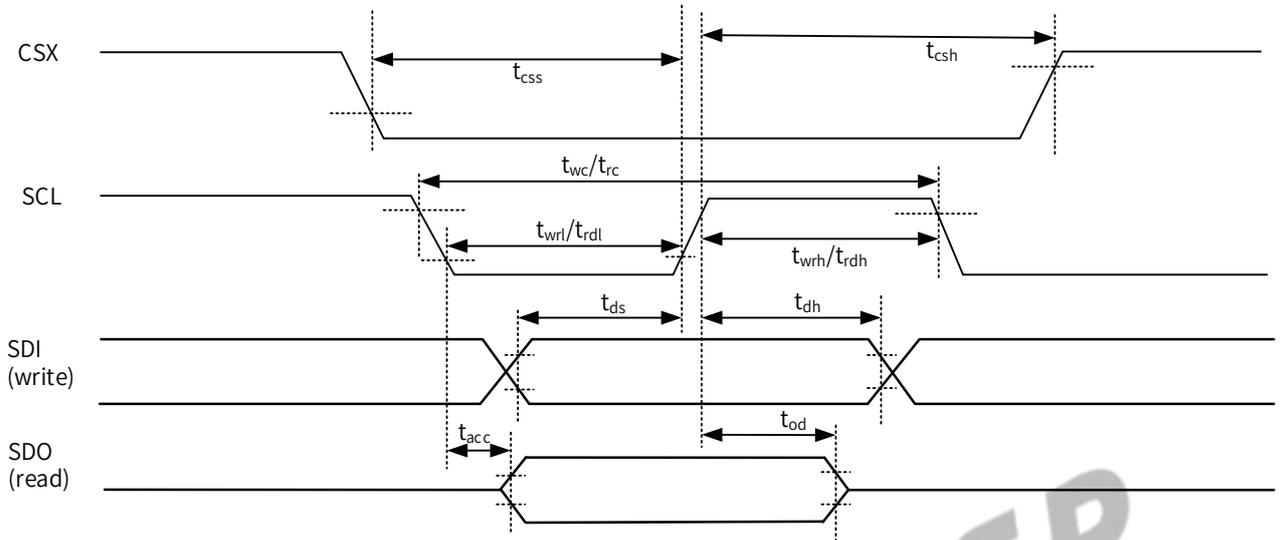
Table 6-26 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse H duration	t_{wrh}	7		ns
	Control pulse L duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7[1]		ns
	Data hold time	t_{dt}	7[1]		ns
Note:					
Range of required clock frequency: 0-60 MHz.					

Table 6-27 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse H duration	t_{rdh}	60		ns
	Control pulse L duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10[1]	50	ns
	Output disable time	t_{od}	15[1]	50	ns

Signal	Parameter	Symbol	Min	Max	Unit
Note:					
Range of required clock frequency: 0-6.67 MHz.					

Figure 6-27 DBI 4-line Serial Interface Timing
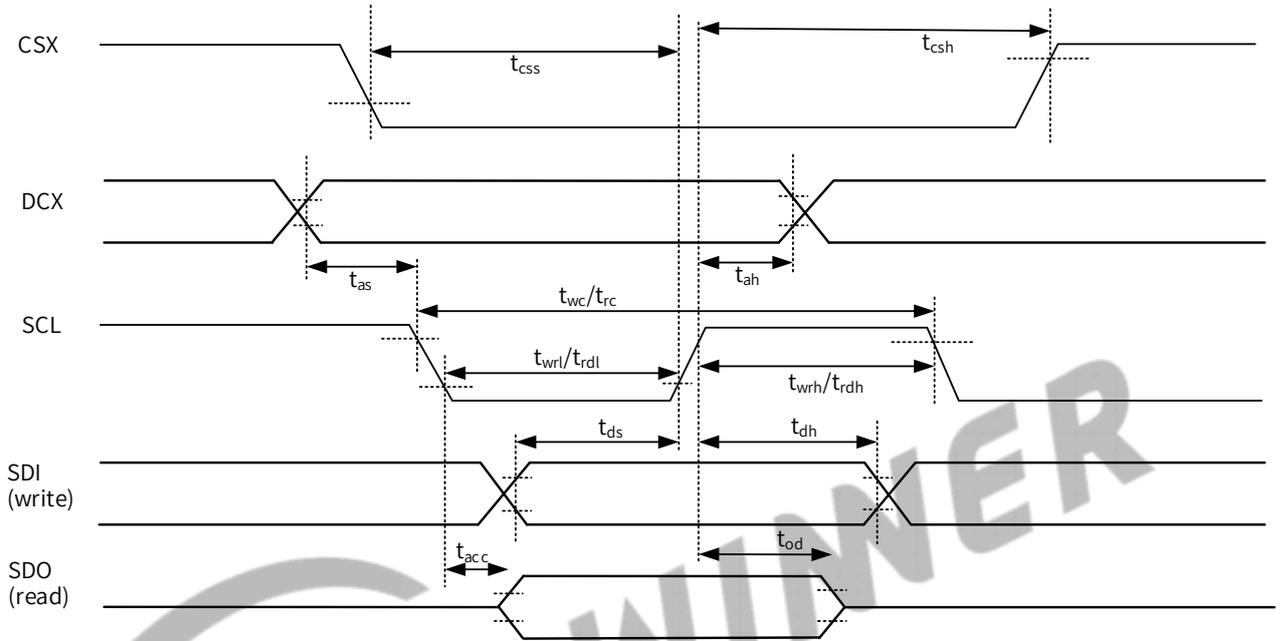
Table 6-28 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse H duration	t_{wrh}	7		ns
	Control pulse L duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7[1]		ns
	Data hold time	t_{dt}	7[1]		ns
	Output disable time	t_{od}	15[1]	50	ns
Note:					
Range of required clock frequency: 0-60 MHz.					

Table 6-29 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse　H　duration	t_{rdh}	60		ns
	Control pulse　L　duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15[1]	50	ns
Note:					
Range of required clock frequency: 0-6.67 MHz.					

6.11.6　SPI Flash Interface Timing

6.11.6.1　Controller Output to Target Input Timing

Figure 6-28 xSPI Target Data Input Timing
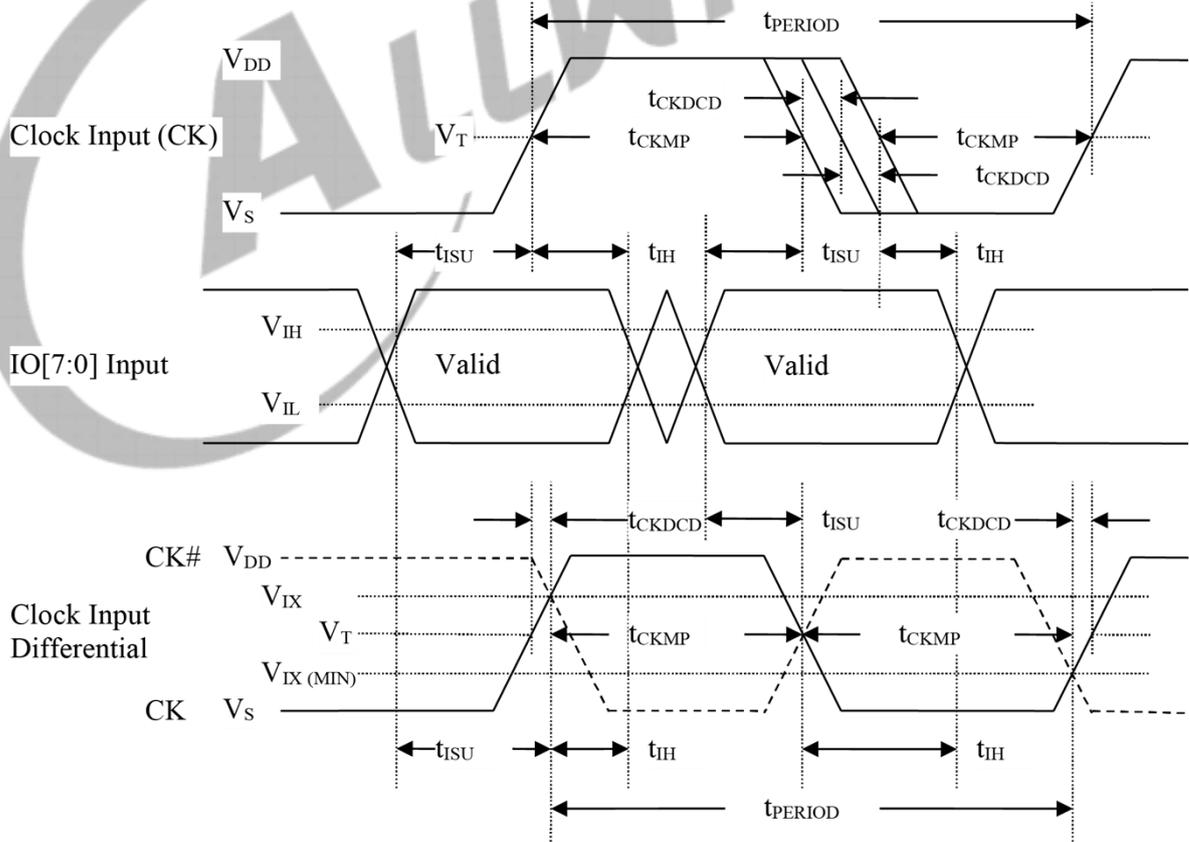
Table 6-30 Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	$V_{T\,(AC)}$	0.50 * V_{DD}	0.50 * V_{DD}	V
Input differential crossing (AC)	$V_{IX\,(AC)}$	0.4 * V_{DD}	0.60 * V_{DD}	V

Table 6-31 xSPI Device Input Timing

Parameter	Symbol	xSPI-333[1]		xSPI-266[2]		xSPI-200[3]		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Input CK									
Cycle Time Data Transfer Mode	t_{PERIOD}	6	-	7.5	-	10	-	ns	150 MHz (max) between the rising edges with respect to V_T.
Slew Rate	SR	0.94	-	0.75	-	0.56	-	V/ns	With respect to VIH/VIL.
Duty Cycle Distortion	t_{CKDCD}	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{CKMPW}	2.7	-	3.375	-	4.5	-	ns	With respect to V_T.
Input Signals (Referenced to CK)									
Input Setup Time (DTR)	t_{ISUddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (DTR)	t_{IHddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Setup Time (STR)	t_{ISU}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (STR)	t_{IH}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Slew Rate @ 1.8 V	SR	0.94	--	0.75	-	0.56	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 3.0 V	SR	1.72	-	1.37	-	1.03	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference

Parameter	Symbol	xSPI-333[1]		xSPI-266[2]		xSPI-200[3]		Unit	Comments
		Min	Max	Min	Max	Min	Max		
									load.

Note:

(1) xSPI-333: Up to 166 MHz; up to 333 MT/s.

(2) xSPI-266: Up to 133 MHz; up to 266 MT/s.

(3) xSPI-200: Up to 100 MHz; up to 200 MT/s.

6.11.6.2 Target Output to Controller Input Timing

Figure 6-29 xSPI Target Data Output Timing
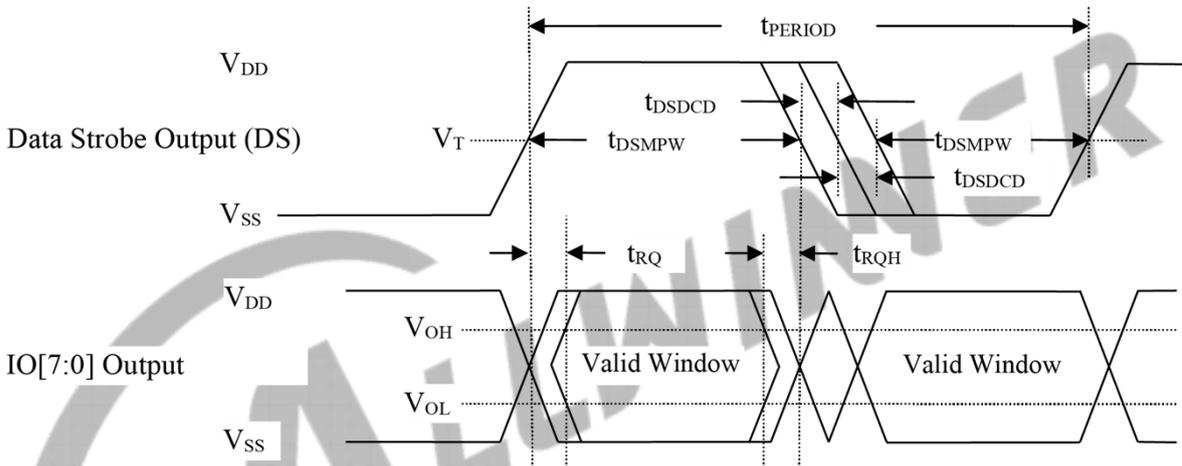
Table 6-32 xSPI Device Output Timing

Parameter	Symbol	xSPI-200[1]		Unit	Comments
		Min	Max		
Data Strobe[2]					
Cycle Time Data Transfer Mode	t_{PERIOD}	10	-	ns	100 MHz (max) between the rising edges with respect to V_T.
Duty Cycle Distortion	t_{DSDCD}	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (tCKDCD) with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{DSMPW}	4.1	-	ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With

Parameter	Symbol	xSPI-200[1]		Unit	Comments
		Min	Max		
					respect to V_T.
Output DATA (Referenced to DS)					
Output skew	t_{RQ}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Output hold skew	t_{RQH}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Note:					
(1) xSPI-200: Up to 100 MHz; up to 200 MT/s.					
(2) Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their related (triggering) CK edges.					

6.11.7   TWI Interface Timing

Figure 6-30 TWI Timing
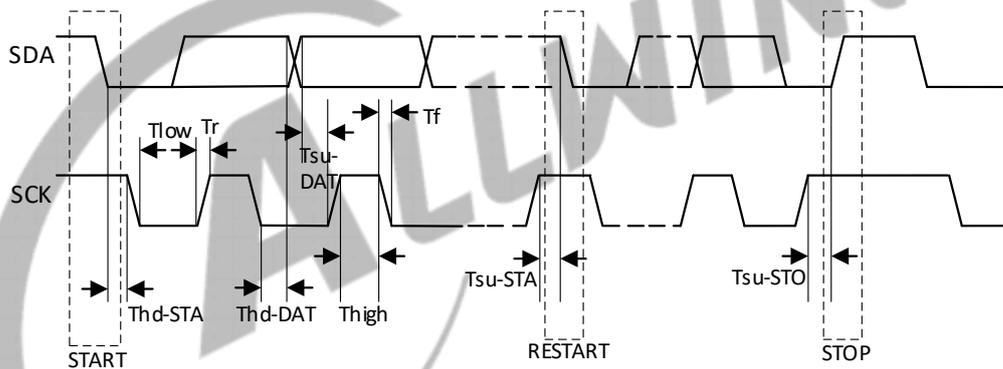
Table 6-33 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	5.0	-	-	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

6.11.8   GMAC Interface Timing

6.11.8.1   RGMII

Figure 6-31 RGMII Receive Timing
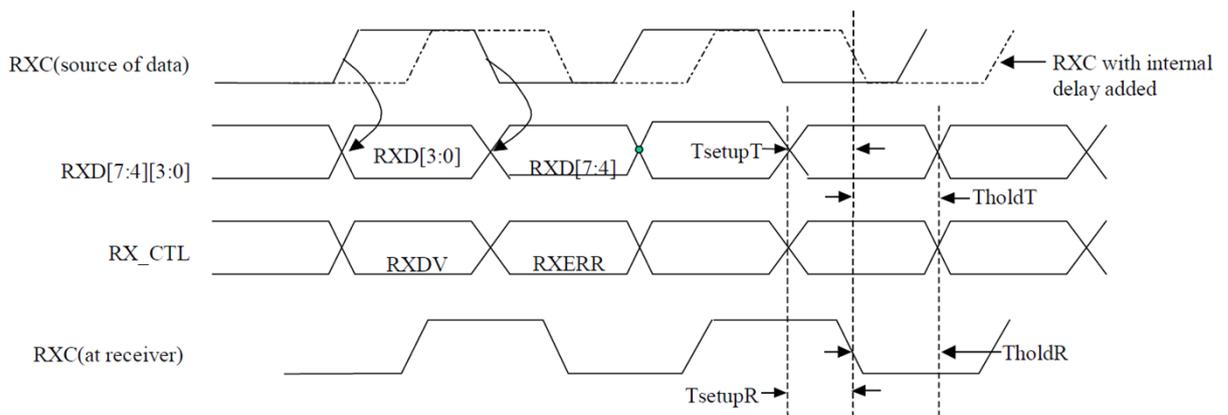
Figure 6-32 RGMII Transmit Timing
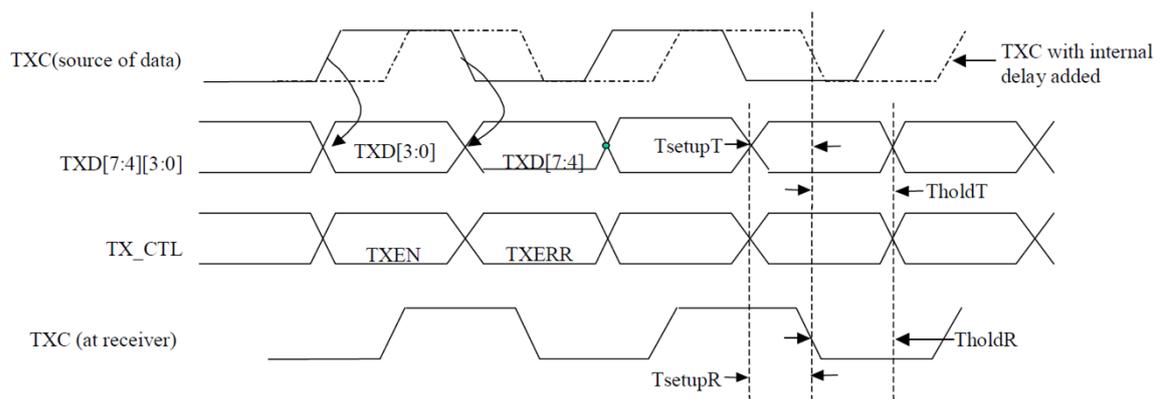
Table 6-34 RGMII Timing Constants

Parameter	Description	Min	Typical	Max	Unit
Tcyc	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%

Parameter	Description	Min	Typical	Max	Unit
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to Clock Output Setup (at Transmitter Integrated Delay)	1.2	2.0	-	ns
TholdT	Data to Clock Output Hold (at Transmitter Integrated Delay)	1.2	2.0	-	ns
TsetupR	Data to Clock Input Setup (at Receiver Integrated Delay)	1.0	2.0	-	ns
TholdR	Data to Clock Input Hold (at Receiver Integrated Delay)	1.0	2.0	-	ns
For 10Mbps and 100Mbps, Tcyc will scale 400ns±40ns and 40ns±4ns.					

6.11.8.2   RMII

Figure 6-33 RMII Receive Timing
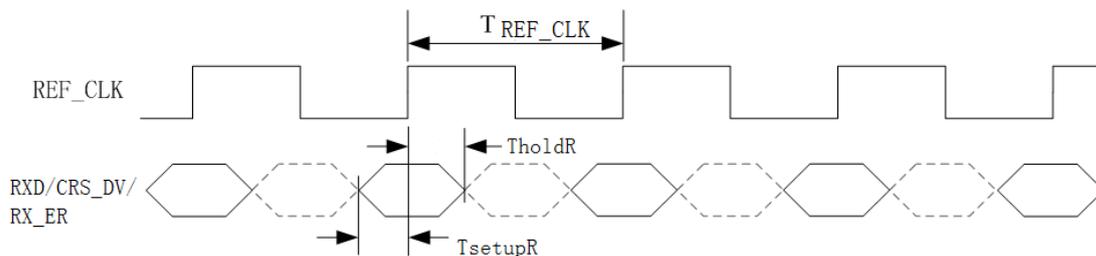
Figure 6-34 RMII Transmit Timing
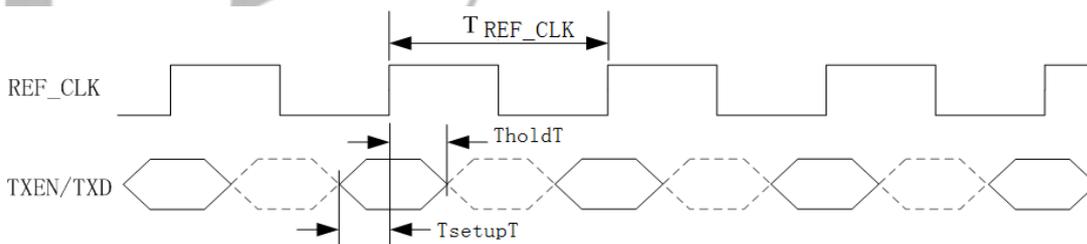
Table 6-35 RMII Timing Constants

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK Duty Cycle	35	-	65	%
TsetupT	TXD/TXEN to REF_CLK Setup Time	4	-	-	ns
TholdT	TXD/TXEN to REF_CLK Hold Time	2	-	-	ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK Setup Time	4	-	-	ns

Parameter	Description	Min	Typ	Max	Unit
TholdR	RXD/CRS_DV/RX_ER to REF_CLK Hold Time	2	-	-	ns

6.11.9　GMAC200 Interface Timing

6.11.9.1　RGMII

Figure 6-35 RGMII Receive Timing
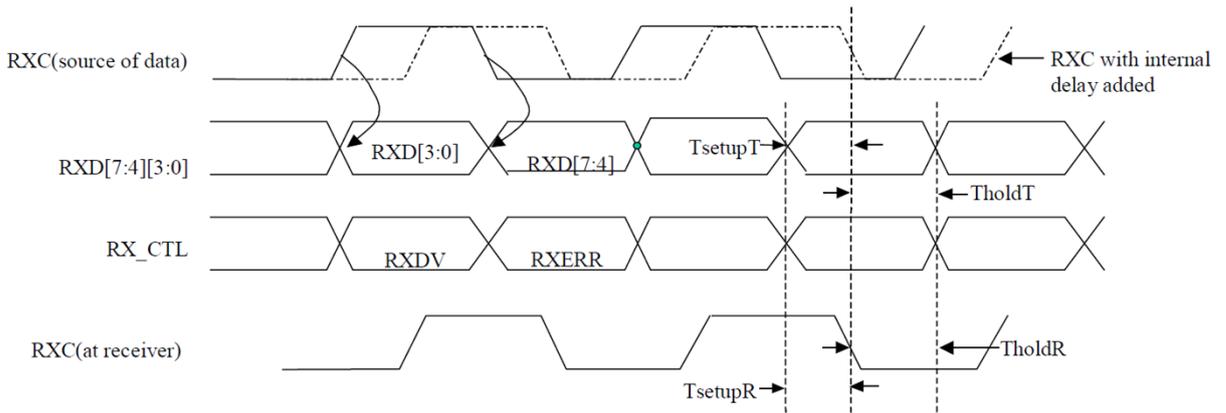
Figure 6-36 RGMII Transmit Timing
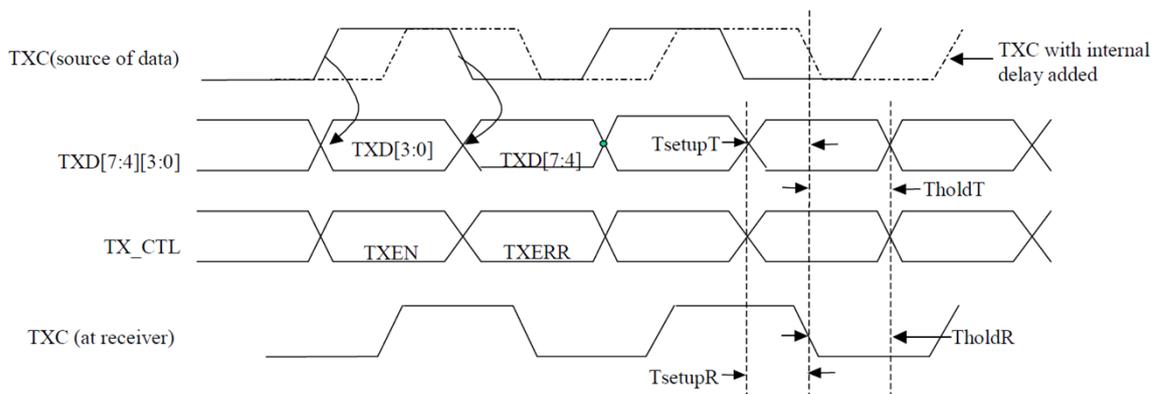
Table 6-36 RGMII Timing Parameters

Parameter	Description	Min	Typical	Max	Unit
Tcyc	Clock Cycle Duration　*note1	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to clock output setup(at Transmitter integrated delay)	1.2	2.0		ns

Parameter	Description	Min	Typical	Max	Unit
TholdT	Data to clock output hold(at Transmitter integrated delay)	1.2	2.0		ns
TsetupR	Data to clock input setup(at Receiver integrated delay)	1.0	2.0		ns
TholdR	Data to clock input hold(at Receiver integrated delay)	1.0	2.0		ns
For 10Mbps and 100Mbps, Tcyc will scale 400ns±40ns and 40ns±4ns.					

6.11.9.2 RMII

Figure 6-37 RMII Receive Timing
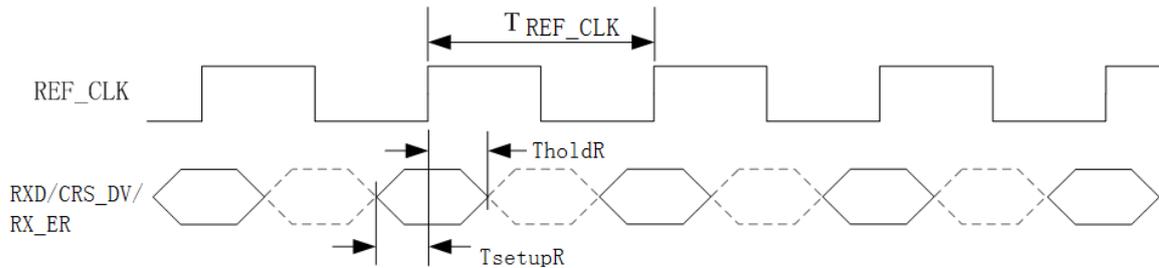
Figure 6-38 RMII Transmit Timing
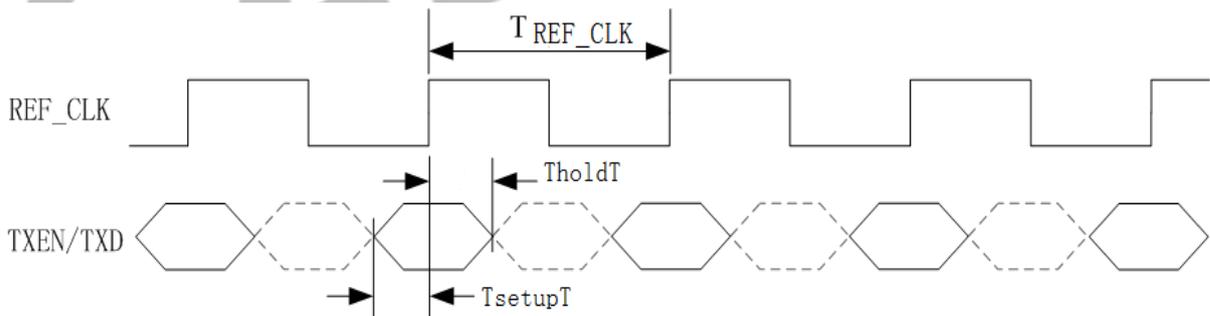
Table 6-37 RMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
T$_{REF\_CLK}$	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

6.11.10 LCD Interface Timing

Figure 6-39 HV_IF Vertical Timing
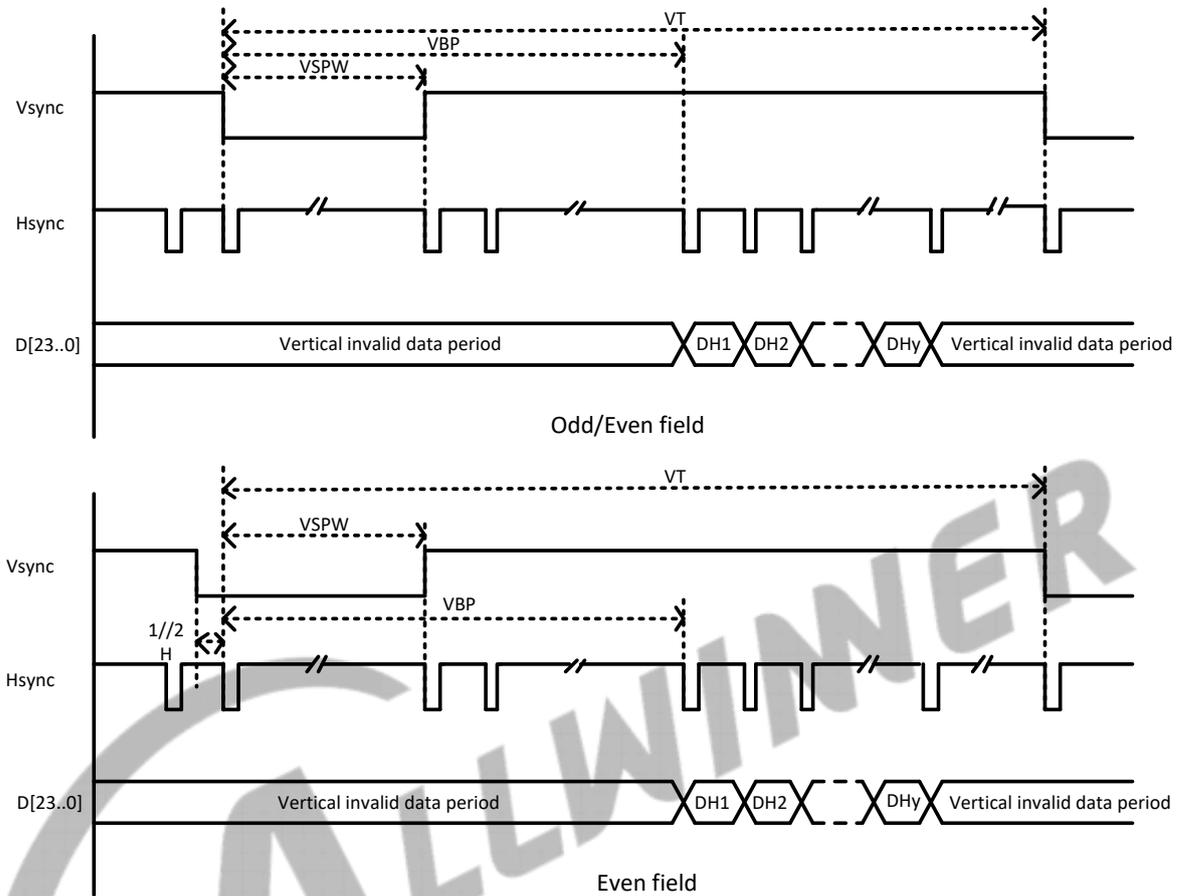
Figure 6-40 HV_IF Horizontal Timing

📖 NOTE

The following timings are illustrated in 320 x 240@60 fps resolution.

Parallel Mode Horizontal Timing:

Serial Mode Horizontal Timing:
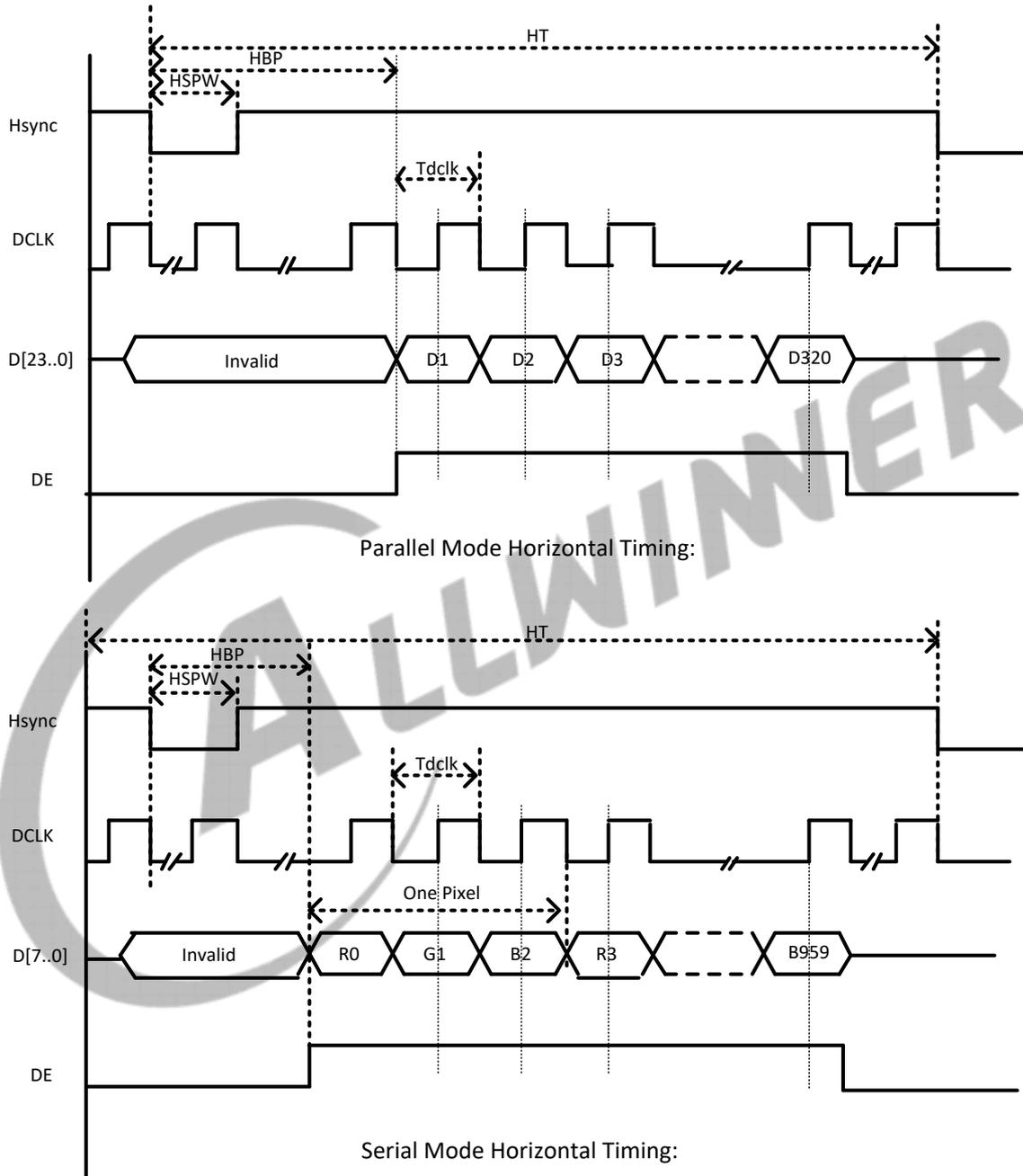
Table 6-38 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK

Parameter	Symbol	Min	Typ	Max	Unit
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT
Vsync Back Porch	tVBP	-	VBP+1	-	tHT

(1) Vsync: Vertical sync, indicates one new frame.

(2) Hsync: Horizontal sync, indicate one new scan line.

(3) DCLK: Dot clock, pixel data are sync by this clock.

(4) DE: LCD data enable.

(5) D[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

6.11.11　MIPI DPHY Interface Timing

Figure 6-41 MIPI DPHY Timing
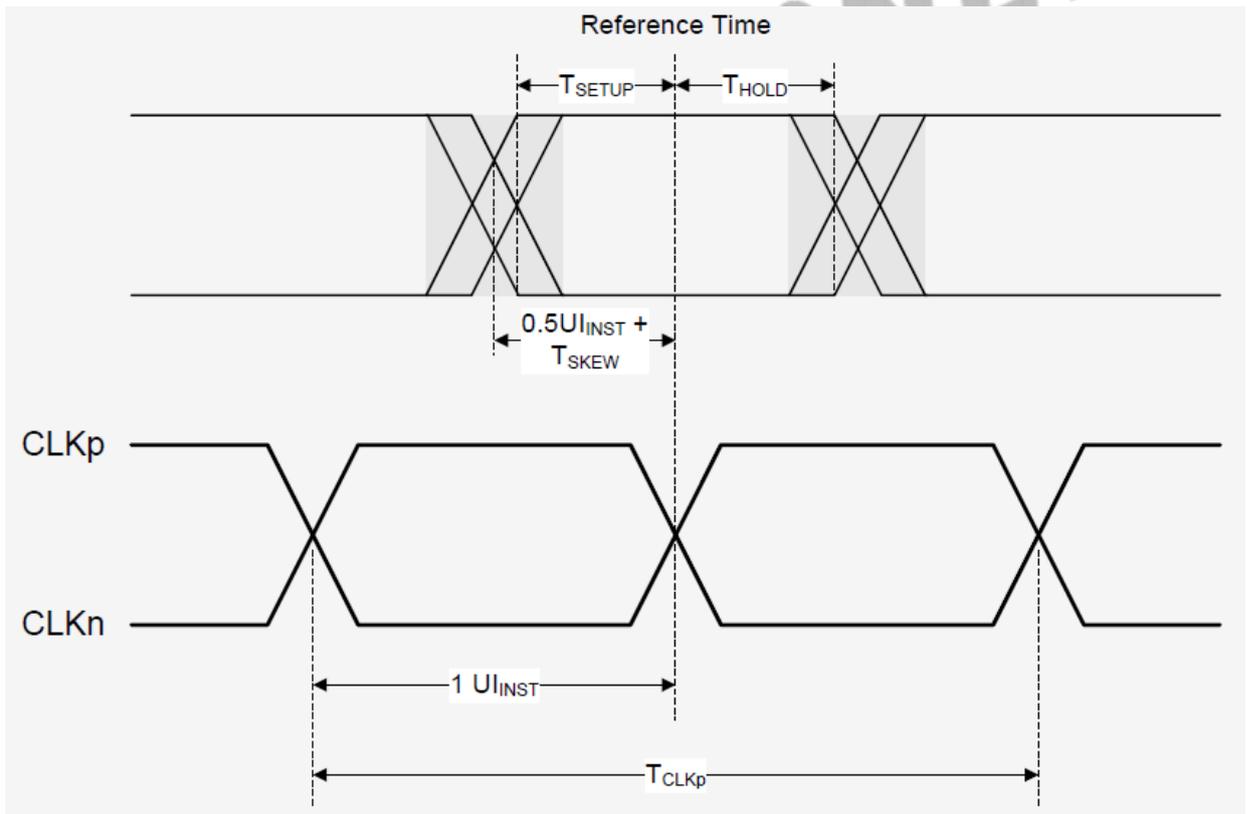
Table 6-39 MIPI DPHY Timing Constants

Parameter	Symbol	Units in UIinst	Operational Frequency in Gbps

		Min	Max	Total	Min	Max
Data to Clock Skew	T_{skew[tx]}	-0.15	0.15	0.3	0.08	1.0
		-0.20	0.20	0.4	>1.0	1.5
Data to Clock Setup Time	T_{setup[rx]}	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5
Clock to Data Hold Time	T_{hold[rx]}	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5

6.11.12 DMIC Interface Timing

Figure 6-42 DMIC Timing
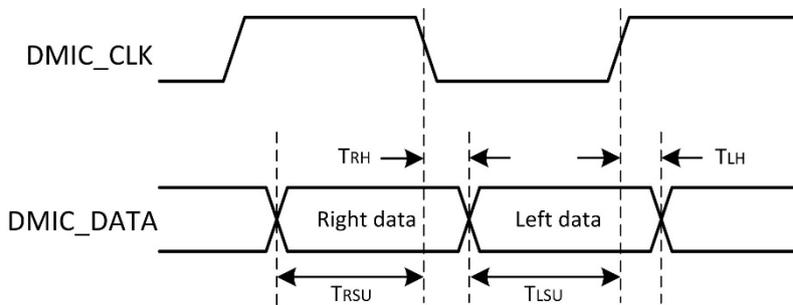
Table 6-40 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) Setup Time to Falling Edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) Hold Time from Falling Edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) Setup Time to Rising Edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) Hold Time From Rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

6.11.13 I2S/PCM Interface Timing

6.11.13.1 Data Output timing of I2S/PCM in Master mode

The Data Output timing of I2S/PCM in Master mode and the Data Input timing of Peripheral I2S/PCM in Slave mode show in Figure 6-43.

Figure 6-43 Data Output Timing of I2S/PCM in Master Mode
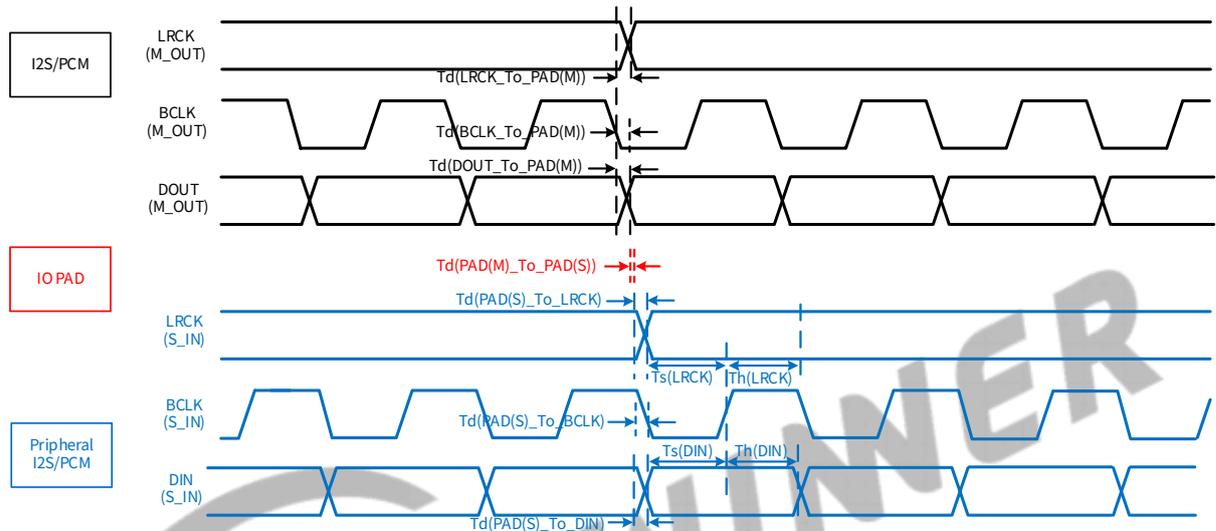
The Data Output timing parameters of I2S/PCM in Master mode and The Data Input timing parameters of Peripheral I2S/PCM in Slave mode show in Table 6-41.

Table 6-41 Data Output Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
T_d(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5 (restriction)	T_w1<2.5(requirement)	ns
T_d(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(restriction)		
T_d(DOUT_To_PAD(M))	DOUT to PAD(M) Delay	/	T3<6.5(restriction)		
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
T_d(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T4*<7.0(estimation)	T_w2*<1.0(requirement)	ns

Parameter		Min	Max	Skew	Units
	BCLK PAD(M) to BCLK PAD(S) Delay	/	T5*<7.0(estimation)		
	DOUT PAD(M) to DIN PAD(S) Delay	/	T6*<7.0(estimation)		
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
T_d(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T7*<6.5(assumption)	T_w3*<2.5(requirement)	ns
T_d(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T8*<6.5(assumption)		
T_d(PAD(S)_To_DIN)	PAD(S) to DIN Delay	/	T9*<6.5(assumption)		
T_s(LRCK)	LRCK Setup Slack	T10*(analysis)	/	/	ns
T_h(LRCK)	LRCK Hold Slack	T11*(analysis)	/	/	ns
T_s(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
T_h(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

6.11.13.2 Data Input timing of I2S/PCM in Master mode

The Data Input timing of I2S/PCM in Master mode and the Data Output timing of Peripheral I2S/PCM in Slave mode show in Figure 6-44.

Figure 6-44 Data Input Timing of I2S/PCM in Master Mode
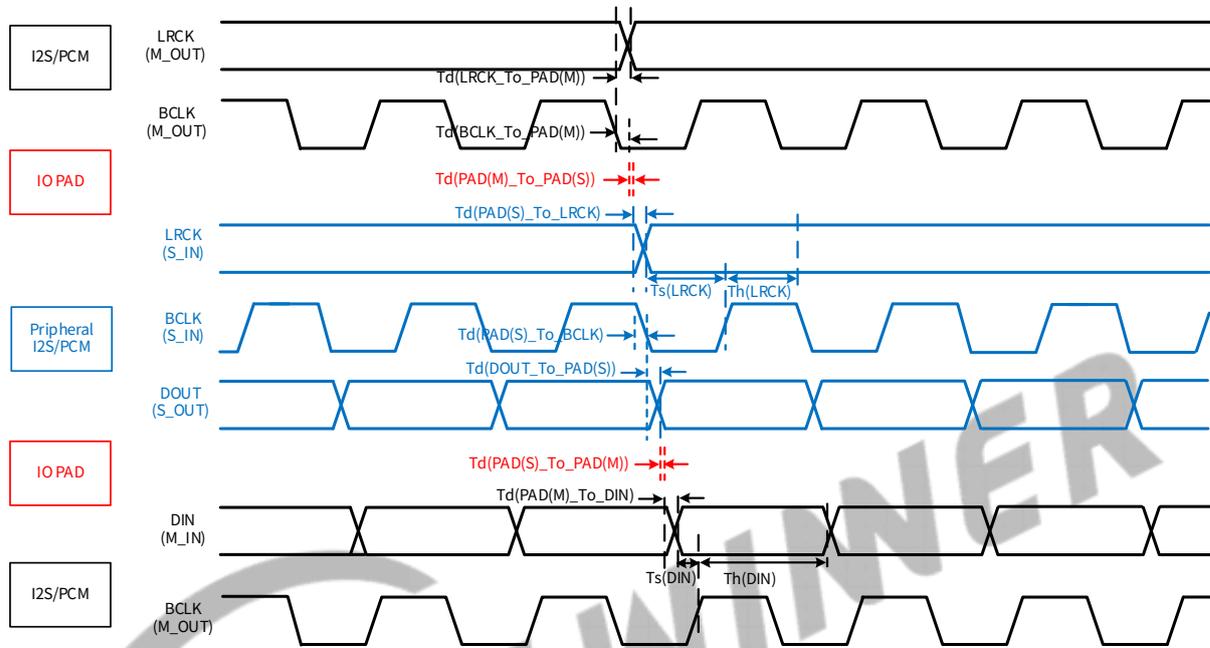
The Data Input timing parameters of I2S/PCM in Master mode and The Data Output timing parameters of Peripheral I2S/PCM in Slave mode are shown in Table 6-42.

Table 6-42 Data Input Timing Parameters of I2S/PCM in Master Mode

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(LRCK_To_PAD(M))	LRCK to PAD(M) Delay	/	T1<6.5(requirement)	Tw1<2.5 (estimation)	ns
Td(BCLK_To_PAD(M))	BCLK to PAD(M) Delay	/	T2<6.5(requirement)		ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(M)_To_PAD(S))	LRCK PAD(M) to LRCK PAD(S) Delay	/	T3*<7.0(requirement)	Tw2*<1.0 (estimation)	ns
	BCLK PAD(M) to BCLK PAD(S) Delay		T4*<7.0(requirement)		

Parameter		Min	Max	Skew	Units
Sequence requirement of internal signal of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_LRCK)	PAD(S) to LRCK Delay	/	T5*<6.5(requirement)	Tw3*<2.5 (estimation)	ns
Td(PAD(S)_To_BCLK)	PAD(S) to BCLK Delay	/	T6*<6.5(requirement)		ns
Td(DOUT_To_PAD(S))	DOUT to PAD(S) Delay	/	T7*<6.5(requirement)	/	ns
Ts(LRCK)	LRCK Setup Slack	T8*(analysis)	/	/	ns
Th(LRCK)	LRCK Hold Slack	T9*(analysis)	/	/	ns
Sequence requirement of the IO pad of I2S/PCM in Master mode connecting to the external IO pad of Peripheral I2S/PCM in Slave mode					
Td(PAD(S)_To_PAD(M))	DOUT PAD(S) to DIN PAD(M) Delay	/	T10*<7.0(requirement)	/	ns
Sequence requirement of internal signal of I2S/PCM in Master mode					
Td(PAD(M)_To_DIN)	PAD(M) to DIN Delay	/	T11<6.5(requirement)	/	ns
Ts(DIN)	DIN Setup Slack	T12*(analysis)	/	/	ns
Th(DIN)	DIN Hold Slack	T13*(analysis)	/	/	ns

6.11.14 OWA Interface Timing

Figure 6-45 OWA Timing
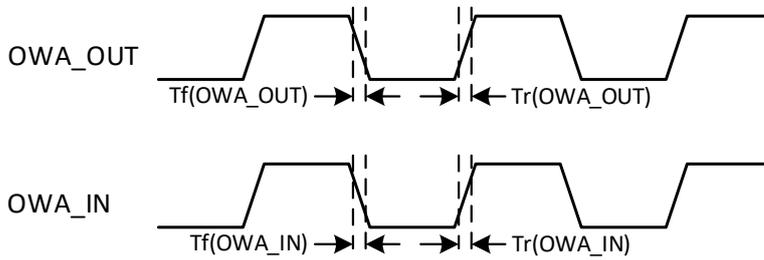
Table 6-43 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT Fall Time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN Rise Time	Tr(OWA_IN)	-	-	4	ns
OWA_IN Fall Time	Tf(OWA_IN)	-	-	4	ns

6.12 Power-On and Power-Off Sequence

📖 **NOTE**

- All Tn markers represent different steps during power-on and power-off process and show the minimum time interval between current step and previous step.
- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90%-110% of their nominal voltage, unless stated otherwise.
- Different power rails at the same step should become stable within 1ms.

6.12.1 Power-On Sequence

The following figure shows an example of the power-on sequence for the T527 device. The description of the power-on sequence is as follows:

- VCC-LVDS0 must be ramped before VCC-PD.
- VCC-MCSI must be ramped before 3.3 V VCC-PK. (There is no power-on step requirement for the 1.8 V VCC-PK.)
- VCC-EFUSE must be ramped after VDD-SYS.
- VCC-LVDS1 must be ramped before VCC-PJ.

- During the entire power on sequence, the reset signal must be held on low until all other power rails (except 24 MHz CLK) are stable for at least 6 ms.
- The 24MHz clock starts oscillating and be stable within 4 ms after the reset signal is stable.

Figure 6-46 Power-on Timing
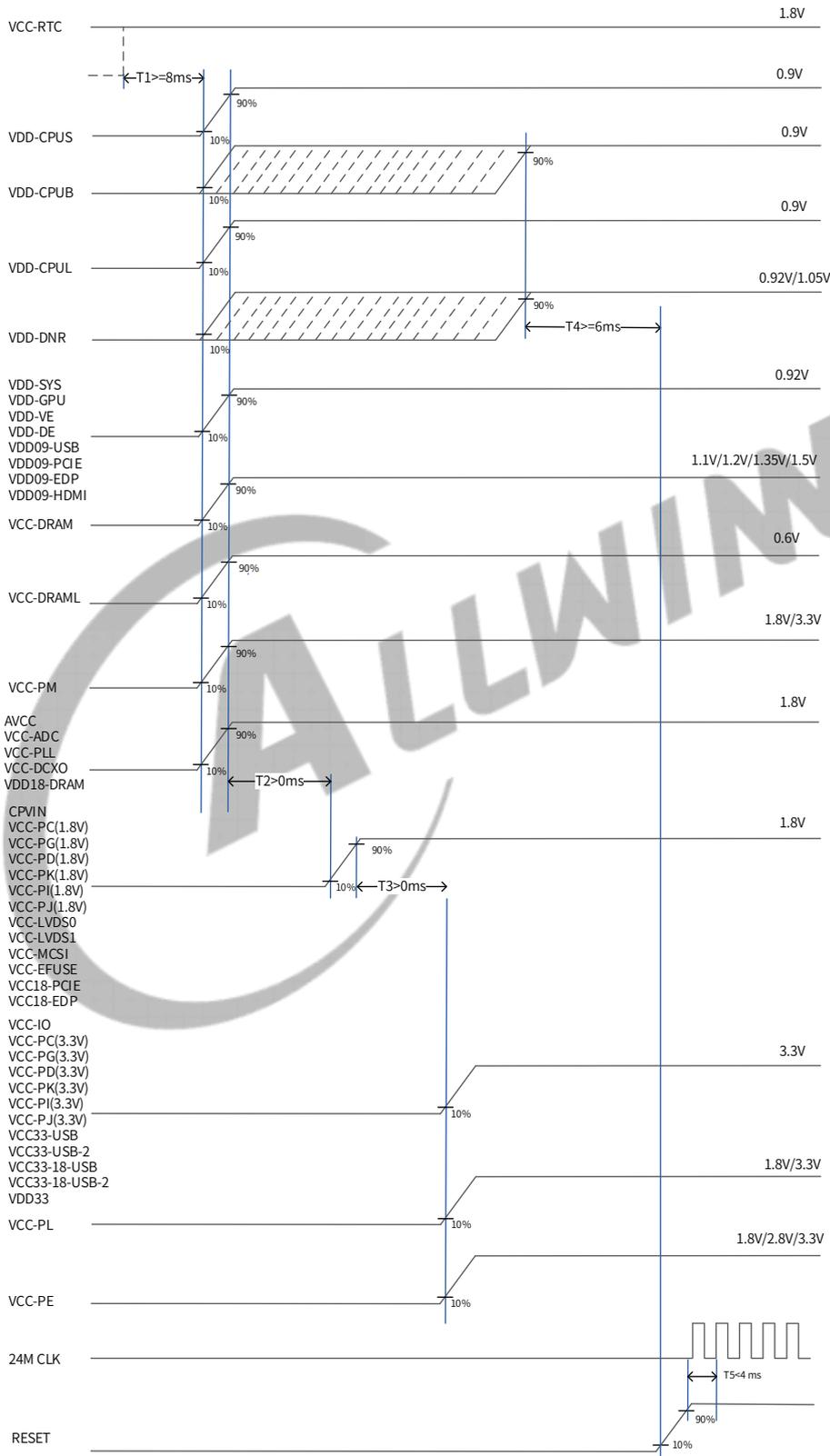
6.12.2　Power-Off Sequence

The following steps give an example of the power off sequence supported by the T527 device. The following figure shows an example of the device power off sequence.

- Reset T527 device. After PMIC receives the power-down command, pull-down RESET.

- VCC-RTC holds high.

- After RESET ramps down, other powers start to ramp down, and the ramp rate of each power rail is generally determined by the load on that power.

Figure 6-47 Power-off Timing
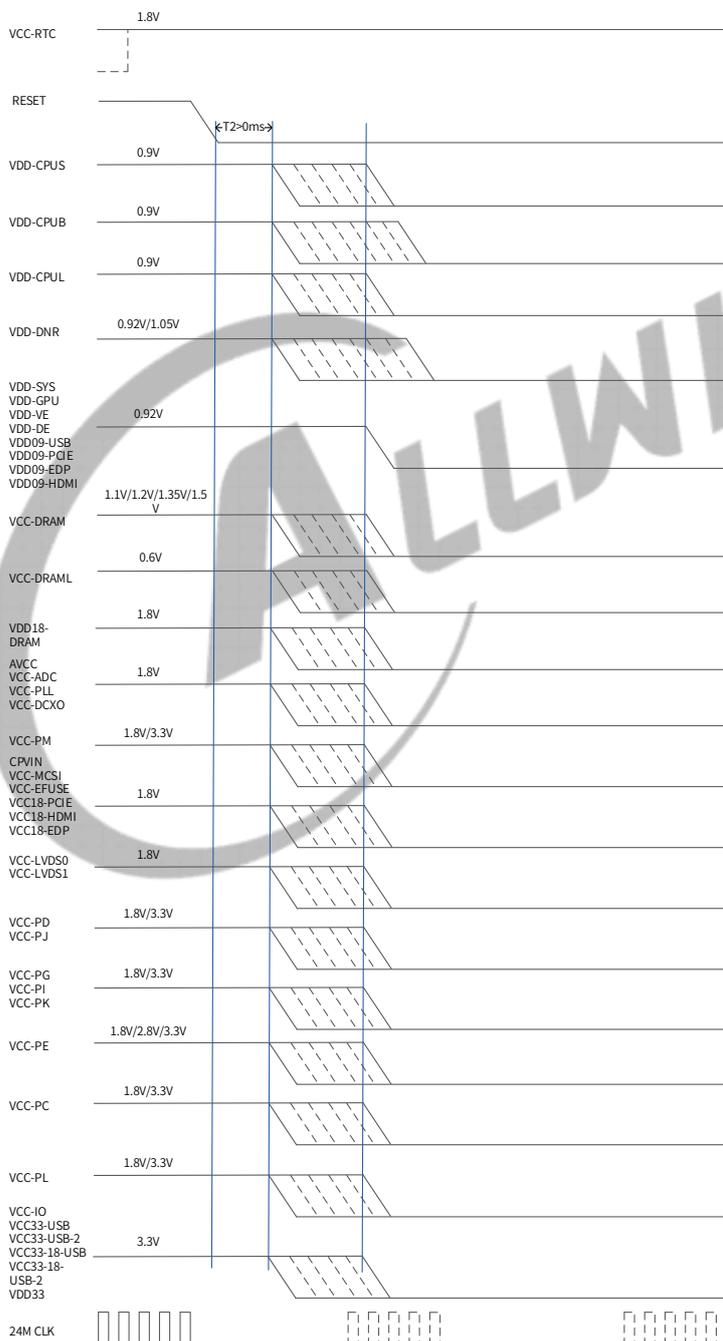
7 Temperature and Thermal Characteristics

7.1 Temperature

The following tables describe the temperature of T527.

Table 7-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
Ta	Ambient Operating Temperature	-40	85	°C
T_{STG}	Storage Temperature	-40	150	°C

Table 7-2 Junction Temperature

Chip	Working junction temperature (Tj)		Destructive Junction Temperature[2]	Unit
	Min	Max[1]		
T527	-40	115	125	°C

(1) The junction temperature of the chip should be less than or equal to this value under normal operating conditions.

(2) The junction temperature of chip should not be more than this value under any conditions.

7.2 Package Thermal Characteristics

The maximum chip junction temperature (T_J max) must never exceed the values given in Table 7-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the T527. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 7-3 T527 Package Thermal Characteristics

Symbol	Parameter	Min	Typ[1][2]	Max	Unit

Symbol	Parameter	Min	Typ[1][2]	Max	Unit
θ$_{JA}$	Junction-to-Ambient Thermal Resistance	-	19.27	-	°C/W
θ$_{JB}$	Junction-to-Board Thermal Resistance	-	6.48	-	°C/W
θ$_{JC}$	Junction-to-Case Thermal Resistance	-	0.2	-	°C/W

(1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions (b)Natural Convection (Still Air). Available from www.jedec.org.

(2) The testing PCB is 4 layers, 114.3 mm x 76.2 mm body, and 1.6mm thickness. Ambient temperature is 25 °C.

8 Pin Assignment

8.1 Pin Map

For T527, HS-FCBGA 664 balls, 17 mm x 17 mm, 0.5 mm ball pitch, 0.3 mm ball size package is offered. The following figure shows the pin map of the T527.

Figure 8-1 T527 Pin Map

8.2   Package Dimension

The following figure shows the top, bottom, and side views of T527 package dimension.

Figure 8-2 T527 Package Dimension
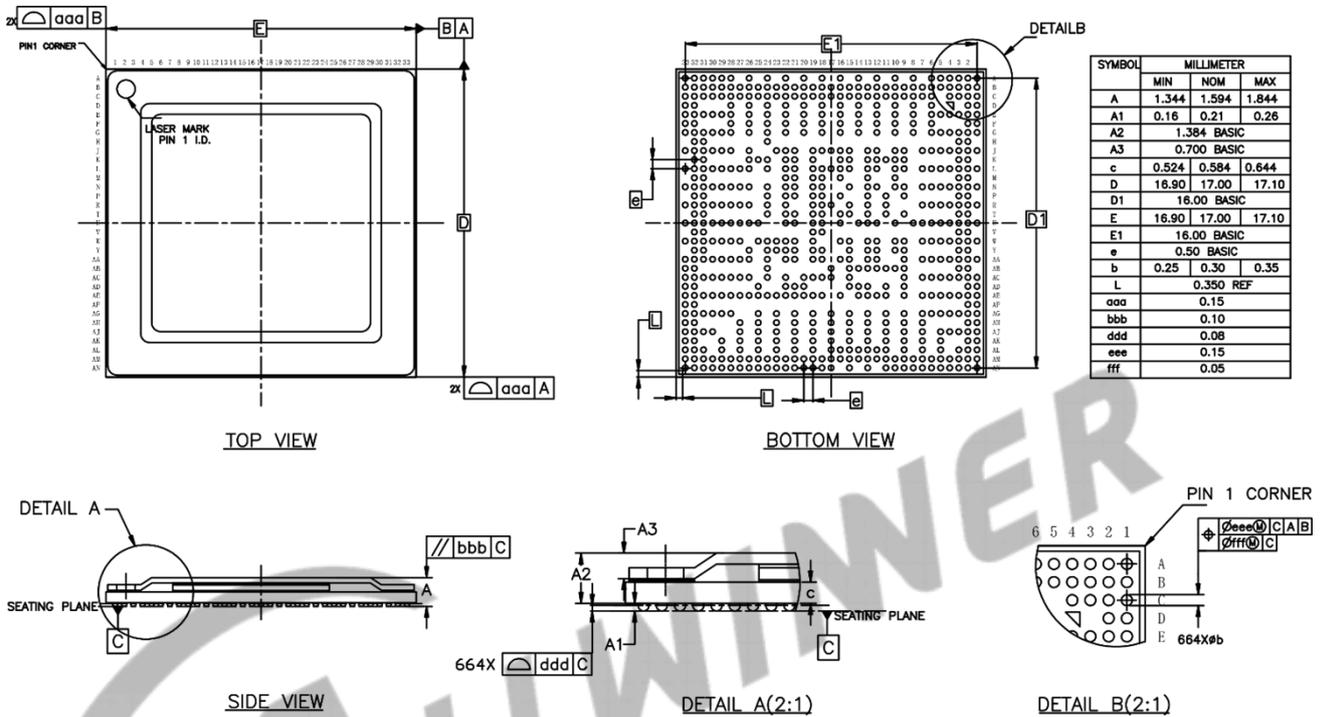
9 Carrier, Storage and Backing Information

9.1 Carrier

The following table shows the T527 matrix tray carrier information.

Table 9-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 135.9 mm x 7.62 mm	90 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

The following table shows the T527 packing quantity.

Table 9-2 T527 Packing Quantity Information

Sample	Size (mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
T527	17 x 17	90	10	900	6	5400

The following figure shows tray dimension drawing of the T527.

Figure 9-1 T527 Tray Dimension Drawing
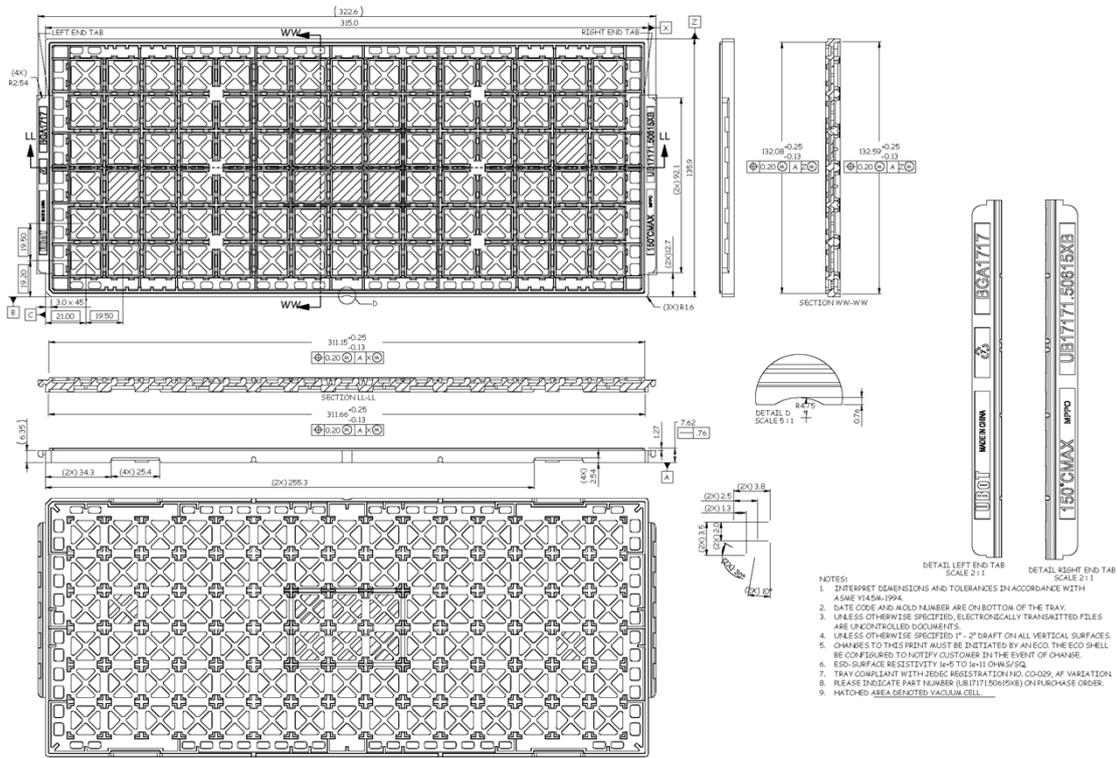
9.2 Storage

Reliability is affected if any condition specified in Section 9.2.2 and Section 9.2.3 has been exceeded.

9.2.1 Moisture Sensitivity Level (MSL)

A package s MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 9-3 defines all MSL.

Table 9-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	30°C / 85%RH
2	1 year	30°C / 60%RH
2a	4 weeks	30°C / 60%RH
3	168 hours	30°C / 60%RH
4	72 hours	30°C / 60%RH
5	48 hours	30°C / 60%RH
5a	24 hours	30°C / 60%RH
6	Time on Label (TOL)	30°C / 60%RH

📖 NOTE

The T527 device samples are classified as MSL3.

9.2.2 Bagged Storage Conditions

The following table defines the shelf life of the T527 device samples.

Table 9-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20(b26°C
Storage humidity	40%(b60%RH
Shelf life	12 months

9.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of the T527 is as follows.

Table 9-5 Out-of-bag Duration

Storage temperature	20(±6°C
Storage humidity	40%(±60%RH
Moisture sensitive level (MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

9.3 Baking

It is not necessary to bake the T527 if the conditions specified in Section 9.2.2 and Section 9.2.3 have not been exceeded. It is necessary to bake the T527 if any condition specified in Section 9.2.2 and Section 9.2.3 has been exceeded.

It is necessary to bake the T527 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 time due to a risk of deformation.
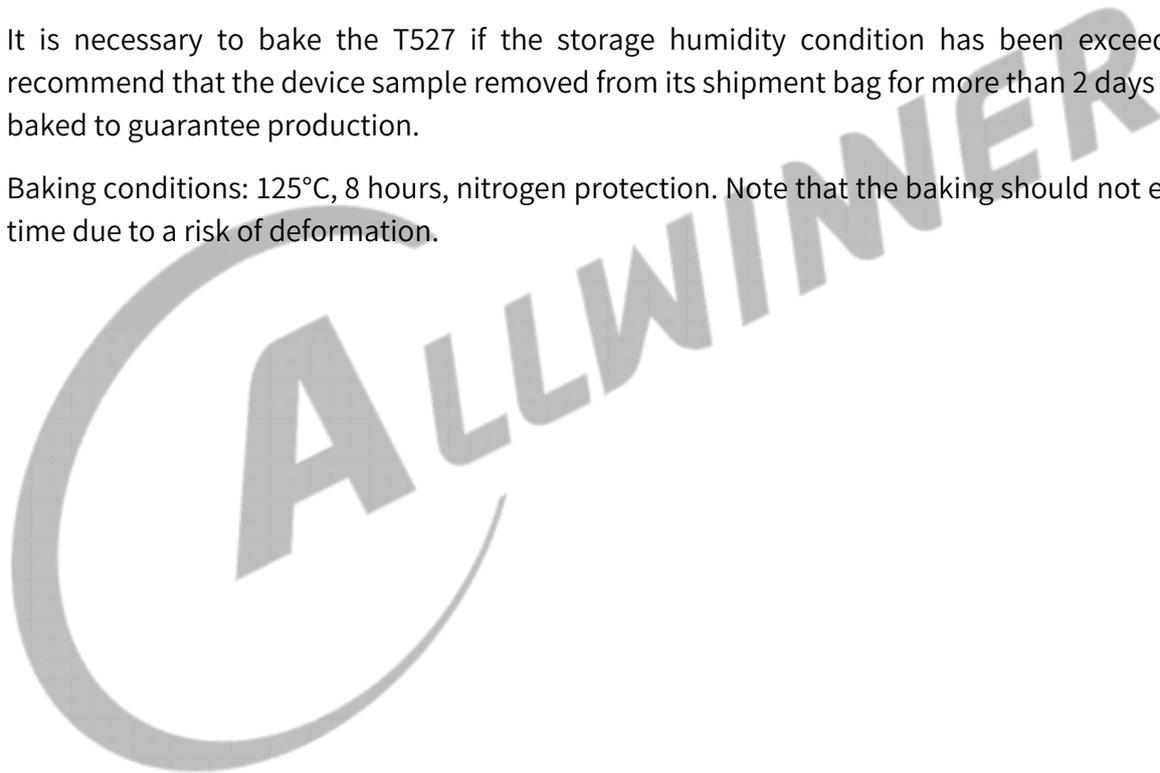
10 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 10-1 Lead-free Reflow Profile
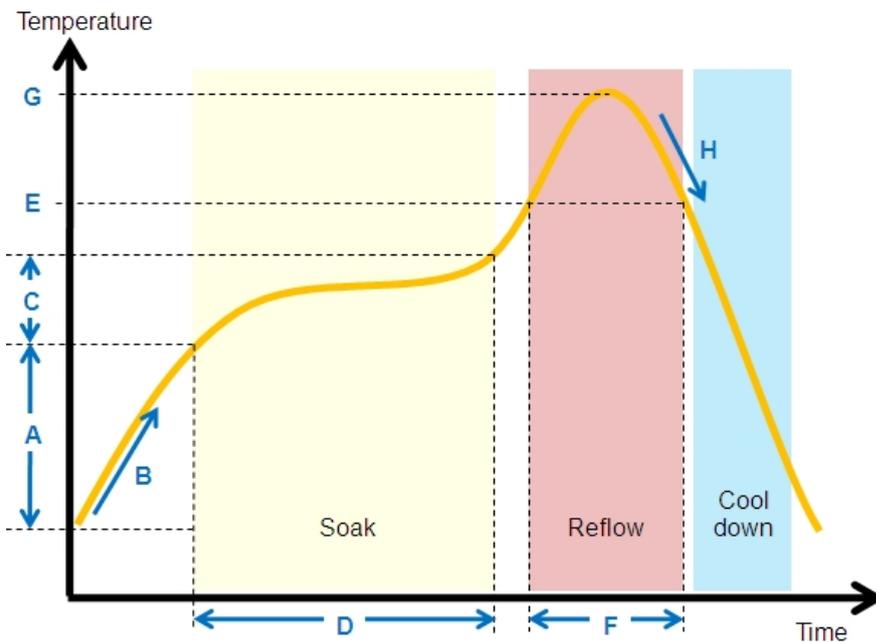
Table 10-1 Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5(b)2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80(b)110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60(b)90 s
G	Peak temperature	240(b)250 °C
H	Cool down temperature rate	4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 10-2.

Figure 10-2 Measuring the Reflow Soldering Process
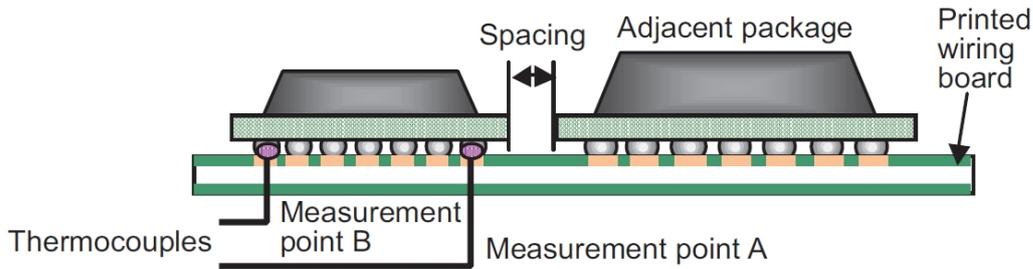
> **NOTE**
>
> To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

11 FT/QA/QC Test

11.1 FT Test

FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.

11.2 QA Test

QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

11.3 QC Test

QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

12 Part Marking

12.1 T527M02X0DCH

The following figure shows the T527M02X0DCH marking.

Figure 12-1 T527M02X0DCH Marking

The following table describes the T527M02X0DCHmarking definitions.

Table 12-1 T527M02X0DCH Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T527M02X0DCH	Product name	Fixed
3	LLLLLCA	Lot number	Dynamic
4	XXXF	Date code	Dynamic

12.2 T527M00X0DCH

The following figure shows the T527M00X0DCH marking.

Figure 12-2 T527M00X0DCH Marking
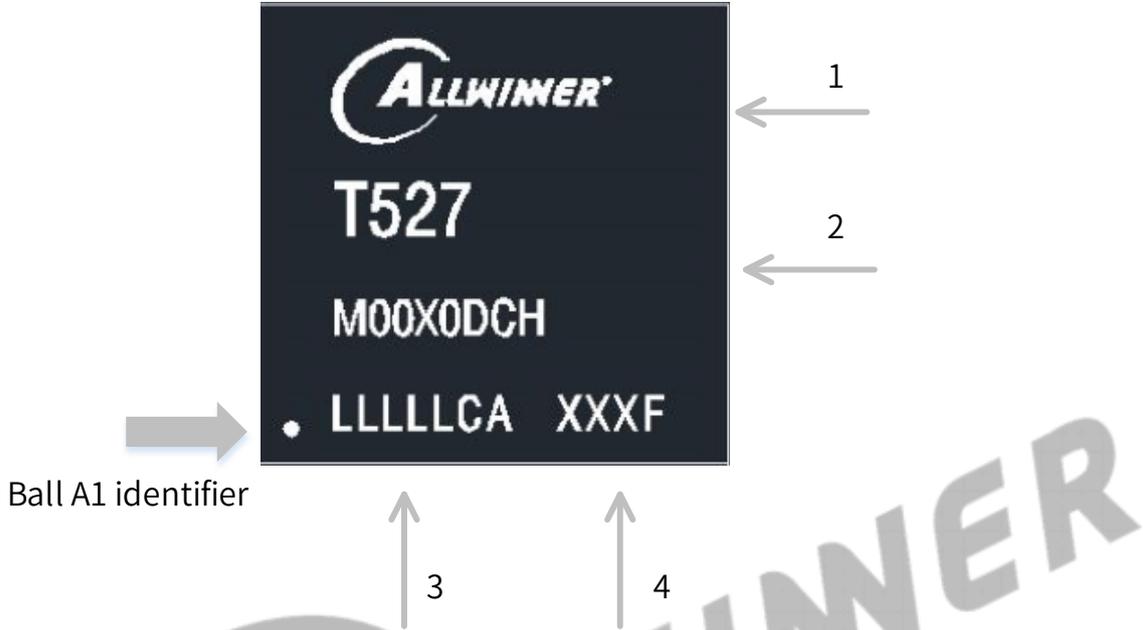
The following table describes the T527M00X0DCH marking definitions.

Table 12-2 T527M00X0DCH Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T527M00X0DCH	Product name	Fixed
3	LLLLLCA	Lot number	Dynamic
4	XXXF	Date code	Dynamic

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