A63 Datasheet

High Performance 64-bit Quad-Core Tablet Solution

Revision 1.0

Oct.23,2017

Revision History

Revision	Date	Description
1.0	Oct.23,2017	First Release Version

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About This Documentation

Purpose

The documentation describes features of each module, pin/signal characteristics, current consumption, the interface timing, thermal and package of the A63 processor. For details about register descriptions of each module, see the *A63 User Manual.pdf*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1. Overview

Allwinner's A63 is a quad-core,64-bit SoC targeted for high performance tablets. The A63 integrates a higher energy efficiency ARM Cortex™-A53 CPU architecture, and also includes advanced graphics computing processor MaliT760MP2, high-definition video decoding/encoding, low power audio codec, excellent display controllers and a broad range of interfaces.

The A63 supports H.265 high-definition hardware video decoding by 4K@30fps ,and mainstream high-definition video decoding including H.264 by 4K@30fps, VP9 by 4K@30fps, MPEG1/2/4 by 1080p@60fps, AVS/AVS+ by 1080p@60fps, VC1 by 1080p@60fps,etc. In the aspect of video encoding, the A63 supports 1080p@30fps H.264 encoding ability.

Integrated analog Audio Codec supports 20bit/192kHz audio playback to deliver high quality sound, also digital audio interfaces support I2S/PCM for connecting to an external audio codec . The A63 supports Allwinner's new-generation SmartColor3.0 technology and various display output interfaces, content can be displayed by 8-lane MIPI DSI up to 2560x1600@60fps, or by eDP panel up to 2560x1600@60fps. It provides end users with an enhanced visual entertainment experience.

The A63 supports many types of external memory devices, including DDR2/DDR3/DDR3L/LPDDR2/LPDDR3, NAND Flash with full disk encryption, SD/SDIO/MMC including eMMC up to rev5.0.

Security functions are enabled and accelerated by hardware crypto engine, secure boot, secure JTAG and secure efuse. To deliver better architecture scalability, the A63 comes with extensive connectivity and interfaces, such as CSI, USB OTG/Host, SPI, UART, TWI.

2. Features

2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 Processor
- Power-efficient ARM v8 architecture
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced SIMD(Single Instruction Multiple Data)instruction for acceleration of media and signal processing functions
- Supports Large Physical Address Extensions(LPAE)
- VFPv4 Floating Point Unit
- 32KB L1 Instruction cache and 32KB L1 Data cache per core
- 512KB L2 cache shared

2.2. GPU Architecture

- MaliT760MP2
- Supports OpenGL ES 3.2/3.1/3.0/2.0/1.1, Direct3D 11.1, OpenCL 1.2/1.1 and Renderscript standard

2.3. Memory Subsystem

2.3.1. Boot ROM

- On-chip memory
- Supports system boot from the following devices:
  - NAND Flash
  - SD card
  - eMMC
  - SPI Nor Flash
- Supports secure boot and normal boot
- Supports one key USB mass production upgrade
- Supports system code download through USB OTG and card
- Supports boot media priority sequence through boot select pin and efuse

2.3.2. SDRAM

- Compatible with JEDEC standard DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Supports clock frequency up to 933MHz for DDR3/DDR3L
- Supports clock frequency up to 933MHz for LPDDR3
- Supports clock frequency up to 533MHz for LPDDR2
- Supports clock frequency up to 400MHz for DDR2
- Supports 2 chip selects
- Up to 3GB address space
- 32-bit bus width
- 16 address signal lines and 3 bank signal lines
- Supports Memory Dynamic Frequency Scale(MDFS)

2.3.3. NAND Flash

- 8-bit data bus width
- Supports 2 CE signals and 2 RB signals
- Up to 80-bit ECC per 1024 bytes
- Supports 1024,2048,4096,8192,16384,32768 bytes size per page
- Supports SLC/MLC/TLC flash and EF-NAND memory
- Supports SDR,ONFI DDR and Toggle DDR NAND
- Supports full disk encryption(FDE) function
- Embedded DMA to do data transfer
- Supports data transfer together with normal DMA

2.3.4. SD/MMC

- Up to 3 SD/MMC host controller(SMHC) interfaces
- SMHC0 controls the device that comply with the Secure Digital Memory(SD3.0)
  - 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output(SDIO3.0)
  - 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 50MHz@1.8V IO pad
- SMHC2 controls the devices that comply with the MultiMediaCard(MMC5.1)
  - 8-bit bus width
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 100MHz@1.8V IO pad
  - DDR mode 50MHz@3.3V IO pad
- SMHC2 supports full disk encryption(FDE) function
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.4. System Peripheral

2.4.1. Timer

- The timer module implements the timing and counting functions, which includes Timer0 and Timer1,Watchdog, AVS and 64-bit counter
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factor
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode
  - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transimitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing
- 2 AVS counters(AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime
  - 12-bit frequency divider factor
  - Pause/Start function
- One 64-bit Counter to count timing for GPU

- Supports clear zero function
- Performs latch operation once before getting the current counter value

2.4.2. High Speed Timer

- One high speed timer with 56-bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers

2.4.3. RTC

- Calendar :Counters second,minute,hour,day,week,month and year with leap year generator
- Alarm: general alarm and weekly alarm
- Multi clock sources: 24MHz crystal, 16MHz RC clock, 32768Hz crystal clock
- One 32768Hz fanout

2.4.4. GIC

- Supports 16 Software Generated Interrupts(SGIs), 16 Private Peripheral Interrupts(PPIs) and 147 Shared Peripheral Interrupts(SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization
- Uniprocessor and multiprocessor environments
- ARM architecture security extensions
- ARM architecture virtualization extensions
- Wakeup events in power-management environments

2.4.5. DMA

- Up to 12-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.4.6. CCU

- 11 PLLs
- One on-chip RC oscillator
- Supports one external 24 MHz oscillator and one external 32.768 kHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.4.7. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE0/2, VE_R, VE, CSI, VP9 parallel address mapping
- Supports DE0/2, VE_R, VE, CSI, VP9 bypass function independently
- Supports DE0/2,VE_R,VE,CSI,VP9 prefetch independently

- Supports DE0/2,VE_R,VE,CSI,VP9 interrupt handing mechanism independently
- Supports level1 and level2 TLB for special using, and level2 TLB for sharing
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission
- Performance: Average (L1+L2)TLB Hit rate: up to 99.9%, Average Latency: 5±1cycle

2.4.8. GPADC

- SAR analog-to-digital converter with 12-bit resolution
- Maximum sampling frequency up to 1 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode

2.4.9. PWM

- Up to two PWM channels
- Supports two kinds of outputting waveform: continuous waveform and single pulse waveform
- 0% to 100% adjustable duty cycle
- Up to 24MHz output frequency
- The minimum resolution is 1/65536

2.4.10. Thermal Sensor

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Three sensors:sensor0 for GPU,sensor1 for VE,sensor2 for CPU

2.4.11. Crypto Engine(CE)

- Supports Symmetrical algorithm: AES,DES,TDES,XTS
  - Supports ECB,CBC,CTS,CTR,CFB,OFB,CBC-MAC mode for AES
  - Supports 128/192/256-bit key for AES
  - Supports ECB,CBC,CTR,CBC-MAC mode for DES/TDES
  - Supports 256/512-bit key for XTS
- Supports Hash algorithm: MD5,SHA,HMAC
  - Supports SHA1,SHA224,SHA384,SHA512 for SHA
  - Supports HMAC-SHA1,HMAC-SHA256 for HMAC
  - MD5,SHA,HMAC are padded using hardware
- Supports Asymmetrical algorithm: RSA, ECC
  - RSA supports 512/1024/2048/4096-bit width
  - ECC Supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Internal Embedded DMA to do data transfer
- Supports secure and non-secure interfaces respectively
- Supports task chain mode for each request. Task or task chain are executed at request order
- 8 scatter group(sg) are supported for both input and output data
- DMA has multiple channels, each corresponding to one suit of algorithms

2.4.12. Embedded Crypto Engine(EMCE)

- Connects directly to SMHC or NDFC for disc encryption application
- Supports AES algorithm

- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports ECB, CBC, XTS modes

2.4.13. Security ID

- Supports 2.5K-bit EFUSE for chip ID and security application

2.4.14. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control, CP15 control, and power control, etc
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc

2.4.15. Message Box

- Provides interrupt communication mechanism for on-chip processor
- Two users for Message Box: user0 for CPUS, user1 for CPUX
- Each of Queue has a 4x32-bit FIFO for eight Message Queues
- Each of Queue could be configured as transmitter or receiver

2.5. Display Subsystem

2.5.1. DE3.0

- Output size up to 2560x1600
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports AFBC buffer in main display
- Supports input format semi-planar of YUV422/YUV420/YUV411 and planar of YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor 3.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
  - Content adaptive backlight control
- Supports writeback and rotation for high efficient dual display and miracast

2.5.2. Display Output

- Supports 2-channel MIPI DSI output, each MIPI DSI is 4-lane
  - Single channel(4-lane) MIPI DSI with up to 1920x1080@60fps or 1440x1440@60fps resolution
  - Dual channel(8-lane) MIPI DSI with up to 2560x1600@60fps resolution
- Supports eDP output
  - Compliant with eDP V1.2 protocol
  - Up to 2560x1600@60fps resolution
  - Configurable of 1/2/4 lane mode

2.6. Video Engine

2.6.1. Video Decoder

- Supports multi-format video decoder, include:
  - H.265 Main/L5.0: 4K@30fps
  - H.264 BP/MP/HP Level4.2: 4K@30fps
  - H.263 BP: 1080p@60fps
  - MPEG1 MP/HL: 1080p@60fps
  - MPEG2 MP/HL: 1080p@60fps
  - MPEG4 SP/ASP L5: 1080p@60fps
  - Sorenson Spark : 1080p@60fps
  - VP8: 1080p@60fps
  - VP9 Profile 0: 4K@30fps
  - VC1 SP/MP/AP: 1080p@60fps
  - AVS-P2/AVS-P16(AVS+) jizhun: 1080p@60fps
  - xvid: 1080p@60fps
- Supports 1080p blu-ray 3D
- Supports 3D size:3840x1080,1920x2160
- Supports decoding output formats: T32 x 32, YV12, NV12, NV21

2.6.2. Video Encoder

- Supports H.264 video encoder up to 1080p@30fps
- JPEG baseline: picture size up to 4096x4096
- Supports input formats: YU12/YV12/NV12/NV21/YUYV/YVYU/UYVY/VYUY/ARGB/BGRA/RGBA/ABGR/YU16/YV16/TILE32/TILE128
- Supports Alpha blending
- Supports thumb generation
- Supports 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Supports rotated input

2.7. Image In

2.7.1. CSI

- Supports 8/10-bit digital camera interface
- Supports BT656 interface
- Supports ITU-R BT.656 time-multiplexed format
- Maximum still capture resolution for parallel interface to 5M
- Maximum video capture resolution for parallel interface to 1080p@30fps
- Maximum pixel clock for parallel to 148.5MHz

2.8. Audio Subsystem

2.8.1. Audio Codec

- Two audio digital-to-analog(DAC) channels
  - 20-bit sample resolution
  - 8 kHz to 192 kHz sample rate
  - 95±3dB SNR@A-weight, THD+N-80±3dB, output level 0.56Vrms
  - DAC power consumption 3.1mA@1.8V
- Three audio outputs:
  - One differential Speaker output
  - One Headphone amplifier L/R channel output
  - One Line-out L/R output
- Capless stereo headphone driver

  - Headphone driver 10mW(CPVDD=0.9V,16Ω load)
  - 95±3dB SNR@A-weight, THD+N-77±3dB, output level 0.4Vrms@16Ω
  - Headphone power consumption 2.4mA@1.8V(AVCC),100mA@0.9V(CPVDD)
- Two audio analog-to-digital(ADC) channels
  - 20-bit sample resolution
  - 8 kHz to 48 kHz sample rate
  - 90±3dB SNR@A-weight, THD+N-77±3dB
  - ADC power consumption 5.5mA@1.8V
- Five audio inputs:
  - Three differential microphone inputs
  - One mono differential Phone input
  - One stereo Line-in L/R input
- Supports analog/digital volume control
- Analog low-power loop from line-in/microphone to headphone/lineout/speaker outputs
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- Supports Dynamic Range Control(DRC) adjusting the ADC recording output
- Two low-noise analog microphone bias outputs
- Supports analog/digital volume control
- Accessory button press detection
- Two I2S/PCM interfaces
- One 128x24 bits FIFO for data transmit, one 64x24 bits FIFO for data receive
- Programmable FIFO thresholds

2.8.2. I2S/PCM

- Up to 3 I2S/PCM controllers
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Supports full-duplex synchronous work mode
- Supports master/slave mode
- Supports clock up to 24.576MHz
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8 kHz to 384 kHz(channels =2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds

2.8.3. DMIC

- Up to 8 channels
- Supports maximum 8 digital microphones
- Supports sample rate from 8 kHz to 48 kHz

2.9. External Peripherals

2.9.1. USB

- One USB 2.0 OTG, with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) and Low-Speed(LS,1.5 Mbit/s) in host mode
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) in device mode
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
  - Up to 10 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1,

Endpoint2, Endpoint3, Endpoint4, Endpoint5)
- Supports (8KB+64Bytes) FIFO for EPs(including EP0)
- Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode

- One USB2.0 Host, with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS,480 Mbit/s),Full-Speed(FS,12 Mbit/s) and Low-Speed(LS,1.5 Mbit/s) device

2.9.2. UART

- Up to 5 UART controllers
- Two of 5 UART controllers support 2-wire while others support 4-wire
- Compatible with industry-standard 16550 UARTs
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.9.3. SPI

- Up to 3 SPI controllers
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Support 3-wire/4-wire SPI
- Support programmable serial data frame length: 0bit to 32bits
- Support Standard SPI,Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI

2.9.4. Two Wire Interface(TWI)

- Up to 8 TWI(Two Wire Interface) controllers
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency

2.9.5. RSB™

- Designed and implemented by the Allwinner Technology
- Up to 20MHz speed with ultra low power
- Supports push-pull bus
- Supports host mode and multi-devices
- Programmable output delay of CD signal
- Supports parity check for address and data transmission

2.10. Package

- FBGA463 balls, 0.65mm ball pitch, 15mm x 15mm

3. Block Diagram

Figure 3-1 shows the block diagram of the A63.

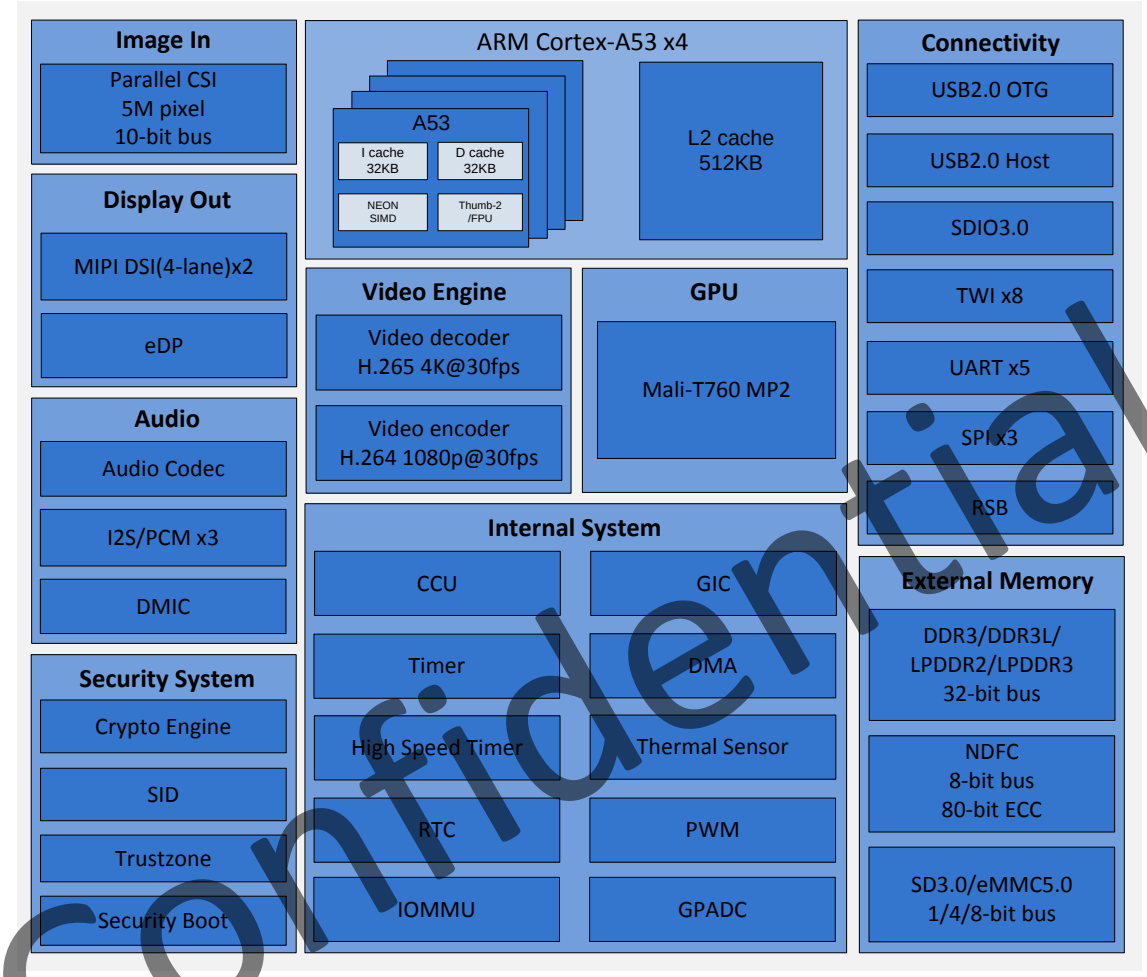


Figure 3-1. A63 Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of A63 pins from the following ten aspects.

(1).**Ball#** : Package ball numbers associated with each signals.

(2).**Pin Name** : The name of the package pin.

(3).**Signal Name** : The signal name for that pin in the mode being used.

(4).**Function** : Multiplexing function number.

(5).**Ball Reset Rel. Function** : The function is automatically configured after RESET from low to high.

(6).**Type** : Denotes the signal direction

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
P (Power),
G (Ground)

(7).**Ball Reset State** : The state of the terminal at reset.

(8).**Pull Up/Down** : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

(9).**Buffer Strength** : Defines drive strength of the associated output buffer.

(10).**Power Supply** : The voltage supply for the terminal's IO buffers.

Table 4-1. Pin Characteristics

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
DRAM									
W16	SA0	SA0	NA	NA	O	Z	NA	NA	VCC-DRAM
Y19	SA1	SA1	NA	NA	O	Z	NA	NA	VCC-DRAM
W18	SA2	SA2	NA	NA	O	Z	NA	NA	VCC-DRAM
Y15	SA3	SA3	NA	NA	O	Z	NA	NA	VCC-DRAM
AA20	SA4	SA4	NA	NA	O	Z	NA	NA	VCC-DRAM
V8	SA5	SA5	NA	NA	O	Z	NA	NA	VCC-DRAM
Y7	SA6	SA6	NA	NA	O	Z	NA	NA	VCC-DRAM
Y5	SA7	SA7	NA	NA	O	Z	NA	NA	VCC-DRAM
AA4	SA8	SA8	NA	NA	O	Z	NA	NA	VCC-DRAM
Y3	SA9	SA9	NA	NA	O	Z	NA	NA	VCC-DRAM
AA18	SA10	SA10	NA	NA	O	Z	NA	NA	VCC-DRAM
Y16	SA11	SA11	NA	NA	O	Z	NA	NA	VCC-DRAM
Y18	SA12	SA12	NA	NA	O	Z	NA	NA	VCC-DRAM
AA3	SA13	SA13	NA	NA	O	Z	NA	NA	VCC-DRAM
Y20	SA14	SA14	NA	NA	O	Z	NA	NA	VCC-DRAM
V16	SA15	SA15	NA	NA	O	Z	NA	NA	VCC-DRAM
Y10	SBA0	SBA0	NA	NA	O	Z	NA	NA	VCC-DRAM
V15	SBA1	SBA1	NA	NA	O	Z	NA	NA	VCC-DRAM
W8	SBA2	SBA2	NA	NA	O	Z	NA	NA	VCC-DRAM
W5	SCAS	SCAS	NA	NA	O	Z	NA	NA	VCC-DRAM
AB10	SCKN	SCKN	NA	NA	O	Z	NA	NA	VCC-DRAM
AC11	SCKP	SCKP	NA	NA	O	Z	NA	NA	VCC-DRAM
W13	SCKE0	SCKE0	NA	NA	O	Z	NA	NA	VCC-DRAM
V11	SCKE1	SCKE1	NA	NA	O	Z	NA	NA	VCC-DRAM
W11	SCS0	SCS0	NA	NA	O	Z	NA	NA	VCC-DRAM
V13	SCS1	SCS1	NA	NA	O	Z	NA	NA	VCC-DRAM
Y11	SODT0	SODT0	NA	NA	O	Z	NA	NA	VCC-DRAM
Y13	SODT1	SODT1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA16	SDQ0	SDQ0	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA15	SDQ1	SDQ1	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB15	SDQ2	SDQ2	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC14	SDQ3	SDQ3	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB13	SDQ4	SDQ4	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA12	SDQ5	SDQ5	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB12	SDQ6	SDQ6	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC12	SDQ7	SDQ7	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB21	SDQ8	SDQ8	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC21	SDQ9	SDQ9	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB20	SDQ10	SDQ10	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC20	SDQ11	SDQ11	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC18	SDQ12	SDQ12	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB18	SDQ13	SDQ13	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB17	SDQ14	SDQ14	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC17	SDQ15	SDQ15	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB9	SDQ16	SDQ16	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC9	SDQ17	SDQ17	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB8	SDQ18	SDQ18	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC8	SDQ19	SDQ19	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA6	SDQ20	SDQ20	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA7	SDQ21	SDQ21	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC6	SDQ22	SDQ22	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB6	SDQ23	SDQ23	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC4	SDQ24	SDQ24	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB4	SDQ25	SDQ25	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC3	SDQ26	SDQ26	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB3	SDQ27	SDQ27	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA1	SDQ28	SDQ28	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB1	SDQ29	SDQ29	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y1	SDQ30	SDQ30	NA	NA	I/O	Z	NA	NA	VCC-DRAM
Y2	SDQ31	SDQ31	NA	NA	I/O	Z	NA	NA	VCC-DRAM

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
AB16	SDQM0	SDQM0	NA	NA	O	Z	NA	NA	VCC-DRAM
AC22	SDQM1	SDQM1	NA	NA	O	Z	NA	NA	VCC-DRAM
AA9	SDQM2	SDQM2	NA	NA	O	Z	NA	NA	VCC-DRAM
AB5	SDQM3	SDQM3	NA	NA	O	Z	NA	NA	VCC-DRAM
AB14	SDQS0N	SDQS0N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA13	SDQS0P	SDQS0P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC19	SDQS1N	SDQS1N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB19	SDQS1P	SDQS1P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AA8	SDQS2N	SDQS2N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB7	SDQS2P	SDQS2P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AC2	SDQS3N	SDQS3N	NA	NA	I/O	Z	NA	NA	VCC-DRAM
AB2	SDQS3P	SDQS3P	NA	NA	I/O	Z	NA	NA	VCC-DRAM
W7	SRAS	SRAS	NA	NA	O	Z	NA	NA	VCC-DRAM
W4	SRST	SRST	NA	NA	O	Z	NA	NA	VCC-DRAM
V10	SVREF	SVREF	NA	NA	P	Z	NA	NA	VCC-DRAM
Y4	SWE	SWE	NA	NA	O	Z	NA	NA	VCC-DRAM
W2	SZQ	SZQ	NA	NA	AI	Z	NA	NA	VCC-DRAM
U8,U9,U10,U11, U12,U14,U15, U16	VCC-DRAM	VCC-DRAM	NA	NA	P	NA	NA	NA	NA
AB22	VDD18-DRAM	VDD18-DRAM	NA	NA	P	NA	NA	NA	NA
GPIOB									
T4	PB0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_TX	2		O				
		Reserved	3		NA				
		JTAG_MS0	4		I				
		Reserved	5		NA				
		PB_EINT0	6		I				
		IO Disable	7		OFF				
T3	PB1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_RX	2		I				
		Reserved	3		NA				
		JTAG_CK0	4		I				
		Reserved	5		NA				
		PB_EINT1	6		I				
		IO Disable	7		OFF				
T2	PB2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_RTS	2		O				
		Reserved	3		NA				
		JTAG_DO0	4		O				
		Reserved	5		NA				
		PB_EINT2	6		I				
		IO Disable	7		OFF				
T1	PB3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART2_CTS	2		I				
		Reserved	3		NA				
		JTAG_DI0	4		I				
		Reserved	5		NA				
		PB_EINT3	6		I				
		IO Disable	7		OFF				
V1	PB4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		AIF2_SYNC	2		I/O				
		I2S0_LRCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PB_EINT4	6		I				
		IO Disable	7		OFF				
U2	PB5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		AIF2_BCLK	2		I/O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		I2S0_BCLK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PB_EINT5	6		I				
		IO Disable	7		OFF				
V2	PB6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		AIF2_DOUT	2		O				
		I2S0_DOUT	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PB_EINT6	6		I				
		IO Disable	7		OFF				
U3	PB7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		AIF2_DIN	2		I				
		I2S0_DIN	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PB_EINT7	6		I				
		IO Disable	7		OFF				
U4	PB8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		I2S0_MCLK	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PB_EINT8	6		I				
		IO Disable	7		OFF				
V3	PB9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		UART0_TX	4		O				
		Reserved	5		NA				
		PB_EINT9	6		I				
		IO Disable	7		OFF				
V4	PB10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		UART0_RX	4		I				
		Reserved	5		NA				
		PB_EINT10	6		I				
		IO Disable	7		OFF				
GPIOC									
K5	PC0	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_WE	2		O				
		Reserved	3		NA				
		SPI0_CLK	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
N3	PC1	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_ALE	2		O				
		SDC2_DS	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
M5	PC2	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		NAND_CLE	2		O				
		Reserved	3		NA				
		SPI0_MOSI	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K6	PC3	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE0	2		O				
		Reserved	3		NA				
		SPI0_MISO	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
N2	PC4	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RE	2		O				
		SDC2_CLK	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
M4	PC5	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RB0	2		I				
		SDC2_CMD	3		I/O				
		SPI0_CS	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K2	PC6	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ0	2		I/O				
		SDC2_D0	3		I/O				
		SPI0_HOLD	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L2	PC7	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ1	2		I/O				
		SDC2_D1	3		I/O				
		SPI0_WP	4		I/O				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
M3	PC8	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ2	2		I/O				
		SDC2_D2	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
J2	PC9	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ3	2		I/O				
		SDC2_D3	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K3	PC10	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		NAND_DQ4	2		I/O				
		SDC2_D4	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K1	PC11	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ5	2		I/O				
		SDC2_D5	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
L1	PC12	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ6	2		I/O				
		SDC2_D6	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
M2	PC13	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQ7	2		I/O				
		SDC2_D7	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
K4	PC14	Input	0	Function7	I	Z	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_DQS	2		I/O				
		SDC2_RST	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
M6	PC15	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_CE1	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
J6	PC16	Input	0	Function7	I	PU	PU/PD	20	VCC-PC
		Output	1		O				
		NAND_RB1	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
J7	VCC-PC	VCC-PC	NA	NA	P	NA	NA	NA	NA
GPIOD									
W21	PD0	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		PWM0	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
V19	PD1	Input	0	Function7	I	Z	PU/PD	20	VCC-PD
		Output	1		O				
		PWM1	2		O				
		CPU_CUR_W	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U18	VCC-PD	VCC-PD	NA	NA	P	NA	NA	NA	NA
GPIOE									
T23	PE0	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_PCLK	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T21	PE1	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_MCLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U23	PE2	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_HSYNC	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T22	PE3	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_VSYNC	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U22	PE4	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D0	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T20	PE5	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D1	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U20	PE6	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D2	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	6		NA				
		IO Disable	7		OFF				
T19	PE7	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D3	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
U21	PE8	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D4	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
W23	PE9	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D5	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
V22	PE10	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D6	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
W22	PE11	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D7	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
V21	PE12	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_SCK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
V20	PE13	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
Y23	PE14	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D8	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	6		NA				
		IO Disable	7		OFF				
AA23	PE15	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		CSI_D9	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
Y22	PE16	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		Reserved	2		NA				
		TWI2_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
AB23	PE17	Input	0	Function7	I	Z	PU/PD	20	VCC-PE
		Output	1		O				
		Reserved	2		NA				
		TWI2_SDA	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		Reserved	6		NA				
		IO Disable	7		OFF				
T17	VCC-PE	VCC-PE	NA	NA	P	NA	NA	NA	NA
GPIOF									
J4	PF0	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		SDC0_D1	2		I/O				
		JTAG_MS1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT0	6		I				
		IO Disable	7		OFF				
J3	PF1	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		SDC0_D0	2		I/O				
		JTAG_DI1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT1	6		I				
		IO Disable	7		OFF				
J5	PF2	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		SDC0_CLK	2		O				
		UART0_TX	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT2	6		I				
		IO Disable	7		OFF				
G5	PF3	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		SDC0_CMD	2		I/O				
		JTAG_DO1	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT3	6		I				
		IO Disable	7		OFF				
G4	PF4	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		SDC0_D3	2		I/O				
		UART0_RX	3		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT4	6		I				
		IO Disable	7		OFF				
H3	PF5	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		SDC0_D2	2		I/O				
		JTAG_CK1	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT5	6		I				
		IO Disable	7		OFF				
H2	PF6	Input	0	Function7	I	Z	PU/PD	20	VCC-PF
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PF_EINT6	6		I				
		IO Disable	7		OFF				
G6	VCC-PF	VCC-PF	NA	NA	P	NA	NA	NA	NA
GPIOG									
M22	PG0	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT0	6		I				
		IO Disable	7		OFF				
N23	PG1	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_CMD	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT1	6		I				
		IO Disable	7		OFF				
M19	PG2	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D0	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT2	6		I				
		IO Disable	7		OFF				
P23	PG3	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D1	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT3	6		I				
		IO Disable	7		OFF				
P22	PG4	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		SDC1_D2	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT4	6		I				
		IO Disable	7		OFF				
N22	PG5	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		SDC1_D3	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT5	6		I				
		IO Disable	7		OFF				
N19	PG6	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT6	6		I				
		IO Disable	7		OFF				
N20	PG7	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT7	6		I				
		IO Disable	7		OFF				
P21	PG8	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_RTS	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT8	6		I				
		IO Disable	7		OFF				
N21	PG9	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		UART1_CTS	2		I				
		I2S1_MCLK	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT9	6		I				
		IO Disable	7		OFF				
R22	PG10	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		AIF3_SYNC	2		I/O				
		I2S1_LRCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT10	6		I				
		IO Disable	7		OFF				
R21	PG11	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		AIF3_BCLK	2		I/O				
		I2S1_BCLK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT11	6		I				
		IO Disable	7		OFF				
R20	PG12	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				
		AIF3_DOUT	2		O				
		I2S1_DOUT	3		O				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT12	6		I				
		IO Disable	7		OFF				
R19	PG13	Input	0	Function7	I	Z	PU/PD	20	VCC-PG
		Output	1		O				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		AIF3_DIN	2		I				
		I2S1_DIN	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PG_EINT13	6		I				
		IO Disable	7		OFF				
M17	VCC-PG	VCC-PG	NA	NA	P	NA	NA	NA	NA
GPIOH									
N4	PH0	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI0_SCK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT0	6		I				
		IO Disable	7		OFF				
N6	PH1	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI0_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT1	6		I				
		IO Disable	7		OFF				
N5	PH2	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI1_SCK	2		I/O				
		CPU_CUR_W	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT2	6		I				
		IO Disable	7		OFF				
P3	PH3	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		TWI1_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT3	6		I				
		IO Disable	7		OFF				
P2	PH4	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART3_TX	2		O				
		I2S2_MCLK	3		O				
		SPI1_CS	4		I/O				
		TWI3_SCK	5		I/O				
		PH_EINT4	6		I				
		IO Disable	7		OFF				
P1	PH5	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART3_RX	2		I				
		I2S2_LRCK	3		I/O				
		SPI1_CLK	4		I/O				
		TWI3_SDA	5		I/O				
		PH_EINT5	6		I				
		IO Disable	7		OFF				
R6	PH6	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART3_RTS	2		O				
		I2S2_BCLK	3		I/O				
		SPI1_MOSI	4		I/O				
		TWI4_SCK	5		I/O				
		PH_EINT6	6		I				
		IO Disable	7		OFF				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
R5	PH7	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		UART3_CTS	2		I				
		I2S2_DOUT	3		O				
		SPI1_MISO	4		I/O				
		TWI4_SDA	5		I/O				
		PH_EINT7	6		I				
		IO Disable	7		OFF				
R4	PH8	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		DMIC_DATA3	2		I				
		I2S2_DIN	3		I				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT8	6		I				
		IO Disable	7		OFF				
R3	PH9	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		DMIC_DATA2	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT9	6		I				
		IO Disable	7		OFF				
R2	PH10	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		DMIC_DATA1	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT10	6		I				
		IO Disable	7		OFF				
T6	PH11	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		DMIC_DATA0	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT11	6		I				
		IO Disable	7		OFF				
T5	PH12	Input	0	Function7	I	Z	PU/PD	20	VCC-IO
		Output	1		O				
		DMIC_CLK	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		PH_EINT12	6		I				
		IO Disable	7		OFF				
GPIO L									
H21	PL0	Input	0	Function7	I	PU	PU/PD	20	VCC-RTC
		Output	1		O				
		S_RSB_SCK	2		I/O				
		S_TWI0_SCK	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT0	6		I				
		IO Disable	7		OFF				
G21	PL1	Input	0	Function7	I	PU	PU/PD	20	VCC-RTC
		Output	1		O				
		S_RSB_SDA	2		I/O				
		S_TWI0_SDA	3		I/O				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT1	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
G20	PL2	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_UART_TX	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT2	6		I				
		IO Disable	7		OFF				
G22	PL3	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_UART_RX	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT3	6		I				
		IO Disable	7		OFF				
H19	PL4	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_MS	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT4	6		I				
		IO Disable	7		OFF				
H22	PL5	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_CK	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT5	6		I				
		IO Disable	7		OFF				
J19	PL6	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_DO	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT6	6		I				
		IO Disable	7		OFF				
H20	PL7	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_JTAG_DI	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT7	6		I				
		IO Disable	7		OFF				
J20	PL8	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_TWI1_SCK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT8	6		I				
		IO Disable	7		OFF				
J21	PL9	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_TWI1_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT9	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
J22	PL10	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_TWI2_SCK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT10	6		I				
		IO Disable	7		OFF				
H23	PL11	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_TWI2_SDA	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT11	6		I				
		IO Disable	7		OFF				
J23	PL12	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_SPI0_CS	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT12	6		I				
		IO Disable	7		OFF				
K18	PL13	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_SPI0_CLK	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT13	6		I				
		IO Disable	7		OFF				
K20	PL14	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_SPI0_MOSI	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT14	6		I				
		IO Disable	7		OFF				
K22	PL15	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_SPI0_MISO	2		I/O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT15	6		I				
		IO Disable	7		OFF				
K21	PL16	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_PWM	2		O				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT16	6		I				
		IO Disable	7		OFF				
K19	PL17	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		S_CPU_CUR_W	2		I				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT17	6		I				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		IO Disable	7		OFF				
M21	PL18	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT18	6		I				
		IO Disable	7		OFF				
M20	PL19	Input	0	Function7	I	Z	PU/PD	20	VCC-PL
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PL_EINT19	6		I				
		IO Disable	7		OFF				
G17	VCC-PL	VCC-PL	NA	NA	P	NA	NA	NA	NA
GPIOM									
F22	PM0	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT0	6		I				
		IO Disable	7		OFF				
E22	PM1	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT1	6		I				
		IO Disable	7		OFF				
E23	PM2	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT2	6		I				
		IO Disable	7		OFF				
F21	PM3	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT3	6		I				
		IO Disable	7		OFF				
F23	PM4	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				
		Reserved	5		NA				
		S_PM_EINT4	6		I				
		IO Disable	7		OFF				
G19	PM5	Input	0	Function7	I	Z	PU/PD	20	VCC-PM
		Output	1		O				
		Reserved	2		NA				
		Reserved	3		NA				
		Reserved	4		NA				

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
		Reserved	5		NA				
		S_PM_EINT5	6		I				
		IO Disable	7		OFF				
H18	VCC-PM	VCC-PM	NA	NA	P	NA	NA	NA	NA
System									
D19	NMI	NMI	NA	NA	I/O,OD	Z	PU/PD	NA	VCC-RTC
E21	RESET	RESET	NA	NA	I	Z	PU/PD	NA	VCC-RTC
E19	TEST	TEST	NA	NA	I	PD	PU/PD	NA	VCC-RTC
E12	UBOOT	UBOOT	NA	NA	I	PU	PU/PD	NA	AVCC
V6	JTAG-SEL	JTAG-SEL	NA	NA	I	PU	PU/PD	NA	VCC-IO
B11	BOOT-SEL0	BOOT-SEL0	NA	NA	I	PU	PU/PD	NA	AVCC
L20	AP-CK-MUX	AP-CK-MUX	NA	NA	I	PU	PU/PD	NA	VCC-RTC
ADC									
D10	GPADC	GPADC	NA	NA	AI	NA	NA	NA	AVCC
MIPI DSI									
C8	DSI0-CKN	DSI0-CKN	NA	NA	AO	NA	NA	NA	VCC-DSI
B8	DSI0-CKP	DSI0-CKP	NA	NA	AO	NA	NA	NA	VCC-DSI
B10	DSI0-DN0	DSI0-DN0	NA	NA	A I/O	NA	NA	NA	VCC-DSI
A10	DSI0-DP0	DSI0-DP0	NA	NA	A I/O	NA	NA	NA	VCC-DSI
C9	DSI0-DN1	DSI0-DN1	NA	NA	AO	NA	NA	NA	VCC-DSI
B9	DSI0-DP1	DSI0-DP1	NA	NA	AO	NA	NA	NA	VCC-DSI
B7	DSI0-DN2	DSI0-DN2	NA	NA	AO	NA	NA	NA	VCC-DSI
A7	DSI0-DP2	DSI0-DP2	NA	NA	AO	NA	NA	NA	VCC-DSI
C6	DSI0-DN3	DSI0-DN3	NA	NA	AO	NA	NA	NA	VCC-DSI
B6	DSI0-DP3	DSI0-DP3	NA	NA	AO	NA	NA	NA	VCC-DSI
B4	DSI1-CKN	DSI1-CKN	NA	NA	AO	NA	NA	NA	VCC-DSI
C4	DSI1-CKP	DSI1-CKP	NA	NA	AO	NA	NA	NA	VCC-DSI
C5	DSI1-DN0	DSI1-DN0	NA	NA	A I/O	NA	NA	NA	VCC-DSI
B5	DSI1-DP0	DSI1-DP0	NA	NA	A I/O	NA	NA	NA	VCC-DSI
A4	DSI1-DN1	DSI1-DN1	NA	NA	AO	NA	NA	NA	VCC-DSI
A5	DSI1-DP1	DSI1-DP1	NA	NA	AO	NA	NA	NA	VCC-DSI
B3	DSI1-DN2	DSI1-DN2	NA	NA	AO	NA	NA	NA	VCC-DSI
C3	DSI1-DP2	DSI1-DP2	NA	NA	AO	NA	NA	NA	VCC-DSI
B2	DSI1-DN3	DSI1-DN3	NA	NA	AO	NA	NA	NA	VCC-DSI
A2	DSI1-DP3	DSI1-DP3	NA	NA	AO	NA	NA	NA	VCC-DSI
D6,D7	VCC-DSI	VCC-DSI	NA	NA	P	NA	NA	NA	NA
eDP									
G1	EDPTX0N	EDPTX0N	NA	NA	AO	NA	NA	NA	VCC-EDP
G2	EDPTX0P	EDPTX0P	NA	NA	AO	NA	NA	NA	VCC-EDP
F1	EDPTX1N	EDPTX1N	NA	NA	AO	NA	NA	NA	VCC-EDP
F2	EDPTX1P	EDPTX1P	NA	NA	AO	NA	NA	NA	VCC-EDP
E1	EDPTX2N	EDPTX2N	NA	NA	AO	NA	NA	NA	VCC-EDP
E2	EDPTX2P	EDPTX2P	NA	NA	AO	NA	NA	NA	VCC-EDP
D1	EDPTX3N	EDPTX3N	NA	NA	AO	NA	NA	NA	VCC-EDP
D2	EDPTX3P	EDPTX3P	NA	NA	AO	NA	NA	NA	VCC-EDP
C1	EDPAUXN	EDPAUXN	NA	NA	AO	NA	NA	NA	VCC-EDP
C2	EDPAUXP	EDPAUXP	NA	NA	AO	NA	NA	NA	VCC-EDP
F5	EDPHPD	EDPHPD	NA	NA	AO	NA	NA	NA	VCC-EDP
F4	VCC-EDP	VCC-EDP	NA	NA	P	NA	NA	NA	NA
E4	GND-EDP	GND-EDP	NA	NA	G	NA	NA	NA	NA
USB									
A13	USB0-DM	USB0-DM	NA	NA	A I/O	NA	NA	NA	VCC-USB
B13	USB0-DP	USB0-DP	NA	NA	A I/O	NA	NA	NA	VCC-USB
A12	USB1-DM	USB1-DM	NA	NA	A I/O	NA	NA	NA	VCC-USB
B12	USB1-DP	USB1-DP	NA	NA	A I/O	NA	NA	NA	VCC-USB
C11	VCC-USB	VCC-USB	NA	NA	P	NA	NA	NA	NA
Audio Codec									
D18	PHONEINN	PHONEINN	NA	NA	AI	NA	NA	NA	AVCC
D17	PHONEINP	PHONEINP	NA	NA	AI	NA	NA	NA	AVCC
A18	MICIN1P	MICIN1P	NA	NA	AI	NA	NA	NA	AVCC
B18	MICIN1N	MICIN1N	NA	NA	AI	NA	NA	NA	AVCC
A19	MICIN2P	MICIN2P	NA	NA	AI	NA	NA	NA	AVCC
B19	MICIN2N	MICIN2N	NA	NA	AI	NA	NA	NA	AVCC
A20	MICIN3P	MICIN3P	NA	NA	AI	NA	NA	NA	AVCC

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
B20	MICIN3N	MICIN3N	NA	NA	AI	NA	NA	NA	AVCC
C18	MIC-DET	MIC-DET	NA	NA	AI	NA	NA	NA	AVCC
D14	MBIAS	MBIAS	NA	NA	AO	NA	NA	NA	VDD33
A15	SPKLN	SPKLN	NA	NA	AO	NA	NA	NA	AVCC
B15	SPKLP	SPKLP	NA	NA	AO	NA	NA	NA	AVCC
C16	SPKRN	SPKRN	NA	NA	AO	NA	NA	NA	AVCC
D16	SPKRP	SPKRP	NA	NA	AO	NA	NA	NA	AVCC
C15	VRA2	VRA2	NA	NA	AO	NA	NA	NA	AVCC
D15	VRP	VRP	NA	NA	AO	NA	NA	NA	AVCC
F16	AVCC	AVCC	NA	NA	P	NA	NA	NA	NA
A16	LINEINR	LINEINR	NA	NA	AI	NA	NA	NA	AVCC
B16	LINEINL	LINEINL	NA	NA	AI	NA	NA	NA	AVCC
B17	LINEOUTR	LINEOUTR	NA	NA	AO	NA	NA	NA	AVCC
C17	LINEOUTL	LINEOUTL	NA	NA	AO	NA	NA	NA	AVCC
E16	AGND	AGND	NA	NA	G	NA	NA	NA	NA
B14	HPOUTR	HPOUTR	NA	NA	AO	NA	NA	NA	CPVIN
C14	HPOUTL	HPOUTL	NA	NA	AO	NA	NA	NA	CPVIN
E15	HBIAS	HBIAS	NA	NA	AO	NA	NA	NA	VDD33
D13	HP-DET	HP-DET	NA	NA	AI	NA	NA	NA	CPVIN
C13	HPOUTFB	HPOUTFB	NA	NA	AI	NA	NA	NA	CPVIN
C19	REXT	REXT	NA	NA	AO	NA	NA	NA	AVCC
E11	CPVDD	CPVDD	NA	NA	P	NA	NA	NA	NA
D12	CPVEE	CPVEE	NA	NA	P	NA	NA	NA	NA
E13	CPVIN	CPVIN	NA	NA	P	NA	NA	NA	NA
F14	VEE	VEE	NA	NA	P	NA	NA	NA	NA
E14	VPP	VPP	NA	NA	P	NA	NA	NA	NA
G15	VDD33	VDD33	NA	NA	P	NA	NA	NA	NA
Clock									
D22	X32KIN	X32KIN	NA	NA	AI	NA	NA	NA	VCC-RTC
C23	X32KOUT	X32KOUT	NA	NA	AO	NA	NA	NA	VCC-RTC
D20	X32KFOUT	X32KFOUT	NA	NA	AO,OD	NA	NA	NA	VCC-RTC
D21	VCC-RTC	VCC-RTC	NA	NA	P	NA	NA	NA	NA
E20	RTC-VIO	RTC-VIO	NA	NA	AO	NA	NA	NA	VCC-RTC
L23	X24MIN	X24MIN	NA	NA	AI	NA	NA	NA	VCC-PLL
L22	X24MOUT	X24MOUT	NA	NA	AO	NA	NA	NA	VCC-PLL
M23	PLLTEST	PLLTEST	NA	NA	AO,OD	NA	NA	NA	VCC-PLL
J18	VCC-PLL	VCC-PLL	NA	NA	P	NA	NA	NA	NA
DCXO									
B22	DXIN	DXIN	NA	NA	AI	NA	NA	NA	VCC-RTC
B23	DXOUT	DXOUT	NA	NA	AO	NA	NA	NA	VCC-RTC
C22	DXLDO_OUT	DXLDO_OUT	NA	NA	AO	NA	NA	NA	VCC-RTC
C21	DXVCCIO	DXVCCIO	NA	NA	P	NA	NA	NA	NA
A22	REFCLK_OUT	REFCLK_OUT	NA	NA	AO	NA	NA	NA	VCC-RTC
B21	WREQIN	WREQIN	NA	NA	AI	NA	NA	NA	DXVCCIO
Efuse									
G12	VCC-EFUSE	VCC-EFUSE	NA	NA	P	NA	NA	NA	NA
Power									
R8	VDD-CPUFB	VDD-CPUFB	NA	NA	P	NA	NA	NA	NA
R17	VDD-GPUFB	VDD-GPUFB	NA	NA	P	NA	NA	NA	NA
R7,T7	VCC-IO	VCC-IO	NA	NA	P	NA	NA	NA	NA
L15,L16	VDD-VE	VDD-VE	NA	NA	P	NA	NA	NA	NA
N15,P14,P15,P16, R14,R16	VDD-GPU	VDD-GPU	NA	NA	P	NA	NA	NA	NA
M9,M11,N8,N9, N10,P8,P10,P11	VDD-CPU	VDD-CPU	NA	NA	P	NA	NA	NA	NA
G16	VDD-CPUS	VDD-CPUS	NA	NA	P	NA	NA	NA	NA
G8,G9,H8,H9, H10,H11,J10,J11	VDD-SYS	VDD-SYS	NA	NA	P	NA	NA	NA	NA
Ground									
A1,A11,A21,A23, B1,C10,C12,C20, D3,D4,D5,D8,D9, D11,D23,E3,E5, E6,E7,E8,E9,E18, F3,F6,F7,F8,F9, F10,F13,F17,G3, G7,G10,G11,G13, G14,G18,H1,H6, H7,H12,H13,H14,	GND	GND	NA	NA	G	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Signal Name[3]	Function[4]	Ball Reset Rel. Function[5]	Type[6]	Ball Reset State[7]	Pull Up/Down[8]	Buffer Strength[9] (mA)	Power Supply[10]
H15,H16,H17,J8, J9,J12,J13,J14, J15,J16,J17,K7,K8, K9,K10,K11,K12, K13,K14,K15,K16, K17,L3,L7,L8,L9, L10,L11,L12,L13, L14,L21,M8,M10, M12,M13,M14, M15,M16,N1,N7, N11,N12,N13, N14,N16,N17, N18,P7,P9,P12, P13,P17,P18,R9, R10,R11,R12,R13, R15,T8,T9,T10, T11,T12,T13,T14, T15,T16,U7,U13, U17,V7,V18,W1, W3,W10,W15, W19,Y8,AA2,AA5, AA14,AA19,AA21, AA22,AB11,AC1, AC10,AC16,AC23									
Other									
E10	NC	NC	NA	NA	NA	NA	NA	NA	NA

(1).NA: No Application.
(2).OFF: Disable IO function of GPIO.

4.2. Detailed Signal Description

Table 4-2 shows the detailed function description of every signal based on the different interface.

(1).**Signal Name**: The name of every signal.

(2).**Description**: The detailed function description of every signal.

(3).**Type**: Denotes the signal direction:

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-2. Detailed Signal Description

Signal Name(1)	Description(2)	Type(3)
DRAM		
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQS[3:0]P	DRAM Active-high Bidirectional Data Strobes to the Memory Device	I/O
SDQS[3:0]N	DRAM Active-low Bidirectional Data Strobes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	O
SCKP	DRAM Active-high Clock Signal to the Memory Device	O
SCKN	DRAM Active-low Clock Signal to the Memory Device	O
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device for Two Chip Select	O
SA[15:0]	DRAM Address Signal to the Memory Device	O
SWE	DRAM Write Enable Strobe to the Memory Device	O
SCAS	DRAM Column Address Strobe to the Memory Device	O
SRAS	DRAM Row Address Strobe to the Memory Device	O
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SBA[2:0]	DRAM Bank Address Signal to the Memory Device	O
SODT[1:0]	DRAM On-Die Termination Output Signal for Two Chip Select	O
SRST	DRAM Reset Signal to the Memory Device	O
SZQ	DRAM ZQ Calibration	AI
SVREF	DRAM Reference Voltage Input	P
VCC-DRAM	DRAM Power Supply	P
VDD18-DRAM	DRAM Power Supply	P
System Control		
TEST	TEST Signal	I
NMI	Non-Maskable Interrupt	I
RESET	RESET Signal	I/O
UBOOT	USB BOOT	I
JTAG-SEL	JTAG Mode Select	I

Signal Name[1]	Description[2]	Type[3]
BOOT-SEL0	BOOT Media Select	I
AP-CK-MUX	Application Processor Clock Source Select	I
Clock		
RTC-VIO	Internal LDO Output Bypass	AO
X32KIN	Clock Input of 32768Hz Crystal	AI
X32KOUT	Clock Output of 32768Hz Crystal	AO
X32KFOUT	Clock Output of LOSC	AO,OD
VCC-RTC	RTC Power Supply	P
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
PLLTEST	PLL Test	AO,OD
VCC-PLL	PLL Power Supply	P
DCXO		
DXVCCIO	Digital Compensated Crystal Oscillator Power Supply	P
DXLDO_OUT	Internal Supply Regulator Output	AO
REFCLK_OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
WREQIN	Digital Compensated Crystal Oscillator Wakeup Signal, High Active	AI
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
USB		
USB0-DM	USB Data Signal DM	A I/O
USB0-DP	USB Data Signal DP	A I/O
USB1-DM	USB Data Signal DM	A I/O
USB1-DP	USB Data Signal DP	A I/O
VCC-USB	USB Power Supply	P
ADC		
GPADC	General Purpose ADC Input	AI
AUDIO CODEC		
LINEINL	LINE-IN Left Channel Input	AI
LINEINR	LINE-IN Right Channel Input	AI
LINEOUTL	LINE-OUT Left Channel Output, or Positive Differential Output	AO
LINEOUTR	LINE-OUT Right Channel Output, or Negative Differential Output	AO
MIC-DET	Headphone MIC Detect	AI
HBIAS	Master Analog Headphone Bias Voltage Output	AO
HPOUTL	Headphone Output Left Channel	AO
HPOUTR	Headphone Output Right Channel	AO
HP-DET	Headphone Detect	AI
HPOUTFB	Pseudo Differential Headphone Ground Reference	AI
MBIAS	Master Analog Microphone Bias Voltage Output	AO
MICIN1N	Microphone Negative Input 1	AI
MICIN1P	Microphone Positive Input 1	AI
MICIN2N	Microphone Negative Input 2	AI
MICIN2P	Microphone Positive Input 2	AI
MICIN3P	Microphone Positive Input 3	AI

Signal Name[1]	Description[2]	Type[3]
MICIN3N	Microphone Negative Input 3	AI
PHONEINP	Phone Positive Differential Input, or Right Single-end Input	AI
PHONEINN	Phone Negative Differential Input, or Left Single-end Input	AI
SPKLP	Left Speaker Positive Output	AO
SPKLN	Left Speaker Negative Output	AO
SPKRP	Right Speaker Positive Output	AO
SPKRN	Right Speaker Negative Output	AO
VRA2	Reference Voltage	AO
VRP	Reference Voltage	AO
REXT	External Reference Pin	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
CPVIN	Analog Power for LDO	P
CPVDD	Analog Power for Headphone Charge Pump	P
CPVEE	Charge Pump Negative Voltage Output	P
VEE	PA Negative Voltage Input	P
VPP	PA Positive Voltage Input	P
VDD33	Analog Power 3.3V	P
SD /MMC		
SDC0_CMD	Command Signal for SD/TF Card	I/O
SDC0_CLK	Clock for SD/TF Card	O
SDC0_D[3:0]	Data Input and Output for SD/TF Card	I/O
SDC1_CMD	Command Signal for SDIO WIFI	I/O
SDC1_CLK	Clock for SDIO WIFI	O
SDC1_D[3:0]	Data Input and Output for SDIO WIFI	I/O
SDC2_CMD	Command Signal for SD/eMMC	I/O
SDC2_CLK	Clock for SD/eMMC	O
SDC2_D[7:0]	Data Input and Output for SD/eMMC	I/O
SDC2_RST	Reset Signal for SD/eMMC	O
SDC2_DS	Data Strobe for SD/eMMC	I/O
NAND		
NAND_DQ[7:0]	Nand Flash Data Bit	I/O
NAND_WE	Nand Flash Write Enable	O
NAND_ALE	Nand Flash Address Latch Enable	O
NAND_CLE	Nand Flash Command Latch Enable	O
NAND_CE1	Nand Flash Chip Select	O
NAND_CE0	Nand Flash Chip Select	O
NAND_RE	Nand Flash Read Enable	O
NAND_RB0	Nand Flash Ready/Busy Bit	I
NAND_RB1	Nand Flash Ready/Busy Bit	I
NAND_DQS	Nand Flash Data Strobe	I/O
I2S/PCM(x=[2:0])		
I2Sx_MCLK	I2S Master Clock	O
I2Sx_LRCK	I2S/PCM Sample Rate Clock/Sync	I/O

Signal Name[1]	Description[2]	Type[3]
I2Sx_BCLK	I2S/PCM Sample Rate Clock	I/O
I2Sx_DOUT	I2S/PCM Serial Data Output	O
I2Sx_DIN	I2S/PCM Serial Data Input	I
DMIC		
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA[3:0]	Digital Microphone Data Input	I
Interrupt		
PB_EINT[10:0]	GPIO B Interrupt	I
PF_EINT[6:0]	GPIO F Interrupt	I
PG_EINT[13:0]	GPIO G Interrupt	I
PH_EINT[12:0]	GPIO H Interrupt	I
S_PL_EINT[19:0]	GPIO L Interrupt	I
S_PM_EINT[5:0]	GPIO M Interrupt	I
PWM		
PWM[1:0]	Pulse Width Modulation Output Channel0	O
S_PWM	Pulse Width Modulation Output Channel for CPUS	O
eDP		
EDPAUXP	eDP Auxiliary Positive	AO
EDPAUXN	eDP Auxiliary Negative	AO
EDPHPD	eDP Hot Plug Detection	AO
EDPTX0P	eDP Data Transmit Positive0	AO
EDPTX0N	eDP Data Transmit Negative0	AO
EDPTX1P	eDP Data Transmit Positive1	AO
EDPTX1N	eDP Data Transmit Negative1	AO
EDPTX2P	eDP Data Transmit Positive2	AO
EDPTX2N	eDP Data Transmit Negative2	AO
EDPTX3P	eDP Data Transmit Positive3	AO
EDPTX3N	eDP Data Transmit Negative3	AO
GND-EDP	eDP Ground	G
VCC-EDP	eDP Power Supply	P
CSI		
CSI_PCLK	CSI Pixel Clock	I
CSI_MCLK	CSI Master Clock	O
CSI_HSYNC	CSI Horizontal SYNC	I
CSI_VSYNC	CSI Vertical SYNC	I
CSI_D[9:0]	CSI Data Input	I
CSI_SCK	CSI Command Serial Clock Signal	O
CSI_SDA	CSI Command Serial Data Signal	I/O
MIPI DSI(x=[1:0])		
DSIx-CKN	MIPI DSI Negative Differential Clock Line	AO
DSIx-CKP	MIPI DSI Positive Differential Clock Line	AO
DSIx-DN0	MIPI DSI Negative Differential Data Line0	A I/O
DSIx-DP0	MIPI DSI Positive Differential Data Line0	A I/O
DSIx-DN1	MIPI DSI Negative Differential Data Line1	AO

Signal Name[1]	Description[2]	Type[3]
DSIx-DP1	MIPI DSI Positive Differential Data Line1	AO
DSIx-DN2	MIPI DSI Negative Differential Data Line2	AO
DSIx-DP2	MIPI DSI Positive Differential Data Line2	AO
DSIx-DN3	MIPI DSI Negative Differential Data Line3	AO
DSIx-DP3	MIPI DSI Positive Differential Data Line3	AO
VCC-DSI	MIPI DSI Power Supply	P
SPI		
SPI0_CS	SPI0 Chip Select Signal, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0_WP	SPI0 Write Protect	I/O
SPI0_HOLD	SPI0 Hold Signal	I/O
SPI1_CS	SPI1 Chip Select Signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
S_SPI0_CS	SPI Chip Select Signal for CPUS, Low Active	I/O
S_SPI0_CLK	SPI Clock Signal for CPUS	I/O
S_SPI0_MOSI	SPI Master Data Out, Slave Data In for CPUS	I/O
S_SPI0_MISO	SPI Master Data In, Slave Data Out for CPUS	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear to Send	I
UART1_RTS	UART1 Data Request to Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear to Send	I
UART2_RTS	UART2 Data Request to Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear to Send	I
UART3_RTS	UART3 Data Request to Send	O
S_UART_TX	UART Data Transmit for CPUS	O
S_UART_RX	UART Data Receive for CPUS	I
TWI		
TWI0_SCK	TWI0 Serial Clock Signal	I/O
TWI0_SDA	TWI0 Serial Data Signal	I/O
TWI1_SCK	TWI1 Serial Clock Signal	I/O
TWI1_SDA	TWI1 Serial Data Signal	I/O
TWI2_SCK	TWI2 Serial Clock Signal	I/O

Signal Name[1]	Description[2]	Type[3]
TWI2_SDA	TWI2 Serial Data Signal	I/O
TWI3_SCK	TWI3 Serial Clock Signal	I/O
TWI3_SDA	TWI3 Serial Data Signal	I/O
TWI4_SCK	TWI4 Serial Clock Signal	I/O
TWI4_SDA	TWI4 Serial Data Signal	I/O
S_TWI0_SCK	TWI0 Serial Clock Signal for CPUS	I/O
S_TWI0_SDA	TWI0 Serial Data Signal for CPUS	I/O
S_TWI1_SCK	TWI1 Serial Clock Signal for CPUS	I/O
S_TWI1_SDA	TWI1 Serial Data Signal for CPUS	I/O
S_TWI2_SCK	TWI2 Serial Clock Signal for CPUS	I/O
S_TWI2_SDA	TWI2 Serial Data Signal for CPUS	I/O
JTAG		
JTAG_MS[1:0]	JTAG Mode Select	I
JTAG_CK[1:0]	JTAG Clock Signal	I
JTAG_DO[1:0]	JTAG Data Output	O
JTAG_DI[1:0]	JTAG Data Input	I
S_JTAG_MS	JTAG Mode Select for CPUS	I
S_JTAG_CK	JTAG Clock Signal for CPUS	I
S_JTAG_DO	JTAG Data Output for CPUS	O
S_JTAG_DI	JTAG Data Input for CPUS	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
$I_{I/O}$	In/Out Current for Input and Output		-40	40	mA
AVCC	Power Supply for Analog Part		-0.3	1.98	V
DXVCCIO	Power Supply for DCXO-IO		-0.3	3.63	V
VCC-PC	Digital GPIO C Power		-0.3	3.63	V
VCC-PD	Digital GPIO D Power		-0.3	3.63	V
VCC-PE	Digital GPIO E Power		-0.3	3.63	V
VCC-PF	Digital GPIO F Power		-0.3	3.63	V
VCC-PG	Digital GPIO G Power		-0.3	3.63	V
VCC-PL	Digital GPIO L Power		-0.3	3.63	V
VCC-PM	Digital GPIO M Power		-0.3	3.63	V
VCC-IO	Power Supply for 3.3V Digital Part		-0.3	3.63	V
VCC-RTC	Power Supply for RTC		-0.3	1.98	V
VCC-PLL	Power Supply for System PLL		-0.3	1.98	V
VCC-DSI	Power Supply for MIPI DSI		-0.3	1.98	V
VCC-EDP	Power Supply for eDP		-0.3	1.98	V
VCC-USB	Power Supply for USB		-0.3	3.63	V
VCC-DRAM	Power Supply for DRAM		-0.3	1.98	V
VDD18-DRAM	Power Supply for DRAM Controller		-0.3	1.98	V
VDD-VE	Power Supply for VE		-0.3	1.4	V
VDD-GPU	Power Supply for GPU		-0.3	1.4	V
VDD-CPU	Power Supply for CPU0~3		-0.3	1.4	V
VDD-CPUS	Power Supply for CPUS		-0.3	1.4	V
VDD-SYS	Power Supply for System		-0.3	1.4	V
T_{STG}	Storage Temperature		-40	125	℃
V_{ESD}	Electrostatic Discharge	Human Body Model(HBM)[1]	-	2000	V
		Charged Device Model(CDM)[2]	-	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin[3]		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin[4]		Pass		

(1). Test method: JEDEC JS-001-2014. JEDEC publication JEP155 states that 500V HBM allows safe manufacturing with a

standard ESD control process.
(2). Test method: JEDEC JS-002-2014. JEDEC publication JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3). Current test performance: Pins stressed per JEDEC JESD78D and passed with I/O pin injection current as defined in JEDEC.
(4). Over voltage performance: Supplies stressed per JEDEC JESD78D and passed voltage injection as defined in JEDEC.

5.2. Recommended Operating Conditions

All A63 modules are used under the operating conditions contained in Table 5-2.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	70	°C
Tj	Junction Temperature Range	-20	-	110	°C
AVCC	Power Supply for Analog Part	1.782	1.8	1.818	V
DXVCCIO	Power Supply for DCXO-IO	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PC	Digital GPIO C Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PD	Digital GPIO D Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PE	Digital GPIO E Power 1.8V voltage 2.8V voltage 3.3V voltage	1.62 2.52 2.97	1.8 2.8 3.3	1.98 3.08 3.63	V
VCC-PF	Digital GPIO F Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PG	Digital GPIO G Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PL	Digital GPIO L Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PM	Digital GPIO M Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-IO	Power Supply for 3.3V Digital Part	2.97	3.3	3.63	V
VCC-RTC	Power Supply for RTC	1.62	1.8	1.98	V
VCC-PLL	Power Supply for System PLL	1.62	1.8	1.98	V
VCC-EFUSE	Power Supply for EFUSE Program Mode	1.8	1.89	1.98	V
VCC-DSI	Power Supply for MIPI DSI	1.62	1.8	1.98	V
VCC-EDP	Power Supply for eDP	1.62	1.8	1.98	V
VCC-USB	Power Supply for USB	3.07	3.3	3.6	V
VCC-DRAM	Power Supply for DDR2	1.7	1.8	1.9	V
	Power Supply for DDR3	1.425	1.5	1.575	V
	Power Supply for DDR3L	1.425	1.5	1.575	V
	Power Supply for LPDDR2	1.14	1.2	1.3	V

	Power Supply for LPDDR3	1.14	1.2	1.3	V
VDD18-DRAM	Power Supply for DRAM Controller	1.7	1.8	1.95	V
VDD-VE	Power Supply for VE	0.81	0.9	0.99	V
VDD-GPU	Power Supply for GPU	0.81	-	1.08	V
VDD-CPU	Power Supply for CPU0~3	0.81	-	1.08	V
VDD-CPUS	Power Supply for CPUS	0.87	0.9	0.93	V
VDD-SYS	Power Supply for System	0.87	0.9	0.93	V

5.3. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

5.4. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of A63.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	50	100	150	kΩ
R_{PD}	Input Pull-down Resistance	50	100	150	kΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.5. GPADC Electrical Characteristics

GPADC contains one-channel analog-to-digital(ADC) converter. The ADC is a type of successive approximation register(SAR) converter. Table 5-4 lists GPADC electrical characteristics.

Table 5-4. GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

5.6. Oscillator Electrical Characteristics

A63 contains two external input clocks:X24MIN and X32KIN, two output clocks:X24MOUT and X32KOUT.
The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X24MIN. Table 5-5 lists the 24MHz crystal specifications.

Table 5-5. 24MHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	-	-	2	ms
	Frequency Tolerance at 25 °C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
P_{ON}	Drive Level	-	-	300	uW
C_L	Equivalent Load Capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	-	25	50	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	4.72	-	fF
C_{SHUNT}	Shunt Capacitance	5	6.5	7.5	pF
R_I	Insulation Resistor	500MΩ Minimum at D.C.100V			

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN.Table 5-6 lists the 32768Hz crystal specifications.

Table 5-6. 32768Hz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	32768	-	Hz
t_{ST}	Startup Time	-	-		ms
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-20	-	+20	ppm
P_{ON}	Drive Level	-	-	1.0	uW
C_L	Equivalent Load Capacitance	-	18	-	pF
R_S	Series Resistance(ESR)	-	-	70	kΩ
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	2	-	fF
C_{SHUNT}	Shunt Capacitance	-	1.1	-	pF
R_I	Insulation Resistor	500MΩ Minimum at D.C.100V			

5.7. External Memory AC Electrical Characteristics

5.7.1. Nand Flash AC Electrical Characteristics

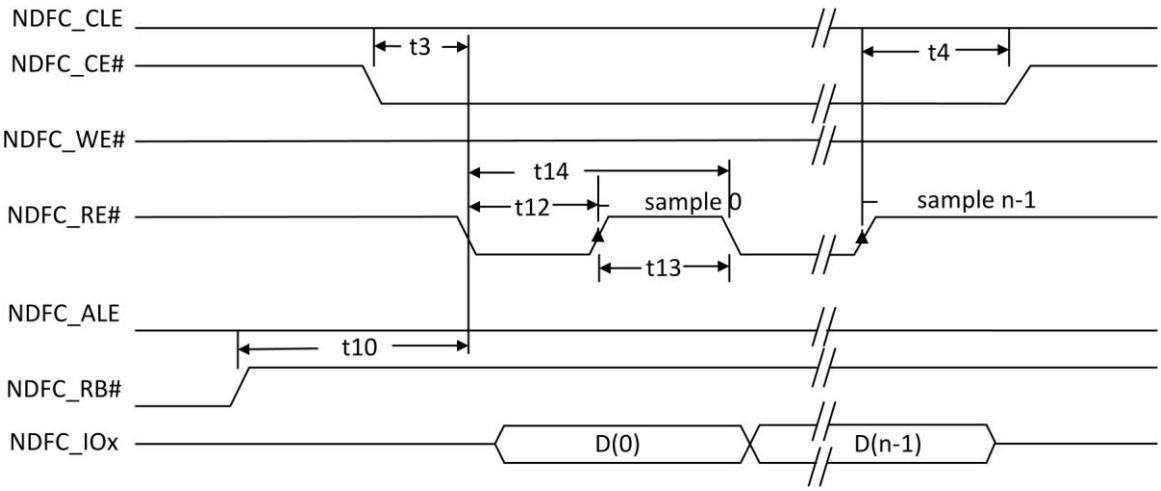


Figure 5-1. Conventional Serial Access Cycle Timing (SAM0)

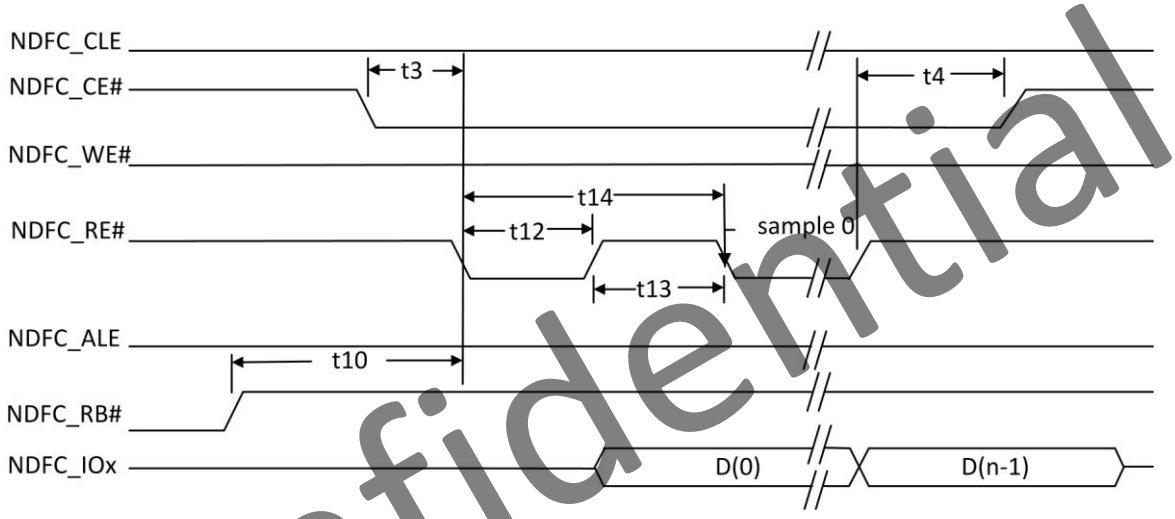


Figure 5-2. EDO Type Serial Access after Read Cycle Timing (SAM1)

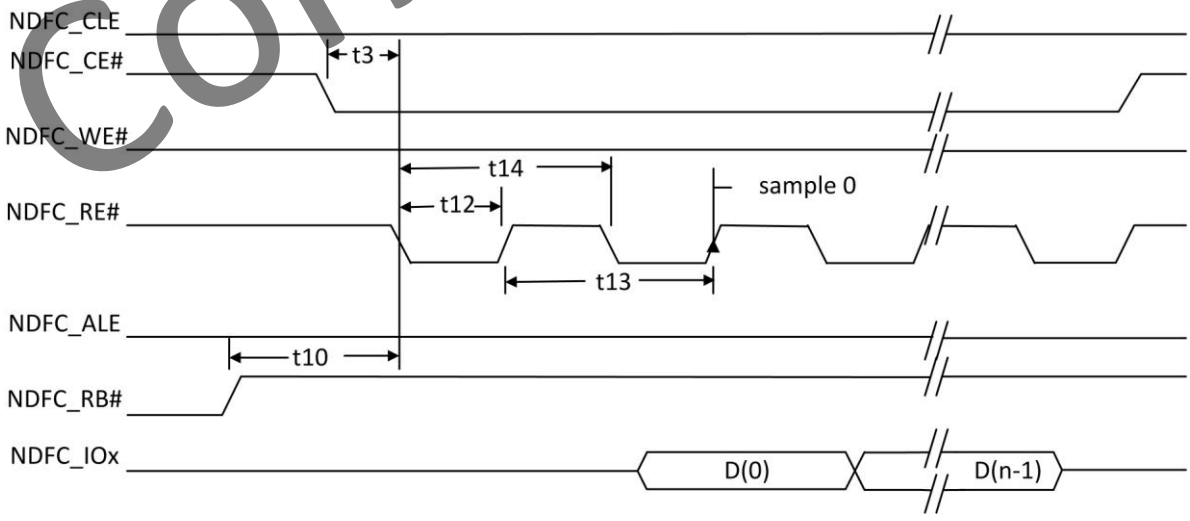


Figure 5-3. Extending EDO Type Serial Access Mode Timing (SAM2)

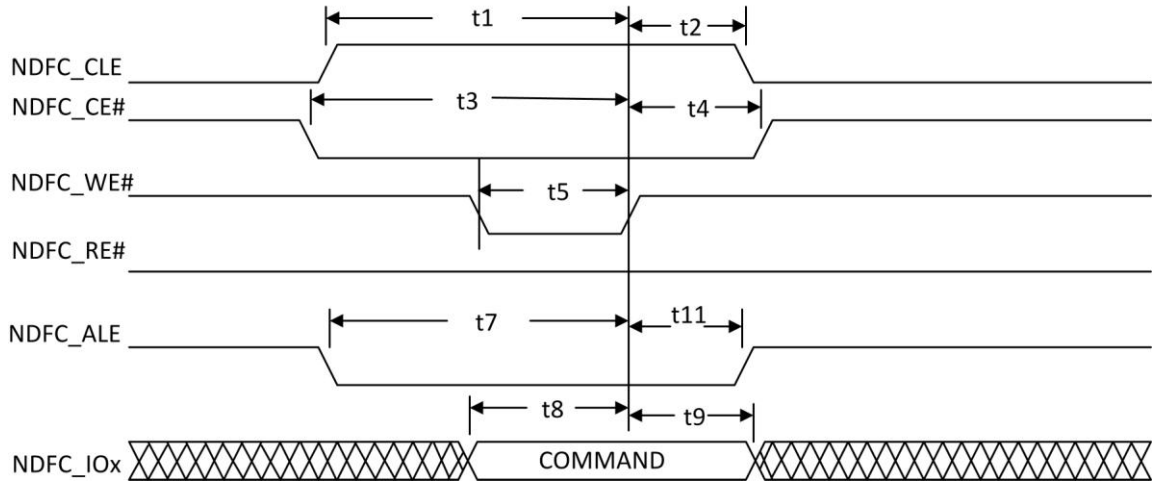


Figure 5-4. Command Latch Cycle Timing

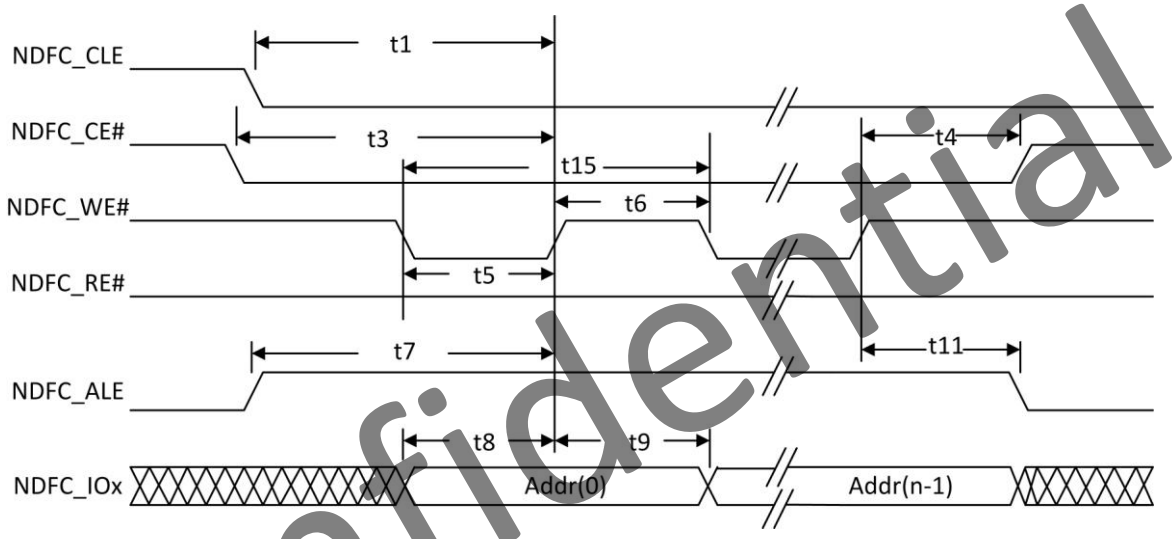


Figure 5-5. Address Latch Cycle Timing

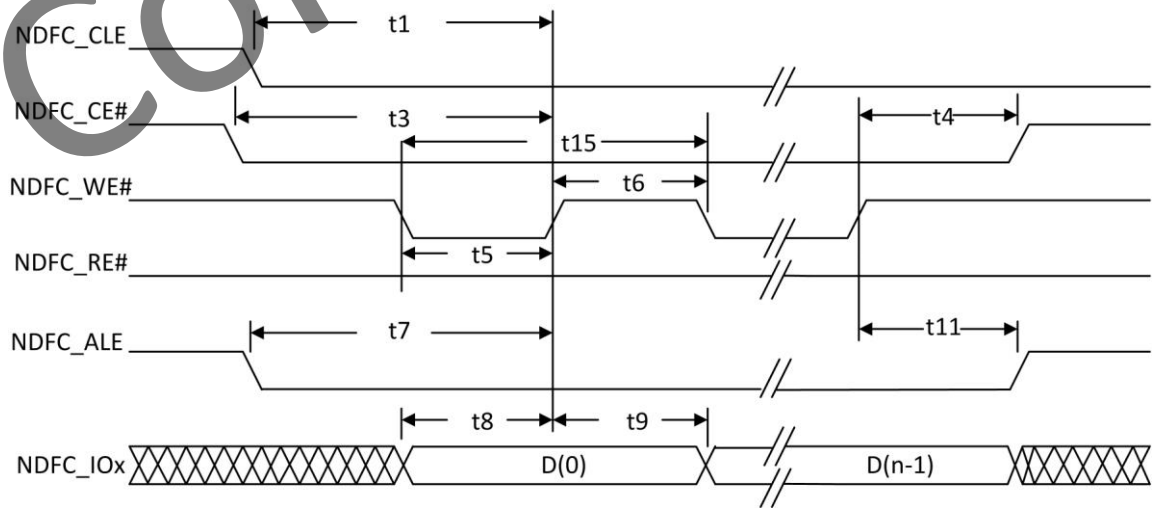


Figure 5-6. Write Data to Flash Cycle Timing

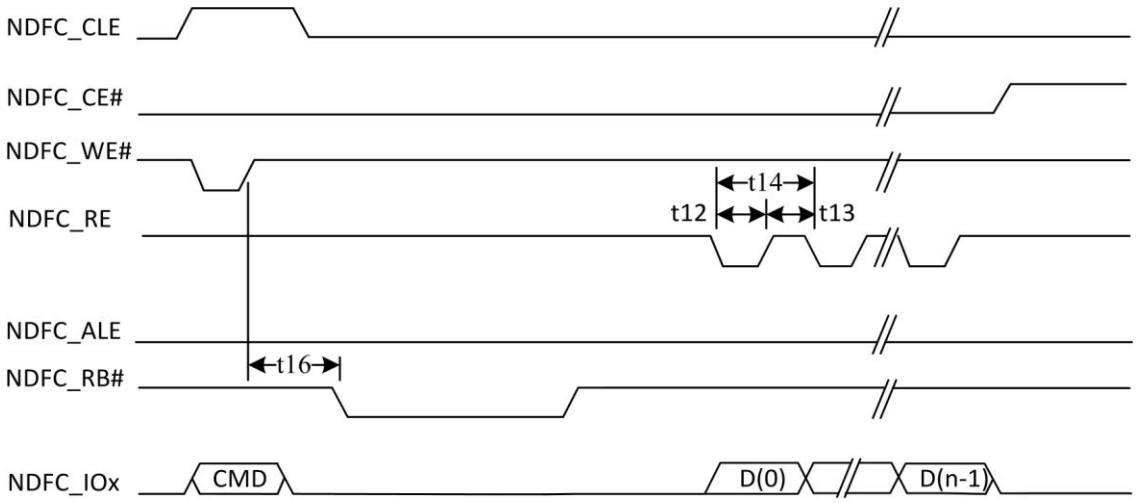


Figure 5-7. Waiting R/B# Ready Timing

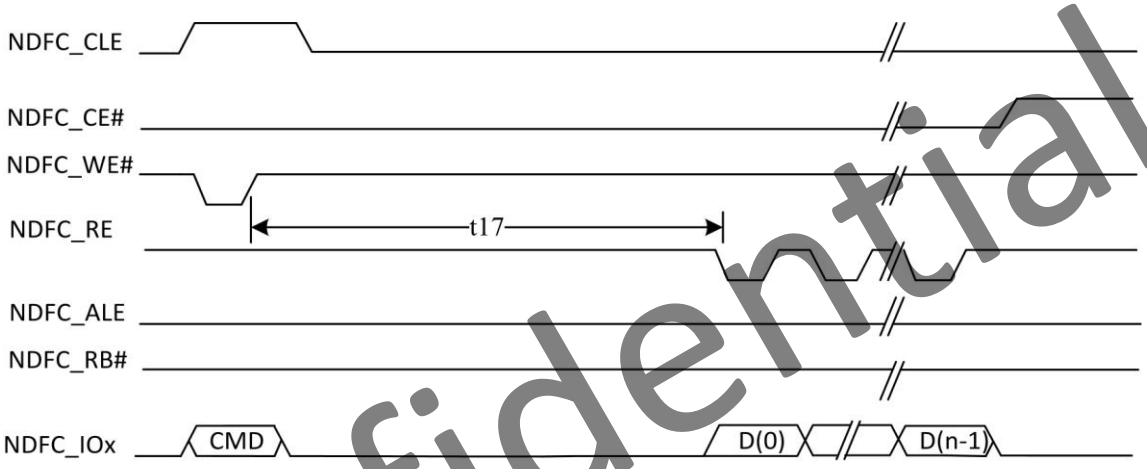


Figure 5-8. WE# High to RE# Low Timing

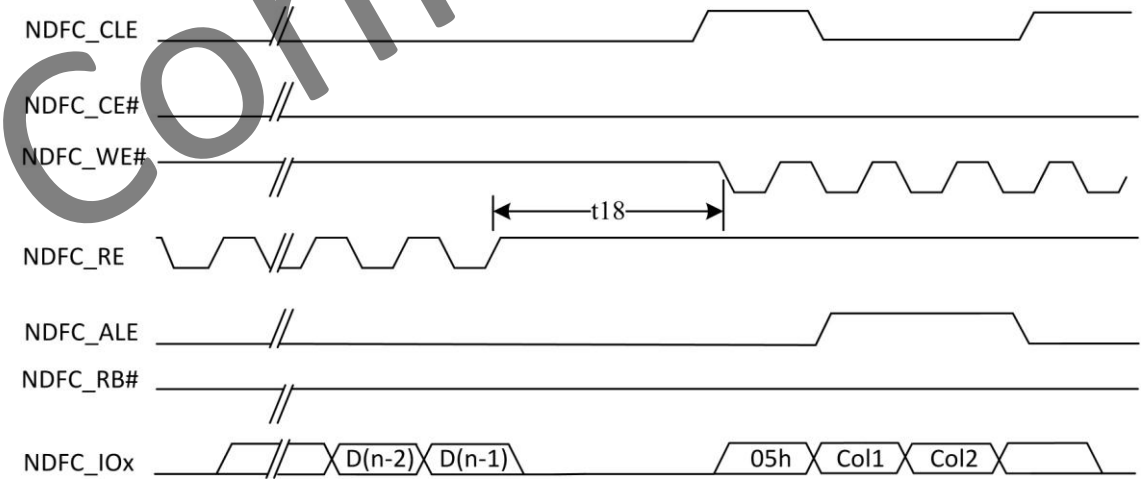


Figure 5-9. RE# High to WE# Low Timing

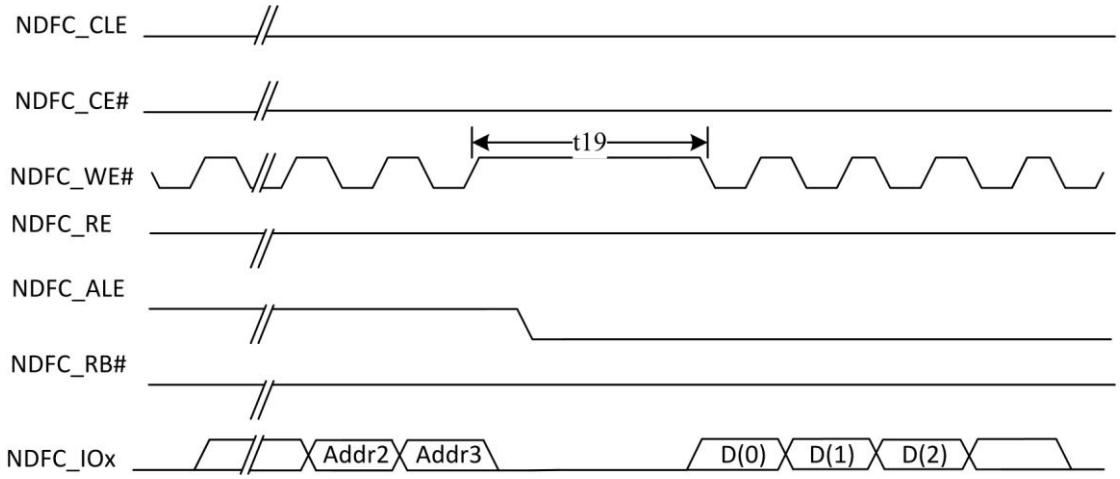


Figure 5-10. Address to Data Loading Timing

Table 5-7. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T(1)	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns
NOTE (1):T is the cycle of clock. **NOTE (2),(3),(4),(5):**This values are configurable in Nand Flash Controller. The value of T_WB could be 28T/44T/60T/76T, the value of T_WHR could be 0T/12T/28T/44T, the value of T_RHW could be 8T/24T/40T/56T, the value of T_ADL could be 0T/12T/28T/44T.			

5.7.2. SMHC AC Electrical Characteristics

5.7.2.1. SMHC0 AC Electrical Characteristics

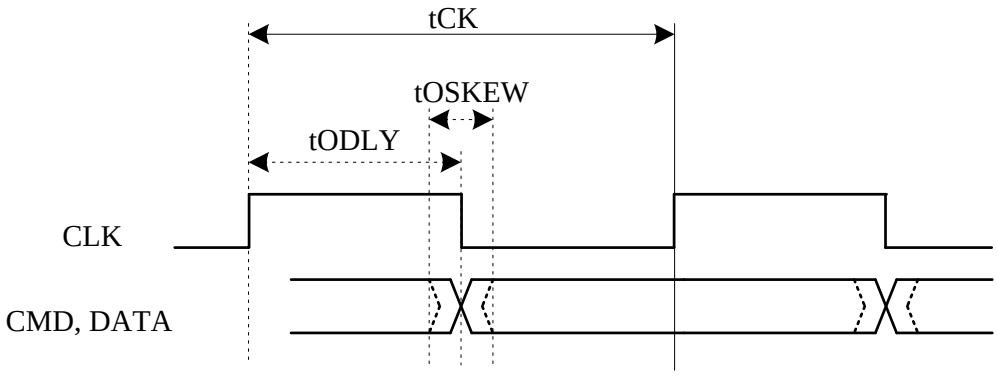


Figure 5-11. SMHC0 Output Timing Diagram in High-Speed Mode

Table 5-8. SMHC0 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

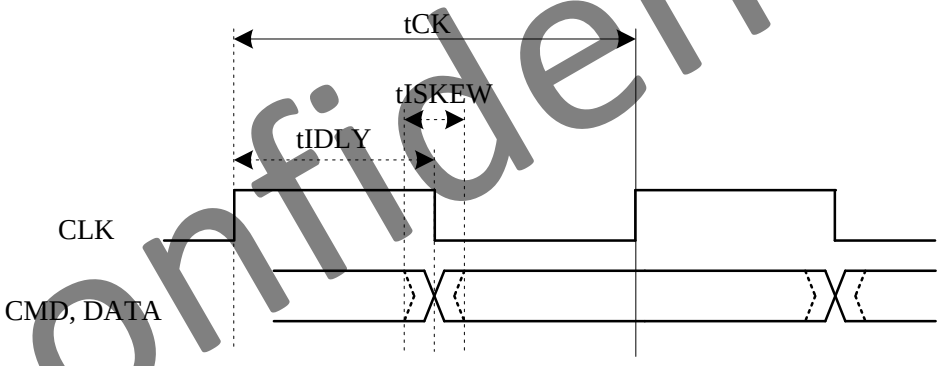


Figure 5-12. SMHC0 Input Timing Diagram in High-Speed Mode

Table 5-9. SMHC0 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	1	ns
The GPIO's driver strength level is 2 for test.					

5.7.2.2. SMHC1 AC Electrical Characteristics

(1) SDR Mode

It is used for DS,HS,SDR12,SDR25,SDR50,SDR104(<100MHz).

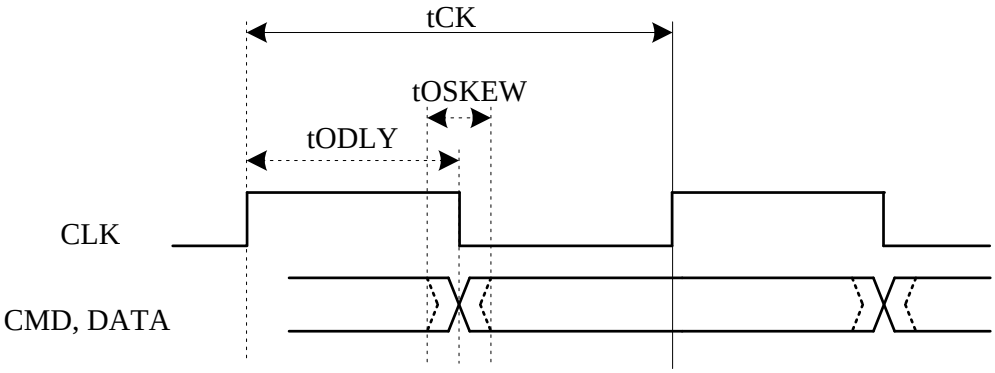


Figure 5-13. SMHC1 Output Timing Diagram in High-Speed Mode

Table 5-10. SMHC1 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

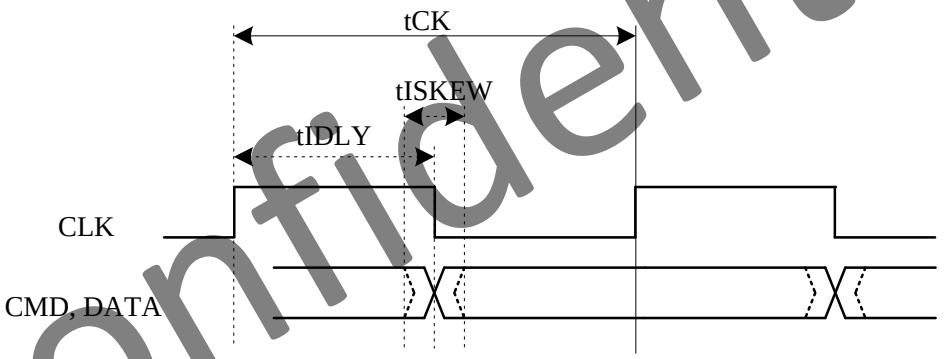


Figure 5-14. SMHC1 Input Timing Diagram in High-Speed Mode

Table 5-11. SMHC1 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	1	ns
The GPIO's driver strength level is 2 for test.					

(2) DDR50 Mode

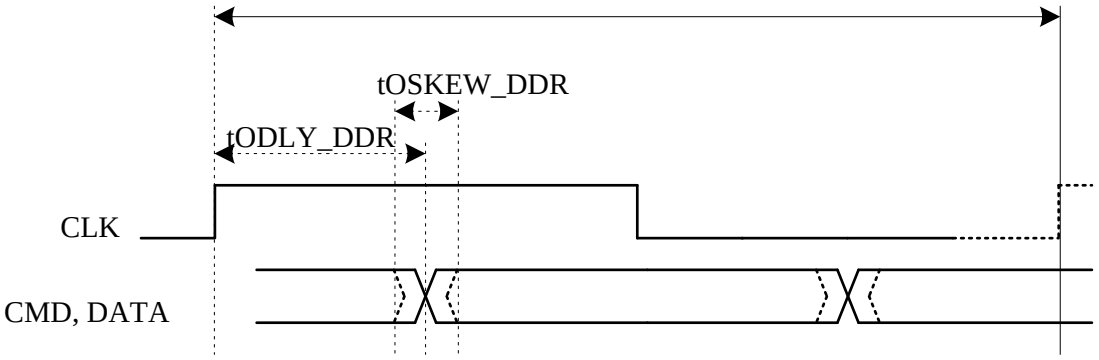


Figure 5-15. SMHC1 Output Timing Diagram in HS-DDR Mode

Table 5-12. SMHC1 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.4	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

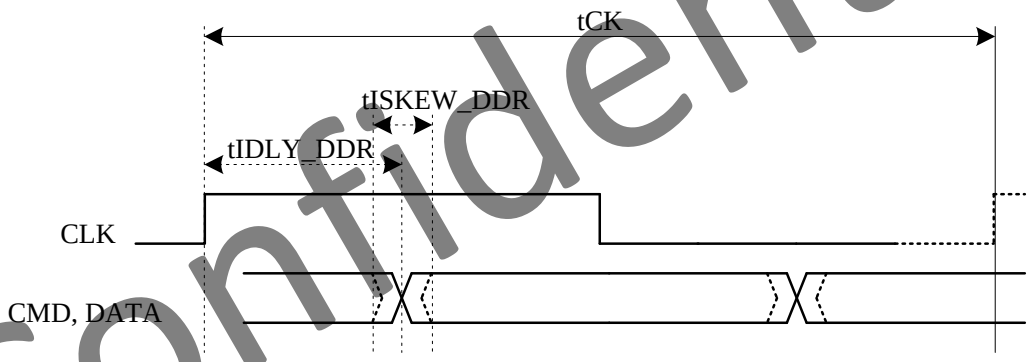


Figure 5-16. SMHC1 Input Timing Diagram in HS-DDR Mode

Table 5-13. SMHC1 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	7	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.4	ns
The GPIO's driver strength level is 2 for test.					

(3) SDR104 Mode(>100MHz)

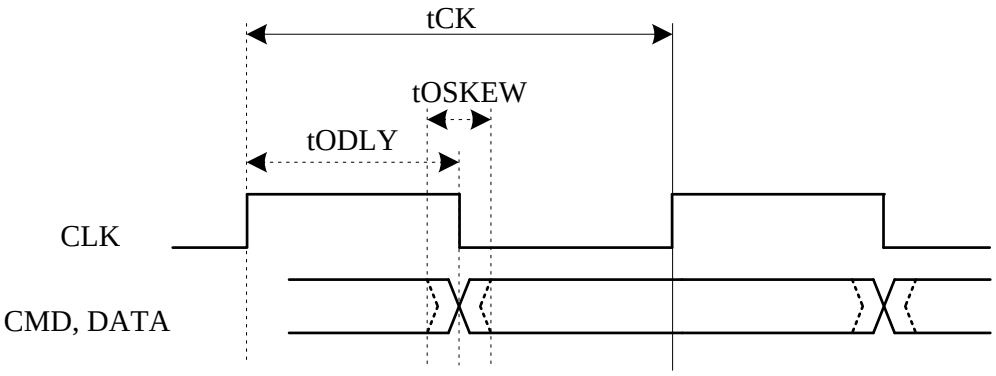


Figure 5-17. SMHC1 Output Timing Diagram in High-Speed Mode

Table 5-14. SMHC1 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.4	ns
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.					

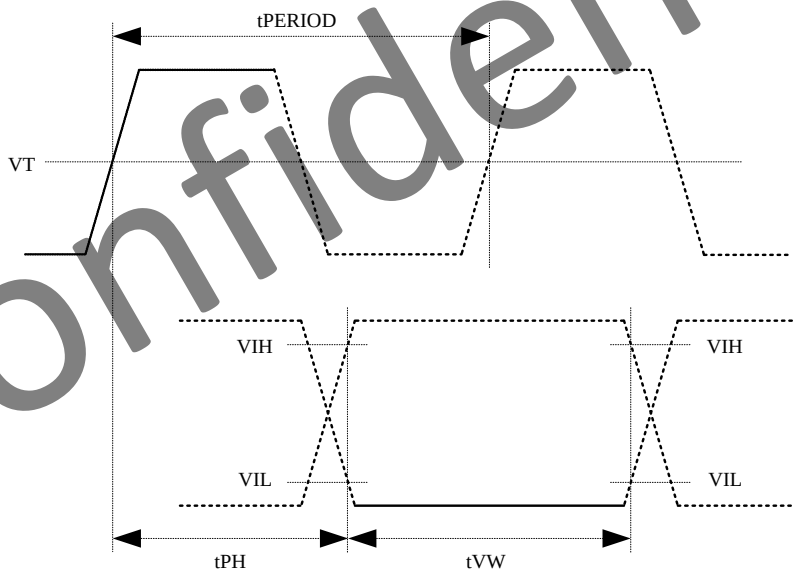


Figure 5-18. SMHC1 Input Timing Diagram in High-Speed Mode

Table 5-15. SMHC1 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
(1).Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz.						

(2).The GPIO's driver strength level is 3 for test.
(3).Temperature variation: -20°C.
(4).Temperature variation: 90°C.

5.7.2.3. SMHC2 AC Electrical Characteristics

(1) HS-SDR/HS-DDR Mode

The IO voltage is 1.8V or 3.0V.

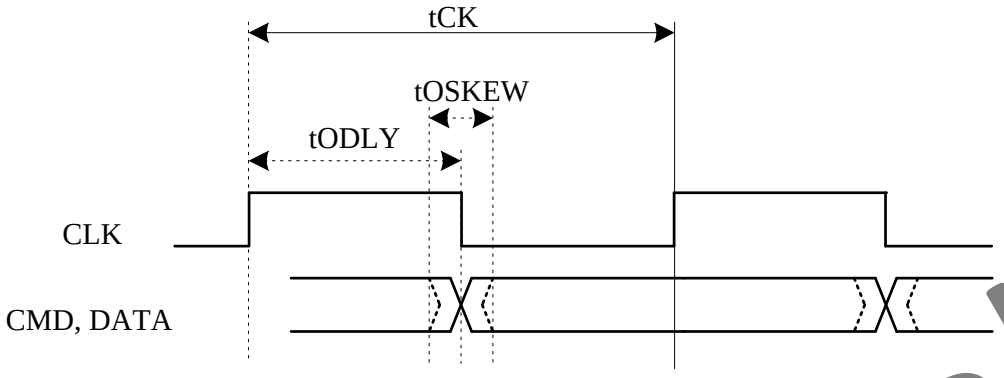


Figure 5-19. SMHC2 Output Timing Diagram in HS-SDR Mode

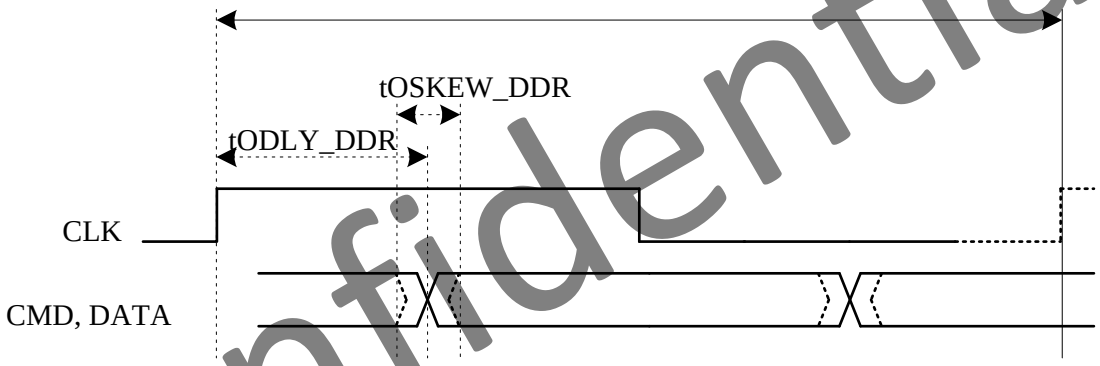


Figure 5-20. SMHC2 Output Timing Diagram in HS-DDR Mode

Table 5-16. SMHC2 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-	0.4	ns	
(1).Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. (2).The GPIO's driver strength level is 2 for test.						

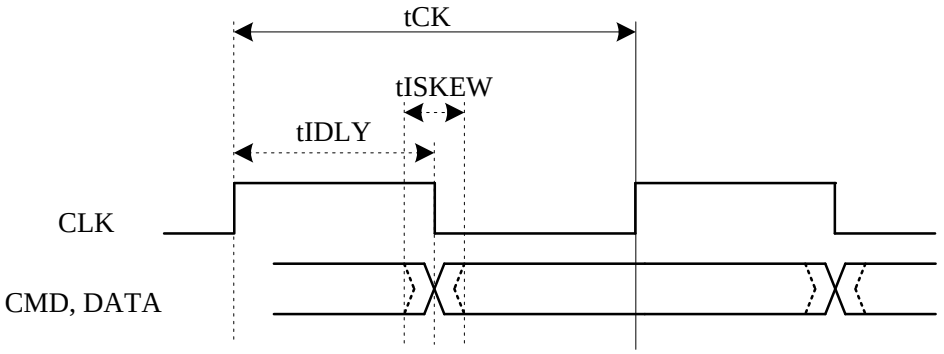


Figure 5-21. SMHC2 Input Timing Diagram in HS-SDR Mode

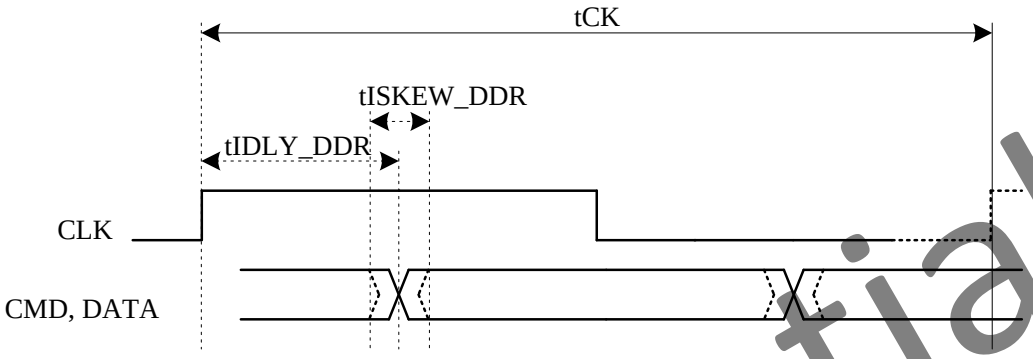


Figure 5-22.SMHC2 Input Timing Diagram in HS-DDR Mode

Table 5-17. SMHC2 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty Cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	21	ns	
Data input delay in DDR mode.It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	8	ns	
Data input skew time in SDR mode	tISKEW	-	-	1.7	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.5	ns	
The GPIO's driver strength level is 2 for test.						

(2) HS200 Mode

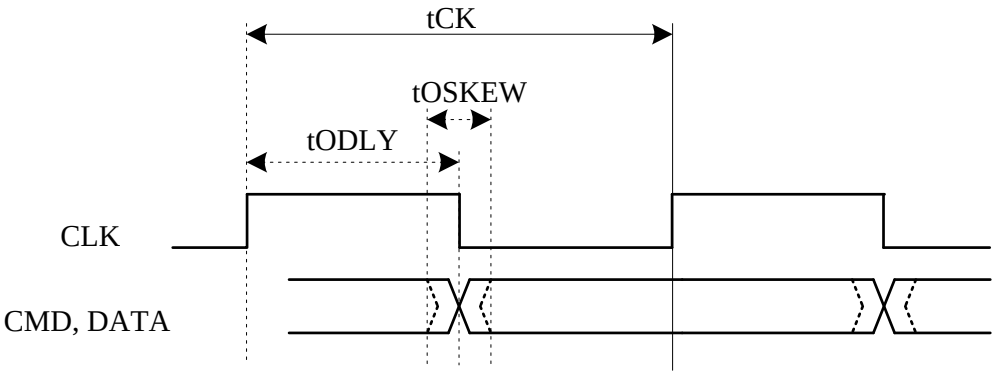


Figure 5-23. SMHC2 HS200 Output Timing Diagram

Table 5-18. SMHC2 HS200 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-	0.4	ns	
(1).Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. (2).The GPIO's driver strength level is 3 for test.						

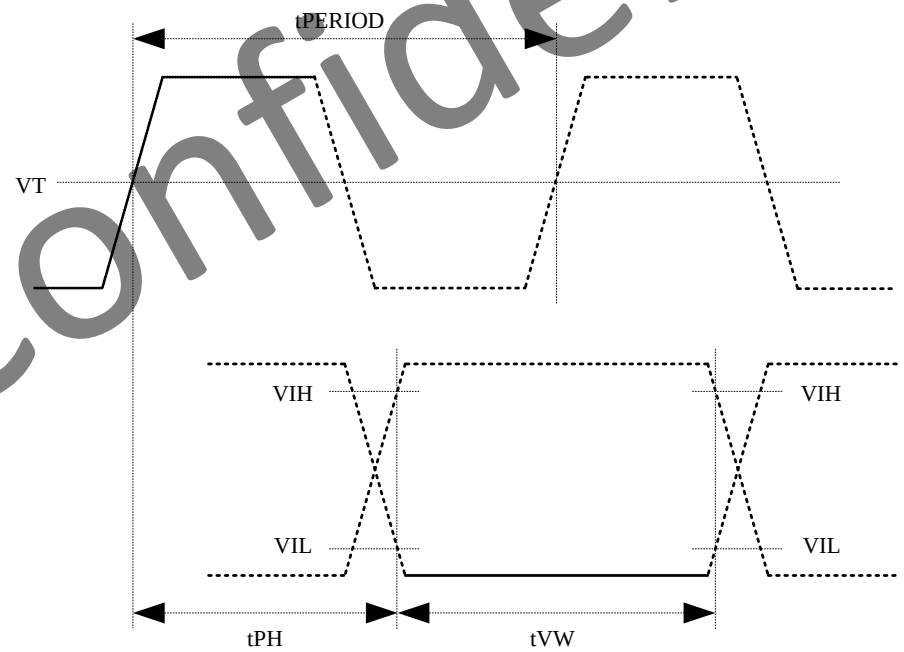


Figure 5-24. SMHC2 HS200 Input Timing Diagram

Table 5-19. SMHC2 HS200 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	

Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
(1).Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. (2).The GPIO's driver strength level is 3 for test. (3).Temperature variation: -20°C. (4).Temperature variation: 90°C.						

(3) HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

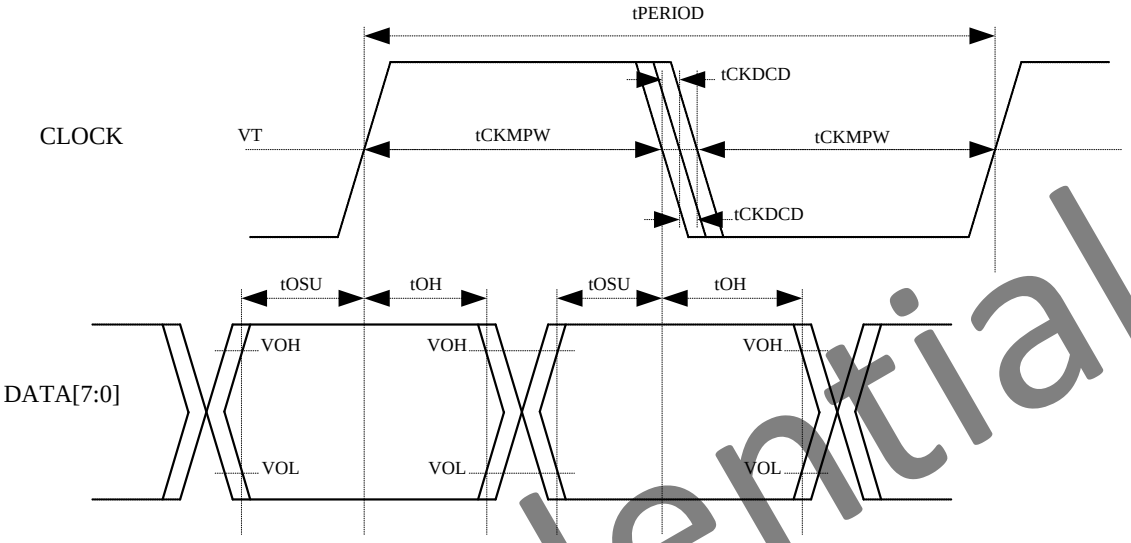


Figure 5-25. SMHC2 HS400 Output Timing Diagram

Table 5-20. SMHC2 HS400 Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output CMD, DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	
(1).Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. (2).The GPIO's driver strength level is 3 for test.						

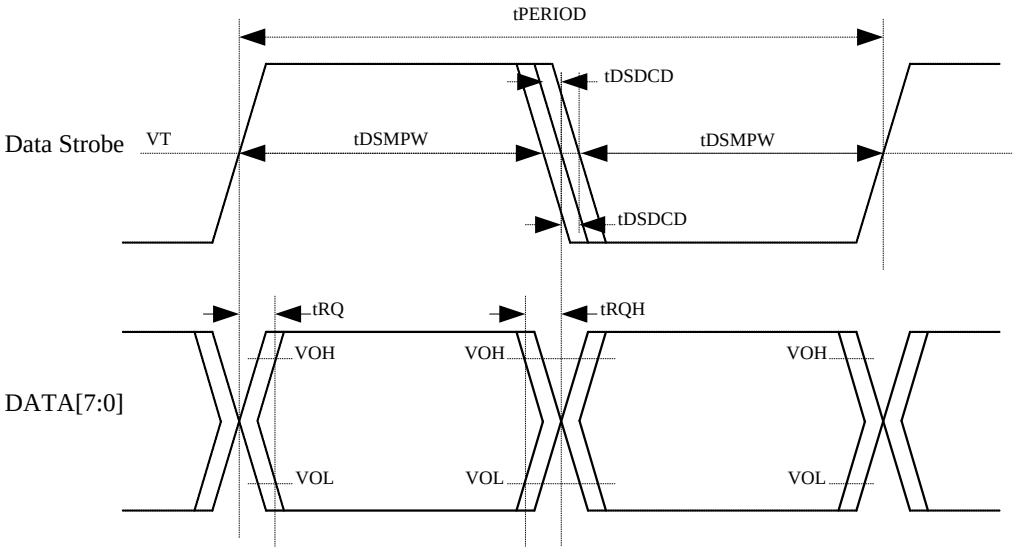


Figure 5-26. SMHC2 HS400 Input Timing Diagram

Table 5-21. SMHC2 HS400 Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Input DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
(1).Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. (2).The GPIO's driver strength level is 3 for test.						

5.8. External Peripheral AC Electrical Characteristics

5.8.1. LCD AC Electrical Characteristics

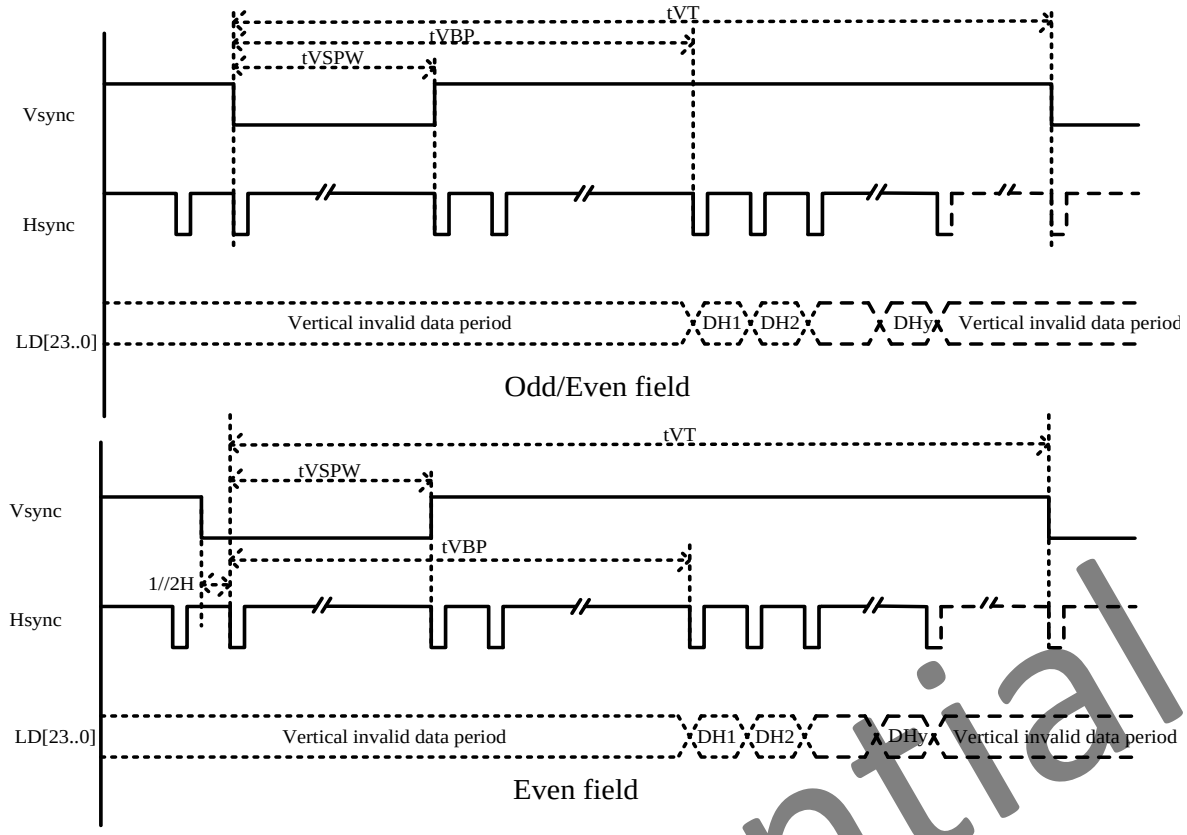


Figure 5-27. HV_IF Interface Vertical Timing

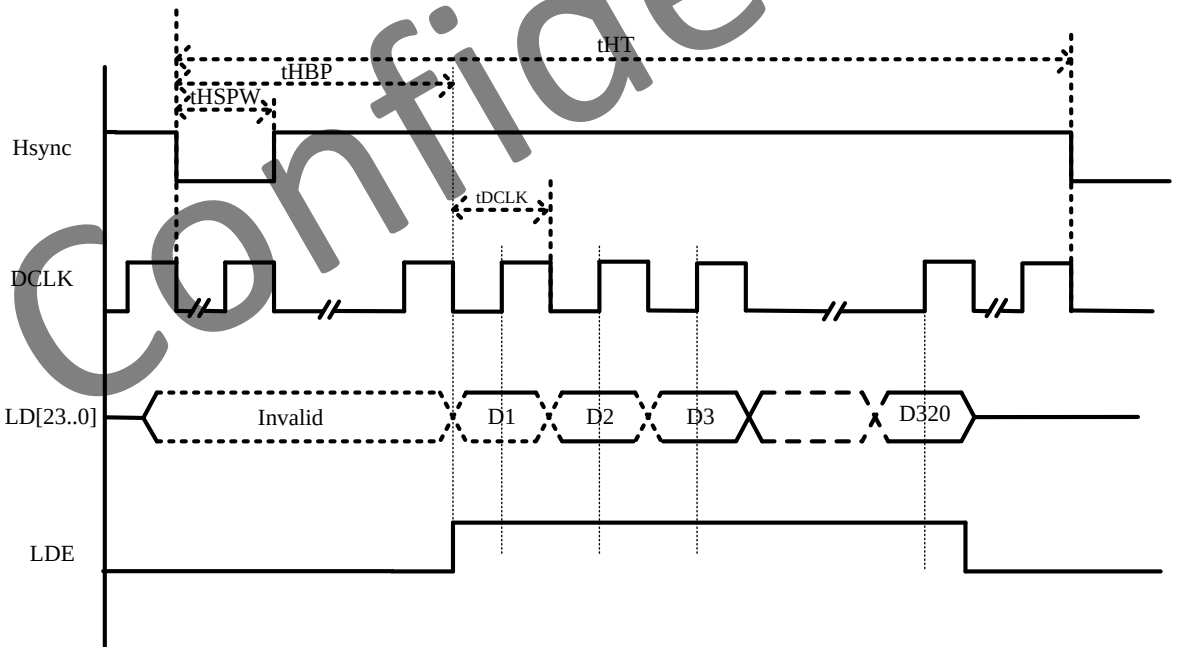


Figure 5-28. HV_IF Interface Parallel Mode Horizontal Timing

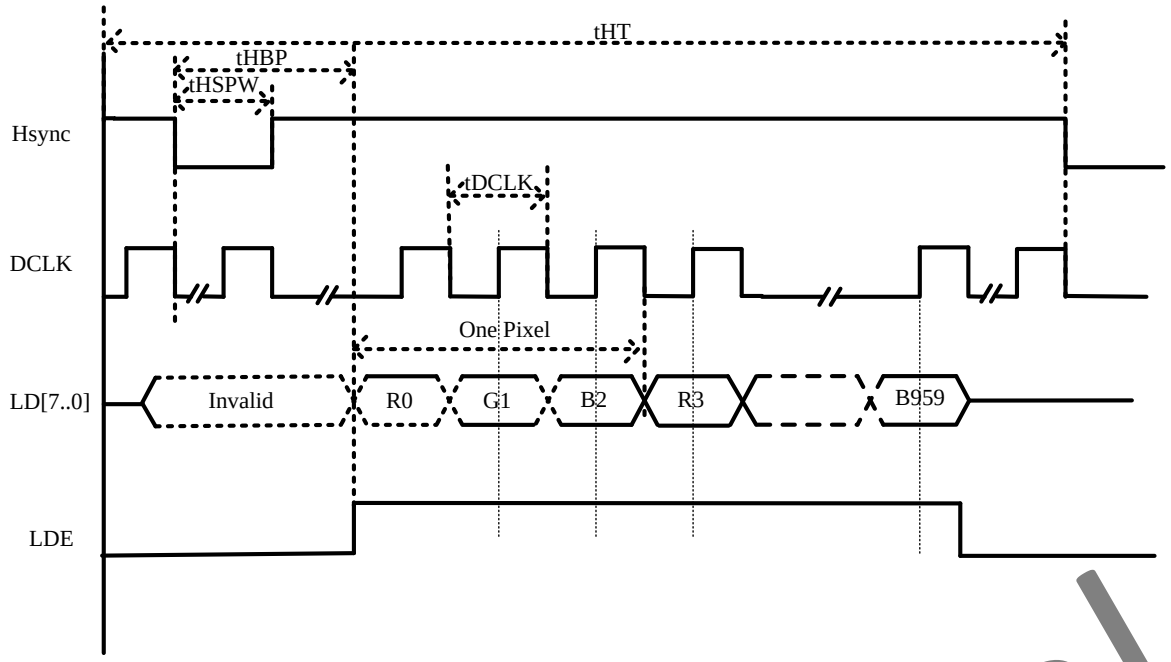


Figure 5-29. HV_IF interface Serial Mode Horizontal Timing

Table 5-22. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT
(1). Vsync: Vertical sync, indicates one new frame (2). Hsync: Horizontal sync, indicate one new scan line (3). DCLK: Dot clock, pixel data are sync by this clock (4). LDE: LCD data enable (5). LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel					

5.8.2. CSI AC Electrical Characteristics

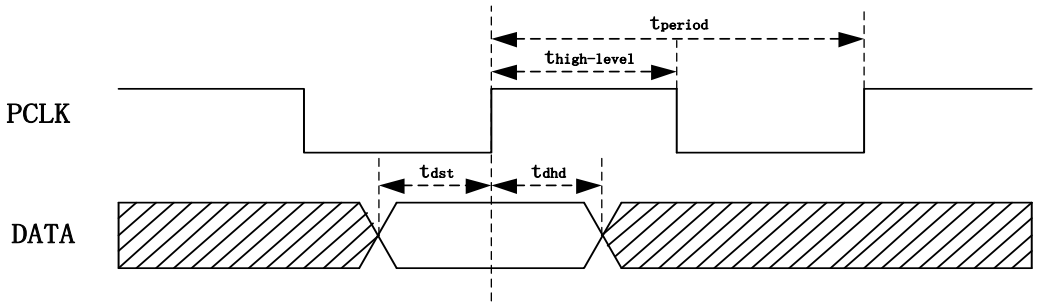


Figure 5-30. CSI Data Sample Timing

Table 5-23. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk Period	t_{period}	6.73	-	-	ns
Pclk Frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk Duty	$t_{high-level}/t_{period}$	40	50	60	%

Data input Setup time	t_{dst}	0.6	-	-	ns
Data input Hold time	t_{dhd}	0.6	-	-	ns

5.8.3. SPI AC Electrical Characteristics

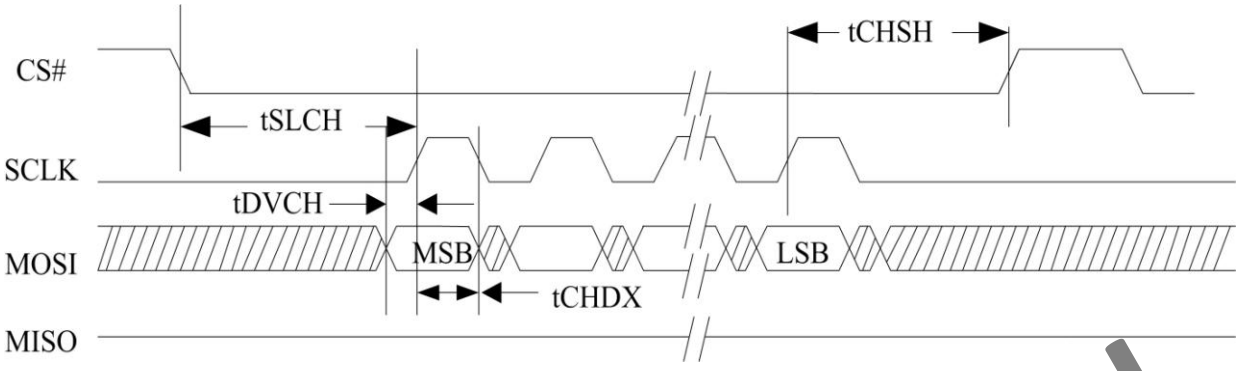


Figure 5-31. SPI MOSI Timing

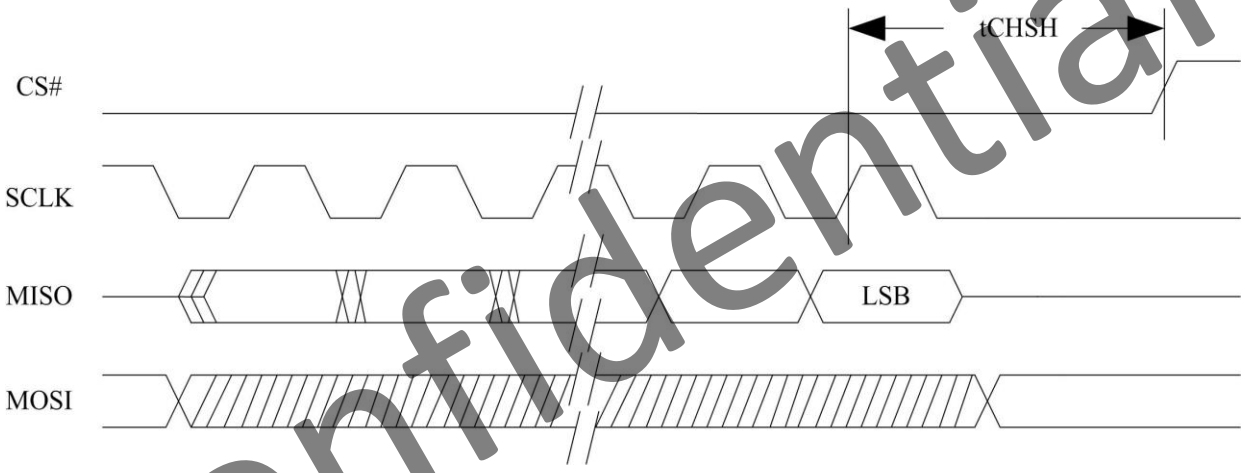


Figure 5-32. SPI MISO Timing

Table 5-24. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	tSLCH	-	2T	-	ns
CS# Active Hold Time	tCHSH	-	2T(1)	-	ns
Data In Setup Time	tDVCH	-	T/2-3	-	ns
Data In Hold Time	tCHDX	-	T/2-3	-	ns
NOTE (1):T is the cycle of clock.					

5.8.4. UART AC Electrical Characteristics

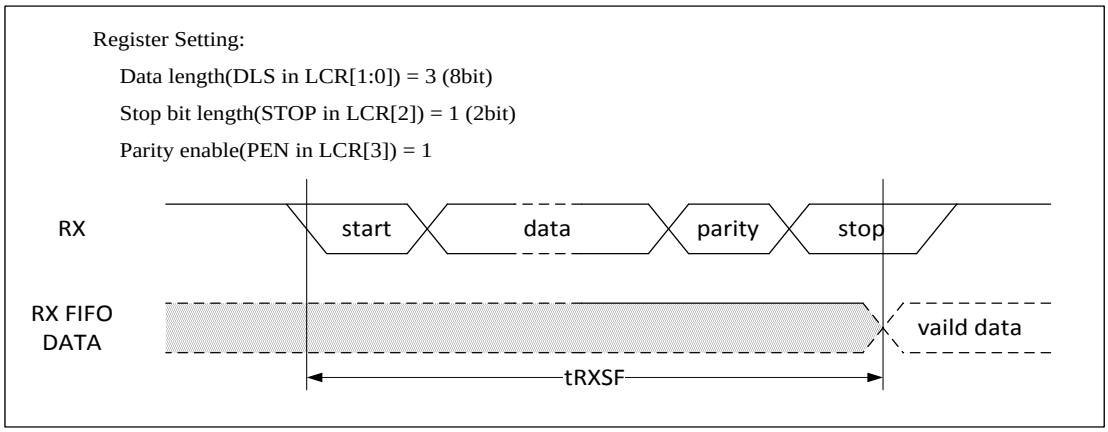


Figure 5-33. UART RX Timing

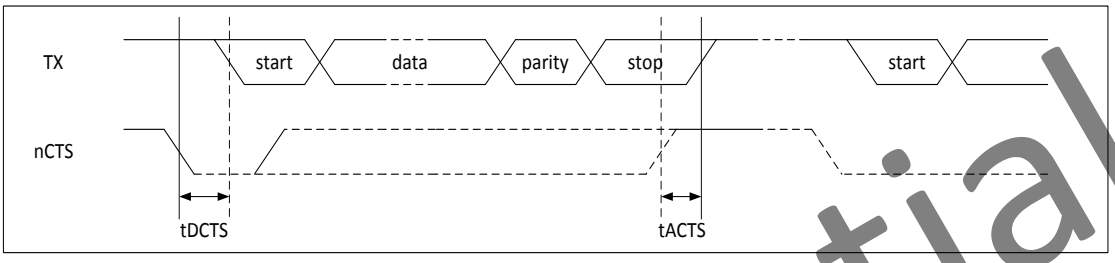


Figure 5-34. UART nCTS Timing

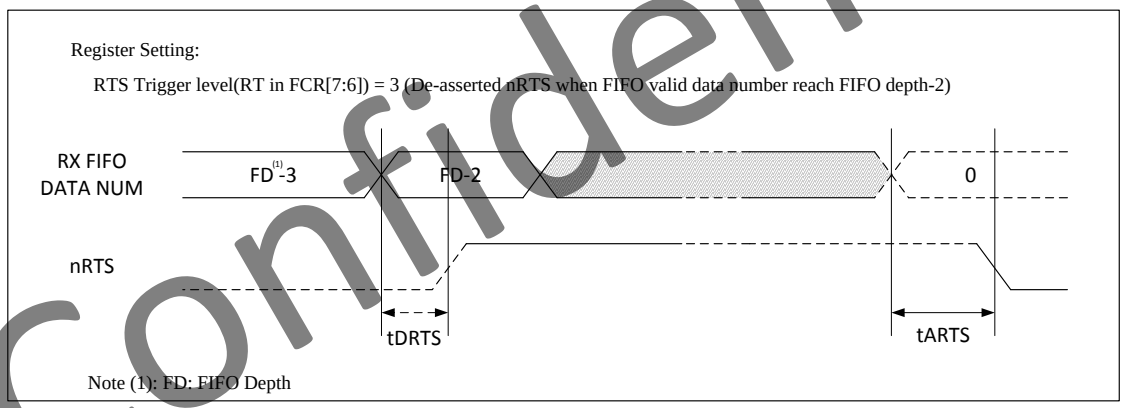


Figure 5-35. UART nRTS Timing

Table 5-25. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
NOTE (1): BRP(Baud-Rate Period).					

5.8.5. TWI AC Electrical Characteristics

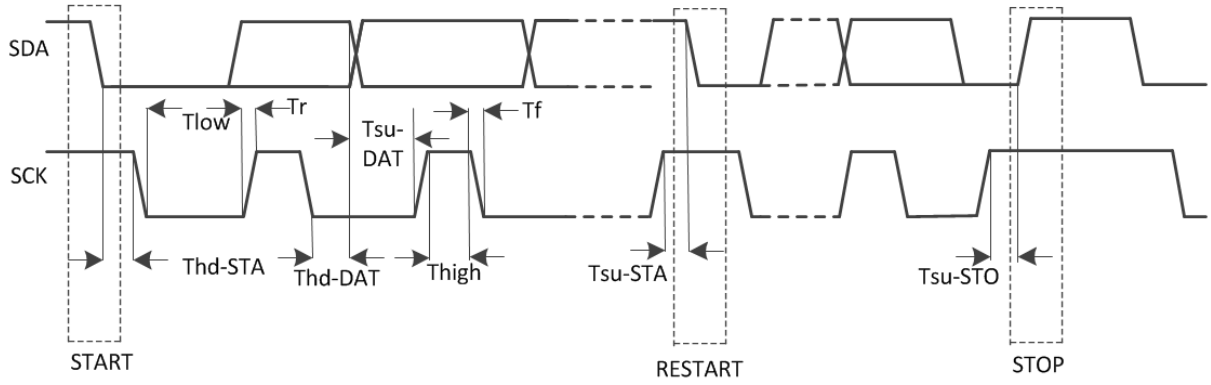


Figure 5-36. TWI Timing

Table 5-26. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK Clock Frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	5.0	-	-	-	ns
Setup Time In Stop	Tsu-STO	4.0	-	6.0	-	us
SCK Low Level Time	Tlow	4.7	-	1.3	-	us
SCK High Level Time	Thigh	4.0	-	0.6	-	ns
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.8.6. I2S/PCM AC Electrical Characteristics

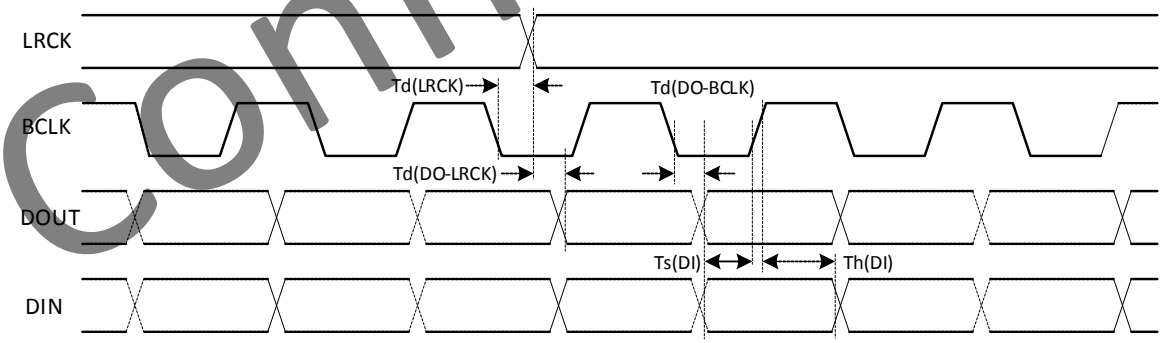


Figure 5-37. I2S/PCM Timing in Master Mode

Table 5-27. I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Delay	T_d(LRCK)			10	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)			10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)			10	ns
DIN Setup	T_s(DI)	4			ns
DIN Hold	T_h(DI)	4			ns
BCLK Rise Time	T_r			8	ns
BCLK Fall Time	T_f			8	ns

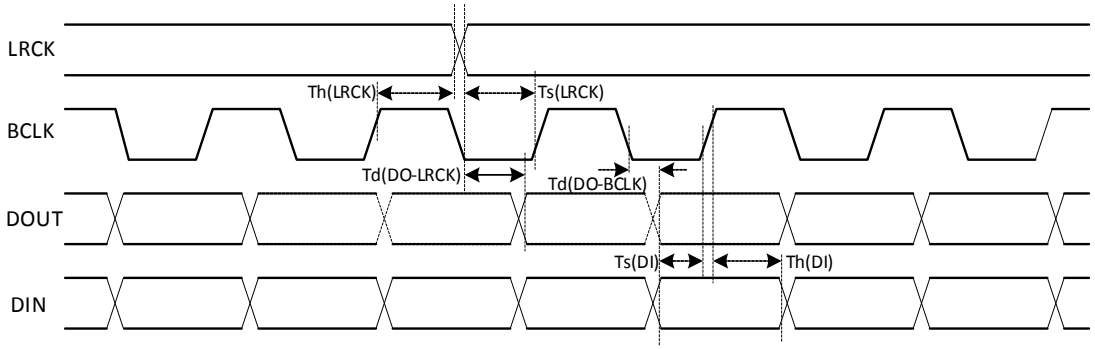


Figure 5-38. I2S/PCM Timing in Slave Mode

Table 5-28. I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Setup	T_s(LRCK)	4			ns
LRCK Hold	T_h(LRCK)	4			ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)			10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)			10	ns
DIN Setup	T_s(DI)	4			ns
DIN Hold	T_h(DI)	4			ns
BCLK Rise Time	T_r			4	ns
BCLK Fall Time	T_f			4	ns

5.8.7. DMIC AC Electrical Characteristics

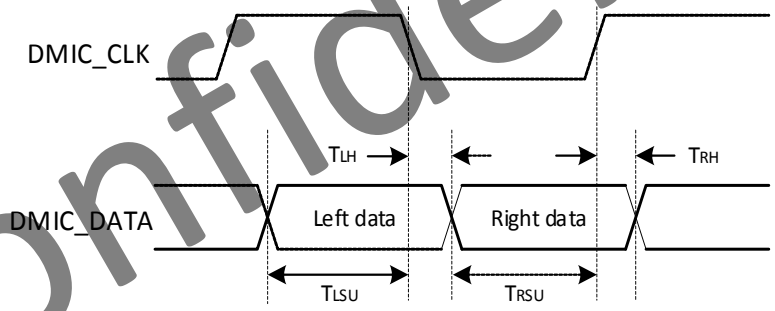


Figure 5-39. DMIC Timing

Table 5-29. DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Left) setup time to falling DMIC_CLK edge	TLSU	15			ns
DMIC_DATA(Left) hold time from falling DMIC_CLK edge	TLH	0			ns
DMIC_DATA(Right) setup time to rising DMIC_CLK edge	TRSU	15			ns
DMIC_DATA(Right) hold time from rising DMIC_CLK edge	TRH	0			ns

5.9. Power-On and Power-Off Sequence

The section provides information about the A63 power on and power off sequence requirements.

5.9.1. Power-On Sequence

Figure 5-40 shows an example of the power on sequence for the A63 device. The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- VCC-RTC should remain powered on continuously, to maintain internal real-time clock status. Otherwise, it has to

be powered on together with VDD-CPUS and VDD-SYS, or preceding VDD-CPUS and VDD-SYS.

- VDD-CPUS should be powered on together, or any time after VCC-RTC.
- VDD-SYS should be powered on together, or any time after VCC-RTC.
- 32K clock need to start oscillating and be stable.
- Other power domains can ramp after VDD-SYS and VDD-CPUS are stabilized.
- During the entire power on sequence, the RESET pin must be held on low until 32K clock and all power domains are stable.

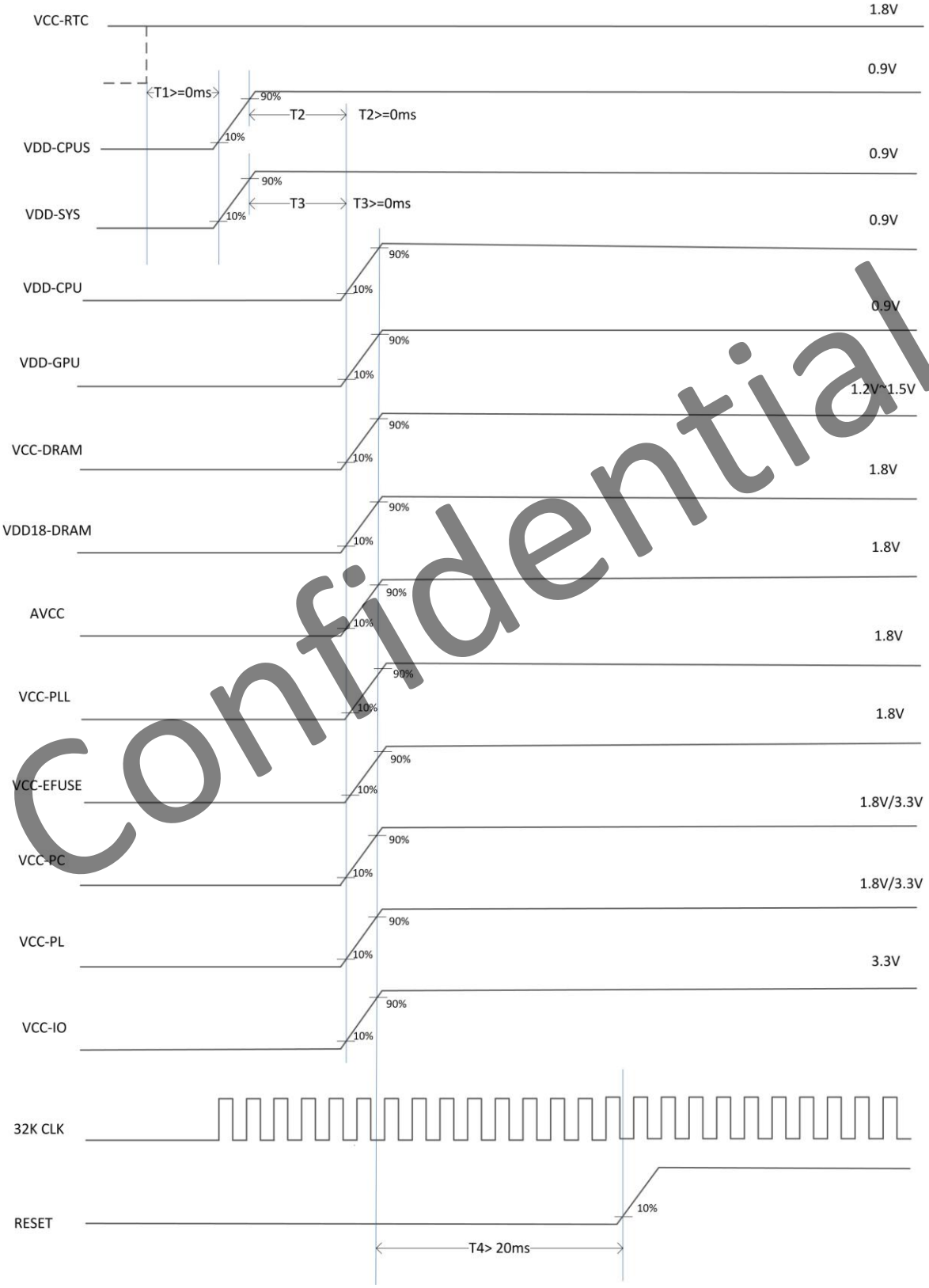


Figure 5-40. Power On Timing

5.9.2. Power-Off Sequence

The following steps give an example of the power off sequence supported by the A63 device. Figure 5-41 shows an example of the device power off sequence.

- Reset A63 device.
- VCC-RTC holds high.
- After PMIC receives the power-down command, pull-down RESET#.
- After T5, other powers ramp down at the same time, and the ramp rate of each power rail is generally determined by the load on that power.

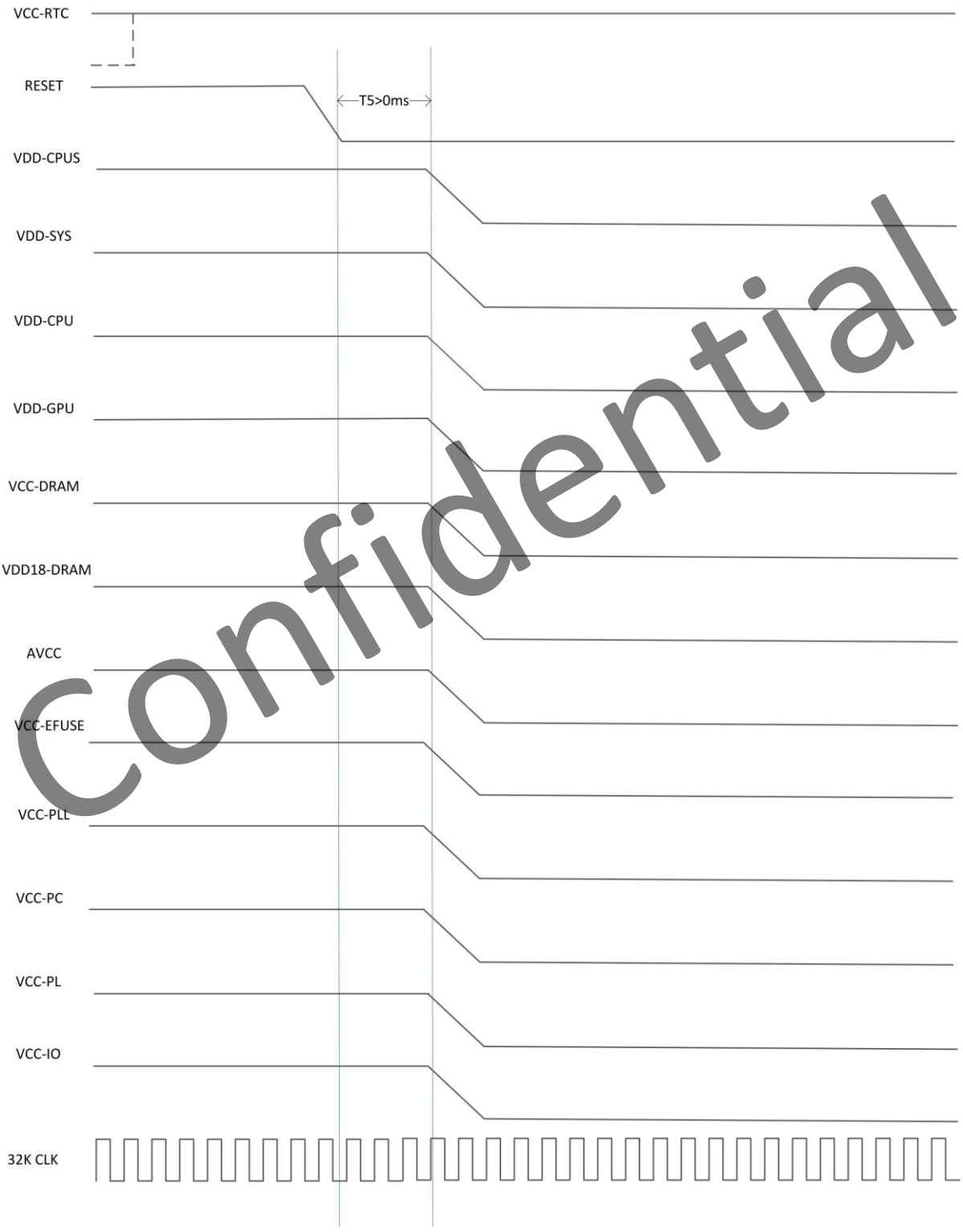


Figure 5-41. Power Off Timing

6. Package Thermal Characteristics

Table 6-1 shows thermal resistance parameters of the A63. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51 , the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board(2s2p),natural convection, no air flow.

Table 6-1. A63 Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	21.3	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	11.58	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	7.09	-	°C/W

7. Reflow Profile

Reflow profile conditions of the A63 processor are given in Table 7-1. The table is for reference only.

Table 7-1. A63 Reflow Profile Conditions

Profile Stage	Description	Symbol	High Temperature Condition Limits
Preheat	Initial ramp temperature range	A	25°C to 150°C
	Initial ramp rate	B	< 3°C/s
Soak	Soak temperature range	C	150°C to 180°C
	Soak time	D	40s to 60s
Reflow	Liquidus temperature	E	217°C
	Time above liquidus	F	60s to 90s
	Peak temperature	G	235°C to 250°C
Cool down	Cool down temperature rate	H	> -4°C/s

Figure 7-1 shows the typical reflow profile of the A63 processor.

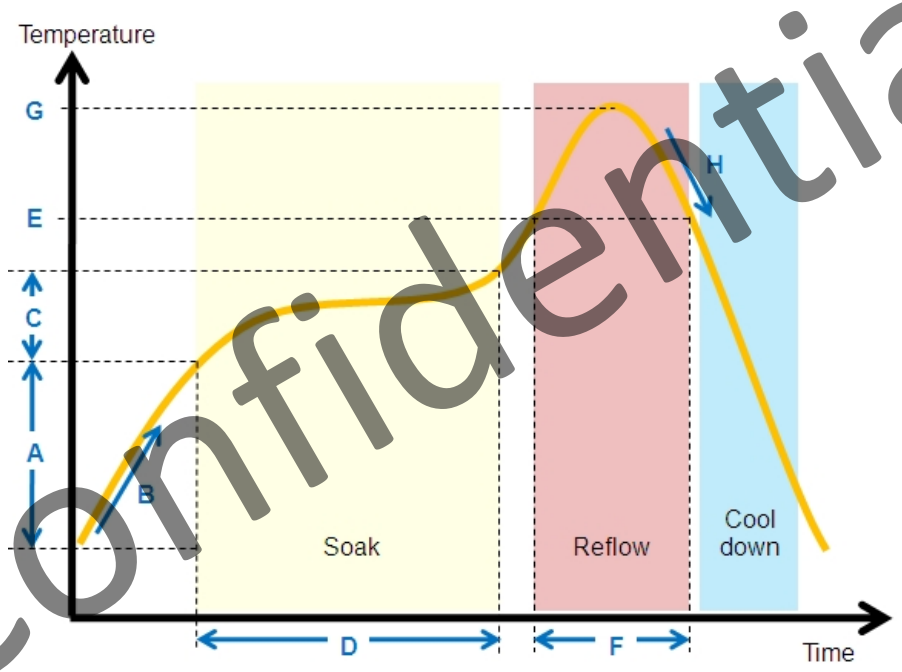


Figure 7-1. A63 Typical Reflow Profile

8. Pin Assignment

8.1. Pin Map

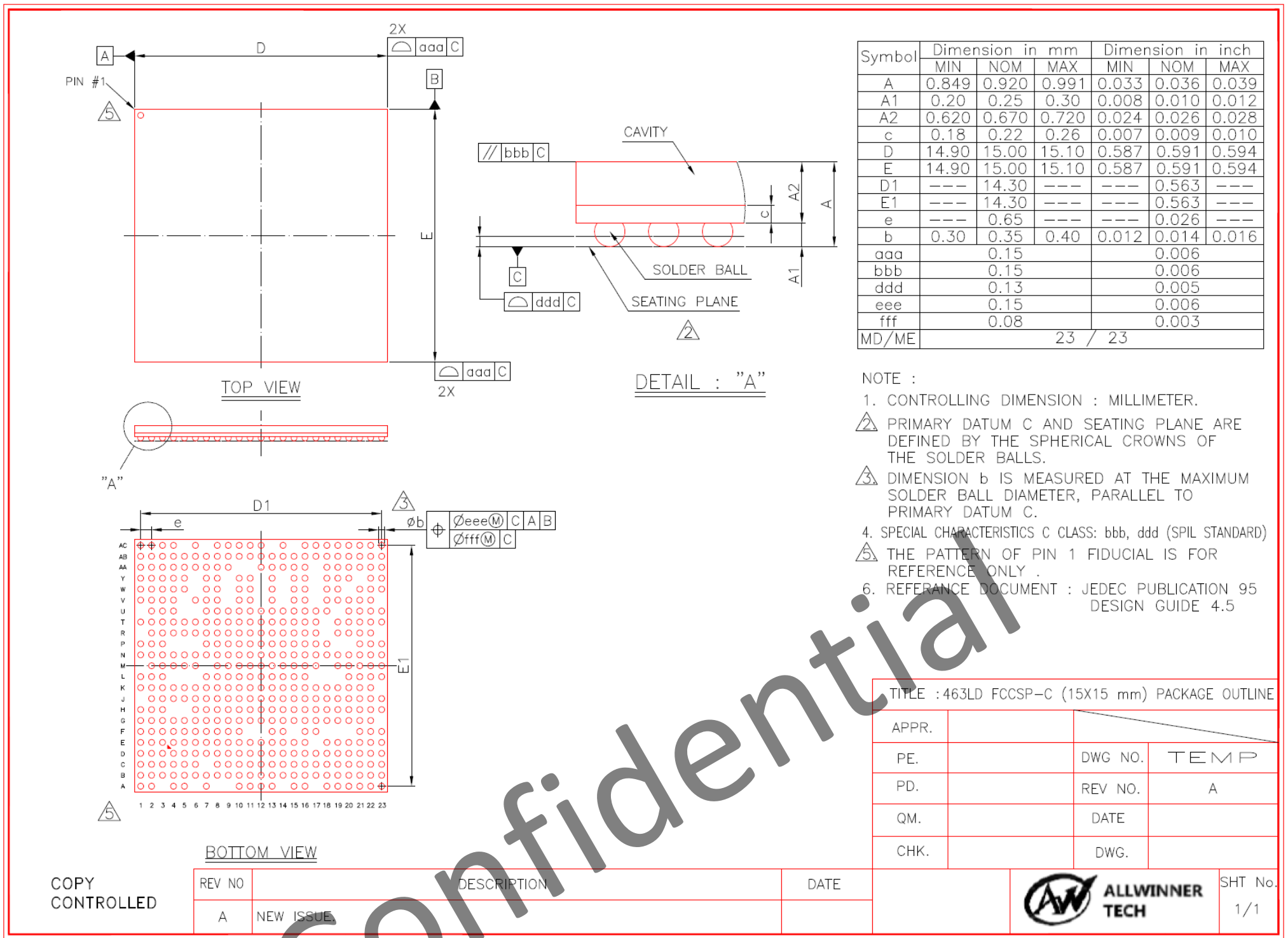
For A63, FBGA 463 balls, 15mm x 15mm,0.65mm pitch package is offered. The pin maps are illustrated in Figure 8-1 for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	GND	DSI1-DP3		DSI1-DN1	DSI1-DP1		DSI0-DP2			DSI0-DP0	GND	USB1-DM	USB0-DM		SPKLN	LINEINR		MICIN1P	MICIN2P	MICIN3P	GND	REFCLK_OUT	GND
B	GND	DSI1-DN3	DSI1-DN2	DSI1-CKN	DSI1-DP0	DSI0-DP3	DSI0-DN2	DSI0-CKP	DSI0-DP1	DSI0-DN0	BOOT-SEL0	USB1-DP	USB0-DP	HPOUTR	SPKLP	LINEINL	LINEOUTR	MICIN1N	MICIN2N	MICIN3N	WREQIN	DXIN	DXOUT
C	EDPAUXN	EDPAUXP	DSI1-DP2	DSI1-CKP	DSI1-DN0	DSI0-DN3		DSI0-CKN	DSI0-DN1	GND	VCC-USB	GND	HPOUTFB	HPOUTL	VRA2	SPKRN	LINEOUTL	MIC-DET	REXT	GND	DXVCCIO	DXLDO_OUT	X32KOUT
D	EDPTX3N	EDPTX3P	GND	GND	GND	VCC-DSI	VCC-DSI	GND	GND	GPADC	GND	CPVEE	HP-DET	MBIAS	VRP	SPKRP	PHONEINP	PHONEINN	NMI	X32KFOUT	VCC-RTC	X32KIN	GND
E	EDPTX2N	EDPTX2P	GND	GND-EDP	GND	GND	GND	GND	GND	NC	CPVDD	UBOOT	CPVIN	VPP	HBIAS	AGND		GND	TEST	RTC-VIO	RESET	PM1	PM2
F	EDPTX1N	EDPTX1P	GND	VCC-EDP	EDPHPD	GND	GND	GND	GND	GND			GND	VEE		AVCC	GND				PM3	PM0	PM4
G	EDPTX0N	EDPTX0P	GND	PF4	PF3	VCC-PF	GND	VDD-SYS	VDD-SYS	GND	GND	VCC-EFUSE	GND	GND	VDD33	VDD-CPUS	VCC-PL	GND	PM5	PL2	PL1	PL3	
H	GND	PF6	PF5			GND	GND	VDD-SYS	VDD-SYS	VDD-SYS	VDD-SYS	GND	GND	GND	GND	GND	GND	VCC-PM	PL4	PL7	PL0	PL5	PL11
J		PC9	PF1	PF0	PF2	PC16	VCC-PC	GND	GND	VDD-SYS	VDD-SYS	GND	GND	GND	GND	GND	GND	VCC-PLL	PL6	PL8	PL9	PL10	PL12
K	PC11	PC6	PC10	PC14	PC0	PC3	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PL13	PL17	PL14	PL16	PL15	
L	PC12	PC7	GND				GND	GND	GND	GND	GND	GND	GND	GND	VDD-VE	VDD-VE				AP-CK-MUX	GND	X24MOUT	X24MIN
M		PC13	PC8	PC5	PC2	PC15		GND	VDD-CPU	GND	VDD-CPU	GND	GND	GND	GND	GND	VCC-PG		PG2	PL19	PL18	PG0	PLLTEST
N	GND	PC4	PC1	PH0	PH2	PH1	GND	VDD-CPU	VDD-CPU	VDD-CPU	GND	GND	GND	GND	VDD-GPU	GND	GND	GND	PG6	PG7	PG9	PG5	PG1
P	PH5	PH4	PH3				GND	VDD-CPU	GND	VDD-CPU	VDD-CPU	GND	GND	VDD-GPU	VDD-GPU	VDD-GPU	GND	GND			PG8	PG4	PG3
R		PH10	PH9	PH8	PH7	PH6	VCC-IO	VDD-CPUFB	GND	GND	GND	GND	GND	VDD-GPU	GND	VDD-GPU	VDD-GPUFB		PG13	PG12	PG11	PG10	
T	PB3	PB2	PB1	PB0	PH12	PH11	VCC-IO	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC-PE		PE7	PE5	PE1	PE3	PE0
U		PB5	PB7	PB8			GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	GND	VCC-PD		PE6	PE8	PE4	PE2
V	PB4	PB6	PB9	PB10		JTAG-SEL	GND	SA5		SVREF	SCKE1		SCS1		SBA1	SA15		GND	PD1	PE13	PE12	PE10	
W	GND	SZQ	GND	SRST	SCAS		SRAS	SBA2		GND	SCS0		SCKE0		GND	SA0		SA2	GND		PD0	PE11	PE9
Y	SDQ30	SDQ31	SA9	SWE	SA7		SA6	GND		SBA0	SODT0		SODT1		SA3	SA11		SA12	SA1	SA14		PE16	PE14
AA	SDQ28	GND	SA13	SA8	GND	SDQ20	SDQ21	SDQS2N	SDQM2			SDQ5	SDQS0P	GND	SDQ1	SDQ0		SA10	GND	SA4	GND	GND	PE15
AB	SDQ29	SDQS3P	SDQ27	SDQ25	SDQM3	SDQ23	SDQS2P	SDQ18	SDQ16	SCKN	GND	SDQ6	SDQ4	SDQS0N	SDQ2	SDQM0	SDQ14	SDQ13	SDQS1P	SDQ10	SDQ8	VDD18-DRAM	PE17
AC	GND	SDQS3N	SDQ26	SDQ24		SDQ22		SDQ19	SDQ17	GND	SCKP	SDQ7		SDQ3		GND	SDQ15	SDQ12	SDQS1N	SDQ11	SDQ9	SDQM1	GND

Figure 8-1. A63 Pin Map

8.2. Package Dimension

Figure 8-2 shows the top,bottom,and side views of A63 package dimension.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.849	0.920	0.991	0.033	0.036	0.039
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.620	0.670	0.720	0.024	0.026	0.028
c	0.18	0.22	0.26	0.007	0.009	0.010
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	14.30	---	---	0.563	---
E1	---	14.30	---	---	0.563	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa		0.15			0.006	
bbb		0.15			0.006	
ddd		0.13			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		23 / 23				

Figure 8-2. A63 Package Dimension

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