# F1C800 Datasheet

*HD Video Boombox Processor*

**Revision 1.0**

**Mar. 14, 2017**

# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | Mar.14,2017 | Initial Release Version. |

# Declaration

THIS DOCUMENTATION IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF ALLWINNER TECHNOLOGY ("ALLWINNER"). REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF ALLWINNER AND GIVE CLEAR ACKNOWLEDGEMENT TO THE COPYRIGHT OWNER.

THE INFORMATION FURNISHED BY ALLWINNER IS BELIEVED TO BE ACCURATE AND RELIABLE. ALLWINNER RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE. ALLWINNER DOES NOT ASSUME ANY RESPONSIBILITY AND LIABILITY FOR ITS USE. NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF ALLWINNER. THIS DATASHEET NEITHER STATES NOR IMPLIES WARRANTY OF ANY KIND, INCLUDING FITNESS FOR ANY PARTICULAR APPLICATION.

THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. ALLWINNER SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. ALLWINNER SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.

# Contents

1. Overview ..... 8
2. Features ..... 9
2.1. CPU ..... 9
2.2. Memory Subsystem ..... 9
2.3. System Peripheral ..... 9
2.4. Display Subsystem ..... 11
2.5. Video Engine ..... 12
2.6. Image Subsystem ..... 12
2.7. Audio Subsystem ..... 13
2.8. External Peripherals ..... 13
2.9. Package ..... 15
3. Block Diagram ..... 16
4. Pin Description ..... 18
4.1. Pin Characteristics ..... 18
4.2. Signal Descriptions ..... 28
5. Electrical Characteristics ..... 33
5.1. Absolute Maximum Ratings ..... 33
5.2. Recommended Operating Conditions ..... 33
5.3. DC Electrical Characteristics ..... 34
5.4. PLL Electrical Characteristics ..... 34
5.4.1. CPU PLL Electrical Parameters ..... 34
5.4.2. Audio PLL Electrical Parameters ..... 34
5.4.3. Peripheral0/1(2X) PLL Electrical Parameters ..... 35
5.4.4. DDR1 PLL Electrical Parameters ..... 35
5.4.5. Video0/1 PLL Electrical Parameters ..... 35
5.4.6. DE PLL Electrical Parameters ..... 35
5.4.7. VE PLL Electrical Parameters ..... 36
5.4.8. MIPI PLL Electrical Parameters ..... 36
5.5. KEYADC Electrical Characteristics ..... 36
5.6. TP Electrical Characteristics ..... 36
5.7. Oscillator Electrical Characteristics ..... 37
5.8. Maximum Current Consumption ..... 38
5.9. External Memory Electrical Characteristics ..... 38
5.9.1. SMHC AC Electrical Characteristics ..... 38
5.10. External Peripherals Electrical Characteristics ..... 39
5.10.1. LCD AC Electrical Characteristics ..... 39
5.10.2. SPI AC Electrical Characteristics ..... 42
5.10.3. UART AC Electrical Characteristics ..... 42
5.10.4. TWI AC Electrical Characteristics ..... 44
5.10.5. CIR Receiver AC Electrical Characteristics ..... 44
5.10.6. SCR AC Electrical Characteristics ..... 45
5.10.7. TSC AC Electrical Characteristics ..... 46
5.10.8. I2S/PCM AC Electrical Characteristics ..... 46
5.11. Power-up and Power-down Sequence ..... 47
5.11.1. Power-up Sequence ..... 47
5.11.2. Power-down Sequence ..... 48
6. Package Thermal Characteristics ..... 49
7. Pin Assignment ..... 50
7.1. Pin Map ..... 50
7.2. Package Dimension ..... 51

# Figures

Figure 3-1. F1C800 Block Diagram ..... 16
Figure 3-2. F1C800 Application Diagram ..... 17
Figure 5-1. SMHC Output Timing Diagram ..... 38
Figure 5-2. SMHC Input Timing Diagram ..... 39
Figure 5-3. HV_IF Interface Vertical Timing Diagram ..... 40
Figure 5-4. HV_IF Interface Parallel Mode Horizontal Timing Diagram ..... 40
Figure 5-5. HV_IF Interface Serial Mode Horizontal Timing Diagram ..... 41
Figure 5-6. SPI MOSI Timing Diagram ..... 42
Figure 5-7. SPI MISO Timing Diagram ..... 42
Figure 5-8. UART RX Timing Diagram ..... 43
Figure 5-9. UART nCTS Timing Diagram ..... 43
Figure 5-10. UART nRTS Timing Diagram ..... 43
Figure 5-11. TWI Timing Diagram ..... 44
Figure 5-12. CIR Receiver Timing Diagram ..... 44
Figure 5-13. SCR Activation and Cold Reset Timing Diagram ..... 45
Figure 5-14. SCR Warm Reset Timing Diagram ..... 45
Figure 5-15. TSC Data and Clock Timing ..... 46
Figure 5-16. I2S/PCM Master Mode Timing ..... 46
Figure 5-17. I2S/PCM Slave Mode Timing ..... 47
Figure 5-18. F1C800 Power Up Sequence ..... 48
Figure 7-1. F1C800 Pin Map ..... 50
Figure 7-2. F1C800 Package Dimension ..... 51

# Tables

Table 4-1. Pin Characteristics ..... 19
Table 4-2. Signal Descriptions ..... 28
Table 5-1. Absolute Maximum Ratings ..... 33
Table 5-2. Recommended Operating Conditions ..... 33
Table 5-3. DC Electrical Characteristics ..... 34
Table 5-4. CPU PLL Electrical Parameters ..... 34
Table 5-5. Audio PLL Electrical Parameters ..... 34
Table 5-6. Peripheral0/1(2X) PLL Electrical Parameters ..... 35
Table 5-7. DDR1 PLL Electrical Parameters ..... 35
Table 5-8. Video0/1 PLL Electrical Parameters ..... 35
Table 5-9. DE PLL Electrical Parameters ..... 35
Table 5-10. VE PLL Electrical Parameters ..... 36
Table 5-11. MIPI PLL Electrical Parameters ..... 36
Table 5-12. KEYADC Electrical Characteristics ..... 36
Table 5-13. TP Electrical Characteristics ..... 36
Table 5-14. 24MHz Crystal Characteristics ..... 37
Table 5-15. 32768Hz Crystal Characteristics ..... 37
Table 5-16. Maximum Current Consumption ..... 38
Table 5-17. SMHC Output Timing Constants ..... 38
Table 5-18. SMHC Input Timing Constants ..... 39
Table 5-19. LCD HV_IF Interface Timing Constants ..... 41
Table 5-20. SPI Timing Constants ..... 42
Table 5-21. UART Timing Constants ..... 43
Table 5-22. TWI Timing Constants ..... 44
Table 5-23. CIR Receiver Timing Constants ..... 44
Table 5-24. SCR Timing Constants ..... 45
Table 5-25. TSC Timing Constants ..... 46
Table 5-26. I2S/PCM Master Mode Timing Constants ..... 46
Table 5-27. I2S/PCM Slave Mode Timing Constants ..... 47
Table 6-1. F1C800 Thermal Resistance Characteristics ..... 49

# About This Documentation

The documentation describes features of each module, pin/signal characteristics, current consumption, PLL electrical characteristics, the interface timing, thermal and package of F1C800 processor. The documentation is intended to provide guidance to the hardware designers for electronics or sales personnel for electronic components. This documentation assumes that the reader has a background in electronic components. For details about register descriptions of each module, see the *F1C800 User Manual*.

# 1. Overview

The F1C800 processor represents Allwinner's latest achievement in HD Video Boombox products. The processor adopts the latest H.265 video decoder, advanced audio system, low-power technology and high integration architecture design. These features help F1C800 keep the leading user experience in HD video playback, image quality and total performance. Integrated 4-lane MIPI DSI display output interface is up to 1080p@60fps. In order to reduce the BOM cost, the F1C800 integrates an internal DDR2 memory. A number of interfaces, such as RGB LCD, LVDS, TVIN, TVOUT, USB, I2S/PCM, UART, SPI, provide the flexible connecting solutions.

# 2. Features

## 2.1. CPU

- ARM926-EJS
- Supports 32 KB Instruction cache and 32 KB Data cache

## 2.2. Memory Subsystem

### Boot ROM

- On-chip memory
- Supports system boot from the following device:
  - SD Card
  - SPI Nor Flash
  - SPI Nand Flash
  - USB OTG

### SDRAM

- SIP DDR2 memory
- Supports clock frequency up to 400 MHz

### SMHC

- Up to 2 SD/MMC Host Controller(SMHC) interfaces
- Compliant with SD physical layer specification V2.0, SDIO card specification V2.0
- 1-bit or 4-bit data bus transfer mode up to 50 MHz in SDR mode
- Supports block size of 1 to 65535 bytes
- Embedded special DMA to do data transfer

## 2.3. System Peripheral

### CCU

- 10 PLLs
- Supports an external 24 MHz crystal oscillator , an external 32.768 kHz crystal oscillator and an on-chip 16 MHz RC oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

### Timer

- 2 on-chip Timers with interrupt-based operation
- 1 Watchdog to generate reset signal or interrupt

- Two 33-bit Audio/Video Sync(AVS) Counters to synchronize video and audio in the player

## High Speed Timer

- 1 High Speed Timer(HSTimer) with 56-bit counter
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register
- Clock source is synchronized with AHB1 clock, and the pre-scale range is from 1 to 16
- More accurate than other timers

## RTC

- Time, Calendar
- Counters second, minute, hour, day, week, month and year with leap year generator
- Alarm: general alarm and weekly alarm

## INTC

- Controls the nIRQ Processor
- Sixty-four individually maskable interrupt sources
- 4-level interrupt priority setting
- Supports fast forcing

## DMA

- Up to 8-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Programs the DMA burst size
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

## PWM

- Up to 7 PWM channels
- Supports single-pulse, long-period and complementary pair output
- Supports capture input
- Supports programming deadzone output
- Build-in the programmable dead-time generator
- Supports three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- 0% to 100% adjustable duty cycle
- Up to 100 MHz output frequency
- Minimum resolution is 1/65536
- Supports interrupt generation for PWM output and capture input

## KEYADC

- Analog to digital converter with 6-bit resolution for key application
- Maximum sampling frequency up to 250 Hz
- Supports general key, hold key and already hold key

- Supports single , normal and continuous work mode

### TP

- 12-bit SAR type A/D converter
- 4-wire I/F
- Touch-pressure measurement (Supports programmable threshold)
- Sampling frequency up to 1 MHz
- Single-ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Supports X, Y change

### Crypto Engine(CE)

- Supports AES, DES, 3DES, SHA-1, MD5
- Supports 160-bit hardware PRNG with 175-bit seed
- 128-bit, 192-bit and 256-bit key size for AES
- Supports ECB, CBC ,CTR,CTS modes for AES
- Supports ECB, CBC,CTR modes for DES/3DES
- Supports 32 words RX FIFO and 32 words TX FIFO for high speed application
- Supports CPU mode and DMA mode

### Security ID

- On-chip 512-bit EFUSE for chip ID and other applications
- Supports on-line LDO programming

## 2.4. Display Subsystem

### DE2.0

- Output size up to 2048 x 2048
- Supports 1 UI channel and 1 video channel for main display RT-Mixer
- Supports 1 video channel for aux display
- Supports four layers in each overlay channel, and has a independent scaler
- Supports potter-duff compatible blending operation
- Supports input format :YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor 2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports dual display: LCD + CVBS Out
- Supports writeback and rotation for high efficient dual display
- Supports online/offline de-interlacer

### Display Output

- Supports 18-bit RGB interface
  - Up to 1920x1080@60fps
  - Supports dither function
  - Supports Gamma parameter adjusting
- Supports LVDS interface
  - Dual link LVDS mode output up to 1920x1080@60fps
  - Single link LVDS mode output up to 1366x768@60fps
  - Multiplex pin with RGB interface
- Supports 1-ch TV CVBS output
  - Supports NTSC and PAL mode
  - Plug status auto detecting
- Supports 4-lane MIPI DSI output
  - Up to 1080p@60fps
  - Compliance with MIPI DSI v1.01 and MIPI D-PHY v1.00
  - 1/2/3/4 data lane configuration and up to 1Gbps per lane
  - Supports video mode with sync pulse/burst mode
  - Supports pixel format: RGB888, RGB666, RGB666 packed, and RGB565

## 2.5. Video Engine

### Video Decoder

- Supports multi-format video playback, including:
  - H.265 MP/L5.2: 1080p@45fps
  - H.264 BP/MP/HP Level4.2: 1080p@45fps
  - H.263 BP: 1080p@45fps
  - MPEG1 MP/HL: 1080p@45fps
  - MPEG2 MP/HL: 1080p@45fps
  - MPEG4 SP/ASP L5: 1080p@45fps
  - Sorenson Spark: 1080p@45fps
  - VP8 N/A: 1080p@45fps
  - AVS/AVS+ JiZhun: 1080p@45fps
  - xvid N/A: 1080p@45fps
  - WMV9/VC1 SP/MP/AP: 1080p@30fps
  - JPEG: 45MPPS

## 2.6. Image Subsystem

### TVIN

- 2 channels TV CVBS input to 1 channel CVBS decoder
- Supports NTSC and PAL mode
- Supports YUV422, YUV420 format
- With 3D comb filter
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

# 2.7. Audio Subsystem

## Audio Codec

- Two audio digital-to-analog(DAC) channels
  - 100 ± 3 dB SNR@A-weight
  - Supports ADC sample rates from 8 kHz to 192 kHz
- One audio analog-to-digital(ADC) channel
  - 92 ± 3 dB SNR@A-weight
  - Supports ADC sample rates from 8 kHz to 48 kHz
- Supports analog/digital volume control
- Analog low-power loop from analog to analog outputs
- Supports Dynamic Range Controller(DRC) adjusting the DAC playback output
- Supports Dynamic Range Control(DRC) adjusting the ADC recording input
- Three audio inputs:
  - One microphone input
  - One mono line-in input
  - One stereo FMIN input
- One audio output: One stereo headphone output
- Interrupt and DMA support

## I2S/PCM

- Compliant with standard Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Supports 8-channel in TDM mode
- Full-duplex synchronous work mode
- Master and slave mode configured
- Clock frequency up to 100 MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Supports up to 8 slots which has adjustable width from 8-bit to 32-bit.
- Supports sample rate from 8 kHz to 192 kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 x 32-bit width FIFO for data transmit, one 64 x 32-bit width FIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support

# 2.8. External Peripherals

## USB

- One USB 2.0 OTG, with integrated USB PHY
- Supports host/device dual-role function
- Complies with USB 2.0 Specification
- Complies with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a for host mode
- Supports High-Speed (HS, 480 Mbit/s),Full-Speed(FS, 12 Mbit/s) and Low-Speed(LS, 1.5 Mbit/s) in host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
- Up to 8 user-configurable endpoints (Endpoint1, Endpoint2, Endpoint3, Endpoint4) in device mode

## TWI

- Up to 3 TWI(Two Wire Interface) controllers
- Supports Standard mode(up to 100 kbit/s) and Fast mode(up to 400 kbit/s)
- Master/slave configurable
- Allows 10-bit addressing transactions
- Perform arbitration and clock synchronization
- Allows operation from a wide range of input clock frequencies

## SPI

- Up to 2 SPI controllers, each SPI has one chip select signal
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation
- Polarity and phase of the chip select(SPI_SS) and SPI_Clock(SPI_SCLK) are configurable
- Supports single and dual IO mode
- Maximum frequency up to 100 MHz

## UART

- Up to 3 UART controllers: one UART for CPU debug, two UART for UART applications
- UART0: 2-wire; UART1/2: 4-wire
- Compliant with industry-standard 16450 and 16550 UARTs
- Supports RS232 protocol
- Supports word length from 5 to 8 bits, an optional parity bit and 1,1.5 or 2 stop bits
- Programmable parity(even, odd and no parity)
- 64 bytes transmit and receive data FIFOs
- Supports clock frequency up to 4 Mbit/s

## CIR Receiver

- A flexible receiver for IR remote
- Programmable FIFO threshold

## SCR

- One SCR(Smart Card Reader) controller
- Supports ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports asynchronous half-duplex character transmission and block transmission
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card

### TSC

- One TSC(Transport Stream Controller)
- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter for TSF
- Multiple transport stream packet (188, 192, 204) format support
- SPI and SSI timing parameters are configurable
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- Configurable SPI transport stream generator for streams in DRAM memory

## 2.9. Package

- eLQFP128(SIP DDR2), 14 mm x 14 mm

# 3. Block Diagram

Figure 3-1 shows the block diagram of the F1C800 processor.

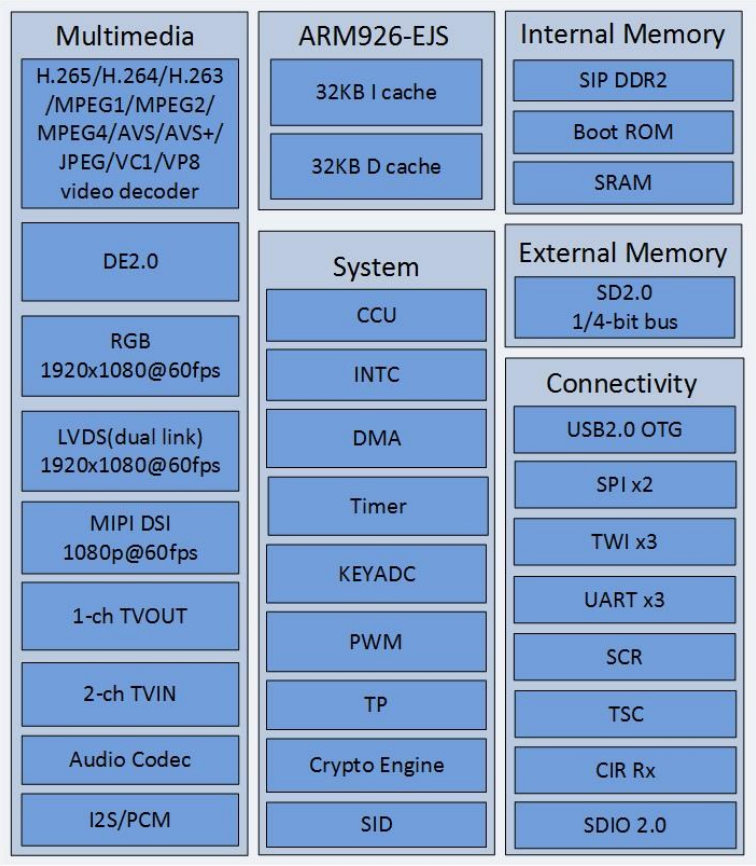



**Figure 3-1. F1C800 Block Diagram**

The F1C800 typical application diagram is shown in Figure 3-2.

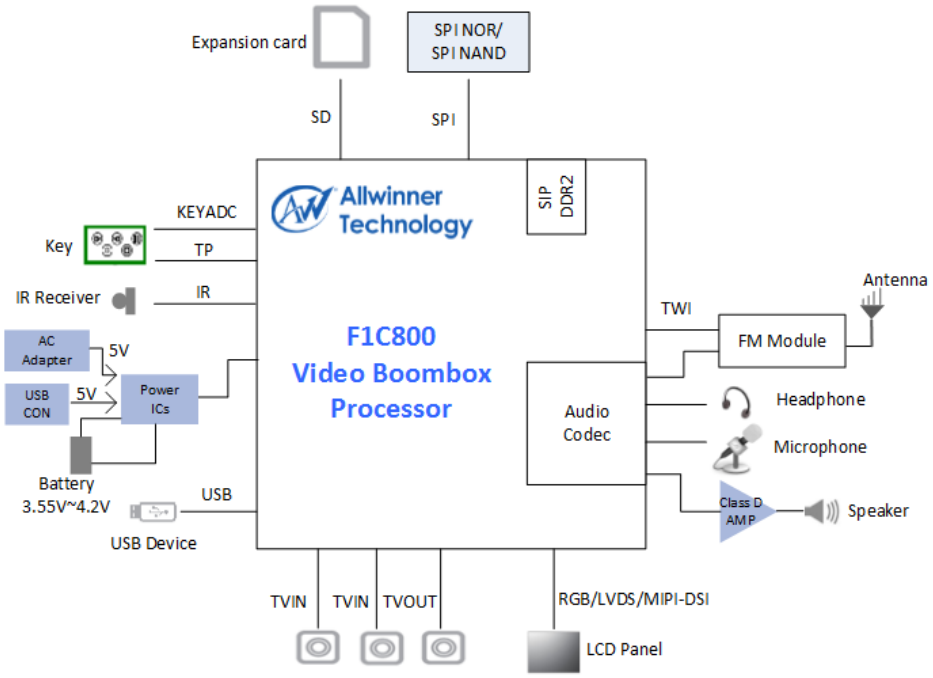



**Figure 3-2. F1C800 Application Diagram**

# 4. Pin Description

## 4.1. Pin Characteristics

Table 4-1 lists the characteristics of F1C800 pins from the following ten aspects.

(1).**Ball#** : Package ball numbers associated with each signals.

(2).**Pin Name** : The name of the package pin.

(3).**Signal Name** : The signal name for that pin in the mode being used.

(4).**Function** : Multiplexing function number.

(5).**Ball Reset Rel. Function** : The function is automatically configured after RESET from low to high.

(6).**Type** : Denotes the signal direction

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output)
P (Power),
G (Ground)

(7).**Ball Reset State** : The state of the terminal at reset.

(8).**Pull Up/Down** : Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

(9).**Buffer Strength** : Defines drive strength of the associated output buffer.

(10).**Power Supply** : The voltage supply for the terminal's IO buffers.

**Table 4-1. Pin Characteristics**

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| **SDRAM** | | | | | | | | | |
| 72 | SVREF0 | SVREF0 | NA | NA | P | Z | NA | NA | NA |
| 67 | SVREF1 | SVREF1 | NA | NA | P | Z | NA | NA | NA |
| 77 | SZQ | SZQ | NA | NA | AI | Z | NA | NA | NA |
| 63 | VCC-DRAM1 | VCC-DRAM1 | NA | NA | P | Z | NA | NA | NA |
| 64 | VCC-DRAM2 | VCC-DRAM2 | NA | NA | P | Z | NA | NA | NA |
| 65 | VCC-DRAM3 | VCC-DRAM3 | NA | NA | P | Z | NA | NA | NA |
| 66 | VCC-DRAM4 | VCC-DRAM4 | NA | NA | P | Z | NA | NA | NA |
| 69 | VCC-DRAM5 | VCC-DRAM5 | NA | NA | P | Z | NA | NA | NA |
| 70 | VCC-DRAM6 | VCC-DRAM6 | NA | NA | P | Z | NA | NA | NA |
| 71 | VCC-DRAM7 | VCC-DRAM7 | NA | NA | P | Z | NA | NA | NA |
| 73 | VCC-DRAM8 | VCC-DRAM8 | NA | NA | P | Z | NA | NA | NA |
| 74 | VCC-DRAM9 | VCC-DRAM9 | NA | NA | P | Z | NA | NA | NA |
| 75 | VCC-DRAM10 | VCC-DRAM10 | NA | NA | P | Z | NA | NA | NA |
| 83 | VCC-DRAM11 | VCC-DRAM11 | NA | NA | P | Z | NA | NA | NA |
| **GPIOB** | | | | | | | | | |
| 11 | PB0 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART0_TX | 2 | | O | | | | |
| | | PWM0 | 3 | | I/O | | | | |
| | | TWI1_SCK | 4 | | I/O | | | | |
| | | SIM_VPPEN | 5 | | O | | | | |
| | | PB_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 12 | PB1 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | UART0_RX | 2 | | I | | | | |
| | | PWM1 | 3 | | I/O | | | | |
| | | TWI1_SDA | 4 | | I/O | | | | |
| | | SIM_VPPPP | 5 | | O | | | | |
| | | PB_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 13 | PB2 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | CLK_OUT | 2 | | O | | | | |
| | | IR_RX | 3 | | I | | | | |
| | | PLL_LOCK_DBG | 4 | | I/O | | | | |
| | | SIM_PWREN | 5 | | O | | | | |
| | | PB_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 14 | PB3 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_CS | 2 | | I/O | | | | |
| | | UART1_TX | 3 | | O | | | | |
| | | TWI2_SCK | 4 | | I/O | | | | |
| | | SIM_CLK | 5 | | O | | | | |
| | | PB_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 16 | PB4 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_CLK | 2 | | I/O | | | | |
| | | UART1_RX | 3 | | I | | | | |
| | | TWI2_SDA | 4 | | I/O | | | | |
| | | SIM_DATA | 5 | | I/O | | | | |
| | | PB_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 17 | PB5 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_MOSI | 2 | | I/O | | | | |
| | | UART1_RTS | 3 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | PWM2 | 4 | | I/O | | | | |
| | | SIM_RST | 5 | | O | | | | |
| | | PB_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 18 | PB6 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI1_MISO | 2 | | I/O | | | | |
| | | UART1_CTS | 3 | | I | | | | |
| | | PWM3 | 4 | | I/O | | | | |
| | | SIM_DET | 5 | | I | | | | |
| | | PB_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 19 | PB7 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI0_SCK | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 20 | PB8 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI0_SDA | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT8 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 21 | PB9 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_CS | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT9 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 23 | PB10 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_CLK | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT10 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 24 | PB11 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_MOSI | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT11 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 25 | PB12 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SPI0_MISO | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PB_EINT12 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOD** | | | | | | | | | |
| 26 | PD0 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | LCD_D2 | 2 | | O | | | | |
| | | LVDS0_VP0 | 3 | | O | | | | |
| | | SIM_PWREN | 4 | | O | | | | |
| | | UART1_TX | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 27 | PD1 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D3 | 2 | | O | | | | |
| | | LVDS0_VN0 | 3 | | O | | | | |
| | | SIM_CLK | 4 | | O | | | | |
| | | UART1_RX | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 28 | PD2 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D4 | 2 | | O | | | | |
| | | LVDS0_VP1 | 3 | | O | | | | |
| | | SIM_DATA | 4 | | I/O | | | | |
| | | UART1_RTS | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 29 | PD3 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D5 | 2 | | O | | | | |
| | | LVDS0_VN1 | 3 | | I | | | | |
| | | SIM_RST | 4 | | O | | | | |
| | | UART1_CTS | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 31 | PD4 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D6 | 2 | | O | | | | |
| | | LVDS0_VP2 | 3 | | O | | | | |
| | | SIM_DET | 4 | | I | | | | |
| | | UART2_TX | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 32 | PD5 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D7 | 2 | | O | | | | |
| | | LVDS0_VN2 | 3 | | O | | | | |
| | | I2S_MCLK | 4 | | O | | | | |
| | | UART2_RX | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 33 | PD6 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D10 | 2 | | O | | | | |
| | | LVDS0_VPC | 3 | | O | | | | |
| | | I2S_SYNC | 4 | | I/O | | | | |
| | | UART2_RTS | 5 | | O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 34 | PD7 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D11 | 2 | | O | | | | |
| | | LVDS0_VNC | 3 | | O | | | | |
| | | I2S_CLK | 4 | | I/O | | | | |
| | | UART2_CTS | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 35 | PD8 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | Output | 1 | | O | | | | |
| | | LCD_D12 | 2 | | O | | | | |
| | | LVDS0_VP3 | 3 | | O | | | | |
| | | I2S_DOUT | 4 | | O | | | | |
| | | PWM6 | 5 | | I/O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 36 | PD9 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D13 | 2 | | O | | | | |
| | | LVDS0_VN3 | 3 | | O | | | | |
| | | I2S_DIN | 4 | | I | | | | |
| | | PWM7 | 5 | | I/O | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 37 | PD10 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D14 | 2 | | O | | | | |
| | | LVDS1_VP0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_CLK | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 38 | PD11 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D15 | 2 | | O | | | | |
| | | LVDS1_VN0 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_ERR | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 39 | PD12 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D18 | 2 | | O | | | | |
| | | LVDS1_VP1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_SYNC | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 40 | PD13 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D19 | 2 | | O | | | | |
| | | LVDS1_VN1 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_DVLD | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 42 | PD14 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D20 | 2 | | O | | | | |
| | | LVDS1_VP2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D0 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 43 | PD15 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D21 | 2 | | O | | | | |
| | | LVDS1_VN2 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D1 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| 44 | PD16 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D22 | 2 | | O | | | | |
| | | LVDS1_VPC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D2 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 45 | PD17 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_D23 | 2 | | O | | | | |
| | | LVDS1_VNC | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D3 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 46 | PD18 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_CLK | 2 | | O | | | | |
| | | LVDS1_VP3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D4 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 47 | PD19 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_DE | 2 | | O | | | | |
| | | LVDS1_VN3 | 3 | | O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D5 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 49 | PD20 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_HSYNC | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D6 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 50 | PD21 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | LCD_VSYNC | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | TS_D7 | 5 | | I | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 51 | PD22 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | PWM0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | Reserved | 6 | | NA | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOF** | | | | | | | | | |
| 110 | PF0 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D1 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_MS | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | PF_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 111 | PF1 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D0 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_DI | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 112 | PF2 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_CLK | 2 | | O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | UART0_TX | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 113 | PF3 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_CMD | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_DO | 4 | | O | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 114 | PF4 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D3 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | UART0_RX | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 115 | PF5 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC0_D2 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | JTAG_CK | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 116 | PF6 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | Reserved | 2 | | NA | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PF_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **GPIOG** | | | | | | | | | |
| 8 | PG0 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC1_D1 | 2 | | I/O | | | | |
| | | SPI1_CS | 3 | | I/O | | | | |
| | | I2S_MCLK | 4 | | O | | | | |
| | | UART2_TX | 5 | | O | | | | |
| | | PG_EINT0 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 7 | PG1 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC1_D0 | 2 | | I/O | | | | |
| | | SPI1_CLK | 3 | | I/O | | | | |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| | | I2S_SYNC | 4 | | I/O | | | | |
| | | UART2_RX | 5 | | I | | | | |
| | | PG_EINT1 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 6 | PG2 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC1_CLK | 2 | | O | | | | |
| | | SPI1_MOSI | 3 | | I/O | | | | |
| | | I2S_CLK | 4 | | I/O | | | | |
| | | UART2_RTS | 5 | | O | | | | |
| | | PG_EINT2 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 4 | PG3 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC1_CMD | 2 | | I/O | | | | |
| | | SPI1_MISO | 3 | | I/O | | | | |
| | | I2S_DOUT | 4 | | O | | | | |
| | | UART2_CTS | 5 | | I | | | | |
| | | PG_EINT3 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 3 | PG4 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC1_D3 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | I2S_DIN | 4 | | I | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT4 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 2 | PG5 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | SDC1_D2 | 2 | | I/O | | | | |
| | | Reserved | 3 | | NA | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | Reserved | 5 | | NA | | | | |
| | | PG_EINT5 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 1 | PG6 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI1_SCK | 2 | | I/O | | | | |
| | | TWI2_SCK | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | IR_RX | 5 | | I | | | | |
| | | PG_EINT6 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| 128 | PG7 | Input | 0 | Function7 | I | Z | PU/PD | 20 | VCC-IO |
| | | Output | 1 | | O | | | | |
| | | TWI1_SDA | 2 | | I/O | | | | |
| | | TWI2_SDA | 3 | | I/O | | | | |
| | | Reserved | 4 | | NA | | | | |
| | | PWM4 | 5 | | I/O | | | | |
| | | PG_EINT7 | 6 | | I | | | | |
| | | IO Disable | 7 | | OFF | | | | |
| **System** | | | | | | | | | |
| 78 | RESET | RESET | NA | NA | I | - | PU/PD | NA | VCC-RTC |
| **KEYADC** | | | | | | | | | |
| 107 | KEYADC0 | KEYADC0 | NA | NA | AI | NA | NA | NA | AVCC |
| **TP** | | | | | | | | | |
| 124 | X1 | X1 | NA | NA | AI | NA | NA | NA | VCC-USB |
| 122 | X2 | X2 | NA | NA | AI | NA | NA | NA | VCC-USB |
| 123 | Y1 | Y1 | NA | NA | AI | NA | NA | NA | VCC-USB |
| 121 | Y2 | Y2 | NA | NA | AI | NA | NA | NA | VCC-USB |
| MIPI-DSI | | | | | | | | | |
| 52 | DSI-D0P | DSI-D0P | NA | NA | A | NA | NA | NA | VCC-DSI |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| 53 | DSI-D0N | DSI-D0N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 54 | DSI-D1P | DSI-D1P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 55 | DSI-D1N | DSI-D1N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 59 | DSI-D2P | DSI-D2P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 60 | DSI-D2N | DSI-D2N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 61 | DSI-D3P | DSI-D3P | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 62 | DSI-D3N | DSI-D3N | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 56 | VCC-DSI | VCC-DSI | NA | NA | P | NA | NA | NA | NA |
| 57 | DSI-CKP | DSI-CKP | NA | NA | AO | NA | NA | NA | VCC-DSI |
| 58 | DSI-CKN | DSI-CKN | NA | NA | AO | NA | NA | NA | VCC-DSI |
| **USB** | | | | | | | | | |
| 118 | USB-DM | USB-DM | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| 119 | USB-DP | USB-DP | NA | NA | A I/O | NA | NA | NA | VCC-USB |
| 120 | VCC-USB | VCC-USB | NA | NA | P | NA | NA | NA | NA |
| **TVIN** | | | | | | | | | |
| 91 | TVIN0 | TVIN0 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| 92 | TVIN1 | TVIN1 | NA | NA | AI | NA | NA | NA | VCC-TVIN |
| 89 | TVIN-VRN | TVIN-VRN | NA | NA | P | NA | NA | NA | NA |
| 90 | TVIN-VRP | TVIN-VRP | NA | NA | P | NA | NA | NA | NA |
| 87 | VCC-TVIN | VCC-TVIN | NA | NA | P | NA | NA | NA | NA |
| 88 | GND-TVIN | GND-TVIN | NA | NA | G | NA | NA | NA | NA |
| **TVOUT** | | | | | | | | | |
| 84 | TVOUT | TVOUT | NA | NA | AO | NA | NA | NA | VCC-TVOUT |
| 86 | VCC-TVOUT | VCC-TVOUT | NA | NA | P | NA | NA | NA | NA |
| 85 | GND-TVOUT | GND-TVOUT | NA | NA | G | NA | NA | NA | NA |
| **Audio Codec** | | | | | | | | | |
| 93 | ACLDOIN | ACLDOIN | NA | NA | P | NA | NA | NA | NA |
| 96 | AGND | AGND | NA | NA | G | NA | NA | NA | NA |
| 94 | AVCC | AVCC | NA | NA | P | NA | NA | NA | ACLDOIN |
| 99 | FMINL | FMINL | NA | NA | AI | NA | NA | NA | AVCC |
| 98 | FMINR | FMINR | NA | NA | AI | NA | NA | NA | AVCC |
| 105 | HPCOMFB | HPCOMFB | NA | NA | AI | NA | NA | NA | NA |
| 103 | HPL | HPL | NA | NA | AO | NA | NA | NA | HPVCC |
| 102 | HPR | HPR | NA | NA | AO | NA | NA | NA | HPVCC |
| 104 | HPVCC | HPVCC | NA | NA | P | NA | NA | NA | HPVCCIN |
| 106 | HPVCCIN | HPVCCIN | NA | NA | P | NA | NA | NA | NA |
| 101 | LINEINL | LINEINL | NA | NA | AI | NA | NA | NA | AVCC |
| 100 | MICIN | MICIN | NA | NA | AI | NA | NA | NA | AVCC |
| 95 | VRA1 | VRA1 | NA | NA | AO | NA | NA | NA | AVCC |
| 97 | VRA2 | VRA2 | NA | NA | AO | NA | NA | NA | AVCC |
| **PLL&RTC** | | | | | | | | | |
| 125 | X24MIN | X24MIN | NA | NA | AI | NA | NA | NA | VCC-PLL |
| 126 | X24MOUT | X24MOUT | NA | NA | AO | NA | NA | NA | VCC-PLL |
| 127 | VCC-PLL | VCC-PLL | NA | NA | P | NA | NA | NA | NA |
| 81 | X32KIN | X32KIN | NA | NA | AI | NA | NA | NA | VCC-RTC |
| 82 | X32KOUT | X32KOUT | NA | NA | AO | NA | NA | NA | VCC-RTC |
| 79 | VCC-RTC | VCC-RTC | NA | NA | P | NA | NA | NA | NA |
| 80 | RTC-VIO | RTC-VIO | NA | NA | AO | NA | NA | NA | VCC-RTC |
| **Efuse** | | | | | | | | | |
| 108 | VCC-EFUSEBP | VCC-EFUSEBP | NA | NA | O | NA | NA | NA | NA |
| **Power** | | | | | | | | | |
| 9 | VDD-CORE1 | VDD-CORE1 | NA | NA | P | NA | NA | NA | NA |
| 10 | VDD-CORE2 | VDD-CORE2 | NA | NA | P | NA | NA | NA | NA |
| 48 | VDD-CORE3 | VDD-CORE3 | NA | NA | P | NA | NA | NA | NA |
| 68 | VDD-CORE4 | VDD-CORE4 | NA | NA | P | NA | NA | NA | NA |
| 76 | VDD-CORE5 | VDD-CORE5 | NA | NA | P | NA | NA | NA | NA |
| 117 | VDD-CORE6 | VDD-CORE6 | NA | NA | P | NA | NA | NA | NA |
| 5 | VCC-IO1 | VCC-IO1 | NA | NA | P | NA | NA | NA | NA |
| 15 | VCC-IO2 | VCC-IO2 | NA | NA | P | NA | NA | NA | NA |
| 22 | VCC-IO3 | VCC-IO3 | NA | NA | P | NA | NA | NA | NA |
| 30 | VCC-IO4 | VCC-IO4 | NA | NA | P | NA | NA | NA | NA |
| 41 | VCC-IO5 | VCC-IO5 | NA | NA | P | NA | NA | NA | NA |
| 109 | VCC-IO6 | VCC-IO6 | NA | NA | P | NA | NA | NA | NA |

| Ball#[1] | Pin Name[2] | Signal Name[3] | Function[4] | Ball Reset Rel. Function[5] | Type[6] | Ball Reset State[7] | Pull Up/Down[8] | Buffer Strength[9] (mA) | Power Supply[10] |
|---|---|---|---|---|---|---|---|---|---|
| **Ground** | | | | | | | | | |
| 129 | EPAD | EPAD | NA | NA | G | NA | NA | NA | NA |

(1).OFF: Disable IO function
(2).NA: No Application

## 4.2. Signal Descriptions

F1C800 contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 4-1. Table 4-2 shows the detailed function description of every signal based on the different interface.

(1).**Signal Name**: The name of every signal.

(2).**Description**: The detailed function description of every signal.

(3).**Type**: Denotes the signal direction.

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

**Table 4-2. Signal Descriptions**

| Signal Name(1) | Description(2) | Type(3) |
|---|---|---|
| **SDRAM** | | |
| SZQ | SDRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer) | AI |
| SVREF[1:0] | SDRAM Reference Voltage Input | P |
| VCC-DRAM[11:1] | SDRAM Power Supply | P |
| **System Control** | | |
| RESET | Reset Signal | I |
| **Interrupt** | | |
| PB_EINT[12:0] | GPIO B Interrupt | I |
| PF_EINT[6:0] | GPIO F Interrupt | I |
| PG_EINT[7:0] | GPIO G Interrupt | I |
| **PWM** | | |
| PWM[4:0] | Pulse Width Modulation Channel[4:0] | I/O |
| PWM[7:6] | Pulse Width Modulation Channel[7:6] | I/O |
| **I2S** | | |
| I2S_MCLK | I2S/PCM Master Clock | O |
| I2S_SYNC | I2S/PCM Sample Rate Clock/Sync | I/O |
| I2S_CLK | I2S/PCM Sample Rate Serial Clock | I/O |
| I2S_DOUT | I2S/PCM Serial Data Output | O |
| I2S_DIN | I2S/PCM Serial Data Input | I |
| **SMHC** | | |
| SDC0_CMD | Command Signal for SD/TF Card | I/O |

| Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| SDC0_CLK | Clock for SD/TF Card | O |
| SDC0_D[3:0] | Data Input and Output for SD/TF Card | I/O |
| SDC1_CMD | Command Signal for SDIO WIFI | I/O |
| SDC1_CLK | Clock for SDIO WIFI | O |
| SDC1_D[3:0] | Data Input and Output for SDIO WIFI | I/O |
| **SCR** | | |
| SIM_PWREN | Smart Card 0 Power Enable | O |
| SIM_CLK | Smart Card 0 Clock | O |
| SIM_DATA | Smart Card 0 Data | I/O |
| SIM_RST | Smart Card 0 Reset | O |
| SIM_DET | Smart Card 0 Detect | I |
| SIM_VPPEN | Smart Card 0 Program Voltage Enable | O |
| SIM_VPPPP | Smart Card 0 Program Control | O |
| **CIR** | | |
| IR_RX | CIR Data Receive | I |
| **TSC** | | |
| TS_D[7:0] | Transport Stream Data | I |
| TS_CLK | Transport Stream Clock | I |
| TS_ERR | Transport Stream Error Indicate | I |
| TS_SYNC | Transport Stream Sync | I |
| TS_DVLD | Transport Stream Data Valid | I |
| **TWIx(x=0,1,2)** | | |
| TWIx_SCK | TWI Serial Clock Signal | I/O |
| TWIx_SDA | TWI Serial Data Signal | I/O |
| **SPIx (x=0,1)** | | |
| SPIx_CS | SPI Chip Select Signal, Low Active | I/O |
| SPIx_CLK | SPI Clock Signal | I/O |
| SPIx_MOSI | SPI Master Data Out, Slave Data In | I/O |
| SPIx_MISO | SPI Master Data In, Slave Data Out | I/O |
| **UART** | | |
| UART0_TX | UART0 Data Transmit | O |
| UART0_RX | UART0 Data Receive | I |
| UART1_TX | UART1 Data Transmit | O |
| UART1_RX | UART1 Data Receive | I |
| UART1_CTS | UART1 Data Clear to Send | I |
| UART1_RTS | UART1 Data Request to Send | O |
| UART2_TX | UART2 Data Transmit | O |
| UART2_RX | UART2 Data Receive | I |
| UART2_CTS | UART2 Data Clear to Send | I |
| UART2_RTS | UART2 Data Request to Send | O |
| **LVDS** | | |
| LVDS0_VP[3:0] | LVDS0 Data Positive Signal Output | AO |
| LVDS0_VN[3:0] | LVDS0 Data Negative Signal Output | AO |

| Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| LVDS0_VPC | LVDS0 Clock Positive Output | AO |
| LVDS0_VNC | LVDS0 Clock Negative Output | AO |
| LVDS1_VP[3:0] | LVDS1 Data Positive Signal Output | AO |
| LVDS1_VN[3:0] | LVDS1 Data Negative Signal Output | AO |
| LVDS1_VPC | LVDS1 Clock Positive Output | AO |
| LVDS1_VNC | LVDS1 Clock Negative Output | AO |
| **LCD** | | |
| LCD_D2 | LCD Data Output | O |
| LCD_D3 | LCD Data Output | O |
| LCD_D4 | LCD Data Output | O |
| LCD_D5 | LCD Data Output | O |
| LCD_D6 | LCD Data Output | O |
| LCD_D7 | LCD Data Output | O |
| LCD_D10 | LCD Data Output | O |
| LCD_D11 | LCD Data Output | O |
| LCD_D12 | LCD Data Output | O |
| LCD_D13 | LCD Data Output | O |
| LCD_D14 | LCD Data Output | O |
| LCD_D15 | LCD Data Output | O |
| LCD_D18 | LCD Data Output | O |
| LCD_D19 | LCD Data Output | O |
| LCD_D20 | LCD Data Output | O |
| LCD_D21 | LCD Data Output | O |
| LCD_D22 | LCD Data Output | O |
| LCD_D23 | LCD Data Output | O |
| LCD_CLK | LCD Clock Signal | O |
| LCD_DE | LCD Data Enable | O |
| LCD_HSYNC | LCD Horizontal SYNC | O |
| LCD_VSYNC | LCD Vertical SYNC | O |
| **JTAG** | | |
| JTAG_MS | JTAG Mode Select | I |
| JTAG_CK | JTAG Clock Signal | I |
| JTAG_DO | JTAG Data Output | O |
| JTAG_DI | JTAG Data Input | I |
| **USB** | | |
| USB-DM | USB Data Signal DM | A I/O |
| USB-DP | USB Data Signal DP | A I/O |
| VCC-USB | USB Power Supply | P |
| **ADC** | | |
| KEYADC0 | ADC Input for Key | AI |
| **Audio Codec** | | |
| FMINL | FMIN Left Input | AI |
| FMINR | FMIN Right Input | AI |

| Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| MICIN | Microphone Input | AI |
| LINEINL | Linein Input | AI |
| HPL | Headphone Left Output | AO |
| HPR | Headphone Right Output | AO |
| HPVCC | HPVCC Bypass | P |
| HPVCCIN | Headphone Amplifier Power Input | P |
| HPCOMFB | Headphone Common Reference Feedback Input | AI |
| VRA1 | Reference Output1 | AO |
| VRA2 | Reference Output2 | AO |
| AVCC | Analog Power | P |
| AGND | Analog Ground | G |
| ACLDOIN | Analog LDO Input | P |
| **TP** | | |
| X1 | Touch Panel X1 Input | AI |
| X2 | Touch Panel X2 Input | AI |
| Y1 | Touch Panel Y1 Input | AI |
| Y2 | Touch Panel Y2 Input | AI |
| **MIPI DSI** | | |
| DSI-D0P | DSI Data0 Positive Output | AO |
| DSI-D0N | DSI Data0 Negative Output | AO |
| DSI-D1P | DSI Data1 Positive Output | AO |
| DSI-D1N | DSI Data1 Negative Output | AO |
| DSI-D2P | DSI Data2 Positive Output | AO |
| DSI-D2N | DSI Data2 Negative Output | AO |
| DSI-D3P | DSI Data3 Positive Output | AO |
| DSI-D3N | DSI Data3 Negative Output | AO |
| DSI-CKP | DSI Clock Positive Output | AO |
| DSI-CKN | DSI Clock Negative Output | AO |
| VCC-DSI | DSI Power Supply | P |
| **TVOUT** | | |
| TVOUT | TVOUT Output | AO |
| VCC-TVOUT | TVOUT Power Supply | P |
| GND-TVOUT | TVOUT Ground | G |
| **TVIN** | | |
| TVIN0 | TVIN Channel0 Input | AI |
| TVIN1 | TVIN Channel1 Input | AI |
| TVIN-VRN | TVIN Reference Voltage Positive | P |
| TVIN-VRP | TVIN Reference Voltage Negative | P |
| VCC-TVIN | TVIN Power Supply | P |
| GND-TVIN | TVIN Ground | G |
| **PLL&RTC** | | |
| X24MIN | Clock Input of 24MHz Crystal | AI |
| X24MOUT | Clock Output of 24MHz Crystal | AO |

| Signal Name[1] | Description[2] | Type[3] |
|---|---|---|
| VCC-PLL | PLL Power Supply | P |
| X32KIN | Clock Input of 32768Hz Crystal | AI |
| X32KOUT | Clock Output of 32768Hz Crystal | AO |
| RTC-VIO | Internal LDO Output Bypass | AO |
| VCC-RTC | RTC Power Supply | P |

# 5. Electrical Characteristics

## 5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

***Note***: All measurements in the F1C800 Datasheet are taken at room temperature of 25°C unless other noted.

**Table 5-1. Absolute Maximum Ratings**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{I/O}$ | In/Out Current for Input and Output | | -40 | 40 | mA |
| AVCC | Power Supply for Analog Part | | -0.3 | 3.6 | V |
| VCC-IO[6:1] | Power Supply for Port B,D,F,G | | -0.3 | 3.6 | V |
| VDD-CORE[6:1] | Power Supply for System Core and CPU | | -0.3 | 1.5 | V |
| VCC-PLL | Power Supply for System PLL | | -0.3 | 3.6 | V |
| VCC-RTC | Power Supply for RTC | | -0.3 | 3.6 | V |
| VCC-USB | Power Supply for USB | | -0.3 | 3.6 | V |
| VCC-DRAM[11:1] | Power Supply for DRAM | | -0.3 | 1.98 | V |
| VCC-DSI | Power Supply for MIPI-DSI | | -0.3 | 3.6 | V |
| VCC-TVOUT | Power Supply for TVOUT | | -0.3 | 3.6 | V |
| VCC-TVIN | Power Supply for TVIN | | -0.3 | 3.6 | V |
| $T_{STG}$ | Storage Temperature Range | | -40 | 125 | °C |
| $V_{ESD}$ | Electrostatic Discharge | Human Body Model(HBM) (1) | -4000 | +4000 | V |
| | | Charged Device Model(CDM) (2) | -550 | +550 | V |
| $I_{Latch-up}$ | Latch-up I-test performance current-pulse injection on each IO pin (3) | | pass | | |
| | Latch-up over-voltage performance voltage injection on each IO pin (4) | | pass | | |

(1). Test method: JEDEC JS-002-2014(Class-3A). JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2). Test method: JEDEC JS-002-2014(Class-C2). JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
(3).Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.
(4).Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

## 5.2. Recommended Operating Conditions

All F1C800 modules are used under the operating conditions contained in Table 5-2.

**Table 5-2. Recommended Operating Conditions**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ta | Ambient Operating Temperature | -20 | - | +70 | °C |
| Tc | Case Temperature | TBD | - | TBD | °C |
| Tj | Junction Temperature | TBD | - | TBD | °C |

| | | | | | |
|---|---|---|---|---|---|
| AVCC | Power Supply for Analog Part | - | 2.8 | - | V |
| VCC-IO[6:1] | Power Supply for Port B,D,F,G | 3.0 | 3.3 | 3.6 | V |
| VDD-CORE[6:1] | Power Supply for System Core and CPU | 1.0 | 1.2 | 1.4 | V |
| VCC-PLL | Power Supply for System PLL | 3.0 | 3.3 | 3.3 | V |
| VCC-RTC | Power Supply for RTC | 3.0 | 3.3 | 3.3 | V |
| VCC-USB | Power Supply for USB | 3.0 | 3.3 | 3.6 | V |
| VCC-DRAM[11:1] | Power Supply for DRAM | 1.7 | 1.8 | 1.9 | V |
| VCC-DSI | Power Supply for MIPI DSI | 3.24 | 3.3 | 3.36 | V |
| VCC-TVOUT | Power Supply for TVOUT | 3.24 | 3.3 | 3.36 | V |
| VCC-TVIN | Power Supply for TVIN | 3.24 | 3.3 | 3.36 | V |

## 5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of F1C800.

**Table 5-3. DC Electrical Characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital GPIO | High-Level Input Voltage | $V_{IH}$ | 0.7 * VCC-IO | - | VCC-IO + 0.3 | V |
| | Low-Level Input Voltage | $V_{IL}$ | -0.3 | - | 0.3 * VCC-IO | V |
| | Input Pull-up Resistance | $R_{PU}$ | 50 | 100 | 150 | KΩ |
| | Input Pull-down Resistance | $R_{PD}$ | 50 | 100 | 150 | KΩ |
| | High-Level Input Current | $I_{IH}$ | - | - | 10 | uA |
| | Low-Level Input Current | $I_{IL}$ | - | - | 10 | uA |
| | High-Level Output Voltage | $V_{OH}$ | VCC-IO - 0.2 | - | VCC-IO | V |
| | Low-Level Output Voltage | $V_{OL}$ | 0 | - | 0.2 | V |
| | Tri-State Output Leakage Current | $I_{OZ}$ | -10 | - | 10 | uA |
| | Input Capacitance | $C_{IN}$ | - | - | 5 | pF |
| | Output Capacitance | $C_{OUT}$ | - | - | 5 | pF |

## 5.4. PLL Electrical Characteristics

### 5.4.1. CPU PLL Electrical Parameters

**Table 5-4. CPU PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 60 MHz ~ 2.1 GHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 1.5 ms |
| Max. Peak-to-Peak Supply Noise | 200 ps |

### 5.4.2. Audio PLL Electrical Parameters

**Table 5-5. Audio PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 72 MHz ~ 504 MHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 500 us |
| Max. Peak-to-Peak Supply Noise | 200 ps |

### 5.4.3. Peripheral0/1(2X) PLL Electrical Parameters

**Table 5-6. Peripheral0/1(2X) PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 504 MHz ~ 1.4 GHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 500 us |
| Max. Peak-to-Peak Supply Noise | 200 ps |

### 5.4.4. DDR1 PLL Electrical Parameters

**Table 5-7. DDR1 PLL Electrical Parameters**

| Parameter | Value | |
|---|---|---|
| Clock Output Range | 192 MHz ~ 1.6 GHz | |
| Reference Clock | 24 MHz | |
| Max. Lock Time | 2 ms | |
| Max. Peak-to-Peak Supply Noise | 200 MHz ~ 800 MHz | 200 ps |
| | 800 MHz ~ 1.3 GHz | 140 ps |
| | 1.3 GHz ~ 1.8 GHz | 100 ps |

### 5.4.5. Video0/1 PLL Electrical Parameters

**Table 5-8. Video0/1 PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192 MHz ~ 600 MHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 500 us |
| Max. Peak-to-Peak Supply Noise | 200 ps |

### 5.4.6. DE PLL Electrical Parameters

**Table 5-9. DE PLL Electrical Parameters**

| Parameter | Value |
|---|---|

| | |
|---|---|
| Clock Output Range | 192 MHz ~ 600 MHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 500 us |
| Max. Peak-to-Peak Supply Noise | 200 ps |

### 5.4.7. VE PLL Electrical Parameters

**Table 5-10. VE PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192 MHz ~ 600 MHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 500 us |
| Max. Peak-to-Peak Supply Noise | 200 ps |

### 5.4.8. MIPI PLL Electrical Parameters

**Table 5-11. MIPI PLL Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock Output Range | 192 MHz ~ 1400 MHz |
| Reference Clock | 24 MHz |
| Max. Lock Time | 500 us |
| Max. Peak-to-Peak Supply Noise | 200 ps |

## 5.5. KEYADC Electrical Characteristics

KEYADC is an analog-to-digital(ADC) converter for key application. Table 5-13 lists KEYADC electrical characteristics.

**Table 5-12. KEYADC Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ADC Resolution | - | 6 | - | bits |
| Full-scale Input Range | 0 | - | 0.667*AVCC | V |
| Quantizing Error | - | 1 | - | LSB |
| Clock Frequency | - | - | 250 | Hz |
| Conversion Time | - | 14 | - | ADC Clock Cycles |

## 5.6. TP Electrical Characteristics

TP controller is an analog-to-digital(ADC) converter. The ADC is a type of successive approximation register(SAR) converter. Table 5-14 lists TP electrical characteristics.

**Table 5-13. TP Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| ADC Resolution | - | 12 | - | bits |
| Full-scale Input Range | - | 3.3 | - | V |
| Clock Frequency | - | 1 | - | MHz |
| Conversion Time | - | 14*N | - | ADC Clock Cycles |
| **Note:** N is relevant with TP working mode. When TP is in single touch mode with pressure measurement, N is 4. When TP is in single touch mode without pressure measurement, N is 2. When TP is in general ADC mode, N is 1. | | | | |

## 5.7. Oscillator Electrical Characteristics

The 24.000MHz frequency is used to generate the main source clock for PLL and the main digital blocks. The 24.000MHz crystal is connected between the X24MIN and X24MOUT. The clock is provided through X24MIN. Table 5-15 lists the 24.000MHz crystal specifications.

**Table 5-14. 24MHz Crystal Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | - | 24.000 | - | MHz |
| $t_{ST}$ | Startup Time | - | - | - | ms |
| | Frequency Tolerance at 25 °C | -10 | - | +10 | ppm |
| | Oscillation Mode | Fundamental | | | - |
| | Maximum Change Over Temperature Range | -10 | - | +10 | ppm |
| $P_{ON}$ | Drive Level | - | - | 300 | uW |
| $C_L$ | Equivalent Load Capacitance | 12 | 18 | 22 | pF |
| $R_S$ | Series Resistance(ESR) | - | 25 | - | Ω |
| | Duty Cycle | 30 | 50 | 70 | % |
| $C_M$ | Motional Capacitance | - | - | - | pF |
| $C_{SHUT}$ | Shunt Capacitance | 5 | 6.5 | 7.5 | pF |
| $R_{BIAS}$ | Internal Bias Resistor | 0.5 | 0.6 | 0.7 | MΩ |

The 32768Hz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN.Table 5-16 lists the 32768Hz crystal specifications.

**Table 5-15. 32768Hz Crystal Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $1/(t_{CPMAIN})$ | Crystal Oscillator Frequency Range | - | 32768 | - | Hz |
| $t_{ST}$ | Startup Time | - | - | - | ms |
| | Frequency Tolerance at 25 °C | -20 | - | +20 | ppm |
| | Oscillation Mode | Fundamental | | | - |
| | Maximum Change Over Temperature Range | -20 | - | +20 | ppm |
| $P_{ON}$ | Drive Level | - | - | 1.0 | uW |
| $C_L$ | Equivalent Load Capacitance | - | 12.5 | - | pF |
| $R_S$ | Series Resistance(ESR) | - | - | 35 | kΩ |
| | Duty Cycle | 30 | 50 | 70 | % |
| $C_M$ | Motional Capacitance | - | - | - | F |
| $C_{SHUT}$ | Shunt Capacitance | - | 1.1 | - | pF |

## 5.8. Maximum Current Consumption

Table 5-17 lists the peak power consumption of F1C800.

**Table 5-16. Maximum Current Consumption**

| Parameter | Sub Parameter | Power Supply | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Internal Core Power | SYS | VDD-CORE | @1.2V | - | - | TBD | mA |
| GPIO Power | | VCC-IO | @3.3V | - | - | TBD | mA |
| Memory I/O Power | | VCC-DRAM | @1.8V | - | - | TBD | mA |
| Oscillator | | VCC-PLL | @3.3V | - | - | TBD | mA |
| USB 3.0V Power of PHY | | VCC-USB | @3.3V | - | - | TBD | mA |
| RTC Power | | VCC-RTC | @3.3V | - | - | TBD | mA |
| ADC Analog Power | | AVCC | @2.8V | - | - | TBD | mA |
| DAC Analog Power | | AVCC | @2.8V | - | - | TBD | mA |
| PLL Power | | VCC-PLL | @3.3V | - | - | TBD | mA |

## 5.9. External Memory Electrical Characteristics

### 5.9.1. SMHC AC Electrical Characteristics

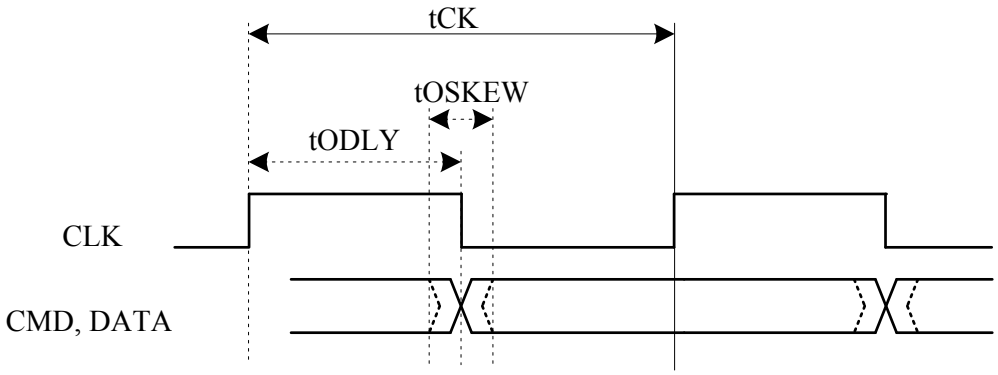



**Figure 5-1. SMHC Output Timing Diagram**

**Table 5-17. SMHC Output Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty Cycle | DC | 45 | 50 | 55 | % |
| **Output CMD, DATA(referenced to CLK)** | | | | | |
| CMD, Data output delay time | tODLY | - | 0.25 | 0.5 | UI |
| Data output delay skew time | tOSKEW | - | - | 0.4 | ns |
| **Note:**<br>(1).Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50 MHz.<br>(2).The driver strength level of GPIO is 2 for test. | | | | | |

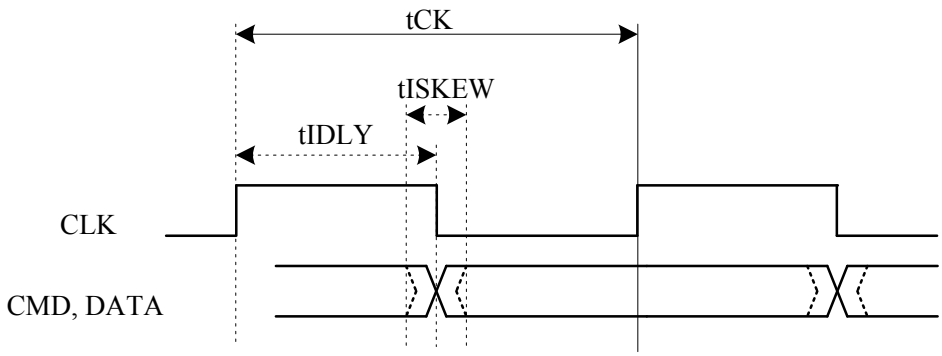



**Figure 5-2. SMHC Input Timing Diagram**

**Table 5-18. SMHC Input Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CLK** | | | | | |
| Clock frequency | tCK | 0 | 50 | 50 | MHz |
| Duty Cycle | DC | 45 | 50 | 55 | % |
| **Input CMD, DATA(referenced to CLK 50MHz)** | | | | | |
| Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay | tIDLY | - | - | 20 | ns |
| Data input skew time in SDR mode | tISKEW | - | - | 1 | ns |
| **Note:**<br>(1).The driver strength level of GPIO is 2 for test. | | | | | |

# 5.10. External Peripherals Electrical Characteristics

## 5.10.1. LCD AC Electrical Characteristics

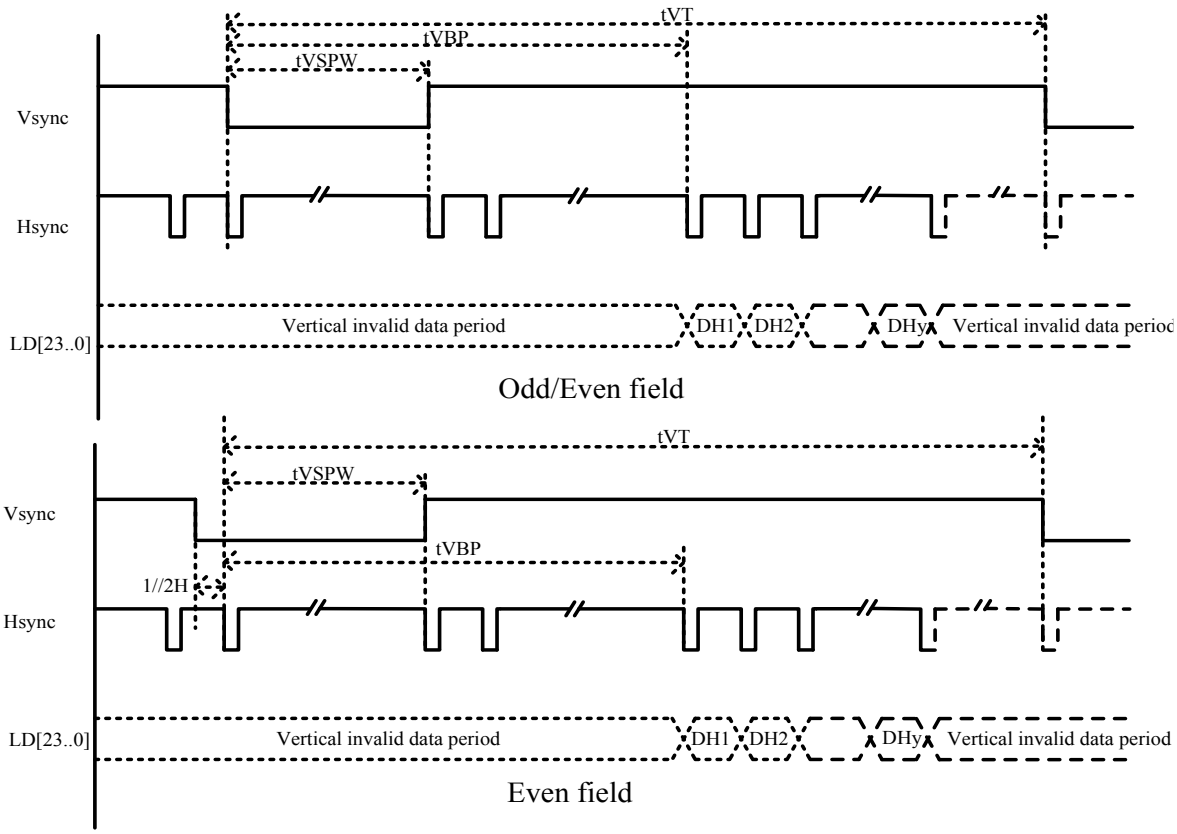



**Figure 5-3. HV_IF Interface Vertical Timing Diagram**

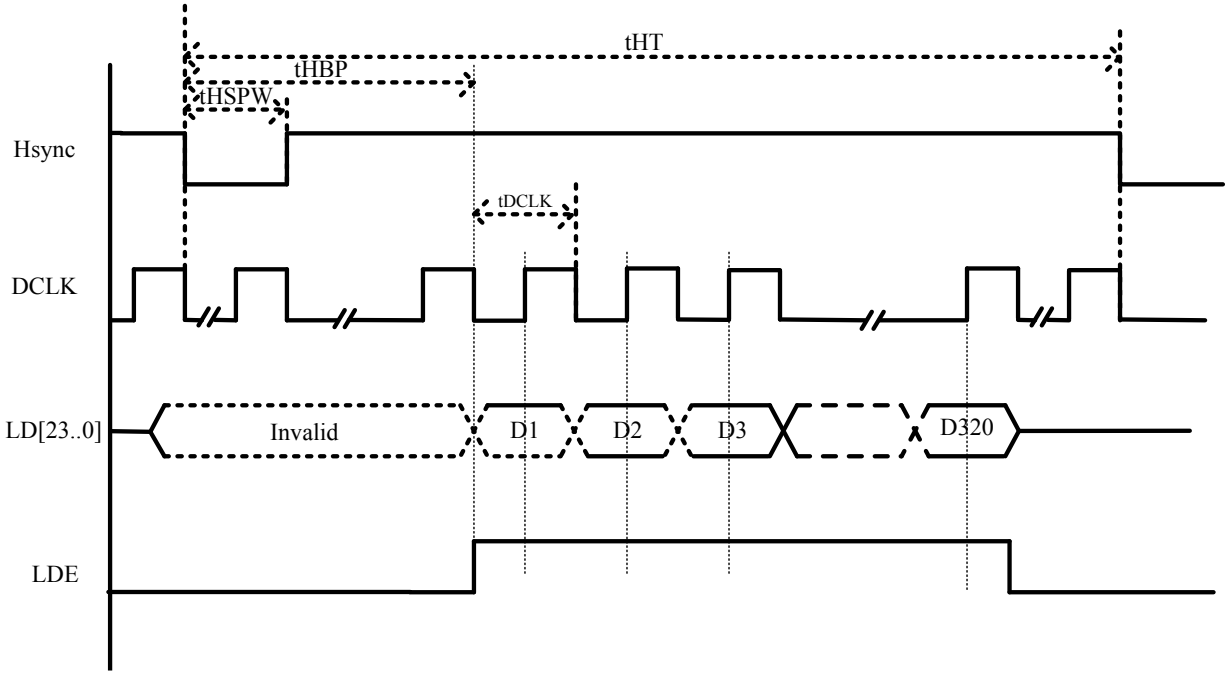



**Figure 5-4. HV_IF Interface Parallel Mode Horizontal Timing Diagram**

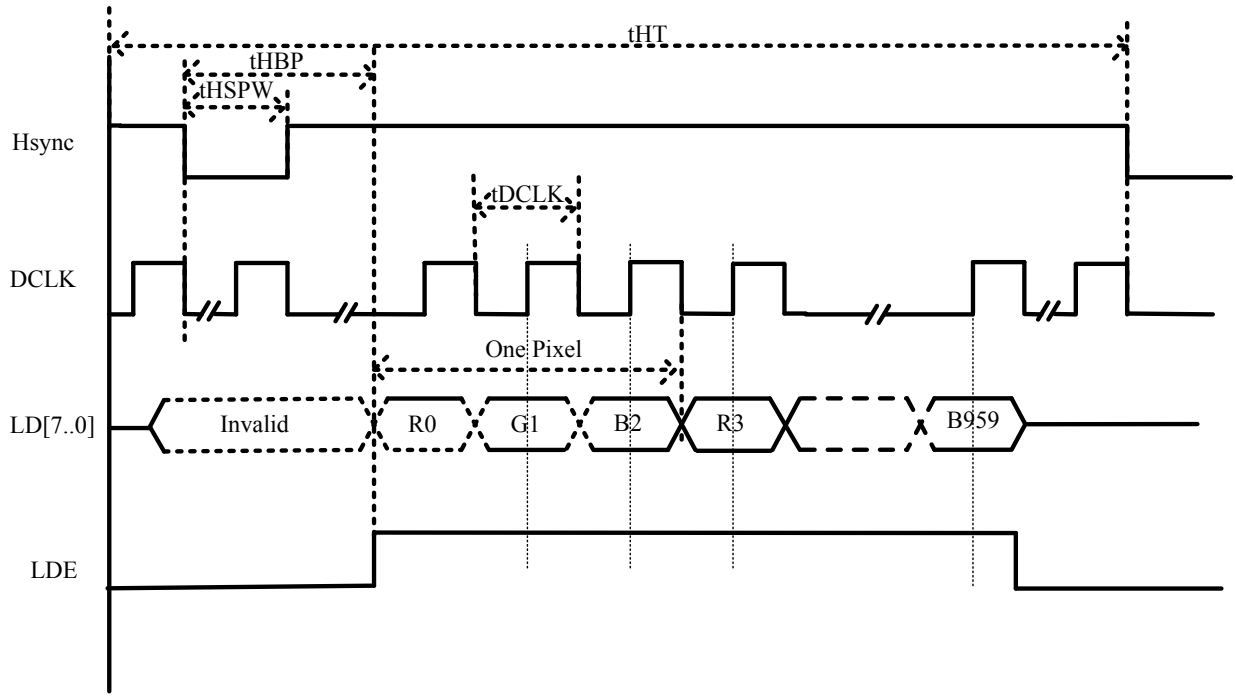



**Figure 5-5. HV_IF Interface Serial Mode Horizontal Timing Diagram**

**Table 5-19. LCD HV_IF Interface Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DCLK cycle time | tDCLK | 5 | - | - | ns |
| HSYNC period time | tHT | - | HT+1 | - | tDCLK |
| HSYNC width | tHSPW | - | HSPW+1 | - | tDCLK |
| HSYNC back porch | tHBP | - | HBP+1 | - | tDCLK |
| VSYNC period time | tVT | - | VT/2 | - | tHT |
| VSYNC width | tVSPW | - | VSPW+1 | - | tHT |
| VSYNC back porch | tVBP | - | VBP+1 | - | tHT |

**Note:**
(1). Vsync: Vertical sync, indicates one new frame
(2). Hsync: Horizontal sync, indicate one new scan line
(3). DCLK: Dot clock, pixel data are sync by this clock
(4). LDE: LCD data enable
(5). LD[23..0]: 18Bit RGB/YUV output from input FIFO for panel

### 5.10.2. SPI AC Electrical Characteristics

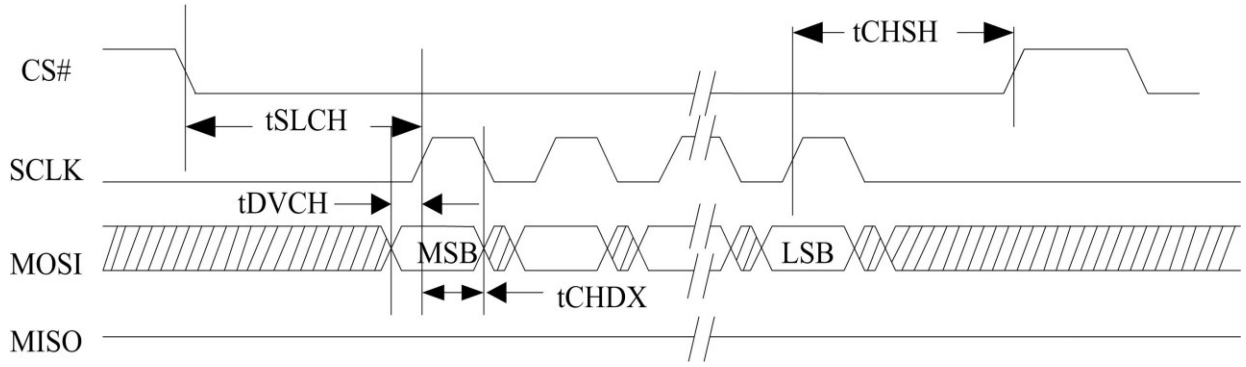



**Figure 5-6. SPI MOSI Timing Diagram**

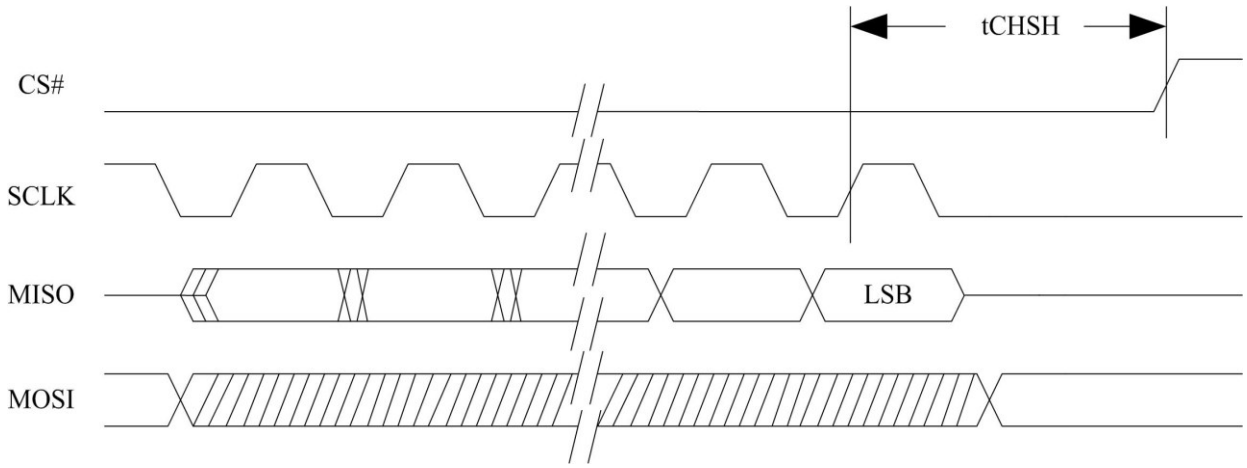



**Figure 5-7. SPI MISO Timing Diagram**

**Table 5-20. SPI Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CS# active setup time | tSLCH | - | 2T | - | ns |
| CS# active hold time | tCHSH | - | 2T(1) | - | ns |
| Data in setup time | tDVCH | - | T/2-3 | - | ns |
| Data in hold time | tCHDX | - | T/2-3 | - | ns |
| **Note (1)**:T is the cycle of clock. | | | | | |

### 5.10.3. UART AC Electrical Characteristics

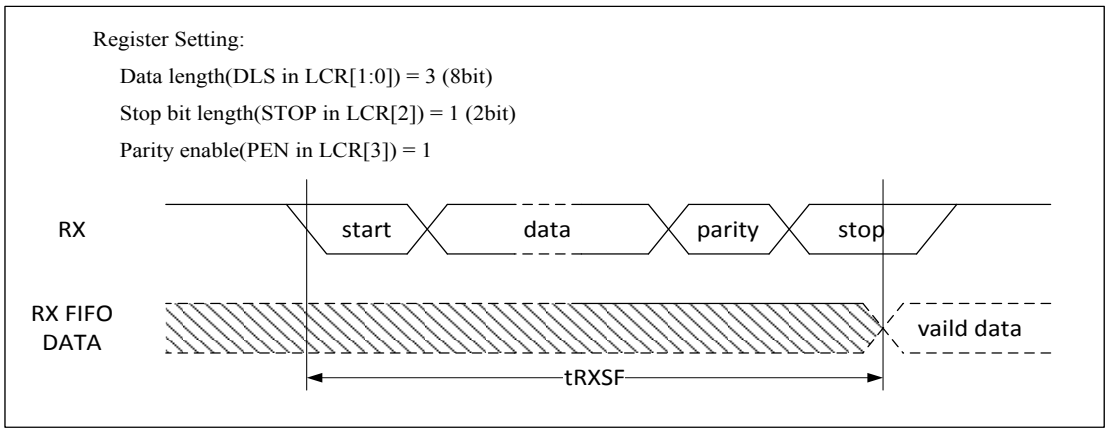



**Figure 5-8. UART RX Timing Diagram**

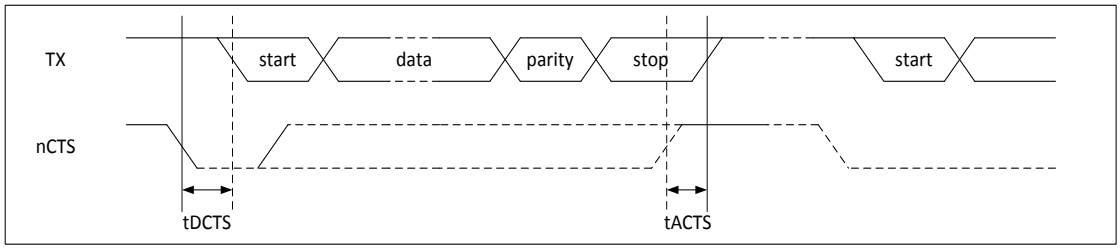



**Figure 5-9. UART nCTS Timing Diagram**

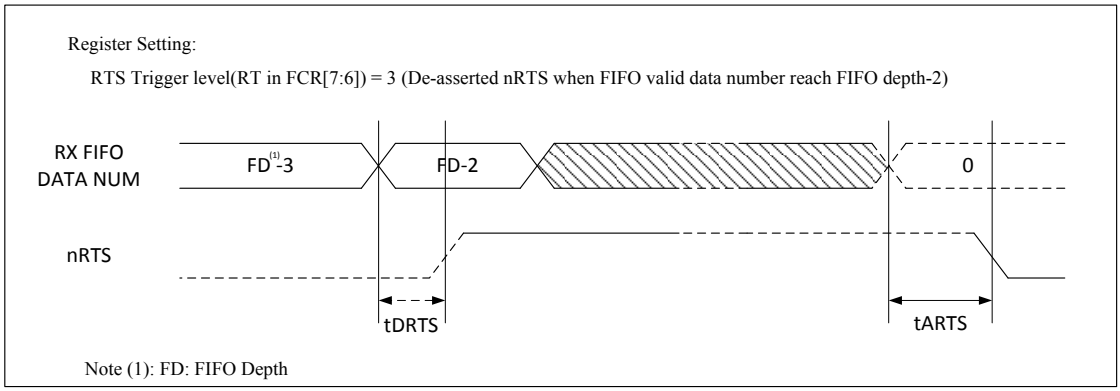



**Figure 5-10. UART nRTS Timing Diagram**

**Table 5-21. UART Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX start to RX FIFO | tRXSF | 10.5 × BRP(1) | - | 11 × BRP(1) | ns |
| Delay time of de-asserted nCTS to TX start | tDCTS | - | - | BRP(1) | ns |
| Step time of asserted nCTS to stop next transmission | tACTS | BRP(1)/4 | - | - | ns |
| Delay time of de-asserted nRTS | tDRTS | - | - | BRP(1) | ns |
| Delay time of asserted nRTS | tARTS | - | - | BRP(1) | ns |
| **Note (1)**: BRP(Baud-Rate Period). | | | | | |

### 5.10.4. TWI AC Electrical Characteristics

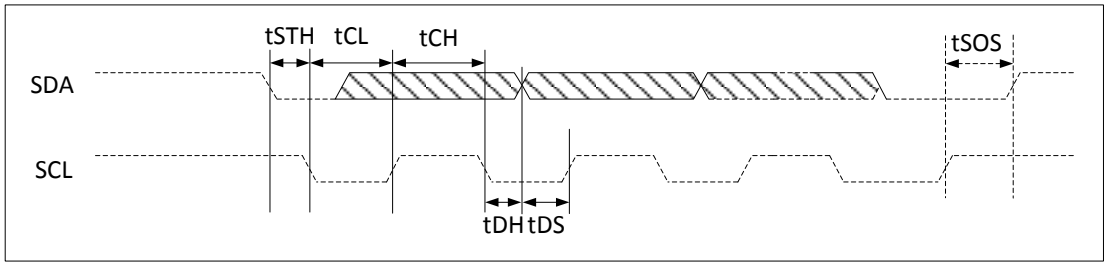



**Figure 5-11. TWI Timing Diagram**

**Table 5-22. TWI Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| High period of SCL | tCH | 0.96 | - | - | μs |
| Low period of SCL | tCL | 1.5 | - | - | μs |
| SCL hold time for START condition | tSTH | 1.5 | - | - | μs |
| SCL step time for STOP condition | tSOS | 1.6 | - | - | μs |
| SDA hold time | tDH | 0.82 | - | - | μs |
| SDA step time | tDS | 0.72 | - | - | μs |

### 5.10.5. CIR Receiver AC Electrical Characteristics

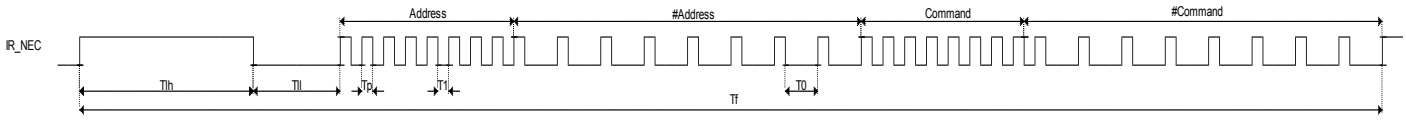



**Figure 5-12. CIR Receiver Timing Diagram**

**Table 5-23. CIR Receiver Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frame Period | Tf | - | 67.5 | - | ms |
| Lead Code High Time | Tlh | - | 9 | - | ms |
| Lead Code Low Time | Tll | - | 4.5 | - | ms |
| Pulse Time | Tp | - | 560 | - | us |
| Logical 1 Low Time | T1 | - | 1680 | - | us |
| Logical 0 Low Time | T0 | - | 560 | - | us |

### 5.10.6. SCR AC Electrical Characteristics

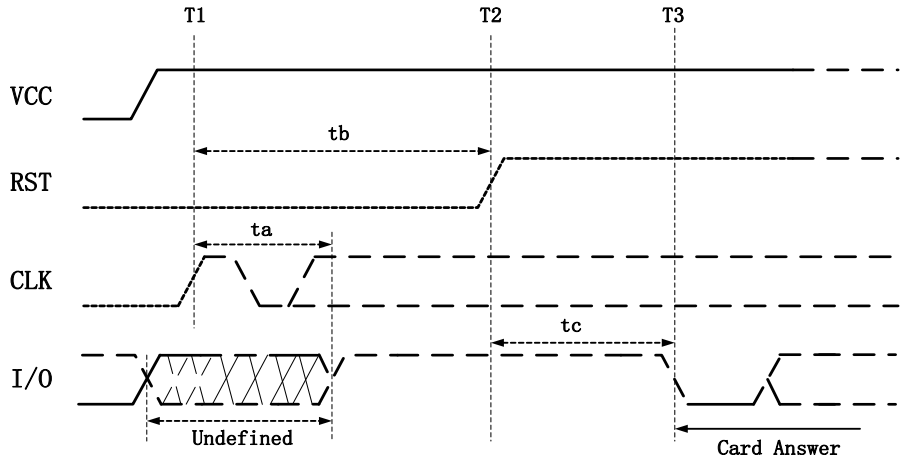



**Figure 5-13. SCR Activation and Cold Reset Timing Diagram**

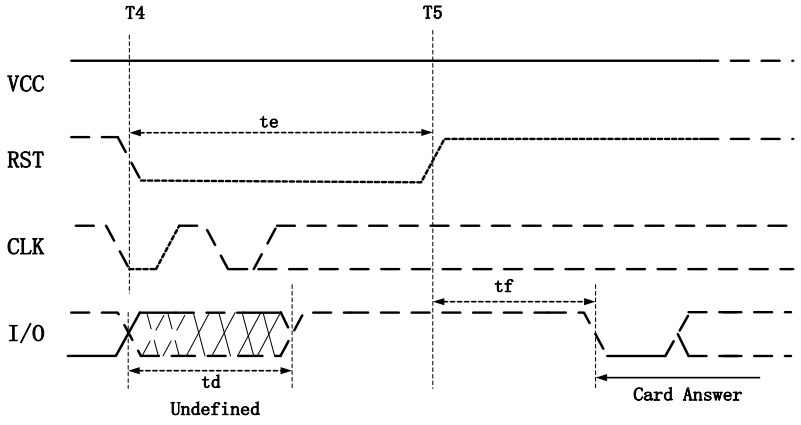



**Figure 5-14. SCR Warm Reset Timing Diagram**

**Table 5-24. SCR Timing Constants**

| Symbol | Min | Type | Max | Unit |
|---|---|---|---|---|
| ta | - | - | 200/f | us |
| tb | 400/f | - | - | us |
| tc | 400/f | - | 40000/f | us |
| td | - | - | 200/f | us |
| te | 400/f | - | - | us |
| tf | 400/f | - | 40000/f | us |

**Note:**
(1). Activation: Before time T1
(2). Cold Reset: After time T1
(3). T1: The clock signal is applied to CLK at time T1.
(4). T2: The RST is put to state H.
(5). T3: The card begin answer at time T3
(6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
(7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
(8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
(9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).

(10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12). f is the frequency of clock.

### 5.10.7. TSC AC Electrical Characteristics

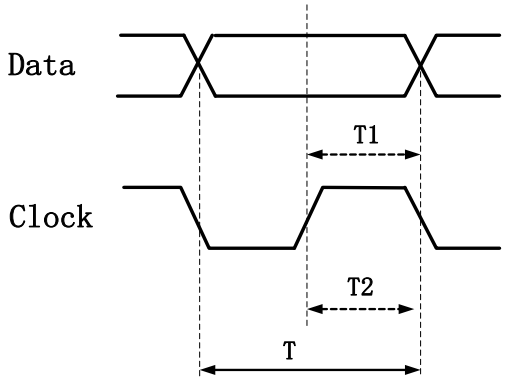



**Figure 5-15. TSC Data and Clock Timing**

**Table 5-25. TSC Timing Constants**

| Parameter | Symbol | Min | Type | Max | Unit |
|---|---|---|---|---|---|
| Data hold time | T1 | T/2-T/10 | T(1)/2 | T/2+T/10 | us |
| Clock pulse width | T2 | T/2-T/10 | T/2 | T/2+T/10 | us |
| **Note (1):**T is the cycle of clock. | | | | | |

### 5.10.8. I2S/PCM AC Electrical Characteristics

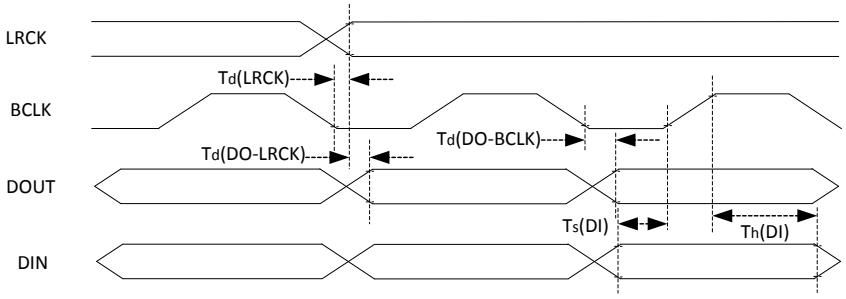



**Figure 5-16. I2S/PCM Master Mode Timing**

**Table 5-26. I2S/PCM Master Mode Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LRCK delay | $T_d$(LRCK) | - | - | 10 | ns |
| LRCK to DOUT delay(For LJF) | $T_d$(DO-LRCK) | - | - | 10 | ns |
| BCLK to DOUT delay | $T_d$(DO-BCLK) | - | - | 10 | ns |
| DIN setup | $T_s$(DI) | 4 | - | - | ns |
| DIN hold | $T_h$(DI) | 4 | - | - | ns |
| BCLK rise time | $T_r$ | - | - | 8* | ns |
| BCLK fall time | $T_f$ | - | | 8 | ns |
| **Note:** * is relevant with the size of capacitive loads. | | | | | |

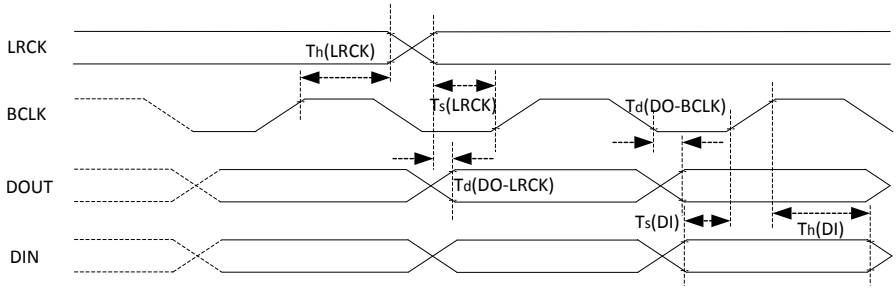



**Figure 5-17. I2S/PCM Slave Mode Timing**

**Table 5-27. I2S/PCM Slave Mode Timing Constants**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LRCK setup | $T_s$(LRCK) | 4 | - | - | ns |
| LRCK hold | $T_h$(LRCK) | 4 | - | - | ns |
| LRCK to DOUT delay(For LJF) | $T_d$(DO-LRCK) | - | - | 10 | ns |
| BCLK to DOUT delay | $T_d$(DO-BCLK) | - | - | 10 | ns |
| DIN setup | $T_s$(DI) | 4 | - | - | ns |
| DIN hold | $T_h$(DI) | 4 | - | - | ns |
| BCLK rise time | $T_r$ | - | - | 4 | ns |
| BCLK fall time | $T_f$ | - | - | 4 | ns |

## 5.11. Power-up and Power-down Sequence

The section provides information about the F1C800 power up and power down sequence requirements.

### 5.11.1. Power-up Sequence

The following steps give an example of power-up sequence supported by the F1C800 device. All power rails start to ramp up simultaneously. During the entire power-up sequence, the RESET pin must be held on low until all power domains are stable. The low level of RESET signal is less than 1.8V.

Figure 5-18 shows an example of the device power up sequence.

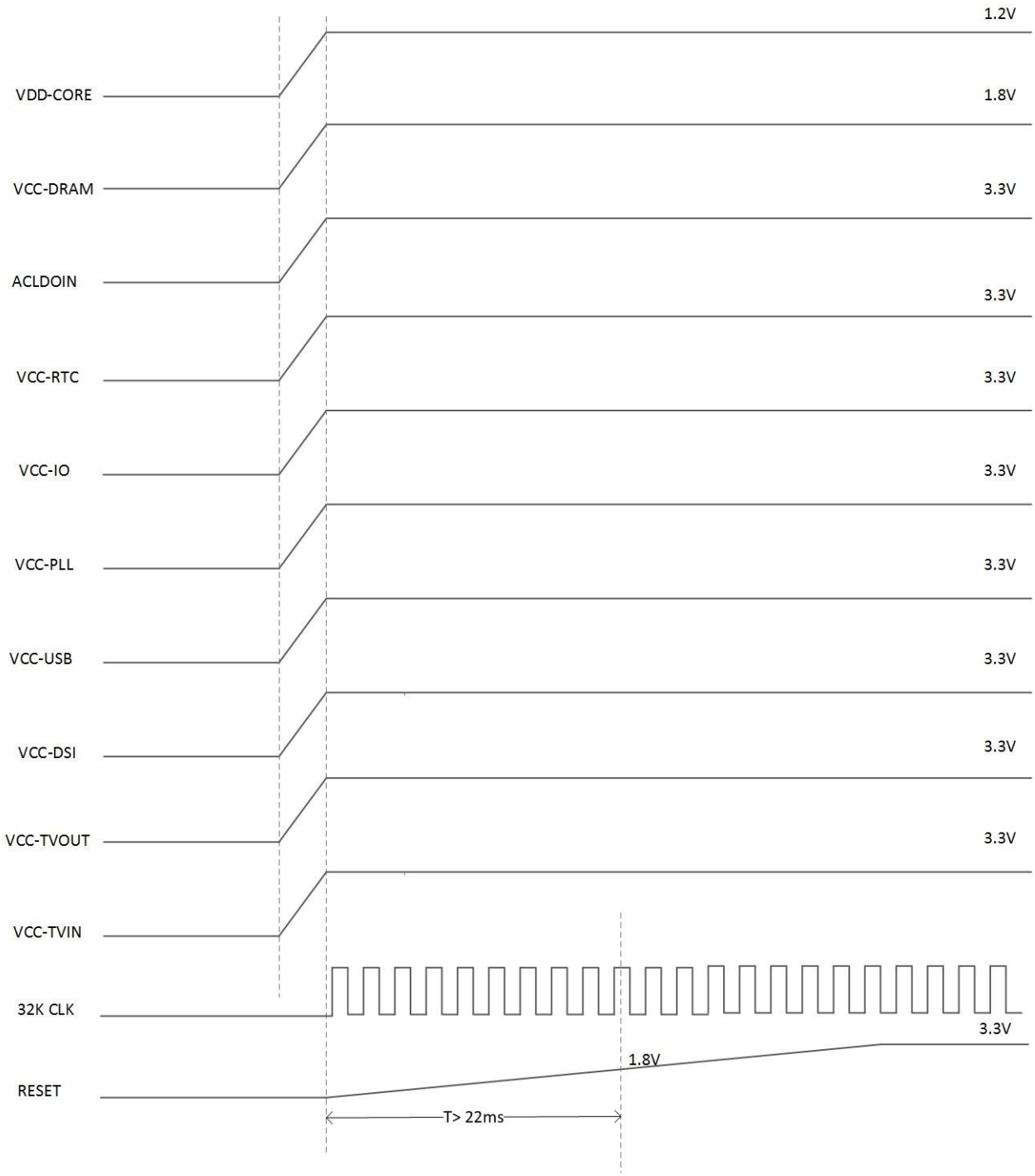



**Figure 5-18. F1C800 Power Up Sequence**

### 5.11.2. Power-down Sequence

For F1C800 processor, the power-down sequence has no special restrictions.

# 6. Package Thermal Characteristics

For reliability and operability concerns, the absolute maximum junction temperature of F1C800 has to be below 125°C.The testing PCB is based on 4 layers. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the system design and temperature could be different with JEDEC JESD51 , the simulating resulting data is a reference only, please prevail in the actual application condition test.

**Table 6-1. F1C800 Thermal Resistance Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Ta | Ambient Operating Temperature | -20 | - | +70 | °C |
| $T_J$ | Junction Temperature | - | - | +125 | °C |
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance | - | 38.7 | - | °C/W |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | - | TBD | - | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | - | TBD | - | °C/W |
| $\psi_{JT}$ | Junction-to-Top Characterization Parameter | - | TBD | - | °C/W |
| $\psi_{JB}$ | Junction-to-Board Characterization Parameter | - | TBD | - | °C/W |

# 7. Pin Assignment

## 7.1. Pin Map

For F1C800, eLQFP128, 14 mm x 14 mm package is offered. The pin maps are illustrated in Figure 7-1 for this package.

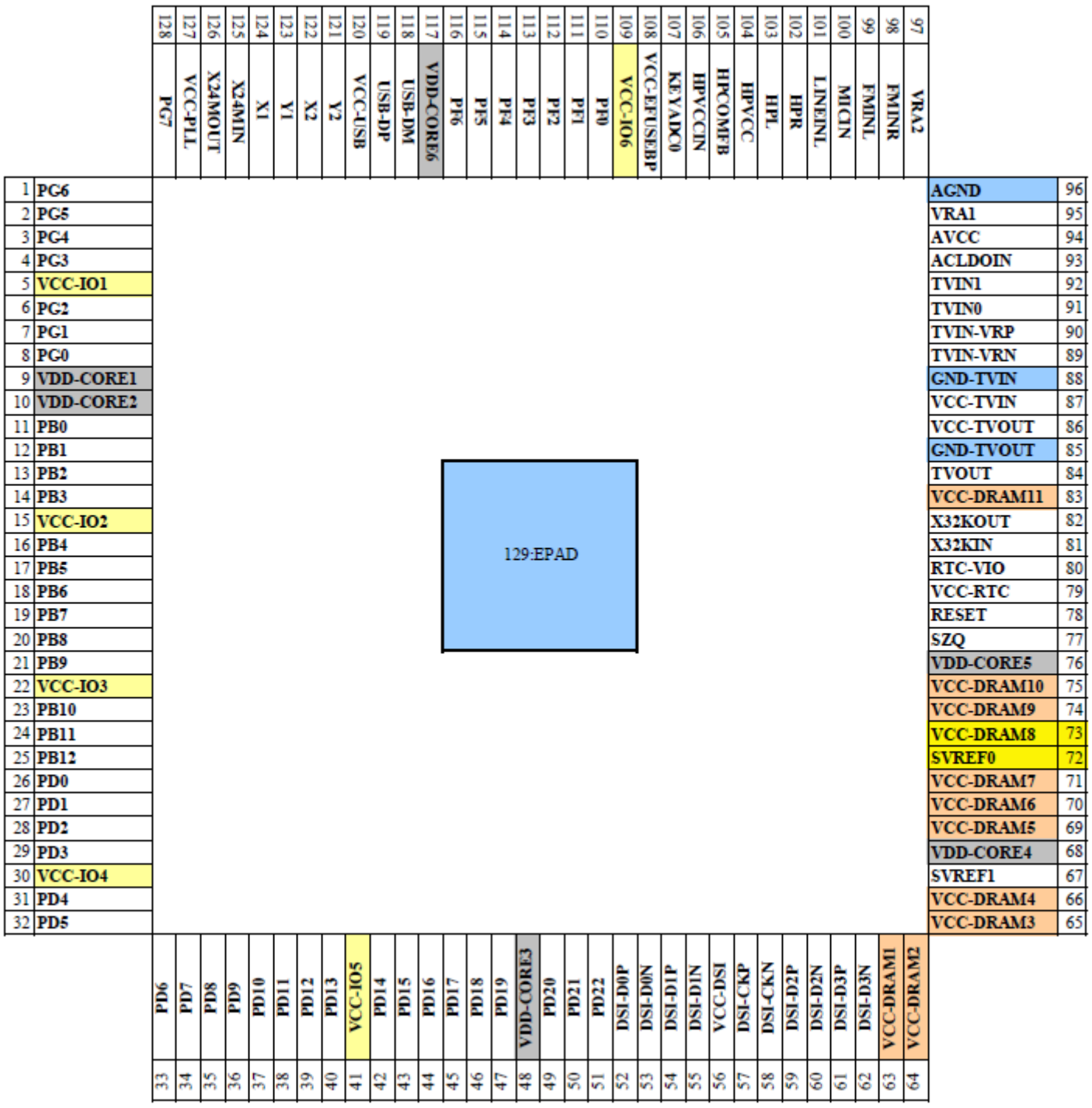
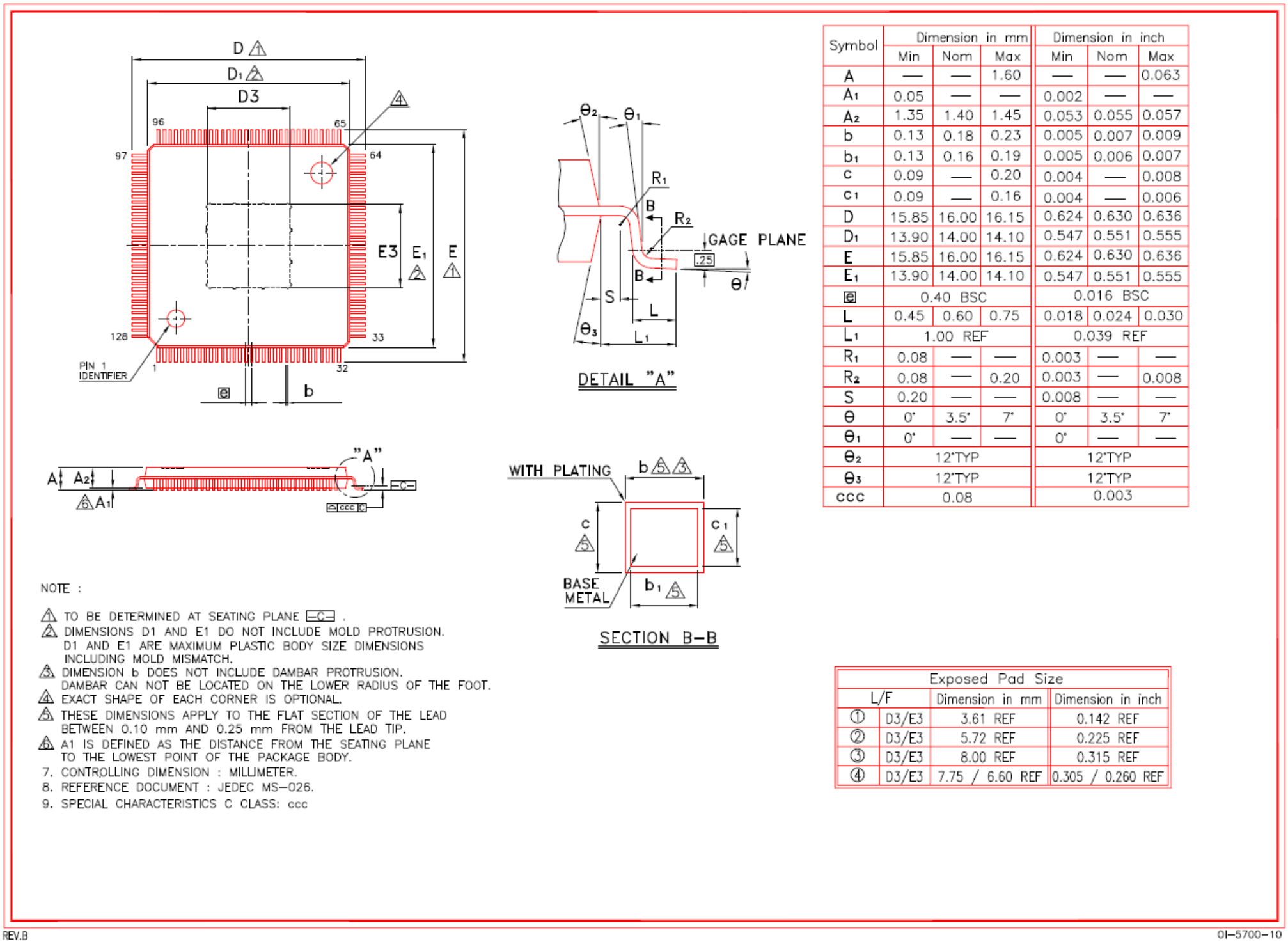



**Figure 7-1. F1C800 Pin Map**

## 7.2. Package Dimension

Figure 7-2 shows package views and package dimensions of F1C800.




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | — | 0.002 | — | — |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.13 | 0.18 | 0.23 | 0.005 | 0.007 | 0.009 |
| b1 | 0.13 | 0.16 | 0.19 | 0.005 | 0.006 | 0.007 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| c1 | 0.09 | — | 0.16 | 0.004 | — | 0.006 |
| D | 15.85 | 16.00 | 16.15 | 0.624 | 0.630 | 0.636 |
| D1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 15.85 | 16.00 | 16.15 | 0.624 | 0.630 | 0.636 |
| E1 | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| R1 | 0.08 | — | — | 0.003 | — | — |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| S | 0.20 | — | — | 0.008 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 12°TYP | | | 12°TYP | | |
| θ3 | 12°TYP | | | 12°TYP | | |
| ccc | 0.08 | | | 0.003 | | |

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

| Exposed Pad Size | | | |
|---|---|---|---|
| L/F | | Dimension in mm | Dimension in inch |
| ① | D3/E3 | 3.61 REF | 0.142 REF |
| ② | D3/E3 | 5.72 REF | 0.225 REF |
| ③ | D3/E3 | 8.00 REF | 0.315 REF |
| ④ | D3/E3 | 7.75 / 6.60 REF | 0.305 / 0.260 REF |

REV.B

0I–5700–10

**Figure 7-2. F1C800 Package Dimension**

Allwinner Technology Co.,Ltd.

No.9 Technology Road 2,High-Tech Zone,

Zhuhai, Guangdong Province, China

Contact US:

Service@allwinnertech.com

www.allwinnertech.com