V833/V831 Professional IP Camera SoC

Datasheet

Revision 1.1

Jun.02, 2020

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Revision History

Revision	Date	Description
1.0	Mar.03, 2020	Initial release version
1.1	Jun.02, 2020	Delete SPI2 information of V831

About This Document

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module about V833/V831. The document also describes the interface timings and related parameters, the pins, pin usages, performance parameters, and package dimension of V833/V831 in detail.

CAUTION

The document defines two devices: V833, V831. Throughout this document, the devices are referred to as V833/V831 when material being presented applies to all of them. Unless other stated, V833 and V831 contents are consistent.

Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.

NOTE	Provides additional information to emphasize or supplement important points of the main text.

Notes

Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write
R/WAC	Read/Write-Automatic-Clear, clear the bit automatically when the operation of complete. Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear. Writing 1 has no effect
R/W1C	Read/Write 1 to Clear. Writing 0 has no effect
R/W1S	Read/Write 1 to Set. Writing 0 has no effect
W	Write Only

Reset Value Conventions

In the register definition tables:
If other column value in a bit or multiple bits row is "/", that this bit or these multiple bits are unused.
If the default value of a bit or multiple bits is "UDF", that the default value is undefined.

Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression,X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

Acronyms and Abbreviations

The following table contains acronyms and abbreviations used in this document.

ADC	Analog-to-Digital Converter
AE	Automatic Exposure
AEC	Audio Echo Cancellation
AES	Advanced Encryption Standard
AF	Automatic Focus
AGC	Automatic Gain Control
AHB	AMBA High-Speed Bus
ALC	Automatic Level Control
ANR	Active Noise Reduction
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
AVS	Audio Video Standard
AWB	Automatic White Balance
BROM	Boot ROM
CMOS	Complementary Metal-Oxide Semiconductor
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DDR	Double Data Rate
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card

ESD	Electrostatic Discharge
FBGA	Fine Pitch Ball Grid Array
FEL	Fireware Exchange Launch
FIFO	First In First Out
GIC	Generic Interrupt Controller
GPIO	General Purpose Input Output
HD	High Definition
HDCP	High-bandwidth Digital Content Protection
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
ISP	Image Signal Processor
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid-Crystal Display
LFBGA	Low Profile Fine Pitch Ball Grid Array
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MIC	Microphone
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
NVM	Non Volatile Storage Medium
OHCI	Open Host Controller Interface
OSD	On-Screen Display
OTP	One Time Programmable
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
R	Read only/non-Write
RGB	Read Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory

RSA	Rivest-Shamir-Adleman
RTC	Real Time Clock
SAR	Successive Approximation Register
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SDRAM	Sychronous Dynamic Random Access Memory
SDXC	Secure Digital Extended Capacity
SLC	Single-Level Cell
SMC	Secure Memory Control
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TDES	Triple Data Encryption Standard
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

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Tables

Chapter 1 Product Description

1.1. Description

1.1.1. V833

The V833 is a high performance and low-power IP Camera SoC for the video encoding industry that can be widely used in security monitor, SDV, driving recorder, Police BODY-WORN CAMERA, etc. The V833 integrates single-core ARM Cortex-A7 that supports frequency up to 1.2GHz. Integrated H.264/H.265 video encoding supports encoding of multiple streams, the performance of H.265 video encoding is up to 5M@30fps + 720p@30fps. The V833 integrates the latest generation of ISP image processor, NPU, EISE, wide-angle distortion correction, fisheye and PTZ calibration and other image correction algorithms to achieve professional image effects. The V833 adopts advanced low-power technology and low-power consumption architecture design, which significantly reduces the BOM cost. The Allwinner SDK features high stability and ease of use, supports rapid mass production.

1.1.2. V831

The V831 is a high performance and low-power IP Camera SoC for the video encoding industry that can be widely used in security monitor, SDV, driving recorder, Police BODY-WORN CAMERA, etc. The V831 integrates single-core ARM Cortex-A7 that supports frequency up to 800MHz. Integrated H.264/H.265 video encoding supports encoding of multiple streams, the performance of H.265 video encoding is up to 1080p@30fps. The V831 integrates the latest generation of ISP image processor, NPU, EISE, wide-angle distortion correction, fisheye and PTZ calibration and other image correction algorithms to achieve professional image effects. To reduce the BOM cost, a 64MB DDR2 die is embedded for the V831. The V831 adopts advanced low-power technology and low-power consumption architecture design, which significantly reduces the BOM cost. The Allwinner SDK features high stability and ease of use, supports rapid mass production.

1.2. Device Difference

The V833/V831 is configured with different sets of features in different devices. The feature differences across different devices are shown in Table 1-1. For detail pins, see the *V833/V831_PINOUT.xls*.

Table 1- 1. Device Feature Differences

Contents	V833	V831
CPU	Up to 1.2GHz	Up to 800MHz
Video encoder	H.264, up to 5M@20fps H.265, up to 5M@30fps JPEG, up to 1080p@60fps	H.264, up to 1080p@30fps H.265, up to 1080p@30fps JPEG, up to 1080p@30fps
NPU	0.4T	0.2T
EISE	Up to 1080p@60fps	Up to 1080p@30fps
SDRAM	DDR2/DDR3/DDR3L	SIP 64MB DDR2
SMHC	SMHC x3 (SDC0, SDC1, SDC2)	SMHC x2 (SDC0, SDC1)
SPI	SPI x3 (SPI0, SPI1, SPI2)	SPI x2 (SPI0, SPI1)
LCD	Parallel RGB, Serial RGB, i8080	Serial RGB, i8080
DSPO	BT1120, BT656	BT656
I2S	I2S x2 (I2S0, I2S1)	I2S x1 (I2S0)
Parallel CSI	Support	No support
Ethernet	10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces	10/100 Mbit/s Ethernet port with RMII interface
TWI	TWI x5 (TWI0, TWI1, TWI2, TWI3, S_TWI0)	TWI x4 (TWI0, TWI1, TWI2, TWI3)
RSB	Support	No support
GPADC	2-ch	1-ch
Audio codec	Output: LINEOUTP/N Input: MICIN1P/N, LINEINL	Output: LINEOUTP Input: MICIN1P/N
MIPI CSI	4-lane, up to 8M@30fps	2-lane, up to 1080p@60fps
MIPI DSI	Support	No support
Package	LFBGA273	QFN88

1.3. Application Scenarios

1.3.1. V833 HD IP Camera Solution

Figure 1-1 shows the HD IP camera solution of the V833.

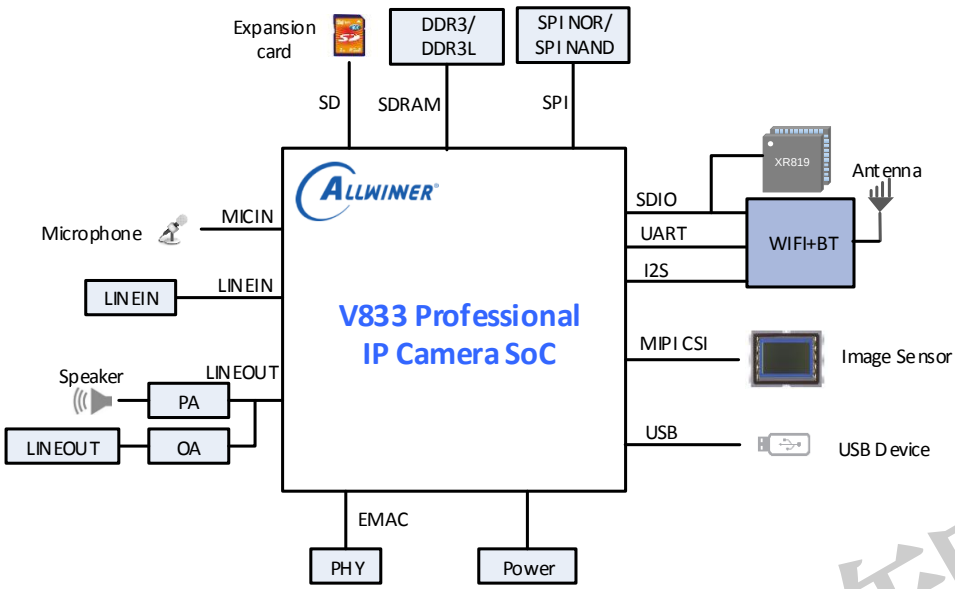

Figure 1- 1. V833 HD IP Camera Solution

1.3.2. V831 HD IP Camera Solution

Figure 1-2 shows the HD IP camera solution of the V831.

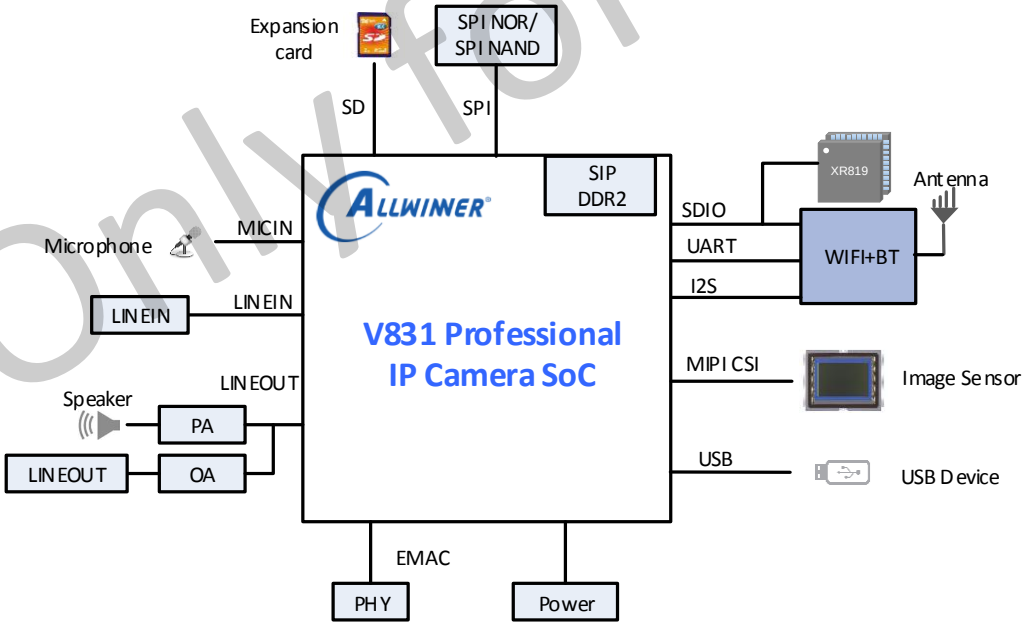

Figure 1- 2. V831 HD IP Camera Solution

1.4. Architecture

1.4.1. Block Diagram

1.4.1.1. V833

The logic block diagram of the V833 is shown in Figure 1-3.

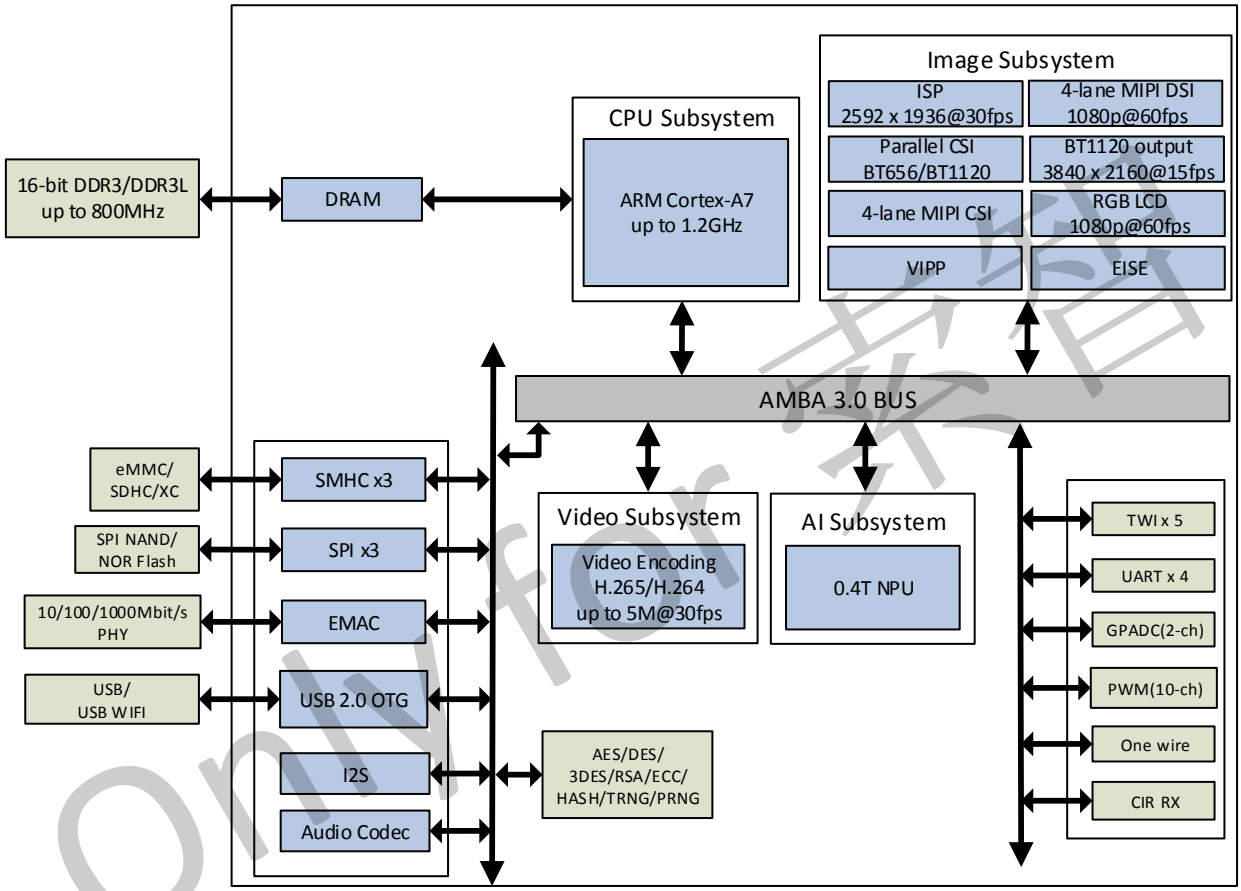

Figure 1- 3. V833 Block Diagram

1.4.1.2. V831

The logic block diagram of the V831 is shown in Figure 1-4.

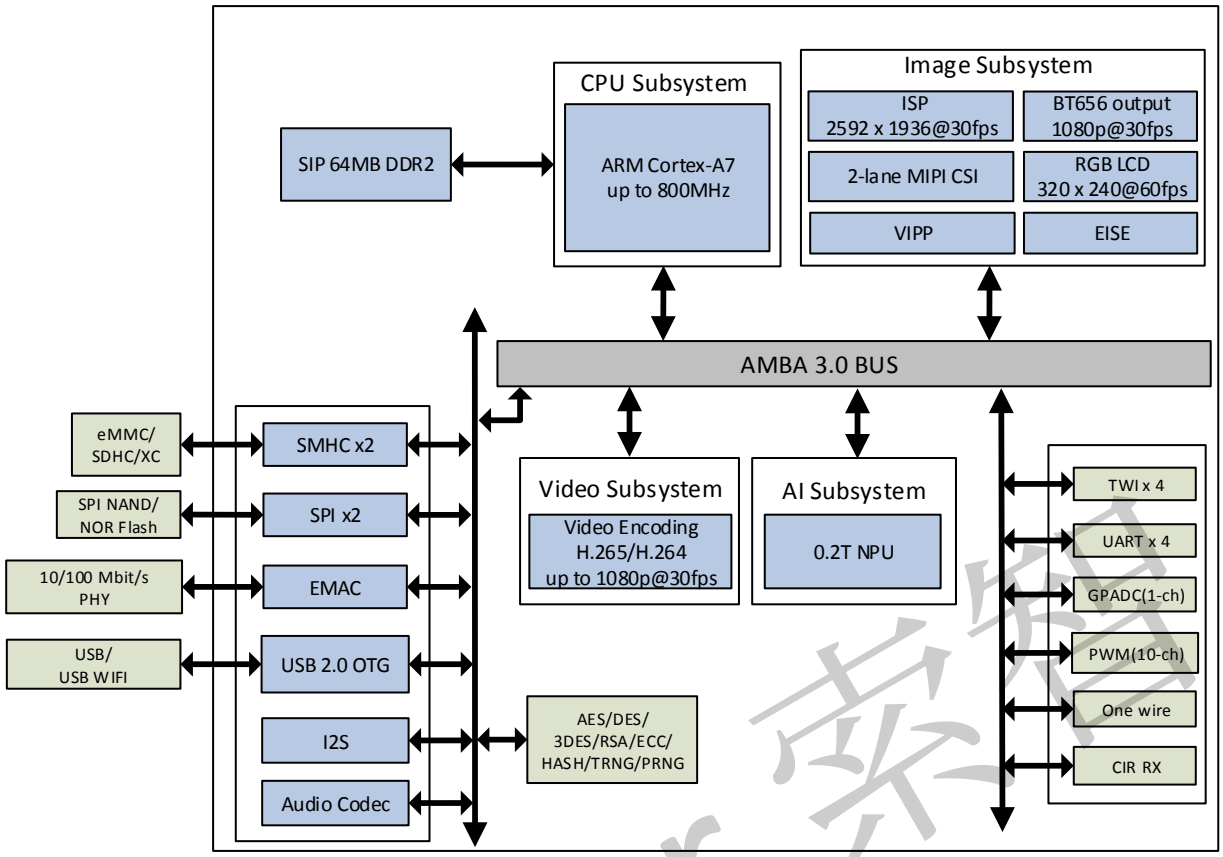

Figure 1- 4. V831 Block Diagram

1.4.2. Processor Core

- Single-core ARM Cortex™-A7 Processor
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- 32KB L1 Instruction cache and 32KB L1 Data cache
- 128KB L2 cache

1.4.3. Video Encoding Specifications

- H.264 BP/MP/HP
- H.265 MP
- H.264/H.265 supports I/P frame, dual-P frame
- JPEG baseline

1.4.4. Video Encoding Performance

For V833:

- Maximum 8-megapixel resolution for H.264/H.265 encoding
- Real-time multiple streams H.264/H.265 encoding capability:
  5M@20fps + 1080p@20fps (or 1080p@60fps + VGA@60fps) H.264
  5M@30fps + 720p@30fps (or 1080p@90fps) H.265
- JPEG snapshot performance of 1080p@60fps independently
- Supports three kinds of bit-rate control modes: constant bit rate(CBR), variable bit rate(VBR) and FIXQP
- Output bit-rate ranging from 2kbit/s to 100Mbit/s
- Maximum 16 regions of interest(ROIs) without encoding for AI
- Encoding frame rate ranging from 1/16 fps to 60 fps

For V831:

- Maximum 2-megapixel resolution for H.264/H.265 encoding
- Real-time multiple streams H.264/H.265 encoding capability:
  1080p@30fps H.264
  1080p@30fps H.265
- JPEG snapshot performance of 1080p@30fps independently
- Supports three kinds of bit-rate control modes: constant bit rate(CBR), variable bit rate(VBR) and FIXQP
- Output bit-rate ranging from 2kbit/s to 100Mbit/s
- Maximum 16 regions of interest(ROIs) without encoding for AI
- Encoding frame rate ranging from 1/16fps to 30fps

1.4.5. Video and Graphics Processing

- Supports Electronic Image Stabilization Engine(EISE)
- Lens distortion correction, fisheye(wall mounting/top mounting/bottom mounting) and PTZ calibration
- Picture rotation by 90^0, 180^0 or 270^0
- Supports 2 Video channels, one up to 1080p@60fps, the other up to 720p@60fps
- Supports 1 UI channel, up to 1080p@60fps
- Blending of 2 Video channels and 1 UI channel
- Supports SmartColor for excellent display experience

1.4.6. NPU

- **V833**: Maximum performance up to 0.4Tops
- **V831**: Maximum performance up to 0.2Tops
- Supports Conv, Activation, Pooling, BN, LRN, FC/Inner Product
- Supports solidified face recognition, face detection and humanoid detection network

1.4.7. ISP

- Supports 1 individual image signal processor(ISP), with maximum resolution of 2688 x 2688
- Maximum frame rate of 2592x1936@30fps
- Adjustable 3A functions, including automatic exposure(AE), automatic white balance(AWB) and automatic focus (AF)
- Highlight compensation, backlight compensation, gamma correction and color enhancement
- Defect pixel correction, 2D/3D denoising
- Sensor build-in WDR, 2F-line base WDR, local tone mapping
- Graphics mirror and flip
- ISP tuning tools for the PC

1.4.8. VIPP

- Four VIPP YUV22 or YUV420 outputs
- Four VIPPs support 16 ORLs
- Maximum resolution of 2688 x 2688
- Each VIPP supports 1 to 1/256 video scaling
- VIPP0/1 supports YUV422 to YUV420

1.4.9. Security Engine

- Encryption and decryption algorithms implemented by using hardware, including AES,DES,3DES and XTS
- Signature and verification algorithms implemented by using hardware, including RSA512/1024/2048/3072/4096 bits, ECC160/224/256/384/521bits
- HASH tamper proofing algorithms implemented by using hardware, including MD5/SHA/HMAC
- Hardware true random number generator(TRNG) and hardware pseudo random number generator(PRNG)
- Integrated 1Kbits efuse storage space

1.4.10. Video Interfaces

1.4.10.1. Input

- **V833:** One 4-lane MIPI CSI input
  - Compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00.00
  - Maximum video capture resolution for serial interface up to 2592 x 1936@30fps RAW data or 4*1080p@25fps YUV422 data
- **V831:** One 2-lane MIPI CSI input
  - Compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00.00
  - Maximum video capture resolution for serial interface up to 1080p@60fps
- **V833:** One 12-bit parallel CSI input
  - Compatibility with mainstream HD CMOS sensors provided by Sony, Aptina, Omni Vision and Panasonic

- BT.601, BT.656 and BT.1120 video input interfaces
- Maximum video capture resolution for parallel interface to 5M@15fps or 1080p@30fps

1.4.10.2. Output

- **V833:** One MIPI digital serial interface(DSI) output
  - Compliance with MIPI DSI v1.01, MIPI D-PHY v1.00 and MIPI DCS v1.02
  - Up to 1920 x 1080@60fps
- **V833:** One RGB output, up to 1920 x 1080@60fps
- **V831:** One RGB output, up to 320 x 240@60fps
- **V833:** One BT1120/BT656 video output, up to 3840 x 2160@15fps
- **V831:** One BT656 video output, up to 1080p@30fps

1.4.11. Audio Interfaces

- Integrated audio codec, supporting 20-bit audio input and output
- Inter-IC sound(I2S)/time division multiplex(TDM) interface for connecting to an external audio codec

1.4.12. Peripheral Interfaces

- One internal RTC
- Four UART interfaces
- Three SPI interfaces(**for V833**), two SPI interfaces(**for V831**)
- One PWM controller(10-ch)
- One USB2.0 OTG interface
- One one-wire interface
- Two channels general purpose analog-to-digital converter(GPADC, **for V833**), one channel GPADC(**for V831**)
- Three SD3.0/SDIO3.0 interfaces(**for V833**), two SD3.0/SDIO3.0 interfaces(**for V831**), supporting secure digital extended capacity(SDXC)
- 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces(**for V833**), 10/100 Mbps Ethernet port with RMII interface(**for V831**)
- Five TWI interfaces(**for V833**), four TWI interfaces(**for V831**)
- 99 GPIO interfaces(**for V833**), 54 GPIO interfaces(**for V831**)

1.4.13. External Memory Interfaces

- DDR2/DDR3/DDR3L interface(**for V833**)
  - Supports 16-bit DDR3/DDR3L, up to 800MHz
  - Supports 16-bit DDR2, up to 533MHz
  - Memory capacity up to 3GByte

NOTE

V831 is embedded with 64MB DDR2.

- SPI Nor Flash interface
  - 1-, 2-, 4-wire mode
  - 3 bytes or 4 bytes address mode
- SPI Nand Flash interface
- eMMC 5.0 interface
- Booting from SPI NOR, SPI NAND, eMMC, SD, USB, UART, one-key FEL
- Hardware boot select pin or eFuse booting sequence

1.4.14. Physical Specifications

- Power consumption
  - TBD
  - Multi-level power-saving mode
- Operating voltages
  - 0.9V core voltage
  - 3.3V IO voltage
  - 1.8V, 1.5V, 1.35V for DDR2/DDR3/DDR3L interface
- Package
  - Restrictions on the use of certain hazardous substances(RoHS)
  - **V833**: Low profile fine-pitch ball grid array(LFBGA), 273 pins, body size of 12 mm x 12 mm, 0.65 mm ball pitch, 0.35 mm ball size
  - **V831**: QFN, 88 pins, body size of 9 mm x 9 mm, 0.35 mm pin pitch

1.5. Boot Modes

The V833/V831 can boot from the following devices:

- SD/eMMC
- SPI NOR
- SPI NAND
- USB
- UART

During power-on reset, the boot mode depends on the values of BOOT_SEL[1:0] and FEL, the details are shown in Table 1-2.

Table 1- 2. Boot Select Setting and Boot Media

Device	BOOT_SEL[1:0]	FEL	Boot Media	Note
V833	XX	0	UART->USB	X indicates not concerned about the value.

	00	1	SMHC0->SPI NOR	
	01	1	SMHC0->SPI NAND	
	10	1	SMHC0->SMHC2	
	11	1	SMHC0->SPI NOR->SPI NAND->SMHC2	
V831	No pin	No pin	SMHC0->SPI NOR->SPI NAND->SMHC2->UART	

NOTE

SMHC0 usually is external SD / TF Card.

SMHC2 usually is external eMMC.

Contents

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Chapter 2 Hardware

2.1. Package and Pinout

2.1.1. Package

2.1.1.1. V833

The V833 uses the LFBGA package, it has 273 pins, its body size is 12 mm x 12 mm, and its ball pitch is 0.65 mm. Figure 2-1 shows the top view of the 12 mm x 12 mm package, Figure 2-2 shows the bottom view of the 12 mm x 12 mm package, and Figure 2-3 shows the side view of the 12 mm x 12 mm package, Figure 2-4 shows the enlarged view of detail “A” in the side view, Figure 2-5 shows the dimensions of the 12 mm x 12 mm package.

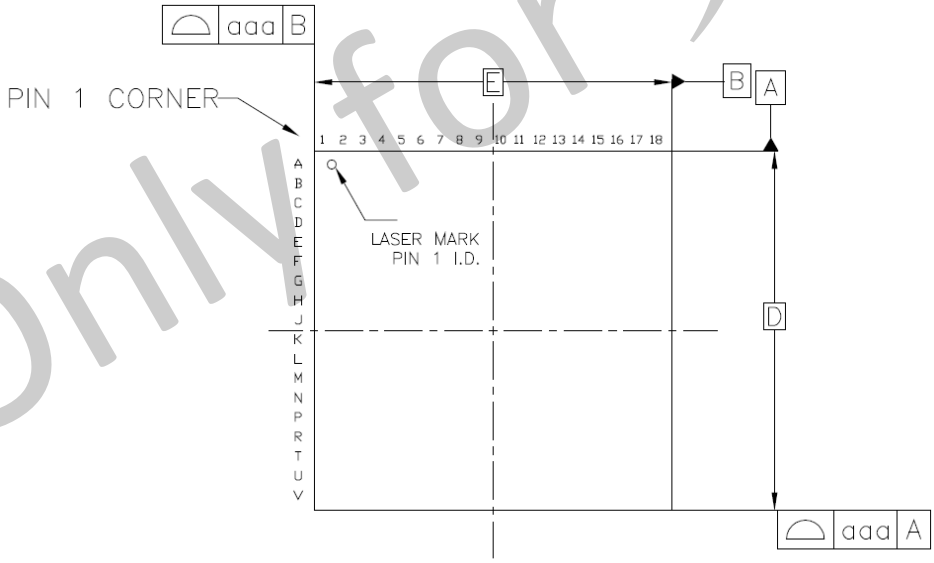

Figure 2- 1. 12 mm x 12 mm Package Top View

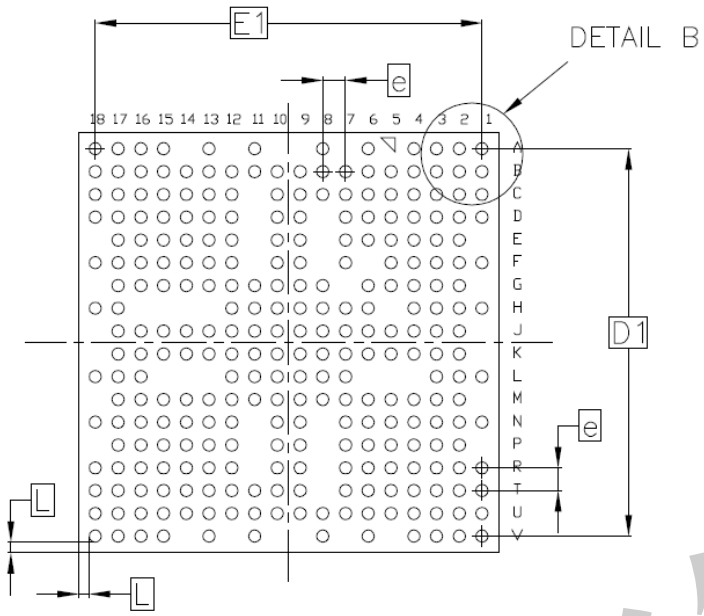

Figure 2- 2. 12 mm x 12 mm Package Bottom View

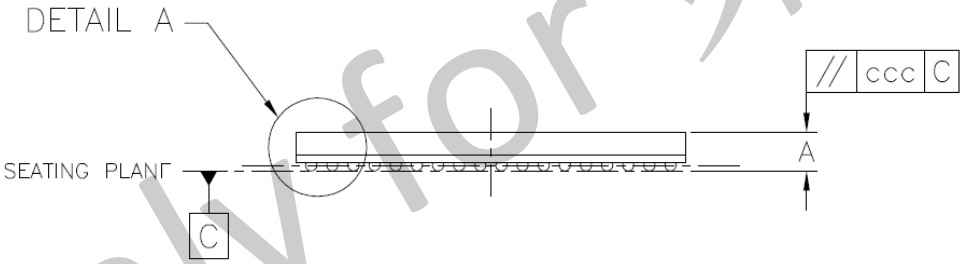

Figure 2- 3. 12 mm x 12 mm Package Side View

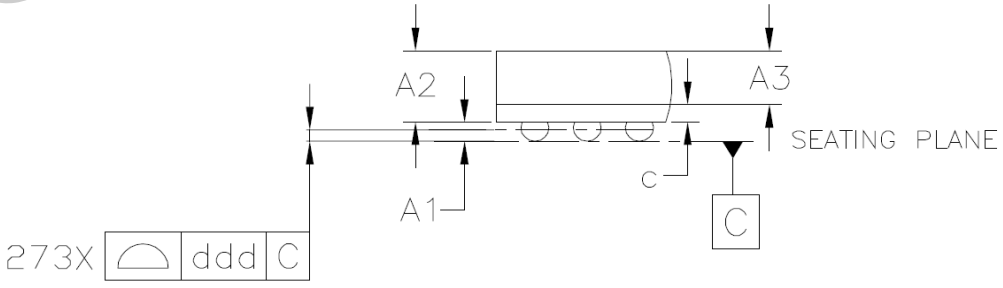

Figure 2- 4. Enlarged View of Detail "A"

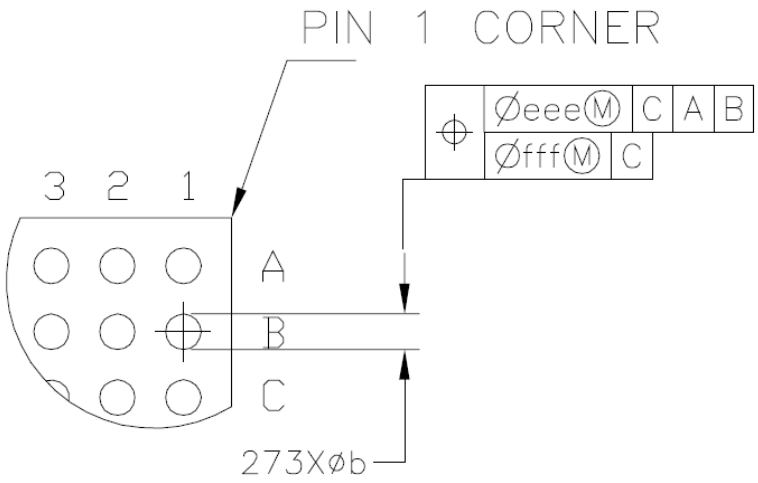

Figure 2- 5. Enlarged View of Detail "B"

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.10	1.18	1.26
A1	0.20	0.25	0.30
A2	0.88	0.93	0.98
A3	0.70 BASIC		
c	0.19	0.23	0.27
D	11.90	12.00	12.10
D1	11.05 BASIC		
E	11.90	12.00	12.10
E1	11.05 BASIC		
e	0.65 BASIC		
b	0.30	0.35	0.40
L	0.300 REF		
aaa	0.15		
ccc	0.15		
ddd	0.12		
eee	0.15		
fff	0.08		

Figure 2- 6. 12 mm x 12 mm Package Dimensions

2.1.1.2. V831

The V831 uses the QFN package, it has 88 pins, its body size is 9 mm x 9 mm, and its pin pitch is 0.35 mm. Figure 2-7 shows the top view of the 9 mm x 9 mm package, Figure 2-8 shows the bottom view of the 9 mm x 9 mm package ,

and Figure 2-9 shows the side view of the 9 mm x 9 mm package, Figure 2-10 shows the enlarged view of detail “A” in the side view, Figure 2-11 shows the dimensions of the 9 mm x 9 mm package.

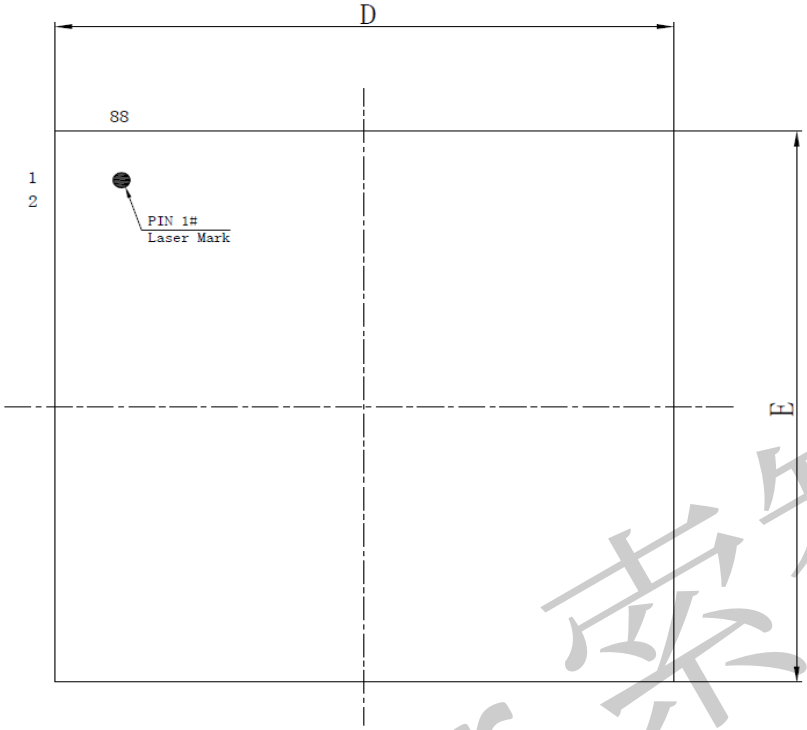

Figure 2- 7. 9 mm x 9 mm Package Top View

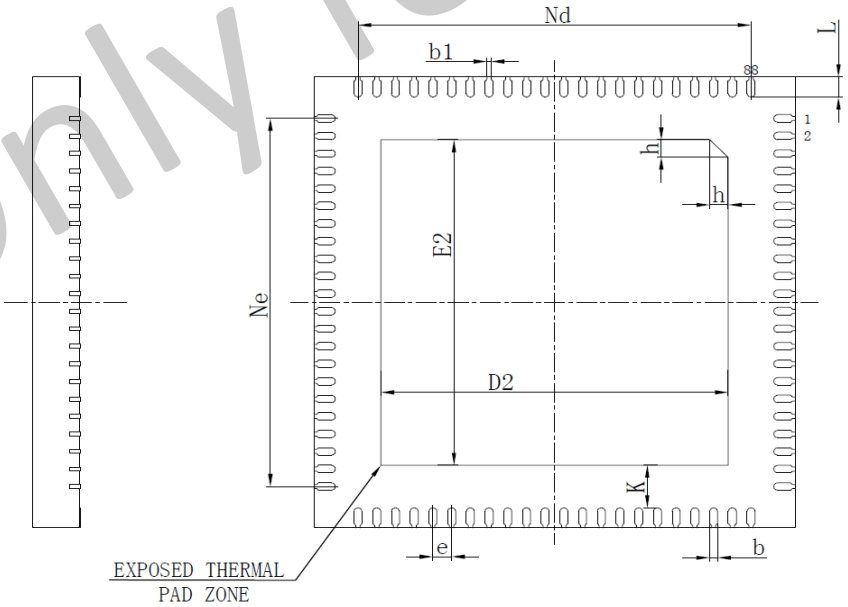

Figure 2- 8. 9 mm x 9 mm Package Bottom View

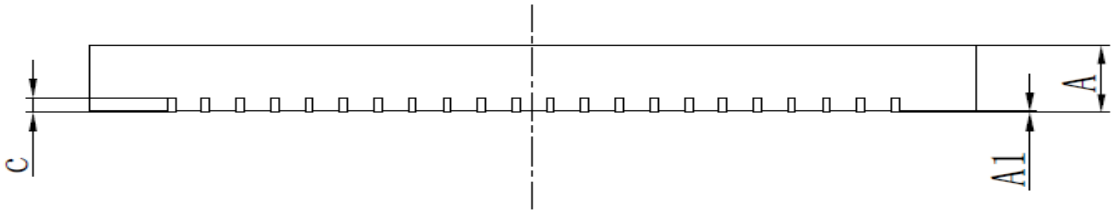

Figure 2- 9. 9 mm x 9 mm Package Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 85	0. 90	0. 95
A1	0	0. 02	0. 05
b	0. 10	0. 15	0. 20
b1	0. 08REF		
c	0. 203REF		
D	8. 90	9. 00	9. 10
D2	6. 40	6. 50	6. 60
e	0. 35BSC		
Ne	7. 35BSC		
Nd	7. 35BSC		
E	8. 90	9. 00	9. 10
E2	6. 40	6. 50	6. 60
L	0. 35	0. 40	0. 45
h	0. 30	0. 35	0. 40
K	0. 85REF		

Figure 2- 10. 9 mm x 9 mm Package Dimensions

2.1.2. Pin Quantity

Table 2- 1. V833 Pin Quantity

Pin Type	Quantity
I/O	200
Power	25
GND	42
DDR Power	6
Total	273

Table 2- 2. V831 Pin Quantity

Pin Type	Quantity
I/O	71
Power	14
GND	1
DDR Power	2
Total	88

2.2. Pin Description

For details about pin description of the V833/V831, see the *V833/V831_PINOUT.xls.*

2.3. Electrical Characteristics

2.3.1. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

2.3.2. Thermal Resistance Parameters

Table 2-3 shows thermal resistance parameters. The following thermal resistance characteristics is based on JEDEC JESD51 standard, because the actual system design could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

NOTE

Test condition: four-layer board(2s2p), natural convection, no air flow.

Table 2- 3. Thermal Resistance Parameters

Device	Package	Parameter	Symbol	Min	Typ	Max	Unit
V833	LFBGA273	Junction-to-Ambient Thermal Resistance	θ_{JA}	-	28.6	-	°C/W
		Junction-to-Board Thermal Resistance	θ_{JB}	-	10.86	-	°C/W
		Junction-to-Case Thermal Resistance	θ_{JC}	-	8.55	-	°C/W
V831	QFN88	Junction-to-Ambient Thermal Resistance	θ_{JA}	-	25.1	-	°C/W
		Junction-to-Board Thermal Resistance	θ_{JB}	-	7.9	-	°C/W
		Junction-to-Case Thermal Resistance	θ_{JC}	-	7.9	-	°C/W

2.3.3. Operating Conditions

All V833 modules are used under the operating conditions contained in Table 2-4.

Table 2- 4. Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	70	°C
Tj	Junction Temperature Range	-20	-	115	°C
AVCC	Analog and ADC Power	1.764	1.8	1.836	V
VCC_IO	Some GPIO and System Control Power	2.97	3.3	3.63	V
VCC_PC	Port C Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC_PD	Port D Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC_PE	Port E Power 1.8V voltage 2.8V voltage 3.3V voltage	1.62 2.52 2.97	1.8 2.8 3.3	1.98 3.08 3.63	V
VCC18_PF	Port F Power	1.62	1.8	1.98	V
VCC_PG	Port G Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC_PI	Port I Power 1.8V voltage 2.8V voltage 3.3V voltage	1.62 2.52 2.97	1.8 2.8 3.3	1.98 3.08 3.63	V
VCC_PL	Port L Power 1.8V voltage 3.3V voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC_PLL	System PLL Power	1.62	1.8	1.98	V
VCC_RTC	RTC Power	1.62	1.8	1.98	V
VCC33_USB	USB Analog Power	3.069	3.3	3.63	V
VDD09_USB	USB Digital Power	0.837	0.9	0.99	V
VCC_EFUSE	EFUSE Program Mode Power	1.8	1.89	1.98	V
VCC18_DSI_CSI	MIPI DSI and MIPI CSI Power	1.62	1.8	1.98	V
VCC_DRAM	DDR2 IO Domain Power	1.7	1.8	1.9	V
	DDR3 IO Domain Power	1.425	1.5	1.575	V
	DDR3L IO Domain Power	1.283	1.35	1.45	V
VDD18_DRAM	DRAM 1.8V Internal PAD Power	1.7	1.8	1.98	V
VDD_SYS	CPU and System Power	0.81	-	1.08	V

2.3.4. Power-On and Power-Off Sequences

The sequence between V833 and V831 is different. Figure 2-11 shows an example of the power on sequence for V833 device. Figure 2-12 shows an example of the power on sequence for V831 device.

The description of the power-on sequence for V833 is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- Before the RESET pin holds on low, the power requirements of the V833 device show at the following table. After all of the preceding powers have stabilized, the RESET can be released. After RESET, 24M clock starts oscillating and be stable.

Power	Voltage	Sequencing Order
VCC_RTC	1.8V	1
VCC_DRAM	1.2V, 1.35V, 1.5V	2
VDD_SYS, VDD09_USB	0.9V	2
VDD18_DRAM, AVCC, VCC_PLL	1.8V	3
VCC18_DSI_CSI, VCC_EFUSE, VCC18_PF, VCC_MCSI	1.8V	3
VCC_PL	3.3V	3
VCC_IO, VCC_PC, VCC_PD, VCC_PG, VCC33_USB	3.3V	3
Reset	1.8V	4
24M CLK	-	5

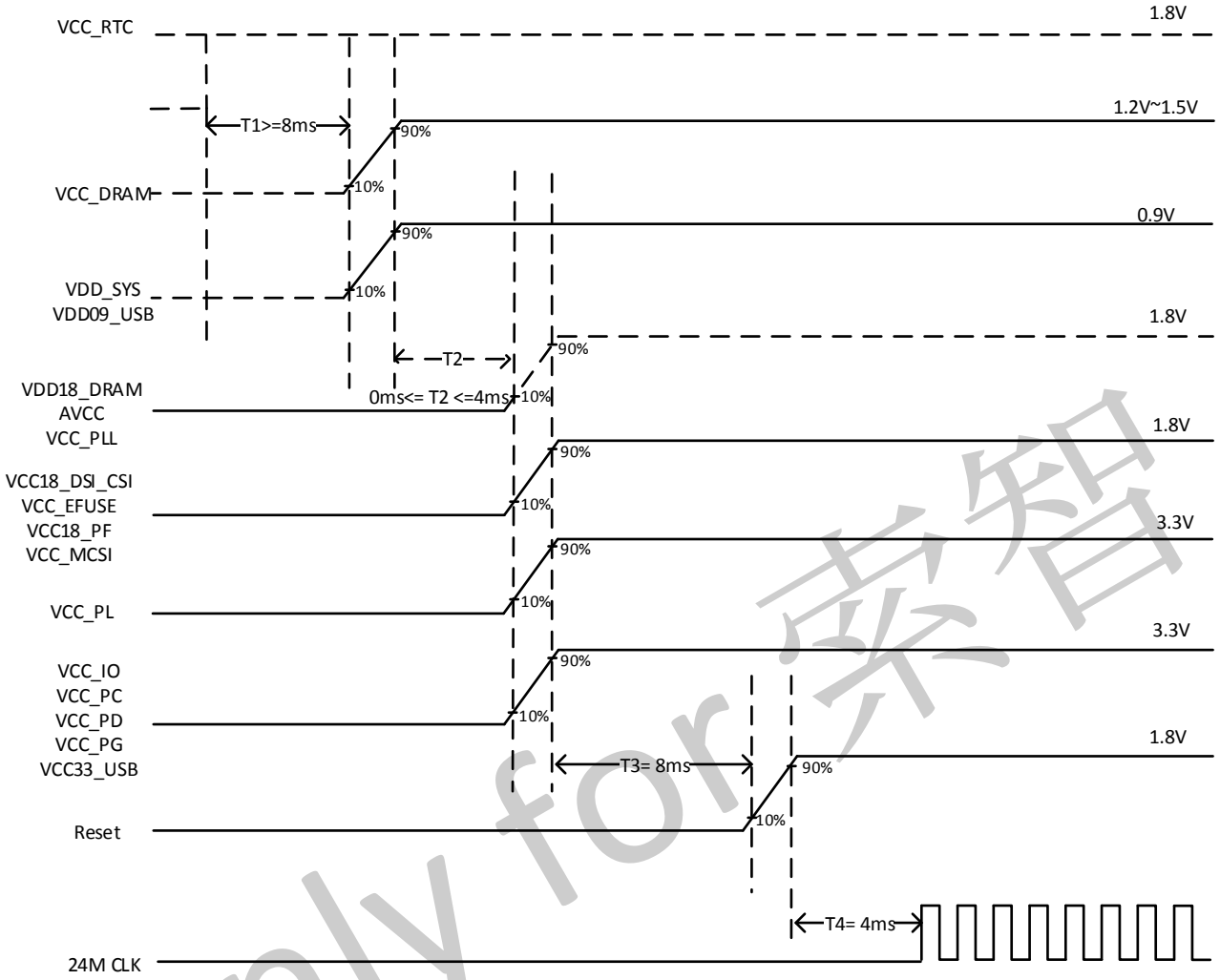

Figure 2- 11. V833 Power-on Sequence

The description of the power-on sequence for V831 is as follows.

- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- T1 >= 0 ms: VCC18_IO can not ramp up later than VCC_PD.
- T2 >= 8 ms: VCC_RTC starts to ramp up at least 8 ms earlier than VDD_SYS.
- T3 > 0 ms: After all of the preceding powers have stabilized, the RESET can be released.
- T4 = 0 ms: 24 MHz clock starts oscillating and be stable after RESET.

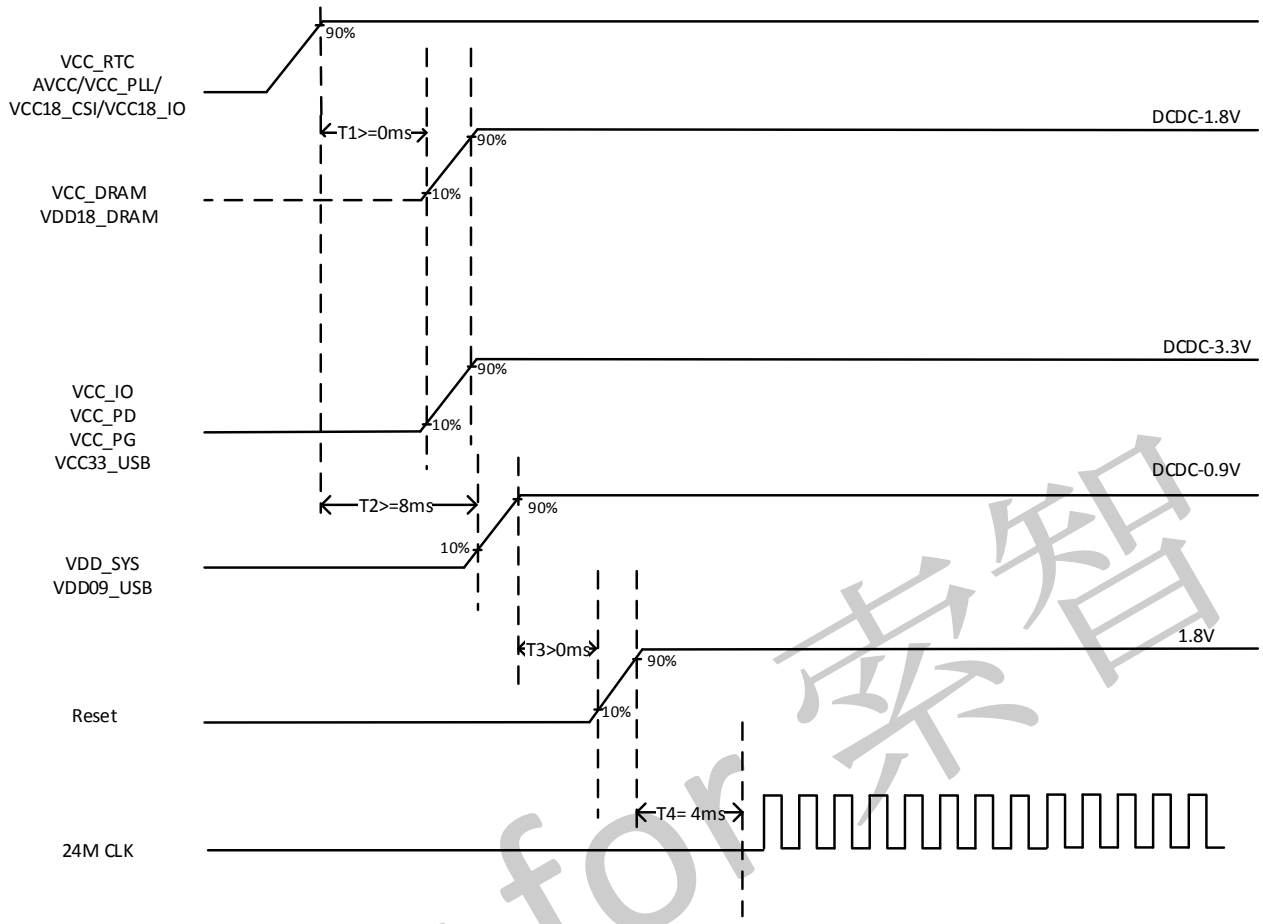

Figure 2- 12. V831 Power-on Sequence

During power-off, all powers start to ramp down at the same time, and the ramp rate of each power rail is generated by the load on the power.

2.3.5. DC Electrical Parameters

Table 2-5 summarizes the DC electrical characteristics of the V833/V831.

Table 2- 5. DC Electrical Parameters
(VCC_IO/VCC_PC/VCC_PD/VCC_PE/VCC_PG/VCC_PI/VCC_PL)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC_IO	-	VCC_IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC_IO	V
R_{PU}	Input Pull-up Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
R_{PD}	Input Pull-down Resistance	80 3.76	100 4.7	120 5.64	kΩ

		12	15	18	
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC_IO - 0.2	-	VCC_IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

NOTE

For GPIOL0~GPIOL1 ports, the R_{PU} and R_{PD} are 4.7kΩ ±20%.
For GPIOC0~GPIOC3, and GPIOF3 ports, the R_{PU} and R_{PD} are 15kΩ ±20%.
For other GPIO ports, the R_{PU} and R_{PD} are 100kΩ ±20%.

2.3.6. SDRAM I/O DC Electrical Parameters

The DDR I/O pads support DDR3/DDR3L operational modes. The SDRAM Controller(DRAMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DRAMC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3F DDR3 JEDEC standard release July,2012
- DDR3L SDRAM compliant to JESD79-3-1A DDR3L JEDEC standard release January,2013

Table 2- 6. DC Input Logic Level

Characteristics	Symbol	Min	Max	Unit
DC input logic high	$V_{IH(DC)}$	V_{ref} +20	-	mV
DC input logic low	$V_{IL(DC)}$	-	V_{ref} –20	mV

Table 2- 7. DDR3/DDR3L mode, DC Input Conditions

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Reference Voltage	V_{ref}	V_{DDQ}	30.1%	31.1%	32.1%	Please refer to Note 1 and 2
On-die termination(ODT) programmable resistances	R_{TT}	ohm	-	open, 120, 60	-	Please refer to Note 3

NOTE

- **If the external V_{ref} to the receivers is enabled, V_{ref} is expected to be set to a nominal value of (VDDQ/2)*RxAtten(RxAttenuation for DDR3/DDR3L is 0.623) through a voltage divider in order to track VDDQ level. It can be adjusted in the system to margin the input DQ signals, although this margin does not necessarily represent the eye height since a change in V_{ref} also changes the input receiver common mode, altering receiver performance.**
- **Externally supplied V_{ref} is not recommended. Internal V_{ref} generation through local V_{ref} generation at each**

receiver is preferred.

- **For DDR3, ODT is a Thevenin resistance to V_{DDQ}/2.**

2.3.7. SDIO Electrical Parameters

The SDIO electrical parameters are related to different supply voltage.

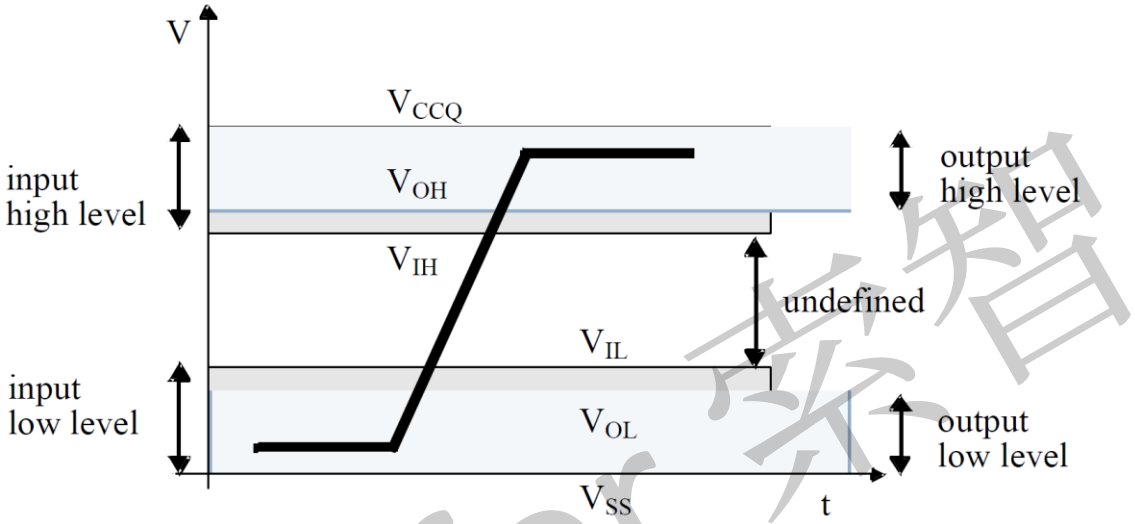

Figure 2- 13. SDIO Voltage Waveform

Table 2-8 shows 3.3V SDIO electrical parameters.

Table 2- 8. 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75* V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS}- 0.3	-	0.25* V_{CCQ}	V

Table 2-9 shows 1.8V SDIO electrical parameters.

Table 2- 9. 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output HIGH voltage	V_{CCQ} -0.45	-	-	V
V_{OL}	Output LOW voltage	-	-	0.45	V
V_{IH}	Input HIGH voltage	0.625* V_{CCQ} (1)	-	V_{CCQ} + 0.3	V

V_{IL}	Input LOW voltage	V_{SS} - 0.3	-	0.35* V_{CCQ} (2)	V
Note: 0.7 * VDD for MMC4.3 or lower. 0.3 * VDD for MMC4.3 or lower.					

2.3.8. Audio Codec Electrical Parameters

Table 2-14 shows audio codec electrical parameters.

Test Conditions:

VDD_SYS = 0.9V, AVCC=1.8V, TA=25°C, 1kHz sinusoid signal, DAC fs = 48kHz, ADC fs = 16kHz, Input gain = 0dB, 16-bit audio data unless otherwise stated.

Figure 2- 14. Audio Codec Electrical Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DAC to LINEOUTP/N(R=10kΩ)**					
	Full-scale Level	0dBFS 1kHz	-	1.1	-	Vrms
	SNR(A-weighted)	0dBFS 1kHz	-	98	-	dB
	THD+N	0dBFS 1kHz	-	-85	-	dB
	Noise	0data	-	12.0	-	uV
ADC Path	**MIC1 via ADC mixer**					
	Output Level	MICP=3.3Vpp/2,MICN=3.3Vpp/2,1kHz,0dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=3.3Vpp/2,MICN=3.3Vpp/2,1kHz,0dB Gain	-	94	-	dB
	THD+N	MICP=3.3Vpp/2,MICN=3.3Vpp/2,1kHz,0dB Gain	-	-90	-	dB
	Output Level	MICP=1.695Vpp/2,MICN=1.695Vpp/2,1kHz,6dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=1.695Vpp/2,MICN=1.695Vpp/2,1kHz,6dB Gain	-	94	-	dB
	THD+N	MICP=1.695Vpp/2,MICN=1.695Vpp/2,1kHz,6dB Gain	-	-90	-	dB
	Output Level	MICP=803.2mVpp/2,MICN=803.2mVpp/2,1kHz,12dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=803.2mVpp/2,MICN=803.2mVpp/2,1kHz,12dB Gain	-	92	-	dB
	THD+N	MICP=803.2mVpp/2,MICN=803.2mVpp/2,1kHz,12dB Gain	-	-88	-	dB
	Output Level	MICP=404.0mVpp/2,MICN=404.0mVpp/2,1kHz,18dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=404.0mVpp/2,MICN=404.0mVpp/2,1kHz,18dB Gain	-	90	-	dB
	THD+N	MICP=404.0mVpp/2,MICN=404.0mVpp/2,1kHz,18dB Gain	-	-85	-	dB
	Output Level	MICP=204.6mVpp/2,MICN=204.6mVpp/2,1kHz,24dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=204.6mVpp/2,MICN=204.6mVpp/2,1kHz,24dB Gain	-	85	-	dB
	THD+N	MICP=204.6mVpp/2,MICN=204.6mVpp/2,1kHz,24dB Gain	-	-81	-	dB
	Output Level	MICP=104.8mVpp/2,MICN=104.8mVpp/2,1kHz,30dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=104.8mVpp/2,MICN=104.8mVpp/2,1kHz,30dB Gain	-	80	-	dB
	THD+N	MICP=104.8mVpp/2,MICN=104.8mVpp/2,1kHz,30dB Gain	-	-75	-	dB
	Output Level	MICP=55.1mVpp/2,MICN=55.1mVpp/2,1kHz,36dB Gain	-	885	-	mFFS
	SNR(A-weighted)	MICP=55.1mVpp/2,MICN=55.1mVpp/2,1kHz,36dB Gain	-	75	-	dB
	THD+N	MICP=55.1mVpp/2,MICN=55.1mVpp/2,1kHz,36dB Gain	-	-70	-	dB

2.4. PCB Design Recommendations

For details about PCB design recommendations, see the *V833/V831 Hardware Design User Guide*.

2.5. Interface Timings

2.5.1. SDRAM Interface Timing

2.5.1.1. DDR3/DDR3L Parameters

Figure 2-15 shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 2-10.

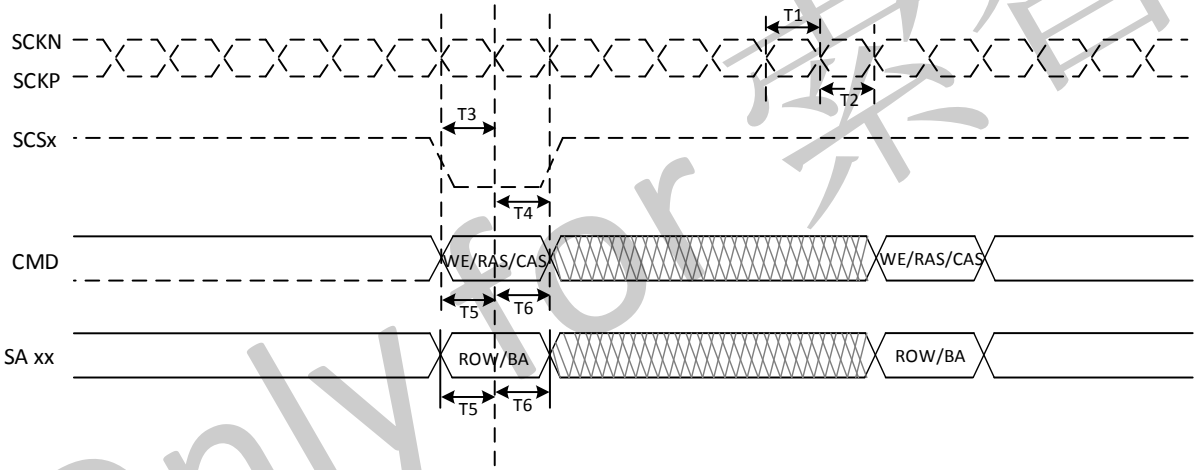

Figure 2- 15. DDR3/DDR3L Command and Address Timing

Table 2- 10. DDR3/DDR3L Timing Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T1	Clock high-level width	t_{CH}	0.47	-	0.53	tck
T2	Clock low-level width	t_{CL}	0.47	-	0.53	tck
T3	CS setup time	t_{IS}	170	295	-	ps
T4	CS hold time	t_{IH}	120	245	-	ps
T5	Command and Address setup time to Clock edge	t_{IS}	170	295	-	ps
T6	Command and Address hold time to Clock edge	t_{IH}	120	245	-	ps

T1 and T2 are in reference to V_{ref} level.

T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 2-16 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 2-11.

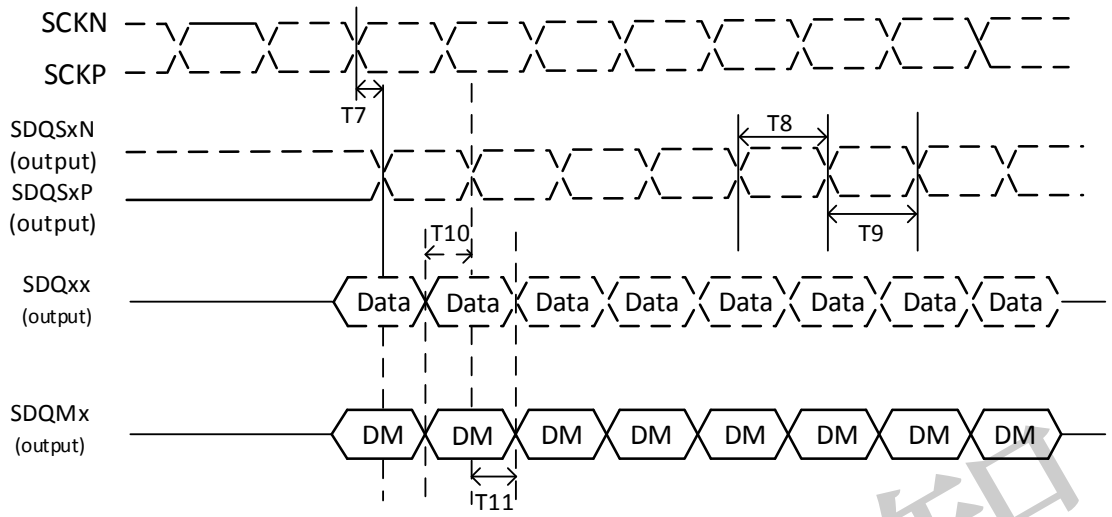

Figure 2- 16. DDR3/DDR3L Write Cycle

Table 2- 11. DDR3/DDR3L Write Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQS high level width	t_{DQSH}	0.45	-	0.55	t_{CK}
T9	SDQS low level width	t_{DQSL}	0.45	-	0.55	t_{CK}
T10	Data setup time to SDQS	t_{DS}	10	145	-	ps
T11	Data hold time to SDQS	t_{DH}	45	180	-	ps

To receive the reported setup and hold values, writing calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.

T7,T8, and T9 are in reference to V_{ref} level.

T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 2-17 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 2-12.

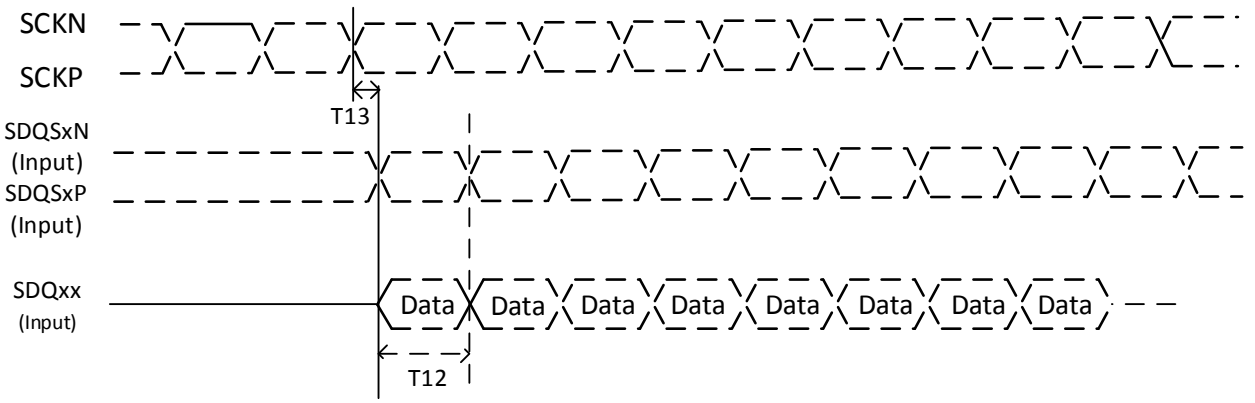

Figure 2- 17. DDR3/DDR3L Read Cycle

Table 2- 12. DDR3/DDR3L Read Cycle Parameters

ID	Parameter	Symbol	Clock = 800 MHz		Unit
			Min	Max	
T12	Read Data valid width	t_{Data}	200	-	ps
T13	SDQS rising edge to SCK rising edge	t_{DQSCK}	-225	225	ps

T12 and T13 are in reference to V_{ref} level.

2.5.2. SMHC Interface Timing

2.5.2.1. SMHC0/1 Interface Timing

(1) SDR Mode(<100MHz)

The contents of this section can be applied to DS, HS, SDR12, SDR25, SDR50, SDR104(<100MHz) speed mode.

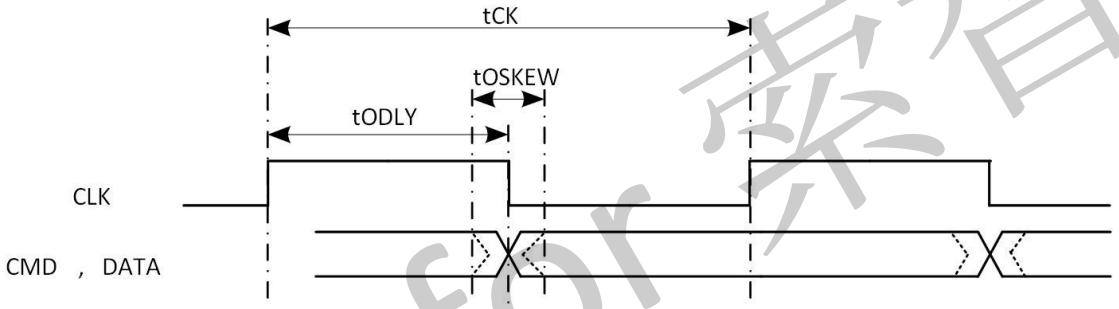

Figure 2- 18. SMHC0/1 SDR Mode Output Timing Diagram

Table 2- 13. SMHC0/1 SDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.625	ns
Note: Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. And the driver strength level of GPIO is 2 for test.					

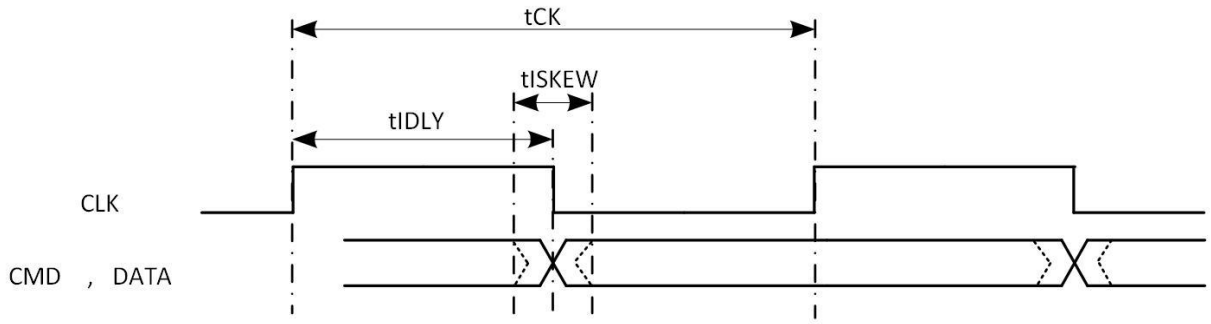

Figure 2- 19. SMHC0/1 SDR Mode Input Timing Diagram

Table 2- 14. SMHC0/1 SDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
Note: The driver strength level of GPIO is 2 for test.					

(2) DDR50 Mode

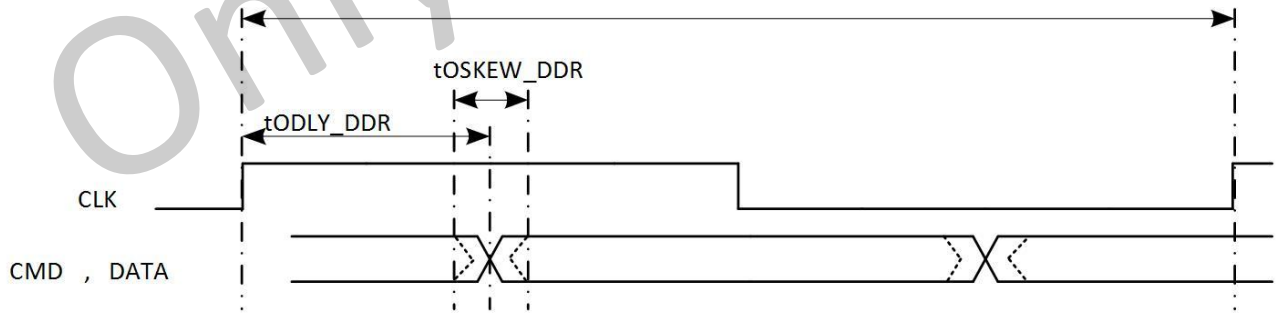

Figure 2- 20. SMHC0/1 DDR50 Mode Output Timing Diagram

Table 2- 15. SMHC0/1 DDR50 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY	-	0.25	0.25	UI

Data output delay skew time	tOSKEW	-	-	0.884	ns
Note: Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. And the driver strength level of GPIO is 2 for test.					

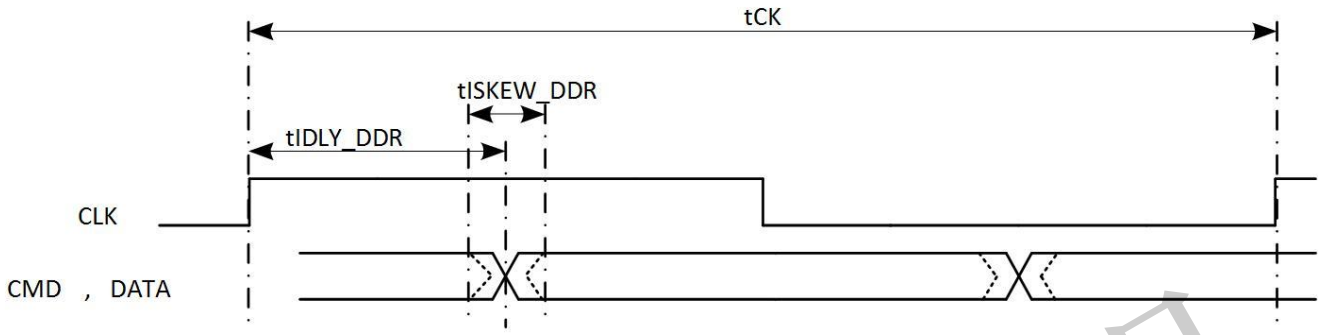

Figure 2- 21. SMHC0/1 DDR50 Mode Input Timing Diagram

Table 2- 16. SMHC0/1 DDR50 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	8.3	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns
Note: The driver strength level of GPIO is 2 for test.					

(3) SDR104 Mode(>100MHz)

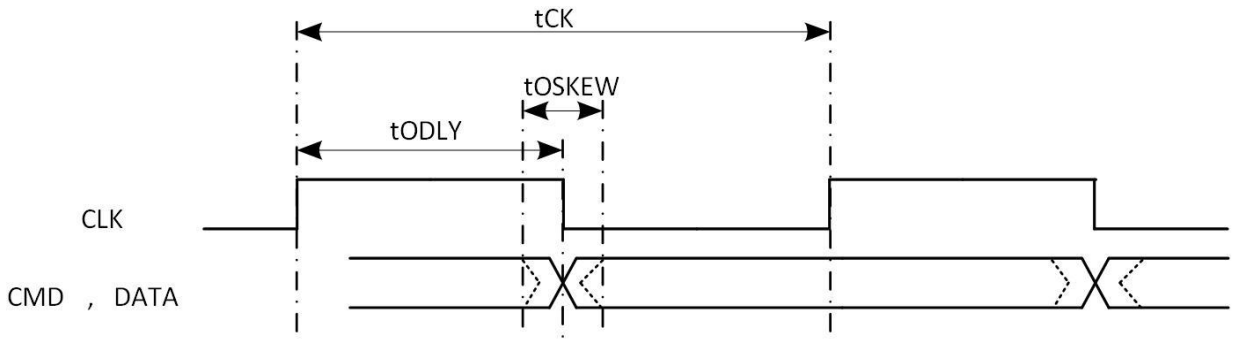

Figure 2- 22. SMHC0/1 SDR104 Mode Output Timing Diagram

Table 2- 17. SMHC0/1 SDR104 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
Note: Unit Interval(UI) is one bit nominal time. For example, UI=20ns at 50MHz. And the driver strength level of GPIO is 2 for test.					

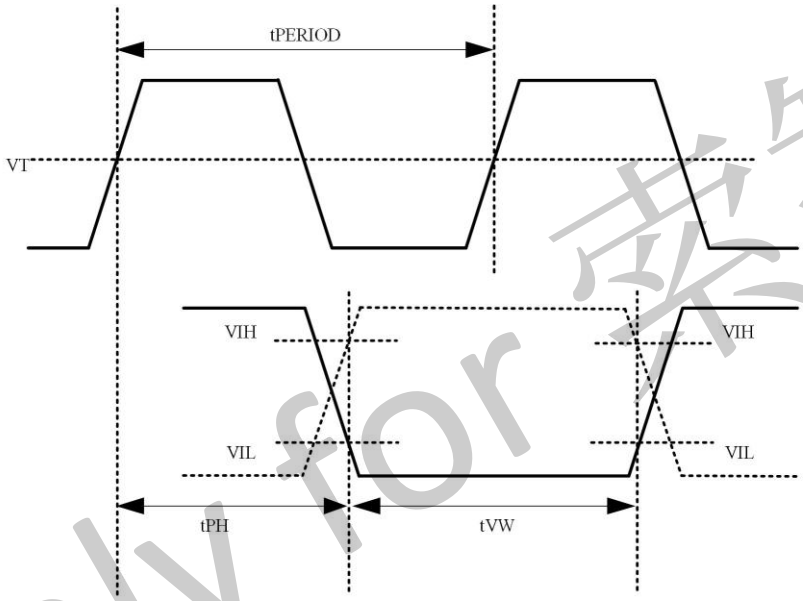

Figure 2- 23. SMHC0/1 SDR-104 Mode Input Timing Diagram

Table 2- 18. SMHC0/1 SDR-104 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
NOTE(1): Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE(2): The driver strength level of GPIO is 3 for test.** **NOTE(3): Temperature variation: -20°C.** **NOTE(4): Temperature variation: 90°C.**						

2.5.2.2. SMHC2 Interface Timing

(1) HS-SDR/HS-DDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

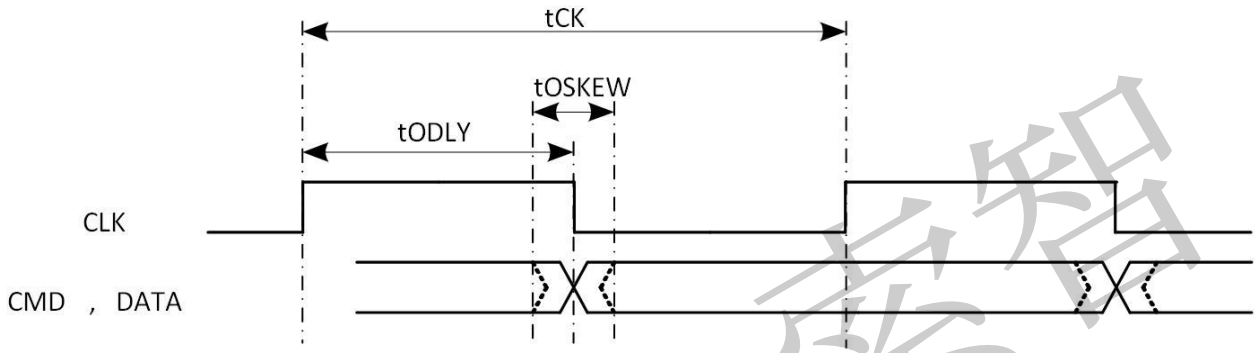

Figure 2- 24. SMHC2 HS-SDR Mode Output Timing Diagram

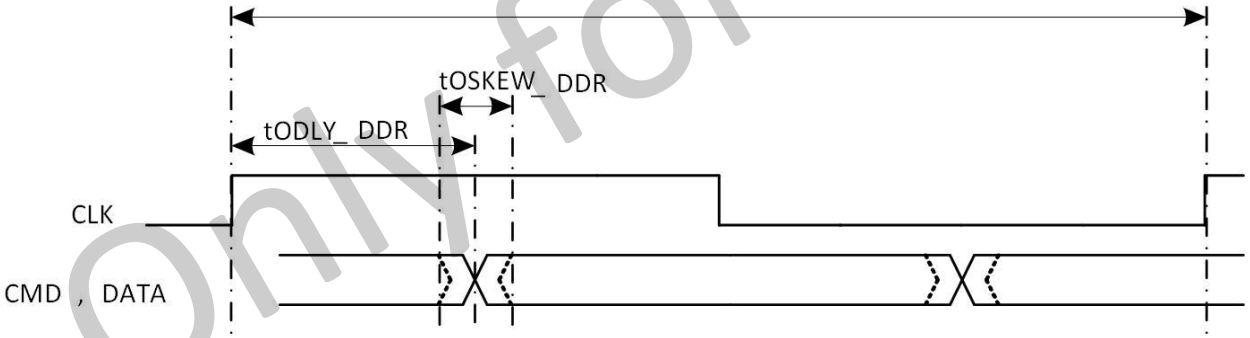

Figure 2- 25. SMHC2 HS-DDR Mode Output Timing Diagram

Table 2- 19. SMHC2 HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
Note: Unit Interval(UI)is one bit nominal time. For example, UI=20ns at 50MHz. And the driver strength level of GPIO is 2 for test.						

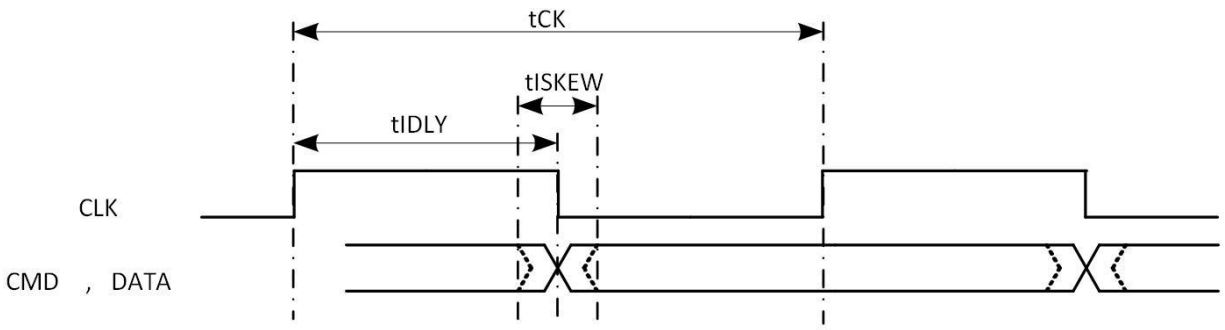

Figure 2- 26. SMHC2 HS-SDR Mode Input Timing Diagram

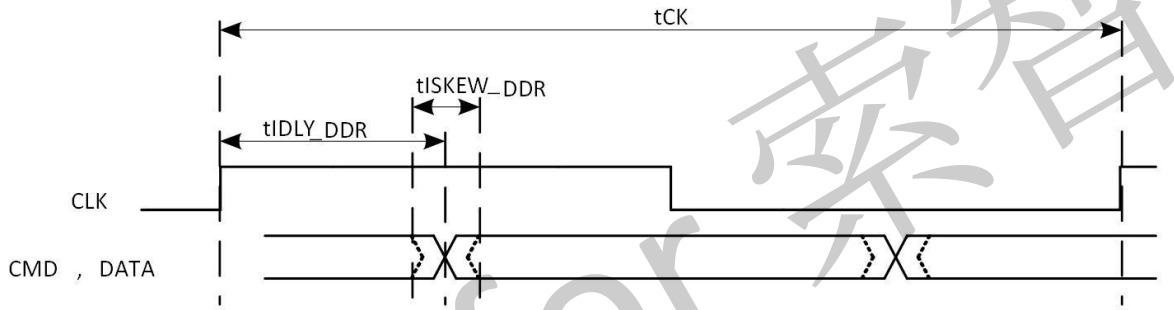

Figure 2- 27. SMHC2 HS-DDR Mode Input Timing Diagram

Table 2- 20. SMHC2 HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes PCB delay time of clock, PCB delay time of data and data output delay of device	tIDLY	-	-	20	ns	
Data input delay in DDR mode. It includes PCB delay time of clock, PCB delay time of data and data output delay of device	tIDLY_DDR	-	-	8.3	ns	
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns	
Note: The driver strength level of GPIO is 2 for test.						

(2) HS200 Mode

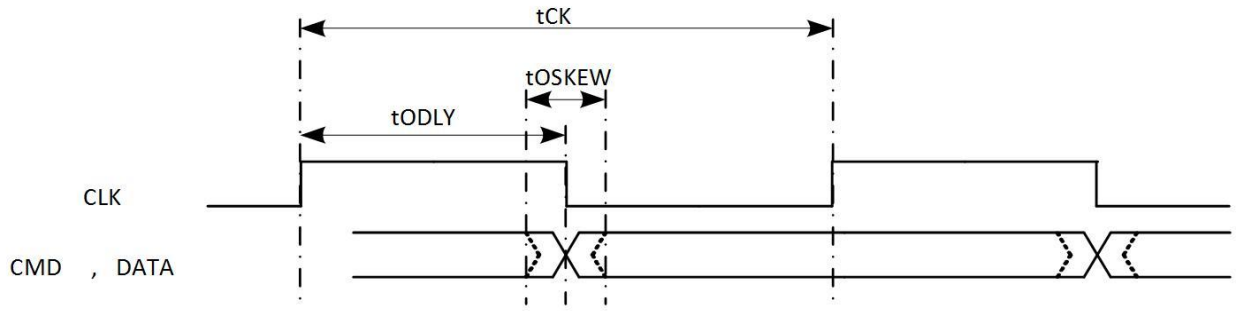

Figure 2- 28. SMHC2 HS200 Mode Output Timing Diagram

Table 2- 21. SMHC2 HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
Note: Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. And the driver strength level of GPIO is 3 for test.						

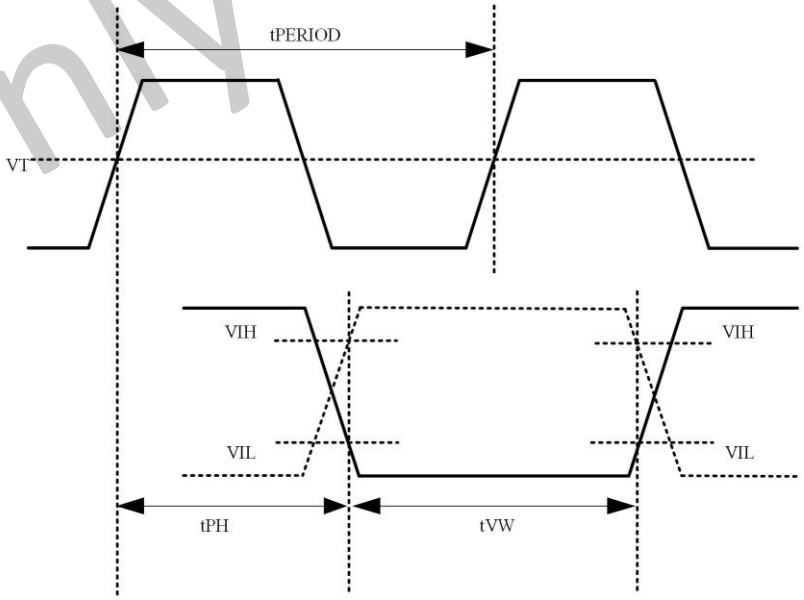

Figure 2- 29. SMHC2 HS200 Mode Input Timing Diagram

Table 2- 22. SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark

CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, DATA valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.** **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**						

(3) HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

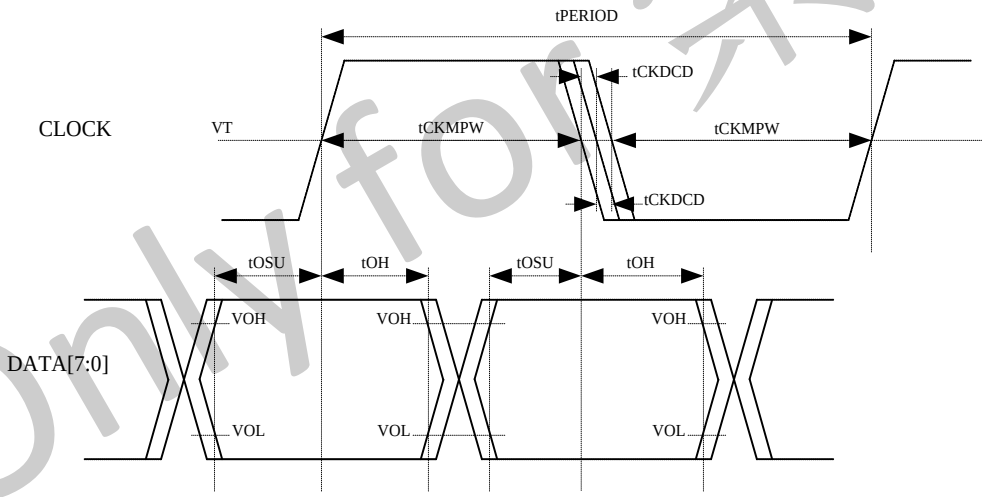

Figure 2- 30. SMHC2 HS400 Mode Data Output Timing Diagram

Table 2- 23. SMHC2 HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	

Note: Unit Interval(UI) is one bit nominal time. For example, UI=10ns at 100MHz. And the driver strength level of GPIO is 3 for test.

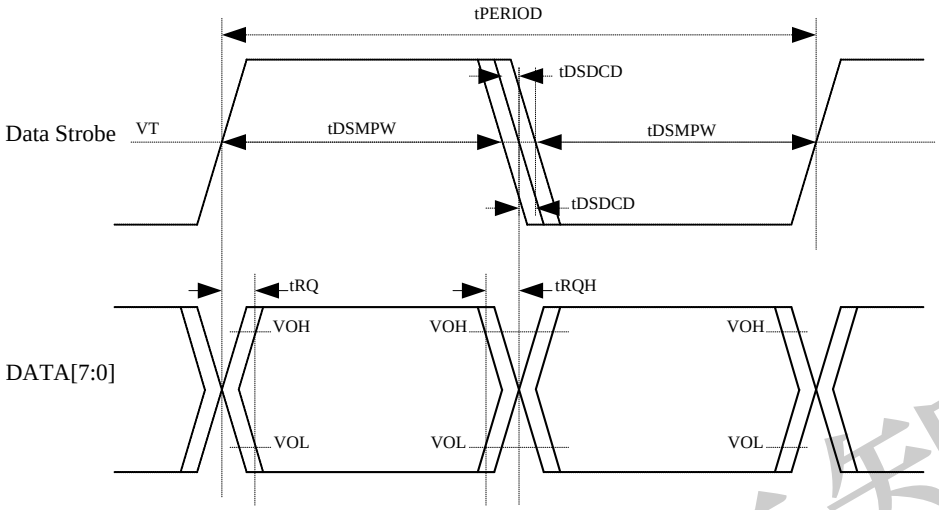

Figure 2- 31. SMHC2 HS400 Mode Data Input Timing Diagram

Table 2- 24. SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
Note: Unit Interval(UI)is one bit nominal time. For example, UI=10ns at 100MHz. And the driver strength level of GPIO is 3 for test.						

2.5.3. LCD Interface Timing

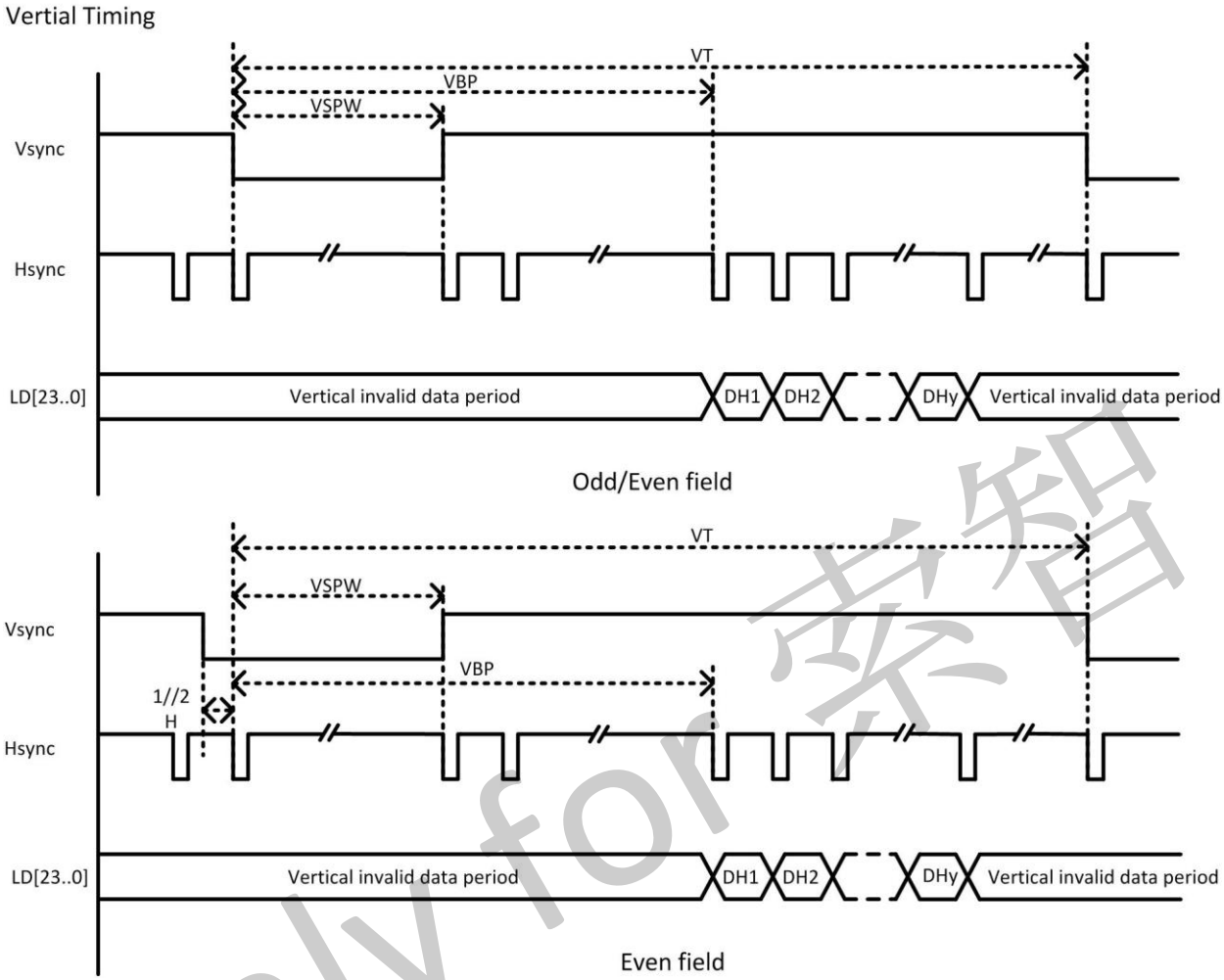

Figure 2- 32. HV_IF Interface Vertical Timing

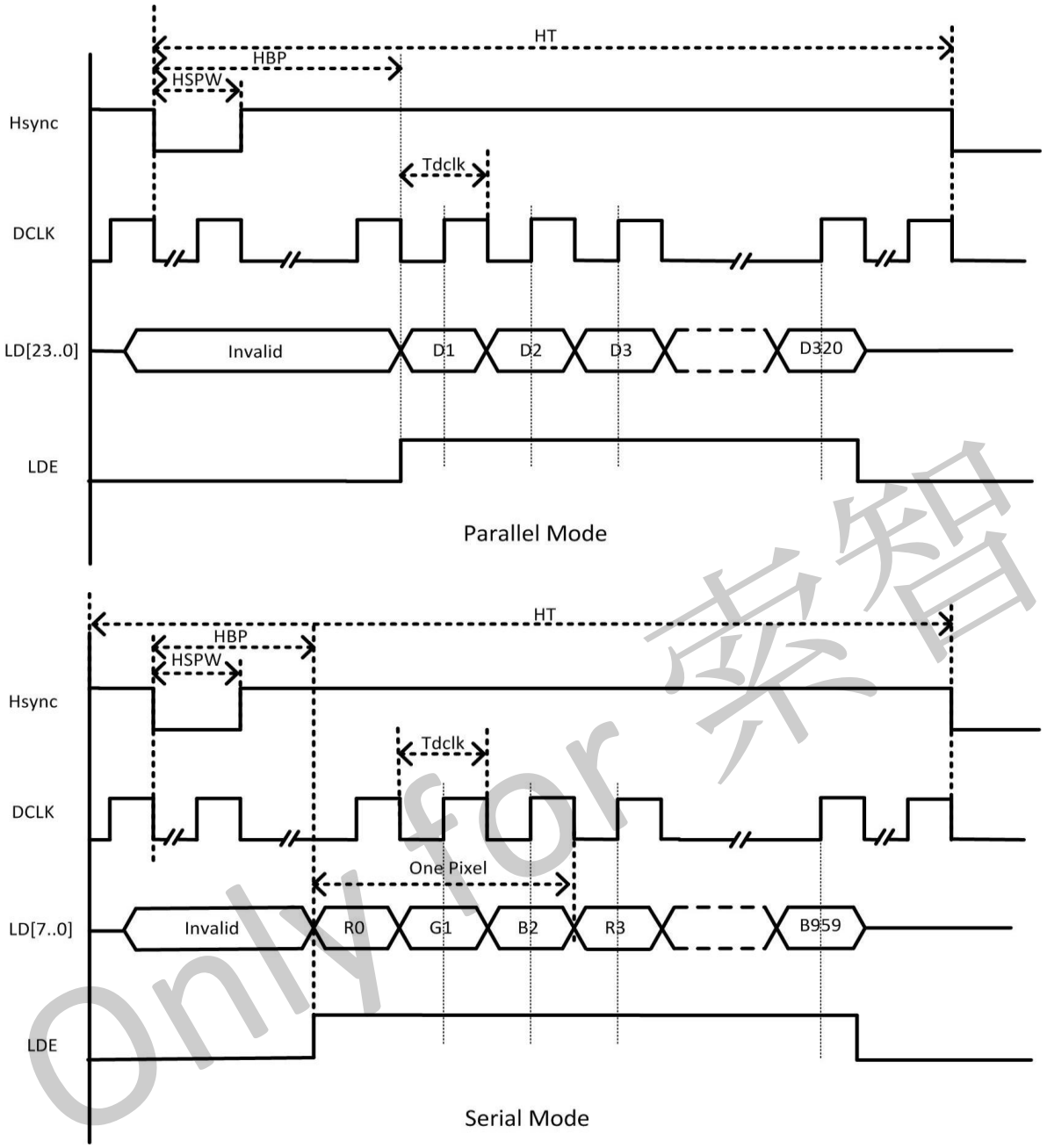

Figure 2- 33. HV Interface Horizontal Timing

Table 2- 25. HV Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK
VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT
Vsync: Vertical sync, indicates one new frame.					

Hsync: Horizontal sync, indicates one new scan line. **DCLK: Dot clock, pixel data are sync by this clock.** **LDE: LCD data enable.** **LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.**

2.5.4. CSI Interface Timing

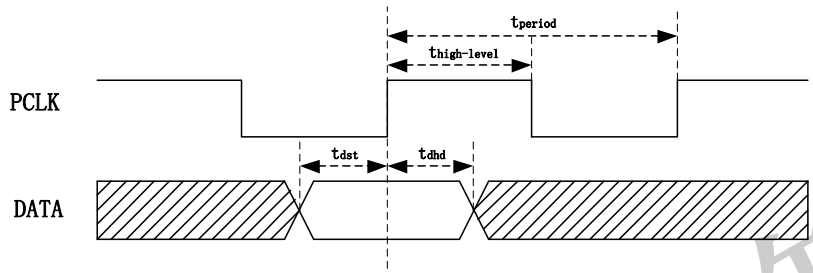

Figure 2- 34. CSI Interface Timing

Table 2- 26. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.7	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

2.5.5. EMAC Interface Timing

2.5.5.1. RGMII

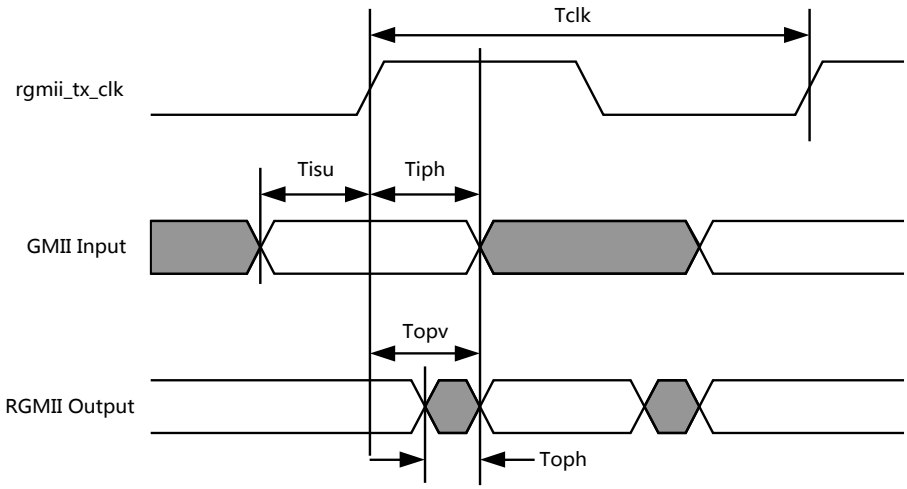

Figure 2- 35. RGMII Transmit Timing

Table 2- 27. RGMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_tx_clk clock period	Tclk	8	-	DC	ns
RGMII/TBI input set up prior to rgmii_tx_clk	Tisu	2.8	-	-	ns
RGMII/TBI input data hold after rgmii_tx_clk	Tiph	0.1	-	-	ns
RGMII output data valid after rgmii_tx_clk	Topv	-	-	0.85	ns
RGMII output data hold after rgmii_tx_clk	Toph	0	-	-	ns

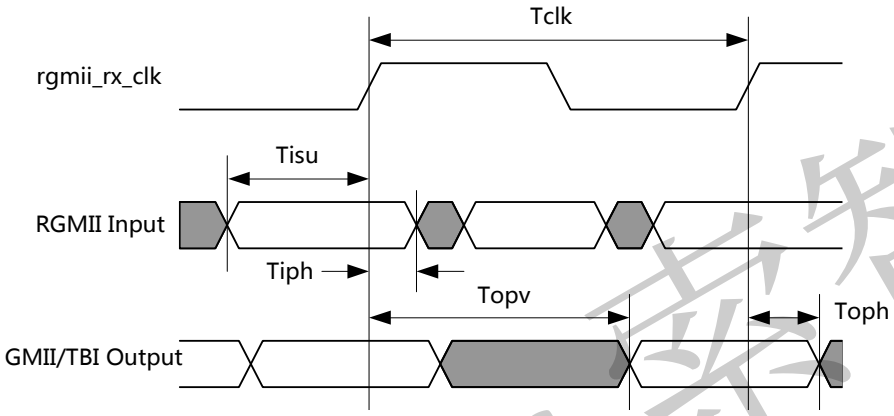

Figure 2- 36. RGMII Receive Timing

Table 2- 28. RGMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
rgmii_rx_clk clock period	Tclk	8	-	DC	ns
RGMII input set up prior to rgmii_rx_clk	Tisu	2.6	-	-	ns
RGMII input data hold after rgmii_rx_clk	Tiph	0.8	-	-	ns
GMII/TBI input data valid after rgmii_rx_clk	Topv	-	-	5.2	ns
GMII output data hold after rgmii_rx_clk TBI output data hold after rgmii_rx_clk	Toph	0.1 0.5	-	-	ns

2.5.5.2. RMII

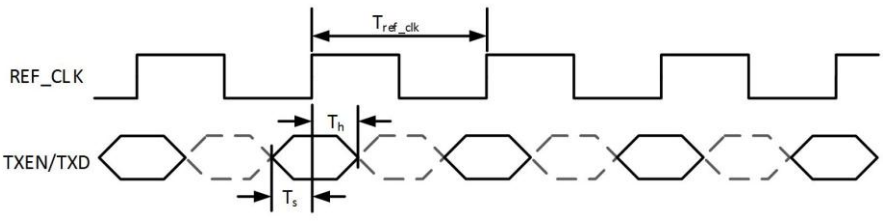

Figure 2- 37. RMII Transmit Timing

Table 2- 29. RMII Transmit Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock Period	T_{ref_clk}	-	20	-	ns
TXD/TXEN to REF_CLK setup time	T_s	4	-	-	ns
TXD/TXEN to REF_CLK hold time	T_h	2	-	-	ns

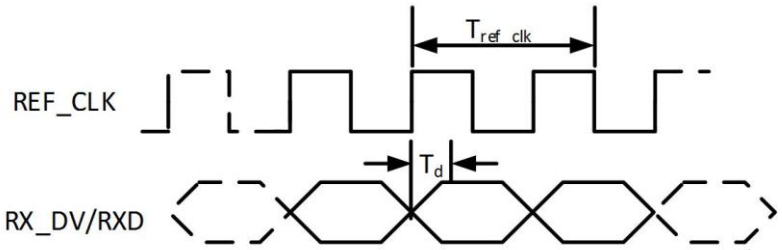

Figure 2- 38. RMII Receive Timing

Table 2- 30. RMII Receive Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock Period	T_{ref_clk}	-	20	-	ns
REF_CLK rising edge to RX_DV/RXD	T_d	-	10	12	ns

2.5.6. I2S/PCM Interface Timing

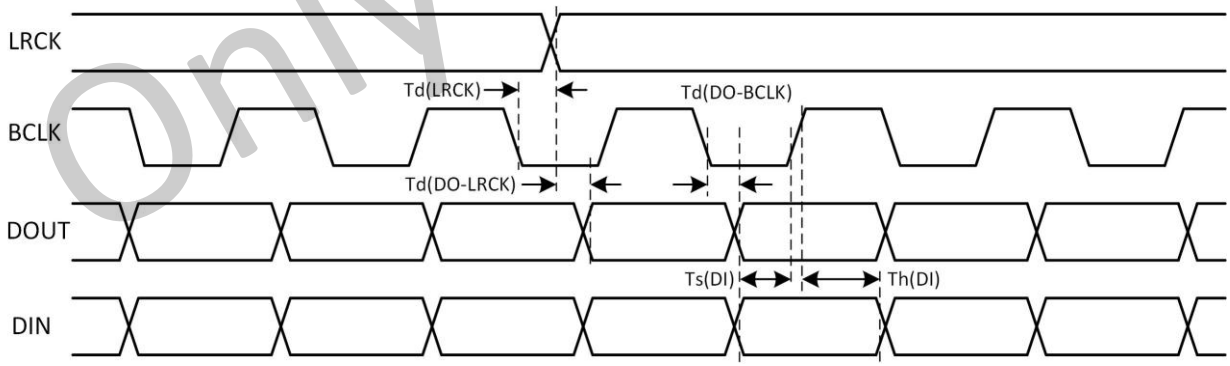

Figure 2- 39. I2S/PCM in Master Mode Timing

Table 2- 31. I2S/PCM in Master Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)	-	-	10	ns
DIN Setup	T_s(DI)	4	-	-	ns
DIN Hold	T_h(DI)	4	-	-	ns

BCLK Rise Time	T_r	-	-	8	ns
BCLK Fall Time	T_f	-	-	8	ns

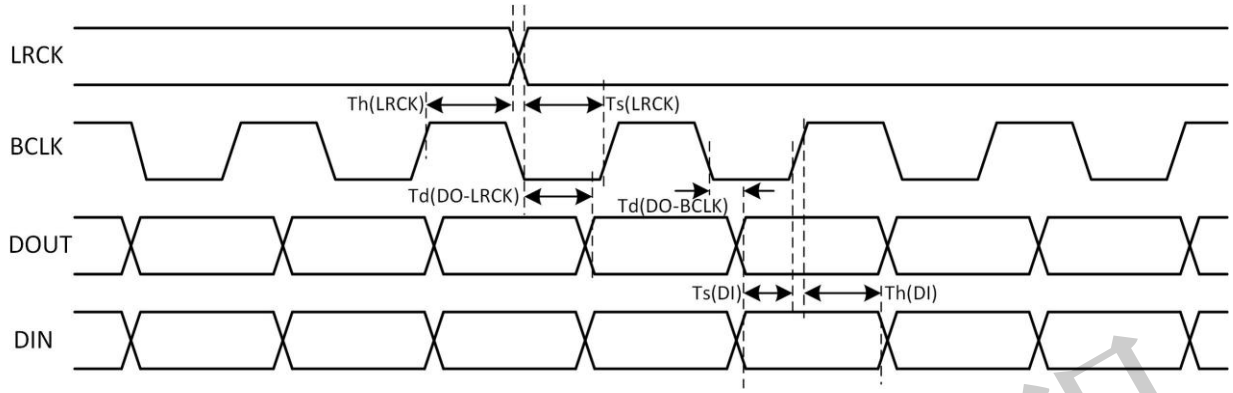

Figure 2- 40. I2S/PCM in Slave Mode Timing

Table 2- 32. I2S/PCM in Slave Mode Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
LRCK Setup	T_s(LRCK)	4	-	-	ns
LRCK Hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT Delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT Delay	T_d(DO-BCLK)	-	-	10	ns
DIN Setup	T_s(DI)	4	-	-	ns
DIN Hold	T_h(DI)	4	-	-	ns
BCLK Rise Time	T_r	-	-	4	ns
BCLK Fall Time	T_f	-	-	4	ns

2.5.7. SPI Interface Timing

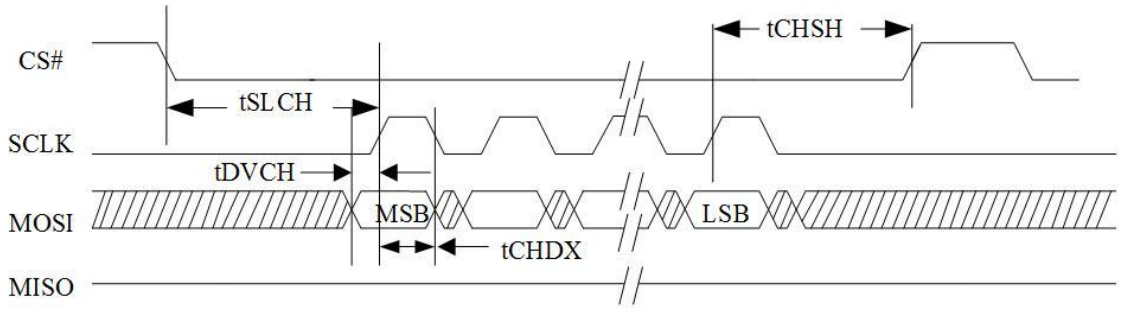

Figure 2- 41. SPI MOSI Timing

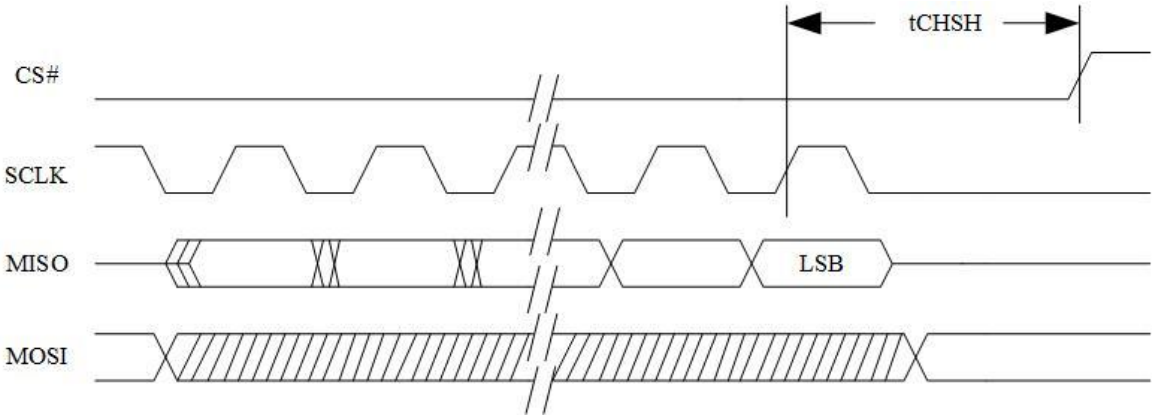

Figure 2- 42. SPI MISO Timing

Table 2- 33. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
Note: T is the cycle of clock.					

2.5.8. UART Interface Timing

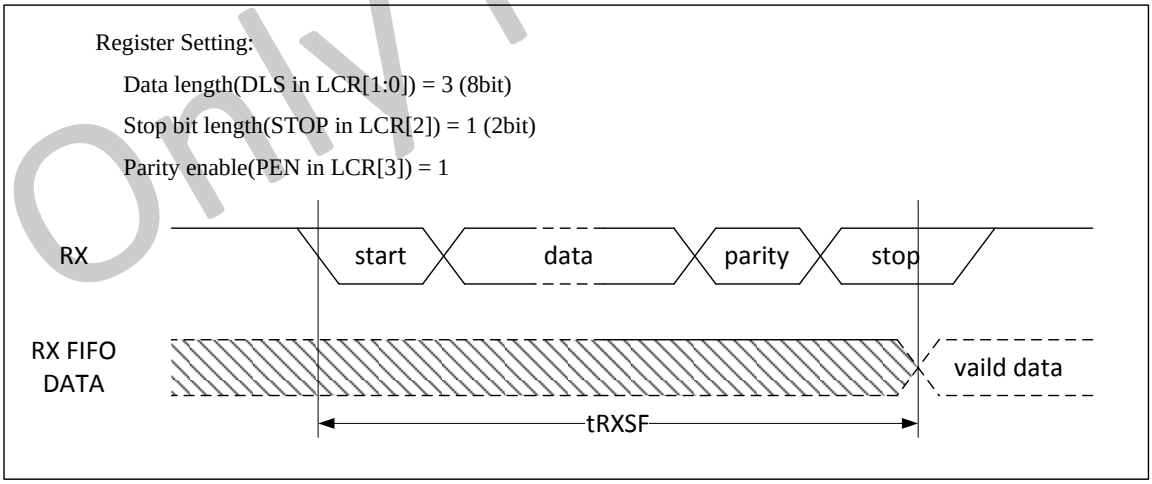

Figure 2- 43. UART RX Timing

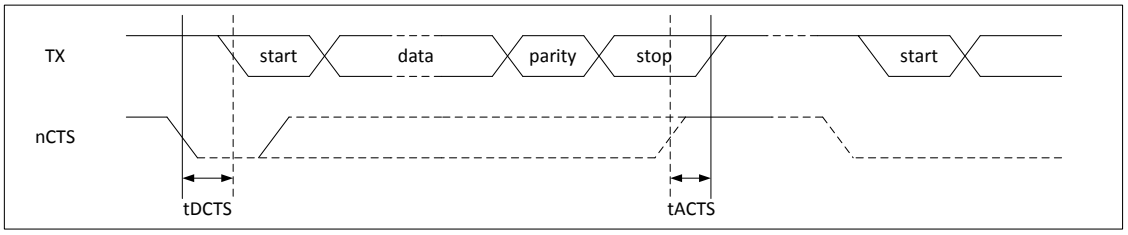

Figure 2- 44. UART nCTS Timing

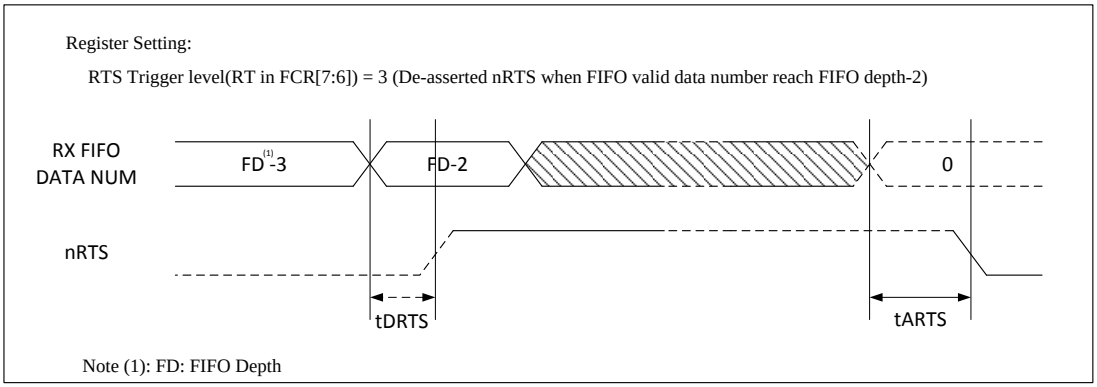

Figure 2- 45. UART nRTS Timing

Table 2- 34. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP	ns
Delay time of asserted nRTS	tARTS	-	-	BRP	ns
BRP: Baud-Rate Period.					

2.5.9. TWI Interface Timing

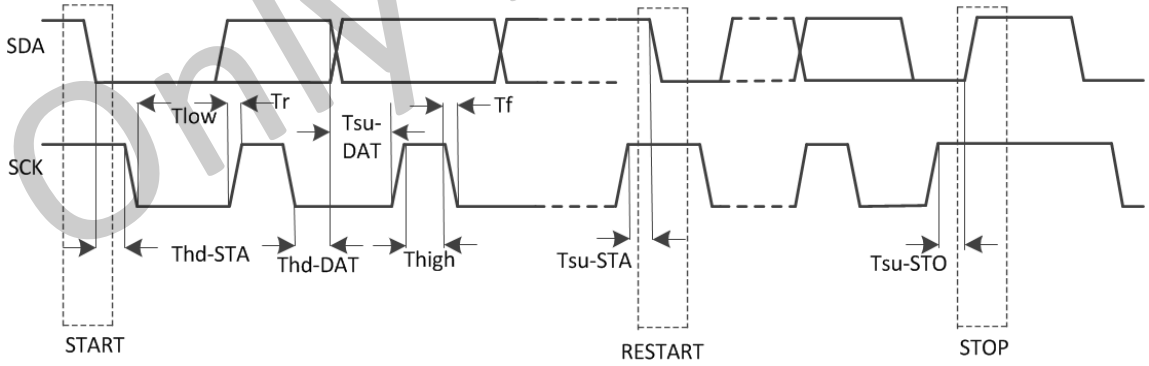

Figure 2- 46. TWI Timing

Table 2- 35. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in start	Tsu-STA	4.7	-	0.6	-	us
Hold time in start	Thd-STA	4.0	-	0.6	-	us
Setup time in data	Tsu-DAT	250	-	100	-	ns
Hold time in data	Thd-DAT	5.0	-	-	-	ns

Setup time in stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns
SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

2.5.10. MIPI DSI Interface Timing

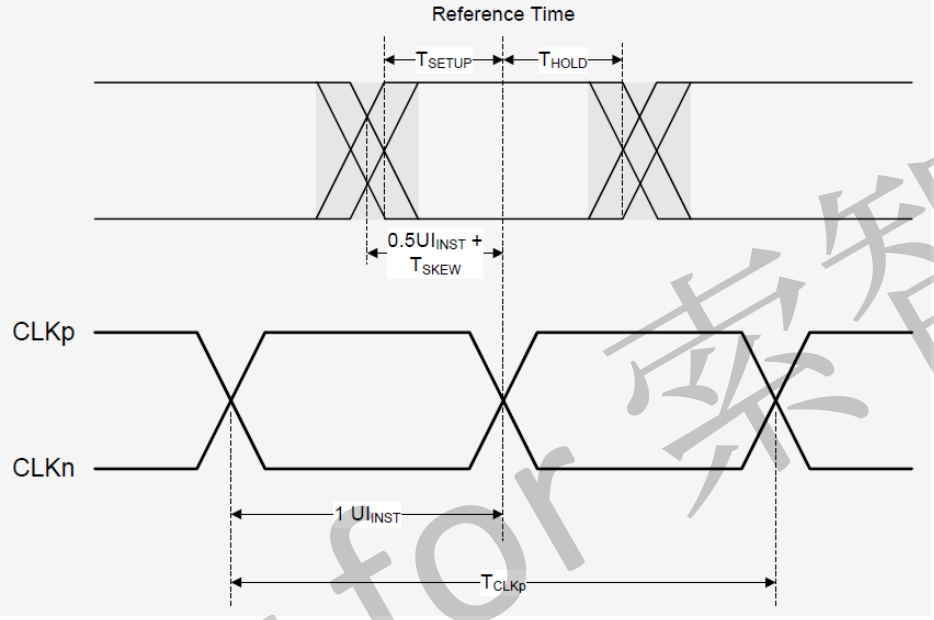

Figure 2- 47. MIPI DSI Timing Diagram

Table 2- 36. MIPI DSI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock Skew	T_{SKEW}	-0.15	-	0.15	UI_{INST}
Data to Clock Setup Time	T_{SETUP}	0.15	-	-	UI_{INST}
Clock to Data Hold Time	T_{HOLD}	0.15	-	-	UI_{INST}

Contents

Figures

Tables

Chapter 3 System

3.1. Memory Mapping

Module	Address(It is for Cluster CPU)	Size(Bytes)
N-BROM	0x0000 0000---0x0000 FFFF	64K
SRAM A1	0x0002 0000---0x0003 7FFF	96K(support Byte operation, clock source is AHB1)
SRAM C	0x0003 8000---0x0005 8FFF	Borrow VE 132K, supports Byte operation, clock source is AHB1
Accelerator		
DE	0x0100 0000---0x013F FFFF	4M
G2D	0x0148 0000---0x014B FFFF	256K
CE_NS	0x0190 4000---0x0190 47FF	2K
CE_S	0x0190 4800---0x0190 4FFF	2K
VE SRAM	0x01A0 0000---0x01BF FFFF	2M
VE	0x01C0 E000---0x01C0 FFFF	8K
ISP_SRAM	0x01D0 0000---0x020F FFFF	4M
ISP	0x0210 0000---0x0210 5FFF	24K
EISE	0x0230 0000---0x0230 0FFF	4K
EISE_SRAM	0x0230 1000---0x0238 0FFF	512K
NPU	0x0240 0000---0x0251 FFFF	1152K
System Resources		
SYS_CFG	0x0300 0000---0x0300 0FFF	4K
CCU	0x0300 1000---0x0300 1FFF	4K
DMA	0x0300 2000---0x0300 2FFF	4K
HSTIMER	0x0300 5000---0x0300 5FFF	4K
SID	0x0300 6000---0x0300 6FFF	4K
SMC	0x0300 7000---0x0300 7FFF	4K
TIMER	0x0300 9000---0x0300 93FF	1K
PWM	0x0300 A000---0x0300 A3FF	1K
GPIO	0x0300 B000---0x0300 B3FF	1K
PSI	0x0300 C000---0x0300 C3FF	1K
DCU	0x0301 0000---0x0301 FFFF	64K
GIC	0x0302 0000---0x0302 FFFF	64K
IOMMU	0x030F 0000---0x030F FFFF	64K

Memory		
MSI_CTRL	0x0400 2000---0x0400 2FFF	4K
DRAM_CTRL&PHY	0x0400 3000---0x0400 5FFF	12K
SMHC0	0x0402 0000---0x0402 0FFF	4K
SMHC1	0x0402 1000---0x0402 1FFF	4K
SMHC2	0x0402 2000---0x0402 2FFF	4K
Interfaces		
UART0	0x0500 0000---0x0500 03FF	1K
UART1	0x0500 0400---0x0500 07FF	1K
UART2	0x0500 0800---0x0500 0BFF	1K
UART3	0x0500 0C00---0x0500 0FFF	1K
TWI0	0x0500 2000---0x0500 23FF	1K
TWI1	0x0500 2400---0x0500 27FF	1K
TWI2	0x0500 2800---0x0500 2BFF	1K
TWI3	0x0500 2C00---0x0500 2FFF	1K
SPI0	0x0501 0000---0x0501 0FFF	4K
SPI1	0x0501 1000---0x0501 1FFF	4K
SPI2	0x0501 2000---0x0501 2FFF	4K
EMAC0	0x0502 0000---0x0502 FFFF	64K
GPADC	0x0507 0000---0x0507 03FF	1K
THS	0x0507 0400---0x0507 07FF	1K
I2S/PCM0	0x0509 0000---0x0509 0FFF	4K
I2S/PCM1	0x0509 1000---0x0509 1FFF	4K
Audio Codec	0x0509 6000---0x0509 6FFF	4K
USB0(USB2.0_OTG)	0x0510 0000---0x051F FFFF	1M
Display		
MIPI_DSI0	0x0650 4000---0x0650 5FFF	8K
DISP_IF_TOP	0x0651 0000---0x0651 0FFF	4K
TCON_LCD0	0x0651 1000---0x0651 1FFF	4K
DSPO	0x0654 3000---0x0654 33FF	1K
CSI	0x0660 0000---0x0661 FFFF	128K
CSI_SRAM	0x0662 0000---0x0669 FFFF	512K
CPUS Domain		
RTC	0x0700 0000---0x0700 03FF	1K
R_PRCM	0x0701 0000---0x0701 03FF	1K
R_GPIO	0x0702 2000---0x0702 23FF	1K
R_OWC	0x0704 0400---0x0704 07FF	1K
R_TWI0	0x0708 1400---0x0708 17FF	1K
R_RSB	0x0708 3000---0x0708 33FF	1K
CPUX Related		
CPU_SUBSYS_CFG	0x0810 0000---0x0810 03FF	1K
TIMESTAMP_STU	0x0811 0000---0x0811 0FFF	4K
TIMESTAMP_CTRL	0x0812 0000---0x0812 0FFF	4K
IDC	0x0813 0000---0x0813 0FFF	3K

C0_CPUX_CFG	0x0901 0000---0x0901 03FF	1K
C0_CPUX_MBIST	0x0902 0000---0x0902 0FFF	4K
DRAM		
DRAM	0x4000 0000---0xFFFF FFFF	3G

3.2. CPUX Configuration

3.2.1. Overview

The C0_CPUX_CFG module is used for configuring cluster0(single Cortex-A7, 32KB I-cache and 32KB D-cache, 128KB L2 cache), such as reset, control, cache, debug, CPU status.
The CPU_SUBSYS_CTRL module is used for the system resource control of CPU sub-system, such as GIC-400, JTAG.

The CPUX_CFG includes the following features:

- CPU reset system: core reset, debug circuit reset and other reset function
- CPU related control: interface control, CP15 control
- CPU status check: idle status, SMP status, interrupt status and so on
- CPU debug related register for control and status

3.2.2. Operations and Functional Descriptions

3.2.2.1. Signal Description

For the detail of CPUX signal, please refer to ***ARM Cortex-A7 TRM***, such as ***DDI0464F_cortex_a7_mpcore_r0p5_trm.pdf.***

3.2.2.2. L2 Idle Mode

When the L2 cache of Cluster needs to enter WFI mode, firstly make sure that the CPU[0] of Cluster enters WFI mode, which can be checked through the bit[16] of **Cluster CPU Status Register**, and then pull high the **ACINACTM** of Cluster by writing 1 to the bit0 of **Cluster Control Register1** , and then check whether L2 enters idle status by checking whether the **STANDBYWFIL2** is high. Note that set the **ACINACTM** to low when exiting the L2 idle mode.

3.2.2.3. CPUX Reset System

The CPUX reset includes **core reset**, **power-on reset** and **H_Reset**. And their scopes rank: **core reset** < **power-on Reset** < **H_Reset**. The description of all reset signal in CPUX reset system is as follows.

Table 3- 1. Reset Signal Description

Reset Signal	Description
CORE_RST	This is the primary reset signal which resets the corresponding core logic that includes NEON and VFP, Debug, ETM, breakpoint and watchpoint logic. This maps to a warm reset that covers reset of the processor logic.

PWRON_RST	This power-on reset signal resets all the processor logic, including the Debug, ETM trace unit, breakpoint, watchpoint logic, and performance monitors logic. This maps to a cold reset that covers reset of the processor logic and the integrated debug functionality. This does not reset debug logic in the debug power domain. Including CORE_RST/ETM_RST/DBG_RST.
AXI2MBUS_RST	Reset the AXI2MBUS interface logic circuit.
L2_RST	This single, cluster-wide signal resets the L2 memory system and the logic in the SCU.
ETM_RST	Reset ETM debug logic circuit.
DBG_RST	Reset only the debug, and breakpoint and watchpoint logic in the processor power domain. It also resets the debug logic for each processor in the debug power domain.
SOC_DBG_RST	Reset all the debug logic including DBG_RST.
MBIST_RST	Reset all resettable registers in the cluster, for entry into, and exit from, MBIST mode.
H_RST	Including PWRON_RST/L2_RST/MBIST_RST/SOC_DBG_RST/C0_CPUX_CFG.
CPU_SUBSYS_RST	Including C0_H_RST/GIC-400/CPU_SUBSYS_CTRL.

3.2.2.4. CPUX Power Block Diagram

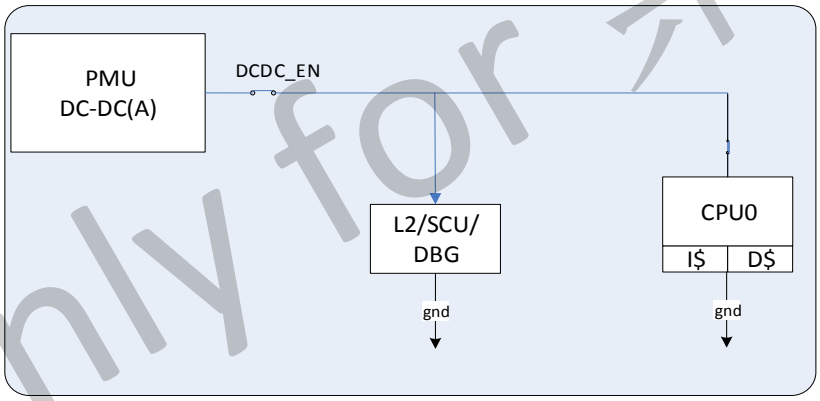

Figure 3- 1. CPUX Power Domain Block Diagram

CPU_SUBSYS_CTRL belongs to system power domain. The power domains of CPU related module are as follows.

Power Domain	Modules	Description
Cluster0	Cluster0/C0_CPUX_CFG/C0_MBIST	Cluster0 circuit, C0_CPUX_CFG module and CPU reset/power/mbist
System	Timestamp/GIC/CPU_SUBSYS_CTRL/Clock	Provide system source of CPU sub-system

3.2.2.5. Operation Principle

The CPU-related operations(such as open/close core, cluster switch, status query) need proper configuration of C0_CPUX_CFG module, as well as related system control resource including BUS, clock.

3.2.3. Programming Guidelines

For CPU core and cluster operation, please see the ***V833_CPU_AP_Note***.

3.2.4. Cluster 0 Configuration Register List

Module Name	Base Address
C0_CPUX_CFG	0x09010000

Register Name	Offset	Description
C0_RST_CTRL	0x0000	Cluster 0 Reset Control Register
C0_CTRL_REG0	0x0010	Cluster 0 Control Register0
C0_CTRL_REG1	0x0014	Cluster 0 Control Register1
C0_CTRL_REG2	0x0018	Cluster 0 Control Register2
CACHE_CFG_REG	0x0024	Cache Configuration Register
C0_CPU_STATUS	0x0080	Cluster 0 CPU Status Register
L2_STATUS_REG	0x0084	Cluster 0 L2 Status Register
DBG_REG0	0x00C0	Cluster 0 Debug Control Register0
DBG_REG1	0x00C4	Cluster 0 Debug Control Register1

3.2.5. Cluster 0 Configuration Register Description

3.2.5.1. 0x0000 Cluster 0 Reset Control Register(Default Value: 0x1311_0101)

Offset: 0x0000			Register Name: C0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	DDR_RST AXI2MBUS Logic Circuit Reset 0: assert 1: de-assert
27:26	/	/	/
25	R/W	0x1	MBIST_RST CPUBIST Reset The reset signal is for test. 0: assert 1: de-assert
24	R/W	0x1	SOC_DBG_RST Cluster SOC Debug Reset 0: assert 1: de-assert

23:21	/	/	/
20	R/W	0x1	ETM_RST Cluster ETM Reset Assert 0: assert 1: de-assert
19:17	/	/	/
16	R/W	0x1	DBG_RST Cluster Debug Reset Assert 0: assert 1: de-assert
15:9	/	/	/
8	R/W	0x1	L2_RST Cluster L2 Cache Reset 0: assert 1: de-assert
7:1	/	/	/
0	R/W	0x1	CORE_RESET Cluster CPU Reset Assert 0: assert 1: de-assert

3.2.5.2. 0x0010 Cluster 0 Control Register0(Default Value: 0x8000_0000)

Offset: 0x0010			Register Name: C0_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	SYSBAR_DISABLE Disable broadcasting of barriers onto system bus 0: Barriers are broadcast onto system bus, this requires an AMBA4 interconnect 1: Barriers are not broadcast onto the system bus. This is compatible with an AXI3 interconnect
30	R/W	0x0	BROADCAST_INNER Enable broadcasting of inner shareable transactions 0: Inner shareable transactions are not broadcasted externally 1: Inner shareable transactions are broadcasted externally
29	R/W	0x0	BROADCAST_OUTER Enable broadcasting of outer shareable transactions 0: Outer Shareable transactions are not broadcasted externally 0: Outer Shareable transactions are broadcasted externally
28	R/W	0x0	BROADCAST_CACHE_MAINT Enable broadcasting of cache maintenance operations to downstream caches 0: Cache maintenance operations are not broadcasted to downstream caches

			1: Cache maintenance operations are broadcasted to downstream caches
27:9	/	/	/
8	R/W	0x0	CP15S_DISABLE Disable write access to some secure CP15 register
7:5	/	/	/
4	R/W	0x0	L2_RST_DISABLE Disable automatic L2 cache invalidate at reset 0: L2 cache is reset by hardware 1: L2 cache is not reset by hardware
3:1	/	/	/
0	R/W	0x0	L1_RST_DISABLE Disable automatic Cluster CPU0 L1 cache invalidate at reset 0: L1 cache is reset by hardware 1: L1 cache is not reset by hardware

3.2.5.3. 0x0014 Cluster 0 Control Register1(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: C0_CTRL_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ACINACTM Snoop interface is inactive and no longer accepting requests 0: Snoop interface is active 1: Snoop interface is inactive

3.2.5.4. 0x0018 Cluster 0 Control Register2(Default Value: 0x0000_0010)

Offset: 0x0018			**Register Name: C0_CTRL_REG2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	EVENTI Event input for processor wake-up from WFE state. This bit must remain high for at least one clock cycle to be visible by the cores.
23:21	/	/	/
20	R/W	0x0	EXM_CLR[0] Clear the status of interface.
19:0	/	/	/

3.2.5.5. 0x0024 Cache Configuration Register(Default Value: 0x0018_1A1A)

Offset: 0x0024	**Register Name: CACHE_CFG_REG**

Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:19	R/W	0x3	EMA_L2D L2 Cache SRAM EMA control port
18:17	R/W	0x0	EMAW_L2D L2 Cache SRAM EMAW control port
16	R/W	0x0	EMAS_L2D L2 Cache SRAM EMAS control port
15:13	/	/	/
12:11	R/W	0x3	EMA_L1[2:0] L1 Cache SRAM EMA control port
10:9	R/W	0x1	EMAW_L1[1:0] L1 Cache SRAM EMAW control port
8	R/W	0x0	EMAS_L1[1:0] L1 Cache SRAM EMAS control port
7:6	/	/	/
5:3	R/W	0x3	EMA[2:0] Cache RF1P EMA control port
2:1	R/W	0x1	EMAW[1:0] Cache RF1P EMAW control port
0	R/W	0x0	EMAS Cache RF1P EMAS control port

3.2.5.6. 0x0080 Cluster0 CPU Status Register(Default Value: 0x0001_0000)

Offset: 0x0080			Register Name: C0_CPU_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	SMP_AMP CPU[0] is in Symmetric Multiprocessing mode or Asymmetric Multiprocessing mode. 0: AMP mode 1: SMP mode
23:17	/	/	/
16	R	0x1	STANDBYWFI. Indicates if Cluster CPU[0] is in WFI standby mode 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
15:9	/	/	/
8	R	0x0	STANDBYWFE. Indicates if Cluster CPU[0] is in the WFE standby mode 0: Processor not in WFE standby mode 1: Processor in WFE standby mode

7:1	/	/	/
0	R	0x0	STANDBYWFIL2. Indicates if the Cluster L2 memory system is in WFI standby mode. 0: Cluster L2 not in WFI standby mode 1: Cluster L2 in WFI standby mode

3.2.5.7. 0x0084 L2 Status Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: L2_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R	0x0	EVENTO Event output. This bit is asserted HIGH for 3 clock cycles when any core in the cluster executes an SEV instruction.
8:0	/	/	/

3.2.5.8. 0x00C0 Cluster 0 Debug Control Register0(Default Value:0x0000_0001)

Offset: 0x00C0			Register Name: DBG_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	DBGRESTART External restart requests.
7:1	/	/	/
0	R/W	0x1	C_DBGPWRDUP. Cluster Powered-up 0: Core is powered down 1: Core is powered up

3.2.5.9. 0x00C4 Cluster 0 Debug Control Register1(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: DBG_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DBGRESTARTED[0] Handshake for DBGRESTART.
11:5	/	/	/
4	R	0x0	C_DBGNOPWRDWN. No power-down request. Debugger has requested that processor is not powered down. Debug no power down[0].

3:1	/	/	/
0	R	0x0	C_DBGPWRUPREQ. Power up request. Debug power up request[0] 0: Do not request that the core is powered up 1: Request that the core is powered up

3.2.6. CPU Subsystem Control Register List

Module Name	Base Address
CPU_SUBSYS_CTRL	0x08100000

Register Name	Offset	Description
GENER_CTRL_REG0	0x0000	General Control Register0
GIC_JTAG_RST_CTRL	0x000C	GIC and Jtag Reset Control Register
C0_INT_EN	0x0010	Cluster0 Interrupt Enable Control Register
IRQ_FIQ_STATUS	0x0014	IRQ/FIQ Status Register
GENER_CTRL_REG2	0x0018	General Control Register2
DBG_STATE	0x001C	Debug State Register

3.2.7. CPU Subsystem Control Register Description

3.2.7.1. 0x0000 General Control Register0(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GENER_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	GIC_CFGSDISABLE Disables write access to some secure GIC registers.

3.2.7.2. 0x000C GIC and Jtag Reset Control Register(Default Value: 0x0000_0B01)

Offset: 0x000C			Register Name: GIC_JTAG_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EXM_CLR[0] Clear the status of interface, for debug
15:12	/	/	/
11	R/W	0x1	CS_RST CoreSight Reset.

			0: assert 1: de-assert
10	/	/	/
9	R/W	0x1	PORTRST Jtag portrst. 0: assert 1: de-assert
8	R/W	0x1	TRST. Jtag trst. 0: assert 1: de-assert
7:1	/	/	/
0	R/W	0x1	GIC_RST GIC_reset_cpu_reg 0: assert 1: de-assert

3.2.7.3. 0x0010 Cluster 0 Interrupt Enable Register(Default Value: 0x0000_FFFF)

Offset: 0x0010			Register Name: C0_INT_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	C0_GIC_EN Interrupt enable control register. Mask irq_out/firq_out to system domain.

3.2.7.4. 0x0014 GIC IRQ/FIQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: IRQ_FIQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0000	FIQ_OUT[15:0]
15:0	R/W	0x0000	IRQ_OUT[15:0]

3.2.7.5. 0x0018 General Control Register2(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GENER_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CDBGRSTACK Debug Reset ACK
15:1	/	/	/

0	R/W	0x0	C0_TSCLKCHANGE Cluster 0 Time Stamp change bit

3.2.7.6. 0x001C Debug State Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: DBG_STATE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	C0_DBG_STATE Cluster 0 is in debug mode or normal mode

3.3. CCU

3.3.1. Overview

The clock controller unit(CCU) controls the PLLs configuration and most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to other blocks in the system.

The CCU includes the following features:

- 7 PLLs
- Bus source and divisions
- Clock output control
- PLL bias control
- PLL tuning control
- PLL pattern control
- Configuring modules clock
- Bus clock gating
- Bus software reset
- PLL lock control

3.3.2. Operations and Functional Descriptions

3.3.2.1. System Bus Tree

Figure 3-2 shows a block diagram of the system bus tree.

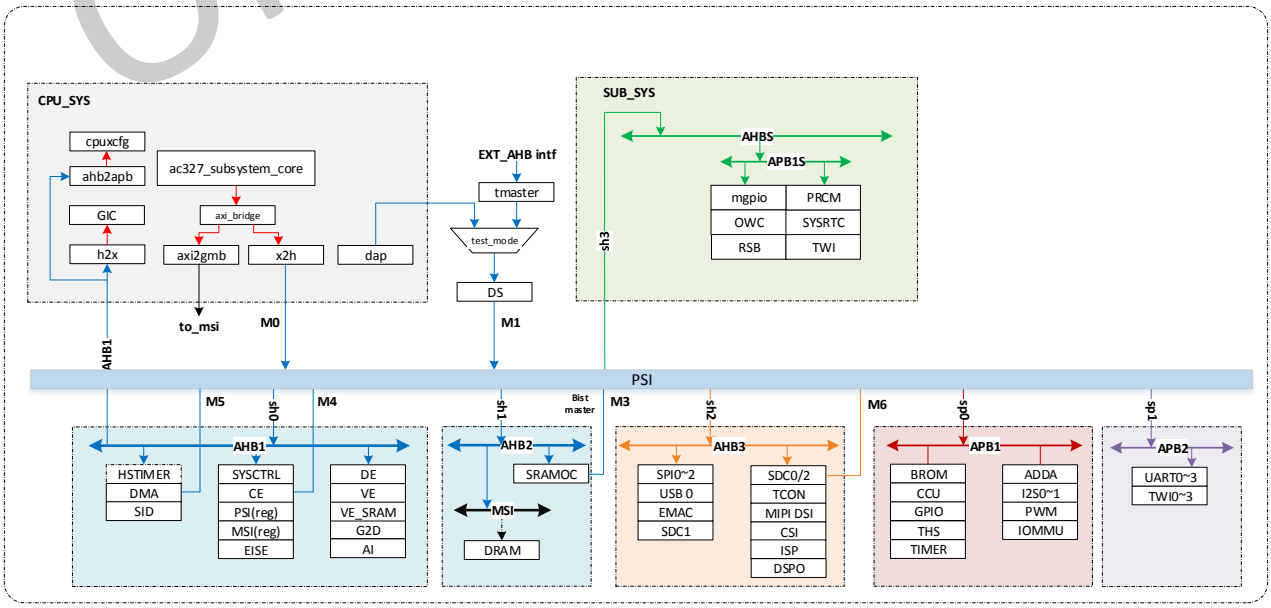

Figure 3- 2. System Bus Tree

3.3.2.2. Bus Clock Generation

Figure 3-3 describes bus clock generation.

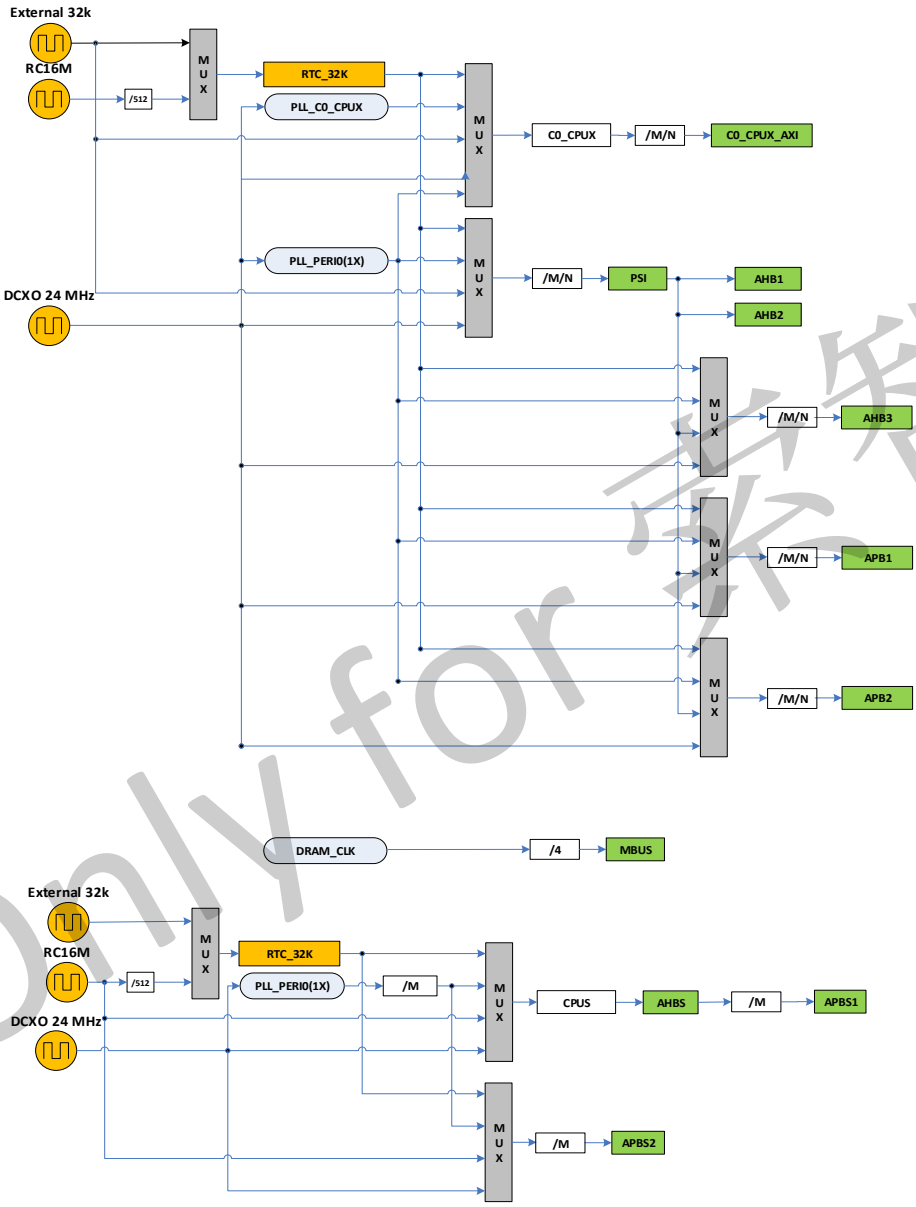

Figure 3- 3. Bus Clock Generation

3.3.2.3. Module Clock Generation

Figure 3-4 describes module clock generation. The frequencies in parantheses are the default typical frequencies.

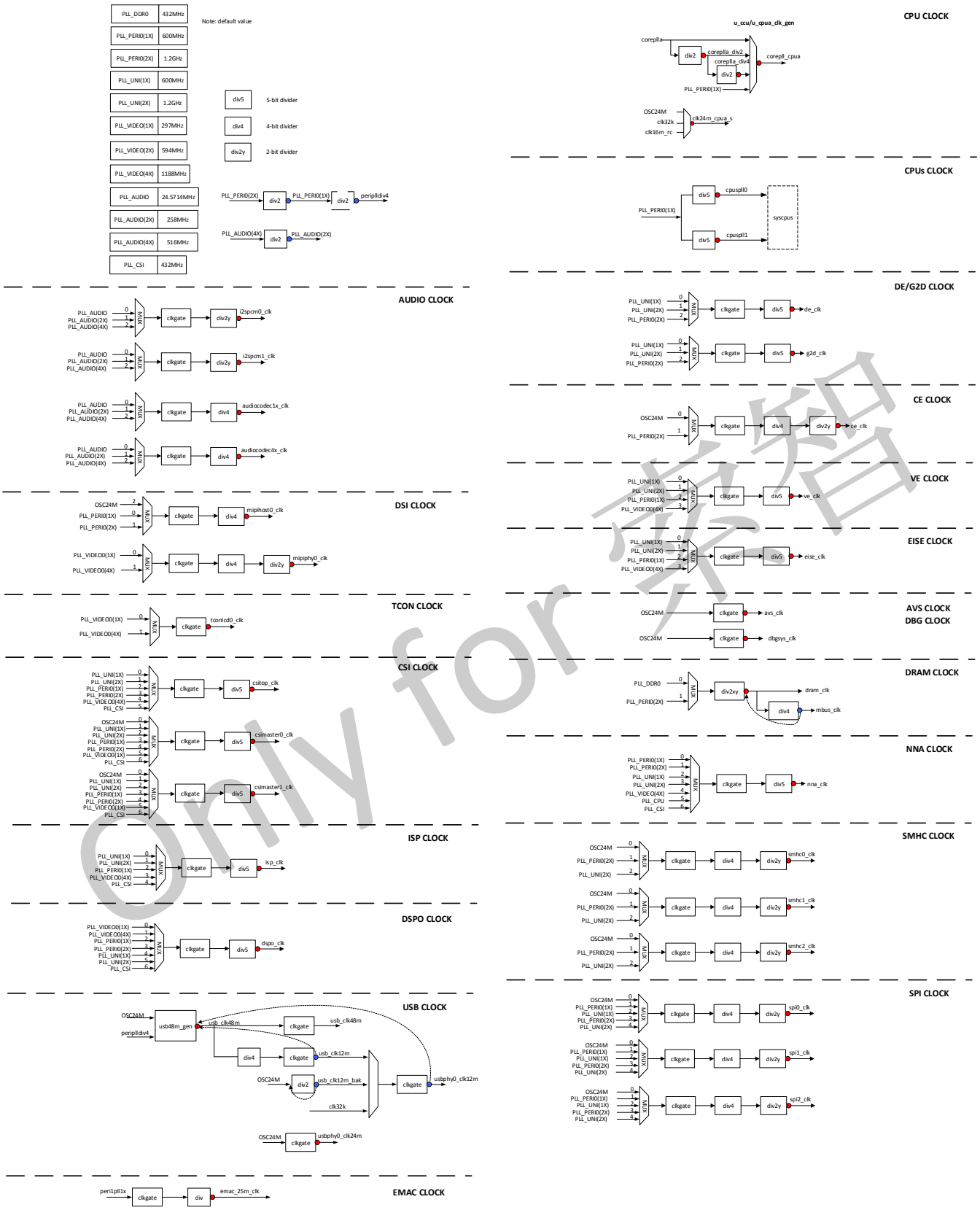

Figure 3- 4. Module Clock Generation

3.3.2.4. PLL Distribution

Figure 3-5 shows the block diagram of PLL distribution.

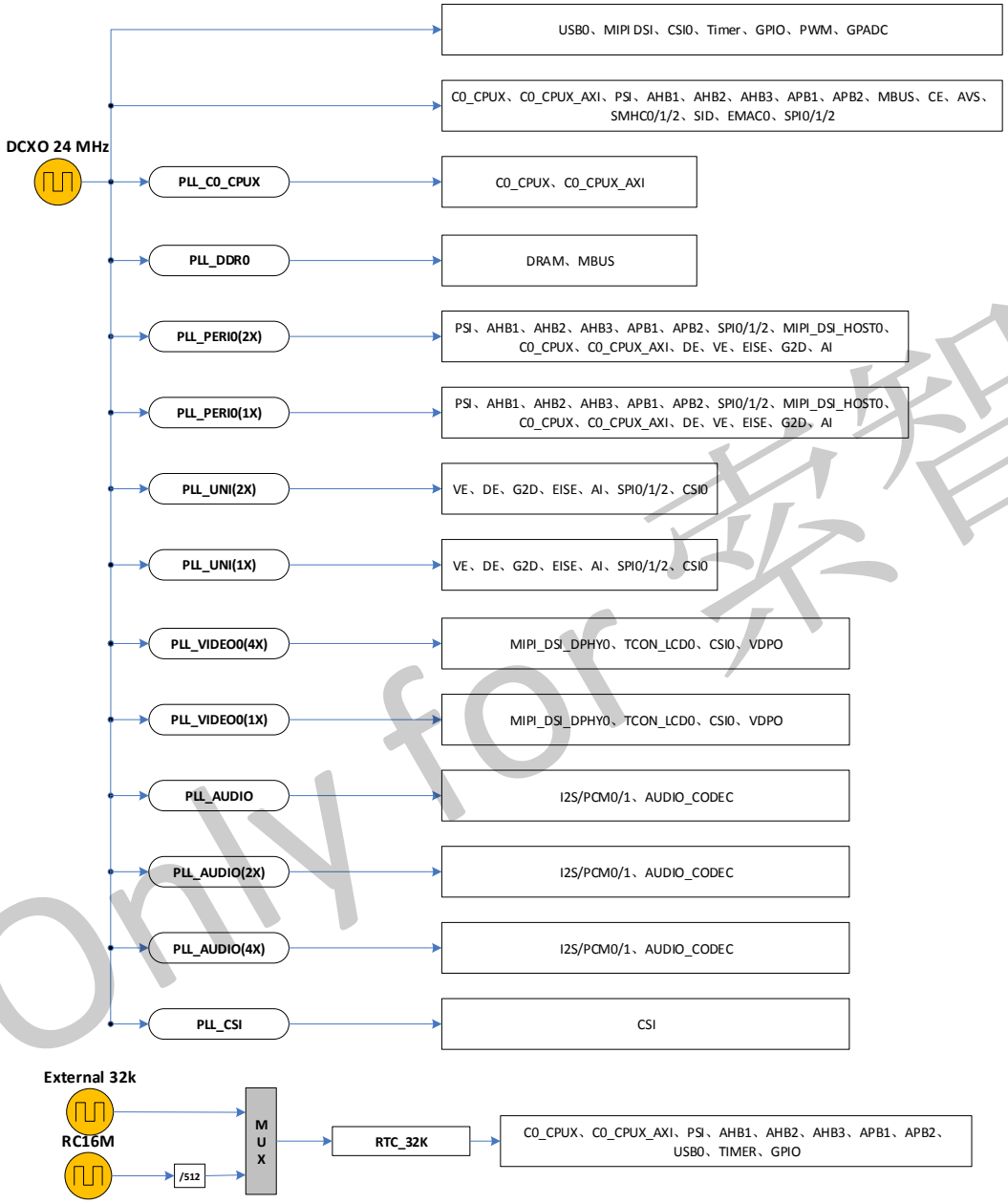

Figure 3- 5. PLL Distribution

3.3.2.5. PLL Features

Table 3- 2. PLL Features

PLL	Stable Operating Frequency	Actual Operating Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Lock Time
PLL_CPUX	288MHz~5.0GHz (24*N/div1)	288MHz~1.8GHz	No	No	No	<200ps	1.5ms
PLL_AUDIO	24.576MHz, 22.5792MHz, (24*N/div1/div2)	24.576MHz, 22.5792MHz, (24.576 * 8) MHz, (22.5792 * 8) MHz	Yes(fractional frequency division)	No	No	<200ps	500us
PLL_PERI0(2X)	180MHz~3.0GHz (24*N/div1/div2)	1.2GHz	Yes	No	No	<200ps	500us
PLL_UNI(2X)	180MHz~3.0GHz (24*N/div1/div2)	1.2GHz	Yes	No	No	<200ps	500us
PLL_VIDEO0(4X)	252MHz~3.0GHz (24*N/div)	192MHz~1.2GHz	Yes	No	No	<200ps	500us
PLL_DDR0	180MHz~3GHz (24*N/div1/div2)	192MHz~2GHz	Yes	No	No	200MHz~800MHz(<200ps) 800MHz~1.3GHz(<140ps) 1.3GHz~2.0GHz(<100ps)	2ms
PLL_CSI	180MHz~3GHz (24*N/div1/div2)	192MHz~600MHz	Yes	No	No	<200ps	500us

Table 3- 3. PLL Common Frequency

PLL Type		Frequency1(MHz)	Frequency2(MHz)	Note
PLL_UNI	PLL_UNI_1X	600	594	For DE,VE
	PLL_UNI_2X	1200	1188	
PLL_AUDIO		24.576	22.5792	For Audio
PLL_DDR0		1066	1600	For DDR, MBUS
PLL_CPU		1000	1200	For CPU
PLL_PERI	PLL_PERI_1X	600	594	For module, including DE, VE, etc
	PLL_PERI_2X	1200	1188	
PLL_VIDEO		600	/	For display interface
PLL_CSI		/	/	For CSI

Table 3- 4. Module Common Frequency

Module	Clock Source	Frequency(MHz)	DIV	Frequency Point(MHz)	Scene
CSI_MCLK	OSC24M	24	1	24	all
	PLL_CSI	297	11	27	
		others	/	others	
CSI_TOP	PLL_UNI_1X	600	15	40	720p30 (RAW data)
			10	60	1080p20 (RAW data)
			6	100	1080p30 (RAW data) 720p30 (YUV data)
			5	120	1080p20 2F WDR (RAW data)
			3	200	1080p30 2F WDR (RAW data) 1080p60/5M30 (RAW data) 1080p30 (YUV data)
	PLL_UNI_2X	1200	3	400	5M30 2F WDR (RAW data)
	PLL_CSI	0 ~600	/	/	others
ISP	PLL_UNI_1X	600	15	40	720p30
			12	50	1080p20 1080p20 2F WDR
			7	86	1080p30 1080p30 2F WDR

			3	200	5M30 5M30 2F WDR
VE/EISE	PLL_UNI_1X	600	6	100	720p30
			4	150	1080p20
			3	200	1080p30
	PLL_UNI_2X	1200	3	400	1080p60/5M30
DE	PLL_UNI_1X	600	8	75	VGA30
			4	150	720p60
			2	300	1080p60
G2D	PLL_UNI_1X	600	2	300	
AI	PLL_UNI_2X	1200	2	600	
			3	400	
			4	300	
			5	240	
			6	200	
			12	100	
SPI	PLL_PERI0_2X	1200	15	80	
SMHC	PLL_PERI0_2X	1200	8	150	
			12	100	
			24	50	
	PLL_UNI_2X	1200	8	150	
			24	50	
CPU	PLL_CPU	Independent PLL			
DDR	PLL_DDR0	1066	1	1066	
			2	533	
		1600	1	1600	
			2	800	
	PLL_PERI_2X	1200	1	1200	
			2	600	

3.3.3. Programming Guidelines

3.3.3.1. Frequency Adjustment of PLL_CPUX

The frequency configuration formula of PLL_CPUX: PLL_CPUX= 24MHz*N/P, where, the N parameter is frequency-doubling factor of PLL, the next parameter configuration can proceed after PLL relock; the P parameter is digital post-frequency division, which can be dynamically switched in real time, and it does not affect the normal work of PLL.

The CPU PLL supports dynamic frequency configuration (modify the value of N). The CPU should first switch to a lower intermediate frequency and then adjust to the target frequency when switching the frequency. The process is as follows.

(1) Before you configure PLL_CPU, switch the clock source of CPU to PLL_PERI0(1X).
(2) Modify the N, P parameter of PLL_CPU.
(3) Write the PLL Lock Enable bit to 0 and then write it to 1.
(4) Wait the Lock bit of PLL_CPUX_CTRL to 1.
(5) Switch the clock source of CPU to PLL_CPU.

3.3.3.2. Frequency Adjustment of PLL_AUDIO

The frequency configuration formula of PLL_AUDIO: PLL_AUDIO = 24MHz*N/M0/M1/P. Changing any parameter of N, M0, M1 and P will affect the normal work of PLL, which needs to be relocked. Therefore, dynamic adjustment is not supported.

For PLL_AUDIO, two frequency points usually are needed: 24.576MHz and 22.5792MHz. There are generally specific recommended configuration factors for the two frequencies. To implement the desired frequency point of PLL_AUDIO, you need to use the decimal frequency division function. The process is as follows.

(1) Configure the N, M1, M0, P factor.
(2) Configure the PLL_SDM_ENABLE bit of PLL_AUDIO_CTRL to 1.
(3) Configure PLL_AUDIO_PAT0_CTRL to enable digital spread spectrum.
(4) Write the PLL Lock Enable bit of PLL_AUDIO_CTRL to 0 and then write it to 1.
(5) Wait the Lock bit of PLL_AUDIO_CTRL to 1.

NOTE

The P factor of PLL_AUDIO is odd number, the clock output is non-equal duty.

3.3.3.3. Frequency Adjustment of PLL_DDR

For the clock of DDR, the switch of the clock source and the frequency division coefficient is burrless, but the frequency adjustment of the module should follow the following rules.

- From high frequency to low frequency: switch the clock source first, and then set the frequency division coefficient;
- From low frequency to high frequency: switch the frequency division coefficient first, and then modify clock source.

3.3.3.4. Frequency Adjustment of General PLL

(1) At present, the PLL should be enabled. If the PLL is not enabled, refer to the PLL process from disable to enable in section 3.3.3.5. For PLL, it is not suggested to switch during PLL using. When clock is not needed, it is suggested to configure the PLL_OUTPUT_EN bit of PLL_CTRL to disable the output gate of PLL.
(2) General PLL cannot be used in the process of frequency modulation. It is suggested to configure the PLL_OUTPUT_EN bit of PLL_CTRL to 0 in the process of PLL adjustment.
(3) Configure the N, M1, M0 factor. (It is not suggested to configure M1 factor, configure according to **<<PLL recommended configuration table>>**)
(4) Write the PLL Lock Enable bit of PLL_CTRL to 0 and then write it to 1.
(5) Wait the Lock bit of PLL_CTRL to 1.
(6) Configure PLL_OUTPUT_EN to 1.

3.3.3.5. PLL Disable to PLL Enable

(1) Configure the N, M1, M0 factor of PLL_CTRL_REG.
(2) Write the Enable bit of PLL_CTRL_REG to 1.
(3) Write the Lock Enable bit of PLL_CTRL_REG to 1.
(4) Wait the status of Lock to 1.
(5) Delay 20us, the PLL can be used.

3.3.3.6. PLL Enable to PLL Disable

(1) Write the Enable bit of PLL to 0.
(2) Write the Lock Enable bit of PLL_CTRL_REG to 0.

CAUTION

In the normal using of PLL, it is not recommended to switch PLL frequently, because the switch of PLL will cause mutual interference between PLL, which will affect the stability of the system. Therefore, it is recommended to turn off PLL by configuring the PLL_OUTPUT_EN bit of PLL_CTRL to 0, instead of writing 0 to the enable bit.

3.3.3.7. Bus Configuration

The Bus clock supports dynamic switching, but the process of switching needs to follow the following two rules.

- From high frequency to low frequency: switch the clock source first, and then set the frequency division factor;
- From low frequency to high frequency: switch the frequency division factor first, and then switch clock source.

3.3.3.8. Module Clock Configuration

For the bus gating and reset register of modules, the reset is de-asserted first, and then the CLK gating is enabled, to ensure that no problem will occur due to the module not being reset synchronously released.

For module clock, except DDR clock, the other clocks first configure the clock source and frequency division factor, then release the clock gating (that is, set to 1). For the configuration order of the clock source and frequency division factor, perform as the following rules:

- With the increasing of the clock source frequency, first configure frequency division factor, then configure the clock source;
- With the decreasing of the clock source frequency, first configure the clock source, then configure the frequency division factor.

3.3.3.9. Spread Spectrum Function

The configuration of spread spectrum follows the following steps.

Step1: Configure PLL_CTRL Register

- According to PLL frequency and PLL frequency formula f = [(N+1)/(M0+1)/(M1+1)+X] * 24MHz, suppose the value of divisor M0 and divisor M1, calculate factor N and decimal value X, and write M0、M1、N and PLL frequency to the PLL_CTRL register.
- Configure the SDM_Enable bit of the PLL_CTRL register to 1 to enable spread spectrum function.

NOTE

Having different PLL calculate formula for different PLL, please refer to each PLL_CTRL register.

Step 2: Configure PLL_PAT Register

- According to decimal value X and spread spectrum frequency (the bit[18:17] of the PLL_PAT register), calculate WAVE_BOT (= 2^{17} * X1) and WAVE_STEP (= 2^{17} * (X2-X1) / (24MHz/PREQ) * 2).
- Configure spread spectrum mode (SPR_FREQ_MODE) to 2 or 3.
- Configure the spread spectrum clock source select bit (SDM_CLK_SEL) to 0 by default. But if the PLL_INPUT_DIV_M1 bit of the PLL_CTRL register is 1, the bit should set to 1.
- Write WAVE_BOT、WAVE_STEP、PREQ、SPR_FREQ_MODE and SDM_CLK_SEL to the PLL_PAT register, and configure SIG_DELT_PAT_EN to 1.

Step 3: Delay 20us

3.3.4. Register List

Module Name	Base Address
CCU	0x03001000

Register Name	Offset	Description
PLL_CPUX_CTRL_REG	0x0000	PLL_CPUX Control Register
PLL_DDR0_CTRL_REG	0x0010	PLL_DDR0 Control Register
PLL_PERI0_CTRL_REG	0x0020	PLL_PERI0 Control Register
PLL_UNI_CTRL_REG	0x0028	PLL_UNI Control Register
PLL_VIDEO0_CTRL_REG	0x0040	PLL_VIDEO0 Control Register
PLL_AUDIO_CTRL_REG	0x0078	PLL_AUDIO Control Register
PLL_CSI_CTRL_REG	0x00E0	PLL_CSI Control Register
PLL_DDR0_PAT_CTRL_REG	0x0110	PLL_DDR0 Pattern Control Register
PLL_PERI0_PAT0_CTRL_REG	0x0120	PLL_PERI0 Pattern0 Control Register
PLL_PERI0_PAT1_CTRL_REG	0x0124	PLL_PERI0 Pattern1 Control Register
PLL_UNI_PAT0_CTRL_REG	0x0128	PLL_UNI Pattern0 Control Register
PLL_UNI_PAT1_CTRL_REG	0x012C	PLL_UNI Pattern1 Control Register
PLL_VIDEO0_PAT0_CTRL_REG	0x0140	PLL_VIDEO0 Pattern0 Control Register
PLL_VIDEO0_PAT1_CTRL_REG	0x0144	PLL_VIDEO0 Pattern1 Control Register
PLL_AUDIO_PAT0_CTRL_REG	0x0178	PLL_AUDIO Pattern0 Control Register
PLL_AUDIO_PAT1_CTRL_REG	0x017C	PLL_AUDIO Pattern1 Control Register
PLL_CSI_PAT0_CTRL_REG	0x01E0	PLL_CSI Pattern0 Control Register
PLL_CSI_PAT1_CTRL_REG	0x01E4	PLL_CSI Pattern1 Control Register
PLL_CPUX_BIAS_REG	0x0300	PLL_CPUX Bias Register
PLL_DDR0_BIAS_REG	0x0310	PLL_DDR0 Bias Register
PLL_PERI0_BIAS_REG	0x0320	PLL_PERI0 Bias Register
PLL_UNI_BIAS_REG	0x0328	PLL_UNI Bias Register
PLL_VIDEO0_BIAS_REG	0x0340	PLL_VIDEO0 Bias Register
PLL_AUDIO_BIAS_REG	0x0378	PLL_AUDIO Bias Register
PLL_CSI_BIAS_REG	0x03E0	PLL_CSI Bias Register
PLL_CPUX_TUN_REG	0x0400	PLL_CPUX Tuning Register
CPUX_AXI_CFG_REG	0x0500	CPUX_AXI Configuration Register
PSI_AHB1_AHB2_CFG_REG	0x0510	PSI_AHB1_AHB2 Configuration Register
AHB3_CFG_REG	0x051C	AHB3 Configuration Register
APB1_CFG_REG	0x0520	APB1 Configuration Register
APB2_CFG_REG	0x0524	APB2 Configuration Register
MBUS_CFG_REG	0x0540	MBUS Configuration Register
DE_CLK_REG	0x0600	DE Clock Register
DE_BGR_REG	0x060C	DE Bus Gating Reset Register

G2D_CLK_REG	0x0630	G2D Clock Register
G2D_BGR_REG	0x063C	G2D Bus Gating Reset Register
CE_CLK_REG	0x0680	CE Clock Register
CE_BGR_REG	0x068C	CE Bus Gating Reset Register
VE_CLK_REG	0x0690	VE Clock Register
VE_BGR_REG	0x069C	VE Bus Gating Reset Register
EISE_CLK_REG	0x06D0	EISE Clock Register
EISE_BGR_REG	0x06DC	EISE Bus Gating Reset Register
NPU_CLK_REG	0x06E0	NPU Clock Register
NPU_BGR_REG	0x06EC	NPU Bus Gating Reset Register
DMA_BGR_REG	0x070C	DMA Bus Gating Reset Register
HSTIMER_BGR_REG	0x073C	HSTIMER Bus Gating Reset Register
AVS_CLK_REG	0x0740	AVS Clock Register
DBGSYS_BGR_REG	0x078C	DBGSYS Bus Gating Reset Register
PSI_BGR_REG	0x079C	PSI Bus Gating Reset Register
PWM_BGR_REG	0x07AC	PWM Bus Gating Reset Register
DRAM_CLK_REG	0x0800	DRAM Clock Register
MBUS_MAT_CLK_GATING_REG	0x0804	MBUS Master Clock Gating Register
DRAM_BGR_REG	0x080C	DRAM Bus Gating Reset Register
SMHC0_CLK_REG	0x0830	SMHC0 Clock Register
SMHC1_CLK_REG	0x0834	SMHC1 Clock Register
SMHC2_CLK_REG	0x0838	SMHC2 Clock Register
SMHC_BGR_REG	0x084C	SMHC Bus Gating Reset Register
UART_BGR_REG	0x090C	UART Bus Gating Reset Register
TWI_BGR_REG	0x091C	TWI Bus Gating Reset Register
SPI0_CLK_REG	0x0940	SPI0 Clock Register
SPI1_CLK_REG	0x0944	SPI1 Clock Register
SPI2_CLK_REG	0x0948	SPI2 Clock Register
SPI_BGR_REG	0x096C	SPI Bus Gating Reset Register
EPHY_25M_CLK_REG	0x0970	EPHY_25M Clock Register
EMAC_BGR_REG	0x097C	EMAC Bus Gating Reset Register
GPADC_BGR_REG	0x09EC	GPADC Bus Gating Reset Register
THS_BGR_REG	0x09FC	THS Bus Gating Reset Register
I2S/PCM0_CLK_REG	0x0A10	I2S/PCM0 Clock Register
I2S/PCM1_CLK_REG	0x0A14	I2S/PCM1 Clock Register
I2S/PCM2_CLK_REG	0x0A18	I2S/PCM2 Clock Register
I2S/PCM_BGR_REG	0x0A1C	I2S/PCM Bus Gating Reset Register
AUDIO_CODEC_1X_CLK_REG	0x0A50	AUDIO CODEC 1X Clock Register
AUDIO_CODEC_4X_CLK_REG	0x0A54	AUDIO CODEC 4X Clock Register
AUDIO_CODEC_BGR_REG	0x0A5C	AUDIO CODEC Bus Gating Reset Register
USB0_CLK_REG	0x0A70	USB0 Clock Register
USB_BGR_REG	0x0A8C	USB Bus Gating Reset Register
MIPI_DSI_DPHY0_HS_CLK_REG	0x0B20	MIPI DSI DPHY0 High Speed Clock Register

MIPI_DSI_HOST0_CLK_REG	0x0B24	MIPI DSI Host0 Clock Register
MIPI_BGR_REG	0x0B4C	MIPI DSI BUS GATING RESET Register
DISPLAY_IF_TOP_BGR_REG	0x0B5C	DISPLAY_IF_TOP BUS GATING RESET Register
TCON_LCD0_CLK_REG	0x0B60	TCON LCD0 Clock Register
TCON_LCD_BGR_REG	0x0B7C	TCON LCD BUS GATING RESET Register
CSI_MISC_CLK_REG	0x0C00	CSI MISC Clock Register
CSI_TOP_CLK_REG	0x0C04	CSI TOP Clock Register
CSI_MST_CLK0_REG	0x0C08	CSI_ Master Clock0 Register
CSI_MST_CLK1_REG	0x0C0C	CSI_ Master Clock1 Register
ISP_CLK_REG	0x0C20	ISP Clock Register
CSI_BGR_REG	0x0C2C	CSI Bus Gating Reset Register
DSPO_CLK_REG	0x0C60	DSPO Clock Register
DSPO_BGR_REG	0x0C6C	DSPO BUS GATING RESET Register
PLL_LOCK_DBG_CTRL_REG	0x0F04	PLL Lock Debug Control Register

3.3.5. Register Description

3.3.5.1. 0x0000 PLL_CPUX Control Register (Default Value: 0x0A00_1000)

Offset: 0x0000			**Register Name: PLL_CPUX_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_CPUX=24MHz*N/P **The PLL_CPUX output frequency must be in the range from 200MHz to 3GHz. And the default value of PLL_CPUX is 408MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:24	R/W	0x0	PLL_LOCK_TIME. PLL lock time The bit indicates the step amplitude from one frequency to another.
23:18	/	/	/

17:16	R/W	0x0	PLL_OUT_EXT_DIVP PLL Output External Divider P 00: 1 01: 2 10: 4 11: / When output clock is less than 288MHz, clock frequency is output by dividing P.
15:8	R/W	0x10	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M PLL Factor M M = PLL_FACTOR_M + 1 PLL_FACTOR_M is from 0 to 3. **Note: The bit is only for testing.**

3.3.5.2. 0x0010 PLL_DDR0 Control Register (Default Value: 0x0800_2301)

Offset: 0x0010			**Register Name: PLL_DDR0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_DDR0= 24MHz*N/M0/M1 **The default value of PLL_DDR0 is 432MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0:Disable

			1:Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.3. 0x0020 PLL_PERI0 Control Register (Default Value: 0x0800_3100)

Offset: 0x0020			**Register Name: PLL_PERI0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_PERI0(2X) = 24MHz*N/M0/M1 PLL_PERI0(1X) = 24MHz*N/M0/M1/2 **The default value of PLL_PERI0(2X) is 1.2GHz. The output clock of PLL_PERI0(2X) shall be fixed at 1.2GHz. It is not recommended to modify the value.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE

			0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x1	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1. PLL Input Div M1. M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0. PLL Output Div M0. M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.4. 0x0028 PLL_UNI Control Register (Default Value: 0x0800_3100)

Offset: 0x0028			**Register Name: PLL_UNI_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_UNI(2X) = 24MHz*N/M0/M1. PLL_UNI(1X) = 24MHz*N/M0/M1/2. **The default value of PLL_UNI(2X) is 1.2GHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable

			1: Enable
23:16	/	/	/
15:8	R/W	0x31	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x0	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.5. 0x0040 PLL_VIDEO0 Control Register (Default Value: 0x0800_6203)

Offset: 0x0040			**Register Name: PLL_VIDEO0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable For application, PLL_VIDEO0(4X)= 24MHz*N/M. PLL_VIDEO0(1X)=24MHz*N/M/4. **The default value of PLL_VIDEO0(4X) is 1188MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable

			1: Enable
23:16	/	/	/
15:8	R/W	0x62	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x1	PLL_INPUT_DIV_M PLL Input Div M M1=PLL_INPUT_DIV_M + 1 PLL_INPUT_DIV_M is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_D PLL Output Div D M0=PLL_OUTPUT_DIV_D + 1 PLL_OUTPUT_DIV_D is from 0 to 1. The bit is only for testing. For test, PLL_VIDEO0(4X) =24MHz*N/M/D

3.3.5.6. 0x0078 PLL_AUDIO Control Register (Default Value: 0x0814_2A01)

Offset: 0x0078			**Register Name: PLL_AUDIO_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable This PLL is for Audio. PLL_AUDIO = 24MHz*N/M0/M1/P. PLL_AUDIO(4X) = (24MHz*N/M1)/2 PLL_AUDIO(2X) = (24MHz*N/M1)/4 **7.5≤N/M0/M1≤125 and 12≤N** **The range of 24MHz*N/M0/M1 is from 180MHz to 3GHz.** **The default value of PLL_AUDIO is 24.5714MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0:Unlocked 1: Locked (It indicates that the PLL has been stable.) **Note: The bit is only valid when the bit29 is set to 1.**
27	R/W	0x1	PLL_OUTPUT_ENABLE 0:Disable 1:Enable

			The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE Spread Spectrum and Decimal Frequency Division 0: Disable 1: Enable
23:22	/	/	/
21:16	R/W	0x14	PLL_POST_DIV_P PLL Post-div P P= PLL_POST_DIV_P +1 PLL_POST_DIV_P is from 0 to 63.
15:8	R/W	0x2A	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.7. 0x00E0 PLL_CSI Control Register (Default Value: 0x0000_2301)

Offset: 0x00E0			**Register Name: PLL_CSI_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable PLL_CSI = 24MHz*N/M0/M1 **The default value of PLL_CSI is 432MHz.**
30	/	/	/
29	R/W	0x0	LOCK_ENABLE Lock Enable 0: Disable 1: Enable
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)

27	R/W	0x1	PLL_OUTPUT_ENABLE 0: Disable 1: Enable The bit is used to control the output enable of PLL.
26:25	/	/	/
24	R/W	0x0	PLL_SDM_ENABLE 0: Disable 1: Enable
23:16	/	/	/
15:8	R/W	0x23	PLL_FACTOR_N PLL Factor N N= PLL_FACTOR_N +1 PLL_FACTOR_N is from 0 to 254. In application, PLL_FACTOR_N shall be more than or equal to 11.
7:2	/	/	/
1	R/W	0x0	PLL_INPUT_DIV_M1 PLL Input Div M1 M1=PLL_INPUT_DIV_M1 + 1 PLL_INPUT_DIV_M1 is from 0 to 1.
0	R/W	0x1	PLL_OUTPUT_DIV_M0 PLL Output Div M0 M0=PLL_OUTPUT_DIV_M0 + 1 PLL_OUTPUT_DIV_M0 is from 0 to 1.

3.3.5.8. 0x0110 PLL_DDR0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0110			**Register Name: PLL_DDR0_PAT_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**

18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.9. 0x0120 PLL_PERI0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: PLL_PERI0_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1bit) 11: Triangular(nbit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.10. 0x0124 PLL_PERI0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: PLL_PERI0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/

24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.11. 0x0128 PLL_UNI Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0128			**Register Name: PLL_UNI_PAT0_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.12. 0x012C PLL_UNI Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x012C			**Register Name: PLL_UNI_PAT1_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN

19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.13. 0x0140 PLL_VIDEO0 Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PLL_VIDEO0_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.14. 0x0144 PLL_VIDEO0 Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: PLL_VIDEO0_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.15. 0x0178 PLL_AUDIO Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: PLL_AUDIO_PAT0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.16. 0x017C PLL_AUDIO Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x017C			Register Name: PLL_AUDIO_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.17. 0x01E0 PLL_CSI Pattern0 Control Register (Default Value: 0x0000_0000)

Offset: 0x01E0	Register Name: PLL_CSI_PAT0_CTRL_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN Sigma-Delta Pattern Enable
30:29	R/W	0x0	SPR_FREQ_MODE Spread Frequency Mode 00: DC=0 01: DC=1 10: Triangular(1 bit) 11: Triangular(n bit)
28:20	R/W	0x0	WAVE_STEP Wave Step
19	R/W	0x0	SDM_CLK_SEL SDM Clock Select 0: 24 MHz 1: 12 MHz **Note: When PLL_INPUT_DIV_M1 is 1, the bit is set to 1.**
18:17	R/W	0x0	FREQ Frequency 00: 31.5 kHz 01: 32 kHz 10: 32.5 kHz 11: 33 kHz
16:0	R/W	0x0	WAVE_BOT Wave Bottom

3.3.5.18. 0x01E4 PLL_CSI Pattern1 Control Register (Default Value: 0x0000_0000)

Offset: 0x01E4			Register Name: PLL_CSI_PAT1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DITHER_EN
23:21	/	/	/
20	R/W	0x0	FRAC_EN
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN

3.3.5.19. 0x300 PLL_CPUX Bias Register (Default Value: 0x8010_0000)

Offset: 0x0300			Register Name: PLL_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST VCO reset in

30:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CURRENT PLL current bias control [4:0], CPU_CP.
15:0	/	/	/

3.3.5.20. 0x310 PLL_DDR0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0310			Register Name: PLL_DDR0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.21. 0x320 PLL_PERI0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0320			Register Name: PLL_PERI0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.22. 0x0328 PLL_UNI Bias Register (Default Value: 0x0003_0000)

Offset: 0x0328			Register Name: PLL_UNI_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.23. 0x0340 PLL_VIDEO0 Bias Register (Default Value: 0x0003_0000)

Offset: 0x0340			Register Name: PLL_VIDEO0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.24. 0x0378 PLL_AUDIO Bias Register (Default Value: 0x0003_0000)

Offset: 0x0378			Register Name: PLL_AUDIO_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.25. 0x03E0 PLL_CSI Bias Register (Default Value: 0x0003_0000)

Offset: 0x03E0			Register Name: PLL_CSI_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x3	PLL_BIAS_CTRL PLL bias control [4:0]
15:0	/	/	/

3.3.5.26. 0x0400 PLL_CPUX Tuning Register (Default Value: 0x4440_4000)

Offset: 0x0400			Register Name: PLL_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x4	VCO_RNG_CTRL VCO range control [2:0] **Note: The value is recommended to use the default value, otherwise it will cause stability problems.**
27	/	/	/
26:24	R/W	0x4	KVCO_GAIN_CTRL KVCO gain control [2:0]
23	/	/	/
22:16	R/W	0x40	CNT_INIT_CTRL Counter initial control [6:0]
15	R/W	0x0	C_OD0 C-REG-OD0 for verify
14:8	R/W	0x40	C_B_IN C-B-IN [6:0] for verify
7	R/W	0x0	C_OD1 C-REG-OD1 for verify
6:0	RO	0x0	C_B_OUT

			C-B-OUT [6:0] for verify

3.3.5.27. 0x0500 CPUX_AXI Configuration Register (Default Value: 0x0000_0301)

Offset: 0x0500			Register Name: C0_CPUX_AXI_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: RTC_32K 010: RC16M 011: PLL_CPUX 100: PLL_PERI0(1X) 101: reserved 110: reserved 111: reserved CPUX Clock = Clock Source CPUX_AXI Clock = Clock Source/M CPUX _APB Clock = Clock Source/N
23:10	/	/	/
9:8	R/W	0x3	CPUX_APB_FACTOR_N 00:/1 01:/2 10:/4 11:/4
7:2	/	/	/
1:0	R/W	0x1	FACTOR_ M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.28. 0x0510 PSI_AHB1_AHB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0510			Register Name: PSI_AHB1_AHB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: RC16M 11: PLL_PERI0(1X) PSI_AHB1_AHB2 CLK = Clock Source/M/N.

23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.29. 0x051C AHB3 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x051C			Register Name: AHB3_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: PSI 11: PLL_PERI0(1X) AHB3 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.30. 0x0520 APB1 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0520			Register Name: APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL

			Clock Source Select 00: OSC24M 01: RTC_32K 10: PSI 11: PLL_PERI0(1X) APB1 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.31. 0x0524 APB2 Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0524			Register Name: APB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: RTC_32K 10: PSI 11: PLL_PERI0(1X) APB2 CLK = Clock Source/M/N.
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.32. 0x0540 MBUS Configuration Register (Default Value: 0xC000_0000)

Offset: 0x0540			Register Name: MBUS_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x1	MBUS_RST MBUS Reset 0: Assert 1: De-assert **Note: The clock of MBUS is from DRAM_CLK/4.**
29:0	/	/	/

3.3.5.33. 0x0600 DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0600			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_UNI(1X) 01: PLL_UNI(2X) 10: PLL_PERI0(2X) 11: /
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.34. 0x060C DE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x060C			Register Name: DE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DE_RST DE Reset 0: Assert 1: De-assert

15:1	/	/	/
0	R/W	0x0	DE_GATING Gating Clock For DE 0: Mask 1: Pass

3.3.5.35. 0x0630 G2D Clock Register (Default Value: 0x0000_0000)

Offset: 0x0630			Register Name: G2D_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_UNI(1X) 01: PLL_UNI(2X) 10: PLL_PERI0(2X) 11: /
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.36. 0x063C G2D Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x063C			Register Name: G2D_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	G2D_RST G2D Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	G2D_GATING Gating Clock For G2D 0: Mask 1: Pass

3.3.5.37. 0x0680 CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0680			Register Name: CE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:25	/	/	/
24	R/W	0x0	CLK_SRC_SEL Clock Source Select 0: OSC24M 1: PLL_PERI0(2X)
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.38. 0x068C CE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x068C			Register Name: CE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CE_RST CE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CE_GATING Gating Clock for CE 0: Mask 1: Pass

3.3.5.39. 0x0690 VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0690			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_UNI(1X) 01: PLL_UNI(2X) 10: PLL_PERI0(1X) 11: PLL_VIDEO0(4X)
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.40. 0x069C VE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x069C			Register Name: VE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	VE_RST VE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	VE_GATING Gating Clock for VE 0: Mask 1: Pass

3.3.5.41. 0x06D0 EISE Clock Register (Default Value: 0x0000_0000)

Offset: 0x06D0			Register Name: EISE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock

			0: Clock is OFF 1: Clock is ON SCLK = Clock Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_UNI(1X) 01: PLL_UNI(2X) 10: PLL_PERI0(1X) 11: PLL_VIDEO0(4X)
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.42. 0x06DC EISE Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06DC			Register Name: EISE_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EISE_RST EISE Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	EISE_GATING Gating Clock for EISE 0: Mask 1: Pass

3.3.5.43. 0x06E0 NPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x06E0			Register Name: NPU_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30	R/W	0x0	MODULE RST NPU Module Reset Control 0: Assert

			1: De-assert
29:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_PERI0(1X) 001: PLL_PERI0(2X) 010: PLL_UNI(1X) 011: PLL_UNI(2X) 100: PLL_VIDEO(4X) 101: PLL_CPU 110: PLL_CSI
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.44. 0x06EC NPU Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x06EC			Register Name: NPU_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	NPU_RST NPU Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	NPU_GATING Gating Clock for NPU 0: Mask 1: Pass

3.3.5.45. 0x070C DMA Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x070C			Register Name: DMA_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DMA_RST DMA Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DMA_GATING

			Gating Clock for DMA 0: Mask 1: Pass **Note: The working clock of DMA is from AHB1.**

3.3.5.46. 0x073C HSTIMER Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x073C			Register Name: HSTIMER_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HSTIMER_RST HSTIMER Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	HSTIMER_GATING Gating Clock for HSTIMER 0: Mask 1: Pass **Note: The working clock of HSTIMER is from AHB1.**

3.3.5.47. 0x0740 AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0740			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.5.48. 0x078C DBGSYS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x078C			Register Name: DBGSYS_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DBGSYS_RST DBGSYS Reset 0: Assert 1: De-assert

15:1	/	/	/
0	R/W	0x0	DBGSYS_GATING Gating Clock for DBGSYS 0: Mask 1: Pass **Note: The working clock of DBGSYS is from OSC24M.**

3.3.5.49. 0x079C PSI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x079C			**Register Name: PSI_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PSI_RST PSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PSI_GATING Gating Clock for PSI 0: Mask 1: Pass **Note: The working clock of PSI is from PSI clock.**

3.3.5.50. 0x07AC PWM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x07AC			**Register Name: PWM_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PWM_RST PWM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	PWM_GATING Gating Clock for PWM 0: Mask 1: Pass **Note: The working clock of PWM is from APB1 or OSC24M.**

3.3.5.51. 0x0800 DRAM Clock Register (Default Value: 0x0100_0000)

Offset: 0x0800			Register Name: DRAM_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	MODULE_RST Module Reset 0: Assert 1: De-assert SCLK = Clock Source/M.
29:26	/	/	/
25:24	R/W	0x1	CLK_SRC_SEL Clock Source Select 00: PLL_DDR0 01: PLL_PERI0(2X) Others: / **Note: A no-burr switch is necessary.**
23:2	/	/	/
1:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 3.

3.3.5.52. 0x0804 MBUS Master Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0804			Register Name: MBUS_MAT_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	VDPO_MCLK_GATING Gating MBUS Clock For VDPO 0:Mask 1:Pass
24	/	/	/
23	R/W	0x0	EISE_MCLK_GATING Gating MBUS Clock For EISE 0: Mask 1: Pass
22:11	/	/	/
10	R/W	0x0	G2D_MCLK_GATING Gating MBUS Clock For G2D 0: Mask 1: Pass
9	R/W	0x0	ISP_MCLK_GATING Gating MBUS Clock For ISP

			0: Mask 1: Pass
8	R/W	0x0	CSI_MCLK_GATING Gating MBUS Clock For CSI 0: Mask 1: Pass
7:3	/	/	/
2	R/W	0x0	CE_MCLK_GATING Gating MBUS Clock For CE 0: Mask 1: Pass
1	R/W	0x0	VE_MCLK_GATING Gating MBUS Clock For VE 0: Mask 1: Pass
0	R/W	0x0	DMA_MCLK_GATING Gating MBUS Clock For DMA 0: Mask 1: Pass

NOTE

DE MCLK is put in DE module to control.

3.3.5.53. 0x080C DRAM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x080C			Register Name: DRAM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DRAM_RST DRAM Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DRAM_GATING Gating Clock for DRAM 0: Mask 1: Pass

3.3.5.54. 0x0830 SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0830	Register Name: SMHC0_CLK_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_UNI(2X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.55. 0x0834 SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0834			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_UNI(2X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N

			Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.56. 0x0838 SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0838			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL_PERI0(2X) 10: PLL_UNI(2X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.57. 0x084C SMHC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x084C			Register Name: SMHC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:19	/	/	/
18	R/W	0x0	SMHC2_RST SMHC2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SMHC1_RST SMHC1 Reset 0: Assert 1: De-assert
16	R/W	0x0	SMHC0_RST SMHC0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SMHC2_GATING Gating Clock For SMHC2 0: Mask 1: Pass
1	R/W	0x0	SMHC1_GATING Gating Clock For SMHC1 0: Mask 1: Pass
0	R/W	0x0	SMHC0_GATING Gating Clock For SMHC0 0: Mask 1: Pass

3.3.5.58. 0x090C UART Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x090C			Register Name: UART_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	UART3_RST UART3 Reset 0: Assert 1: De-assert
18	R/W	0x0	UART2_RST UART2 Reset 0: Assert 1: De-assert
17	R/W	0x0	UART1_RST UART1 Reset 0: Assert 1: De-assert

16	R/W	0x0	UART0_RST UART0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	UART3_GATING Gating Clock for UART3 0: Mask 1: Pass
2	R/W	0x0	UART2_GATING Gating Clock for UART2 0: Mask 1: Pass
1	R/W	0x0	UART1_GATING Gating Clock for UART1 0: Mask 1: Pass
0	R/W	0x0	UART0_GATING Gating Clock for UART0 0: Mask 1: Pass

NOTE

The working clock of UART is APB2.

3.3.5.59. 0x091C TWI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x091C			Register Name: TWI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TWI3_RST TWI3 Reset 0: Assert 1: De-assert
18	R/W	0x0	TWI2_RST TWI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	TWI1_RST TWI1 Reset 0: Assert 1: De-assert

16	R/W	0x0	TWI0_RST TWI0 Reset 0: Assert 1: De-assert
15:4	/	/	/
3	R/W	0x0	TWI3_GATING Gating Clock for TWI3 0: Mask 1: Pass
2	R/W	0x0	TWI2_GATING Gating Clock for TWI2 0: Mask 1: Pass
1	R/W	0x0	TWI1_GATING Gating Clock for TWI1 0: Mask 1: Pass
0	R/W	0x0	TWI0_GATING Gating Clock for TWI0 0: Mask 1: Pass

NOTE

The working clock of TWI is APB2.

3.3.5.60. 0x0940 SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0940			Register Name: SPI0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_UNI(1X) 011: PLL_PERI0(2X) 100: PLL_UNI(2X)

			Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.61. 0x0944 SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0944			Register Name: SPI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_UNI(1X) 011: PLL_PERI0(2X) 100: PLL_UNI(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.62. 0x0948 SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0948			Register Name: SPI2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_PERI0(1X) 010: PLL_UNI(1X) 011: PLL_PERI0(2X) 100: PLL_UNI(2X) Others: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.63. 0x096C SPI Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x096C			Register Name: SPI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	SPI2_RST SPI2 Reset 0: Assert 1: De-assert
17	R/W	0x0	SPI1_RST SPI1 Reset 0: Assert 1: De-assert

16	R/W	0x0	SPI0_RST SPI0 Reset 0: Assert 1: De-assert
15:3	/	/	/
2	R/W	0x0	SPI2_GATING Gating Clock for SPI2 0: Mask 1: Pass
1	R/W	0x0	SPI1_GATING Gating Clock for SPI1 0: Mask 1: Pass
0	R/W	0x0	SPI0_GATING Gating Clock for SPI0 0: Mask 1: Pass

3.3.5.64. 0x0970 EPHY_25M Clock Register (Default Value: 0x0000_0000)

Offset: 0x0970			Register Name: EPHY_25M_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = PLL_PERI0(1X)/24 = 25M.
30	R/W	0x0	PLL_PERI0_GATING Gating PLL_PERI0 Clock 0: Clock is OFF 1: Clock is ON
29:0	/	/	/

3.3.5.65. 0x097C EMAC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x097C			Register Name: EMAC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	EMAC0_RST EMAC0 Reset 0: Assert 1: De-assert

15:1	/	/	/
0	R/W	0x0	EMAC0_GATING Gating Clock for EMAC0 0: Mask 1: Pass **Note: The working clock of EMAC is from AHB3.**

3.3.5.66. 0x09EC GPADC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09EC			**Register Name: GPADC_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	GPADC_RST GPADC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	GPADC_GATING Gating Clock for GPADC 0: Mask 1: Pass **Note: The working clock of GPADC is from OSC24M.**

3.3.5.67. 0x09FC THS Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x09FC			**Register Name: THS_BGR_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	THS_RST THS Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	THS_GATING Gating Clock for THS 0: Mask 1: Pass **Note: The working clock of THS is from OSC24M.**

3.3.5.68. 0x0A10 I2S/PCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A10			Register Name: I2S/PCM0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.69. 0x0A14 I2S/PCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A14			Register Name: I2S/PCM1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N

			Factor N 00: 1 01: 2 10: 4 11: 8
7:0	/	/	/

3.3.5.70. 0x0A1C I2S/PCM Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A1C			Register Name: I2S/PCM_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	I2S/PCM1_RST I2S/PCM1 Reset 0: Assert 1: De-assert
16	R/W	0x0	I2S/PCM0_RST I2S/PCM0 Reset 0: Assert 1: De-assert
15:2	/	/	/
1	R/W	0x0	I2S/PCM1_GATING Gating Clock for I2S/PCM1 0: Mask 1: Pass
0	R/W	0x0	I2S/PCM0_GATING Gating Clock for I2S/PCM0 0: Mask 1: Pass

3.3.5.71. 0x0A50 AUDIO CODEC 1X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A50			Register Name: AUDIO_CODEC_1X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select

			00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.72. 0x0A54 AUDIO CODEC 4X Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A54			Register Name: AUDIO_CODEC_4X_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_AUDIO 01: PLL_AUDIO(2X) 10: PLL_AUDIO(4X) 11: /
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.73. 0x0A5C AUDIO CODEC Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A5C			Register Name: AUDIO_CODEC_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	AUDIO_CODEC_RST AUDIO_CODEC Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	AUDIO_CODEC_GATING Gating Clock For AUDIO_CODEC

			0: Mask 1: Pass

3.3.5.74. 0x0A70 USB0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0A70			Register Name: USB0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING_OHCI0 Gating Special Clock For OHCI0 0: Clock is OFF 1: Clock is ON
30	R/W	0x0	USBPHY0_RST USB PHY0 Reset 0: Assert 1: De-assert
29	R/W	0x0	SCLK_GATING_USBPHY0 Gating Special Clock For USBPHY0 0: Clock is OFF 1: Clock is ON SCLK is from OSC24M.
28:26	/	/	/
25:24	R/W	0x0	OHCI0_12M_SRC_SEL OHCI0 12M Source Select 00: 12M divided from 48MHz 01: 12M divided from 24MHz 10: LOSC 11: /
23:0	/	/	/

3.3.5.75. 0x0A8C USB Bus Gating Reset Register (Default Value: 0x0000_0000)

Offset: 0x0A8C			Register Name: USB_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	USBOTG_RST USBOTG Reset 0: Assert 1: De-assert
23:21	/	/	/
20	R/W	0x0	USBEHCI0_RST USBEHCI0 Reset 0: Assert

			1: De-assert
19:17	/	/	/
16	R/W	0x0	USBOHCI0_RST USBOHCI0 Reset 0: Assert 1: De-assert
15:9	/	/	/
8	R/W	0x0	USBOTG_GATING Gating Clock For USBOTG 0: Mask 1: Pass
7:6	/	/	/
5	R/W	0x0	Reserved
4	R/W	0x0	USBEHCI0_GATING Gating Clock For USBEHCI0 0: Mask 1: Pass
3:1	/	/	/
0	R/W	0x0	USBOHCI0_GATING Gating Clock For USBOHCI0 0: Mask 1: Pass

3.3.5.76. 0x0B20 MIPI DSI DPHY0 High Speed Clock Register (Default Value: 0x0000_0000)

Offset: 0x0B20			Register Name: MIPI_DSI_DPHY0_HS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_VIDEO0(1X) 01: PLL_VIDEO0(4X) 10:/ 11:/
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N Factor N 00: 1

			01: 2 10: 4 11: 8
7:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.77. 0x0B24 MIPI DSI Host0 Clock Register(Default Value: 0x0000_0000)

Offset: 0x0B24			Register Name: MIPI_DSI_HOST0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: PLL_PERI0(1X) 01: PLL_PERI0(2X) 10: OSC24M 11:/
23:4	/	/	/
3:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 15.

3.3.5.78. 0x0B4C MIPI DSI Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0B4C			Register Name: MIPI_DSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MIPI_DSI_RST MIPI_DSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	MIPI_DSI_GATING Gating Clock For MIPI_DSI 0: Mask

			1: Pass

3.3.5.79. 0x0B5C DISPLAY_IF_TOP Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0B5C			Register Name: DISPLAY_IF_TOP_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	DISPLAY_IF_TOP_RST DISPLAY_IF_TOP Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DISPLAY_IF_TOP_GATING Gating Clock For DISPLAY_IF_TOP 0: Mask 1: Pass

3.3.5.80. 0x0B60 TCON LCD0 Clock Register(Default Value: 0x0000_0000)

Offset: 0x0B60			Register Name: TCON_LCD0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) 010: / 011: / 1XX:/
23:0	/	/	/

3.3.5.81. 0x0B7C TCON LCD0 Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0B7C			Register Name: TCON_LCD0_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/

16	R/W	0x0	TCON_LCD0_RST TCON_LCD0 Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	TCON_LCD0_GATING Gating Clock For TCON_LCD0 0: Mask 1: Pass

3.3.5.82. 0x0C04 CSI TOP Clock Register(Default Value: 0x0000_0000)

Offset: 0x0C04			Register Name: CSI_TOP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_UNI(1X) 001: PLL_UNI(2X) 010: PLL_PERI0(1X) 011: PLL_PERI0(2X) 100: PLL_VIDEO0(4X) 101: PLL_CSI Ohters: /
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.83. 0x0C08 CSI_Master Clock0 Register(Default Value: 0x0000_0000)

Offset: 0x0C08			Register Name: CSI_MST_CLK0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK0_GATING Gating CSI Master Clock0, this clock output to external device. 0: Clock is OFF 1: Clock is ON MCLK0 = Clock Source/M

30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_UNI(1X) 010: PLL_UNI(2X) 011: PLL_PERI0(1X) 100: PLL_PERI0(2X) 101: PLL_VIDEO0(1X) 110: PLL_CSI
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.84. 0x0C0C CSI_Master Clock1 Register(Default Value: 0x0000_0000)

Offset: 0x0C0C			Register Name: CSI_MST_CLK1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCLK1_GATING Gating CSI Master Clock1 0: Clock is OFF 1: Clock is ON MCLK1 = Clock Source/M
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: OSC24M 001: PLL_UNI(1X) 010: PLL_UNI(2X) 011: PLL_PERI0(1X) 100: PLL_PERI0(2X) 101: PLL_VIDEO0(1X) 110: PLL_CSI
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.85. 0x0C20 ISP Clock Register(Default Value: 0x0000_0000)

Offset: 0x0C20			Register Name: CSI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 000: PLL_UNI(1X) 001: PLL_UNI(2X) 010: PLL_PERI0(1X) 011: PLL_VIDEO0(4X) 100: PLL_CSI
23:5	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31.

3.3.5.86. 0x0C2C CSI Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0C2C			Register Name: CSI_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	CSI_RST CSI Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	CSI_GATING Gating Clock For CSI 0: Mask 1: Pass

3.3.5.87. 0x0C60 DSPO Clock Register(Default Value: 0x0000_0000)

Offset: 0x0C60			Register Name: DSPO_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = Clock Source/M/N.

30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO0(4X) 010: PLL_PERI0(1X) 011: PLL_PERI0(2X) 100: PLL_UNI(1X) 101: PLL_UNI(2X) 110: PLL_CSI
23:10	/	/	/
9:8	R/W	0x0	FACTOR_N. Factor N 00: 1 01: 2 10: 4 11: 8
7:4	/	/	/
4:0	R/W	0x0	FACTOR_M Factor M.(M= FACTOR_M +1) FACTOR_M is from 0 to 31

3.3.5.88. 0x0C6C DSPO Bus Gating Reset Register(Default Value: 0x0000_0000)

Offset: 0x0C6C			Register Name: DSPO_BGR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
16	R/W	0x0	DSPO_RST DSPO Reset 0: Assert 1: De-assert
15:1	/	/	/
0	R/W	0x0	DSPO_GATING Gating Clock For DSPO 0: Mask 1: Pass

3.3.5.89. 0x0F04 PLL Lock Debug Control Register(Default Value: 0x0000_0000)

Offset: 0x0F04			Register Name: PLL_LOCK_DBG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DBG_EN

			Debug Enable 0: Disable 1: Enable
30:25	/	/	/
24:20	R/W	0x0	DBG_SEL Debug Select 00000: PLL_CPUX 00001: / 00010: PLL_DDR0 00011:/ 00100: PLL_PERI0 00101: PLL_UNI 00110:/ 00111:/ 01000: PLL_VIDEO0 01001: / 01010: / 01011: / 01100: / 01101: / 01110: / 01111: PLL_AUDIO 10000: / 10001: / 10010: / 10011: / 10100: / 10101: / 10110: / 10111: / 11000: / 11001: / 11010: / 11100: PLL_CSI Others: /
19	/	/	/
18:17	R/W	0x0	UNLOCK_LEVEL Unlock Level 00: 21-29 Clock Cycles 01: 22-28 Clock Cycles 1X: 20-30 Clock Cycles
16	R/W	0x0	LOCK_LEVEL Lock Level 0: 24-26 Clock Cycles 1: 23-27 Clock Cycles

15:0	/	/	/

3.4. BROM System

3.4.1. Overview

The BROM system has several ways to boot. It has an integrated on-chip Boot ROM (BROM) which could be considered the primary program-loader. On startup process, the V833/V831 starts to fetch the first instruction from address 0x0, where is the BROM located at.

The BROM system is split up into two parts: FEL and Media Boot. The task of FEL is to write the external data to the local NVM, the task of the Media Boot is to load an effective and legitimate BOOT0 from NVM and running.

The module can support only be loaded after the certified firmware, this feature is enabled depending on the Anti Blushing bit, which is the AntiBlushing at SID module. If this bit is 1, it is enabled.

The BROM system includes the following features:

- CPU0 boot process
- Supports warm boot process
- Mandatory upgrade process through SMHC0, USB and UART
- Supports GPIO pin or eFuse to select the kind of boot media to boot
- Supports loading only certified firmware

3.4.2. Operations and Functional Descriptions

3.4.2.1. Boot Media Select

The BROM system supports the following boot media:

- SD/eMMC
- SPI NOR FLASH
- SPI NAND FLASH

There are two ways of Boot Select: **GPIO Pin Select** and **eFuse Select**. On startup, the BROM will read the state of BOOT_MODE, according to the state of BOOT_MODE to decide whether GPIO pin or eFuse to select the kind of boot media to boot. The BOOT_MODE is actually a bit at SID. Table 3-5 shows BOOT_MODE Setting.

Table 3- 5. BOOT_MODE Setting

BOOT_MODE(BROM_CONFIG[0] at SID)	Boot Select Type
0	GPIO pin select
1	eFuse select

If the state of the BOOT_MODE is 0, that is to choose GPIO pin. And in GPIO pin mode, there are two bits to select which boot media to boot. Table 3-6 shows boot media devices in GPIO pin mode.

Table 3- 6. GPIO Pin Boot Select Configuration

Pin_Boot_Select(at 0x03000024[10:9])	Boot Media
00	SMHC0->SPI NOR
01	SMHC0->SPI NAND
10	SMHC0->EMMC2
11	try

If the state of the BOOT_MODE is 1, that is to choose the eFuse type. The eFuse type has one 12 bits configuration, every 3 bits is divided into a group of the Boot Select, so it has four groups of boot_select. Table 3-7 shows eFuse Boot Select Configuration.

Table 3- 7. eFuse Boot Select Configuration

eFuse_Boot_Select_Cfg[11:0] (at BROM_TRY[11:0] of SID module)	Description
eFuse_Boot_Select[2:0]	eFuse_Boot_Select_1
eFuse_Boot_Select[5:3]	eFuse_Boot_Select_2
eFuse_Boot_Select[8:6]	eFuse_Boot_Select_3
eFuse_Boot_Select[11:9]	eFuse_Boot_Select_4

Table 3-8 describes each group of the eFuse Boot Select Setting. The first group to the third group are the same settings, but the fourth group need to be careful. If eFuse_Boot_Select_4 is set to 7, that means the way of the *Try*. The way of *Try* is followed by SMHC0, SPI NOR, SPI NAND, SMHC2.

Table 3- 8. eFuse Boot Select Setting

eFuse_Boot_Select_n	Boot Media
000	*Try*
001	Reserved
010	SMHC0->EMMC_USER->EMMC_BOOT
011	SMHC0->SPI NOR
100	SMHC0->SPI NAND
101	Reserved
110	SMHC0->EMMC_BOOT->EMMC_USER
111	The next group of the eFuse_Boot_Select. But when the n is equal to 7, it will be a way of *Try*.

Usually, no matter which boot media is selected, BROM will always try SMHC0 first at start up. It is possible to stop BROM from trying boot from SMHC0 by SMHC0_CLOSE setting. Table 3-9 shows SMHC0_CLOSE setting.

Table 3- 9. SMHC0_CLOSE Setting

SMHC0_CLOSE(at BROM_CONFIG[15] of SID module)	Try Boot from SMHC0
0	enabled
1	disabled

3.4.2.2. BROM Process

In Normal boot mode, the system boot will start from CPU0, BROM will read the Hotplug Flag Regsiter, according to the flag whether to go through the appropriate process. Finally, BROM will read the state of the FEL Pin, if the FEL Pin signal is detected pulling to high level, then the system will jump to the Try Media Boot process, or jump to the mandatory upgrade process. Figure 3-6 shows the BROM Process.

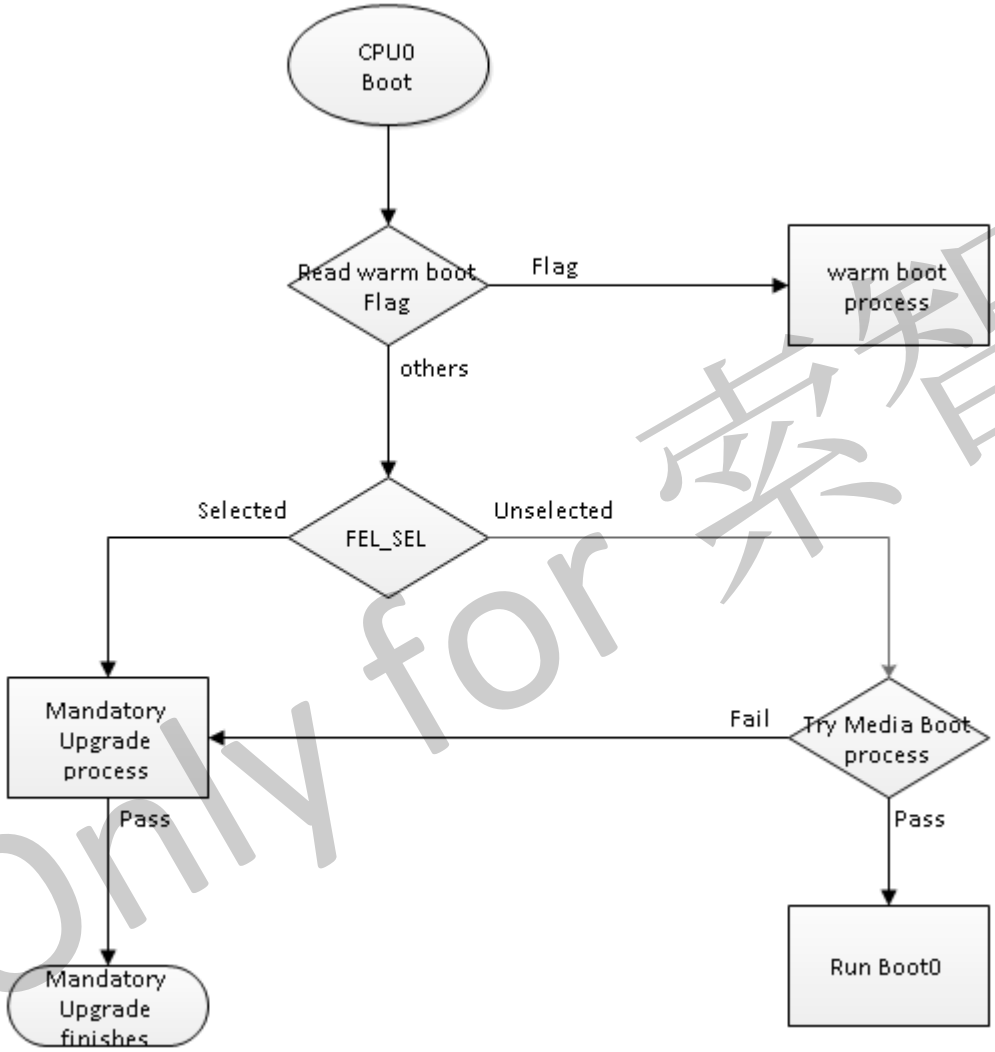

Figure 3- 6. Boot Process

3.4.2.3. BROM Process Description

3.4.2.3.1. Warm Boot Process

When the warm boot flag is set, BROM will set SRAM A1 to normal mode, then set up PLL, and run Boot0 Code, which is assumed already loaded into SRAM A1 properly.

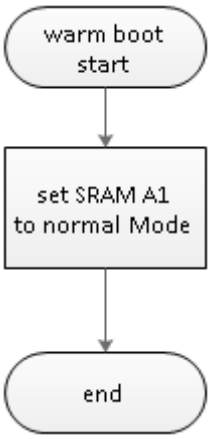

Figure 3- 7. Warm Boot Process

To enable warm boot, OS needs to set up flag and entry standby mode, as Figure 3-8 shows.

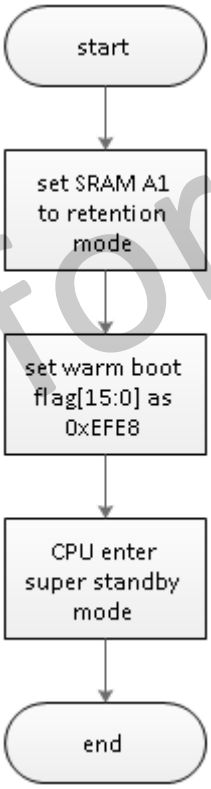

Figure 3- 8. Warm Boot Setting

3.4.2.3.2. Mandatory Upgrade Process

If the FEL Pin signal is detected pulling low, then the system will jump to mandatory upgrade process. And the process will first enter to UART Upgrade Process. After enter UART Upgrade Process, if system does not successfully hand shake before hand shake time out, it will enter the USB Upgrade Process. Figure 3-9 shows the mandatory upgrade process.

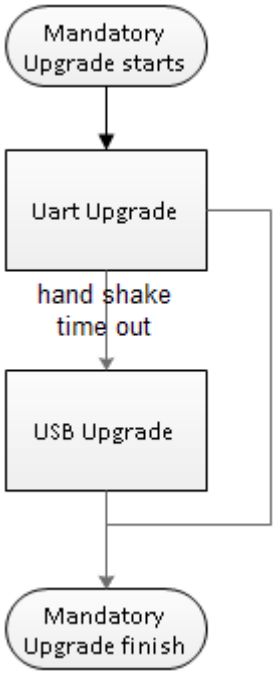

Figure 3- 9. Mandatory Upgrade Process

NOTE

The FEL address of the Normal BROM is 0x20.

3.4.2.3.3. FEL Process

When the system chooses to enter Mandatory Upgrade Process, then the system will jump to the FEL process. Figure 3-10 shows the FEL upgrade process.

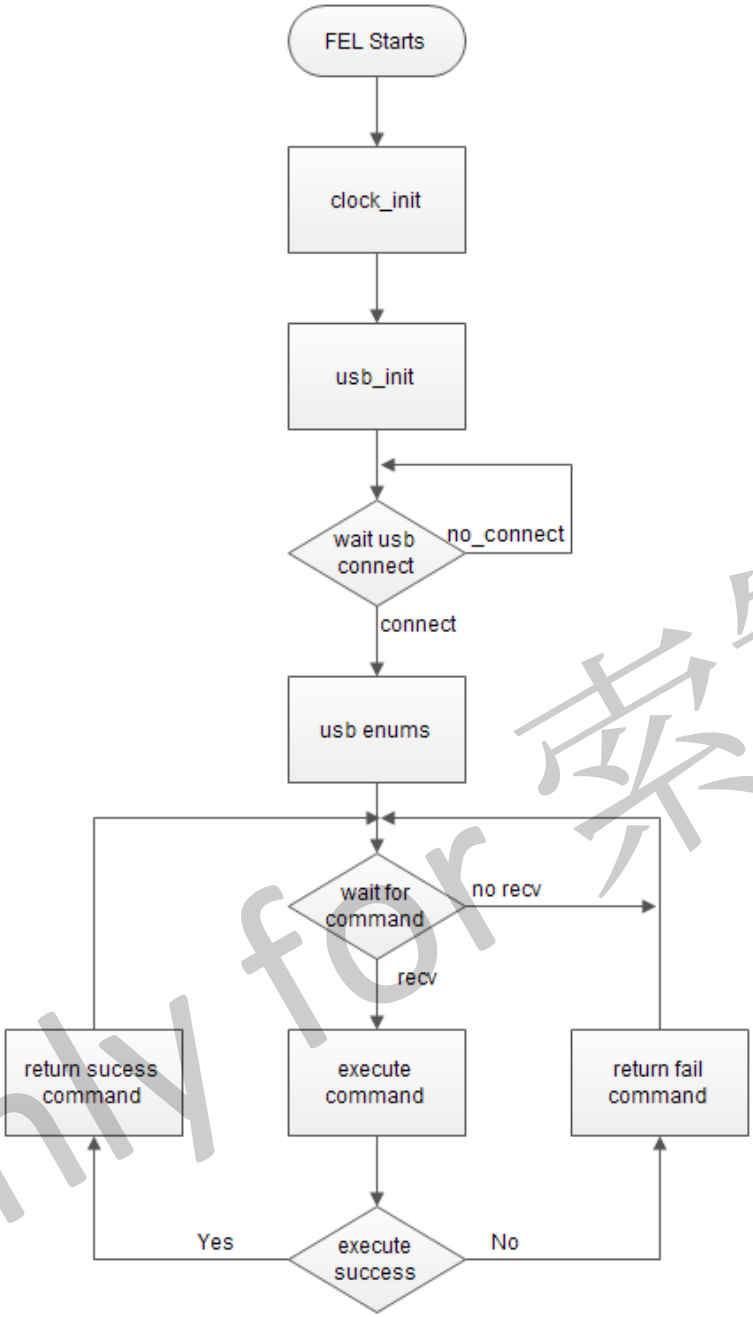

Figure 3- 10. USB FEL Process

3.4.2.3.4. UART Upgrade Process

When the system chooses to enter Mandatory Upgrade Process, if the boot_select2 pin signal is detected pulling low, then the system will jump to the UART Upgrade Process.

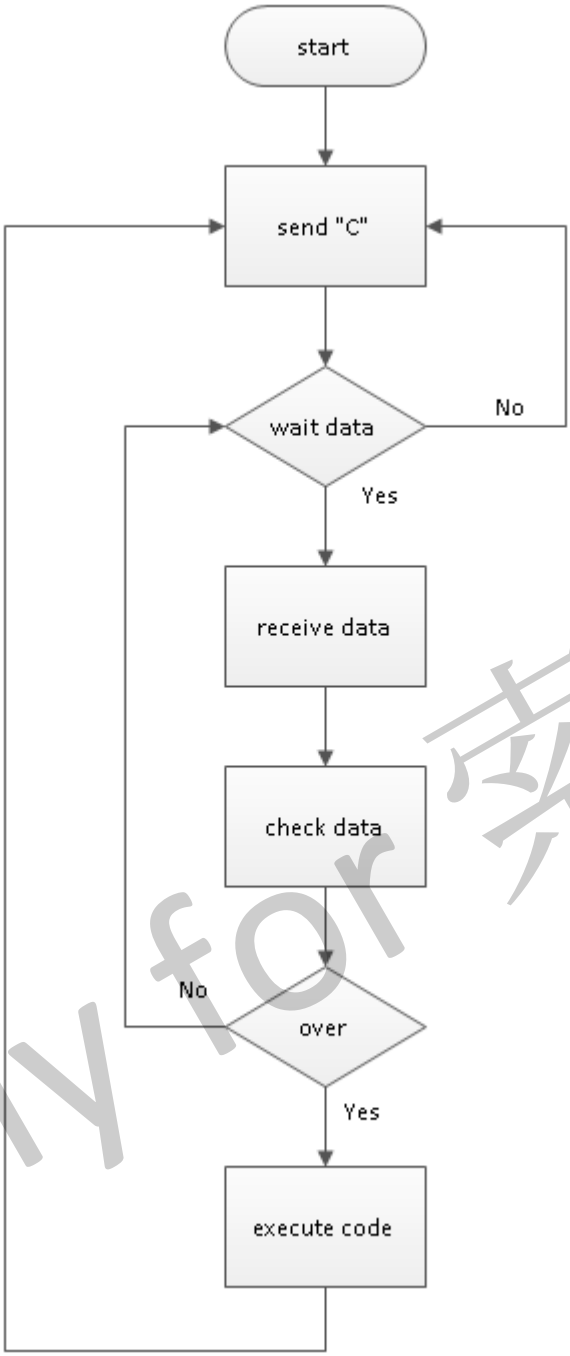

Figure 3- 11. UART Boot Process Diagram

3.4.2.3.5. Try Media Boot Process

When the system chooses to whether enter mandatory upgrade process, if the FEL pin signal is detected pulling high, then the system will jump to the try media boot process.

Try Media Boot Process will read the state of BOOT_MODE register, the state of BOOT_MODE decides whether to boot from GPIO pin or efuse. Figure 3-12 shows GPIO pin boot select process. Figure 3-13 shows efuse boot select process.

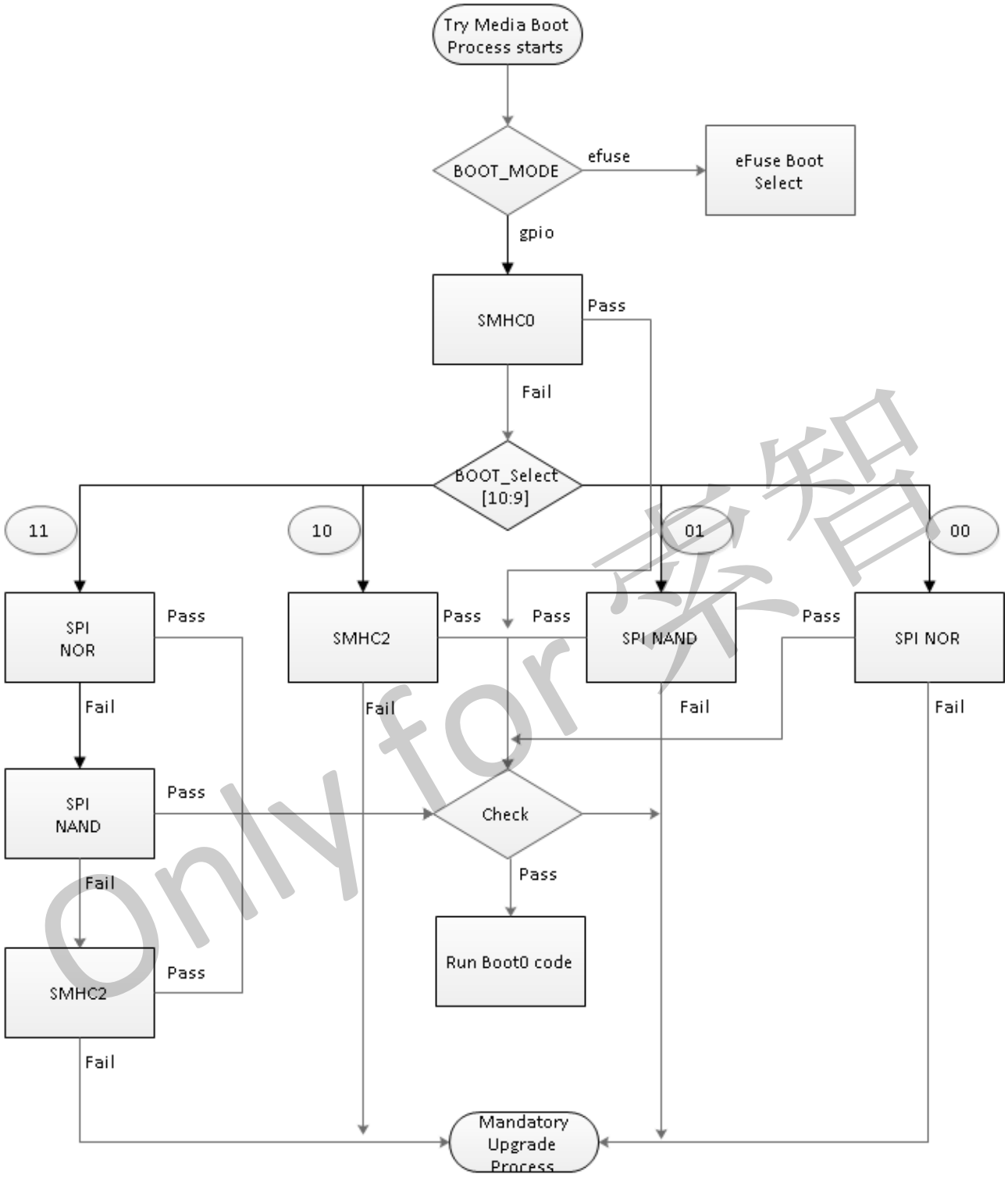

Figure 3- 12. GPIO Pin Boot Select Process

NOTE

SMHC0 usually is external SD / TF Card.

SMHC2 usually is external eMMC.

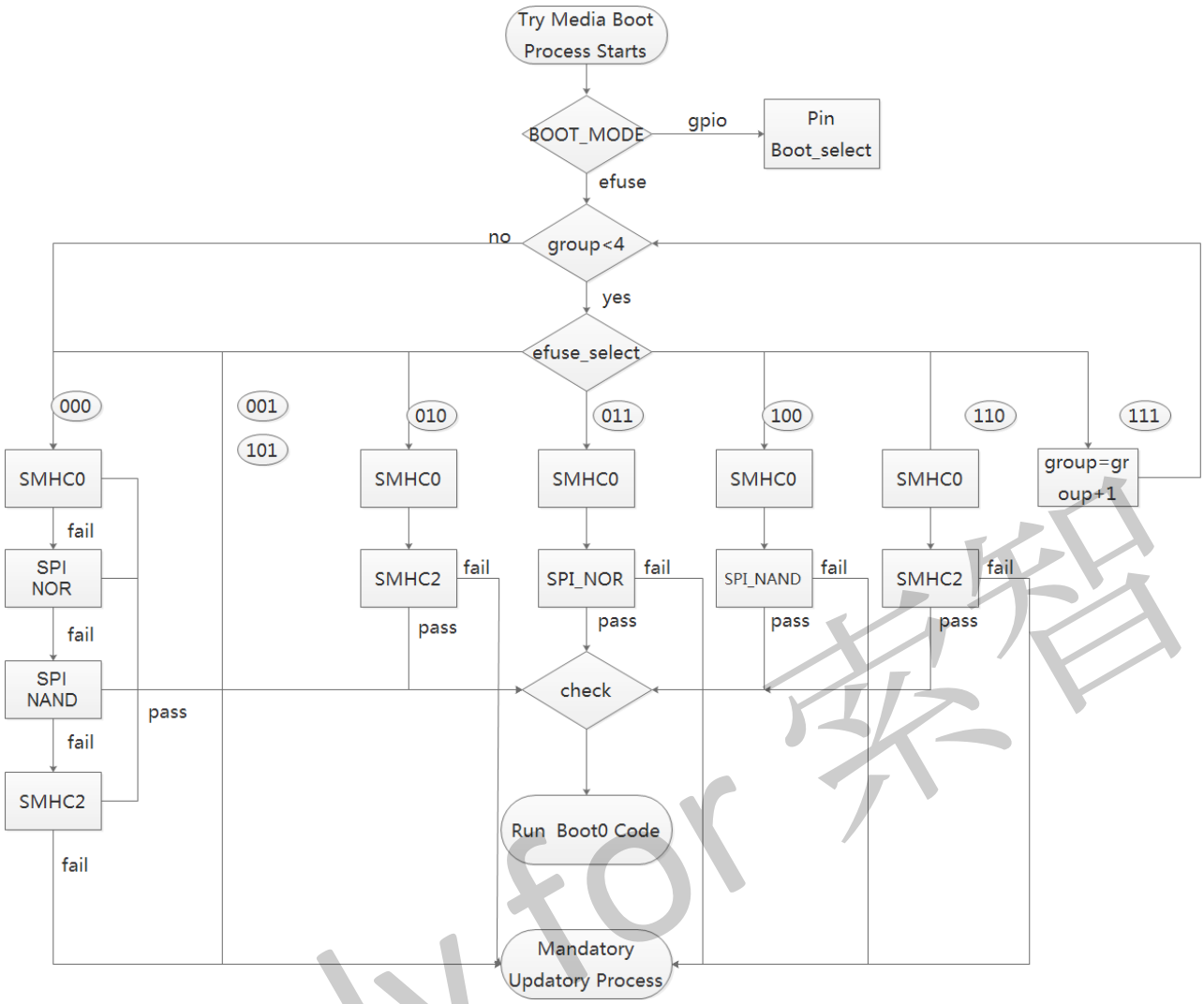

Figure 3- 13. eFuse Boot Select Process

3.5. System Configuration

3.5.1. Overview

The system configuration module is used to configure parameter for system domain, such as SRAM, CPU, PLL, BROM, and so on.

The address range of SRAM is as follows.

Area	Address	Size
SRAM A1	0x0002 0000---0x0003 7FFF	96K(supports Byte operation, the clock source is AHB1)
SRAM C	0x0003 8000---0x0005 8FFF	132KB(Borrows 132KB from VE, supports Byte operation, the clock source can be switched to AHB1)

3.6. Timer

3.6.1. Overview

The timer module implements the timing and counting functions. The timer module includes timer0, timer1, watchdog and AVS.

The timer0 and timer1 are completely consistent. The timer0/1 has the following features:

- Configurable count clock: LOSC and OSC24M. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transmit a reset signal to reset the entire system after an exception occurs in the system. The watchdog has the following features:

- Single clock source: OSC24M/750
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

The AVS is used to the synchronization of audio and video. The AVS module includes AVS0 and AVS1, the AVS0 and AVS1 are completely consistent. The AVS has the following features:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Initial value can be updated anytime
- 12-bit frequency divider factor
- Pause/Start function

3.6.2. Block Diagram

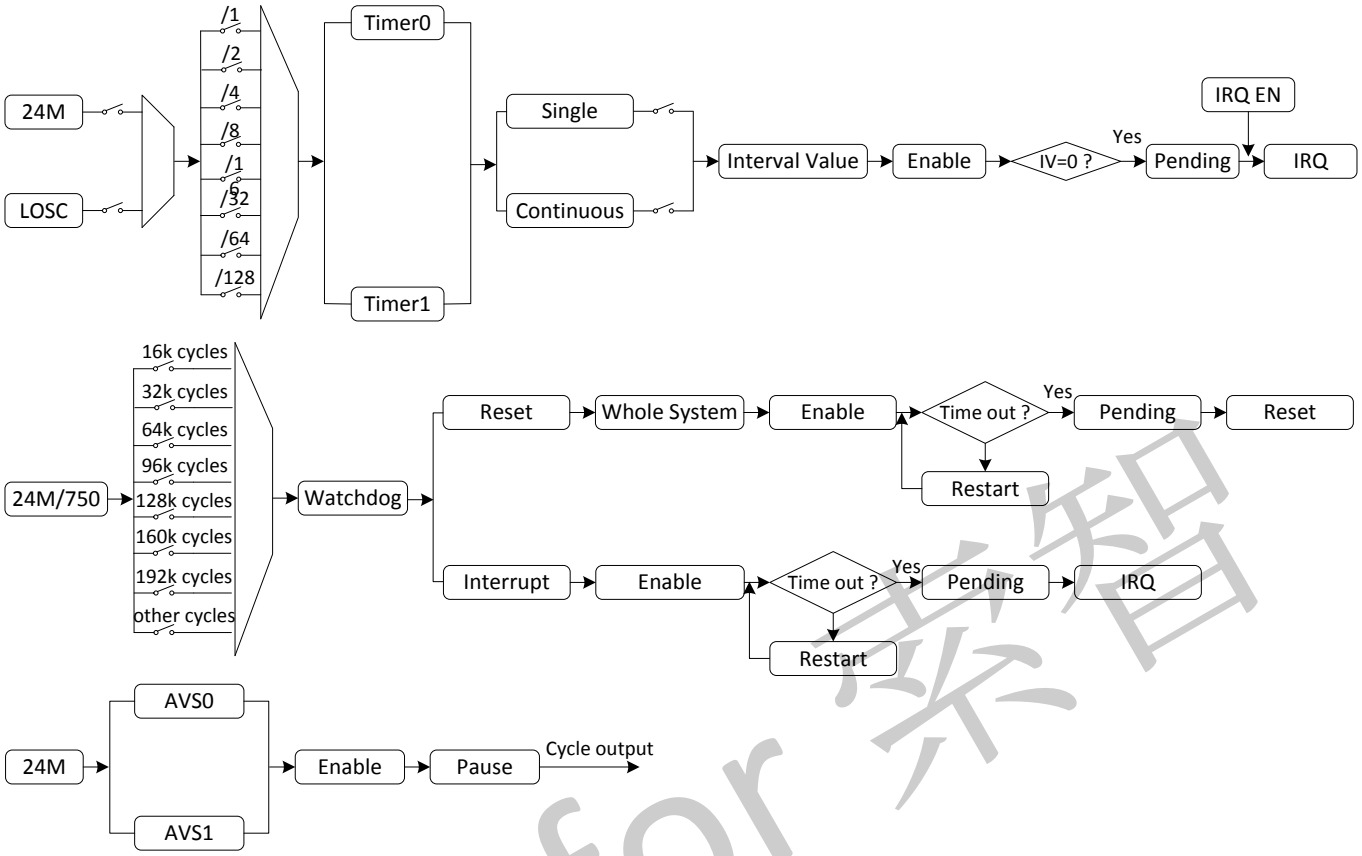

Figure 3- 14. Timer Block Diagram

3.6.3. Operations and Functional Descriptions

3.6.3.1. Timer Formula

Using Timer0 as an example.

$$T_{timer0} = \frac{TMR0\_INTV\_VALUE\_REG - TMR0\_CUR\_VALUE\_REG}{TMR0\_CLK\_SRC} \times TMR0\_CLK\_PRES$$

TMR0_INTV_VALUE_REG: timer initial value;
TMR0_CUR_VALUE_REG: timer current counter;
TMR0_CLK_SRC: timer clock source;
TMR0_CLK_PRES: timer clock prescale ratio.

3.6.3.2. Typical Application

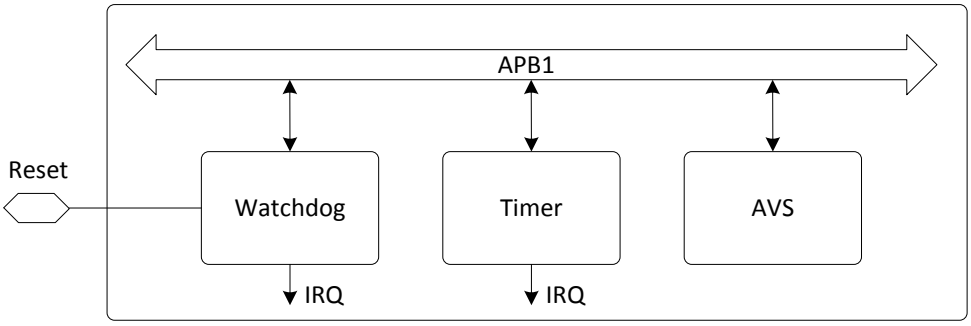

Figure 3- 15. Timer Application Diagram

Timer, watchdog and AVS configure register by APB1 bus.
Timer and watchdog have interrupt mode.
The system configures the time of watchdog, if the system has no timing for restart watchdog(such as bus hang dead), then watchdog sends out watchdog reset external signal to reset system; meanwhile watchdog outputs signal to RESET pad to reset PMIC.

3.6.3.3. Function Implemention

3.6.3.3.1. Timer

The timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each timer has independent interrupt.

The timer has two operating modes.

- **Continuous mode**

The bit7 of the TMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the timer module reloads data from TMRn_INTV_VALUE_REG then continues to count.

- **Single mode**

The bit7 of the TMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the timer stops counting. The timer starts to count again only when a new initial value is loaded.

Each timer has a prescaler that divides the working clock frequency of each timer by 1,2,4,8,16,32,64,128.

3.6.3.3.2. Watchdog

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The watchdog has three operating modes.

- **Interrupt mode**

The WDOG0_CFG_REG is set to 0x2, when the counter value reaches 0 and WDOG0_IRQ_EN_REG is enabled, the watchdog generates an interrupt, the watchdog enters into interrupt mode.

- **Reset mode**

The WDOG0_CFG_REG is set to 0x1, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.

The clock source of the watchdog is OSC24M/750. There are 12 configurable initial count values.
The watchdog can restart to count by setting the WDOG0_CTRL_REG: write 0xA57 to bit[12:1], then write 1 to bit[0].

- **Soft Reset mode**

Configure WDOG_SOFT_RST_REG to 0x16AA0001 to reset the system.

CAUTION

In soft reset mode, the watchdog should be off.

3.6.3.3.3. AVS

The AVS is a 33-bit up counter. The counter value is increased by 1 on each rising edge of the count clock.
The AVS can be operated after its clock gating in CCU module is opened.
The AVS has an OSC24M clock source and a 12-bit division factor(N1 or N2). When the timer increases to N1 or N2 from 0, AVS counter adds 1; when the counter reaches 33-bit upper limit, the AVS will start to count from initial value again.
In counter working process, the division factor and initial counter of the AVS can be changed anytime. And the AVS can stop or start to operate counter anytime.

3.6.3.4. Operating Mode

3.6.3.4.1. Timer Initial

(1) Configure the timer parameters: clock source, prescale factor, working mode. The configurations of these parameters have no sequence, and can be implemented by writing **TMRn_CTRL_REG**.
(2) Write the initial value: write **TMRn_INTV_VALUE_REG** to provide an initial value for the timer; write the bit[1] of **TMRn_CTRL_REG** to load the initial value to the timer, if the bit[1] is 1, writing operation cannot perform; if is 0, this indicates successful loading.
(3) Enable timer: write the bit[0] of **TMRn_CTRL_REG** to enable timer count; read **TMRn_CUR_VALUE_REG** to get the current count value.

3.6.3.4.2. Timer Interrupt

(1) Enable interrupt: write corresponding interrupt enable bit of **TMR_IRQ_EN_REG**, when timer counter time reaches, the corresponding interrupt generates.
(2) After enter interrupt process, write **TMR_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.3. Watchdog Initial

(1) Write **WDOG0_CFG_REG** to configure the generation of the interrupts and the output of reset signal.
(2) Write **WDOG0_MODE_REG** to configure the initial count value.
(3) Write **WDOG0_MODE_REG** to enable the watchdog.

3.6.3.4.4. Watchdog Interrupt

Watchdog interrupt is only used for the counter.
(1) Write **WDOG0_IRQ_EN_REG** to enable the interrupt.
(2) After enter the interrupt process, write **WDOG0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(3) Resume the interrupt and continue to execute the interrupted process.

3.6.3.4.5. AVS Start/Pause

(1) Write **AVS_CNT_DIV_REG** to configure the division factor.
(2) Write **AVS_CNT_REG** to configure the initial count value.
(3) Write **AVS_CNT_CTL_REG** to enable AVS counter. AVS counter can be paused at any time.

3.6.4. Programming Guidelines

3.6.4.1. Timer

Take making a 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR_0_INTV);                  //Set interval value
writel(0x94, TMR_0_CTRL);                   //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);  //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);            //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);  //Enable Timer0
```


3.6.4.2. Watchdog Reset

In the following instance making configurations for Watchdog: configure clock source as 24M/750, configure Interval Value as 1s and configure Watchdog Configuration as To whole system. This instance indicates that reset system after 1s.

```
writel(0x1, WDOG_CONFIG);                          //To whole system
writel(0x10, WDOG_MODE);                           //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);        //Enable Watchdog
```

3.6.4.3. Watchdog Restart

In the following instance making configurations for Watchdog: configure clock source as 24M/750, configure Interval Value as 1s and configure Watchdog Configuration as To whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(0x1, WDOG_CONFIG);                          //To whole system
writel(0x10, WDOG_MODE);                           //Interval Value set 1s
writel(readl(WDOG_MODE)|(1<<0), WDOG_MODE);        //Enable Watchdog
----other codes---
writel(readl(WDOG_CTRL)|(0xA57<<1)|(1<<0), WDOG_CTRL); //Writel 0xA57 at Key Field and Restart Watchdog
```

3.6.5. Register List

Module Name	Base Address
Timer	0x03009000

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
WDOG_IRQ_EN_REG	0x00A0	Watchdog IRQ Enable Register
WDOG_IRQ_STA_REG	0x00A4	Watchdog Status Register
WDOG_SOFT_RST_REG	0x00A8	Watchdog Software Reset Register
WDOG_CTRL_REG	0x00B0	Watchdog Control Register
WDOG_CFG_REG	0x00B4	Watchdog Configuration Register

WDOG_MODE_REG	0x00B8	Watchdog Mode Register
WDOG_OUTPUT_CFG_REG	0x00BC	Watchdog Output Configuration Register
AVS_CNT_CTL_REG	0x00C0	AVS Control Register
AVS_CNT0_REG	0x00C4	AVS Counter 0 Register
AVS_CNT1_REG	0x00C8	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x00CC	AVS Divisor Register

3.6.6. Register Description

3.6.6.1. 0x0000 Timer IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	TMR1_IRQ_EN Timer 1 Interrupt Enable 0: No effect 1: Timer 1 Interval Value reached interrupt enable
0	R/W1S	0x0	TMR0_IRQ_EN Timer 0 Interrupt Enable 0: No effect 1: Timer 0 Interval Value reached interrupt enable

3.6.6.2. 0x0004 Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	TMR1_IRQ_PEND Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached
0	R/W1C	0x0	TMR0_IRQ_PEND Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached

3.6.6.3. 0x0010 Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:8	/	/	/
7	R/W	0x0	TMR0_MODE Timer 0 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC 00:LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR0_RELOAD Timer 0 Reload 0: No effect 1: Reload timer 0 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR0_EN Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.4. 0x0014 Timer 0 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0014	Register Name: TMR0_INTV_VALUE_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_INTV_VALUE Timer 0 Interval Value

NOTE

The value setting should consider the system clock and the timer clock source.

3.6.6.5. 0x0018 Timer 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR0_CUR_VALUE Timer 0 Current Value Timer 0 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.6. 0x0020 Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TMR1_MODE Timer 1 mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES Select the pre-scale of timer 1 clock source 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC 00: LOSC 01: OSC24M 10: / 11: /
1	R/W	0x0	TMR1_RELOAD Timer 1 Reload

			0: No effect 1: Reload timer 1 Interval value After the bit is set, it can not be written again before it is cleared automatically.
0	R/W	0x0	TMR1_EN Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.6.6.7. 0x0024 Timer 1 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE Timer 1 Interval Value

NOTE

The value should consider the system clock and the timer clock source.

3.6.6.8. 0x0028 Timer 1 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name:TMR1_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_CUR_VALUE Timer 1 Current Value Timer 1 current value is a 32-bit down-counter (from interval value to 0).

3.6.6.9. 0x00A0 Watchdog IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name:WDOG_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1S	0x0	WDOG_IRQ_EN Watchdog Interrupt Enable

			0: No effect 1: Watchdog interrupt enable

3.6.6.10. 0x00A4 Watchdog Status Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name:WDOG_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	WDOG_IRQ _PEND Watchdog IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending. Watchdog interval value is reached.

3.6.6.11. 0x00A8 Watchdog Software Reset Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name:WDOG_SOFT_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15:1	/	/	/
0	R/W1C	0x0	Soft Reset Enable 0: De-assert 1: Reset System **Note: When using the bit to reset system, the watchdog should be off.**

3.6.6.12. 0x00B0 Watchdog Control Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name:WDOG_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD Watchdog Key Field It should be written to 0xA57. Writing any other value in this field aborts the write operation.
0	R/W1S	0x0	WDOG_RESTART Watchdog Restart 0: No effect 1: Restart the Watchdog

3.6.6.13. 0x00B4 Watchdog Configuration Register (Default Value: 0x0000_0001)

Offset: 0x00B4			Register Name:WDOG_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	WDOG_CONFIG 00: / 01: To whole system 10: Only interrupt 11: /

3.6.6.14. 0x00B8 Watchdog Mode Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name:WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	WDOG_INTV_VALUE Watchdog Interval Value Watchdog clock source is OSC24M/750. If the clock source is turned off, Watchdog will not work. 0000: 16000 cycles (0.5s) 0001: 32000 cycles (1s) 0010: 64000 cycles (2s) 0011: 96000 cycles (3s) 0100: 128000 cycles (4s) 0101: 160000 cycles (5s) 0110: 192000 cycles (6s) 0111: 256000 cycles (8s) 1000: 320000 cycles (10s) 1001: 384000 cycles (12s) 1010: 448000 cycles (14s) 1011: 512000 cycles (16s) Others: Reserved
3:1	/	/	/
0	R/W1S	0x0	WDOG_EN Watchdog Enable 0: No effect 1: Enable the Watchdog

3.6.6.15. 0x00BC Watchdog Output Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name:WDOG_OUTPUT_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:12	/	/	/
11:0	R/W	0x1F	Wdog output configuration Wdog rst valid time config T=1/32ms*(N+1) Default 1ms

3.6.6.16. 0x00C0 AVS Counter Control Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: AVS_CNT_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/Disable The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 0 Enable/Disable The counter source is OSC24M. 0: Disable 1: Enable

3.6.6.17. 0x00C4 AVS Counter 0 Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: AVS_CNT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter will not increase.

3.6.6.18. 0x00C8 AVS Counter 1 Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name:AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/Video Sync Application The high 32 bits of the internal 33-bit counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter will not increase.

3.6.6.19. 0x00CC AVS Counter Divisor Register (Default Value: 0x05DB_05DB)

Offset: 0x00CC			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter 1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit [27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter 0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit [11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. It can be configured by software at any time.

3.7. High Speed Timer

3.7.1. Overview

The high speed timer(HSTimer) module implements more precise timing and counting functions.

The HSTimer has the following features:

- Timing clock is AHB1 that can provides more precise timing clock
- Configurable 5 prescale factor
- Configurable 56-bit down timer
- Supports 2 working modes: continuous mode and single mode
- Supports test mode
- Generates an interrupt when the count is decreased to 0

3.7.2. Block Diagram

Figure 3-16 shows a block diagram of the HSTimer.

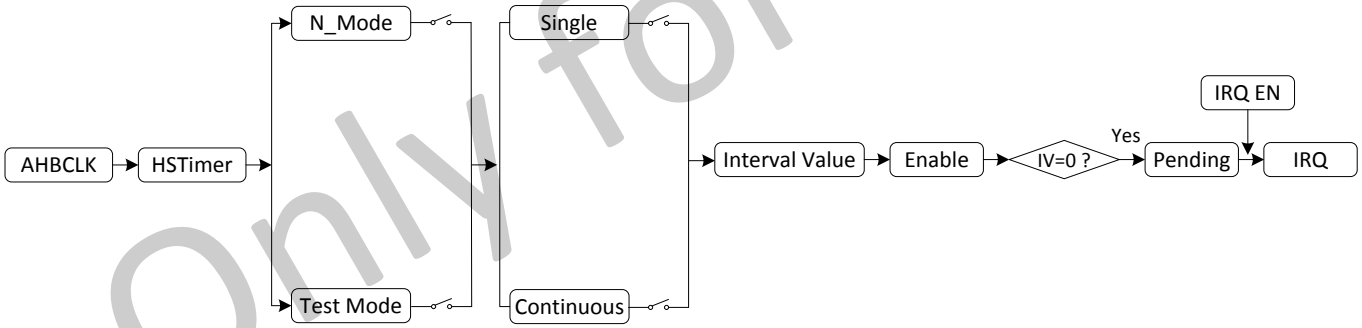

Figure 3- 16. HSTimer Block Diagram

3.7.3. Operations and Functional Descriptions

3.7.3.1. HSTimer Formula

$$\frac{(HS\_TMR\_INTV\_HI\_REG<<32 + HS\_TMR\_INTV\_LO\_REG) - (HS\_TMR\_CURNT\_HI\_REG<<32 + HS\_TMR\_CURNT\_LO\_REG)}{AHB1CLK} \times HS\_TMR\_CLK$$

HS_TMR_INTV_HI_REG: Initial of Counter Higher Bit
HS_TMR_INTV_LO_REG: Initial of Counter Lower Bit
HS_TMR_CURNT_HI_REG: Current Value of Counter Higher Bit
HS_TMR_CURNT_LO_REG: Current Value of Counter Lower Bit

AHB1CLK: AHB1 Clock Frequency
HS_TMR_CLK: Time Prescale Ratio of Counter

3.7.3.2. Typical Application

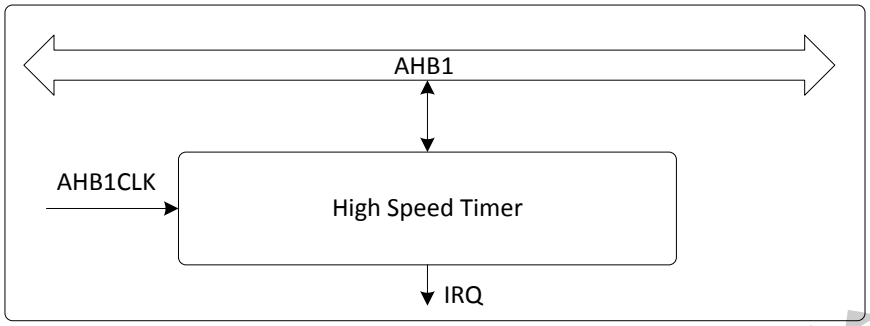

Figure 3- 17. HSTimer Application Diagram

The high speed timer is on AHB1, and the high speed timer controls registers by AHB1.
The high speed timer has single clock source: AHB. The high speed timer can generate interrupt.

3.7.3.3. Function Implemention

The high speed timer is a 56-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The high speed timer has two timing modes.

- Continuous mode: The bit7 of **HS_TMR0_CTRL_REG** is set to the continuous mode, when the count value is decreased to 0, the high speed timer module reloads data from **HS_TMR_INTV_LO_REG** and **HS_TMR_INTV_HI_REG,** then continues to count.
- Single mode: The bit7 of **HS_TMR0_CTRL_REG** is set to the single mode, when the count value is decreased to 0, the high speed timer stops counting. The high speed timer starts to count again only when a new initial value is loaded.

The high speed timer has two operating modes.

- Normal mode: When the bit31 of **HS_TMR0_CTRL_REG** is set to the normal mode, the high speed timer is used as 56-bit down counter, which can finish continuous timing and single timing.
- Test mode: When the bit31 of **HS_TMR0_CTRL_REG** is set to the test mode, then **HS_TMR_INTV_LO_REG** must be set to 0x1, the high speed timer is used as 24-bit down counter, and **HS_TMR_INTV_HI_REG** is the initial value of the high speed timer.

Each high speed timer has a prescaler that divides the working clock frequency of each working timer by 1,2,4,8,16.

3.7.3.4. Operating Mode

3.7.3.4.1. HSTimer Initial

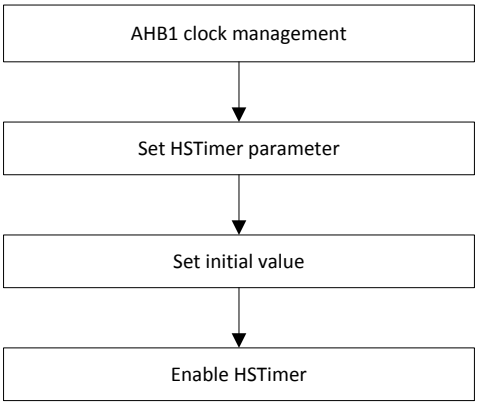

Figure 3- 18. HSTimer Initialization Process

(1) AHB1 clock management: Open the clock gating of AHB1 and de-assert the soft reset of AHB1 in CCU.
(2) Configure the corresponding parameters of the high speed timer: clock source, prescaler factor, working mode, counting mode. These parameters that are written to **HS_TMR0_CTRL_REG** have no sequences.
(3) Write the initial value: Firstly write the low-bit register **HS_TMR_INTV_LO_REG**, then write the high-bit register **HS_TMR_INTV_HI_REG**. Write the bit1 of **HS_TMR0_CTRL_REG** to load the initial value. If in timing stop stage of high speed timer, write the bit1 and bit0 of **HS_TMR0_CTRL_REG** to reload the initial value.
(4) Enable high speed timer: Write the bit[0] of **HS_TMR0_CTRL_REG** to enable high speed timer to count.
(5) Reading **HS_TMR_CURNT_LO_REG** and **HS_TMR_CURNT_HI_REG** can get current counting value.

3.7.3.4.2. HSTimer Interrupt

(1) Enable interrupt: Write the corresponding interrupt enable bit of **HS_TMR_IRQ_EN_REG**, when the counting time of high speed timer reaches, the corresponding interrupt generates.
(2) After enter the interrupt process, write **HS_TMR_IRQ_STAS_REG** to clear the interrupt pending.
(3) Resume the interrupt and continue to execute the interrupted process.

3.7.4. Programming Guidelines

Take making a 1us delay using HSTimer0 for an instance as follows, AHB1CLK will be configured as 100MHz and n_mode,single mode and 2 pre-scale will be selected in this instance.

```
writel(0x32, HS_TMR0_INTV_LO);                    //Set interval value Lo 0x32
writel(0x0, HS_TMR0_INTV_HI);                     //Set interval value Hi 0x0
writel(0x90, HS_TMR0_CTRL);                       //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL); //Set Reload bit
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL); //Enable HSTimer0
```



```
while(!(readl(HS_TMR_IRQ_STAS)&1));          //Wait for HSTimer0 to generate pending
writel(1,HS_TMR_IRQ_STAS);                    //Clear HSTimer0 pending
```

3.7.5. Register List

Module Name	Base Address
High Speed Timer	0x03005000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HS Timer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HS Timer Status Register
HS_TMR0_CTRL_REG	0x0020	HS Timer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0024	HS Timer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0028	HS Timer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x002C	HS Timer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0030	HS Timer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0040	HS Timer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0044	HS Timer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0048	HS Timer 1 Interval Value High Register
HS_TMR1_CURNT_LO_REG	0x004C	HS Timer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0050	HS Timer 1 Current Value High Register

3.7.6. Register Description

3.7.6.1. 0x0000 HS Timer IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1S	0x0	HS_TMR1_INT_EN High Speed Timer 1 Interrupt Enable 0: No effect 1: High Speed Timer1 interval value reached interrupt enable
0	R/W1S	0x0	HS_TMR0_INT_EN High Speed Timer 0 Interrupt Enable 0: No effect 1: High Speed Timer0 interval value reached interrupt enable

3.7.6.2. 0x0004 HS Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	HS_TMR1_IRQ_PEND High Speed Timer 1 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 1 interval value is reached.
0	R/W1C	0x0	HS_TMR0_IRQ_PEND High Speed Timer 0 IRQ Pending Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 0 interval value is reached.

3.7.6.3. 0x0020 HS Timer 0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST High Speed Timer 0 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE High Speed Timer 0 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

1	R/W1S	0x0	HS_TMR0_RELOAD High Speed Timer 0 Reload 0: No effect 1: Reload High Speed Timer 0 Interval Value
0	R/W	0x0	HS_TMR0_EN High Speed Timer 0 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.4. 0x0024 HS Timer 0 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: HS_TMR0_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO High Speed Timer 0 Interval Value [31:0]

3.7.6.5. 0x0028 HS Timer 0 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: HS_TMR0_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI High Speed Timer 0 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.7.6.6. 0x002C HS Timer 0 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO

			High Speed Timer 0 Current Value [31:0]

3.7.6.7. 0x0030 HS Timer 0 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI High Speed Timer 0 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

3.7.6.8. 0x0040 HS Timer 1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR1_TEST High Speed Timer 1 Test Mode In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode
30:8	/	/	/
7	R/W	0x0	HS_TMR1_MODE High Speed Timer 1 Mode 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/

1	R/W1S	0x0	HS_TMR1_RELOAD High Speed Timer 1 Reload 0: No effect 1: Reload High Speed Timer 1 Interval Value
0	R/W	0x0	HS_TMR1_EN High Speed Timer 1 Enable 0: Stop/Pause 1: Start If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.6.9. 0x0044 HS Timer 1 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO High Speed Timer 1 Interval Value [31:0]

3.7.6.10. 0x0048 HS Timer 1 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: HS_TMR1_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI High Speed Timer 1 Interval Value [55:32]

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written first. And the High register should be written after the Lo register.

3.7.6.11. 0x004C HS Timer 1 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO

			High Speed Timer 1 Current Value [31:0]

3.7.6.12. 0x0050 HS Timer 1 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI High Speed Timer 1 Current Value [55:32]

NOTE

HS timer current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

3.8. GIC

3.8.1. Interrupt Source

Interrupt Number	Interrupt Source	Interrupt Vector	Description
0	SGI 0	0x0000	SGI 0 interrupt
1	SGI 1	0x0004	SGI 1 interrupt
2	SGI 2	0x0008	SGI 2 interrupt
3	SGI 3	0x000C	SGI 3 interrupt
4	SGI 4	0x0010	SGI 4 interrupt
5	SGI 5	0x0014	SGI 5 interrupt
6	SGI 6	0x0018	SGI 6 interrupt
7	SGI 7	0x001C	SGI 7 interrupt
8	SGI 8	0x0020	SGI 8 interrupt
9	SGI 9	0x0024	SGI 9 interrupt
10	SGI 10	0x0028	SGI 10 interrupt
11	SGI 11	0x002C	SGI 11 interrupt
12	SGI 12	0x0030	SGI 12 interrupt
13	SGI 13	0x0034	SGI 13 interrupt
14	SGI 14	0x0038	SGI 14 interrupt
15	SGI 15	0x003C	SGI 15 interrupt
16	PPI 0	0x0040	PPI 0 interrupt
17	PPI 1	0x0044	PPI 1 interrupt
18	PPI 2	0x0048	PPI 2 interrupt
19	PPI 3	0x004C	PPI 3 interrupt
20	PPI 4	0x0050	PPI 4 interrupt
21	PPI 5	0x0054	PPI 5 interrupt
22	PPI 6	0x0058	PPI 6 interrupt
23	PPI 7	0x005C	PPI 7 interrupt
24	PPI 8	0x0060	PPI 8 interrupt
25	PPI 9	0x0064	PPI 9 interrupt
26	PPI 10	0x0068	PPI 10 interrupt
27	PPI 11	0x006C	PPI 11 interrupt
28	PPI 12	0x0070	PPI 12 interrupt
29	PPI 13	0x0074	PPI 13 interrupt
30	PPI 14	0x0078	PPI 14 interrupt
31	PPI 15	0x007C	PPI 15 interrupt
32	GPADC	0x0080	GPADC interrupt
33	THS	0x0084	Thermal sensor interrupt
34~40	/	/	/
41	DRAM	0x00A4	DRAM interrupt

Interrupt Number	Interrupt Source	Interrupt Vector	Description
42	DMA	0x00A8	DMA interrupt
43~45	/	/	/
46	WDOG	0x00B8	Watchdog interrupt
47	PWM	0x00BC	PWM interrupt
48	/	/	/
49	BUS_TIMEOUT	0x00C4	Bus Timeout interrupt
50	SMC	0x00C8	SMC interrupt
51	PSI	0x00CC	PSI interrupt
52	NPU	0x00D0	NPU Interrupt
53	G2D	0x00D4	G2D interrupt
54~56	/	/	/
57	VE	0x00E4	VE interrupt
58	EISE	0x00E8	EISE Interrupt
59	EMAC0	0x00EC	EMAC0 interrupt
60	Audio Codec	0x00F0	Audio Codec interrupt
61~62	/	/	/
63	DE	0x00FC	DE interrupt
64	/	/	/
65	ISP0	0x0104	ISP0 interrupt
66	/	/	/
67	CE_NS	0x010C	CE_NS interrupt
68	CE_S	0x0110	CE_S interrupt
69	I2S/PCM0	0x0114	I2S/PCM0 interrupt
70	I2S/PCM1	0x0118	I2S/PCM1 interrupt
71~72	/	/	/
73	TWI0	0x0124	TWI0 interrupt
74	TWI1	0x0128	TWI1 interrupt
75	TWI2	0x012C	TWI2 interrupt
76	TWI3	0x0130	TWI3 Interrupt
77	MIPI_DSI0	0x0134	MIPI_DSI0 interrupt
78	SMHC0	0x0138	SMHC0 interrupt
79	SMHC1	0x013C	SMHC1 interrupt
80	SMHC2	0x0140	SMHC2 interrupt
81	UART0	0x0144	UART0 interrupt
82	UART1	0x0148	UART1 interrupt
83	UART2	0x014C	UART2 interrupt
84	UART3	0x0150	UART3 interrupt
85	/	/	/
86	SPI0	0x0158	SPI0 interrupt
87	SPI1	0x015C	SPI1 interrupt
88	SPI2	0x0160	SPI2 interrupt
89	/	/	/

Interrupt Number	Interrupt Source	Interrupt Vector	Description
90	HSTIMER0	0x0168	High speed timer0 interrupt
91	HSTIMER1	0x016C	High speed timer1 interrupt
92	TIMER0	0x0170	Timer0 interrupt
93	TIMER1	0x0174	Timer1 interrupt
94	TCON_LCD0	0x0178	TCON_LCD0 interrupt
95	/	/	/
96	USB2.0_OTG_DEVICE	0x0180	USB2.0_OTG_DEVICE
97	USB2.0_OTG_EHCI	0x0184	USB2.0_OTG_EHCI interrupt
98	USB2.0_OTG_OHCI	0x0188	USB2.0_OTG_OHCI interrupt
99	GPIOC	0x018C	GPIOC interrupt
100	GPIOD	0x0190	GPIOD interrupt
101	GPIOE	0x0194	GPIOE interrupt
102	GPIOF	0x0198	GPIOF interrupt
103	GPIOG	0x019C	GPIOG interrupt
104	GPIOH	0x01A0	GPIOH interrupt
105	GPIOI	0x01A4	GPIOI interrupt
106	CSI_DMA0	0x01A8	CSI_DMA0 interrupt
107	CSI_DMA1	0x01AC	CSI_DMA1 interrupt
108	CSI_DMA2	0x01B0	CSI_DMA2 interrupt
109	CSI_DMA3	0x01B4	CSI_DMA3 interrupt
110	CSI_PARSER0	0x01B8	CSI_PARSER0 interrupt
111	CSI_PARSER1	0x01BC	CSI_PARSER1 interrupt
112	/	0x01C0	/
113	/	0x01C4	/
114	CSI_ MIPI0_RX	0x01C8	CSI_MIPI interrupt
115	/	0x01CC	/
116	/	0x01D0	/
117	/	0x01D4	/
118	/	0x01D8	/
119	/	0x01DC	/
120	/	0x01E0	/
121	/	0x01E4	/
122	/	0x01E8	/
123	/	0x01EC	/
124	CSI_TOP_PKT	0x01F0	CSI_TOP_PKT interrupt
125	DSPO	0x01F4	DSPO Interrupt
126	/	0x01F8	/
127	IOMMU	0x01FC	IOMMU interrupt
CPUS Domain			
136	External NMI	0x0220	External NMI interrupt
137	R_Alarm0	0x0224	R_Alarm0 interrupt
138	R_GPIOL	0x0228	R_GPIOL interrupt

Interrupt Number	Interrupt Source	Interrupt Vector	Description
139	R_TWI0	0x022C	R_TWI0 interrupt
142	R_RSB	0x0238	R_RSB interrupt
146	R_OWC	0x0248	One wire interface interrupt
CPUX Related			
160	C0_CTI0	0x0280	C0_CTI0 interrupt
164	C0_COMMTX0	0x0290	C0_COMMTX0 interrupt
168	C0_COMMRX0	0x02A0	C0_COMMRX0 interrupt
172	C0_PMU0	0x02B0	C0_PMU0 interrupt
176	C0_AXI_ERROR	0x02C0	C0_AXI_ERROR interrupt
178	AXI_WR_IRQ	0x02C8	C0_AXI_WR interrupt
179	AXI_RD_IRQ	0x02CC	C0_AXI_RD interrupt

For complete GIC information, refer to the ***GIC PL400 technical reference manual*** and ***ARM GIC Architecture Specification V2.0***.

3.9. DMA

3.9.1. Overview

The direction memory access (DMA) is used to transfer data between a peripheral and a memory, between peripherals, or between memories. DMA is a high-speed data transfer operation that reduces the CPU resources.

The DMA has the following features:

- 8 channels DMA
- Provides 50 peripheral DMA requests for data read and 50 peripheral DMA requests for data write
- Transfer with linked list
- Programmable 8-,16-,32-,64-bit data width
- Programmable DMA burst length
- DRQ response includes wait mode and handshake mode
- Memory devices support non-aligned transform
- DMA channel supports pause function

3.9.2. Block Diagram

The following figure shows a block diagram of DMA.

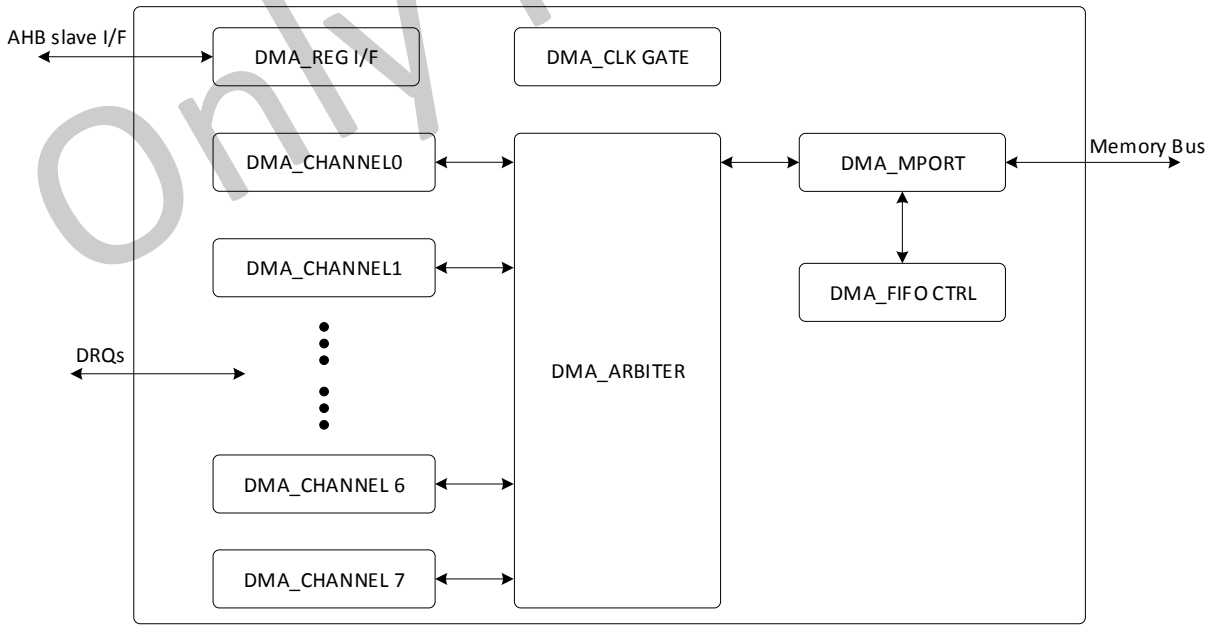

Figure 3- 19. DMA Block Diagram

DMA_ARBITER: Arbitrate DMA read/write requirement of each channel, and convert to read/write requirement of each port.

DMA_CHANNEL: DMA transform engine. Each channel is independent. The priorities of DMA channels uses polling mechanism. When the DMA requests from two peripherals are valid simultaneously, if DMA_ARBITER is non-idle, the

next channel of the current channel has the higher priority; if DMA_ARBITER is idle, the channel0 has the highest priority, whereas the channel 7 has the lowest priority.
DMA_MPORT: Receive read/write requirement of DMA_ARBITER , and convert to the corresponding MBUS access.
DMA_FIFOCTL: Internal FIFO cell control module.
DMA_REGIF: Common register module, mainly used to resolve AHB1 demand.
DMA_CLKGATE: Hardware auto clock gating control module.

DMA integrates 8 independent DMA channels. When DMA channel starts, DMA gets DMA descriptor by DMA_DESC_ADDR_REG to use for the configuration information of the current DMA package transfer, and DMA can transfer data between the specified peripherals through the configuration information. When a package transfer finished, DMA judges if the current channel transfer finished through the linked information in descriptor.

3.9.3. Operations and Functional Descriptions

3.9.3.1. Clock and Reset

DMA is on AHB1. The clock of AHB1 influences the transfer efficiency of DMA.

3.9.3.2. Typical Application

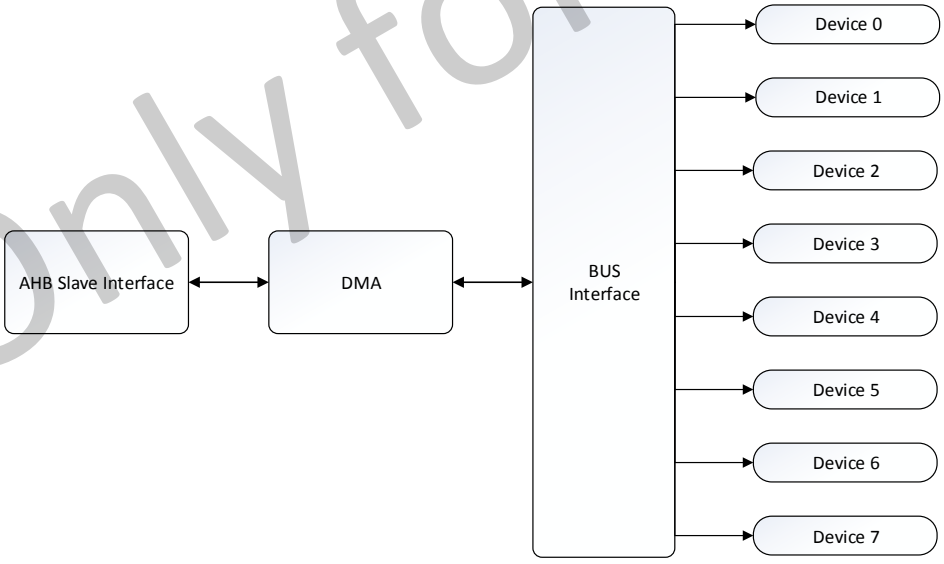

Figure 3- 20. DMA Typical Application Diagram

3.9.3.3. DRQ Type

Table 3- 10. DMA DRQ Table

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM

port1	DRAM	port1	DRAM
port2		port2	
port3	I2S/PCM0-RX	port3	I2S/PCM0-TX
port4	I2S/PCM1-RX	port4	I2S/PCM1-TX
port5		port5	
port6	Audio Codec	port6	Audio Codec
port7		port7	
port8		port8	
port9		port9	
port10		port10	
port11		port11	
port12	GPADC	port12	
port13		port13	
port14	UART0-RX	port14	UART0-TX
port15	UART1-RX	port15	UART1-TX
port16	UART2-RX	port16	UART2-TX
port17	UART3-RX	port17	UART3-TX
port18		port18	
port19		port19	
port20		port20	
port21		port21	
port22	SPI0-RX	port22	SPI0-TX
port23	SPI1-RX	port23	SPI1-TX
port24	SPI2-RX	port24	SPI2-TX
port25		port25	
port26		port26	
port27		port27	
port28		port28	
port29		port29	
Port30	OTG_EP1	Port30	OTG_EP1
Port31	OTG_EP2	Port31	OTG_EP2
Port32	OTG_EP3	Port32	OTG_EP3
Port33	OTG_EP4	Port33	OTG_EP4
Port34	OTG_EP5	Port34	OTG_EP5
Port35		Port35	
Port36		Port36	
Port37		Port37	
Port38		Port38	
Port39		Port39	
Port40		Port40	
Port41		Port41	
Port42		Port42	
Port43	TWI0	Port43	TWI0
Port44	TWI1	Port44	TWI1

Port45	TWI2	Port45	TWI2
Port46	TWI3	Port46	TWI3
Port47			
Port48	S-TWI0		S-TWI0
Port49			

3.9.3.4. DMA Descriptor

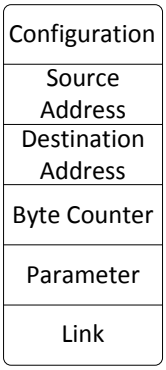

Figure 3- 21. DMA Descriptor

DMA descriptor is the configuration information of DMA transfer that decides the DMA working mode. Each descriptor includes 6 words, in turn, configuration, source address, destination address, byte counter, parameter, link.

(1) Configuration: Configure the following information by DMA_CFG_REG.

- **DRQ type of source and destination:** the DRQ signal of devices is as driving signal of DMA transfer.
- **Transferred address count mode**: IO mode indicates the address is fixed during transfer; linear mode indicates the address is increasing during transfer.
- **Transferred block length**: block length is the amount of DMA transferred data in one-shot valid DRQ. The block length supports 1-bit, 4-bit, 8-bit or 16-bit mode.
- **Transferred data width**: data width indicates the data width of every operation, and supports 8-bit, 16-bit, 32-bit or 64-bit mode.

(2) Source Address: Configure the transferred source address.

(3) Destination Address: Configure the transferred destination address.

DMA reads data from the source address, then writes data to the destination address.

(4) Byte counter: Configure the amount of a package. The maximum package is not more than (2^25-1) bytes. If the amount of the package reaches the maximum value, even if DRQ is valid, DMA should stop the current transfer.

(5) Parameter: Configure the interval between data block. The parameter is valid for non-memory peripherals. When DMA detects that DRQ is high level, DMA transfers block cycle. And during time, the changing of DRQ is ignored. After transferred, DMA waits the setting cycle(WAIT_CYC), then executes the next DRQ detection.

(6) Link: If the value of the link is 0xFFFFF800, the current package is at the end of the linked list. DMA will stop transfer after the package is transferred; if the value of the link is not 0xFFFFF800, the value of the link is considered the descriptor address of the next package.

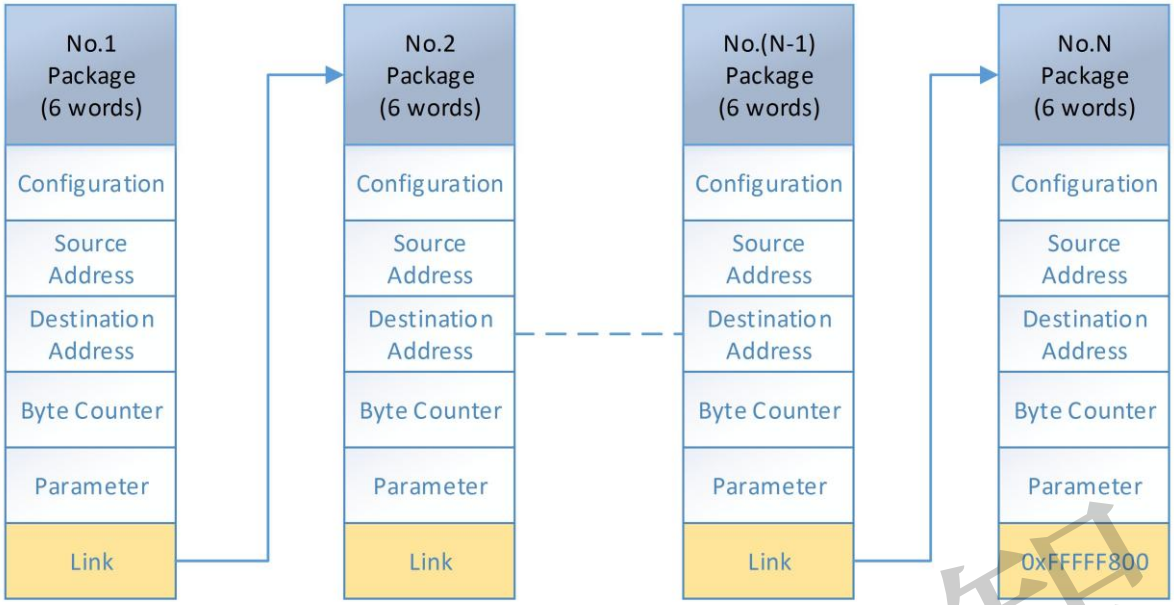

Figure 3- 22. DMA Chain Transfer

3.9.3.5. Interrupt

The half package interrupt is enabled, DMA sends half package interrupt after the half package transfer completes. The total package interrupt is enabled, DMA sends package end interrupt after the total package transfer completes. The total queue interrupt is enabled, DMA sends queue end interrupt after the total queue completes.
Notice that when CPU does not respond to the interrupts timely, or two DMA interrupts generate very closely, the later interrupt may override the former one. So For CPU, the DMA has only a system interrupt source.

3.9.3.6. Clock Gating

DMA CLK GATE module is the clock module of auto-controlled by hardware. DMA CLK GATE module is mainly used to generate the clock of DMA sub-module and the local circuit in module, including clock gating of channel and clock gating of public part.

The clock gating of the channel indicates DMA clock can auto-open when the system accesses the current DMA channel register and DMA channel is enabled. When DMA transfer is completed, DMA channel clock can auto-close after 16 HCLK delay, meanwhile the clock of the corresponding channel control and FIFO control will be closed.

The clock gating of the common part indicates the clock of the common circuit can auto-close when all DMA channels are opened. The common circuit includes the common circuit of FIFO control module, MPORT module and memory bus clock.

DMA clock gating can support all the functions stated above or not by software.

3.9.3.7. Transfer Mode

DMA supports two data transfer modes: wait mode and handshake mode.

(1) Wait Mode

When device request signal enters DMA, the device request signal is transformed into the internal DRQ signal through block and wait counter. The transformed principle is as follows.

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically.
- After the internal DRQ holds low automatically at the DMA cycle of wait counter times, DMA restarts to detect the external request, if the external request signal is valid, then the next transfer starts.

(2) Handshake Mode

- When DMA detects the external request signal valid, DMA starts to operate the device, the internal DRQ always holds high level before the block operating amount reaches.
- When the transfer amount of DMA reaches the block operating amount, the internal DRQ pulls low automatically; meanwhile within the last DMA operation before reaching block amount, DMA follows the operating demand to send DMA last signal simultaneously.
- The DMA last signal that is used as a part of DMA demand transmits at BUS, when the device receives the operating demand of DMA last at BUS, the device can judge DMA transfer block length finished, that is before transmit the request again, DMA operation cannot appear, and a DMA active signal is generated to the DMA controller. Notice that each DRQ signal of device corresponds to an active signal, if the device has many DRQ signals, then DMA returns different active signal through different bus operation.
- When DMA receives the transmitted active signal of devices, DMA ACK signal is returned to devices.
- After the device receives DMA ACK signal, if all operations of devices are completed, FIFO status and DRQ status are refreshed, then active signal is set as invalid.
- When DMA detects the falling edge of active signal, then the corresponding ACK signal is set as invalid, and DMA restarts to detect the external request signal. If the request signal is valid, then the next transfer starts.

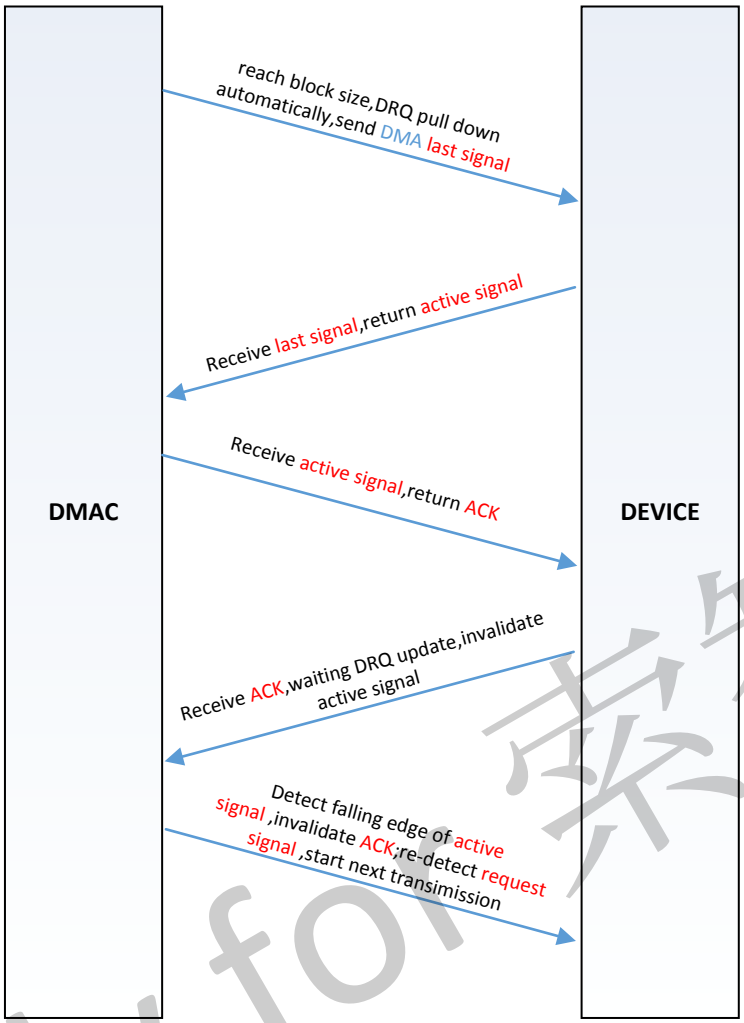

Figure 3- 23. DMA Transfer Mode

3.9.3.8. Auto-alignment Function

The DMA supports address alignment of non-IO devices, that is when the start address of non-IO devices is non 32-byte aligned, DMA firstly aligns the burst transfer within 32-byte to 32-byte. If the device of a DMA channel is configured to non-IO type, and the start address is 0x86, then DMA firstly aligns 26-byte burst transfer to 0xA0, then DMA transfers by 64-byte burst(maximum transfer amount of MBUS allowed). The address 32-byte alignment helps to improve the DRAM access efficiency.

IO devices do not support address alignment, so the bit width of IO devices must match the address offset, or not DMA ignores the non-consistency and indirectly transmits data of the corresponding bit width to the address.

The DMA descriptor address does not support auto-aligned function. The address must ensure word-aligned, or not DMA cannot identify descriptor.

3.9.3.9. Operating Mode

3.9.3.9.1. DMA Clock Control

- The DMA clock is synchronous with AHB1 clock. Make sure that open the DMA gating bit of AHB1 clock before access DMA register.
- The reset input signal of DMA is asynchronous with AHB1, and is low valid by default. Make sure that de-assert the reset signal of DMA before access DMA register.
- To avoid indefinite state within registers, firstly de-assert the reset signal, secondly open the gating bit of AHB1.
- DMA has the function of clock auto gating, DMA clock can be disabled in DMA idle state using software to reduce power consumption. DMA enables clock auto gating by default.

3.9.3.9.2. DMA Transfer Process

The DMA transfer process is as follows.

(1) Request DMA channel, and judge the idle state of the channel by whether DMA channel is enabled.
(2) Write the descriptor(6 words) into memory, the descriptor must be word-aligned. Refer to ***3.9.3.4 DMA descriptor*** in detail.
(3) Write the start address of storing descriptor to **DMA_DESC_ADDR_REG**.
(4) Enable DMA channel, and write the corresponding channel to **DMA_EN_REG**.
(5) DMA obtains the descriptor information.
(6) Start to transmit a package, when half package is completed, DMA sends **Half Package Transfer Interrupt**; when total package is completed, DMA sends **Package End Transfer Interrupt**. These interrupt status can be read by **DMA_IRQ_PEND_REG**.
(7) Set **DMA_PAU_REG** to pause or resume the data transfer.
(8) After completed the total package transfer, DMA decides to start the next package transfer or end the transfer by the link of the descriptor. If the link is 0xFFFFF800, the transfer ends; if the link is other value, the next package starts to transmit. When the transfer ends, DMA sends **Queue End Transfer Interrupt**.
(9) Disable the DMA channel.

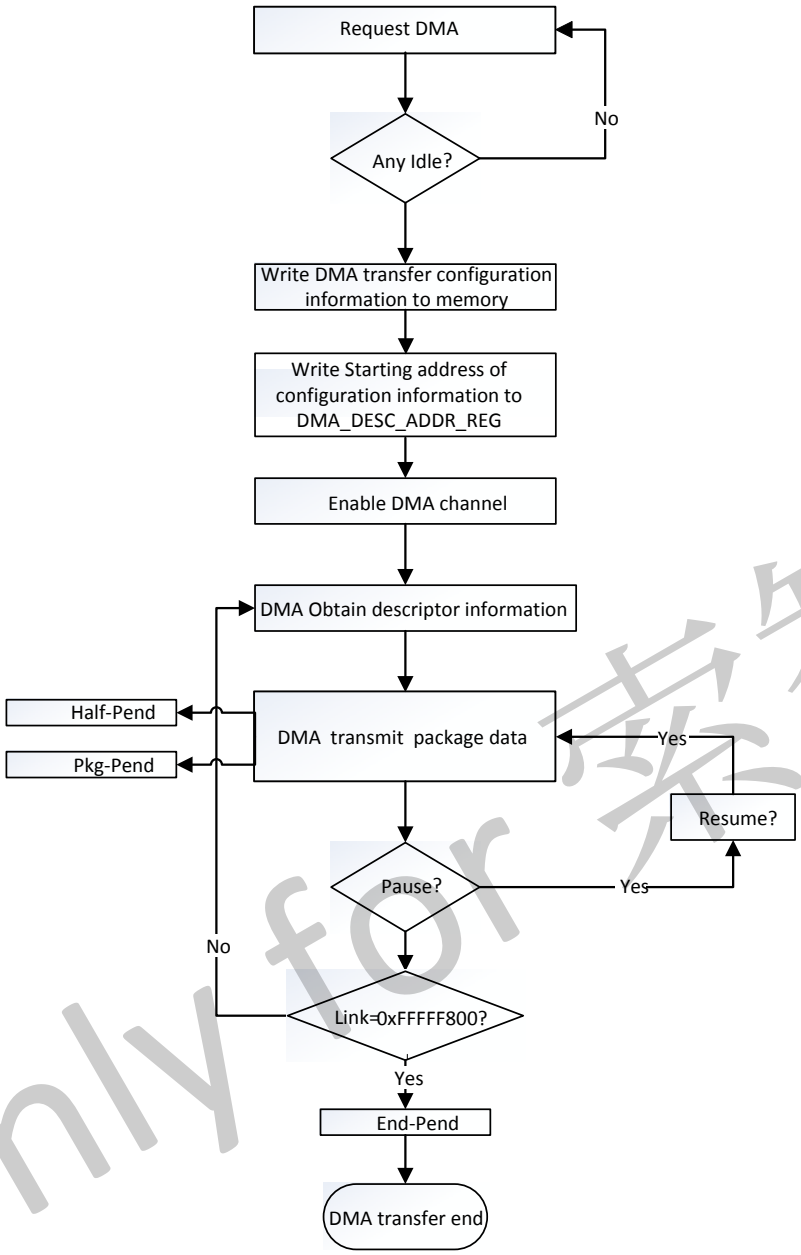

Figure 3- 24. DMA Transfer Process

3.9.3.9.3. DMA Interrupt

(1) Enable interrupt: write the corresponding interrupt enable of **DMA_IRQ_EN_REG**, when the corresponding interrupt condition is satisfied, the corresponding interrupt generates.

(2) After enter the interrupt process, write **DMA_IRQ_PEND_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.

(3) Resume the interrupt and continue to execute the interrupted process.

3.9.4. Programming Guidelines

(1) The transfer width of IO type device is consistent with the offset of start address.
(2) MBUS protocol does not support read operation of non-integer word, so for non-integer word read operation, device must ignore redundant inconsistent data between data width and configuration, that is, the device of non-integer word must interpret DMA demand through its FIFO width instead of read demand width.
(3) When the DMA transfer is paused, this is equivalent to invalid DRQ. Because DMA transfer command has a certain time delay, DMA will not stop transfer immediately until the current command and the command in Arbiter finished, at most 32byte data.

DMA application example:

```
writel(0x00000000, mem_address + 0x00);   //Setting configuration, mem_address must be word-aligned
writel(0x00001000, mem_address + 0x04);    // Setting the start address for the source device
writel(0x20000000, mem_address + 0x08);   //Setting the start address for the destination device
writel(0x00000020, mem_address + 0x0C);   // Setting data package size
writel(0x00000000, mem_address + 0x10);   //Setting parameter
writel(0xFFFFF800, mem_address + 0x14);    //Setting the start address for the next descriptor
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Setting the start address for the DMA channel0 descriptor
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure writing operation valid
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);     // Enable DMA channel0 transfer
```

DMA supports increasing data package in transfer, there are a few points to note here.

- When the value of **DMA Channel Descriptor Address Register** is 0xFFFFF800, it indicates that DMA channel has got back the descriptor of the last package. When DMA channel completed the package data transfer, DMA channel will stop automatically data transfer.
- If data packages are needed to increase, then at first it is essential to judge that whether DMA channel has got back the descriptor of the last package, if DMA channel has got back the descriptor of the last package, then this is impossible for increasing data package, DMA channel need start again. If DMA is not transmitting the last package, then the last descriptor address 0xFFFFF800 can be changed to the start address of the next descriptor.
- To ensure that the data changed valid, we can read again the value of **DMA Channel Descriptor Address Register** after changed the data. If there is not 0xFFFFF800, then it indicates that increasing data package is succeed, and fail otherwise. Because the process of increasing data package needs some time, during this time, DMA channel may get back the descriptor of the last package. At the moment we can read again **DMA Channel Current Source Address Register** and **DMA Channel Current Destination Address Register**, if the increasing memory address accords with the information of the increasing data package, then the increasing data package is succeed, and fail otherwise.
- To ensure the higher success rate, it is suggested that increase data package before half package interrupt of penultimate data package.

3.9.5. Register List

Module Name	Base Address
DMA	0x03002000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register 0
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register 0
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x0040	DMA Channel Enable Register (N=0~7)
DMA_PAU_REG	0x0100+N*0x0040+0x0004	DMA Channel Pause Register(N=0~7)
DMA_DESC_ADDR_REG	0x0100+N*0x0040+0x0008	DMA Channel Start Address Register(N=0~7)
DMA_CFG_REG	0x0100+N*0x0040+0x000C	DMA Channel Configuration Register(N=0~7)
DMA_CUR_SRC_REG	0x0100+N*0x0040+0x0010	DMA Channel Current Source Register(N=0~7)
DMA_CUR_DEST_REG	0x0100+N*0x0040+0x0014	DMA Channel Current Destination Register(N=0~7)
DMA_BCNT_LEFT_REG	0x0100+N*0x0040+0x0018	DMA Channel Byte Counter Left Register(N=0~7)
DMA_PARA_REG	0x0100+N*0x0040+0x001C	DMA Channel Parameter Register(N=0~7)
DMA_MODE_REG	0x0100+N*0x0040+0x0028	DMA Mode Register(N=0~7)
DMA_FDESC_ADDR_REG	0x0100+N*0x0040+0x002C	DMA Former Descriptor Address Register(N=0~7)
DMA_PKG_NUM_REG	0x0100+N*0x0040+0x0030	DMA Package Number Register(N=0~7)

3.9.6. Register Description

3.9.6.1. 0x0000 DMA IRQ Enable Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
27	/	/	/

26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable

			0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable 0: Disable 1: Enable

3.9.6.2. 0x0010 DMA IRQ Pending Status Register 0 (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND

			DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it.

			0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND DMA 0 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.9.6.3. 0x0028 DMA Auto Gating Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	DMA_MCLK_CIRCUIT DMA MCLK interface circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT DMA common circuit auto gating bit 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT DMA channel circuit auto gating bit 0: Auto gating enable 1: Auto gating disable

NOTE

When initializing DMA Controller, the bit-2 should be set up.

3.9.6.4. 0x0030 DMA Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	MBUS FIFO Status 0: Empty 1: Not Empty
29:8	/	/	/
7	R	0x0	DMA7_STATUS DMA Channel 7 Status 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS

			DMA Channel 4 Status 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status 0: Idle 1: Busy

3.9.6.5. 0x0100+N*0x0040 DMA Channel Enable Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040 (N=0~7)			Register Name: DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_EN DMA Channel Enable 0: Disable 1: Enable

3.9.6.6. 0x0104+N*0x0040 DMA Channel Pause Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0004(N=0~7)			Register Name: DMA_PAU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE Pausing DMA Channel Transfer Data 0: Resume Transferring 1: Pause Transferring

3.9.6.7. 0x0108+N*0x0040 DMA Channel Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0008(N=0~7)			Register Name: DMA_DESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMA_DESC_ADDR DMA Channel Descriptor Address The Descriptor Address must be word-aligned.

3.9.6.8. 0x010C+N*0x0040 DMA Channel Configuration Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x000C(N=0~7)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH DMA Destination Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	R	0x0	DMA_ADDR_MODE DMA Destination Address Mode 0: Linear Mode 1: IO Mode
23:22	R	0x0	DMA_DEST_BLOCK_SIZE DMA Destination Block Size 00: 1 01: 4 10: 8 11: 16
21:16	R	0x0	DMA_DEST_DRQ_TYPE DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH DMA Source Data Width 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	R	0x0	DMA_SRC_ADDR_MODE DMA Source Address Mode 0: Linear Mode 1: IO Mode

7:6	R	0x0	DMA_SRC_BLOCK_SIZE DMA Source Block Size 00: 1 01: 4 10: 8 11: 16
5:0	R	0x0	DMA_SRC_DRQ_TYPE DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

3.9.6.9. 0x0110+N*0x0040 DMA Channel Current Source Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0010(N=0~7)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC DMA Channel Current Source Address, read only.

3.9.6.10. 0x0114+N*0x0040 DMA Channel Current Destination Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0014(N=0~7)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST DMA Channel Current Destination Address, read only.

3.9.6.11. 0x0118+N*0x0040 DMA Channel Byte Counter Left Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0018(N=0~7)			Register Name: DMA_BCNT_LEFT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT DMA Channel Byte Counter Left, read only.

3.9.6.12. 0x011C+N*0x0040 DMA Channel Parameter Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x001C(N=0~7)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	WAIT_CYC Wait Clock Cycles

3.9.6.13. 0x0128+N*0x0040 DMA Mode Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0028(N=0~7)			Register Name: DMA_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE 0: Wait mode 1: Handshake mode
2	R/W	0x0	DMA_SRC_MODE 0: Wait mode 1: Handshake mode
1:0	/	/	/

3.9.6.14. 0x012C+N*0x0040 DMA Former Descriptor Address Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x002C(N=0~7)			Register Name: DMA_FDESC_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_FDESC_ADDR This register is used to store the former value of DMA Channel Descriptor Address Register.

3.9.6.15. 0x0130+N*0x0040 DMA Package Number Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0040+0x0030(N=0~7)			Register Name: DMA_PKG_NUM_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_PKG_NUM This register will record the number of packages which has been completed in one transmission.

3.10. Thermal Sensor Controller

3.10.1. Overview

Thermal sensors have became common elements in wide range of modern system on chip (SOC) platform. Thermal sensors are used to constantly monitor the temperature on the chip.

The Thermal Sensor Controller(THS) embeds four thermal sensors, sensor0 is located in CPU, sensor1 is located in VE, sensor2 is located in AI, sensor3 is located in DDR. The thermal sensor can generate interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

The THS has the following features:

- Temperature Accuracy : ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Power supply voltage: 1.8V
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt

3.10.2. Block Diagram

Figure 3-25 shows a block diagram of the Thermal Sensor Controller.

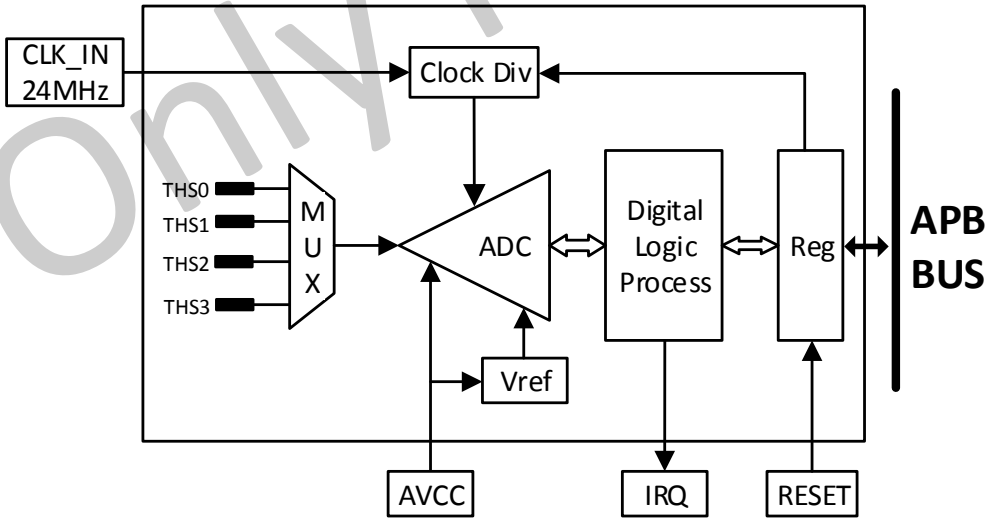

Figure 3- 25. Thermal Sensor Controller Block Diagram

3.10.3. Operations and Functional Descriptions

3.10.3.1. Clock Sources

The THS gets one clock source. Table 3-9 describes the clock source for Thermal Sensor Controller. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 3- 9. Thermal Sensor Controller Clock Sources

Clock Sources	Description
OSC24M	24M OSC

3.10.3.2. Timing Requirements

CLK_IN = 24MHz
CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)
TACQ> 1/(24MHz/24Cycles)
THERMAL_PER > ADC Sample Frequency > TACQ+CONV_TIME

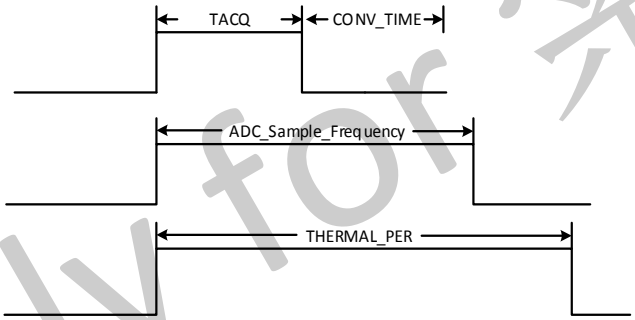

Figure 3- 26. Thermal Sensor Time Requirement

3.10.3.3. Interrupt

The THS has four interrupt sources, such as DATA_IRQ, SHUTDOWN_IRQ, ALARM_IRQ and ALARM_OFF_IRQ. Figure 3-27 shows the thermal sensor interrupt sources.

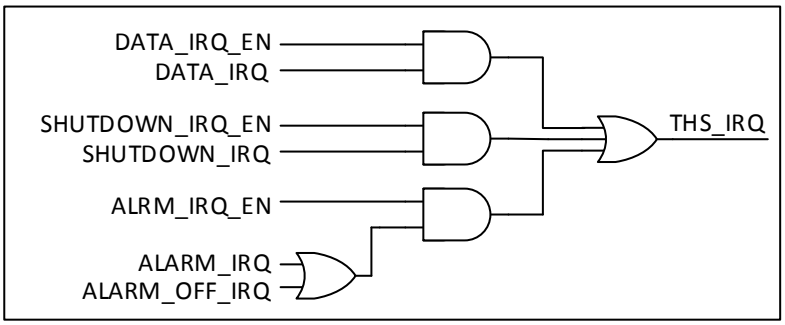

Figure 3- 27. Thermal Sensor Controller Interrupt Source

When temperature is higher than Alarm_Threshold, ALARM_IRQ is generated. When temperature is lower than

Alarm_Off_Thershold, ALARM_OFF_IRQ is generated. ALARM_OFF_IRQ is fall edge trigger.

3.10.3.4. THS Temperature Conversion Formula

T= (sensor_data - 2794)/(-14.882), the unit of T is Celsius.
sensor_data: read from sensor data register.

3.10.4. Programming Guidelines

The initial process of the THS is as follows.

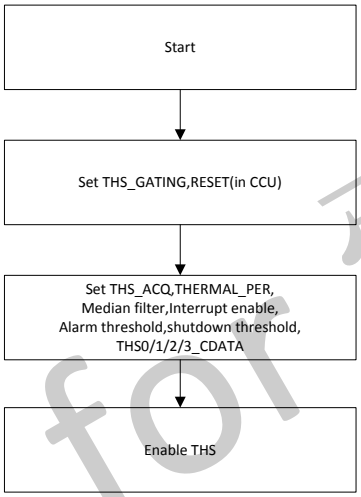

Figure 3- 28. THS Initial Process

The formula of THS is y=-ax+b. In FT stage, THS is calibrated through ambient temperature, the calibration value is written in EFUSE. Please refer to SID Spec about EFUSE information.

Before enabling THS, read EFUSE value and write the value to **THS_CDATA**.

(1).Query Mode

Step1: Write 0x1 to the bit16 of **THS_BGR_REG** to dessert reset.
Step2: Write 0x1 to the bit0 of **THS_BGR_REG** to enable THS clock.
Step3: Write 0x2F to the bit[15:0] of **THS_CTRL** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL** to set ADC sample frequency divider.
Step5: Write 0x3A to the bit[31:12] of **THS_PER** to set THS work period.
Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.
Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.
Step8: Read THS efuse value from SID, then write the efuse value to **THS_CDATA** to calibrate THS.
Step9: Write 0x1 to the bit[0] 0f **THS_EN** to enable THS.
Step10: Read the bit[0] of **THS_DATA_INTS**, if is 1, temperature conversion is complete.
Step11: Read the bit[11:0] of **THS_DATA**, calculate THS temperature based on THS Temperature Conversion Formula in

Section 3.10.3.4.

(2). Interrupt Mode

Step1: Write 0x1 to the bit16 of **THS_BGR_REG** to dessert reset.

Step2: Write 0x1 to the bit0 of **THS_BGR_REG** to open THS clock.

Step3: Write 0x2F to the bit[15:0] of **THS_CTRL** to set ADC acquire time.

Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL** to set ADC sample frequency divider.

Step5: Write 0x3A to the bit[31:12] of **THS_PER** to set THS work period.

Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.

Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.

Step8: Read THS efuse value from SID, then write the efuse value to **THS_CDATA** to calibrate THS.

Step9: Write 0x1 to the bit[0] of **THS_DATA_INTC** to enable the interrupt of THS.

Step10: Set GIC interface based on IRQ 33, write the bit[1] of the 0x03021104 register to 0x1.

Step11: Put interrupt handler address into interrupt vector table.

Step12: Write 0x1 to the bit[0] 0f **THS_EN** to enable THS.

Step13: Read the bit[0] of **THS_DATA_INTS**, if is 1, temperature conversion is complete.

Step14: Read the bit[11:0] of **THS_DATA**, calculate THS temperature based on THS Temperature Conversion Formula in Section 3.10.3.4.

3.10.5. Register List

Module Name	Base Address
Thermal Sensor	0x05070400

Register Name	Offset	Description
THS_CTRL	0x0000	THS Control Register
THS_EN	0x0004	THS Enable Register
THS_PER	0x0008	THS Period Control Register
THS_DATA_INTC	0x0010	THS Data Interrupt Control Register
THS_SHUT_INTC	0x0014	THS Shut Interrupt Control Register
THS_ALARM_INTC	0x0018	THS Alarm Interrupt Control Register
THS_DATA_INTS	0x0020	THS Data Interrupt Status Register
THS_SHUT_INTS	0x0024	THS Shut Interrupt Status Register
THS_ALARMO_INTS	0x0028	THS Alarm off Interrupt Status Register
THS_ALARM_INTS	0x002C	THS Alarm Interrupt Status Register
THS_FILTER	0x0030	THS Median Filter Control Register
THS0_ALARM_CTRL	0x0040	THS0 Alarm Threshold Control Register
THS1_ALARM_CTRL	0x0044	THS1 Alarm Threshold Control Register
THS2_ALARM_CTRL	0x0048	THS2 Alarm Threshold Control Register
THS3_ALARM_CTRL	0x004C	THS3 Alarm Threshold Control Register
THS01_SHUTDOWN_CTRL	0x0080	THS0 & THS1 Shutdown Threshold Control Register
THS23_SHUTDOWN_CTRL	0x0084	THS2 & THS3 Shutdown Threshold Control Register

THS01_CDATA	0x00A0	THS0 & THS1 Calibration Data
THS23_CDATA	0x00A4	THS2 & THS3 Calibration Data
THS0_DATA	0x00C0	THS0 Data Register
THS1_DATA	0x00C4	THS1 Data Register
THS2_DATA	0x00C8	THS2 Data Register
THS3_DATA	0x00CC	THS3 Data Register

3.10.6. Register Description

3.10.6.1. 0x0000 THS Control Register(Default Value : 0x01DF_002F)

Offset: 0x0000			Register Name: THS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1DF	FS_DIV ADC Sample Frequency Divider CLK_IN/(N+1) , N > 0x17 The default value indicates 50 kHz.
15:0	R/W	0x2F	TACQ ADC Acquire Time CLK_IN/(n+1) The default value indicates 2us.

3.10.6.2. 0x0004 THS Enable Register(Default Value : 0x0000_0000)

Offset: 0x0004			Register Name: THS_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	THS3_EN Enable temperature measurement sensor3 0:Disable 1:Enable
2	R/W	0x0	THS2_EN Enable temperature measurement sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_EN Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_EN Enable temperature measurement sensor0 0:Disable

			1:Enable

3.10.6.3. 0x0008 THS Period Control Register(Default Value: 0x0003_A000)

Offset: 0x0008			Register Name: THS_PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x3A	THERMAL_PER 4096*(n+1)/CLK_IN The default value indicates 10ms.
11:0	/	/	/

3.10.6.4. 0x0010 THS Data Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: THS_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	THS3_DATA_IRQ_EN Selects Temperature measurement data of sensor3 0:Disable 1:Enable
2	R/W	0x0	THS2_DATA_IRQ_EN Selects Temperature measurement data of sensor2 0:Disable 1:Enable
1	R/W	0x0	THS1_DATA_IRQ_EN Selects Temperature measurement data of sensor1 0:Disable 1:Enable
0	R/W	0x0	THS0_DATA_IRQ_EN Selects Temperature measurement data of sensor0 0:Disable 1:Enable

3.10.6.5. 0x0014 THS Shut Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: THS_SHUT_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	SHUT_INT3_EN Selects shutdown interrupt for sensor3 0:Disable

			1:Enable
2	R/W	0x0	SHUT_INT2_EN Selects shutdown interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0:Disable 1:Enable

3.10.6.6. 0x0018 THS Alarm Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: THS_ALARM_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	ALARM_INT3_EN Selects Alarm interrupt for sensor3 0:Disable 1:Enable
2	R/W	0x0	ALARM_INT2_EN Selects Alarm interrupt for sensor2 0:Disable 1:Enable
1	R/W	0x0	ALARM_INT1_EN Selects Alarm interrupt for sensor1 0:Disable 1:Enable
0	R/W	0x0	ALARM_INT0_EN Selects Alarm interrupt for sensor0 0:Disable 1:Enable

3.10.6.7. 0x0020 THS Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: THS_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	THS3_DATA_IRQ _STS

			Data interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	THS2_DATA_IRQ _STS Data interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	THS1_DATA_IRQ _STS Data interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	THS0_DATA_IRQ _STS Data interrupt status for sensor0 Write '1' to clear this interrupt.

3.10.6.8. 0x0024 THS Shut Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: THS_SHUT_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	SHUT_INT3_STS Shutdown interrupt status for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	SHUT_INT2_STS Shutdown interrupt status for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt.

3.10.6.9. 0x0028 THS Alarm Off Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: THS_ALARMO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	ALARM_OFF3_STS Alarm interrupt off pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_OFF2_STS Alarm interrupt off pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_OFF1_STS

			Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt.

3.10.6.10. 0x002C THS Alarm Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: THS_ALARM_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	ALARM_INT3_STS Alarm interrupt pending for sensor3 Write '1' to clear this interrupt.
2	R/W1C	0x0	ALARM_INT2_STS Alarm interrupt pending for sensor2 Write '1' to clear this interrupt.
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt.
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt.

3.10.6.11. 0x0030 Median Filter Control Register(Default Value: 0x0000_0001)

Offset: 0x0030			Register Name: THS_FILTER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE Average Filter Type 00: 2 01: 4 10: 8 11: 16

3.10.6.12. 0x0040 THS0 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0040			Register Name: THS0_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal Sensor0 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal Sensor0 alarm threshold for hysteresis temperature

3.10.6.13. 0x0044 THS1 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0044			Register Name: THS1_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal Sensor1 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal Sensor1 alarm threshold for hysteresis temperature

3.10.6.14. 0x0048 THS2 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x0048			Register Name: THS2_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM2_T_HOT Thermal Sensor2 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM2_T_HYST Thermal Sensor2 alarm threshold for hysteresis temperature

3.10.6.15. 0x004C THS3 Alarm Threshold Control Register(Default Value: 0x05A0_0684)

Offset: 0x004C			Register Name: THS3_ALARM_CTRL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM3_T_HOT Thermal Sensor3 alarm threshold for hot temperature
15:12	/	/	/

11:0	R/W	0x684	ALARM3_T_HYST Thermal Sensor3 alarm threshold for hysteresis temperature

3.10.6.16. 0x0080 THS0&1 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0080			Register Name: THS01_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal Sensor1 shutdown threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT0_T_HOT Thermal Sensor0 shutdown threshold for hot temperature

3.10.6.17. 0x0084 THS2&3 Shutdown Threshold Control Register (Default Value: 0x04E9_04E9)

Offset: 0x0084			Register Name: THS23_SHUTDOWN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x4E9	SHUT3_T_HOT Thermal Sensor3 shutdown threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x4E9	SHUT2_T_HOT Thermal Sensor2 shutdown threshold for hot temperature

3.10.6.18. 0x00A0 THS0&1 Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x00A0			Register Name: THS01_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x800	THS1_CDATA Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA Thermal Sensor0 calibration data

3.10.6.19. 0x00A4 THS2&3 Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x00A4			Register Name: THS23_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**

31:28	/	/	/
27:16	R/W	0x800	THS3_CDATA Thermal Sensor3 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS2_CDATA Thermal Sensor2 calibration data

3.10.6.20. 0x00C0 THS0 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: THS0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA Temperature measurement data of sensor0

3.10.6.21. 0x00C4 THS1 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: THS1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA Temperature measurement data of sensor1

3.10.6.22. 0x00C8 THS2 Data Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: THS2_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS2_DATA Temperature measurement data of sensor2

3.10.6.23. 0x00CC THS3 Data Register(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: THS3_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS3_DATA Temperature measurement data of sensor3

3.11. PSI

3.11.1. Overview

PSI(Peripheral System Interconnect) is a peripheral bus interconnect device based on AHB and APB protocol, which supports 16 AHB master and 16 slave bus. The type of slave bus can be AHB bus or APB bus. Each bus supports 64 slave devices.

3.11.2. Block Diagram

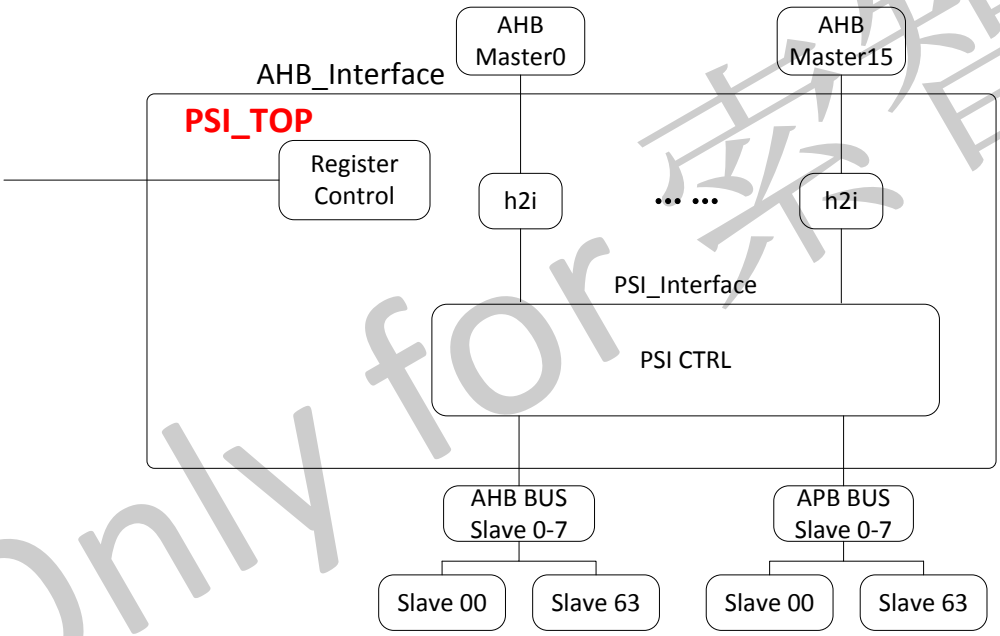

Figure 3- 29. PSI Block Diagram

For complete PSI information, refer to the ***Allwinner V833/V831 PSI Specification***.

3.12. IOMMU

3.12.1. Overview

IOMMU(I/O Memory management unit) is designed for product specific memory requirements. It maps the virtual address(sent by peripheral access memory) to the physical address. IOMMU allows multiple ways to manage the location of physical address, and it can use physical address which has potentially conflict mapping for different processes to allocate memory space, and also allow application of non-continuous address mapping to continuous virtual address space.

Features:

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE, EISE, AI, VE, CSI, ISP, G2D parallel address mapping
- Supports DE, EISE, AI, VE, CSI, ISP, G2D bypass function independently
- Supports DE, EISE, AI, VE, CSI, ISP, G2D prefetch independently
- Supports DE, EISE, AI, VE, CSI, ISP, G2D interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

3.12.2. Block Diagram

IOMMU internal module mainly has the following parts.

Micro TLB: level1 TLB, 64 words. Each peripheral corresponds to a TLB, which caching the level2 page table for the peripheral.

Macro TLB: level2 TLB, 4K words. Each peripheral shares a level2 TLB for caching the level2 page table.

Prefetch Logic: Each Micro TLB corresponds to a Prefetch Logic. By monitoring each master device to predict the bus access, the secondary page table corresponding to the address to be accessed can be read from memory and stored in the secondary TLB to improve hit ratio.

PTW Logic: Page Table Walk, mainly contains PTW Cache and PTW. The PTW Cache is used to store the level1 page table; when the virtual address VA missed in the level1 and level2 TLB, it will trigger the PTW. PTW Cache can store 512 level1 page tables, that is, 512 words.

PMU: Performance Monitoring Unit, which is used to count hit efficiency and latency.

APB Interface: IOMMU register instantiation module. CPU reads and writes the IOMMU register by APB bus.

Figure 3-30 shows the internal block diagram of IOMMU.

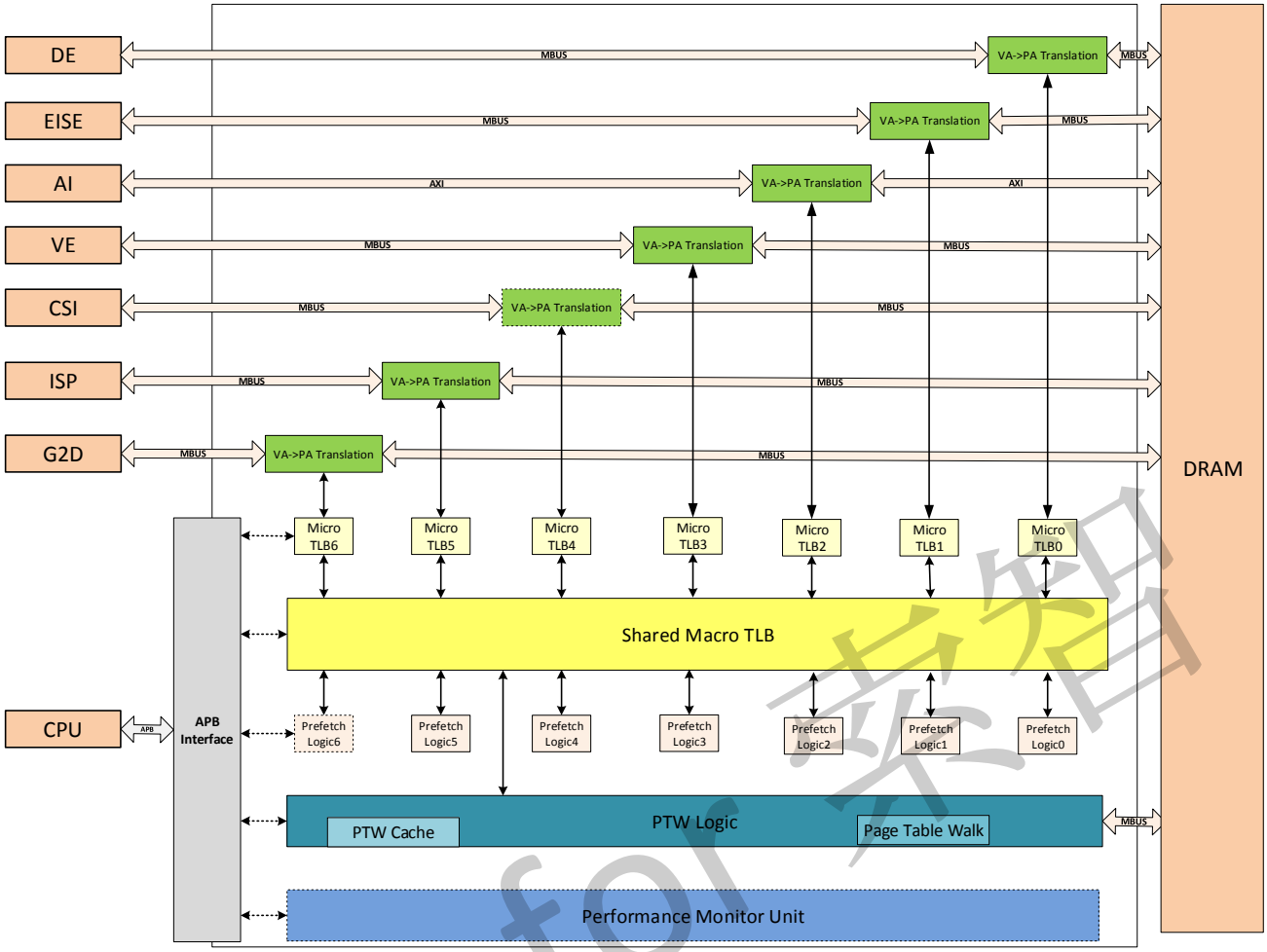

Figure 3- 30. IOMMU Block Diagram

Table 3- 11. Correspondence Relation between Master and Module

Master Number	Module
Master0	DE
Master1	EISE
Master2	AI
Master3	VE
Master4	CSI
Master5	ISP
Master6	G2D

3.12.3. Operations and Functional Descriptions

3.12.3.1. Clock Sources

IOMMU contains two clock domains in the module. Address mapping is generated by MBUS clock domain, and Register and interrupt processing are generated by APB clock domain. The two domains are asynchronous, and they are from different clock sources.

3.12.3.2. Operation Modes

3.12.3.2.1. Initialization

- Release the IOMMU reset signal by writing 1 to the bit[31] of the ***IOMMU Reset Register***;
- Write the base address of the first TLB to the ***IOMMU Translation Table Base Register***;
- Set up the ***IOMMU Interrupt Enable Register***;
- Enable the IOMMU by configuring the ***IOMMU Enable Register*** in the final.

3.12.3.2.2. Address Changing

In the process of address mapping, The peripheral virtual address VA[31:12] are retrieved in the Level1 TLB, when TLB hits, the mapping finished, or they are retrieved in the Level2 TLB in the same way. If TLB hits, it will write the hit mapping to the Level1 TLB, and hits in Level1 TLB. If Level1 and Level2 TLB are retrieved fail, it will trigger the PTW. After opening peripheral bypass function by setting IOMMU Bypass Register, IOMMU will not map the address for peripheral typed the address, and it will output the virtual address as physical address. The typical application is as follows.

- **Micro TLB hit**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;
b). If Micro TLB hits, it will return a corresponding physical addresses and the Level2 page table of permission Index;
c). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB hit**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;
b). If Micro TLB misses, then continue to search Macro TLB;
c). If Macro TLB hits, it will return the Level2 page table to Micro TLB;
d). Micro TLB receives the page table, and puts it to Micro TLB(if this Micro TLB is full, there has replace activities), at the same time, sends page table entries to address translation module;
e). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB miss, PTW Cache hit**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;
b). If Micro TLB misses, then continue to search Macro TLB;
c). If Macro TLB misses, then it will send the request to the PTW to return the corresponding page table;
d). PTW first accesses PTW Cache, confirms that the required Level1 page table exists in the PTW Cache, sends the page table to PTW logic;
e). PTW logic returns the corresponding Level2 page table from memory page table according to Level1 page table,

checks the effectiveness, and sends to Macro TLB;

f). Macro TLB stores the Level2 page table (may happen replace activities), and will return the Level2 page table to Micro TLB;

g). Micro TLB receives the page table entries, puts in the Micro TLB (if this Micro TLB is full, there will happen replace activities), and sends page table entries to address translation module;

h). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Micro TLB miss, Macro TLB miss, PTW Cache miss**

a). The master device sends a transfer command, and also sends the address to the corresponding Micro TLB, and searches virtual address corresponding to the Level2 page table;

b). If Micro TLB misses, then continue to search Macro TLB;

c). If Macro TLB misses, there will send the request to the PTW to return the corresponding page table;

d). PTW accesses PTW Cache, there is no necessary Level1 page table;

e). PTW accesses memory, gets the corresponding Level1 page table and stores in the PTW Cache; (may happen replace activities)

f). PTW logic returns the corresponding Level2 page table from memory page table according to Level1 page table, checks the effectiveness, and sends to Macro TLB;

g). Macro TLB stores the Level2 page table (may happen replace activities), and will return the Level 2 page table to Micro TLB;

h). Micro TLB receives the page table entries, puts in the Micro TLB (if this Micro TLB is full, there will happen replace activities), and sends page table entries to address translation module;

i). Address transform module converts the virtual address into physical address, and checks the permissions at the same time. If pass, transfer is completed.

- **Permission error**

a). Permission checking always performs in the address conversion;

b). Once the permission checking makes mistake, the new access of the master suspends, before this visit continues;

c). Set the error status register;

d). Trigger interrupt.

- **Invalid Level1 page table**

a). Invalid Level1 page table is checked when PTW logic reads the new level page table from memory;

b). The PTW read sequentially two page table entries from the memory (64-bit data, a complete cache line), and stores in the PTW cache;

c). If the current page table is detected invalid, then the error flag is set, and the interrupt is triggered, the cache line need to be invalidated.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid; and the page table stored in PTW Cache with target page table is found to be invalid after using;

If a page table is invalid, then total cache line(that is two page tables) need to be invalidated.

- **Invalid Level2 page table**

a). Invalid Level2 page table checks when Macro TLB reads the new level page table from memory;

b). The Macro TLB read sequentially two page table entries from the memory (64-bit data, a complete cache line), and stores in the Macro TLB;

c). If the current page table is detected invalid, then the error flag is set, and the interrupt is triggered, the cache line need to be invalidated.

NOTE

Invalid page table has two situations: the reading target page table from the memory is invalid; and the page table stored in Macro TLB with target page table is found to be invalid after using.

If a page table is invalid, then total cache line(that is two page tables) need to be invalidated.

The internal address switch process shows in Figure 3-31.

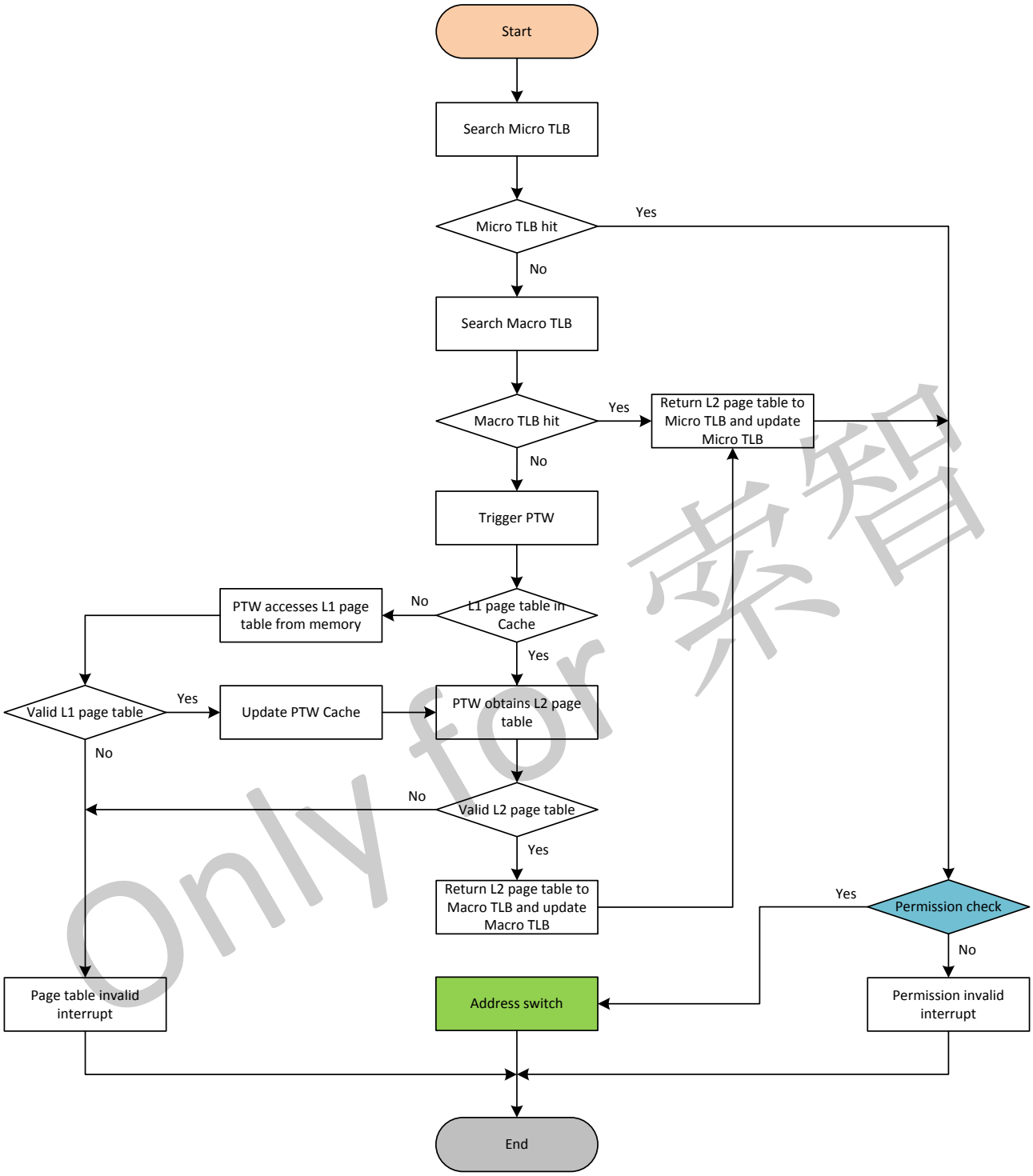

Figure 3- 31. Internal Switch Process

3.12.3.2.3. VA-PA Mapping

IOMMU page table is defined as Level2 mapping, the first level is 1M address space mapping, the second level is 4K address space. This version does not support 1K, 16K and other page table size. IOMMU supports a page table only, its

meaning is:

- All peripherals connected to IOMMU use the same virtual address space;
- The virtual address space of the peripherals can overlap;
- Different virtual addresses can map to the same physical address space;

Base address of the page table is defined by software, and it needs 16KByte address alignment; Page table of the Level2 table item needs 1KByte address alignment. A complete VA-PA address translation process is shown in Figure 3-32.

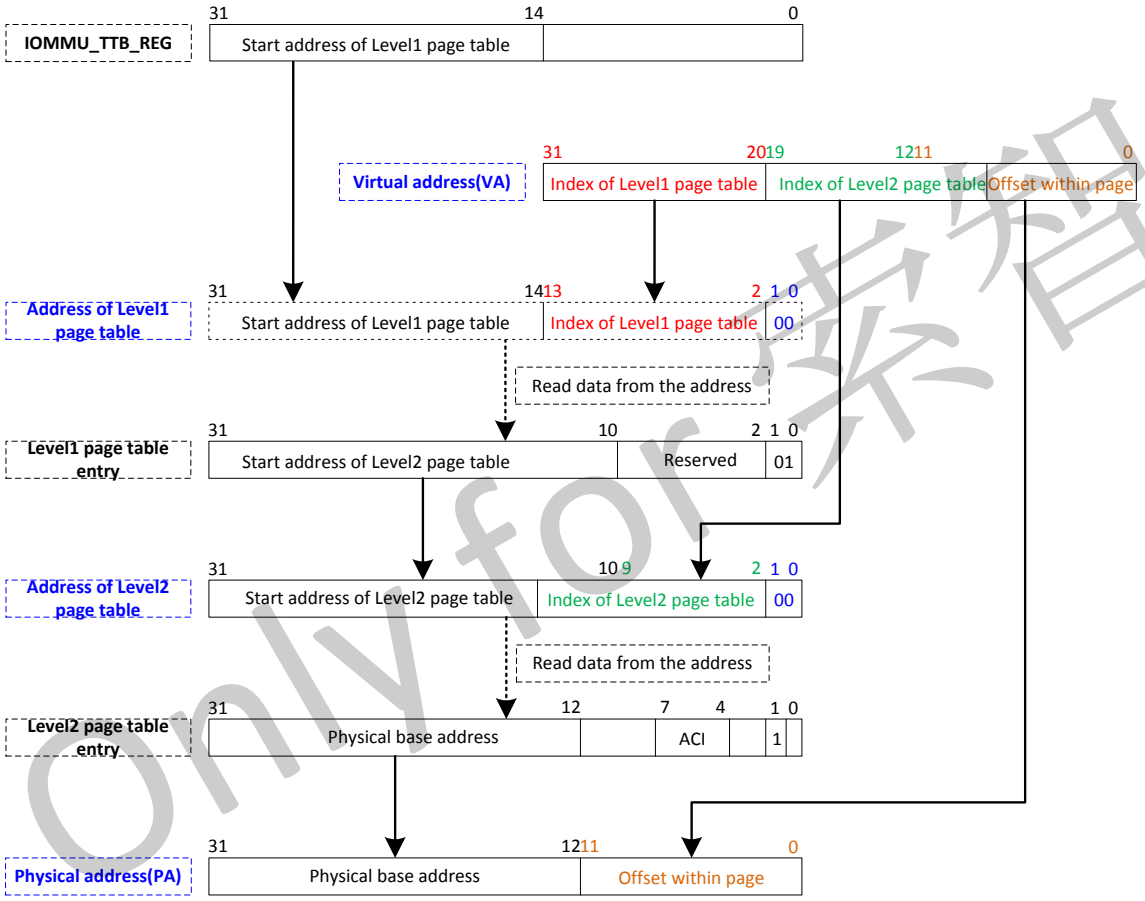

Figure 3- 32. VA-PA Switch Process

3.12.3.2.4. Clear and Invalidate TLB

When multi page table content refresh, or table address changes, all VA-PA mapping which has been cached in TLB will no longer be valid , then you need configure **IOMMU TLB Flush Enable Register** to clear the TLB or PTW Cache. First suspend access to TLB or Cache, then configure the corresponding Flush bit of **IOMMU TLB Flush Enable Register** , after operation takes effect, related peripherals can continue to send new access memory operations.

When some page table is invalid or incorrect mapping, you can set the TLB Invalidation relevant register to invalidate TLB VA-PA mapping pairs. The invalid TLB supports two modes.

(1) Mode0

Firstly, set **IOMMU TLB Invalidation Mode Select Register to 0 to select mode0;**
Secondly, write target address to **IOMMU TLB Invalidation Address Register**;
Thirdly, set configuration values to **IOMMU TLB Invalidation Address Mask Register**, the requirements are as follows:

- The value of **IOMMU TLB Invalidation Address Mask Register** cannot be less than the **IOMMU TLB Invalidation Address Register**.
- The higher bit of **IOMMU TLB Invalidation Address Mask Register** must be continuous 1, the lower bit must be continuous 0, for example, 0xfffff000, 0xffffe000, 0xffffc000, 0xffff8000, 0xffff0000 belongs to the legal value; and 0xffffd000, 0xffffb000, 0xfffa000, 0xffff9000, 0xffff7000 belongs to illegal values.

Finally, configure **IOMMU TLB Invalidation Enable Register** to enable invalid operation. Among the way to determine the invalid address is to get maximum valid bit and determine target address range by target address AND mask address. The process is shown as follows.

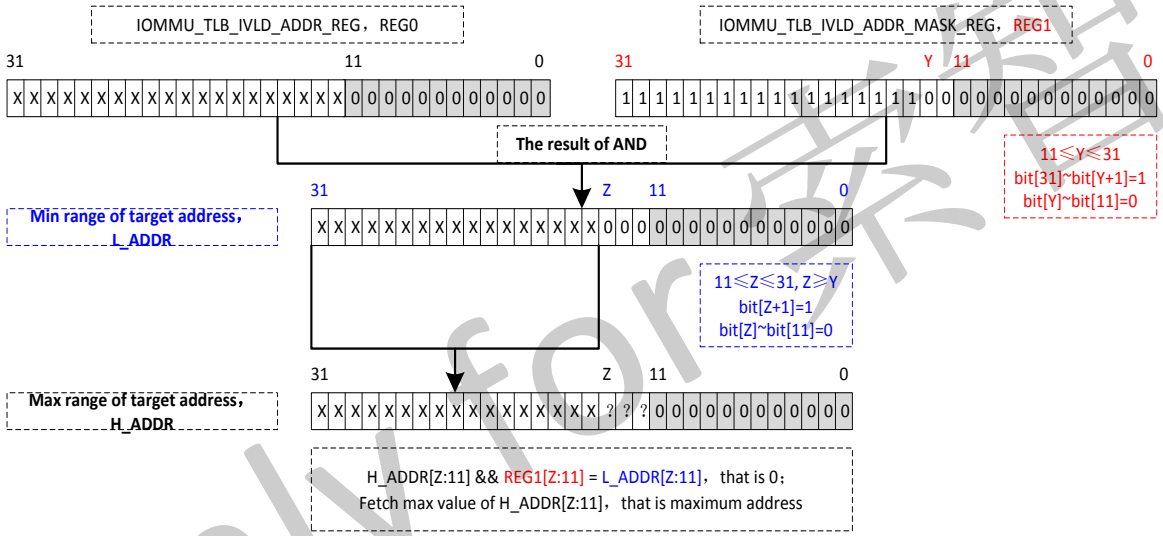

Figure 3- 33. Invalid TLB Address Range

For example:

a). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFF000 by default, the result of AND is target address, that is, only target address is invalid.

b). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFF0000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE1000, then target address range is from 0xEEEE0000 to 0xEEEEF000.

c). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFC000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE8000, then target address range is from 0xEEEE8000 to 0xEEEEB000.

d). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFF8000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEEC000, then target address range is from 0xEEEE8000 to 0xEEEEF000.

e). When the value of **IOMMU TLB Invalidation Address Mask Register** is 0xFFFFC000, the value of **IOMMU TLB Invalidation Address Register** is 0xEEEE0000, then target address range is from 0xEEEE0000 to 0xEEEE3000.

(2) Mode1

Firstly, set **IOMMU TLB Invalidation Mode Select Register to 1 to select mode1;**
Secondly, set the starting address of invalid TLB by **IOMMU TLB Invalidation Start Address Register,** and set the

ending address of invalid TLB **by IOMMU TLB Invalidation Start Address Register;**

Finally, configure **IOMMU TLB Invalidation Enable Register** to enable invalid operation, then invalid related TLB operation can be completed.

3.12.3.3. Page Table Format

3.12.3.3.1. Level1 Page Table

The format of Level1 page table is as follows.

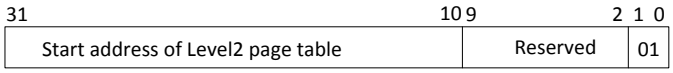

Figure 3- 34. Level1 Page Table Format

Bit[31:10]: Base address of Level2 page table;

Bit[9:2]: Reserved;

Bit[1:0]: 01 is valid page table; others are fault;

3.12.3.3.2. Level2 Page Table

The format of Level2 page table is as follows.

Figure 3- 35. Level1 Page Table Format

Bit[31:12]: Physical address of 4K address;

Bit[11:8]: Reserved;

Bit[7:4]: ACI, permission control index; correspond to permission control bit of **IOMMU Domain Authority Control Register**;

Bit[3:2]: Reserved;

Bit[1]: 1 is valid page table; 0 is fault;

Bit[0]: Reserved

3.12.3.3.3. Permission Index

The read/write access control of series register such as **IOMMU Domain Authority Control Register** is as follows.

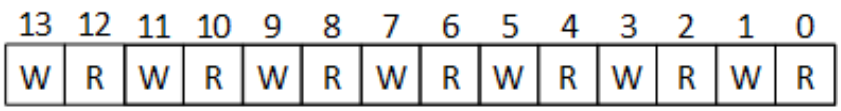

Figure 3- 36. Read/Write Permission Control

Bit[1:0]/Bit[17:16]: Master0 read/write permission control;

Bit[3:2]/Bit[19:18]: Master1 read/write permission control;

Bit[5:4]/Bit[21:20]: Master2 read/write permission control;

Bit[7:6]/Bit[23:22]: Master3 read/write permission control;

Bit[9:8]/Bit[25:24]: Master4 read/write permission control;
Bit[11:10]/Bit[27:26]: Master5 read/write permission control;
Bit[13:12]/Bit[29:28]: Master6 read/write permissiom control.

The value of **IOMMU Domain Authority Control Register** is read-only by default. Other registers can configure through system requirement. In address switch process, the corresponding relation between ACI and Domain is as follows.

Table 3- 12. Relation between ACI and Domain

ACI	Domain	Register
0	Domain 0	IOMMU Domain Authority Control Register 0
1	Domain 1	IOMMU Domain Authority Control Register 0
2	Domain 2	IOMMU Domain Authority Control Register 1
3	Domain 3	IOMMU Domain Authority Control Register 1
4	Domain 4	IOMMU Domain Authority Control Register 2
5	Domain 5	IOMMU Domain Authority Control Register 2
6	Domain 6	IOMMU Domain Authority Control Register 3
7	Domain 7	IOMMU Domain Authority Control Register 3
8	Domain 8	IOMMU Domain Authority Control Register 4
9	Domain 9	IOMMU Domain Authority Control Register 4
10	Domain 10	IOMMU Domain Authority Control Register 5
11	Domain 11	IOMMU Domain Authority Control Register 5
12	Domain 12	IOMMU Domain Authority Control Register 6
13	Domain 13	IOMMU Domain Authority Control Register 6
14	Domain 14	IOMMU Domain Authority Control Register 7
15	Domain 15	IOMMU Domain Authority Control Register 7

After enabled **IOMMU Domain Authority Overwrite Register**, the read/write control permission can override all **IOMMU Domain Authority Control Register**.

3.12.4. Programming Guidelines

3.12.4.1. IOMMU Reset

Before the IOMMU module software reset operation, make sure IOMMU is never opened, or all bus operations are completed, or DRAM and peripherals already open the corresponding switch, to shield the influence of IOMMU reset.

3.12.4.2. IOMMU Enable

Before opening the IOMMU address mapping function, Translation Table Base register should be correctly configured, or all the masters are in the bypass state, or all the masters do not send the bus command.

3.12.4.3. Configure TTB

Operating the register must close IOMMU address mapping function, namely IOMMU_ENABLE_REG [0] is 0; or Bypass function of all masters is set to 1, or no the state of transfer bus commands.

3.12.4.4. Clear TTB

In the Flush operation, all TLB/Cache access will be suspended; but the operation entered the TLB will continue to complete before the Flush starts.

3.12.4.5. Read/Write VA Data

For virtual address, read and write the corresponding physical address data, be sure IOMMU module address mapping function is normal or not. First, make sure to read or write, and then configure the target virtual address or write data, then start to read or write function, after the operation is finished, check if the results are as expected.

3.12.4.6. PMU Statistics

When PMU function is used for the first time, set **IOMMU PMU Enable Register** to enable statistics function; when reading the relevant Register, clear the enable bit of **IOMMU PMU Enable Register**; when PMU function is used next time, first **IOMMU PMU Clear Register** is set, after counter is cleared, set the enable bit of **IOMMU PMU Enable Register**.

Given a Level2 page table administers continuous 4KB address, if Micro TLB misses in continuous virtual address, there may need to return a Level2 page table to hit from Macro TLB; but the hit number is not recorded in the Macro TLB hit and Micro TLB hit related register. So the true hit rate calculation is as follows:

Hit Rate = N1/M1 + (1-N1/M1)*N2/M2

N1: Micro TLB hit number
M1: Micro TLB access number
N2: Macro TLB hit number
M2: Macro TLB access number

3.12.5. Register List

Module Name	Base Address
IOMMU	0x030F0000

Register Name	Offset	Description
IOMMU_RESET _REG	0x0010	IOMMU ResetRegister
IOMMU_ENABLE_REG	0x0020	IOMMU EnableRegister
IOMMU_BYPASS_REG	0x0030	IOMMU BypassRegister
IOMMU_AUTO_GATING_REG	0x0040	IOMMU Auto GatingRegister
IOMMU_WBUF_CTRL_REG	0x0044	IOMMU Write Buffer Control Register
IOMMU_OOO_CTRL_REG	0x0048	IOMMU Out Of Order Control Register
IOMMU_4KB_BDY_PRT_CTRL_REG	0x004C	IOMMU 4KB Boundary Protect Control Register
IOMMU_TTB_REG	0x0050	IOMMU Translation Table BaseRegister
IOMMU_TLB_ENABLE_REG	0x0060	IOMMU TLB EnableRegister
IOMMU_TLB_PREFETCH_REG	0x0070	IOMMU TLB PrefetchRegister
IOMMU_TLB_FLUSH_ENABLE_REG	0x0080	IOMMU TLB Flush Enable Register
IOMMU_TLB_IVLD_MODE_SEL_REG	0x0084	IOMMU TLB Invalidation Mode Select Register
IOMMU_TLB_IVLD_STA_ADDR_REG	0x0088	IOMMU TLB Invalidation Start Address Register
IOMMU_TLB_IVLD_END_ADDR_REG	0x008C	IOMMU TLB Invalidation End Address Register
IOMMU_TLB_IVLD_ADDR_REG	0x0090	IOMMU TLB Invalidation Address Register
IOMMU_TLB_IVLD_ADDR_MASK_REG	0x0094	IOMMU TLB Invalidation Address Mask Register
IOMMU_TLB_IVLD_ENABLE_REG	0x0098	IOMMU TLB Invalidation Enable Register
IOMMU_PC_IVLD_ADDR_REG	0x00A0	IOMMU PC Invalidation Address Register
IOMMU_PC_IVLD_ENABLE_REG	0x00A8	IOMMU PC Invalidation Enable Register
IOMMU_DM_AUT_CTRL_REG0	0x00B0	IOMMU Domain Authority Control Register 0
IOMMU_DM_AUT_CTRL_REG1	0x00B4	IOMMU Domain Authority Control Register 1
IOMMU_DM_AUT_CTRL_REG2	0x00B8	IOMMU Domain Authority Control Register 2
IOMMU_DM_AUT_CTRL_REG3	0x00BC	IOMMU Domain Authority Control Register 3
IOMMU_DM_AUT_CTRL_REG4	0x00C0	IOMMU Domain Authority Control Register 4
IOMMU_DM_AUT_CTRL_REG5	0x00C4	IOMMU Domain Authority Control Register 5
IOMMU_DM_AUT_CTRL_REG6	0x00C8	IOMMU Domain Authority Control Register 6
IOMMU_DM_AUT_CTRL_REG7	0x00CC	IOMMU Domain Authority Control Register 7
IOMMU_DM_AUT_OVWT_REG	0x00D0	IOMMU Domain Authority Overwrite Register
IOMMU_INT_ENABLE _REG	0x0100	IOMMU Interrupt Enable Register
IOMMU_INT_CLR _REG	0x0104	IOMMU Interrupt Clear Register
IOMMU_INT_STA _REG	0x0108	IOMMU Interrupt Status Register
IOMMU_INT_ERR_ADDR_REG0	0x0110	IOMMU Interrupt Error Address Register 0
IOMMU_INT_ERR_ADDR_REG1	0x0114	IOMMU Interrupt Error Address Register 1
IOMMU_INT_ERR_ADDR_REG2	0x0118	IOMMU Interrupt Error Address Register 2
IOMMU_INT_ERR_ADDR_REG3	0x011C	IOMMU Interrupt Error Address Register 3
IOMMU_INT_ERR_ADDR_REG4	0x0120	IOMMU Interrupt Error Address Register 4
IOMMU_INT_ERR_ADDR_REG5	0x0124	IOMMU Interrupt Error Address Register 5
IOMMU_INT_ERR_ADDR_REG6	0x0128	IOMMU Interrupt Error Address Register 6
IOMMU_INT_ERR_ADDR_REG7	0x0130	IOMMU Interrupt Error Address Register 7
IOMMU_INT_ERR_ADDR_REG8	0x0134	IOMMU Interrupt Error Address Register 8
IOMMU_INT_ERR_DATA_REG0	0x0150	IOMMU Interrupt Error Data Register 0
IOMMU_INT_ERR_DATA_REG1	0x0154	IOMMU Interrupt Error Data Register 1
IOMMU_INT_ERR_DATA_REG2	0x0158	IOMMU Interrupt Error Data Register 2

IOMMU_INT_ERR_DATA_REG3	0x015C	IOMMU Interrupt Error Data Register 3
IOMMU_INT_ERR_DATA_REG4	0x0160	IOMMU Interrupt Error Data Register 4
IOMMU_INT_ERR_DATA_REG5	0x0164	IOMMU Interrupt Error Data Register 5
IOMMU_INT_ERR_DATA_REG6	0x0168	IOMMU Interrupt Error Data Register 6
IOMMU_INT_ERR_DATA_REG7	0x0170	IOMMU Interrupt Error Data Register 7
IOMMU_INT_ERR_DATA_REG8	0x0174	IOMMU Interrupt Error Data Register 8
IOMMU_L1PG_INT _REG	0x0180	IOMMU L1 Page Table Interrupt Register
IOMMU_L2PG_INT _REG	0x0184	IOMMU L2 Page Table Interrupt Register
IOMMU_VA_REG	0x0190	IOMMU Virtual Address Register
IOMMU_VA_DATA_REG	0x0194	IOMMU Virtual Address Data Register
IOMMU_VA_CONFIG_REG	0x0198	IOMMU Virtual Address Configuration Register
IOMMU_PMU_ENABLE _REG	0x0200	IOMMU PMU Enable Register
IOMMU_PMU_CLR _REG	0x0210	IOMMU PMU Clear Register
IOMMU_PMU_ACCESS_LOW_REG0	0x0230	IOMMU PMU Access Low Register 0
IOMMU_PMU_ACCESS_HIGH_REG0	0x0234	IOMMU PMU Access High Register 0
IOMMU_PMU_HIT_LOW_REG0	0x0238	IOMMU PMU Hit Low Register 0
IOMMU_PMU_HIT_HIGH_REG0	0x023C	IOMMU PMU Hit High Register 0
IOMMU_PMU_ACCESS_LOW_REG1	0x0240	IOMMU PMU Access Low Register 1
IOMMU_PMU_ACCESS_HIGH_REG1	0x0244	IOMMU PMU Access High Register 1
IOMMU_PMU_HIT_LOW_REG1	0x0248	IOMMU PMU Hit Low Register 1
IOMMU_PMU_HIT_HIGH_REG1	0x024C	IOMMU PMU Hit High Register 1
IOMMU_PMU_ACCESS_LOW_REG2	0x0250	IOMMU PMU Access Low Register 2
IOMMU_PMU_ACCESS_HIGH_REG2	0x0254	IOMMU PMU Access High Register 2
IOMMU_PMU_HIT_LOW_REG2	0x0258	IOMMU PMU Hit Low Register 2
IOMMU_PMU_HIT_HIGH_REG2	0x025C	IOMMU PMU Hit High Register 2
IOMMU_PMU_ACCESS_LOW_REG3	0x0260	IOMMU PMU Access Low Register 3
IOMMU_PMU_ACCESS_HIGH_REG3	0x0264	IOMMU PMU Access High Register 3
IOMMU_PMU_HIT_LOW_REG3	0x0268	IOMMU PMU Hit Low Register 3
IOMMU_PMU_HIT_HIGH_REG3	0x026C	IOMMU PMU Hit High Register 3
IOMMU_PMU_ACCESS_LOW_REG4	0x0270	IOMMU PMU Access Low Register 4
IOMMU_PMU_ACCESS_HIGH_REG4	0x0274	IOMMU PMU Access High Register 4
IOMMU_PMU_HIT_LOW_REG4	0x0278	IOMMU PMU Hit Low Register 4
IOMMU_PMU_HIT_HIGH_REG4	0x027C	IOMMU PMU Hit High Register 4
IOMMU_PMU_ACCESS_LOW_REG5	0x0280	IOMMU PMU Access Low Register 5
IOMMU_PMU_ACCESS_HIGH_REG5	0x0284	IOMMU PMU Access High Register 5
IOMMU_PMU_HIT_LOW_REG5	0x0288	IOMMU PMU Hit Low Register 5
IOMMU_PMU_HIT_HIGH_REG5	0x028C	IOMMU PMU Hit High Register 5
IOMMU_PMU_ACCESS_LOW_REG6	0x0290	IOMMU PMU Access Low Register 6
IOMMU_PMU_ACCESS_HIGH_REG6	0x0294	IOMMU PMU Access High Register 6
IOMMU_PMU_HIT_LOW_REG6	0x0298	IOMMU PMU Hit Low Register 6
IOMMU_PMU_HIT_HIGH_REG6	0x029C	IOMMU PMU Hit High Register 6
IOMMU_PMU_ACCESS_LOW_REG7	0x02D0	IOMMU PMU Access Low Register 7
IOMMU_PMU_ACCESS_HIGH_REG7	0x02D4	IOMMU PMU Access High Register 7
IOMMU_PMU_HIT_LOW_REG7	0x02D8	IOMMU PMU Hit Low Register 7

IOMMU_PMU_HIT_HIGH_REG7	0x02DC	IOMMU PMU Hit High Register 7
IOMMU_PMU_ACCESS_LOW_REG8	0x02E0	IOMMU PMU Access Low Register 8
IOMMU_PMU_ACCESS_HIGH_REG8	0x02E4	IOMMU PMU Access High Register 8
IOMMU_PMU_HIT_LOW_REG8	0x02E8	IOMMU PMU Hit Low Register 8
IOMMU_PMU_HIT_HIGH_REG8	0x02EC	IOMMU PMU Hit High Register 8
IOMMU_PMU_TL_LOW_REG0	0x0300	IOMMU Total Latency Low Register 0
IOMMU_PMU_TL_HIGH_REG0	0x0304	IOMMU Total Latency High Register 0
IOMMU_PMU_ML _REG0	0x0308	IOMMU Max Latency Register 0
IOMMU_PMU_TL_LOW_REG1	0x0310	IOMMU Total Latency Low Register 1
IOMMU_PMU_TL_HIGH_REG1	0x0314	IOMMU Total Latency High Register 1
IOMMU_PMU_ML _REG1	0x0318	IOMMU Max Latency Register 1
IOMMU_PMU_TL_LOW_REG2	0x0320	IOMMU Total Latency Low Register 2
IOMMU_PMU_TL_HIGH_REG2	0x0324	IOMMU Total Latency High Register 2
IOMMU_PMU_ML _REG2	0x0328	IOMMU Max Latency Register 2
IOMMU_PMU_TL_LOW_REG3	0x0330	IOMMU Total Latency Low Register 3
IOMMU_PMU_TL_HIGH_REG3	0x0334	IOMMU Total Latency High Register 3
IOMMU_PMU_ML _REG3	0x0338	IOMMU Max Latency Register 3
IOMMU_PMU_TL_LOW_REG4	0x0340	IOMMU Total Latency Low Register 4
IOMMU_PMU_TL_HIGH_REG4	0x0344	IOMMU Total Latency High Register 4
IOMMU_PMU_ML _REG4	0x0348	IOMMU Max Latency Register 4
IOMMU_PMU_TL_LOW_REG5	0x0350	IOMMU Total Latency Low Register 5
IOMMU_PMU_TL_HIGH_REG5	0x0354	IOMMU Total Latency High Register 5
IOMMU_PMU_ML _REG5	0x0358	IOMMU Max Latency Register 5
IOMMU_PMU_TL_LOW_REG6	0x0360	IOMMU Total Latency Low Register 6
IOMMU_PMU_TL_HIGH_REG6	0x0364	IOMMU Total Latency High Register 6
IOMMU_PMU_ML _REG6	0x0368	IOMMU Max Latency Register 6

3.12.6. Register Description

3.12.6.1. 0x0010 IOMMU Reset Register (Default Value: 0x8003_007F)

Offset: 0x0010			Register Name: IOMMU_RESET _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	IOMMU_RESET IOMMU Software Reset Switch 0: Set reset signal 1: Release reset signal Before IOMMU software reset operation, ensure IOMMU never be opened; Or all bus operations are completed; Or DRAM and the peripherals have opened the corresponding switch, for shielding the effects of IOMMU reset.
30:18	/	/	/
17	R/W	0x1	PTW_CACHE_RESET PTW Cache address convert lane software reset switch.

			0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used to reset PTW Cache individually.
16	R/W	0x1	MACRO_TLB_RESET Macro TLB address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When PTW Cache occurs abnormal, the bit is used to reset PTW Cache individually.
15:7	/	/	/
6	R/W	0x1	MASTER6_RESET Master6 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master6 occurs abnormal, the bit is used to reset PTW Cache individually.
5	R/W	0x1	MASTER5_RESET Master5 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master5 occurs abnormal, the bit is used to reset PTW Cache individually.
4	R/W	0x1	MASTER4_RESET Master4 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master4 occurs abnormal, the bit is used to reset PTW Cache individually.
3	R/W	0x1	MASTER3_RESET Master3 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master3 occurs abnormal, the bit is used to reset PTW Cache individually.
2	R/W	0x1	MASTER2_RESET Master2 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master2 occurs abnormal, the bit is used to reset PTW Cache individually.
1	R/W	0x1	MASTER1_RESET Master1 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal

			When Master1 occurs abnormal, the bit is used to reset PTW Cache individually.
0	R/W	0x1	MASTER0_RESET Master0 address convert lane software reset switch. 0: Set reset signal 1: Release reset signal When Master0 occurs abnormal, the bit is used to reset PTW Cache individually.

3.12.6.2. 0x0020 IOMMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: IOMMU_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ENABLE IOMMU module enable switch 0: Disable IOMMU 1: Enable IOMMU Before IOMMU address mapping function opens, configure the Translation Table Base register; or ensure all masters are in bypass status or no the status of sending bus demand(such as reset)

3.12.6.3. 0x0030 IOMMU Bypass Register (Default Value: 0x0000_007F)

Offset: 0x0030			Register Name: IOMMU_BYPASS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_BYPASS Master6 bypass switch After bypass function is opened, IOMMU can not map the address of Master6 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
5	R/W	0x1	MASTER5_BYPASS Master5 bypass switch After bypass function is opened, IOMMU can not map the address of Master5 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
4	R/W	0x1	MASTER4_BYPASS Master4 bypass switch

			After bypass function is opened, IOMMU can not map the address of Master4 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
3	R/W	0x1	MASTER3_BYPASS Master3 bypass switch After bypass function is opened, IOMMU can not map the address of Master3 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
2	R/W	0x1	MASTER2_BYPASS Master2 bypass switch After bypass function is opened, IOMMU can not map the address of Master2 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
1	R/W	0x1	MASTER1_BYPASS Master1 bypass switch After bypass function is opened, IOMMU can not map the address of Master1 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function
0	R/W	0x1	MASTER0_BYPASS Master0 bypass switch After bypass function is opened, IOMMU can not map the address of Master0 sending, and directly output the virtual address to MBUS as physical address. 0: Disable bypass function 1: Enable bypass function

NOTE

Operating the register belongs to non-accurate timing sequence control function. That is, before the function is valid, master operation will complete address mapping function, and after the operation will not perform address mapping. It is suggested that master is in reset state or in no any bus operation before operating the register .

3.12.6.4. 0x0040 IOMMU Auto Gating Register (Default Value: 0x0000_0001)

Offset: 0x0040			Register Name: IOMMU_AUTO_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

0	R/W	0x1	IOMMU_AUTO_GATING IOMMU circuit auto gating control. The purpose is decreasing power consumption of the module. 0: Disable auto gating function 1: Enable auto gating function

3.12.6.5. 0x0044 IOMMU Write Buffer Control Register (Default Value: 0x0000_0001)

Offset: 0x0044			Register Name: IOMMU_WBUF_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	MASTER0_WBUF_CTRL Master0 write buffer control bit 0: Disable write buffer 1: Enable write buffer

3.12.6.6. 0x0048 IOMMU Out Of Order Control Register (Default Value: 0x0000_007F)

Offset: 0x0048			Register Name: IOMMU_OOO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_OOO_CTRL Master6 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
5	R/W	0x1	MASTER5_OOO_CTRL Master5 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
4	R/W	0x1	MASTER4_OOO_CTRL Master4 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
3	R/W	0x1	MASTER3_OOO_CTRL Master3 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
2	R/W	0x1	MASTER2_OOO_CTRL Master2 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order **Note: AI does not support out-of-order, the bit is invalid.**

1	R/W	0x1	MASTER1_OOO_CTRL Master1 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order
0	R/W	0x1	MASTER0_OOO_CTRL Master0 out-of-order control bit 0: Disable out-of-order 1: Enable out-of-order

3.12.6.7. 0x004C IOMMU 4KB Boundary Protect Control Register (Default Value: 0x0000_007F)

Offset: 0x004C			**Register Name: IOMMU_4KB_BDY_PRT_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x1	MASTER6_4KB_BDY_PRT_CTRL Master6 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
5	R/W	0x1	MASTER5_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
4	R/W	0x1	MASTER4_4KB_BDY_PRT_CTRL Master4 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
3	R/W	0x1	MASTER3_4KB_BDY_PRT_CTRL Master3 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
2	R/W	0x1	MASTER2_4KB_BDY_PRT_CTRL Master2 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect **Note: AI does not support 4KB boundary command, the bit is invalid.**
1	R/W	0x1	MASTER1_4KB_BDY_PRT_CTRL Master1 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect
0	R/W	0x1	MASTER0_4KB_BDY_PRT_CTRL Master0 4KB boundary protect control bit 0: Disable 4KB boundary protect 1: Enable 4KB boundary protect

NOTE

When the virtual address sent by master is over the 4KB boundary, 4KB protection unit will split it into two serial access.

3.12.6.8. 0x0050 IOMMU Translation Table Base Register (Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: IOMMU_TTB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	R/W	0x0	TTB Level1 page table starting address, aligned to 16 KB. When operating the register, IOMMU address mapping function must be closed, namely IOMMU_ENABLE_REG is 0; Or Bypass function of all main equipment is set to 1, or no the state of transfer bus commands (such as setting).
13:0	/	/	/

3.12.6.9. 0x0060 IOMMU TLB Enable Register (Default Value: 0x0003_007F)

Offset: 0x0060			Register Name: IOMMU_TLB_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x1	PTW_CACHE_ENABLE PTW Cache enable bit 0: Disable 1: Enable
16	R/W	0x1	MACRO_TLB_ENABLE Macro TLB enable bit 0: Disable 1: Enable
15:7	/	/	/
6	R/W	0x1	MICRO_TLB6_ENABLE Micro TLB6 enable bit 0: Disable 1: Enable
5	R/W	0x1	MICRO_TLB5_ENABLE Micro TLB5 enable bit 0: Disable 1: Enable
4	R/W	0x1	MICRO_TLB4_ENABLE Micro TLB4 enable bit 0: Disable 1: Enable

3	R/W	0x1	MICRO_TLB3_ENABLE Micro TLB3 enable bit 0: Disable 1: Enable
2	R/W	0x1	MICRO_TLB2_ENABLE Micro TLB2 enable bit 0: Disable 1: Enable
1	R/W	0x1	MICRO_TLB1_ENABLE Micro TLB1 enable bit 0: Disable 1: Enable
0	R/W	0x1	MICRO_TLB0_ENABLE Micro TLB0 enable bit 0: Disable 1: Enable

3.12.6.10. 0x0070 IOMMU TLB Prefetch Register (Default Value: 0x0000_0000)

Offset: 0x0070			**Register Name: IOMMU_TLB_PREFETCH_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	MICRO_TLB6_PREFETCH Micro TLB6 prefetch enable 0: Disable 1: Enable **Note: When G2D accesses DDR, the prefetch function is suggested to disable.**
5	R/W	0x0	MICRO_TLB5_PREFETCH Micro TLB5 prefetch enable 0: Disable 1: Enable
4	R/W	0x0	MICRO_TLB4_PREFETCH Micro TLB4 prefetch enable 0: Disable 1: Enable
3	R/W	0x0	MICRO_TLB3_PREFETCH Micro TLB3 prefetch enable 0: Disable 1: Enable
2	R/W	0x0	MICRO_TLB2_PREFETCH Micro TLB2 prefetch enable 0: Disable 1: Enable

1	R/W	0x0	MICRO_TLB1_PREFETCH Micro TLB1 prefetch enable 0: Disable 1: Enable
0	R/W	0x0	MICRO_TLB0_PREFETCH Micro TLB0 prefetch enable 0: Disable 1: Enable

3.12.6.11. 0x0080 IOMMU TLB Flush Enable Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: IOMMU_TLB_FLUSH_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/WAC	0x0	PTW_CACHE_FLUSH Clear PTW Cache 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
16	R/WAC	0x0	MACRO_TLB_FLUSH Clear Macro TLB 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
15:7	/	/	/
6	R/WAC	0x0	MICRO_TLB6_FLUSH Clear Micro TLB6 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
5	R/WAC	0x0	MICRO_TLB5_FLUSH Clear Micro TLB5 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
4	R/WAC	0x0	MICRO_TLB4_FLUSH Clear Micro TLB4 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
3	R/WAC	0x0	MICRO_TLB3_FLUSH Clear Micro TLB3 0: No clear operation or clear operation completed 1: Enable is cleared

			After Flush operation completes, the bit can clear 0 automatically.
2	R/WAC	0x0	MICRO_TLB2_FLUSH Clear Micro TLB2 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
1	R/WAC	0x0	MICRO_TLB1_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.
0	R/WAC	0x0	MICRO_TLB0_FLUSH Clear Micro TLB1 0: No clear operation or clear operation completed 1: Enable is cleared After Flush operation completes, the bit can clear 0 automatically.

NOTE

When performing flush operation, all TLB/Cache access will be paused.

Before flush starts, the operation that has entered TLB continues to complete.

3.12.6.12. 0x0084 IOMMU TLB Invalidation Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: IOMMU_TLB_IVLD_MODE_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	TLB_IVLD_MODE_SEL 0: Use invalid TLB with Mask mode 1: Use invalid TLB with Start and End mode

3.12.6.13. 0x0088 IOMMU TLB Invalidation Start Address Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: IOMMU_TLB_IVLD_STA_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_STA_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.12.6.14. 0x008C IOMMU TLB Invalidation End Address Register (Default Value: 0x0000_0000)

Offset: 0x008C	Register Name: IOMMU_TLB_IVLD_END_ADDR_REG

Bit	Read/Write	Default/Hex	Description
31:12	R/W	0x0	TLB_IVLD_END_ADDR TLB invalid address, 4KB aligned.
11:0	/	/	/

3.12.6.15. 0x0090 IOMMU TLB Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: IOMMU_TLB_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR TLB invalid address, 4KB aligned
11:0	/	/	/

Operation:

1) Set the virtual address which needed to be operated in **IOMMU_TLB_IVLD_ADDR_REG**.
2) Set the mask of virtual address which needed to be operated in **IOMMU_TLB_IVLD_ADDR_MASK_REG**.
3) Write '1' to **IOMMU_TLB_IVLD_ENABLE_REG[0].**
4) Read **IOMMU_TLB_IVLD_ENABLE_REG[0]**, when it is '0', it indicates that invalidation behavior is finished.

NOTE

When performing invalidation operation, TLB/Cache operation has not affected.

After or Before invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.12.6.16. 0x0094 IOMMU TLB Invalidation Address Mask Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: IOMMU_TLB_IVLD_ADDR_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	TLB_IVLD_ADDR_MASK TLB invalid address mask register, 4KB aligned
11:0	/	/	/

3.12.6.17. 0x0098 IOMMU TLB Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: IOMMU_TLB_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	TLB_IVLD_ENABLE Enable TLB invalid operation 0: No-operation or operation completed 1: Enable is invalid

			After invalidation operation completed, the bit can clear 0 automatically. When operating Invalidation, TLB/Cache operation has not affected. After or Before Invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.12.6.18. 0x00A0 IOMMU PC Invalidation Address Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: IOMMU_PC_IVLD_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	R/W	0x0	PC_IVLD_ADDR PTW Cache invalid address, 1MB aligned.
19:0	/	/	/

3.12.6.19. 0x00A8 IOMMU PC Invalidation Enable Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: IOMMU_PC_IVLD_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	PC_IVLD_ENABLE Enable PTW Cache invalid operation 0: No-operation or operation completed 1: Enable is invalid After invalidation operation completed, the bit can clear 0 automatically. After or Before Invalidation starts, there is no absolute relationship between same address switch operation and Invalidation operation.

3.12.6.20. 0x00B0 IOMMU Domain Authority Control Register 0 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: IOMMU_DM_AUT_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM1_M6_WT_AUT_CTRL Domain1 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM1_M6_RD_AUT_CTRL Domain1 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM1_M5_WT_AUT_CTRL Domain1 write permission control for master5

			0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM1_M5_RD_AUT_CTRL Domain1 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM1_M4_WT_AUT_CTRL Domain1 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM1_M4_RD_AUT_CTRL Domain1 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM1_M3_WT_AUT_CTRL Domain1 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM1_M3_RD_AUT_CTRL Domain1 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM1_M2_WT_AUT_CTRL Domain1 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM1_M2_RD_AUT_CTRL Domain1 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM1_M1_WT_AUT_CTRL Domain1 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM1_M1_RD_AUT_CTRL Domain1 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM1_M0_WT_AUT_CTRL Domain1 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM1_M0_RD_AUT_CTRL Domain1 read permission control for master0 0: The read-operation is available

			1: The read-operation is unavailable
15:14	/	/	/
13	R	0x0	DM0_M6_WT_AUT_CTRL Domain0 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
12	R	0x0	DM0_M6_RD_AUT_CTRL Domain0 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R	0x0	DM0_M5_WT_AUT_CTRL Domain0 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R	0x0	DM0_M5_RD_AUT_CTRL Domain0 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R	0x0	DM0_M4_WT_AUT_CTRL Domain0 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R	0x0	DM0_M4_RD_AUT_CTRL Domain0 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R	0x0	DM0_M3_WT_AUT_CTRL Domain0 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R	0x0	DM0_M3_RD_AUT_CTRL Domain0 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R	0x0	DM0_M2_WT_AUT_CTRL Domain0 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R	0x0	DM0_M2_RD_AUT_CTRL Domain0 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R	0x0	DM0_M1_WT_AUT_CTRL Domain0 write permission control for master1 0: The write-operation is available

			1: The write-operation is unavailable
2	R	0x0	DM0_M1_RD_AUT_CTRL Domain0 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R	0x0	DM0_M0_WT_AUT_CTRL Domain0 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R	0x0	DM0_M0_RD_AUT_CTRL Domain0 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

NOTE

Software can be set up 15 different permission control types , which are set in IOMMU_DM_AUT_CTRL_REG0 ~ 7. As well as a default access control type, domain0. The read/write operation of DOMIAN1 ~ 15 is unlimited by default.

Software needs to set the corresponding permission control domain index of the page table item in the secondary page table entries[7:4], the default value is 0, use domian0, namely the read/write operation is not controlled.

Setting REG_ARD_OVWT can mask Domain control defined by IOMMU_DM_AUT_CTRL_REG0~7. All Level2 page table type are covered by the type of REG_ARD_OVWT. The read/write operation is permitted by default.

3.12.6.21. 0x00B4 IOMMU Domain Authority Control Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: IOMMU_DM_AUT_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM3_M6_WT_AUT_CTRL Domain3 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM3_M6_RD_AUT_CTRL Domain3 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM3_M5_WT_AUT_CTRL Domain3 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM3_M5_RD_AUT_CTRL Domain3 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable

25	R/W	0x0	DM3_M4_WT_AUT_CTRL Domain3 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM3_M4_RD_AUT_CTRL Domain3 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM3_M3_WT_AUT_CTRL Domain3 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM3_M3_RD_AUT_CTRL Domain3 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM3_M2_WT_AUT_CTRL Domain3 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM3_M2_RD_AUT_CTRL Domain3 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM3_M1_WT_AUT_CTRL Domain3 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM3_M1_RD_AUT_CTRL Domain3 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM3_M0_WT_AUT_CTRL Domain3 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM3_M0_RD_AUT_CTRL Domain3 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM2_M6_WT_AUT_CTRL Domain2 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable

12	R/W	0x0	DM2_M6_RD_AUT_CTRL Domain2 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM2_M5_WT_AUT_CTRL Domain2 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM2_M5_RD_AUT_CTRL Domain2 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM2_M4_WT_AUT_CTRL Domain2 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM2_M4_RD_AUT_CTRL Domain2 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM2_M3_WT_AUT_CTRL Domain2 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM2_M3_RD_AUT_CTRL Domain2 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM2_M2_WT_AUT_CTRL Domain2 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM2_M2_RD_AUT_CTRL Domain2 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM2_M1_WT_AUT_CTRL Domain2 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM2_M1_RD_AUT_CTRL Domain2 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM2_M0_WT_AUT_CTRL

			Domain2 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM2_M0_RD_AUT_CTRL Domain2 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.22. 0x00B8 IOMMU Domain Authority Control Register 2 (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: IOMMU_DM_AUT_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM5_M6_WT_AUT_CTRL Domain5 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM5_M6_RD_AUT_CTRL Domain5 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM5_M5_WT_AUT_CTRL Domain5 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM5_M5_RD_AUT_CTRL Domain5 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM5_M4_WT_AUT_CTRL Domain5 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM5_M4_RD_AUT_CTRL Domain5 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM5_M3_WT_AUT_CTRL Domain5 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM5_M3_RD_AUT_CTRL Domain5 read permission control for master3 0: The read-operation is available

			1: The read-operation is unavailable
21	R/W	0x0	DM5_M2_WT_AUT_CTRL Domain5 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM5_M2_RD_AUT_CTRL Domain5 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM5_M1_WT_AUT_CTRL Domain5 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM5_M1_RD_AUT_CTRL Domain5 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM5_M0_WT_AUT_CTRL Domain5 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM5_M0_RD_AUT_CTRL Domain5 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM4_M6_WT_AUT_CTRL Domain4 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
12	R/W	0x0	DM4_M6_RD_AUT_CTRL Domain4 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM4_M5_WT_AUT_CTRL Domain4 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM4_M5_RD_AUT_CTRL Domain4 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM4_M4_WT_AUT_CTRL Domain4 write permission control for master4 0: The write-operation is available

			1: The write-operation is unavailable
8	R/W	0x0	DM4_M4_RD_AUT_CTRL Domain4 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM4_M3_WT_AUT_CTRL Domain4 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM4_M3_RD_AUT_CTRL Domain4 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM4_M2_WT_AUT_CTRL Domain4 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM4_M2_RD_AUT_CTRL Domain4 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM4_M1_WT_AUT_CTRL Domain4 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM4_M1_RD_AUT_CTRL Domain4 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM4_M0_WT_AUT_CTRL Domain4 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM4_M0_RD_AUT_CTRL Domain4 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.23. 0x00BC IOMMU Domain Authority Control Register 3 (Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: IOMMU_DM_AUT_CTRL_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM7_M6_WT_AUT_CTRL

			Domain7 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM7_M6_RD_AUT_CTRL Domain7 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM7_M5_WT_AUT_CTRL Domain7 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM7_M5_RD_AUT_CTRL Domain7 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM7_M4_WT_AUT_CTRL Domain7 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM7_M4_RD_AUT_CTRL Domain7 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM7_M3_WT_AUT_CTRL Domain7 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM7_M3_RD_AUT_CTRL Domain7 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM7_M2_WT_AUT_CTRL Domain7 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM7_M2_RD_AUT_CTRL Domain7 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM7_M1_WT_AUT_CTRL Domain7 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM7_M1_RD_AUT_CTRL Domain7 read permission control for master1

			0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM7_M0_WT_AUT_CTRL Domain7 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM7_M0_RD_AUT_CTRL Domain7 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM6_M6_WT_AUT_CTRL Domain6 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
12	R/W	0x0	DM6_M6_RD_AUT_CTRL Domain6 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM6_M5_WT_AUT_CTRL Domain6 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM6_M5_RD_AUT_CTRL Domain6 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM6_M4_WT_AUT_CTRL Domain6 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM6_M4_RD_AUT_CTRL Domain6 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM6_M3_WT_AUT_CTRL Domain6 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM6_M3_RD_AUT_CTRL Domain6 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM6_M2_WT_AUT_CTRL Domain6 write permission control for master2

			0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM6_M2_RD_AUT_CTRL Domain6 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM6_M1_WT_AUT_CTRL Domain6 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM6_M1_RD_AUT_CTRL Domain6 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM6_M0_WT_AUT_CTRL Domain6 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM6_M0_RD_AUT_CTRL Domain6 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.24. 0x00C0 IOMMU Domain Authority Control Register 4 (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: IOMMU_DM_AUT_CTRL_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM9_M6_WT_AUT_CTRL Domain9 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM9_M6_RD_AUT_CTRL Domain9 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM9_M5_WT_AUT_CTRL Domain9 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM9_M5_RD_AUT_CTRL Domain9 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable

25	R/W	0x0	DM9_M4_WT_AUT_CTRL Domain9 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM9_M4_RD_AUT_CTRL Domain9 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM9_M3_WT_AUT_CTRL Domain9 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM9_M3_RD_AUT_CTRL Domain9 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM9_M2_WT_AUT_CTRL Domain9 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM9_M2_RD_AUT_CTRL Domain9 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM9_M1_WT_AUT_CTRL Domain9 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM9_M1_RD_AUT_CTRL Domain9 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM9_M0_WT_AUT_CTRL Domain9 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM9_M0_RD_AUT_CTRL Domain9 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM8_M6_WT_AUT_CTRL Domain8 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable

12	R/W	0x0	DM8_M6_RD_AUT_CTRL Domain8 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM8_M5_WT_AUT_CTRL Domain8 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM8_M5_RD_AUT_CTRL Domain8 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM8_M4_WT_AUT_CTRL Domain8 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM8_M4_RD_AUT_CTRL Domain8 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM8_M3_WT_AUT_CTRL Domain8 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM8_M3_RD_AUT_CTRL Domain8 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM8_M2_WT_AUT_CTRL Domain8 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM8_M2_RD_AUT_CTRL Domain8 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM8_M1_WT_AUT_CTRL Domain8 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM8_M1_RD_AUT_CTRL Domain8 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM8_M0_WT_AUT_CTRL

			Domain8 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM8_M0_RD_AUT_CTRL Domain8 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.25. 0x00C4 IOMMU Domain Authority Control Register 5 (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: IOMMU_DM_AUT_CTRL_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM11_M6_WT_AUT_CTRL Domain11 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM11_M6_RD_AUT_CTRL Domain11 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM11_M5_WT_AUT_CTRL Domain11 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM11_M5_RD_AUT_CTRL Domain11 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM11_M4_WT_AUT_CTRL Domain11 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM11_M4_RD_AUT_CTRL Domain11 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM11_M3_WT_AUT_CTRL Domain11 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM11_M3_RD_AUT_CTRL Domain11 read permission control for master3 0: The read-operation is available

			1: The read-operation is unavailable
21	R/W	0x0	DM11_M2_WT_AUT_CTRL Domain11 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM11_M2_RD_AUT_CTRL Domain11 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM11_M1_WT_AUT_CTRL Domain11 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM11_M1_RD_AUT_CTRL Domain11 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM11_M0_WT_AUT_CTRL Domain11 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM11_M0_RD_AUT_CTRL Domain11 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM10_M6_WT_AUT_CTRL Domain10 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
12	R/W	0x0	DM10_M6_RD_AUT_CTRL Domain10 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM10_M5_WT_AUT_CTRL Domain10 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM10_M5_RD_AUT_CTRL Domain10 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM10_M4_WT_AUT_CTRL Domain10 write permission control for master4 0: The write-operation is available

			1: The write-operation is unavailable
8	R/W	0x0	DM10_M4_RD_AUT_CTRL Domain10 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM10_M3_WT_AUT_CTRL Domain10 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM10_M3_RD_AUT_CTRL Domain10 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM10_M2_WT_AUT_CTRL Domain10 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM10_M2_RD_AUT_CTRL Domain10 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM10_M1_WT_AUT_CTRL Domain10 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM10_M1_RD_AUT_CTRL Domain10 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM10_M0_WT_AUT_CTRL Domain10 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM10_M0_RD_AUT_CTRL Domain10 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.26. 0x00C8 IOMMU Domain Authority Control Register 6 (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: IOMMU_DM_AUT_CTRL_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM13_M6_WT_AUT_CTRL

			Domain13 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM13_M6_RD_AUT_CTRL Domain13 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM13_M5_WT_AUT_CTRL Domain13 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM13_M5_RD_AUT_CTRL Domain13 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
25	R/W	0x0	DM13_M4_WT_AUT_CTRL Domain13 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM13_M4_RD_AUT_CTRL Domain13 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM13_M3_WT_AUT_CTRL Domain13 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM13_M3_RD_AUT_CTRL Domain13 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM13_M2_WT_AUT_CTRL Domain13 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM13_M2_RD_AUT_CTRL Domain13 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM13_M1_WT_AUT_CTRL Domain13 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM13_M1_RD_AUT_CTRL Domain13 read permission control for master1

			0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM13_M0_WT_AUT_CTRL Domain13 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM13_M0_RD_AUT_CTRL Domain13 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM12_M6_WT_AUT_CTRL Domain12 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
12	R/W	0x0	DM12_M6_RD_AUT_CTRL Domain12 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM12_M5_WT_AUT_CTRL Domain12 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM12_M5_RD_AUT_CTRL Domain12 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM12_M4_WT_AUT_CTRL Domain12 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM12_M4_RD_AUT_CTRL Domain12 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM12_M3_WT_AUT_CTRL Domain12 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM12_M3_RD_AUT_CTRL Domain12 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM12_M2_WT_AUT_CTRL Domain12 write permission control for master2

			0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM12_M2_RD_AUT_CTRL Domain12 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM12_M1_WT_AUT_CTRL Domain12 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM12_M1_RD_AUT_CTRL Domain12 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM12_M0_WT_AUT_CTRL Domain12 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM12_M0_RD_AUT_CTRL Domain12 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.27. 0x00CC IOMMU Domain Authority Control Register 7 (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: IOMMU_DM_AUT_CTRL_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	DM15_M6_WT_AUT_CTRL Domain15 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable
28	R/W	0x0	DM15_M6_RD_AUT_CTRL Domain15 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
27	R/W	0x0	DM15_M5_WT_AUT_CTRL Domain15 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
26	R/W	0x0	DM15_M5_RD_AUT_CTRL Domain15 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable

25	R/W	0x0	DM15_M4_WT_AUT_CTRL Domain15 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
24	R/W	0x0	DM15_M4_RD_AUT_CTRL Domain15 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
23	R/W	0x0	DM15_M3_WT_AUT_CTRL Domain15 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
22	R/W	0x0	DM15_M3_RD_AUT_CTRL Domain15 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
21	R/W	0x0	DM15_M2_WT_AUT_CTRL Domain15 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
20	R/W	0x0	DM15_M2_RD_AUT_CTRL Domain15 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
19	R/W	0x0	DM15_M1_WT_AUT_CTRL Domain15 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
18	R/W	0x0	DM15_M1_RD_AUT_CTRL Domain15 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
17	R/W	0x0	DM15_M0_WT_AUT_CTRL Domain15 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
16	R/W	0x0	DM15_M0_RD_AUT_CTRL Domain15 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable
15:14	/	/	/
13	R/W	0x0	DM14_M6_WT_AUT_CTRL Domain14 write permission control for master6 0: The write-operation is available 1: The write-operation is unavailable

12	R/W	0x0	DM14_M6_RD_AUT_CTRL Domain14 read permission control for master6 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	DM14_M5_WT_AUT_CTRL Domain14 write permission control for master5 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	DM14_M5_RD_AUT_CTRL Domain14 read permission control for master5 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	DM14_M4_WT_AUT_CTRL Domain14 write permission control for master4 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	DM14_M4_RD_AUT_CTRL Domain14 read permission control for master4 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	DM14_M3_WT_AUT_CTRL Domain14 write permission control for master3 0: The write-operation is available 1: The write-operation is unavailable
6	R/W	0x0	DM14_M3_RD_AUT_CTRL Domain14 read permission control for master3 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	DM14_M2_WT_AUT_CTRL Domain14 write permission control for master2 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	DM14_M2_RD_AUT_CTRL Domain14 read permission control for master2 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	DM14_M1_WT_AUT_CTRL Domain14 write permission control for master1 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	DM14_M1_RD_AUT_CTRL Domain14 read permission control for master1 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	DM14_M0_WT_AUT_CTRL

			Domain14 write permission control for master0 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	DM14_M0_RD_AUT_CTRL Domain14 read permission control for master0 0: The read-operation is available 1: The read-operation is unavailable

3.12.6.28. 0x00D0 IOMMU Domain Authority Overwrite Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: IOMMU_DM_AUT_OVWT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DM_AUT_OVWT_ENABLE Domain write/read permission overwrite enable 0: Disable 1: Enable
30:14	/	/	/
13	R/W	0x0	M6_WT_AUT_OVWT_CTRL Master6 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
12	R/W	0x0	M6_RD_AUT_OVWT_CTRL Master6 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
11	R/W	0x0	M5_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
10	R/W	0x0	M5_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
9	R/W	0x0	M4_WT_AUT_OVWT_CTRL Master5 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
8	R/W	0x0	M4_RD_AUT_OVWT_CTRL Master5 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
7	R/W	0x0	M3_WT_AUT_OVWT_CTRL Master3 write permission overwrite control 0: The write-operation is available

			1: The write-operation is unavailable
6	R/W	0x0	M3_RD_AUT_OVWT_CTRL Master3 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
5	R/W	0x0	M2_WT_AUT_OVWT_CTRL Master2 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
4	R/W	0x0	M2_RD_AUT_OVWT_CTRL Master2 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
3	R/W	0x0	M1_WT_AUT_OVWT_CTRL Master1 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
2	R/W	0x0	M1_RD_AUT_OVWT_CTRL Master1 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable
1	R/W	0x0	M0_WT_AUT_OVWT_CTRL Master0 write permission overwrite control 0: The write-operation is available 1: The write-operation is unavailable
0	R/W	0x0	M0_RD_AUT_OVWT_CTRL Master0 read permission overwrite control 0: The read-operation is available 1: The read-operation is unavailable

Setting the **REG_ARD_OVWT** can mask the Domain control defined by **IOMMU_DM_AUT_CTRL_REG0~7.** All the property of Level2 are covered by the property defined in **REG_ARD_OVWT.** Allow read and write for all by default.

3.12.6.29. 0x0100 IOMMU Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x0100			**Register Name: IOMMU_INT_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	L2_PAGE_TABLE_INVALID_EN Level2 page table invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
16	R/W	0x0	L1_PAGE_TABLE_INVALID_EN Level1 page table invalid interrupt enable 0: Mask interrupt

			1: Enable interrupt
15:7	/	/	/
6	R/W	0x0	MICRO_TLB6_INVALID_EN Micro TLB6 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
5	R/W	0x0	MICRO_TLB5_INVALID_EN Micro TLB5 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
4	R/W	0x0	MICRO_TLB4_INVALID_EN Micro TLB4 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
3	R/W	0x0	MICRO_TLB3_INVALID_EN Micro TLB3 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
2	R/W	0x0	MICRO_TLB2_INVALID_EN Micro TLB2 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
1	R/W	0x0	MICRO_TLB1_INVALID_EN Micro TLB1 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt
0	R/W	0x0	MICRO_TLB0_INVALID_EN Micro TLB0 permission invalid interrupt enable 0: Mask interrupt 1: Enable interrupt

NOTE

Invalid page table and permission error can not make one device or multi-devices in system work normally.

Permission error usually happens in MicroTLB. The error generates interrupt, and waits for processing through software.

Invalid page table usually happens in MacroTLB. The error can not influence the access of other devices. So the error page table needs go back the way it comes, but the error should not be written in each level TLB.

3.12.6.30. 0x0104 IOMMU Interrupt Clear Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: IOMMU_INT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	W	0x0	L2_PAGE_TABLE_INVALID_CLR

			Level2 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
16	W	0x0	L1_PAGE_TABLE_INVALID_CLR Level1 page table invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
15:7	/	/	/
6	W	0x0	MICRO_TLB6_INVALID_CLR Micro TLB6 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
5	W	0x0	MICRO_TLB5_INVALID_CLR Micro TLB5 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
4	W	0x0	MICRO_TLB4_INVALID_CLR Micro TLB4 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
3	W	0x0	MICRO_TLB3_INVALID_CLR Micro TLB3 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
2	W	0x0	MICRO_TLB2_INVALID_CLR Micro TLB2 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
1	W	0x0	MICRO_TLB1_INVALID_CLR Micro TLB1 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt
0	W	0x0	MICRO_TLB0_INVALID_CLR Micro TLB0 permission invalid interrupt clear bit 0: Invalid operation 1: Clear interrupt

3.12.6.31. 0x0108 IOMMU Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: IOMMU_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R	0x0	L2_PAGE_TABLE_INVALID_STA Level2 page table invalid interrupt status bit

			0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
16	R	0x0	L1_PAGE_TABLE_INVALID_STA Level1 page table invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
15:7	/	/	/
6	R	0x0	MICRO_TLB6_INVALID_STA Micro TLB6 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
5	R	0x0	MICRO_TLB5_INVALID_STA Micro TLB5 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
4	R	0x0	MICRO_TLB4_INVALID_STA Micro TLB4 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
3	R	0x0	MICRO_TLB3_INVALID_STA Micro TLB3 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
2	R	0x0	MICRO_TLB2_INVALID_STA Micro TLB2 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
1	R	0x0	MICRO_TLB1_INVALID_STA Micro TLB1 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens
0	R	0x0	MICRO_TLB0_INVALID_STA Micro TLB0 permission invalid interrupt status bit 0: Interrupt does not happen or interrupt is cleared 1: Interrupt happens

3.12.6.32. 0x0110 IOMMU Interrupt Error Address Register 0 (Default Value: 0x0000_0000)

Offset: 0x0110			**Register Name: IOMMU_INT_ERR_ADDR_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR0 Virtual address that caused Micro TLB0 to interrupt

3.12.6.33. 0x0114 IOMMU Interrupt Error Address Register 1 (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: IOMMU_INT_ERR_ADDR_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR1 Virtual address that caused Micro TLB1 to interrupt

3.12.6.34. 0x0118 IOMMU Interrupt Error Address Register 2 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: IOMMU_INT_ERR_ADDR_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR2 Virtual address that caused Micro TLB2 to interrupt

3.12.6.35. 0x011C IOMMU Interrupt Error Address Register 3 (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: IOMMU_INT_ERR_ADDR_REG3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR3 Virtual address that caused Micro TLB3 to interrupt

3.12.6.36. 0x0120 IOMMU Interrupt Error Address Register 4 (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: IOMMU_INT_ERR_ADDR_REG4
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR4 Virtual address that caused Micro TLB4 to interrupt

3.12.6.37. 0x0124 IOMMU Interrupt Error Address Register 5 (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: IOMMU_INT_ERR_ADDR_REG5
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_ERR_ADDR5 Virtual address that caused Micro TLB5 to interrupt

3.12.6.38. 0x0128 IOMMU Interrupt Error Address Register 6 (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: IOMMU_INT_ERR_ADDR_REG6
Bit	Read/Write	Default/Hex	Description

31:0	R	0x0	INT_ERR_ADDR6 Virtual address that caused Micro TLB6 to interrupt

3.12.6.39. 0x0130 IOMMU Interrupt Error Address Register 7 (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: IOMMU_INT_ERR_ADDR_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR7 Virtual address that caused L1 page table to interrupt

3.12.6.40. 0x0134 IOMMU Interrupt Error Address Register 8 (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: IOMMU_INT_ERR_ADDR_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_ADDR8 Virtual address that caused L2 page table to interrupt

3.12.6.41. 0x0150 IOMMU Interrupt Error Data Register 0 (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: IOMMU_INT_ERR_DATA_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA0 Corresponding page table of virtual address that caused Micro TLB0 to interrupt

3.12.6.42. 0x0154 IOMMU Interrupt Error Data Register 1 (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: IOMMU_INT_ERR_DATA_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA1 Corresponding page table of virtual address that caused Micro TLB1 to interrupt

3.12.6.43. 0x0158 IOMMU Interrupt Error Data Register 2 (Default Value: 0x0000_0000)

Offset: 0x0158			Register Name: IOMMU_INT_ERR_DATA_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA2 Corresponding page table of virtual address that caused Micro TLB2 to

			interrupt

3.12.6.44. 0x015C IOMMU Interrupt Error Data Register 3 (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: IOMMU_INT_ERR_DATA_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA3 Corresponding page table of virtual address that caused Micro TLB3 to interrupt

3.12.6.45. 0x0160 IOMMU Interrupt Error Data Register 4 (Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: IOMMU_INT_ERR_DATA_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA4 Corresponding page table of virtual address that caused Micro TLB4 to interrupt

3.12.6.46. 0x0164 IOMMU Interrupt Error Data Register 5 (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: IOMMU_INT_ERR_DATA_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA5 Corresponding page table of virtual address that caused Micro TLB5 to interrupt

3.12.6.47. 0x0168 IOMMU Interrupt Error Data Register 6 (Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: IOMMU_INT_ERR_DATA_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA6 Corresponding page table of virtual address that caused Micro TLB6 to interrupt

3.12.6.48. 0x0170 IOMMU Interrupt Error Data Register 7 (Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: IOMMU_INT_ERR_DATA_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA7

			Corresponding page table of virtual address that caused L1 page table to interrupt

3.12.6.49. 0x0174 IOMMU Interrupt Error Data Register 8 (Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: IOMMU_INT_ERR_DATA_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	INT_ERR_DATA8 Corresponding page table of virtual address that caused L2 page table to interrupt

3.12.6.50. 0x0180 IOMMU L1 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: IOMMU_L1PG_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DBG_MODE_L1PG_INT Debug mode address switch causes L1 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L1PG_INT Master6 address switch causes L1 page table to occur interrupt.
5	R	0x0	MASTER5_L1PG_INT Master5 address switch causes L1 page table to occur interrupt.
4	R	0x0	MASTER4_L1PG_INT Master4 address switch causes L1 page table to occur interrupt.
3	R	0x0	MASTER3_L1PG_INT Master3 address switch causes L1 page table to occur interrupt.
2	R	0x0	MASTER2_L1PG_INT Master2 address switch causes L1 page table to occur interrupt.
1	R	0x0	MASTER1_L1PG_INT Master1 address switch causes L1 page table to occur interrupt.
0	R	0x0	MASTER0_L1PG_INT Master0 address switch causes L1 page table to occur interrupt.

3.12.6.51. 0x0184 IOMMU L2 Page Table Interrupt Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: IOMMU_L2PG_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DBG_MODE_L2PG_INT Debug mode address switch causes L2 page table to occur interrupt.
30:7	/	/	/
6	R	0x0	MASTER6_L2PG_INT

			Master6 address switch causes L2 page table to occur interrupt.
5	R	0x0	MASTER5_L2PG_INT Master5 address switch causes L2 page table to occur interrupt.
4	R	0x0	MASTER4_L2PG_INT Master4 address switch causes L2 page table to occur interrupt.
3	R	0x0	MASTER3_L2PG_INT Master3 address switch causes L2 page table to occur interrupt.
2	R	0x0	MASTER2_L2PG_INT Master2 address switch causes L2 page table to occur interrupt.
1	R	0x0	MASTER1_L2PG_INT Master1 address switch causes L2 page table to occur interrupt.
0	R	0x0	MASTER0_L2PG_INT Master0 address switch causes L2 page table to occur interrupt.

3.12.6.52. 0x0190 IOMMU Virtual Address Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: IOMMU_VA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA Virtual address of read/write

3.12.6.53. 0x0194 IOMMU Virtual Address Data Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: IOMMU_VA_DATA _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VA_DATA Data of read/write virtual address

3.12.6.54. 0x0198 IOMMU Virtual Address Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: IOMMU_VA_CONFIG _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MODE_SEL 0: Prefetch 1: Debug Mode It is used to chose prefetch mode or Debug mode.
31:9	/	/	/
8	R/W	0x0	VA_CONFIG 0: Read operation 1: Write operation
7:1	/	/	/

0	R/WAC	0x0	VA_CONFIG_START 0: No operation or operation completes 1: Start After the operation completes, the bit can clear to 0 automatically.

Read operation process:

a) Write IOMMU_VA_REG[31:0];

b) Write IOMMU_VA_CONFIG _REG[8] to 0;

c) Write IOMMU_VA_CONFIG _REG[0] to 1, start read-process;

d) Query IOMMU_VA_CONFIG _REG[0], until it is 0;

e) Read IOMMU_VA_DATA _REG[31:0];

Write operation process:

a) Write IOMMU_VA _REG[31:0];

b) Write IOMMU_VA_DATA _REG[31:0];

c) Write IOMMU_VA_CONFIG _REG[8] to 1;

d) Write IOMMU_VA_CONFIG _REG[0] to 1, start write-process;

e) Query IOMMU_VA_CONFIG _REG[0], until it is 0;

3.12.6.55. 0x0200 IOMMU PMU Enable Register (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: IOMMU_PMU_ENABLE _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PMU_ENABLE 0: Disable statistical function 1: Enable statistical function

3.12.6.56. 0x0210 IOMMU PMU Clear Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: IOMMU_PMU_CLR _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	PMU_CLR 0: No clear operation or clear operation completes 1: Clear counter data After the operation completes, the bit can clear to 0 automatically.

3.12.6.57. 0x0230 IOMMU PMU Access Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0230			Register Name: IOMMU_PMU_ACCESS_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW0

			Record total number of Micro TLB0 access , lower 32-bit register

3.12.6.58. 0x0234 IOMMU PMU Access High Register 0 (Default Value: 0x0000_0000)

Offset: 0x0234			Register Name: IOMMU_PMU_ACCESS_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH0 Record total number of Micro TLB0 access , higher 11-bit register

3.12.6.59. 0x0238 IOMMU PMU Hit Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0238			Register Name: IOMMU_PMU_HIT_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW0 Record total number of Micro TLB0 hit , lower 32-bit register

3.12.6.60. 0x023C IOMMU PMU Hit High Register 0 (Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: IOMMU_PMU_HIT_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH0 Record total number of Micro TLB0 hit , higher 11-bit register

3.12.6.61. 0x0240 IOMMU PMU Access Low Register 1 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: IOMMU_PMU_ACCESS_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW1 Record total number of Micro TLB1 access , lower 32-bit register

3.12.6.62. 0x0244 IOMMU PMU Access High Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: IOMMU_PMU_ACCESS_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH1 Record total number of Micro TLB1 access , higher 11-bit register

3.12.6.63. 0x0248 IOMMU PMU Hit Low Register 1 (Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: IOMMU_PMU_HIT_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW1 Record total number of Micro TLB1 hit , lower 32-bit register

3.12.6.64. 0x024C IOMMU PMU Hit High Register 1 (Default Value: 0x0000_0000)

Offset: 0x024C			Register Name: IOMMU_PMU_HIT_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH1 Record total number of Micro TLB1 hit , higher 11-bit register

3.12.6.65. 0x0250 IOMMU PMU Access Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: IOMMU_PMU_ACCESS_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW2 Record total number of Micro TLB2 access , lower 32-bit register

3.12.6.66. 0x0254 IOMMU PMU Access High Register 2 (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: IOMMU_PMU_ACCESS_HIGH_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH2 Record total number of Micro TLB2 access , higher 11-bit register

3.12.6.67. 0x0258 IOMMU PMU Hit Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: IOMMU_PMU_HIT_LOW_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW2 Record total number of Micro TLB2 hit , lower 32-bit register

3.12.6.68. 0x025C IOMMU PMU Hit High Register 2 (Default Value: 0x0000_0000)

Offset: 0x025C			Register Name: IOMMU_PMU_HIT_HIGH_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH2 Record total number of Micro TLB2 hit , higher 11-bit register

3.12.6.69. 0x0260 IOMMU PMU Access Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: IOMMU_PMU_ACCESS_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW3 Record total number of Micro TLB3 access, lower 32-bit register

3.12.6.70. 0x0264 IOMMU PMU Access High Register 3 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: IOMMU_PMU_ACCESS_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH3 Record total number of Micro TLB3 access , higher 11-bit register

3.12.6.71. 0x0268 IOMMU PMU Hit Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: IOMMU_PMU_HIT_LOW_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW3 Record total number of Micro TLB3 hit, lower 32-bit register

3.12.6.72. 0x026C IOMMU PMU Hit High Register 3 (Default Value: 0x0000_0000)

Offset: 0x026C			Register Name: IOMMU_PMU_HIT_HIGH_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH3 Record total number of Micro TLB3 hit , higher 11-bit register

3.12.6.73. 0x0270 IOMMU PMU Access Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: IOMMU_PMU_ACCESS_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW4 Record total number of Micro TLB4 access, lower 32-bit register

3.12.6.74. 0x0274 IOMMU PMU Access High Register 4 (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: IOMMU_PMU_ACCESS_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH4 Record total number of Micro TLB4 access, higher 11-bit register

3.12.6.75. 0x0278 IOMMU PMU Hit Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: IOMMU_PMU_HIT_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW4 Record total number of Micro TLB4 hit, lower 32-bit register

3.12.6.76. 0x027C IOMMU PMU Hit High Register 4 (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: IOMMU_PMU_HIT_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH4 Record total number of Micro TLB4 hit, higher 11-bit register

3.12.6.77. 0x0280 IOMMU PMU Access Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: IOMMU_PMU_ACCESS_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW5 Record total number of Micro TLB5 access, lower 32-bit register

3.12.6.78. 0x0284 IOMMU PMU Access High Register 5 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: IOMMU_PMU_ACCESS_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH5 Record total number of Micro TLB5 access, higher 11-bit register

3.12.6.79. 0x0288 IOMMU PMU Hit Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: IOMMU_PMU_HIT_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW5 Record total number of Micro TLB5 hit, lower 32-bit register

3.12.6.80. 0x028C IOMMU PMU Hit High Register 5 (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: IOMMU_PMU_HIT_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH5 Record total number of Micro TLB5 hit, higher 11-bit register

3.12.6.81. 0x0290 IOMMU PMU Access Low Register6 (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: IOMMU_PMU_ACCESS_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW6 Record total number of Micro TLB6 access, lower 32-bit register

3.12.6.82. 0x0294 IOMMU PMU Access High Register 6 (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: IOMMU_PMU_ACCESS_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH6 Record total number of Micro TLB6 access, higher 11-bit register

3.12.6.83. 0x0298 IOMMU PMU Hit Low Register 6 (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: IOMMU_PMU_HIT_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW6 Record total number of Micro TLB6 hit, lower 32-bit register

3.12.6.84. 0x029C IOMMU PMU Hit High Register 6 (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: IOMMU_PMU_HIT_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH6 Record total number of Micro TLB6 hit, higher 11-bit register

3.12.6.85. 0x02D0 IOMMU PMU Access Low Register 7 (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: IOMMU_PMU_ACCESS_LOW_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW7 Record total number of Micro TLB7 access, lower 32-bit register

3.12.6.86. 0x02D4 IOMMU PMU Access High Register 7 (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: IOMMU_PMU_ACCESS_HIGH_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH7 Record total number of Micro TLB7 access, higher 11-bit register

3.12.6.87. 0x02D8 IOMMU PMU Hit Low Register 7 (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: IOMMU_PMU_HIT_LOW_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW7 Record total number of Micro TLB7 hit, lower 32-bit register

3.12.6.88. 0x02DC IOMMU PMU Hit High Register 7 (Default Value: 0x0000_0000)

Offset: 0x02DC			Register Name: IOMMU_PMU_HIT_HIGH_REG7
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH7 Record total number of Micro TLB7 hit, higher 11-bit register

3.12.6.89. 0x02E0 IOMMU PMU Access Low Register 8 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name: IOMMU_PMU_ACCESS_LOW_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ACCESS_LOW8 Record total number of PTW Cache access, lower 32-bit register

3.12.6.90. 0x02E4 IOMMU PMU Access High Register 8 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: IOMMU_PMU_ACCESS_HIGH_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_ACCESS_HIGH8 Record total number of PTW Cache access, higher 11-bit register

3.12.6.91. 0x02E8 IOMMU PMU Hit Low Register 8 (Default Value: 0x0000_0000)

Offset: 0x02E8			Register Name: IOMMU_PMU_HIT_LOW_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_HIT_LOW8 Record total number of PTW Cache hit, lower 32-bit register

3.12.6.92. 0x02EC IOMMU PMU Hit High Register 8 (Default Value: 0x0000_0000)

Offset: 0x02EC			Register Name: IOMMU_PMU_HIT_HIGH_REG8
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R	0x0	PMU_HIT_HIGH8 Record total number of PTW Cache hit, higher 11-bit register

3.12.6.93. 0x0300 IOMMU Total Latency Low Register 0 (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: IOMMU_PMU_TL_LOW_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW0 Record total latency of Master0, lower 32-bit register

3.12.6.94. 0x0304 IOMMU Total Latency High Register 0 (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: IOMMU_PMU_TL_HIGH_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH0 Record total latency of Master0, higher 18-bit register

3.12.6.95. 0x0308 IOMMU Max Latency Register 0 (Default Value: 0x0000_0000)

Offset: 0x0308			Register Name: IOMMU_PMU_ML_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML0 Record the max latency of Master0.

3.12.6.96. 0x0310 IOMMU Total Latency Low Register 1(Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: IOMMU_PMU_TL_LOW_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW1 Record total latency of Master1, lower 32-bit register

3.12.6.97. 0x0314 IOMMU Total Latency High Register 1 (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: IOMMU_PMU_TL_HIGH_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH1 Record total latency of Master1, higher 18-bit register

3.12.6.98. 0x0318 IOMMU Max Latency Register 1 (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: IOMMU_PMU_ML_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ML1 Record the max latency of Master1.

3.12.6.99. 0x0320 IOMMU Total Latency Low Register 2 (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: IOMMU_PMU_TL_LOW_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_TL_LOW2 Record total latency of Master2, lower 32-bit register

3.12.6.100. 0x0324 IOMMU Total Latency High Register 2 (Default Value: 0x0000_0000)

Offset: 0x0324			Register Name: IOMMU_PMU_TL_HIGH_REG2
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH2 Record total latency of Master2, higher 18-bit register

3.12.6.101. 0x0328 IOMMU Max Latency Register 2 (Default Value: 0x0000_0000)

Offset: 0x0328			Register Name: IOMMU_PMU_ML_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ ML2 Record the max latency of Master2.

3.12.6.102. 0x0330 IOMMU Total Latency Low Register 3 (Default Value: 0x0000_0000)

Offset: 0x0330			Register Name: IOMMU_PMU_TL_LOW_REG3
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	PMU_ TL_LOW3 Record total latency of Master3, lower 32-bit register

3.12.6.103. 0x0334 IOMMU Total Latency High Register 3 (Default Value: 0x0000_0000)

Offset: 0x0334	Register Name: IOMMU_PMU_TL_HIGH_REG3

Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH3 Record total latency of Master3, higher 18-bit register

3.12.6.104. 0x0338 IOMMU Max Latency Register 3 (Default Value: 0x0000_0000)

Offset: 0x0338			Register Name: IOMMU_PMU_ML_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML3 Record the max latency of Master3.

3.12.6.105. 0x0340 IOMMU Total Latency Low Register 4 (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: IOMMU_PMU_TL_LOW_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW4 Record total latency of Master4, lower 32-bit register

3.12.6.106. 0x0344 IOMMU Total Latency High Register 4 (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: IOMMU_PMU_TL_HIGH_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH4 Record total latency of Master4, higher 18-bit register

3.12.6.107. 0x0348 IOMMU Max Latency Register 4 (Default Value: 0x0000_0000)

Offset: 0x0348			Register Name: IOMMU_PMU_ML_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML4 Record the max latency of Master4.

3.12.6.108. 0x0350 IOMMU Total Latency Low Register 5 (Default Value: 0x0000_0000)

Offset: 0x0350			Register Name: IOMMU_PMU_TL_LOW_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW5

			Record total latency of Master5, lower 32-bit register

3.12.6.109. 0x0354 IOMMU Total Latency High Register 5 (Default Value: 0x0000_0000)

Offset: 0x0354			Register Name: IOMMU_PMU_TL_HIGH_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH5 Record total latency of Master5, higher 18-bit register

3.12.6.110. 0x0358 IOMMU Max Latency Register 5 (Default Value: 0x0000_0000)

Offset: 0x0358			Register Name: IOMMU_PMU_ML_REG5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ ML5 Record the max latency of Master5.

3.12.6.111. 0x0360 IOMMU Total Latency Low Register 6 (Default Value: 0x0000_0000)

Offset: 0x0360			Register Name: IOMMU_PMU_TL_LOW_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_TL_LOW6 Record total latency of Master6, lower 32-bit register

3.12.6.112. 0x0364 IOMMU Total Latency High Register 6 (Default Value: 0x0000_0000)

Offset: 0x0364			Register Name: IOMMU_PMU_TL_HIGH_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R	0x0	PMU_TL_HIGH6 Record total latency of Master6, higher 18-bit register

3.12.6.113. 0x0368 IOMMU Max Latency Register 6 (Default Value: 0x0000_0000)

Offset: 0x0368			Register Name: IOMMU_PMU_ML_REG6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PMU_ML6 Record the max latency of Master6.

3.13. RTC

3.13.1. Overview

The RTC(Real Time Clock) is used to display the real time and periodically wakeup. The RTC can display the year, month, day, week, hour, minute, second in real time. The RTC has the independent power to continue to work in system power-off. The RTC has the following features:

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768kHz low-frequency oscillator for counting clock
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- Stores power-off information in fourteen 32-bit general purpose register

3.13.2. Clock Tree Diagram

The clock tree diagram of RTC is shown in Figure 3-37.

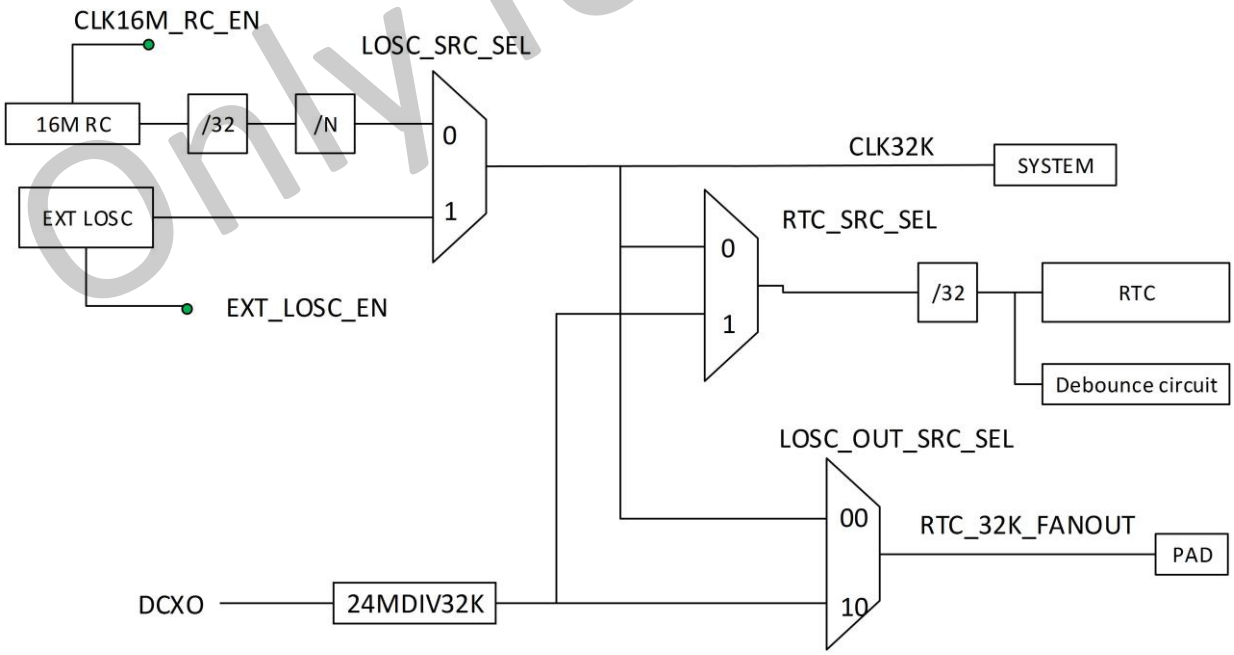

Figure 3- 37. RTC Clock Tree

RTC clock tree can be selected by corresponding switch, there are 3 options: 32K obtained by frequency division of 16M RC, 32K obtained by frequency division of DCXO(HOSC), 32K EXT obtained by external crystal(EXT LOSC).

3.13.3. Operations and Functional Descriptions

3.13.3.1. External Signals

Table 3- 13. RTC External Signals

Signal	Description
X32KIN	32.768kHz oscillator input
X32KOUT	32.768kHz oscillator output
X32KFOUT	32.768kHz clock fanout, provides low frequency clock for external devices
NMI	Alarm wakeup generates low level into NMI
RTC_VIO	RTC low voltage, generated via internal LDO
VCC_RTC	RTC high voltage, generated via external power

3.13.3.2. Clock and Reset

The RTC module has the independent reset signal, the signal follows VCC_RTC. When VCC_RTC powers on, the reset signal resets the RTC module; after VCC_RTC reaches stable, the reset signal always holds high level. Watchdog Reset cannot reset RTC.

The RTC module accesses its register by APBS1.

3.13.3.3. Typical Application

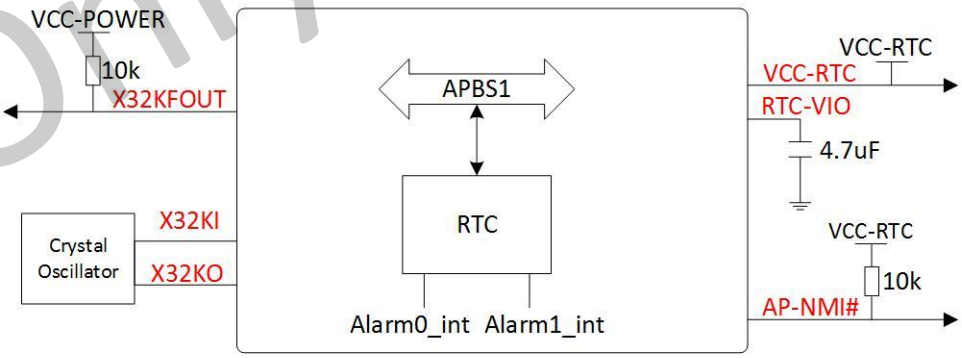

Figure 3- 38. RTC Application Diagram

The system accesses RTC register by APBS1 to generate the real time.

The external low-frequency oscillator must be 32.768 kHz.

If the external devices need low-frequency oscillator, X32KFOUT can provide.

AP-NMI# and alarm0 in common generate low level signal.

3.13.3.4. Function Implementation

3.13.3.4.1. Clock Sources

The RTC has 3 clock sources: internal RC, external low frequency crystal, 32K divided by external 24M crystal.
The internal RC can change RTC clock by changing division ratio; the external clock can not change clock.
The RTC selects the internal RC by default, when the system starts, the RTC can select by software the external low frequency crystal to provide much accuracy clock.
The clock accurate of the RTC is related to the accurate of the external low frequency crystal. Usually select 32.768 kHz crystal with ±20ppm frequency tolerance.

3.13.3.4.2. Real Time Clock

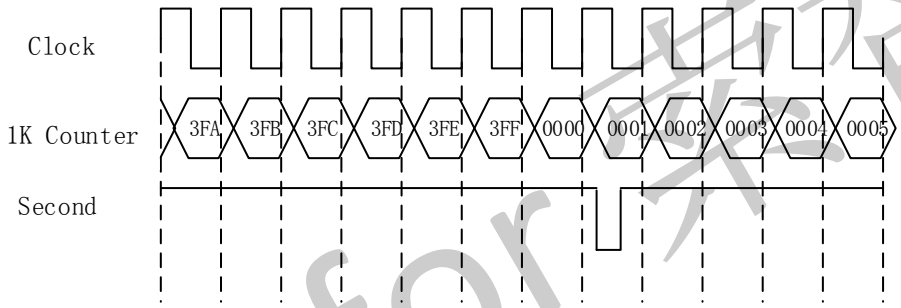

Figure 3- 39. RTC Counter

The 1K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x3FF, 1KHz counter starts to count again from 0, and the second counter adds 1. The step structure of 1KHz counter is as follows.

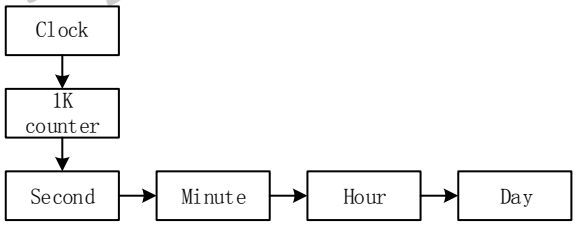

Figure 3- 40. RTC 1KHz Counter Step Structure

According to above implementation, the changing range of each counter is as follows.

Table 3- 14. RTC Counter Changing Range

Counter	Range
Second	0~59
Minute	0~59
Hour	0~23
Day	0~65535

CAUTION

Because there is no error correction mechanism in the hardware, note that each counter configuration should not exceed a reasonable counting range.

3.13.3.4.3. Alarm 0

The principle of alarm0 is a comparator. When RTC timer reaches scheduled time, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.
The RTC only generates one interrupt when RTC timer reached the scheduled day, hour, minute and second counter, then the RTC need set a new scheduled time, the next interrupt can be generated.

3.13.3.4.4. Power-off Storage

The RTC provides fourteen 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.13.3.4.5. RTC_VIO

The RTC module has a LDO, the input source of the LDO is VCC-RTC, the output of the LDO is RTC-VIO, the value of RTC-VIO is adjustable in a range from 0.7V to 0.9V, the RTC-VIO is mainly used for internal digital logic.

CAUTION

The RTC-VIO cannot connect a capacitor, the strength length of the pin is about 20mA.

3.13.3.4.6. NMI Interrupt

The RTC includes NMI interrupt generation module, which can collect external wake-up interrupt, ALARM interrupt and the wake-up interrupt generated by USB, to generate a periodic configurable square wave signal, the square signal can be output to PMU by NMI to wake-up SoC. The function can be masked, the external wake-up interrupt, ALARM interrupt and the wake-up interrupt generated by USB can be sent to PMU by NMI after masked.

3.13.3.5. Operating Mode

3.13.3.5.1. RTC Clock Control

(1) Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default, when the system starts, the clock source can be switched to the external 32K oscillator by software.
(2) Auto switch: After enabled the bit[14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external oscillator could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.
(3) After auto switch is valid, the clock source status bit cannot be changed, because the two functions are independent.

3.13.3.5.2. RTC Calendar

(1) Write time initial value: Write the current time to **RTC_DAY_REG** and **RTC_HH_MM_SS_REG**.
(2) After configured time, read the bit[8:7] of **LOSC_CTRL_REG** to ensure that configuration is completed.
(3) After update time, the RTC restarts to count again. The software can read the current time anytime.

NOTE

The RTC can only provide day counter, so the current day counter need be converted to year, month, day and week by software.
After configured time at each time, you need ensure the bit[8:7] of LOSC_CTRL_REG is 0 before the next setting is performed.

3.13.3.5.3. Alarm0

(1) Enable alram0 interrupt by writing **ALARM0_IRQ_EN**.
(2) Set the counter comparator, write the count-down day, hour, minute, second number to **ALARM0_DAY_REG** and **ALARM0_HH_MM_SS_REG**.
(3) Enable alarm0 function by writing **ALARM0_ENABLE_REG**, then the software can query alarm count value in real time by **ALARM0_DAY_REG** and **ALARM0_HH_MM_SS_REG.** When the setting time reaches, **ALARM0_IRQ_STA_REG** is set to 1 to generate interrupt.
(4) After enter the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the interrupt process.
(5) Resume the interrupt and continue to execute the interrupted process.
(6) Power-off wakeup is generated via SoC hardware and PMIC, the software only need set pending condition of alarm0, and set 1 to **ALARM0_CONFIG_REG**.

3.13.3.5.4. Fanout

Set the bit0 of **32K_FANOUT_GATING_REG** to 1, and ensure external pull-up resistor, voltage, clock source are normal, then 32.768kHz square wave can be output.

3.13.3.5.5. Pad Hold

When the corresponding bit of **GPL_HOLD_OUTPUT_REG** is set to 1, the corresponding pin can hold in stable state (high level, low level or high impedance). The function is used to prevent output pin from changing when corresponding power changes.

3.13.3.5.6. DRAM Data Encrypt

If using DRAM data encrypt, the DRAM data read by CPU is the encrypted data. The steps are as follows.
Before write/read **CRY_KEY_REG** and **CRY_EN_REG**, the bit[15:0] of **CRY_CONFIG_REG** should be written to 0x1689.

3.13.3.5.7. RC Calibration Usage Scenario

- Power-on: Select non-accurate 32KHz clock divided by internal RC.
- Normal scenario: Select 32KHz clock divided by 24MHz, or use external calibration clock 32KHz.
- Standby or power-off scenario: Select 32KHz clock divided by RC16M, or use external calibration clock 32KHz.

3.13.4. Programming Guidelines

3.13.4.1. RTC Clock Sources Setting

Configure **LOSC_CTRL_REG** to set RTC clock source.
For example: select external 32KHz clock source as RTC clock.

```
writel(0x16aa4000,LOSC_CTRL);      //writing key field
writel(0x16aa4001,LOSC_CTRL);      //select external 32K clock
```

3.13.4.2. Real Time Clock

For example: set time- 21', 07:08:09.

```
RTC_DAY_REG = 0x00000015;
RTC_HH_MM_SS_REG = 0x00070809; //0000 0000 000|0 0000(Hour) 00|00 0000(Minute) 00|00 0000(Second)
Read (RTC_DAY_REG);
Read (RTC_HH_MM_SS_REG);
```


3.13.4.3. Alarm 0

```
irq_request(GIC_SRC_R_Alarm0, Alm0_handler);
irq_enable(GIC_SRC_R_Alarm0);
writel(1, ALARM0_DAY_SET_REG);
writel(1, RTC_HH_MM_SS_REG);          //set 1 second corresponding to normal mode
writel(1, ALM0_EN);
writel(1, ALM_CONFIG);                //NMI output
while(!readl(ALM0_IRQ_STA));
writel(1, ALM0_IRQ_EN);
while(readl(ALM0_IRQ_STA));
```

3.13.5. Register List

Module Name	Base Address
RTC	0x07000000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
RTC_DAY_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
32K_FANOUT_GATING_REG	0x0060	32k Fanout Output Gating Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0~13)
BROM_WB_FLAG0_REG	0x0138	Brom Warm Boot Flag0 Register
BROM_WB_FLAG1_REG	0x013C	Brom Warm Boot Flag1 Register
DCXO_CTRL_REG	0x0160	DCXO Control Register
RTC_VIO_REG	0x0190	RTC_VIO Regulate Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDDOFF_GATING_SOF_REG	0x01F4	VDD To RTC Isolation Software Control Register
SP_STDBY_FLAG_REG	0x01F8	Super Standby Flag Register
SP_STDBY_SOFT_ENTRY_REG	0x01FC	Super Standby Software Entry Register
USB_STBY_CTRL_REG	0x0200	USB Standby Control Register

EFUSE_HV_PWRSWT_CTRL_REG	0x0204	Efuse High Voltage Power Switch Control Register
PAD_CTRL_REG	0x0208	PAD Control Register
SRAM_RTEN_CTRL_REG	0x020C	SRAM Retention Control Register
CRY_CONFIG_REG	0x0210	Crypt Configuration Register
CRY_KEY_REG	0x0214	Crypt Key Register
CRY_EN_REG	0x0218	Crypt Enable Register

3.13.6. Register Description

3.13.6.1. 0x0000 LOSC Control Register (Default Value: 0x0000_4010)

Offset:0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit0 and bit1 can be written with the new value.
15	R/W	0x0	LOSC_AUTO_SWT_FUNCTION LOSC auto switch function disable 0: Enable 1: Disable
14	R/W	0x1	LOSC_AUTO_SWT_32K_SEL_EN LOSC auto switch 32K clk source sel enable 0: Disable, when losc lost, 32k clk source will not change to RC 1: Enable, when losc lost, 32k clk source will change to RC(LOSC_SRC_SEL will be changed from 1 to 0)
13:9	/	/	/
8	R/W	0x0	RTC_HHMMSS_ACCE RTC HH-MM-SS access After writing the RTC HH-MM-SS Register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS Register, the RTC HH-MM-SS Register will be refreshed for at most one second.
7	R/W	0x0	RTC_DAY_ACCE. RTC DAY access. After writing the RTC DAY register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC DAY register, the DAY register will be refreshed for at most one second.
6:5	/	/	/
4	R/W	0x1	EXT_LOSC_EN External 32.768kHz Crystal Enable 0: Disable

			1: Enable
3:2	R/W	0x0	EXT_LOSC_GSM External 32.768kHz Crystal GSM 00: Low 01: / 10: / 11 High When GSM is changed, 32K oscillation circuit will arise transient instability. If the auto switch function is enabled, 32K changes to RC16M with certain probability. GSM can influence the time of 32K starting oscillation, the more the GSM, the shorter the time of starting oscillation. So modifying GSM is not recommended. If modifying GSM is necessary, firstly disable the auto switch function(bit15), with a delay of 50us, then change GSM, 32K clock source is changed to external clock.
1	R/W	0x0	RTC_SRC_SEL RTC_TIMER Clock source Select 0:LOSC_SRC 1:24MDIV32K Before changing the bit, 24MDIV32K function need be ensured to open, that is, the bit[16] of 32K_FANOUT_GATING_REG is 1.
0	R/W	0x0	LOSC_SRC_SEL LOSC Clock source Select. 'N' is the value of Internal OSC Clock Prescalar Register. 0: Low Frequency Clock from 16M RC 1: External 32.768kHz OSC

NOTE

If the bit[8:7] of LOSC_CTRL_REG is set, the RTC HH-MM-SS, DD and ALARM DD-HH-MM-SS register cannot be written.

3.13.6.2. 0x0004 LOSC Auto Switch Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	EXT_LOSC_STA Work only when AUTO SWITCH function is enabled. 0: External 32.768kHz OSC work normally 1: External 32.768kHz OSC work abnormally
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND LOSC auto switch pending 0: No effect 1: Auto switch pending, it means LOSC_SRC_SEL is changed from 1 to 0.

			Setting 1 to this bit will clear it.
0	R	0x0	LOSC_SRC_SEL_STA Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar Register. 0: Low Frequency Clock from 16M RC 1: External 32.768kHz OSC

3.13.6.3. 0x0008 Internal OSC Clock Prescalar Register (Default Value: 0x0000_000F)

Offset:0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0xF	INTOSC_32K_CLK_PRESCAL. Internal OSC 32K Clock Prescalar value N. The clock output = Internal RC/32/N. 00000: 1 00001: 2 00002: 3 ..... 11111: 32

3.13.6.4. 0x0010 RTC DAY Register

Offset:0x0010			Register Name: RTC_DAY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	UDF	DAY Day Range from 1~65535.

3.13.6.5. 0x0014 RTC HH-MM-SS Register

Offset:0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	UDF	HOUR Range from 0~23
15:14	/	/	/
13:8	R/W	UDF	MINUTE Range from 0~59
7:6	/	/	/

5:0	R/W	UDF	SECOND Range from 0~59

3.13.6.6. 0x0020 Alarm 0 Day Setting Register (Default Value: 0x0000_0000)

Offset:0x0020			Register Name: ALARM0_COUNTER_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	ALARM0_COUNTER Alarm 0 Counter is based on Day.

3.13.6.7. 0x0024 Alarm 0 HH-MM-SS Setting Register

Offset:0x0024			Register Name: ALARM0_CUR_VLU_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	x	HOUR Range from 0~23
15:14	/	/	/
13:8	R/W	x	MINUTE Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND Range from 0~59

3.13.6.8. 0x0028 Alarm 0 Enable Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: ALARM0_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable If this bit is set to “1”, the valid bits of Alarm 0 Counter Register will down count to zero, and the alarm pending bit will be set to “1”. 0: Disable 1: Enable

3.13.6.9. 0x002C Alarm 0 IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x002C	Register Name: ALARM0_IRQ_EN

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN Alarm 0 IRQ Enable 0: Disable 1: Enable

3.13.6.10. 0x0030 Alarm 0 IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND Alarm 0 IRQ Pending bit 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.13.6.11. 0x0050 Alarm Configuration Register (Default Value: 0x0000_0000)

Offset:0x0050			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.13.6.12. 0x0060 32K FANOUT Gating Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: 32K_FANOUT_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	HOSC_32K_DIVIDER_ENABLE 1: enable the hosc 24m to 32k divider circuit 0: disable the hosc 24m to 32k divider circuit
15:3	/	/	/
2:1	R/W	0x0	LOSC_OUT_SRC_SEL 00:RTC_32K(select by RC_CLK_SRC_SEL & LOSC_SRC_SEL) 01:/

			10:HOSC divided 32K
0	R/W	0x0	32K_FANOUT_GATING Configuration of 32k output, and no 32k output by default. 0: Mask LOSC output gating 1: Enable LOSC output gating

3.13.6.13. 0x0100+N*0x0004 General Purpose Register (Default Value: 0x0000_0000)

Offset:0x0100+N*0x0004 (N=0~13)			Register Name: GP_DATA_REGN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	GP_DATA Data [31:0]

NOTE

General purpose register 0~13 value can be stored if the RTC-VIO is larger than 0.6V.

3.13.6.14. 0x0160 DCXO Control Register (Default Value: 0x883F_F0FC)

Offset:0x0160			Register Name: DCXO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	DCXO_FANOUT_ENB 0: enable DCXO wake up function 1: disable DCXO wake up function
30:28	/	/	/
27:24	R/W	0x8	DCXO_ICTRL DCXO current control value
23	/	/	/
22:16	R/W	0x3F	DCXO_TRIM DCXO cap array value Capacity cell is 55fF
15:13	/	/	/
12:8	R/W	0x10	DCXO_BG DCXO bandgap output voltage
7	R/W	0x1	DCXO_LDO_INRUSHB DCXO LDO driving capacity signal, active high
6	R/W	0x1	XTAL_MODE Xtal mode enable signal, active high 0: For external clk input mode 1: For normal mode
5:4	R/W	0x3	DCXO_RFCLK_ENHANCE DCXO rfclk enhance Enhance driving capacity of output OUT_RF_REFCLK, 0x0 for 5pF, 0x1 for

			10pF, 0x2 for 15pF, 0x3 for 20pF.
3:2	/	/	/
1	R/W	0x1	DCXO_EN DCXO enable 1: Enable 0: Disable
0	R/W	0x1	CLK16M_RC_EN 1: Enable 0: Disable To ensure the reset debounce circuit has a stable clock source, the software is required to configure the relevant registers. The specific requirements are as follows: When starting the first time, the reset debounce circuit of SoC uses 32k clock divided by RC16M by default; When shutdown, the software should read the relevant bit to confirm whether EXT32K is working normally. If it is working normally, the clock source of debounce circuit should be switched to EXT32K first, and then RC16M should be disabled. When no EXT32K scene or plug-in RTC, the software switchs clock source after confirm EXT32K is working normally; if no problem, the software directly does not disable RC16M.

3.13.6.15. 0x0190 RTC_VIO Regulation Register (Default Value: 0x0000_0004)

Offset:0x0190			Register Name:RTC_VIO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	V_SEL 0: resistance divider 1: band gap
3	/	/	/
2:0	R/W	0x4	RTC_VIO_REGU These bits are useful for regulating the RTC_VIO from 0.6V to 1.3V, and the regulation step is 0.1V. 000: 1.0V 001: 0.6V (the configuration can cause RTC reset) 010: 0.7V 011: 0.8V 100: 0.9V 101: 1.1V 110: 1.2V 111: 1.3V RTC-VIO is provided power for RTC digital part, the default value is 0.9V. After power-on, software sets the field to 0.8V to save power-consumption.

3.13.6.16. 0x01F0 IC Characteristic Register (Default Value: 0x0000_0000)

Offset:0x01F0			Register Name: IC_CHARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	IC_CHARA Key Field Should be written at value 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA Return 0x16AA only if the KEY_FIELD is set as 0x16AA when read those bits, otherwise return 0x0.

3.13.6.17. 0x01F4 VDD To RTC Isolation Software Control Register (Default Value: 0x0000_0000)

Offset:0x01F4			Register Name: VDDOFF_GATING_SOF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD Key Field This field should be filled with 0x16AA, and then the bit15 can be configured.
15	WAC	0x0	When use vdd_sys to RTC isolation software control, write this bit to 1, it will only be cleared by reset release.
14:2	/	/	/
1	R/W	0x0	DRAM_ZQ_PAD_HOLD Hold the pad of DRAM channel 0:not hold 1:hold dram ZQ Pad This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.
0	R/W	0x0	DRAM_CH_PAD_HOLD Hold the pad of DRAM channel 0:not hold 1:hold dram Pad This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.

3.13.6.18. 0x01F8 Super Standby Flag Register (Default Value: 0x0000_0000)

Offset:0x01F8			Register Name: SP_STDBY_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0x0	SP_STDBY_FLAG Key Field Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only fellow the appropriate process, the super standby flag can be written in the lower 16 bits.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA When system is turned on, the low 16 bits of the value in the Super Standby Flag Register should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written with 0x16AA at first. Then, software programmer must write 0xAA16XXXX in the Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID.

3.13.6.19. 0x01FC Super Standby Software Entry Register (Default Value: 0x0000_0000)

Offset:0x01FC			Register Name: SP_STDBY_SOFT_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CPU software entry register when acting from supper standby.

3.13.6.20. 0x0200 USB Standby Control Register (Default Value: 0x0000_0000)

Offset:0x0200			Register Name: USB_STBY_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25	R/W	0x0	RC_CLK_EN_USB 0: Disable 1: Enable
24	R/W	0x0	RC_CLK_SEL_USB SCLK_USBPHY, EHCI_HCLK and OHCI_SCLK Clock Source Select. RC16M clock is selected only in USB standby mode if necessary. 0: SCLK_USBPHY is from OSC24M, EHCI_HCLK and OHCI_HCLK are from Hclk 1: SCLK_USBPHY, EHCI_HCLK and OHCI_SCLK are from RC16M
23:17	/	/	/
16	R/W	0x0	USB POWER OFF GATING Gating the VDD_SYS to VDD_USB signal in USB standby mode. It must be set to 1 before entering USB standby mode and set to 0 when exiting Normal mode. 0: disable 1: enable
15:9	/	/	/
8	R/W	0x0	USB_STBY_IRQ_POWER_OFF_GATING

			Gating the USB standby irq signal to RTC module in Super Standby mode when USB module is power off. It must be set to 1 in Super Standby mode and must set to 0 in other mode. 0: disable 1: enable
7:5	/	/	/
4	R/W	0x0	USB_STBY_IRQ_OUTPUT_GATING Mask the USB standby irq output to nmi pad. It must be set to 1 in USB standby mode and set to 0 in other mode. 0: disable irq output 1: enable irq output
3:0	/	/	/

3.13.6.21. 0x0204 Efuse High Voltage Power Switch Control Register (Default Value: 0x0000_0000)

Offset:0x0204			Register Name: EFUSE_HV_PWRSWT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EFUSE_1.8V_POWER_SWITCH_CONTROL 1: open power switch 0: close power switch Before programming efuse, the bit need be set to 1.

3.13.6.22. 0x0208 PAD Control Register (Default Value: 0x0000_0000)

Offset:0x0208			Register Name: PAD_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	WAC	0x0	NMI_PENDING IRQ Pending bit 0: No effect 1: Pending, Setting 1 to this bit will clear it.
15:9	/	/	/
8	R/W	0x0	NMI_GEN_EN 0: Disable 1: Enable
7:6	R/W	0x3	NMI_DLY_SEL 00: 8ms 01: 16ms 10: 32ms 11: 64ms

5	R/W	0x0	EXT_IRQ_EN External IRQ Input Enable 0: Disable 1: Enable
4	/	/	/
3	R/W	0x1	RST_BYP_PAD_PU RST_BYP PIN PAD PULL UP CTRL 0: NOT PULL-UP 1: PULL-UP **For QFN88 package, the bit need be set to 0 after power-on to reduce RTC leakage current.** **For other packages, the bit remains to 1.**
2	R/W	0x1	EXT_IRQ_PAD_EN 0: Enable 1: Disable If using EXT_IRQ_PAD input function, the bit need be set to 0.
1	R/W	0x1	FOUT_PAD_EN 0: Enable 1: Disable
0	R/W	0x1	NMI_PAD_EN 0: Enable 1: Disable If using NMI PAD input function, the bit need be set to 0.

3.13.6.23. 0x020C SRAM Retention Control Register (Default Value: 0x0000_0000)

Offset:0x020C			**Register Name: SRAM_RTEN_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	SRAM_MODE 0: RETENTION MODE 1: NORMAL MODE

3.13.6.24. 0x0210 Crypto Configuration Register (Default Value: 0x0000_0000)

Offset:0x0210			**Register Name: CRY_CONFIG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	KEY_FIELD Key Field If you want to read or write Crypt Key Register/Crypt Enable Register, you should write 0x1689 in these bits.

3.13.6.25. 0x0214 Crypto Key Register (Default Value: 0x0000_0000)

Offset:0x0214			Register Name: CRY_KEY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CRY_KEY Crypto Key

3.13.6.26. 0x0218 Crypto Enable Register (Default Value: 0x0000_0000)

Offset:0x0218			Register Name: CRY_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CRY_EN Crypto Enable

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Figures

Chapter 4 Video and Graphics

4.1. DE

The Display Engine(DE) is a hardware composer to transfer image layers from a local bus or a video buffer to the LCD interface. The DE supports four overlay windows to blend, and supports image post-processing in the video channel. The block diagram of DE is shown in Figure 4-1.

The DE has the following features:

- Output size up to 2048 x 2048
- Three alpha blending channels for main display
- Four overlay layers in each channel, and has an independent scaler(only for video channel)
- Potter-duff compatible blending operation
- Input format: semi-planar YUV422/YUV420/YUV411 and planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports write back only for verification

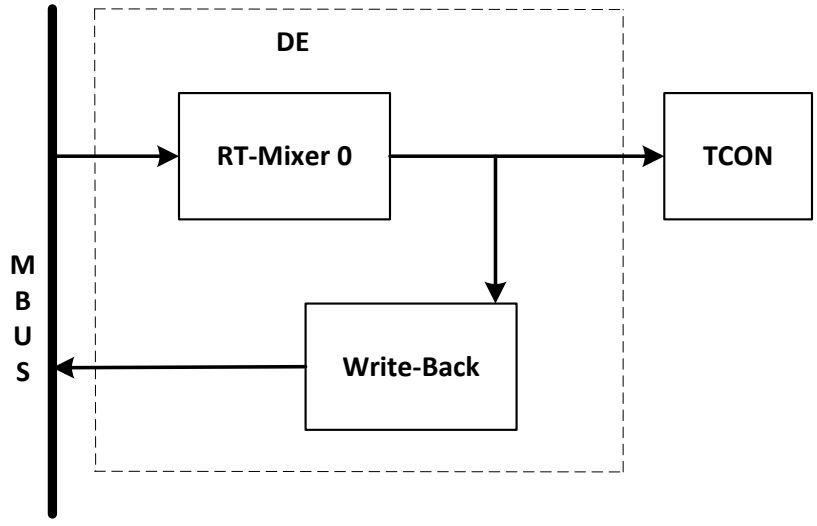

Figure 4- 1. DE Block Diagram

4.2. G2D

The Graphic 2D(G2D) Engine is hardware accelerator for 2D graphic.

The G2D has the following features:

- Supports layer size up to 2048x2048 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats(8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function above
- Supports 1/16× to 32× resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter, 32-phase 4-tap vertical anti-alias filter
- Supports window clip
- Supports FillRectangle, BitBlit, StretchBlit and MaskBlit
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

4.3. Video Encoding

The Video Encoding consists of the video encoding unit(VE) and JPEG encoder(JPGE). The VE supports H.264 and H.265 encoding, and JPGE supports JPEG/MJPEG encoding.

4.3.1. VE

4.3.1.1. Overview

The VE is a CODEC that supports H.264 and H.265 protocol based on ASIC. It is custom-made for the IPC usage and features high compressing rate, low CPU usage, short delay and low power consumption.
The VE has the following features:

- Supports ITU-T H.265 main profile@level 6.0 main-tier encoding
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Encoding of the multiple reference frame, long-term reference frame
  - Three prediction unit (PU) types of 32 x 32, 16 x 16 and 8 x 8 for inter-prediction
  - Four prediction unit types of 32 x 32, 16 x 16, 8 x 8 and 4 x 4 for intra-prediction
  - Skip mode and Merge mode with a maximum of two candidates processing to be merged
  - Four transform unit (TU) types of 32 x 32, 16 x 16, 8 x 8 and 4 x 4
  - CABAC entropy encoding
  - De-blocking filtering
  - Sample adaptive offset (SAO)
- Supports ITU-T H.264 high profile/main profile/baseline profile@level 5.2 encoding
  - Encoding of multiple slice
  - Motion compensation with 1/2 and 1/4 pixel precision
  - Encoding of the multiple reference frame, long-term reference frame
  - Two prediction unit (PU) types of 16 x 16 and 8 x 8 for inter-prediction
  - Three prediction unit types of Intra16x16, Intra8x8 and Intra4x4 for intra-prediction
  - Trans4x4 and trans8x8
  - CABAC and CAVLC entropy encoding
  - De-blocking filtering
- Supports QPMap mode for custom encoding
- Supports SSE/QP/MAD output based on 16 x 16
- Supports Smart, HVS and Alter FrameRate functions in particular
- Supports Classify, MB-RateControl, Fore-3D-Filter, Syclic-Intra-Refresh, Dynamic-ME, Inter-Only-in-P-Frame, Intra-4x4-Disable and HighPass-Filter Functions in general
- Supports the input picture format of semi-planar YCbCr4:2:0
- **V833:** Supports H.264 encoding with the performance of 8-megapixel 1080p@60fps + VGA@60fps or 5M@20fps + 1080p@20fps
- **V831:** Supports H.264 encoding with the performance of 2-megapixel 1080p@30fps
- **V833:** Supports H.265 encoding with the performance of 8-megapixel 1080p@90fps or 5M@30fps + 720p@30fps
- **V831:** Supports H.265 encoding with the performance of 2-megapixel 1080p@30fps

- Supports configurable picture resolutions
  - Minimum picture resolution: 192 x 96
  - Maximum picture resolution: 4096 x 4096(**for V833**), 1920 x 1080(**for V831**)
  - Step of the picture width or height: 2
- Supports region of interest (ROI) encoding
  - Maximum of 8 ROIs
  - Independent enable/disable control for the encoding function of each ROI
- Supports on-screen display (OSD) encoding protection that can be enabled or disabled
- Supports OSD front-end overlaying
  - OSD overlaying before encoding for a maximum of 64 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports three bit rate control modes: constant bit rate (CBR), variable bit rate (VBR) and FIXQP
- Supports the output bit rate ranging from 2kbit/s to 100Mbit/s
- Supports Frame Buffer Compression
- Supports region of interest (ROI) for AI
  - Maximum of 16 ROIs
  - The size of every ROI is from 16 x 16 to 2048 x 2048

4.3.1.2. Block Diagram

The functional block diagram of the VE is as follows.

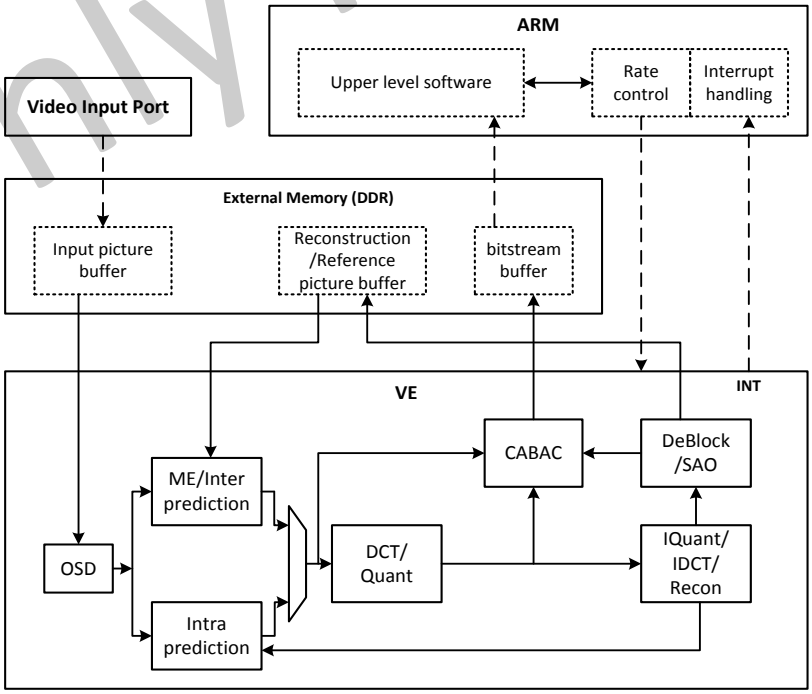

Figure 4- 2. VE Block Diagram

Based on related protocols and algorithms, the VE supports motion estimation/inter-prediction, intra-prediction,

transform/quantization, inverse transform/inverse quantization, CABAC encoding/stream generation and DeBlock/SAO. The ARM software controls the bit-rate and handles interrupt.

Before the VE starts encoding, software allocates three types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**
  The VE reads the source pictures to be encoded from this buffer during encoding. This buffer is typically written by the Video Input Port module.
- **Reconstruction/Reference picture buffer**
  The VE writes reconstruction pictures to this buffer during encoding. These reconstruction pictures are used as the reference pictures of subsequent pictures. During the encoding of P frames and B frames, reference pictures are read from this buffer.
- **Stream buffer**
  This buffer stores encoded streams. The VE writes streams to this buffer during encoding. This buffer is read by software.

4.3.2. JPGE

4.3.2.1. Overview

The JPGE is a high-performance JPEG encoder based on ASIC. It supports 64-megapixel snapshot or HD MJPEG encoding.

The JPGE has the following features:

- Supports ISO/IEC 10918-1 (CCITT T.81) baseline process (DCT sequential) encoding
- Encodes the pictures in the chrominance sampling format of YCbCr4:2:0, YCbCr4:2:2 and YCbCr4:4:4
- Supports multiple input picture formats:
  - Semi-planar YCbCr4:2:0
  - Semi-planar YCbCr4:2:2
  - Semi-planar YCbCr4:4:4
- **V833:** Supports JPEG encoding with the performance of 1080p@60fps
- **V831:** Supports JPEG encoding with the performance of 1080p@30fps
- Supports configurable picture resolutions
  - Minimum picture resolution: 192 x 96
  - Maximum picture resolution: 8192 x 8192(**for V833**), 1920 x 1080(**for V831**)
- Supports the picture width or height step of 8
- Supports configurable quantization tables for the Y component, Cb component and Cr component respectively
- Supports OSD front-end overlapping
  - OSD overlaying before encoding for a maximum of 64 regions
  - OSD overlaying with any size and at any position (within the size and position range of the picture)
  - 16-level alpha blending
  - OSD overlaying control (enabled or disabled)
- Supports the color-to-gray function

4.3.2.2. Block Diagram

The functional block diagram of the JPGE is as follows.

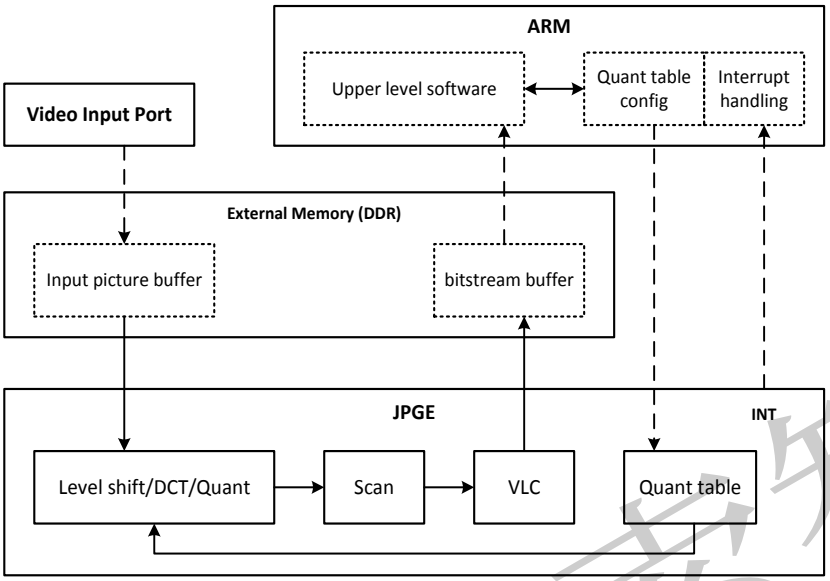

Figure 4- 3. JPGE Block Diagram

The JPGE realizes various protocol processing with large computation such as OSD, level shift, DCT, quantization, scanning, VLC encoding, and stream generation. The ARM software completes the encoding control processing such as quantization table configuration and interrupt processing.

Before the JPGE is enabled for video encoding, the software allocates two types of buffers mainly in the external DDR SDRAM:

- **Input picture buffer**

  The JPGE reads the source pictures to be encoded from this buffer during encoding. This buffer is generally written by the Video Input Port module.

- **Stream buffer**

  This buffer stores encoded streams. The JPGE writes streams to this buffer during encoding. This buffer is read by software.

4.4. EISE

4.4.1. Overview

Electronic Image Stabilization Engine(EISE) is located between the ISP and the Encoder, it is a hardware accelerator for anti-shake processing of continuous video images acquired by Sensor. EISE includes two modes of image distortion correction(IDC) and image stabilization.

The processing capability of the EISE module is as follows.

- **V833**: Supports frame rate of 1080p@60fps
- **V831**: Supports frame rate of 1080p@30fps

4.4.2. EISE Functional Descriptions

4.4.2.1.1. Input

- YUV420 Semi-planar Input
- Only uncompressed image is supported
- Minimum input resolution of 128 x 128
- **V833**: For 360 mode, maximum input resolution is 2048 x 2048. For 180 mode and PTZ mode, maximum input resolution is 2816 x 2816. For LDC mode, maximum input resolution is 3840 x 2220.
- **V831**: For 360 mode, maximum input resolution is 1440 x 1440. For 180 mode and PTZ mode, maximum input resolution is 1440 x 1440. For LDC mode, maximum input resolution is 1920 x 1080.

4.4.2.1.2. Output

- Only NV12 and NV21 is supported
- Only uncompressed image is supported
- Minimum input resolution of 32 x 32
- The height should be a multiple of 8
- The width should be a multiple of 8
- The stride should be a multiple of 32
- Supports cropping

4.4.3. IDC Functional Descriptions

The IDC mode implements Fisheye Correction, Lens Distortion Correction (LDC). The fisheye correction module corrects fisheye images to conform to user habit, and includes 360 panoramic mode, 180 panoramic mode, 360 split panoramic mode and normal mode. The LDC module removes the imaging distortion of wide angle lens.

4.4.3.1. Input

- YUV420 Semi-planar input
- Only uncompressed image is supported
- Minimum input resolution of 128 x 128
- **V833**: For 360 mode, maximum input resolution is 2048 x 2048. For 180 mode and PTZ mode, maximum input resolution is 2816 x 2816. For LDC mode, maximum input resolution is 3840 x 2220.
- **V831**: For 360 mode, maximum input resolution is 1440 x 1440. For 180 mode and PTZ mode, maximum input resolution is 1440 x 1440. For LDC mode, maximum input resolution is 1920 x 1080.

4.4.3.2. Input Image Size

- The height should be a multiple of 8
- The width should be a multiple of 8

4.4.3.3. Output

- Supports YUV420 Semi-planar output, YUV420 Semi-planar output.
- Only uncompressed image is supported
- 180 mode: output height (/width) should be less than or equal to the input height (/width), while the minimum output height (/width) should be greater than 50% of the input height (/width)
- 360 mode: output width should be 2 times of input width, output height should be 1/2 of input height
- Normal mode: output height (/width) should be less than or equal to 1/2 of input height (/width). The minimum output size is 40 x 40
- 360 split mode: output resolution should be equal to input resolution
- LDC mode: output resolution should be equal to input resolution

4.4.3.4. Output Image Size

- The height should be a multiple of 8
- The width should be a multiple of 8

4.4.3.5. PTZ Parameters

- Wall mount: P[25,155], T[25,155], Z[1,4]
- Top mount and bottom mount: P[0,360], T[0,90], Z[1,4]

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Chapter 5 Memory

5.1. SDRAM Controller(DRAMC)

5.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to the industry-standard DDR2/DDR3/DDR3L SDRAM. It supports up to a 24G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The DRAMC includes the following features:

- Single-channel DRAMC
- Supports 16-bit data bus width
- Supports 2 chip select signals
- Supports DDR2/DDR3/DDR3L SDRAM
- Supports different memory device's power voltage of 1.8V, 1.5V, 1.35V
- Supports clock frequency up to 800 MHz(DDR3/DDR3L)
- Supports clock frequency up to 533 MHz(DDR2)
- Supports memory capacity up to 24G bits (3G Bytes)
- 16 address lines and 3 bank address lines per channel
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be changed for different application(MDFS supported)
- Controller clock on/off hardware automatically support
- Auto Self-Refresh Entry(ASRE)/Exit(ASRX) support
- Clock pad enable/disable hardware automatically support when ASRE/ASRX
- Priority of transferring through multiple ports is programmable
- Random read or write operation is supported

NOTE

V831 is embedded with 64MB DDR2.

5.2. SD/MMC Host Controller(SMHC)

5.2.1. Overview

The SD-MMC Host Controller(SMHC) controls the read/write operations on the secure digital(SD) card and multimedia card(MMC), and supports various extended devices based on the secure digital input/output(SDIO) protocol. The V833/V831 provides three SMHC interfaces for controlling the SD card, MMC and SDIO device.

The SMHC has the following features:

- Supports eMMC boot operation
- Supports command completion signal and interrupt to host processor and command completion signal disable feature
- SMHC0 supports SD (Version1.0 to 2.0), 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - DDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
- SMHC1 supports SDIO(Version1.1 to 3.0), 4-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - DDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
- SMHC2 supports MMC(Version3.3 to 5.0), 8-bit bus width
  - SDR mode 50MHz@3.3V IO pad
  - DDR mode 50MHz@3.3V IO pad
  - SDR mode 150MHz@1.8V IO pad
  - DDR mode 100MHz@1.8V IO pad
- Hardware CRC generation and error detection
- Programmable baud rate
- Host pull-up control
- Supports SDIO interrupt in 1-bit and 4-bit modes
- Block size of 1 to 65535 bytes
- Descriptor-based internal DMA controller
- Internal 1KB FIFO for data transfer
- SMHC0 realizes the conversion from 3.3V to 1.8V, no independent LDO power is required

NOTE

V831 only supports two SMHC interfaces: SMHC0, SMHC1.

5.2.2. Block Diagram

Figure 5-1 shows a block diagram of the SMHC.

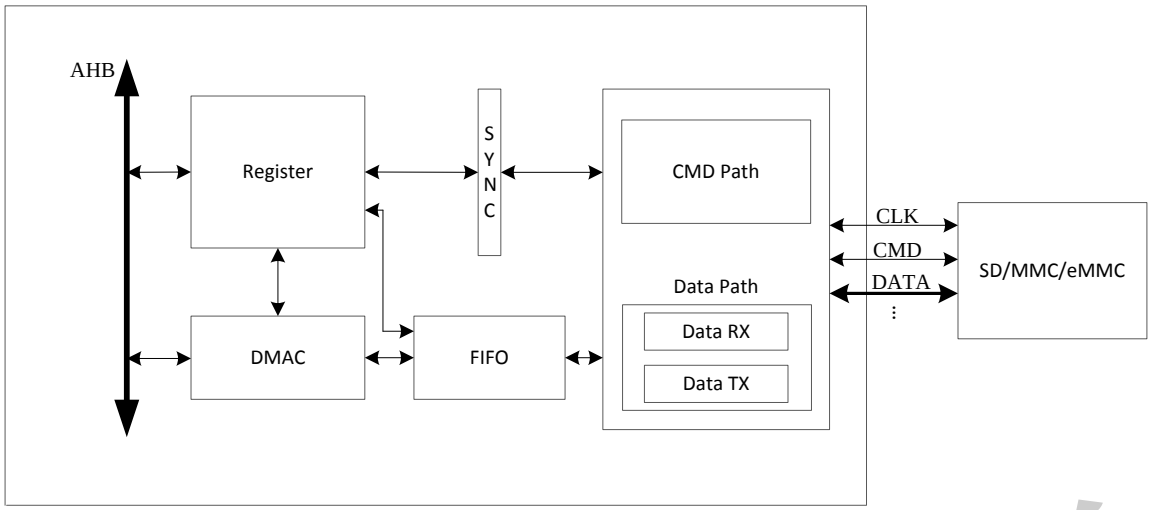

Figure 5- 1. SMHC Block Diagram

5.2.3. Operations and Functional Descriptions

5.2.3.1. External Signals

Table 5-1 describes the external signals of SMHC.

Table 5- 1. SMHC External Signals

V833 Signal	V831 Signal	Width	Type	Description
SDC0_CLK	SDC0_CLK	1	O	Clock output for SD/TF card
SDC0_CMD	SDC0_CMD	1	I/O,OD	CMD line for SD/TF card
SDC0_D[i] (i=0~3)	SDC0_D[i] (i=0~3)	4	I/O	Data line for SD/TF card
SDC1_CLK	SDC1_CLK	1	O	Clock output for SDIO Wi-Fi
SDC1_CMD	SDC1_CMD	1	I/O,OD	CMD line for SDIO Wi-Fi
SDC1_D[i] (i=0~3)	SDC1_D[i] (i=0~3)	4	I/O	Data line for SDIO Wi-Fi
SDC2_CLK	/	1	O	Clock output for MMC
SDC2_CMD	/	1	I/O,OD	CMD line for MMC
SDC2_D[i] (i=0~7)	/	8	I/O	Data line for MMC
SDC2_RST	/	1	O	Reset signal for MMC
SDC2_DS	/	1	I	Data strobe for MMC

5.2.3.2. Clock Sources

Each SMHC gets three different clocks. User can select one of them to make SMHC clock source. Table 5-2 describes the clock sources of SMHC. Users can see CCU in chapter 3.3 for clock setting, configuration and gating information.

Table 5- 2. SMHC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERI0(2X)	Peripheral Clock, the default value is 1.2GHz
PLL_UNI(2X)	UNI Clock, the default value is 1.2GHz

5.2.3.3. Timing Diagram

Please refer to relative specifications:

- Physical Layer Specification Ver3.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card(eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card(eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard(5.0)

5.2.3.4. Internal DMA Controller Description

SMHC has an internal DMA controller (IDMAC) to transfer data between host memory and SMHC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

5.2.3.4.1. IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.

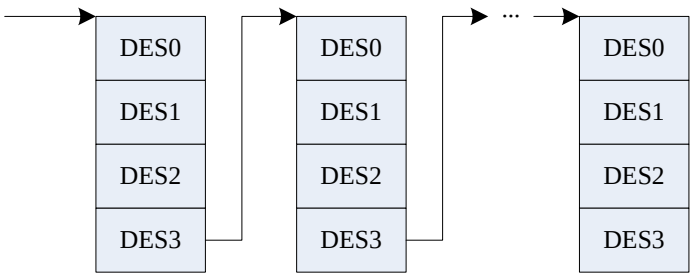

Figure 5- 2. IDMAC Descriptor Structure Diagram

This figure illustrates the internal formats of a descriptor. The descriptor address must be aligned to the bus width used for 32-bit bus. Each descriptor contains 16 bytes of control and status information.

DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, and DES3 to denote [127:96] bits in a descriptor.

5.2.3.4.2. DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:5	/	/
4	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed by this descriptor are the last data buffer
1	Disable Interrupt on Completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed by this descriptor
0	/	/

5.2.3.4.3. DES1 Definition

For SMHC0/SMCH1:

Bits	Name	Descriptor
31:16	/	/
15:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

For SMHC2:

Bits	Name	Descriptor
31:13	/	/

12:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor.

5.2.3.4.4. DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. For SMHC0 and SMHC1, the field is a word address. For SMHC2, the field is a byte address.

5.2.3.4.5. DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present. For SMHC0 and SMHC1, the field is a word address. For SMHC2, the field is a byte address.

5.2.3.5. Calibrate Delay Chain

The sample clock delay chain and Data Strobe delay chain(the chain is only in SMHC2) are used to generate delay to make proper timing between data strobe and data signals. Each delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through **SMHC Bus Gating Reset Register** and **SMHC2 Clock Register**.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(CCU). Calibration delay chain is an internal function in SMHC and does not need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200MHz.

Step3: Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable** (bit[7]) and sets initial delay value 0x20 to **Delay chain**(bit[5:0]). Then write 0x0 to **delay control register** to clear the value.

Step4: Write 0x8000 to **delay control register** to start calibrate delay chain.

Step5: Wait until the flag(bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at bit[13:8] in **delay control register**. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the cycle of SMHC's clock and the result of calibration.

NOTE

In the above descriptions, delay control register contains SMHC Sample Delay Control Register and SMHC Data Strobe Delay Control Register. Delay Software Enable contains Sample Delay Software Enable and Data Strobe Delay Software Enable. Delay chain contains Sample Delay Software and Data Strobe Delay Software.

5.2.4. Programming Guidelines

5.2.4.1. Initialization

Before data and command are exchanged between a card and the SMHC, the SMHC need to be initialized. The SMHC is initialized as follows.

Step1: Configure GPIO register as SMHC function by Port Controller module; reset clock by writing 1 to SMHC_BGR_REG[SMHCx_RST], open clock gating by writing 1 to SMHC_BGR_REG[SMHCx_GATING]; select clock sources and set division factor by configuring the SMHCx_CLK_REG(x=0,1,2) register.

Step2: Configure SMHC_CTRL to reset FIFO and controller, enable total interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupt and error abnormal interrupt, and register interrupt function.

Step3: Configure SMHC_CLKDIV to open clock for device; configure SMHC_CMD as change clock command(for example 0x80202000); send update clock command to deliver clock to device.

Step4: Configure SMHC_CMD to normal command, configure SMHC_CMDARG to set command parameter, configure SMHC_CMD to set response type, etc, then command can send. According to initial process in the protocol, you can finish SMHC initializing by sending corresponding command one by one.

5.2.4.2. Writing a Single Data Block

To Write a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write 0x82 to SMHC_IDMAC to enable IDMAC interrupt, configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 1 data block to the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD24(Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, send CMD24 command to write data to device.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD24 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status, then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.2.4.3. Reading a Single Data Block

To read a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 1 data block from the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD17 command(Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD, send CMD17 command to read data from device to DRAM/SRAM.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD17 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.2.4.4. Writing Open-ended Multiple Data Blocks(CMD25+Auto CMD12)

To write open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks to the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25 command(Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, send CMD25 command to write data to device, when data transfer is complete, CMD12 will be sent automatically .

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status, then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.2.4.5. Reading Open-ended Multiple Data Blocks(CMD18+Auto CMD12)

To read open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks from the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18 command(Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD, send CMD18 command to read data to device, when data transfer is complete, CMD12 will be sent automatically.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD18 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.2.4.6. Writing Pre-defined Multiple Data Blocks(CMD23+CMD25)

To write pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks, setting SMHC_CMDARG to 0x3 to ensure the block number to be operated, writing 0x80000157 to SMHC_CMD to send CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25 command(Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, send CMD25 command to write data to device.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step8: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status, then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

5.2.4.7. Reading Pre-defined Multiple Data Blocks(CMD23+CMD18)

To read pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt, receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks, setting SMHC_CMDARG to 0x3 to ensure the block number to be operated, writing 0x80000157 to SMHC_CMD to send CMD23 command. Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, send CMD18 command to read data from device to DRAM/SRAM.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD18 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

5.2.5. Register List

Module Name	Base Address
SMHC0	0x04020000
SMHC1	0x04021000
SMHC2(only for V833)	0x04022000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register
SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_CTYPE	0x000C	Bus Width Register
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register
SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	FIFO Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_DBGC	0x0050	Current Debug Control Register
SMHC_CSDC	0x0054	CRC Status Detect Control Register (Only for SMHC2)
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_IDMAC	0x0080	IDMAC Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_IDST	0x0088	IDMAC Status Register
SMHC_IDIE	0x008C	IDMAC Interrupt Enable Register
SMHC_THLD	0x0100	Card Threshold Control Register
SMHC_SFC	0x0104	Sample FIFO Control Register (Only for SMHC2)

SMHC_A23A	0x0108	Auto Command 23 Argument Register (Only for SMHC2)
EMMC_DDR_SBIT_DET	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RES_CRC	0x0110	Response CRC from Device (Only for SMHC0, SMHC1)
SMHC_D7_CRC	0x0114	CRC in Data7 from Device (Only for SMHC0, SMHC1)
SMHC_D6_CRC	0x0118	CRC in Data6 from Device (Only for SMHC0, SMHC1)
SMHC_D5_CRC	0x011C	CRC in Data5 from Device (Only for SMHC0, SMHC1)
SMHC_D4_CRC	0x0120	CRC in Data4 from Device (Only for SMHC0, SMHC1)
SMHC_D3_CRC	0x0124	CRC in Data3 from Device (Only for SMHC0, SMHC1)
SMHC_D2_CRC	0x0128	CRC in Data2 from Device (Only for SMHC0, SMHC1)
SMHC_D1_CRC	0x012C	CRC in Data1 from Device (Only for SMHC0, SMHC1)
SMHC_D0_CRC	0x0130	CRC in Data0 from Device (Only for SMHC0, SMHC1)
SMHC_CRC_STA	0x0134	Write CRC Status Register (Only for SMHC0, SMHC1)
SMHC_EXT_CMD	0x0138	Extended Command Register (Only for SMHC2)
SMHC_EXT_RESP	0x013C	Extended Response Register (Only for SMHC2)
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register (Only for SMHC2)
SMHC_FIFO	0x0200	Read/Write FIFO

5.2.6. Register Description

5.2.6.1. 0x0000 SMHC Global Control Register(Default Value: 0x0000_0100)

Offset: 0x0000			**Register Name: SMHC_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 0: DMA bus 1: AHB bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit is used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit is used to calculate data line time out value defined in DTO_LMT. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL

			DDR Mode Select Although eMMC's HS400 speed mode is 8-bit DDR, this filed should be cleared when HS400_MD_EN is set. 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

5.2.6.2. 0x0004 SMHC Clock Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: SMHC_CLKDIV**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control

			0: Card clock always on 1: Turn off card clock when FSM is in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card Clock Divider n: Source clock is divided by 2*n.(n=0~255) when HS400_MD_EN is set, this field must be cleared.

5.2.6.3. 0x0008 SMHC Timeout Register(Default Value:0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit This field can set time of the Host wait for the data from the Device. Ensure to communicate with the Device, this field must be set to maximum that greater than the time N_{AC}. About the N_{AC}, the explanation is as follows: When Host read data,data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the read command(ACMD51,CMD8,CMD17,CMD18). When Host read multiple block(CMD18),a next block's data transmission from the Device starts after the access time delay N_{AC} beginning from the end bit of the previous block. When Host write data, the value is no effect.
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

5.2.6.4. 0x000C SMHC Bus Width Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: SMHC_CTYPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card Width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

5.2.6.5. 0x0010 SMHC Block Size Register(Default Value:0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block Size

5.2.6.6. 0x0014 SMHC Byte Count Register(Default Value:0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred. It must be integer multiple of Block Size(BLK_SZ) for block transfers.

5.2.6.7. 0x0018 SMHC Command Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command This bit is auto cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge When software sets this bit along in mandatory boot operation, the controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode

			00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock When this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send *Stop* or *Abort* command to stop current data transfer in progress.(CMD12, CMD52 for writing "I/O Abort" in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer If set, the **SMHC_RESP1** will record the response of auto CMD12.
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer
8	R/W	0x0	CHK_RESP_CRC Check Response CRC 0: Do not check response CRC

			1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0:Short Response (48 bits) 1:Long Response (136 bits)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without response 1: Command with response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

5.2.6.8. 0x001C SMHC Command Argument Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

5.2.6.9. 0x0020 SMHC Response 0 Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

5.2.6.10. 0x0024 SMHC Response 1 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

5.2.6.11. 0x0028 SMHC Response 2 Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

5.2.6.12. 0x002C SMHC Response 3 Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

5.2.6.13. 0x0030 SMHC Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN

			Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

5.2.6.14. 0x0034 SMHC Masked Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	M_CARD_REMOVAL_INT Card Removed
30	R/W	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R/W	0x0	M_SDIO_INT SDIO Interrupt
15	R/W	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R/W	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R/W	0x0	M_DSE_BC_INT Data Start Error When set during receiving data, it means that host controller found an error start bit. When set during transmitting data, it means that busy signal is cleared.
12	R/W	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R/W	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R/W	0x0	M_DSTO_VSD_INT

			Data Starvation Timeout/V1.8 Switch Done
9	R/W	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R/W	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R/W	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R/W	0x0	M_RCE_INT Response CRC Error
5	R/W	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R/W	0x0	M_DTR_INT Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data.
3	R/W	0x0	M_DTC_INT Data Transfer Complete
2	R/W	0x0	M_CC_INT Command Complete
1	R/W	0x0	M_RE_INT Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occurs.
0	/	/	/

5.2.6.15. 0x0038 SMHC Raw Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bits.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bits.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT

			SDIO Interrupt This is write-1-to-clear bits.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bits.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bits.
13	R/W1C	0x0	DSE_BC Data Start Error When set during receiving data, it means that host controller found a error start bit. It is valid at 4-bit or 8-bit bus mode. When it set, host finds start bit at data0, but does not find start bit at some or all of the other data lines. When set during transmitting data, it means that busy signal is cleared. This is write-1-to-clear bits.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bits.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bits.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bits.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start When set during receiving data, it means host does not find start bit on data0. This is write-1-to-clear bits.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bits.
7	R/W1C	0x0	DCE Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bits.

6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bits.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bits.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there are enough space in FIFO during transmitting data. This is write-1-to-clear bits.
3	R/W1C	0x0	DTC Data Transfer Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
2	R/W1C	0x0	CC Command Complete When set, it means that current command completes even through error occurs. This is write-1-to-clear bits.
1	R/W1C	0x0	RE Response Error When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bits.
0	/	/	/

5.2.6.16. 0x003C SMHC Status Register(Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller

10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card Data Busy Inverted version of DATA[0] 0: card data not busy 1: card data busy
8	R	0x0	CARD_PRESENT Data[3] Status Level of DATA[3], checks whether card is present 0: card not present 1: card present
7:4	R	0x0	FSM_STA Command FSM States 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO Full 1: FIFO full 0: FIFO not full
2	R	0x1	FIFO_EMPTY FIFO Empty 1: FIFO Empty 0: FIFO not Empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level Flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO RX Water Level Flag

			0: FIFO didn't reach receive trigger level 1: FIFO reached receive trigger level

5.2.6.17. 0x0040 SMHC FIFO Water Level Register(Default Value: 0x000F_0000)

Offset: 0x0040			Register Name: SMHC_FIFOTH
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst Size of Multiple Transaction 000: 1 transfers 001: 4 010: 8 011: 16 Others: Reserved It should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) FIFO_DEPTH = 256, FIFO_SIZE = 256 * 32 = 1K Recommended: MSize = 16, TX_TL = 240, RX_TL = 15 (for SMHC2) MSize = 8, TX_TL = 248, RX_TL = 7 (for SMHC0,SMHC1)
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF: Reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA is request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15, for SMHC2) 7 (means greater than 7, for SMHC0,SMHC1)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: No trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When

			FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240, for SMHC2) 248(means less than or equal to 248, for SMHC0,SMHC1)

5.2.6.18. 0x0044 SMHC Function Select Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

5.2.6.19. 0x0048 SMHC Transferred Byte Count Register 0 (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO.

			The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.2.6.20. 0x004C SMHC Transferred Byte Count Register 1 (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between Host/DMA memory and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

5.2.6.21. 0x0054 SMHC CRC Status Detect Control Register(Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 110: HS400 speed mode 011: Other speed mode

NOTE

The register is only for SMHC2.

5.2.6.22. 0x0058 SMHC Auto Command 12 Argument Register (Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A. Auto CMD12 Argument SD_A12A set the argument of command 12 automatically send by controller.

5.2.6.23. 0x005C SMHC New Timing Set Register (Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:28	/	/	/
27	R/W	0x0	DAT0_BYPASS Select data0 input asyn or bypass sample logic, it is used to check card busy or not. 0: Enable data0 bypass 1: Disable data0 bypass
26:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR Clear command line's and data lines' input phase during update clock operation. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Clear data lines' input phase before receive CRC status. 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Clear data lines' input phase before transfer data. 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Clear data lines' input phase before receive data. 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Clear command rx phase before send command. 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0 11: Ignore
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE 00: Sample timing phase offset 90^0 01: Sample timing phase offset 180^0 10: Sample timing phase offset 270^0

			11: Ignore
3:0	/	/	/

NOTE

This register is valid for SMHC0,SMHC1.

5.2.6.24. 0x0078 SMHC Hardware Reset Register (Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

5.2.6.25. 0x0080 SMHC IDMAC Control Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_IDMAC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When IDMAC fetches a descriptor, if the valid bit of a descriptor is not set, IDMAC FSM will go to the suspend state. Setting this bit will make IDMAC refetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	Reserved
7	R/W	0x0	IDMAC_ENB IDMAC Enable When set, the IDMAC is enabled.
6:2	R/W	0x0	Reserved
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

5.2.6.26. 0x0084 SMHC Descriptor List Base Address Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List Contains the base address of the First Descriptor. For SMHC0, SMHC1, it is a word address. For SMHC2, it is a byte address.

5.2.6.27. 0x0088 SMHC IDMAC Status Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_IDST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	Reserved
12:10	R	0x0	IDMAC_ERR_STA Error Bits Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (IDSTS[2]) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved The bit is read-only.
9	R/W1C	0x0	ABN_INT_SUM(AIS) Abnormal Interrupt Summary Logical OR of the following: IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: Descriptor Unavailable bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM(NIS) Normal Interrupt Summary Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM

			Card Error Summary Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt Indicates that a Bus Error occurred (IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit.

5.2.6.28. 0x008C SMHC IDMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	Reserved
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error Summary Interrupt Enable. When set, it enables the Card Interrupt Summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the Descriptor

			Unavailable interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

5.2.6.29. 0x0100 SMHC Card Threshold Control Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_RD_THLD Card Read Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB (only for SMHC2) Card Write Threshold Enable(HS400) 0: Card write threshold disabled 1: Card write threshold enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy clear interrupt disabled 1: Busy clear interrupt enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card read threshold disabled 1: Card read threshold enabled Host controller initiates Read Transfer only if CARD_RD_THLD amount of space is available in receive FIFO.

5.2.6.30. 0x0104 SMHC Sample FIFO Control Register (Default Value: 0x0000_0006)

Offset: 0x0104			Register Name: SMHC_SFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:1	R/W	0x3	STOP_CLK_CTRL Stop Clock Control When receiving data, if CARD_RD_THLD_ENB is set and CARD_RD_THLD is set same with BLK_SZ, the device clock may stop at block gap during data receiving. This field is used to control the position of stopping clock. The value can be changed between 0x0 and 0xF, but actually the available value and the position of stopping clock must be decided by the actual situation. The value increases one in this field is linked to one cycle(two cycles in DDR mode) that the position of stopping clock moved up.
0	R/W	0x0	BYPASS_EN Bypass enable When set, sample FIFO will be bypassed.

NOTE

The register is for SMHC2.

5.2.6.31. 0x0108 SMHC Auto Command 23 Argument Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: SMHC_A23A
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	A23A Auto CMD23 Argument The argument of command 23 is automatically sent by controller with this field.

NOTE

The register is for SMHC2.

5.2.6.32. 0x010C SMHC eMMC4.5 DDR Start Bit Detection Control Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: EMMC_DDR_SBIT_DET
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable

			It is required to set this bit to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications.

5.2.6.33. 0x0110 SMHC Response CRC Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: SMHC_RESP_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.34. 0x0114 SMHC Data7 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: SMHC_DAT7_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT7_CRC Data[7] CRC CRC in data[7] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.35. 0x0118 SMHC Data6 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0118	Register Name: SMHC_DAT6_CRC

Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DAT6_CRC Data[6] CRC CRC in data[6] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.36. 0x011C SMHC Data5 CRC Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SMHC_DAT5_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT5_CRC Data[5] CRC CRC in data[5] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, it is not used. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.37. 0x0120 SMHC Data4 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: SMHC_DAT4_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT4_CRC Data[4] CRC CRC in data[4] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.38. 0x0124 SMHC Data3 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: SMHC_DAT3_CRC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DAT3_CRC Data[3] CRC CRC in data[3] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.39. 0x0128 SMHC Data2 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: SMHC_DAT2_CRC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DAT2_CRC Data[2] CRC CRC in data[2] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.40. 0x012C SMHC Data1 CRC Register (Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: SMHC_DAT1_CRC
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DAT1_CRC Data[1] CRC CRC in data[1] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data.

			In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.41. 0x0130 SMHC Data0 CRC Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: SMHC_DAT0_CRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT0_CRC Data[0] CRC CRC in data[0] from device. In 8 bits DDR mode, the higher 16 bits indicate the CRC of even data, and the lower 16 bits indicate the CRC of odd data. In 4 bits DDR mode, the higher 16 bits indicate the CRC of odd data, and the lower 16 bits indicate the CRC of even data. In SDR mode, the higher 16 bits indicate the CRC of all data.

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.42. 0x0134 SMHC CRC Status Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: SMHC_CRC_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	CRC_STA CRC Status CRC status from device in write operation Positive CRC status token: 3’b010 Negative CRC status token: 3’b101

NOTE

This register is valid for SMHC0, SMHC1.

5.2.6.43. 0x0138 SMHC Extended Command Register (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: SMHC_EXT_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	AUTO_CMD23_EN

			Send CMD23 Automatically When setting this bit, send CMD23 automatically before send command specified in SMHC_CMD register. When SOFT_RST is set, this field will be cleared.

NOTE

This register is valid for SMHC2.

5.2.6.44. 0x013C SMHC Extended Response Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: SMHC_EXT_RESP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SMHC_EXT_RESP When AUTO_CMD23_EN is set, this register stores the response of CMD23.

NOTE

This register is valid for SMHC2.

5.2.6.45. 0x0140 SMHC Drive Delay Control Register (Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select For SMHC0,SMHC1: 0: Data drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode 1: Data drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode For SMHC2: 0: Data drive phase offset is 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4/HS400 mode 1: Data drive phase offset is 180^0 at SDR mode, 90^0 at DDR8 mode, 0^0 at DDR4/HS400 mode
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select For SMHC0,SMHC1: 0: Command drive phase offset is 90^0 at SDR mode, 45^0 at DDR mode 1: Command drive phase offset is 180^0 at SDR mode, 90^0 at DDR mode For SMHC2: 0: Command drive phase offset is 90^0 at SDR mode, 45^0 at DDR8 mode, 90^0 at DDR4/HS400 mode

			1: Command drive phase offset is 180^0 at SDR mode, 90^0 at DDR8 mode, 180^0 at DDR4/HS400 mode
15:0	/	/	/

5.2.6.46. 0x0144 SMHC Sample Delay Control Register (Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in SAMP_DL.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at SAMP_DL_SW
6	/	/	/
5:0	R/W	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of SAMP_DL, the cycle of card clock and device's input timing requirement.

5.2.6.47. 0x0148 SMHC Data Strobe Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0148			Register Name: SMHC_DS_DL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.

14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in DS_DL.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when SAMP_DL_CAL_DONE is set.
7	R/W	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	R/W	0x0	DS_DL_SW Data Strobe Delay Software

5.2.6.48. 0x0200 SMHC FIFO Register (Default Value: 0x0000_0000)

Offset: 0x0200			**Register Name: SMHC_FIFO**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

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Chapter 6 EMAC

6.1. Overview

The Ethernet Medium Access Controller (EMAC) enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10/100/1000 Mbit/s external PHY with RMII/RGMII interface in both full and half duplex mode. The Internal DMA is designed for packet-oriented data transfers based on a linked list of descriptors. 4KBytes TXFIFO and 16KBytes RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are also supported in this module.

The EMAC has the following features:

- Supports 10/100/1000 Mbit/s data transfer rates
- Supports RMII/RGMII PHY interface
- Supports MDIO
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KBytes
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KBytes of data
- Comprehensive status reporting for normal operation and transfers with errors
- 4 KBytes TXFIFO for transmission packets and 16 KBytes RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

NOTE

V833 supports 10/100/1000 Mbit/s Ethernet port with RGMII and RMII interfaces, V831 supports 10/100 Mbit/s Ethernet port with RMII interface.

6.2. Block Diagram

The block diagram of EMAC is shown below.

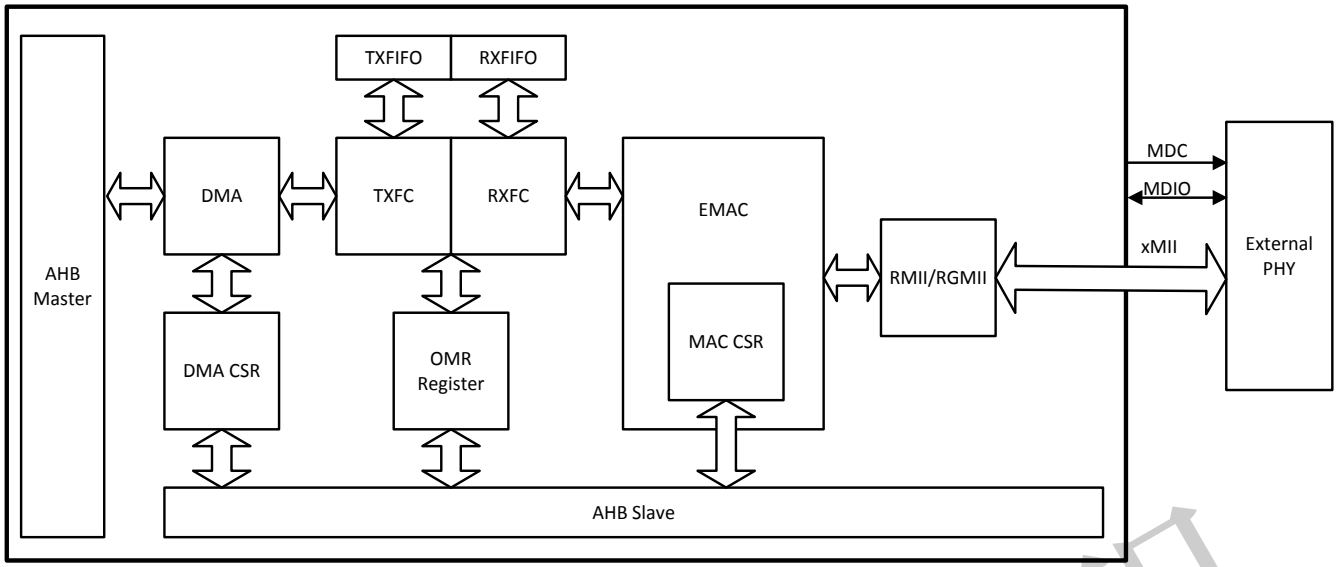

Figure 6- 1. EMAC Block Diagram

6.3. Operations and Functional Descriptions

6.3.1. External Signals

Table 6-1 describes the pin mapping of EMAC.

Table 6- 1. EMAC Pin Mapping

Pin Name	RGMII(only for V833)	RMII
RGMII_RXD3	RXD3	
RGMII_RXD2	RXD2	
RGMII_RXD1/RMII_RXD1	RXD1	RXD1
RGMII_RXD0/RMII_RXD0	RXD0	RXD0
RGMII_RXCK	RXCK	
RGMII_RXCTL/RMII_CRS_DV	RXCTL	CRS_DV
RGMII_CLKIN/ RMII_RXER	CLKIN	RXER
RGMII_TXD3	TXD3	
RGMII_TXD2	TXD2	
RGMII_TXD1/RMII_TXD1	TXD1	TXD1
RGMII_TXD0/RMII_TXD0	TXD0	TXD0
RGMII_TXCK/RMII_TXCK	TXCK	TXCK
RGMII_TXCTL/RMII_TXEN	TXCTL	TXEN
MDC	MDC	MDC
MDIO	MDIO	MDIO
EPHY_25M	EPHY_25M	EPHY_25M

Table 6-2 describes the pin list of RGMII.

Table 6- 2. EMAC RGMII Pin List

Pin Name	Description	Type
RGMII_TXD[3:0]	EMAC RGMII Transmit Data	O
RGMII_TXCTL	EMAC RGMII Transmit Control	O
RGMII_TXCK	EMAC RGMII Transmit Clock	O
RGMII_RXD[3:0]	EMAC RGMII Receive Data	I
RGMII_RXCTL	EMAC RGMII Receive Control	I
RGMII_RXCK	EMAC RGMII Receive Clock	I
RGMII_CKIN	EMAC RGMII 125M Reference Clock Input	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O
EPHY_25M	25MHz Output for EMAC PHY	O

Table 6-3 describes the pin list of RMII.

Table 6- 3. EMAC RMII Pin List

Pin Name	Description	Type
RMII_TXD[1:0]	EMAC RMII Transmit Data	O
RMII_TXEN	EMAC RMII Transmit Enable	O
RMII_TXCK	EMAC RMII Transmit Clock	I
RMII_RXD[1:0]	EMAC RMII Receive Data	I
RMII_CRS_DV	EMAC RMII Receive Data Valid	I
RMII_RXER	EMAC RMII Receive Error	I
MDC	EMAC Management Data Clock	O
MDIO	EMAC Management Data Input Output	I/O
EPHY_25M	25MHz Output for EMAC PHY	O

6.3.2. Clock Sources

Table 6-4 describes the clock of EMAC.

Table 6- 4. EMAC Clock Characteristics

Clock Name	Description	Type
RGMII_TXCK/ RMII_TXCK	In RGMII mode, output 2.5MHz/25MHz/125MHz. In RMII mode, input 5MHz/50MHz.	O/I
RGMII_RXCK	In RGMII mode, input 2.5MHz/25MHz/125MHz. In RMII mode, no input.	I

RGMII_CLKIN	In RGMII mode, input 125MHz Reference Clock In RMII mode, no clock.	I

6.3.3. Typical Application

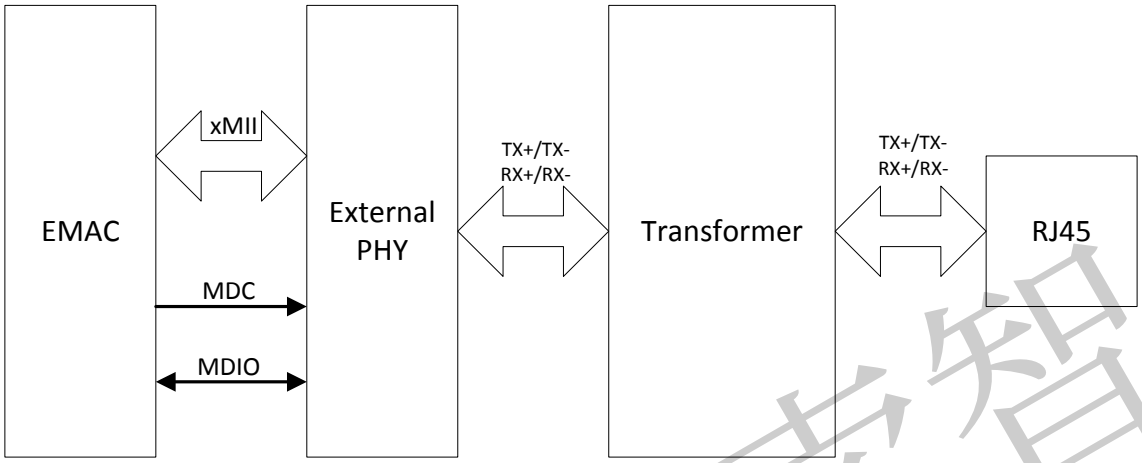

Figure 6- 2. EMAC Typical Application

6.3.4. EMAC RX/TX Descriptor

The internal DMA of EMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in Figure 6-3. The address of each descriptor must be 32-bit aligned.

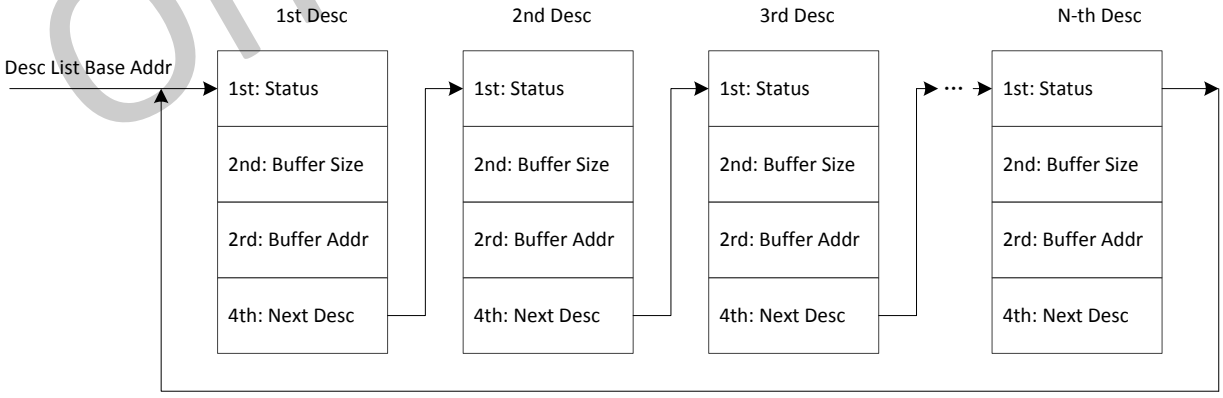

Figure 6- 3. EMAC RX/TX Descriptor List

6.3.5. Transmit Descriptor

6.3.5.1. 1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.
1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the EMAC defers the frame transmission.

6.3.5.2. 2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.

28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

6.3.5.3. 3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

6.3.5.4. 4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

6.3.6. Receive Descriptor

6.3.6.1. 1st Word of Receive Descriptor

Bits	Description
31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame does not pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved
14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame donot pass SA filter.
12	Reserved
11	RX_OVERFLOW_ERR

	When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR When set, there is a late collision during reception in half-duplex mode.
5	Reserved.
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.
2	Reserved.
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

6.3.6.2. 2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When set and a frame have been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

6.3.6.3. 3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

6.3.6.4. 4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

6.4. Register List

Module Name	Base Address
EMAC0	0x05020000

Register Name	Offset	Description
EMAC_BASIC_CTL0	0x0000	EMAC Basic Control Register0
EMAC_BASIC_CTL1	0x0004	EMAC Basic Control Register1
EMAC_INT_STA	0x0008	EMAC Interrupt Status Register
EMAC_INT_EN	0x000C	EMAC Interrupt Enable Register
EMAC_TX_CTL0	0x0010	EMAC Transmit Control Register0
EMAC_TX_CTL1	0x0014	EMAC Transmit Control Register1
EMAC_TX_FLOW_CTL	0x001C	EMAC Transmit Flow Control Register
EMAC_TX_DMA_DESC_LIST	0x0020	EMAC Transmit Descriptor List Address Register
EMAC_RX_CTL0	0x0024	EMAC Receive Control Register0
EMAC_RX_CTL1	0x0028	EMAC Receive Control Register1
EMAC_RX_DMA_DESC_LIST	0x0034	EMAC Receive Descriptor List Address Register
EMAC_RX_FRM_FLT	0x0038	EMAC Receive Frame Filter Register
EMAC_RX_HASH0	0x0040	EMAC Hash Table Register0
EMAC_RX_HASH1	0x0044	EMAC Hash Table Register1
EMAC_MII_CMD	0x0048	EMAC Management Interface Command Register
EMAC_MII_DATA	0x004C	EMAC Management Interface Data Register
EMAC_ADDR_HIGH0	0x0050	EMAC MAC Address High Register0
EMAC_ADDR_LOW0	0x0054	EMAC MAC Address Low Register0
EMAC_ADDR_HIGHx	0x0050+0x08*N(N=1~7)	EMAC MAC Address High RegisterN(N:1~7)
EMAC_ADDR_LOWx	0x0054+0x08*N(N=1~7)	EMAC MAC Address Low RegisterN(N:1~7)
EMAC_TX_DMA_STA	0x00B0	EMAC Transmit DMA Status Register
EMAC_TX_CUR_DESC	0x00B4	EMAC Current Transmit Descriptor Register
EMAC_TX_CUR_BUF	0x00B8	EMAC Current Transmit Buffer Address Register
EMAC_RX_DMA_STA	0x00C0	EMAC Receive DMA Status Register
EMAC_RX_CUR_DESC	0x00C4	EMAC Current Receive Descriptor Register
EMAC_RX_CUR_BUF	0x00C8	EMAC Current Receive Buffer Address Register
EMAC_RGMII_STA	0x00D0	EMAC RGMII Status Register

6.5. Register Description

6.5.1. 0x0000 EMAC Basic Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMAC_BASIC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000 Mbit/s 01: Reserved 10: 10 Mbit/s 11: 100 Mbit/s
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable
0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

6.5.2. 0x0004 EMAC Basic Control Register1 (Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: EMAC_BASIC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA priority 0: Same priority 1: RX priority over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.

6.5.3. 0x0008 EMAC Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: EMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this asserted, the RX DMA cannot acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when writing to RX_DMA_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P

			Frame is transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when writing to TX_DMA_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear it.

6.5.4. 0x000C EMAC Interrupt Enable Register (Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: EMAC_INT_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt

			0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable
8	R/W	0x0	RX_INT_EN Receive Interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit Interrupt 0: Disable 1: Enable

6.5.5. 0x0010 EMAC Transmit Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: EMAC_TX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable Transmitter 0: Disable 1: Enable When disable, transmit will continue until current transmit finishes.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off.
29:0	/	/	/

6.5.6. 0x0014 EMAC Transmit Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start It is cleared internally and always read a 0
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission. 1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH Threshold value of TX DMA FIFO When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode

			0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO 0: Enable 1: Disable

6.5.7. 0x001C EMAC Transmit Flow Control Register (Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/
21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

6.5.8. 0x0020 EMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

6.5.9. 0x0024 EMAC Receive Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable Receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant
28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC Enable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

6.5.10. 0x0028 EMAC Receive Control Register1 (Default Value: 0x0000_0000)

Offset: 0x0028	Register Name: EMAC_RX_CTL1

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	RX_DMA_START When set, the RX DMA will not work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable,base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 **NOTE** **Only valid when RX_MD == 0, full frames with a length less than the threshold are transferred automatically.**
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD

			Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when receive descriptors/buffers is unavailable 1: Disable

6.5.11. 0x0034 EMAC Receive DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: EMAC_RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

6.5.12. 0x0038 EMAC Receive Frame Filter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: EMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable
30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast Frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast Frames Filter 0: Filter according to HASH_MULTICAST 1: Receive All
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter Multicast Frames Set

			0: by comparing the DA field in DA MAC address registers 1: according to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass Frames whose SA field matches SA MAC address registers 1: Pass Frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it passes the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)
0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

6.5.13. 0x0040 EMAC Receive Hash Table Register0 (Default Value: 0x0000_0000)

Offset: 0x0040			**Register Name: EMAC_RX_HASH0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

6.5.14. 0x0044 EMAC Receive Hash Table Register1 (Default Value: 0x0000_0000)

Offset: 0x0044	**Register Name: EMAC_RX_HASH1**

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

6.5.15. 0x0048 EMAC MII Command Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved **NOTE** **MDC Clock is divided from AHB clock.**
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write
0	R/W	0x0	MII_BUSY 0: Write no valid, read 0 indicates finish in read or write operation 1: Write start read or write operation, read 1 indicates busy.

6.5.16. 0x004C EMAC MII Data Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Write to or read from the register in the selected PHY.

6.5.17. 0x0050 EMAC MAC Address High Register0 (Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: EMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16 bits of the 1st MAC address.

6.5.18. 0x0054 EMAC MAC Address Low Register0 (Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: EMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32 bits of 1st MAC address.

6.5.19. 0x0050+0x08*N EMAC MAC Address High Register N (Default Value: 0x0000_0000)

Offset: 0x0050+0x08*N (N=1~7)			Register Name: EMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address Valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: Used to compare with the destination address of the received frame 1: Used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC Address Byte Control Mask The lower bit of mask controls the lower byte of MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/
15:0	R/W	0x0	MAC_ADDR_HIGH The upper 16bits of the MAC address.

6.5.20. 0x0054+0x08*N EMAC MAC Address Low Register N (Default Value: 0x0000_0000)

Offset: 0x0054+0x08*N (N=1~7)			Register Name: EMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32bits of MAC address N (N: 1~7).

6.5.21. 0x00B0 EMAC Transmit DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: EMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The State of Transmit DMA FSM 000: STOP, When reset or disable TX DMA 001: RUN_FETCH_DESC, Fetching TX DMA descriptor 010: RUN_WAIT_STA, Waiting for the status of TX frame 011: RUN_TRANS_DATA, Passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 111: RUN_CLOSE_DESC, Closing TX descriptor 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow

6.5.22. 0x00B4 EMAC Transmit DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: EMAC_TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

6.5.23. 0x00B8 EMAC Transmit DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: EMAC_TX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit DMA buffer.

6.5.24. 0x00C0 EMAC Receive DMA Status Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: EMAC_RX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	RX_DMA_STA The State of RX DMA FSM 000: STOP, When reset or disable RX DMA 001: RUN_FETCH_DESC, Fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, Waiting for frame

			100: SUSPEND, RX descriptor unavailable 101: RUN_CLOSE_DESC, Closing RX descriptor 110: Reserved 111: RUN_TRANS_DATA, Passing frame from host memory to RX DMA FIFO;

6.5.25. 0x00C4 EMAC Receive DMA Current Descriptor Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: EMAC_RX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive descriptor

6.5.26. 0x00C8 EMAC Receive DMA Current Buffer Address Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: EMAC_RX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive DMA buffer

6.5.27. 0x00D0 EMAC RGMII Status Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: EMAC_RGMII_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface 0: down 1: up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

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Chapter 7 Video Output Interfaces

7.1. TCON_LCD

7.1.1. Overview

The TCON_LCD(Timing Controller_LCD) is a module that processes video signals received from system through a complicated arithmetic and then generates control signals and transmits them to the LCD panel driver IC.

The TCON_LCD includes the following features.

V833:

- Parallel RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- i8080 interface, up to 800 x 480@60fps
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

V831:

- Serial RGB/dummy RGB interface, up to 320 x 240@60fps
- i8080 interface, up to 320 x 240@60fps
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence

NOTE

The LCD of V833 is 24-bit data interface; the LCD of V831 is 8-bit data interface.

7.1.2. Block Diagram

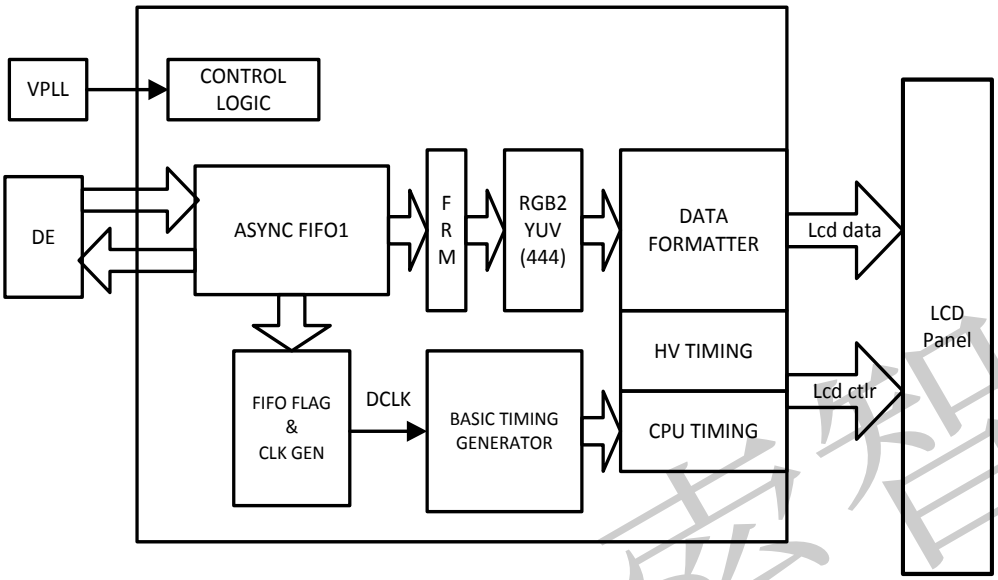

Figure 7- 1. TCON_LCD Block Diagram

7.1.3. Operations and Functional Descriptions

7.1.3.1. External Signals

The LCD external signals are used to connect to panel interface. The panel interface has various types. The signals of V833 package and V831 package are as follows.

Table 7- 1. LCD External Signals

V833 Signal	V831 Signal	Type	Description
LCD_D0	/	O	LCD data0
LCD_D1	/	O	LCD data1
LCD_D2	/	O	LCD data2
LCD_D3	LCD_D3	O	LCD data3
LCD_D4	LCD_D4	O	LCD data4
LCD_D5	LCD_D5	O	LCD data5
LCD_D6	LCD_D6	O	LCD data6
LCD_D7	LCD_D7	O	LCD data7
LCD_D8	/	O	LCD data8
LCD_D9	/	O	LCD data9
LCD_D10	LCD_D10	O	LCD data10
LCD_D11	LCD_D11	O	LCD data11
LCD_D12	LCD_D12	O	LCD data12
LCD_D13	/	O	LCD data13

LCD_D14	/	O	LCD data14
LCD_D15	/	O	LCD data15
LCD_D16	/	O	LCD data16
LCD_D17	/	O	LCD data17
LCD_D18	/	O	LCD data18
LCD_D19	/	O	LCD data19
LCD_D20	/	O	LCD data20
LCD_D21	/	O	LCD data21
LCD_D22	/	O	LCD data22
LCD_D23	/	O	LCD data23
LCD_CLK	LCD_CLK	O	LCD clock
LCD_DE	LCD_DE	O	LCD data enable
LCD_HSYNC	LCD_HSYNC	O	LCD horizontal sync
LCD_VSYNC	LCD_VSYNC	O	LCD vertical sync

7.1.3.1.1. Control Signal and Data Port Mapping

I/O	SYNC RGB					CPU cmd	CPU 18bit	CPU 16bit								CPU 8bit							CPU 9bit	
	Para RGB	SerialRGB			COR 666		256K	256K							65K	256K			65K			256K	
		1st	2nd	3rd				1st	2nd	3rd	1st	2nd	1st	2nd		1st	2nd	3rd	1st	2nd	1st	2nd		
IO0	VSYNC					CS																		
IO1	HSYNC					RD																		
IO2	DCLK					WR																		
IO3	DE					RS																		
D23	R7					D23	R5	R5	B5	G5	R5		R5	B5	R4									
D22	R6					D22	R4	R4	B4	G4	R4		R4	B4	R3									
D21	R5					D21	R3	R3	B3	G3	R3		R3	B3	R2									
D20	R4					D20	R2	R2	B2	G2	R2		R2	B2	R1									
D19	R3					D19	R1	R1	B1	G1	R1		R1	B1	R0									
D18	R2					D18	R0	R0	B0	G0	R0		R0	B0	G5									
D17	R1					D17																		
D16	R0					D16																		
D15	G7					D15	G5								G4									
D14	G6					D14	G4								G3									
D13	G5					D13	G3																	
D12	G4	D17	D27	D37	D7	D12	G2	G5	R5	B5	G5	B5	G5		G2	R5	G5	B5	R4	G2	R5	G2		
D11	G3	D16	D26	D36	D6	D11	G1	G4	R4	B4	G4	B4	G4		G1	R4	G4	B4	R3	G1	R4	G1		
D10	G2	D15	D25	D35	D5	D10	G0	G3	R3	B3	G3	B3	G3		G0	R3	G3	B3	R2	G0	R3	G0		
D9	G1					D9																		
D8	G0					D8																		
D7	B7	D14	D24	D34	D4	D7	B5	G2	R2	B2	G2	B2	G2		B4	R2	G2	B2	R1	B4	R2	B5		
D6	B6	D13	D23	D33	D3	D6	B4	G1	R1	B1	G1	B1	G1		B3	R1	G1	B1	R0	B3	R1	B4		
D5	B5	D12	D22	D32	D2	D5	B3	G0	R0	B0	G0	B0	G0		B2	R0	G0	B0	G5	B2	R0	B3		
D4	B4	D11	D21	D31	D1	D4	B2								B1				G4	B1	G5	B2		
D3	B3	D10	D20	D30	D0	D3	B1								B0				G3	B0	G4	B1		
D2	B2					D2	B0														G3	B0		
D1	B1					D1																		
D0	B0					D0																		

For parallel RGB, the data of LCD is high-aligned. The correspondence is as follows.

V833 LCD I/O	Parallel RGB		
	RGB888	**RGB565**	**RGB666**
LCD_D23	R7	R4	R5
LCD_D22	R6	R3	R4
LCD_D21	R5	R2	R3
LCD_D20	R4	R1	R2
LCD_D19	R3	R0	R1
LCD_D18	R2		R0
LCD_D17	R1		

LCD_D16	R0		
LCD_D15	G7	G5	G5
LCD_D14	G6	G4	G4
LCD_D13	G5	G3	G3
LCD_D12	G4	G2	G2
LCD_D11	G3	G1	G1
LCD_D10	G2	G0	G0
LCD_D9	G1		
LCD_D8	G0		
LCD_D7	B7	B4	B5
LCD_D6	B6	B3	B4
LCD_D5	B5	B2	B3
LCD_D4	B4	B1	B2
LCD_D3	B3	B0	B1
LCD_D2	B2		B0
LCD_D1	B1		
LCD_D0	B0		

7.1.3.1.2. HV Interface (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 application.

Table 7- 2. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicates one new scan line	O
DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
D[23..0]	24-bit RGB output from input FIFO for panel	O

The timing diagram of HV interface is as follows.

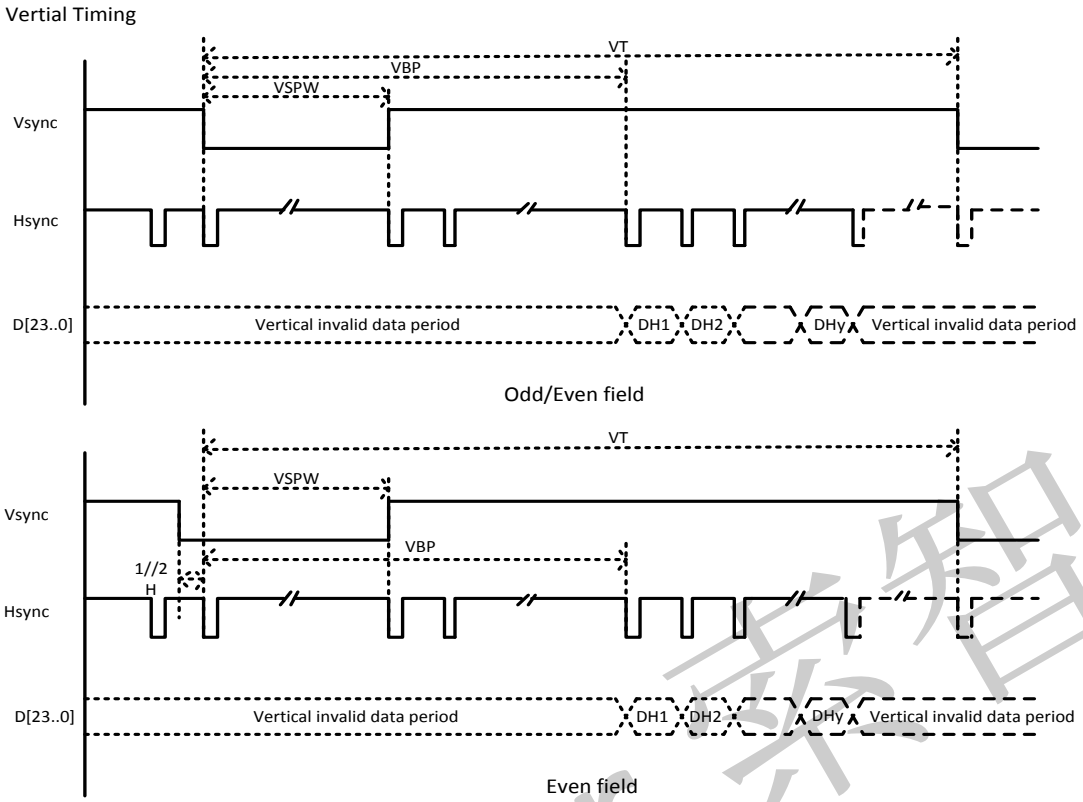

Figure 7- 2. HV Interface Vertical Timing

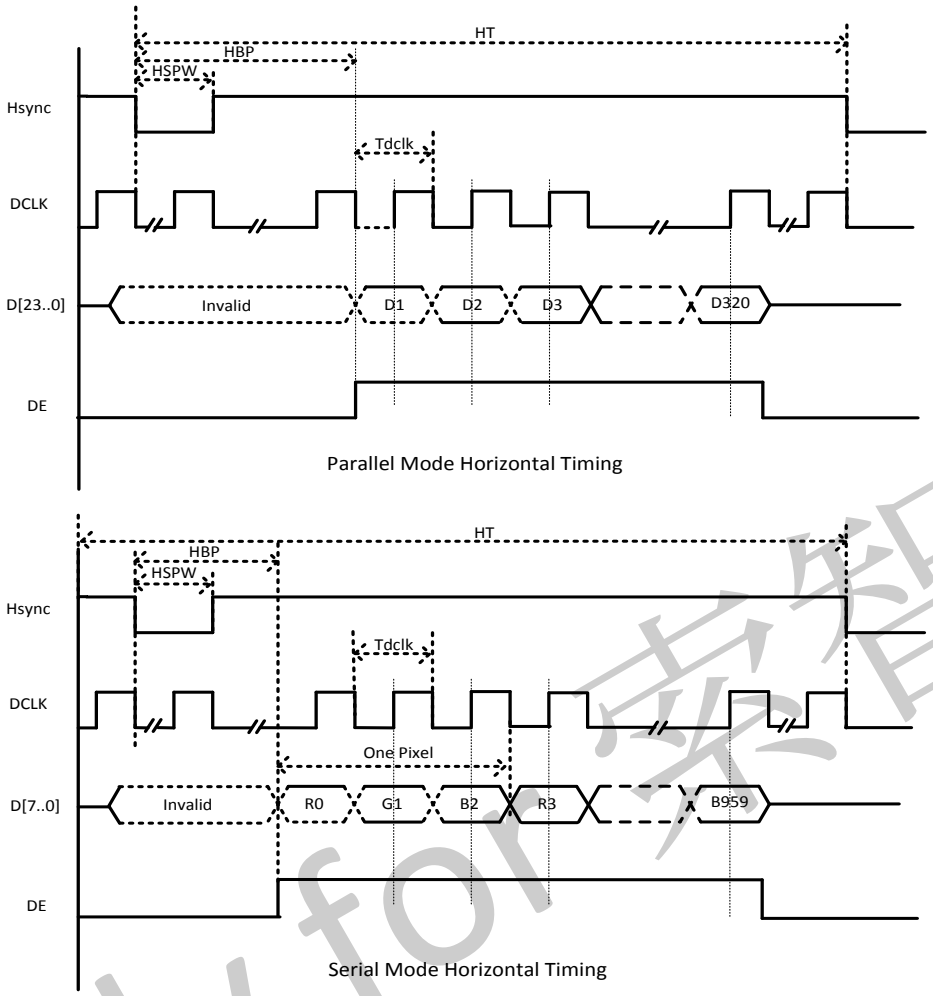

Figure 7- 3. HV Interface Horizontal Timing

7.1.3.1.3. BT656 Interface

In HV serial YUV output mode, its timing is BT656 compatible. SAV adds right before active area every line; EAV adds right after active area every line.

Table 7- 3. BT656 Panel Signals

Signal	Description	Type
DCLK	Clock signal	O
DATA[7:0]	Data signal	O

Its logic is:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕ H

P2 = F ⊕ H

P1 = F ⊕ V

P0 = F ⊕ V ⊕ H

Where ⊕ represents the exclusive-OR function

The 4 byte SAV/EAV sequence is as follows.

Table 7- 4. EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9(MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

7.1.3.1.4. i8080 Interface

i8080 I/F LCD panel is most common interface for small size, low resolution LCD panels. CPU control signals are active low.

Table 7- 5. CPU Panel Signals

Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180° delay of DCLK; CS is active when pixel data is valid; RD is always set to 1; A1 is set by “LCD_CPUI/F”.

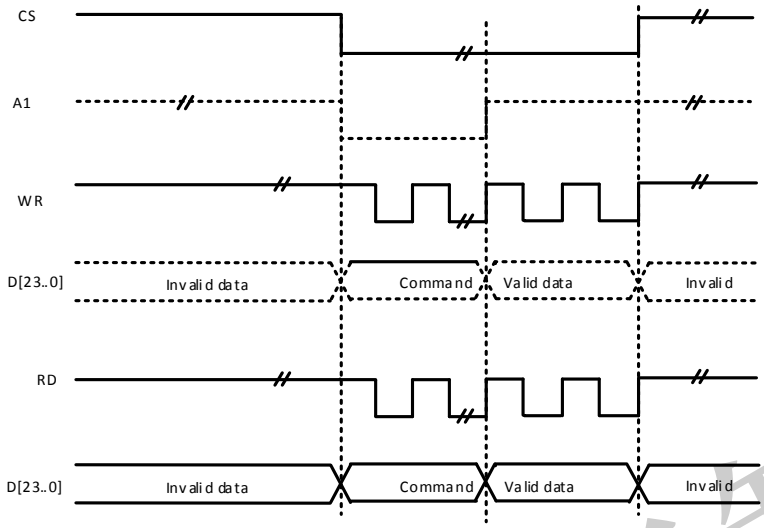

Figure 7- 4. i8080 Interface Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

7.1.3.2. Clock Sources

The following table describes the clock sources of TCON_LCD. Table 7-6 describes the clock sources of TCON_LCD.

Table 7- 6. TCON_LCD Clock Sources

Clock Sources	Description
PLL_VIDEO0(1X)	Video PLL Clock, default value is 297MHz
PLL_VIDEO0(4X)	Video PLL Clock, default value is 1188MHz

7.1.3.3. RGB Gamma Correction

Function: This module correct the RGB input data of DE.

A 256*8*3 Byte register file is used to store the gamma table. The following is the layout.

Table 7- 7. RGB Gamma Correction Table

Offset	Value
0x400	{ B0[7:0], G0[7:0], R0[7:0] }
0x404	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....

0x7FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.1.3.4. CEU Module

This module enhances color data from DE .

R’ = ((Rr*R + Rg*G + Rb*B +16)/16+ Rc+16)/16

G’ = ((Gr*R + Gg*G + Gb*B +16)/16+Gc+16)/16

B’ = ((Br*R + Bg*G + Bb*B +16)/16+ Bc+16)/16

NOTE

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb	**s13**	**(-16,16)**
Rc, Gc, Bc	**s19**	**(-16384, 16384)**
R, G, B	**u8**	**[0-255]**

R’ has the range of [Rmin ,Rmax]

G’ has the range of [Rmin ,Rmax]

B’ has the range of [Rmin ,Rmax]

7.1.3.5. CMAP Module

Function: This module map color data from DE.

Every 4 input pixels as a unit. A unit is divided into 12 bytes. Output byte can select one of those 12 bytes. Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).

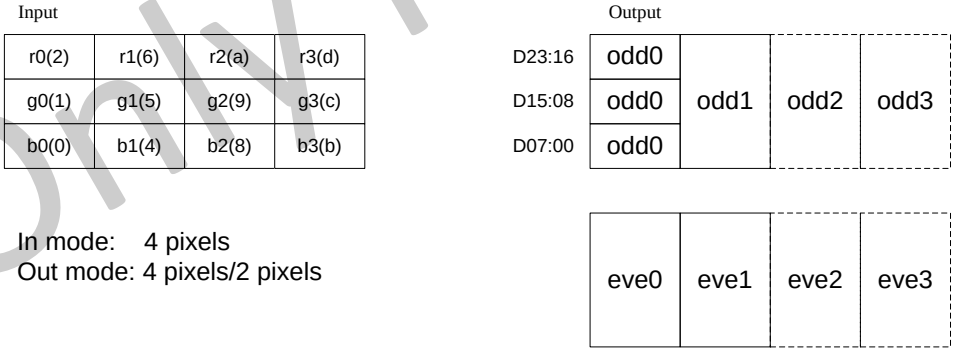

Figure 7- 5. CMAP Module

7.1.4. Programming Guidelines

7.1.4.1. HV Mode Configuration Process

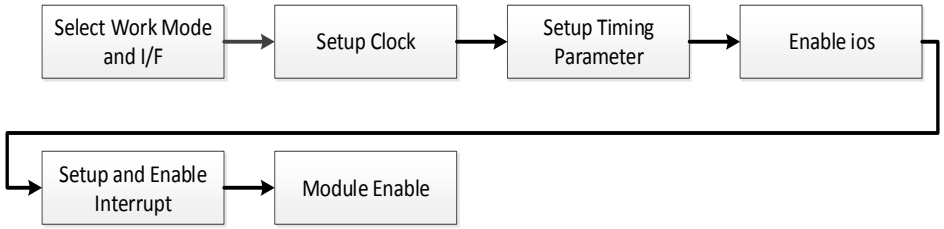

Figure 7- 6. HV Mode Initial Process

Step1: Select HV interface type: parallel RGB or serial RGB.

Step2: Set clock, if phase changing function need be used, then the bit[31:28] of **LCD_DCLK_REG** should be set to 0xf.

Step3: Set timing parameter x,ht,hbp,hspw,y,vt,vbp,vspw. Note that hbp includes hspw, vbp includes vspw, and vt needs be set to twice as actual value.

Step4: Open IO output.

Step5: Set and open interrupt function. Note that when using line interrupt, the **LCD_LINE_INT_NUM** bit of **LCD_GINT1_REG** need be set first, then **LCD_LINE_INT_EN** bit of **LCD_GINT0_REG** is set to 1.

Step6: Open module enable.

7.1.4.2. i8080 Configuration Process

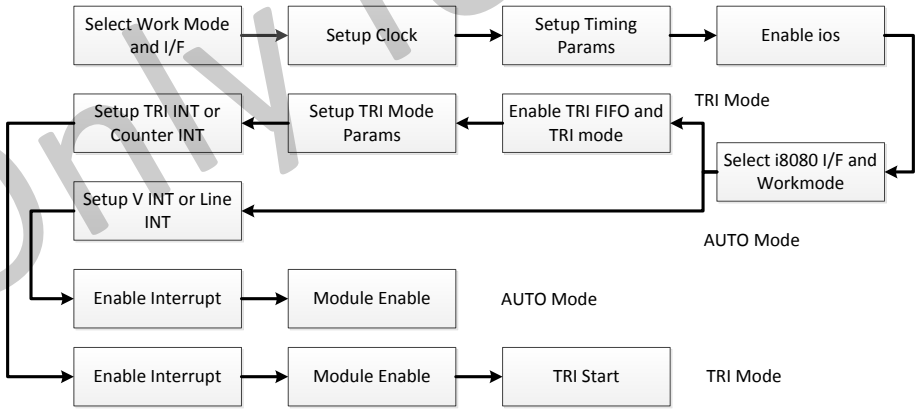

Figure 7- 7. i8080 Mode Initial Process

Step1: Select i8080 interface type.

Step2: The step is the same as HV mode, but pulse adjustment function is invalid.

Step3: The step is the same as HV mode. When using TRI mode, it is best to configure LCD timing parameters in HV mode, or a handful of functions such as CMAP will not be able to apply.

Step4: The step is the same as HV mode.

Step5: Select type and operating mode of i8080, the operating mode includes TRI mode and AUTO mode, and the two operating modes are different.

----------**TRI mode**----------

Step6: Open TRI FIFO switch, and TRI mode function.

Step7: Set parameters of TRI mode, including block size, block space and block number.

NOTE

When output interface is parallel mode, then the setting value of block space parameter is not less than 20.
When output interface is 2 cycle serial mode, then the setting value of block space parameter is not less than 40.
When output interface is 3 cycle serial mode, then the setting value of block space parameter is not less than 60.
When output interface is 4 cycle serial mode, then the setting value of block space parameter is not less than 80.

Step8: Set the tri interrupt or counter interrupt. When using the two interrupts, mainly in the interrupt service function the tri start operation need be operated (the bit1 of LCD_CPU_IF_REG is set to"1"). If using TE trigger interrupt, you select the external input pin as a trigger signal, the 24-bit for offset 0x8C register is set to "1", to open up input of pad.
Step9: Open interrupt total switch.
Step10: Open interrupt total enable.
Step11: Operate tri start operation(the bit1 of LCD_CPU_IF_REG is set to"1")

----------**Auto mode**----------

Step6: Set and open V interrupt or Line interrupt, the step is the same as HV mode.
Step7: Open module total enable.

7.1.4.3. Notes of MIPI DSI Mode

Notes of using MIPI DSI mode:
(1) Using DSI display, data clk of TCON_LCD should start first.
(2) When using TCON_LCD in conjunction with DSI video mode, the block space parameter should satisfy the following relationship:

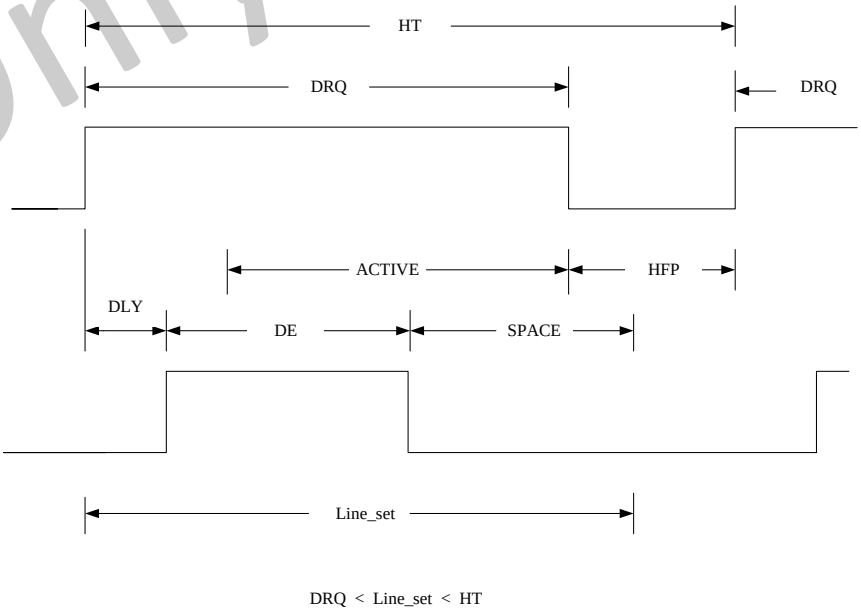

Figure 7- 8. DSI Video Mode Data Request Timing

7.1.5. Register List

Module Name	Base Address
TCON_LCD0	0x06511000

Register Name	Offset	Description
LCD_GCTL_REG	0x0000	LCD Global Control Register
LCD_GINT0_REG	0x0004	LCD Global Interrupt Register0
LCD_GINT1_REG	0x0008	LCD Global Interrupt Register1
LCD_FRM_CTL_REG	0x0010	LCD FRM Control Register
LCD_FRM_SEED_REG	0x0014+N*0x04	LCD FRM Seed Register(N=0,1,2,3,4,5)
LCD_FRM_TAB_REG	0x002C+N*0x04	LCD FRM Table Register(N=0,1,2,3)
LCD_3D_FIFO_REG	0x003C	LCD 3D FIFO Register
LCD_CTL_REG	0x0040	LCD Control Register
LCD_DCLK_REG	0x0044	LCD Data Clock Register
LCD_BASIC0_REG	0x0048	LCD Basic Timing Register0
LCD_BASIC1_REG	0x004C	LCD Basic Timing Register1
LCD_BASIC2_REG	0x0050	LCD Basic Timing Register2
LCD_BASIC3_REG	0x0054	LCD Basic Timing Register3
LCD_HV_IF_REG	0x0058	LCD HV Panel Interface Register
LCD_CPU_IF_REG	0x0060	LCD CPU Panel Interface Register
LCD_CPU_WR_REG	0x0064	LCD CPU Panel Write Data Register
LCD_CPU_RD0_REG	0x0068	LCD CPU Panel Read Data Register0
LCD_CPU_RD1_REG	0x006C	LCD CPU Panel Read Data Register1
LCD_IO_POL_REG	0x0088	LCD IO Polarity Register
LCD_IO_TRI_REG	0x008C	LCD IO Control Register
LCD_DEBUG_REG	0x00FC	LCD Debug Register
LCD_CEU_CTL_REG	0x0100	LCD CEU Control Register
LCD_CEU_COEF_MUL_REG	0x0110+N*0x04	LCD CEU Coefficient Register0(N=0~10)
LCD_CEU_COEF_ADD_REG	0x011C+N*0x10	LCD CEU Coefficient Register1(N=0,1,2)
LCD_CEU_COEF_RANG_REG	0x0140+N*0x04	LCD CEU Coefficient Register2(N=0,1,2)
LCD_CPU_TRI0_REG	0x0160	LCD CPU Panel Trigger Register0
LCD_CPU_TRI1_REG	0x0164	LCD CPU Panel Trigger Register1
LCD_CPU_TRI2_REG	0x0168	LCD CPU Panel Trigger Register2
LCD_CPU_TRI3_REG	0x016C	LCD CPU Panel Trigger Register3
LCD_CPU_TRI4_REG	0x0170	LCD CPU Panel Trigger Register4
LCD_CPU_TRI5_REG	0x0174	LCD CPU Panel Trigger Register5
LCD_CMAP_CTL_REG	0x0180	LCD Color Map Control Register
LCD_CMAP_ODD0_REG	0x0190	LCD Color Map Odd Line Register0
LCD_CMAP_ODD1_REG	0x0194	LCD Color Map Odd Line Register1
LCD_CMAP_EVEN0_REG	0x0198	LCD Color Map Even Line Register0
LCD_CMAP_EVEN1_REG	0x019C	LCD Color Map Even Line Register1
LCD_SAFE_PERIOD_REG	0x01F0	LCD Safe Period Register

LCD_FSYNC_GEN_CTRL_REG	0x023C	Module Enable and Output Value Register
LCD_FSYNC_GEN_DLY_REG	0x0240	Fsync Active Time Register
LCD_GAMMA_TABLE_REG	0x0400-0x07FF	LCD Gamma Table Register

7.1.6. Register Description

7.1.6.1. 0x0000 LCD Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: LCD_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable When it is disabled, the module will be reset to idle state.
30	R/W	0x0	LCD_GAMMA_EN 0: Disable 1: Enable Enable the Gamma correction function.
29:0	/	/	/

7.1.6.2. 0x0004 LCD Global Interrupt Register0(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LCD_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_VB_INT_EN 0: Disable 1: Enable Enable the Vb interrupt.
30	/	/	/
29	R/W	0x0	LCD_LINE_INT_EN 0: Disable 1: Enable Enable the line interrupt.
28	/	/	/
27	R/W	0x0	LCD_TRI_FINISH_INT_EN 0: Disable 1: Enable Enable the trigger finish interrupt.
26	R/W	0x0	LCD_TRI_COUNTER_INT_EN 0: Disable 1: Enable Enable the trigger counter interrupt.

25	R/W	0x0	FSYNC_INT_EN 0: Disable 1: Enable Enable the fsync interrupt.
24	R/W	0x0	DE_INT_EN 0: Disable 1: Enable Enable the data enable interrupt.
23:16	/	/	/
15	R/W0C	0x0	LCD_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	LCD_LINE_INT_FLAG Trigger when SY0 matched the current LCD scan line. Write 0 to clear it.
12	/	/	/
11	R/W0C	0x0	LCD_TRI_FINISH_INT_FLAG Trigger when cpu trigger mode finished. Write 0 to clear it.
10	R/W0C	0x0	LCD_TRI_COUNTER_INT_FLAG Trigger when tri counter reached this value. Write 0 to clear it.
9	R/W0C	0x0	LCD_TRI_UNDERFLOW_FLAG Only used in DSI video mode, tri when sync by DSI but not finish Write 0 to clear it.
8:3	/	/	/
2	R/W	0x0	FSYNC_INT_INV Enable the fsync interrupt set signal inverse polarity. When FSYNC is positive, this bit must be 1. And vice versa.
1	R/W0C	0x0	DE_INT_FLAG Asserted at the first valid line in every frame. Write 0 to clear it.
0	R/W0C	0x0	FSYNC_INT_FLAG Asserted at the fsync signal in every frame. Write 0 to clear it.

7.1.6.3. 0x0008 LCD Global Interrupt Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: LCD_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/

27:16	R/W	0x0	LCD_LINE_INT_NUM Scan line for LCD line trigger(including inactive lines) Setting it for the specified line of trigger0. **NOTE** **SY0 is writable only when LINE_TRG0 is disabled.**
15:0	/	/	/

7.1.6.4. 0x0010 LCD FRM Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: LCD_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_FRM_EN 0:Disable 1:Enable Enable the dither function.
30:7	/	/	/
6	R/W	0x0	LCD_FRM_MODE_R 0: 6-bit frm output 1: 5-bit frm output The R component output bits are in dither function.
5	R/W	0x0	LCD_FRM_MODE_G 0: 6-bit frm output 1: 5-bit frm output The G component output bits are in dither function.
4	R/W	0x0	LCD_FRM_MODE_B 0: 6-bit frm output 1: 5-bit frm output The B component output bits are in dither function.
3:2	/	/	/
1:0	R/W	0x0	LCD_FRM_TEST 00: FRM 01: half 5-/6-bit, half FRM 10: half 8-bit, half FRM 11: half 8-bit, half 5-/6-bit Set the test mode of dither function.

7.1.6.5. 0x0014+N*0x04 LCD FRM Seed Register(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04 (N=0,1,2,3,4,5)			Register Name: LCD_FRM_SEED_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B Set the seed used in dither function. **NOTE** **Avoid setting it to 0**

7.1.6.6. 0x002C+N*0x04 LCD FRM Table Register(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0,1,2,3)			Register Name: LCD_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE Set the data used in dither function. Usually set as follow: Table0 = 0x01010000 Table1 = 0x15151111 Table2 = 0x57575555 Table3 = 0x7F7F7777

7.1.6.7. 0x003C LCD 3D FIFO Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: LCD_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN 0: Disable 1: Enable Enable the 3rd fifo bist test function.
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1 Only valid when 3D_FIFO_SETTING is set as 2.
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING Set the work mode of 3D FIFO. 00: Bypass 01: Used as normal FIFO

			10: Used as 3D interlace FIFO 11: Reserved

7.1.6.8. 0x0040 LCD Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: LCD_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LCD_EN 0: Disable 1: Enable It executes at the beginning of the first blank line of LCD timing.
30:26	/	/	/
25:24	R/W	0x0	LCD_IF 00: HV(Sync+DE) 01: 8080 I/F 1x: Reserved Set the interface type of LCD controller.
23	R/W	0x0	LCD_RB_SWAP 0: Default 1: Swap RED and BLUE data at FIFO1 Enable the function to swap red data and blue data in FIFO1.
22	/	/	/
21	R/W	0x0	LCD_FIFO1_RST Writing 1 and then 0 to this bit will reset FIFO 1 **NOTE** **1 holding time must more than 1 DCLK.**
20	R/W	0x0	LCD_INTERLACE_EN 0:Disable 1:Enable This flag is valid only when LCD_EN == 1
19:9	/	/	/
8:4	R/W	0x0	LCD_START_DELAY The unit of delay is T_{line}. Valid only when LCD_EN == 1
3	/	/	/
2:0	R/W	0x0	LCD_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 110: Reserved

			111: Gridding Check

7.1.6.9. 0x0044 LCD Data Clock Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: LCD_DCLK REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LCD_DCLK_EN LCD clock enable 0000: dclk_en = 0; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0001: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 0010: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 0011: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 0101: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 1111: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1; Others:Reserved
27:7	/	/	/
6:0	R/W	0x0	LCD_DCLK_DIV Tdclk = Tsclk / DCLKDIV **NOTE** **If dclk1&dclk2 used, DCLKDIV >=6. If dclk only, DCLKDIV >=1**

7.1.6.10. 0x0048 LCD Basic Timing Register0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: LCD_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	Y Panel height is Y+1

7.1.6.11. 0x004C LCD Basic Timing Register1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: LCD_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation:

			1) parallel: HT = X + BLANK Limitation: 1) parallel: HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

7.1.6.12. 0x0050 LCD Basic Timing Register2(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: LCD_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

7.1.6.13. 0x0054 LCD Basic Timing Register3(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: LCD_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

7.1.6.14. 0x0058 LCD HV Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: LCD_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE 0000: 24-bit/1cycle parallel mode

			1000: 8-bit/3 cycle RGB serial mode(RGB888) 1010: 8-bit/4 cycle Dummy RGB(DRGB) 1011: 8-bit/4 cycle RGB Dummy(RGBD) 1100: 8-bit/2 cycle YUV serial mode(CCIR656) Set the HV mode of LCD controller.
27:26	R/W	0x0	RGB888_ODD_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at odd lines of the panel (line 1, 3, 5, 7…)
25:24	R/W	0x0	RGB888_EVEN_ORDER 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B Serial RGB888 mode output sequence at even lines of the panel (line 2, 4, 6, 8…)
23:22	R/W	0x0	YUV_SM 00: YUYV 01: YVYU 10: UYVY 11: VYUY Serial YUV mode output sequence 2-pixel-pair of every scan line
21:20	R/W	0x0	YUV EAV/SAV F LINE DELAY 00:F toggle right after active video line 01: delay 2 line(CCIR PAL) 10: delay 3 line(CCIR NTSC) 11: reserved Set the delay line mode.
19	R/W	0x0	CCIR_CSC_DIS 0: Enable 1: Disable Only valid when HV mode is “1100”. Select ‘0’ LCD convert source from RGB to YUV
18:2	/	/	/
1	R/W	0x0	BT656 F_MASK_VALUE 0: BT656 F signal force to 0 1: BT656 F signal force to 1
0	R/W	0x0	BT656 F_MASK 0: Disable 1: Enable

7.1.6.15. 0x0060 LCD CPU Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: LCD_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE 0000: 18-bit/256K mode 0010: 16-bit mode0 0100: 16-bit mode1 0110: 16-bit mode2 1000: 16-bit mode3 1010: 9-bit mode 1100: 8-bit 256K mode 1110: 8-bit 65K mode xxx1: 24-bit for DSI Set the i8080 interface work mode.
27	/	/	/
26	R/W	0x0	DA Pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA Pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG Status of Write Operation 0: Write operation is finishing 1: Write operation is pending
22	R	0x0	RD_FLAG Status of Read Operation 0: Read operation is finishing 1: Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO Auto Transfer Mode If it is 1, all the valid data during this frame are written to panel. This bit is sampled by Vsync.
16	R/W	0x0	FLUSH Direct Transfer Mode If it is enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate is controlled by DCLK.
15:4	/	/	/
3	R/W	0x0	TRIGGER_FIFO_BIST_EN 0: Disable 1: Enable Entry addr is 0xFF8
2	R/W	0x0	TRIGGER_FIFO_EN

			0:Disable 1:Enable Enable the trigger FIFO.
1	R/W1S	0x0	TRIGGER_START Write '1' to start a frame flush, writing '0' has no effect. This flag indicated frame flush is running. Software must write '1' only when this flag is '0'.
0	R/W	0x0	TRIGGER_EN 0: Trigger mode disable 1: Trigger mode enable Enable trigger mode.

7.1.6.16. 0x0064 LCD CPU Panel Write Data Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: LCD_CPU_WR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	W	0x0	DATA_WR Data write on 8080 bus, launch a write operation on 8080 bus

7.1.6.17. 0x0068 LCD CPU Panel Read Data Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: LCD_CPU_RD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD0 Data read on 8080 bus, launch a new read operation on 8080 bus

7.1.6.18. 0x006C LCD CPU Panel Read Data Register1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: LCD_CPU_RD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_RD1 Data read on 8080 bus, without a new read operation on 8080 bus

7.1.6.19. 0x0088 LCD IO Polarity Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: LCD_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	IO_OUTPUT_SEL 0: Normal output 1: Register output When it is set as '1', d[23:0], io0, io1,io3 sync to dclk.
30:28	R/W	0x0	DCLK_SEL 000: Used DCLK0(normal phase offset) 001: Used DCLK1(1/3 phase offset) 010: Used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 Others: Reserved Set the phase offset of clock and data in hv mode.
27	R/W	0x0	IO3_INV 0: Not invert 1: Invert Enable invert function of IO3.
26	R/W	0x0	IO2_ INV 0: Not invert 1: Invert Enable invert function of IO2.
25	R/W	0x0	IO1_INV 0: Not invert 1: Invert Enable invert function of IO1.
24	R/W	0x0	IO0_INV 0: Not invert 1: Invert Enable invert function of IO0.
23:0	R/W	0x0	Data_INV 0: Normal polarity 1: Invert the specify output LCD output port D[23:0] polarity control, with independent bit control.

7.1.6.20. 0x008C LCD IO Control Register(Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: LCD_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN 0: Normal 1: Bits_invert Set the endian of data bits.
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable

			0: Enable Enable the output of IO3.
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO2.
25	R/W	0x1	IO1_OUTPUR_TRI_EN 1: Disable 0: Enable Enable the output of IO1.
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable Enable the output of IO0.
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN 1: Disable 0: Enable LCD output port D[23:0] output enable, with independent bit control.

7.1.6.21. 0x00FC LCD Debug Register(Default Value: 0x2000_0000)

Offset: 0x00FC			Register Name: LCD_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	LCD_FIFO_UNDERFLOW 0: Not underflow 1: Underflow The flag shows whether the fifo is in underflow status.
30	/	/	/
29	R	0x1	LCD_FIELD_POL 0: Second field 1: First field The flag indicates the current field polarity.
28	/	/	/
27:16	R	0x0	LCD_CURRENT_LINE The current scan line.
15:0	/	/	/

7.1.6.22. 0x0100 LCD CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: LCD_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN

			0: Bypass 1: Enable Enable CEU function.
30:0	/	/	/

7.1.6.23. 0x0110+N*0x04 LCD CEU Coefficient Register0(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04(N=0~10)			Register Name: LCD_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb Signed 13bit value, range of (-16,16)

7.1.6.24. 0x011C+N*0x10 LCD CEU Coefficient Add Register(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: LCD_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0: Rc N=1: Gc N=2: Bc Signed 19bit value, range of (-16384, 16384)

7.1.6.25. 0x0140+N*0x04 LCD CEU Coefficient Range Register(Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0,1,2)			Register Name: LCD_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8-bit value, range of [0,255]
15:8	/	/	/

7:0	R/W	0x0	CEU_COEF_RANGE_MAX Unsigned 8-bit value, range of [0,255]

7.1.6.26. 0x0160 LCD CPU Panel Trigger Register0(Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: LCD_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE The spaces between data blocks. It should be set to 20*pixel above.
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE The size of data block. It is usually set as X.

7.1.6.27. 0x0164 LCD CPU Panel Trigger Register1(Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: LCD_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM Shows the current data block transmitting to panel.
15:0	R/W	0x0	BLOCK_NUM The number of data blocks. It is usually set as Y.

7.1.6.28. 0x0168 LCD CPU Panel Trigger Register2(Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: LCD_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DELAY Tdly = (Start_Delay +1) * de_clk*8
15	R/W	0x0	TRANS_START_MODE 0: ecc_fifo+tri_fifo 1: tri_fifo Select the FIFOs used in CPU mode.
14:13	R/W	0x0	SYNC_MODE 0x: auto 10: 0 11: 1 Set the sync mode in CPU interface.
12:0	R/W	0x0	TRANS_START_SET Usually set as the length of a line.

7.1.6.29. 0x016C LCD CPU Panel Trigger Register3(Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: LCD_CPU_TRI3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE 00: Disable 01: Counter mode 10: Te rising mode 11: Te falling mode When it is set as 2b'01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. When it is set as 2b'10 or 2b'11, io0 is map as TE input.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N The value of counter factor.
7:0	R/W	0x0	COUNTER_M The value of counter factor.

7.1.6.30. 0x0170 LCD CPU Panel Trigger Register4(Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: LCD_CPU_TRI4_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN 0: Disable 1: Enable Enable the plug mode used in DSI command mode.
27:25	/	/	/
24	R/W	0x0	A1 Valid in first Block.
23:0	R/W	0x0	D23-D0 Valid in first Block.

7.1.6.31. 0x0174 LCD CPU Panel Trigger Register5(Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: LCD_CPU_TRI5_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	A1

			Valid in Block except first
23:0	R/W	0x0	D23-D0 Valid in Block except first

7.1.6.32. 0x0180 LCD Color Map Control Register(Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: LCD_CMAP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN 0: Bypass 1: Enable Enable the color map function. This module only work when X is divided by 4.
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1 Set the pixel output format in color map function.

7.1.6.33. 0x0190 LCD Color Map Odd Line Register0(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: LCD_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3

			1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.34. 0x0194 LCD Color Map Odd Line Register1(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: LCD_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2

			1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_ODD2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.35. 0x0198 LCD Color Map Even Line Register0(Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: LCD_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1

			0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.36. 0x019C LCD Color Map Even Line Register1(Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: LCD_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0]

			0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.
15:0	R/W	0x0	OUT_EVEN2 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0000: in_b0 0001: in_g0 0010: in_r0 0011: Reserved 0100: in_b1 0101: in_g1 0110: in_r1 0111:Reserved 1000: in_b2 1001: in_g2 1010: in_r2 1011: Reserved 1100: in_b3 1101: in_g3 1110: in_r3 1111: Reserved Indicates the output order of components.

7.1.6.37. 0x01F0 LCD Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: LCD_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM When the data length in line buffer is more than SAFE_PERIOD_FIFO_NUM, LCD controller will allow dram controller to stop working to change frequency.
15:4	R/W	0x0	SAFE_PERIOD_LINE Set a fixed line and during the line time, LCD controller allow dram controller to change frequency.The fixed line should be set in the blanking area.
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at FIFO_CURR_NUM > SAFE_PERIOD_FIFO_NUM 011: safe at 2 and safe at sync active 100: safe at line Select the safe mode.

7.1.6.38. 0x023C Module Enable and Output Value Register(Default Value: 0x0000_0000)

Offset: 0x023C			Register Name: FSYNC_GEN_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:8	R/W	0x0	SENSOR_DIS_TIME Delay 0~2047 Hsync Period
7	/	/	/
6	R/W	0x0	SENSOR_ACT1_VALUE 0: Fsync active_1 period output 0 1: Fsync active_1 period output 1
5	R/W	0x0	SENSOR_ACT0_VALUE 0: Fsync active_0 period output 0 1: Fsync active_0 period output 1
4	R/W	0x0	SENSOR_DIS_VALUE 0: Fsync disable period output 0 1: Fsync disable period output 1
3	/	/	/
2	R/W	0x0	HSYNC_POL_SEL 0: normal 1: opposite hsync to hysnc counter
1	R/W	0x0	SEL_VSYNC_EN 0: select vsync falling edge to start state machine 1: select vsync rising edge to start state machine
0	R/W	0x0	FSYNC_GEN_EN 0: disable

			1: enable

7.1.6.39. 0x0240 Fsync Active Time Register(Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: FSYNC_GEN_DLY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	sensor_act0_time Delay 0~4095 Pixel clk Period
15:12	/	/	/
11:0	R/W	0x0	sensor_act1_time Delay 0~4095 Pixel clk Period

7.1.6.40. 0x0400~0x07FF LCD Gamma Table Register(Default Value: 0x0000_0000)

Offset: 0x0400~0x07FF			Register Name: LCD_GAMMA_TABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x00	Red Component
15:8	R/W	0x00	Green Component
7:0	R/W	0x00	Blue Component

7.2. MIPI DSI

7.2.1. Overview

The MIPI Display Serial Interface(DSI) is a high-speed interface between a host processor and peripheral devices that adhere to MIPI Alliance specifications for mobile device interfaces. This DSI module is composed of a DSI controller which is compliance with MIPI DSI specification V1.01 and a D-PHY module which is compliance with MIPI DPHY specification V1.00. By standardizing this interface, components may be developed to provide higher performance, lower power, less EMI and fewer pins than current devices, while maintain compatibility across products from multiple vendors.

The MIPI DSI includes the following features:

- Compliance with MIPI DSI v1.01, MIPI D-PHY v1.00 and MIPI DCS v1.02
- 1/2/3/4 data lanes configuration and up to 1Gbit/s per lane
- Supports ECC, CRC generation and EOT package
- Supports up to 1920x1080@60fps with 4 data lanes
- Supports video mode
  - Non-burst mode with sync pulses
  - Non-burst mode with sync event
  - Burst mode
- Supports pixel formats: RGB888, RGB666, RGB666 packed, RGB565

NOTE

V831 does not support MIPI DSI.

7.2.2. Operations and Functional Descriptions

7.2.2.1. External Signals

The following table describes the external signals of MIPI DSI.

Table 7- 8. MIPI DSI External Signals

Signal	Description	Type
DSI_CKN	MIPI DSI Differential Clock Negative	AO
DSI_CKP	MIPI DSI Differential Clock Positive	AO
DSI_D0N	MIPI DSI Differential Data0 Negative	A I/O
DSI_D0P	MIPI DSI Differential Data0 Positive	A I/O
DSI_D1N	MIPI DSI Differential Data1 Negative	AO
DSI_D1P	MIPI DSI Differential Data1 Positive	AO
DSI_D2N	MIPI DSI Differential Data2 Negative	AO

DSI_D2P	MIPI DSI Differential Data2 Positive	AO
DSI_D3N	MIPI DSI Differential Data3 Negative	AO
DSI_D3P	MIPI DSI Differential Data3 Positive	AO

7.2.3. Register List

Module Name	Base Address
MIPI DSI	0x06504000+N*0x2000(N=0~3)

Register Name	Offset	Description
PHY_RSTZ	0x0004	D-PHY Reset Control Register
CLKMGR_CFG	0x0008	Clock Configure Register
VID_MODE_CFG	0x0010	Video Mode Configuration Register
VID_PKT_CFG	0x001C	Video Packet Configuration Register
VTIMING_CFG1	0x0020	Vertical Timing Configuration Register1
VTIMING_CFG2	0x0024	Vertical Timing Configuration Register2
TMR_LINE_CFG1	0x0028	Line Timer Configuration Register1
TMR_LINE_CFG2	0x002C	Line Timer Configuration Register2
DPI_CFG1	0x0030	DPI Interface Configuration Register1
DPI_CFG2	0x003C	DPI Interface Configuration Register2
GEN_HDR	0x0040	Generic Packet Header Configuration Register
GEN_PLD_DATA	0x0044	Generic Payload Data In/Out Register
GEN_PKT_STATUS	0x0048	Generic Packet Status Register
PCKHDL_CFG	0x0050	Packet Handler Configuration Register
CMD_MODE_CFG	0x0054	Command Mode Configuration Register
DBI_CFG	0x0080	DBI Interface Configuration Register
DBI_CMDSIZE	0x0084	DBI command Size Configuration Register
CMD_PKT_STATUS	0x0088	Command Packet Status Register
TO_CNT_CFG1	0x00A0	Timeout Timer Configuration Register1
TO_CNT_CFG2	0x00A4	Timeout Timer Configuration Register2
LP_CMD_TIM	0x00A8	Low-Power Command Timing Configuration Register
PHY_TMR_CFG	0x00B0	D-PHY Timing Configuration Register
PHY_IF_CFG	0x00B4	D-PHY Interface Configuration Register
PHY_IF_CTRL	0x00C0	D-PHY PPI Interface Control Register
PHY_STATUS	0x00C4	D-PHY PPI Status Interface Register
PHY_TST_CTRL	0x00F0	D-PHY Test Interface Control Register
ERROR_MSK0	0x01E0	Error Interrupt Mask Register 0
ERROR_MSK1	0x01E4	Error Interrupt Mask Register 1
ERROR_ST0	0x01F0	Interrupt Status Register 0
ERROR_ST1	0x01F4	Interrupt Status Register 1
DSI_CFG0	0x0400	DSI Configure Register0
DSI_CFG1	0x0404	DSI Configure Register1

DSI_CFG2	0x0408	DSI Configure Register2
DSI_CFG3	0x040C	DSI Configure Register3
DSI_STS0	0x0410	DSI Status Register0
DSI_BIST_ENTRY	0x0FFC	DSI BIST Entry

7.2.4. Registers Description

7.2.4.1. 0x0004 D-PHY Reset Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PHY_RSTZ
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	RW	0x0	phy_tx_request_clk_hs This bit controls the D-PHY PPI tx request clk hs signal.
8	RW	0x0	phy_enable_clk When set to 1, this bit enables the D-PHY Clock Lane Module.
7:6	/	/	/
5:4	RW	0x0	LANE_NUM 00: 1 lane 01: 2 lanes 10: 3 lanes 11: 4 lanes
3:2	/	/	/
1	RW	0x0	PHY_RST 0: reset 1: reset disable
0	RW	0x0	PHY_EN 0: disable 1: enable

7.2.4.2. 0x0008 Clock Configure Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CLKMGR_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	RW	0x0	TX_ESC_CLK_DIVISION This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation

7.2.4.3. 0x0010 Video Mode Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: VID_MODE_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	RW	0x0	en_lp_hfp When set to 1, this bit enables the return to low-power inside the HFP period when timing allows.
12	RW	0x0	en_lp_hbp When set to 1, this bit enables the return to low-power inside the HBP period when timing allows.
11	RW	0x0	en_lp_vfp When set to 1, this bit enables the return to low-power inside the VFP period when timing allows.
10	RW	0x0	en_lp_vact When set to 1, this bit enables the return to low-power inside the VACT period when timing allows.
9	RW	0x0	en_lp_vbp When set to 1, this bit enables the return to low-power inside the VBP period when timing allows.
8	RW	0x0	en_lp_vsa When set to 1, this bit enables the return to low-power inside the VSA period when timing allows.
7:6	/	/	/
5:4	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 00: Non-burst with sync pulses 01: Non-burst with sync events 10 and 11: Burst with sync pulses
3:1	/	/	/
0	RW	0x0	en_video_mode When set to 1, this bit enables the DPI Video mode transmission.

7.2.4.4. 0x001C Video Packet Configuration Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: VID_PKT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:20	RW	0x0	null_pkt_size This field configures the number of bytes in a null packet.
19:18	/	/	/
17:8	RW	0x0	num_chunks This field configures the number of chunks to be transmitted during a

			line period (a chunk is a video packet or a null packet).
7:6	/	/	/
5	RW	0x0	en_null_pkt When set to 1, this bit enables the transmission of null packets in the HACT period.
4	RW	0x0	en_multi_pkt When set to 1, this bit enables the transmission of multi video packets in the HACT period.
3:2	/	/	/
1	RW	0x0	lpcmden When set to 1, this bit enables the command transmission only in low-power mode.
0	RW	0x0	frame_BTA_ack When set to 1, this bit enables the request for an acknowledge response at the end of a frame.

7.2.4.5. 0x0020 Vertical Timing Configuration Register1 (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: VTIMING_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	RW	0x0	VBP This field configures the Vertical Back Porch period measured in horizontal lines.
15:4	R	0x0	Reserved.
3:0	RW	0x0	VSA

7.2.4.6. 0x0024 Vertical Timing Configuration Register2(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: VTIMING_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	RW	0x0	VFP
15:11	/	/	/
10:0	RW	0x0	VACT

7.2.4.7. 0x0028 Line Timer Configuration Register1(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: TMR_LINE_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

29:16	RW	0x0	HT This field configures the size of the total lines counted in lane byte cycles.
15:11	/	/	/
10:0	RW	0x0	vid_pkt_size This field configures the number of pixels on a single video packet. If you use the 18-bit mode and do not enable loosely packed stream, this value must be a multiple of 4.

7.2.4.8. 0x002C Line Timer Configuration Register2(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: TMR_LINE_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	RW	0x0	HBP This field configures the Horizontal Back Porch period in lane byte clock cycles.
15:9	/	/	/
8:0	RW	0x0	HSA This field configures the Horizontal Synchronism Active period in lane byte clock cycles.

7.2.4.9. 0x0030 DPI Interface Configuration Register1(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: DPI_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	RW	0x0	dpi_vid This field configures the DPI virtual channel id that is indexed to the Video mode packets.
27:13	/	/	/
12	RW	0x0	en18_loosely When set to 1, this bit enables 18 loosely packed pixel stream.
11	/	/	/
10:8	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 000: 16-bit configuration 1 001: 16-bit configuration 2 010: 16-bit configuration 3 011: 18-bit configuration 1 100: 18-bit configuration 2 101, 110, and 111: 24 bits

7:0	/	/	/

7.2.4.10. 0x003C DPI Interface Configuration Register2(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: DPI_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	RW	0x0	colorm_active_low When set to 1, this bit configures the color mode pin (dpicolorm) as active low.
4	RW	0x0	shutd_active_low When set to 1, this bit configures the shut down pin (dpishutdn) as active low.
3	RW	0x0	dataen_active_low When set to 1, this bit configures the data enable pin (dpidataen) as active low.
2	/	/	/
1	RW	0x0	hsync_active_low When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low.
0	RW	0x0	vsync_active_low When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low.

7.2.4.11. 0x0040 Generic Packet Header Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: GEN_HDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:8	RW	0x0	gen_WC This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets.
7:6	RW	0x0	gen_VC This field configures the virtual channel id of the header packet.
5:0	RW	0x0	gen_DT This field configures the packet data type of the header packet.

7.2.4.12. 0x0044 Generic Payload Data In/Out Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: GEN_PLD_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**

31:24	RW	0x0	gen_pld_b4 This field indicates byte 4 of the packet payload.
23:16	RW	0x0	gen_pld_b3 This field indicates byte 3 of the packet payload.
15:8	RW	0x0	gen_pld_b2 This field indicates byte 2 of the packet payload.
7:0	RW	0x0	gen_pld_b1 This field indicates byte 1 of the packet payload.

7.2.4.13. 0x0048 Generic Packet Status Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: GEN_PKT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO.
7	/	/	/
6	R	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO.
5	R	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO.
4	R	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO.
3	/	/	/
2	R	0x1	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO.
1	R	0x1	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO.
0	R	0x1	gen_cmd_empty This bit indicates the empty status of the generic command FIFO.

7.2.4.14. 0x0050 Packet Handler Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: PCKHDL_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	RW	0x0	gen_vid_rx This field indicates the Generic interface read-back virtual channel identification.
27:11	R	0x0	Reserved.
10	RW	0x0	en_CRC_rx

			When set to 1, this bit enables the CRC reception and error reporting.
9	RW	0x0	en_ECC_rx When set to 1, this bit enables the ECC reception, error correction, and reporting.
8	RW	0x0	en_EOTp_rx When set to 1, this bit enables the EOTp reception.
7:5	/	/	/
4	RW	0x0	en_EOTp_tx When set to 1, this bit enables the EOTp transmission.
3:1	/	/	/
0	RW	0x0	en_BTA When set to 1, this bit enables the Bus Turn-Around (BTA) request.

7.2.4.15. 0x0054 Command Mode Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CMD_MODE_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	RW	0x0	en_tear_fx When set to 1, this bit enables the tearing effect acknowledge request.
27:25	/	/	/
24	RW	0x0	en_ack_rqst When set to 1, this bit enables the acknowledge request after each packet transmission.
23:21	/	/	/
20	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 0: High-speed 1: Low-power
19:17	/	/	/
16	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 0: High-speed 1: Low-power
15	/	/	/
14	RW	0x0	dcs_lw_tx This bit configures the DCS long write packet command transmission type: 0: High-speed 1: Low-power
13	RW	0x0	dcs_sw_1p_tx

			This bit configures the DCS short write packet with one parameter command transmission type: 0: High-speed 1: Low-power
12	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 0: High-speed 1: Low-power
11	/	/	/
10	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: 0: High-speed 1: Low-power
9	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 0: High-speed 1: Low-power
8	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 0: High-speed 1: Low-power
7	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 0: High-speed 1: Low-power
6	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: 0: High-speed 1: Low-power
5	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 0: High-speed 1: Low-power
4	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 0: High-speed 1: Low-power

3:1	/	/	/
0	RW	0x0	en_cmd_mode When set to 1, this bit enables the Command mode protocol for transmissions.

7.2.4.16. 0x0080 DBI Interface Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: DBI_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:28	RW	0x0	dbi_vid This field configures the DBI virtual channel id that is indexed to the DCS packets.
27:17	/	/	/
16	RW	0x0	partitioning_en When set to 1, this bit enables the use of write_memory_continue input commands (system needs to ensure correct partitioning of Long Write commands). When not set, partitioning is automatically performed in the MIPI DSI Host Controller.
15:14	/	/	/
13:12	RW	0x0	lut_size_conf This field configures the size used to transport the Write Lut commands as follows: 00: 16-bit color display 01: 18-bit color display 10: 24-bit color display 11: 16-bit color display
11:8	RW	0x0	out_dbi_conf This field configures the DBI output pixel data as follows: 0000: 8-bit 8 bpp 0001: 8-bit 12 bpp 0010: 8-bit 16 bpp 0011: 8-bit 18 bpp 0100: 8-bit 24 bpp 0101: 9-bit 18 bpp 0110: 16-bit 8 bpp 0111: 16-bit 12 bpp 1000: 16-bit 16 bpp 1001: 16-bit 18 bpp, option 1 1010: 16-bit 18 bpp, option 2 1011: 16-bit 24 bpp, option 1 1100: 16-bit 24 bpp, option 2
7:4	RW	0x0	in_dbi_conf This field configures the DBI input pixel data as follows:

			0000: 8-bit 8 bpp 0001: 8-bit 12 bpp 0010: 8-bit 16 bpp 0011: 8-bit 18 bpp 0100: 8-bit 24 bpp 0101: 9-bit 18 bpp 0110: 16-bit 8 bpp 0111: 16-bit 12 bpp 1000: 16-bit 16 bpp 1001: 16-bit 18 bpp, option 1 1010: 16-bit 18 bpp, option 2 1011: 16-bit 24 bpp, option 1 1100: 16-bit 24 bpp, option 2
3:0	/	/	/

7.2.4.17. 0x0084 DBI Command Size Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: DBI_CMDSIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RW	0x0	allowed_cmd_size This field configures the maximum allowed size of a DCS write memory command. This field is used to partition a write memory command into several write memory continue commands. It is only used if the partitioning_en bit of the DBI_CFG register is disabled. The size of the DSI packet payload is the actual payload size minus 1, because the DCS command is in the DSI packet payload.
15:0	RW	0x0	wr_cmd_size This field configures the size of the DCS write memory commands. The size of DSI packet payload is the actual payload size minus 1, because the DCS command is in the DSI packet payload.

7.2.4.18. 0x0088 Command Packet Status Register(Default Value: 0x0000_0007)

Offset: 0x0088			Register Name: CMD_PKT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R	0x0	dbi_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO.
7	/	/	/
6	R	0x0	dbi_pld_r_full This bit indicates the full status of the DBI read payload FIFO.

5	R	0x0	dbi_pld_w_full This bit indicates the full status of the DBI write payload FIFO.
4	R	0x0	dbi_cmd_full This bit indicates the full status of the DBI command FIFO.
3	/	/	/
2	R	0x1	dbi_pld_r_empty This bit indicates the empty status of the DBI read payload FIFO.
1	R	0x1	dbi_pld_w_empty This bit indicates the empty status of the DBI write payload FIFO.
0	R	0x1	dbi_cmd_empty This bit indicates the empty status of the DBI command FIFO.

7.2.4.19. 0x00A0 Timeout Timer Configuration Register1(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TO_CNT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	RW	0x0	TO_CLK_DIVISION This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.

7.2.4.20. 0x00A4 Timeout Timer Configuration Register2(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TO_CNT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RW	0x0	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in CLKMGR_CFG.TO_CLK_DIVISION cycles).
15:0	RW	0x0	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in CLKMGR_CFG.TO_CLK_DIVISION cycles).

7.2.4.21. 0x00A8 Low-Power Command Timing Configuration Register(Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: LP_CMD_TIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	RW	0x0	outvact_lpcmd_time Outside VACT region command time. This field configures the time

			available to transmit a command in low-power mode. The time value is expressed in a number of bytes format. The number of bytes represents the maximum size of a packet that can fit in a line during the VSA, VBP, and VFP regions. This field must be configured with a value greater than or equal to four bytes to allow the transmission of the DCTRL commands such as shutdown and colorm in low-power mode.
15:8	/	/	/
7:0	RW	0x0	invact_lpcmd_time Inside VACT region command time. This field configures the time available to transmit a command in low-power mode. The time value is expressed in a number of bytes format. The number of bytes represents the maximum size of the packet that can fit a line during the VACT region.

7.2.4.22. 0x00B0 D-PHY Timing Configuration Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PHY_TMR_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	RW	0x0	phy_hs2lp_time This field configures the maximum time that the PHY takes to go from highspeed to low-power transmission measured in lane byte clock cycles.
15:8	/	/	/
7:0	RW	0x0	phy_lp2hs_time This field configures the maximum time that the PHY takes to go from lowpower to high-speed transmission measured in lane byte clock cycles.

7.2.4.23. 0x00B4 D-PHY Interface Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: PHY_IF_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	RW	0x0	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when read commands are not in progress.
15:8	/	/	/
7:0	RW	0x0	phy_stop_wait_time This field configures the minimum wait period to request a high-speed

			transmission after the Stop state is accounted in clock lane cycles.

7.2.4.24. 0x00C0 D-PHY PPI Interface Control Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: PHY_IF_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	RW	0x0	phy_tx_triggers This field controls the trigger transmissions.
15:10	/	/	/
9	RW	0x0	phy_tx exit ulps lan ULPS mode Exit on all active data lanes.
8	RW	0x0	phy_tx req ulps lan ULPS mode Request on all active data lanes.
7:6	/	/	/
5	RW	0x0	phy_tx exit ulps clk ULPS mode Exit on clock lane.
4	RW	0x0	phy_tx req ulps clk ULPS mode Request on clock lane.
3:0	/	/	/

7.2.4.25. 0x00C4 D-PHY PPI Status Interface Register(Default Value: 0x001F_0000)

Offset: 0x00C4			Register Name: PHY_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal.
23:21	/	/	/
20	R	0x1	Phyulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal.
19	R	0x1	ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal.
18	R	0x1	ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal.
17	R	0x1	ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal.
16	R	0x1	ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal.
15:13	/	/	/
12	R	0x0	phystopstateclklane This bit indicates the status of phystopstateclklane D-PHY signal.

11	R	0x0	phystopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal.
10	R	0x0	phystopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal.
9	R	0x0	phystopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal.
8	R	0x0	phystopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal.
7:5	/	/	/
4	R	0x0	Phydirection This bit indicates the status of phydirection D-PHY signal.
3:1	/	/	/
0	R	0x0	Phylock This bit indicates the status of phylock D-PHY signal.

7.2.4.26. 0x00F0 D-PHY Test Interface control Register(Default Value: 0x0000_0001)

Offset: 0x00F0			Register Name: PHY_TST_CTRL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	phy_testdout PHY output 8-bit data bus for read-back and internal probing functionalities.
23:16	RW	0x0	phy_testdin PHY test interface input 8-bit data bus for internal register programming and test functionalities access.
15:5	/	/	/
4	RW	0x0	phy_testen PHY test interface operation selector: When set to 1, this bit configures the address write operation on the falling edge of the testclk signal. When set to 0, this bit configures the data write operation on the rising edge of the testclk signal.
3:2	/	/	/
1	RW	0x0	phy_testclk PHY test interface strobe signal. This bit is used to clock the TESTDIN bus into the D-PHY. In conjunction with testen signal, it controls the operation selection.
0	RW	0x1	phy_testclr PHY test interface clear. When active, this bit performs vendor-specific interface initialization (active high).

7.2.4.27. 0x01E0 Error Interrupt Mask Register 0(Default Value: 0x0000_0000)

This register masks the interrupt generation triggered by the ERROR_ST0 register.

Offset: 0x01E0			Register Name: ERROR_MSK0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.
18	RW	0x0	dphy_errors_2 This bit indicates the control error ErrControl from Lane 0.
17	RW	0x0	dphy_errors_1 This bit indicates the low-power data transmission synchronization error ErrSyncEsc from Lane 0.
16	RW	0x0	dphy_errors_0 This bit indicates the ErrEsc, escape entry error from Lane 0.
15	RW	0x0	ack_with_err_15 This bit masks the DSI protocol violation from the Display Acknowledge error report.
14	RW	0x0	ack_with_err_14 This bit masks the Reserved (specific to device) from the Display Acknowledge error report.
13	RW	0x0	ack_with_err_13 This bit masks the invalid transmission length from the Display Acknowledge error report.
12	RW	0x0	ack_with_err_12 This bit masks the DSI VC ID Invalid from the Display Acknowledge Error Report.
11	RW	0x0	ack_with_err_11 This bit masks the DSI Data Type Not Recognized from the Display Acknowledge error report.
10	RW	0x0	ack_with_err_10 This bit masks the checksum error (long packet only) from the Display Acknowledge error report.
9	RW	0x0	ack_with_err_9 This bit masks the ECC error, multi-bit (detected, not corrected) from the Display Acknowledge error report.
8	RW	0x0	ack_with_err_8 This bit masks the ECC error, single-bit (detected and corrected) from the Display Acknowledge error report.
7	RW	0x0	ack_with_err_7

			This bit masks the Reserved (specific to device) from the Display Acknowledge error report.
6	RW	0x0	ack_with_err_6 This bit masks the False Control error from the Display Acknowledge error report.
5	RW	0x0	ack_with_err_5 This bit masks the HS Receive Timeout error from the Display Acknowledge error report.
4	RW	0x0	ack_with_err_4 This bit masks the LP Transmit Sync error from the Display Acknowledge error report.
3	RW	0x0	ack_with_err_3 This bit masks the Escape Mode Entry Command error from the Display Acknowledge error report.
2	RW	0x0	ack_with_err_2 This bit masks the EoT Sync error from the Display Acknowledge error report.
1	RW	0x0	ack_with_err_1 This bit masks the SoT Sync error from the Display Acknowledge error report.
0	RW	0x0	ack_with_err_0 This bit masks the SoT error from the Display Acknowledge error report.

7.2.4.28. 0x01E4 Error Interrupt Mask Register 1(Default Value: 0x0000_0000)

This register masks the interrupt generation triggered by the ERROR_ST1 register.

Offset: 0x01E4			**Register Name: ERROR_MSK1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	RW	0x0	to_lp_rx This bit masks the low-power reception timeout counter error.
28	RW	0x0	to_hs_tx This bit masks the high-speed transmission timeout counter error.
27:25	/	/	/
24	RW	0x0	dbi_illegal_comm_err This bit masks the error due to an attempt to write an illegal command on DPI.
23	RW	0x0	dbi_pld_recv_err This bit masks the DBI read back packet payload FIFO full error.
22	RW	0x0	dbi_pld_rd_err This bit masks the payload DBI FIFO empty error.
21	RW	0x0	dbi_pld_wr_err

			This bit masks the write payload data DBI FIFO full error.
20	RW	0x0	dbi_cmd_wr_err This bit masks the DBI command FIFO full error.
19:17	/	/	/
16	RW	0x0	gen_pld_recv_err This bit masks the Generic interface packet read back FIFO full error.
15	RW	0x0	gen_pld_rd_err This bit masks the DCS read data payload FIFO empty error.
14	RW	0x0	gen_pld_send_err This bit masks the Generic interface packet build FIFO empty error.
13	RW	0x0	gen_pld_wr_err This bit masks the payload data FIFO of Generic interface full error.
12	RW	0x0	gen_cmd_wr_err This bit masks the command FIFO of Generic interface full error.
11:9	/	/	/
8	RW	0x0	dpi_pld_wr_err This bit masks the DPI pixel line payload FIFO full error.
7:5	R	0x0	Reserved.
4	RW	0x0	pkt_size_err This bit masks the packet size error.
3	RW	0x0	eopt_err This bit masks the EOTp packet not received error.
2	RW	0x0	crc_err This bit masks the CRC error.
1	RW	0x0	ecc_multi_err This bit masks the ECC multiple error.
0	RW	0x0	ecc_single_err This bit masks the ECC single error.

7.2.4.29. 0x01F0 Interrupt Status Register 0(Default Value: 0x0000_0000)

Offset: 0x01F0			**Register Name: ERROR_ST0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20	R	0x0	dphy_errors_4 This bit indicates LP1 contention ErrContentionLP1 from Lane 0.
19	R	0x0	dphy_errors_3 This bit indicates LP0 contention ErrContentionLP0 from Lane 0.
18	R	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0.
17	R	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.

16	R	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	R	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Display Acknowledge error report.
14	R	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Display Acknowledge error report.
13	R	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Display Acknowledge error report.
12	R	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report.
11	R	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Display Acknowledge error report.
10	R	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Display Acknowledge error report.
9	R	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Display Acknowledge error report.
8	R	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Display Acknowledge error report.
7	R	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Display Acknowledge error report.
6	R	0x0	ack_with_err_6 This bit retrieves the False Control error from the Display Acknowledge error report.
5	R	0x0	ack_with_err_5 This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report.
4	R	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Display Acknowledge error report.
3	R	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Display Acknowledge error report.
2	R	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Display Acknowledge error report.

1	R	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Display Acknowledge error report.
0	R	0x0	ack_with_err_0 This bit retrieves the SoT error from the Display Acknowledge error report.

7.2.4.30. 0x01F4 Interrupt Status Register 1(Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: ERROR_ST1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected.
28	R	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected.
27:25	/	/	/
24	R	0x0	dbi_illegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission.
23	R	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted.
22	R	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted.
21	R	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written.
20	R	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written.
19:17	/	/	/
16	R	0x0	gen_pld_recv_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
15	R	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.

14	R	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
13	R	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.
12	R	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
11:9	/	/	/
8	R	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
7:5	/	/	/
4	R	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
3	R	0x0	eopt_err This bit indicates that the EOTp packet is not received at the end of the incoming peripheral transmission.
2	R	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload.
1	R	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet.
0	R	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.

7.2.4.31. 0x0400 DSI Configure Register0(Default Value: 0x0000_0000)

Offset: 0x0400			**Register Name: DSI_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	RW	0x0	forcetxstopmode_3
29	RW	0x0	forcerxmode_3
28	RW	0x0	turndisable_3
27	/	/	/
26	RW	0x0	forcetxstopmode_2
25	RW	0x0	forcerxmode_2

24	RW	0x0	turndisable_2
23	/	/	/
22	RW	0x0	forcetxstopmode_1
21	RW	0x0	forcerxmode_1
20	RW	0x0	turndisable_1
19	/	/	/
18	RW	0x0	forcetxstopmode_0
17	RW	0x0	forcerxmode_0
16	RW	0x0	turndisable_0
15	RW	0x0	biston
14:4	/	/	/
3:0	RW	0x0	basedir

7.2.4.32. 0x0404 DSI Configure Register1(Default Value: 0x0000_0000)

Offset: 0x0404			Register Name: DSI_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	RW	0x0	dpi_en
30:4	/	/	/
3:2	RW	0x0	dpi_input_format 00: 24bit 01: 18bit 10: 16bit 11: reserved
1	RW	0x0	dpi_color_mode
0	RW	0x0	dpi_shut_down

7.2.4.33. 0x0408 DSI Configure Register2(Default Value: 0x0000_0000)

Offset: 0x0408			Register Name: DSI_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	RW	0x0	dbi_en
30:2	/	/	/
1	RW	0x0	lcd_te_en
0	RW	0x0	dbi_rst_n

7.2.4.34. 0x040C DSI Configure Register3(Default Value: 0x0000_0000)

Offset: 0x040C			Register Name: DSI_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

30	RW	0x0	reg_rext
29:28	RW	0x2	reg_rint
27:23	/	/	/
22:20	RW	0x2	reg_snk
19:8	/	/	/
7	RW	0x0	sram3_bist_en 64x32
6	RW	0x0	sram2_bist_en 128x32
5	RW	0x0	sram1_bist_en 1024x32
4	RW	0x0	sram0_bist_en 1536x32
3:1	/	/	/
0	RW	0x0	bist_en

7.2.4.35. 0x0410 DSI Status Register0(Default Value: 0x0000_0000)

Offset: 0x0410			**Register Name: DSI_STS0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	bist_ok

7.3. Display Stream Parallel Output(DSPO)

7.3.1. Overview

The Display Stream Parallel Output (DSPO) is a parallel digital video output interface that compatible with ITU-R BT.656/1120 protocol. It transfers video data in YUV422 up to full-HD format. It works in two mode, 16-bit data output with one Y-channel and one C-channel or 8-bit data output.

The DSPO includes the following features:

- Supports BT1120 (16 bits) max resolution of 2688 x 2688 @15fps / 3840 x 2160 @15fps (**only V833 supports**)
- Supports BT656 (8 bits) max resolution of 1080p@30fps / 720p@60fps
- Supports embedded H.V.F sync or separate H.V.F sync
- Supports 2 DMAs to get RGB888/YUV444/YUV422/YUV420 image data from DRAM
- Supports YUV422/YUV420 image data from ISP or CSIC

The maximum output frequency of GPIO is 150MHz. In BT1120 mode, 16 GPIOs parallel output data displays in 3840 x 2160 @15Hz frame rate. In BT656 mode, only 8 GPIOs parallel output data, the frame rate will be half of BT1120 mode if it is displayed the same video.

NOTE

The DSPO of V833 is 16-bit data interface, the DSPO of V831 is 8-bit data interface.

7.3.2. Block Diagram

The block diagram of DSPO is shown as follows.

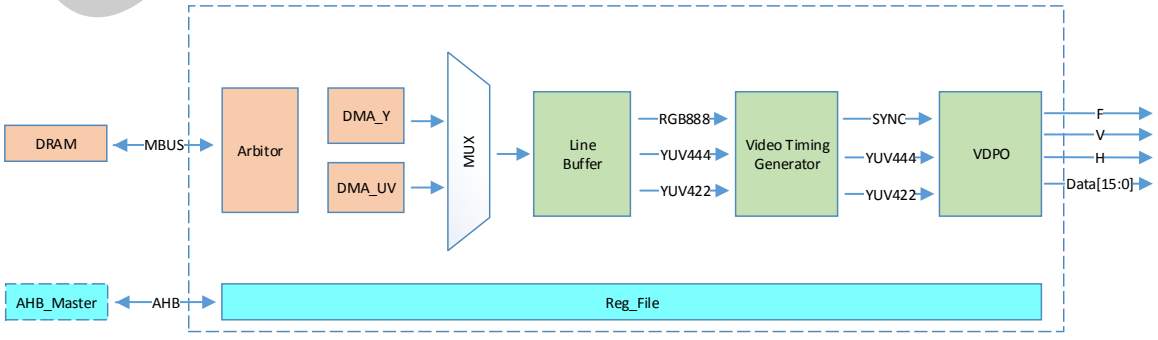

Figure 7- 9. DSPO Block Diagram

7.3.3. Operations and Functional Descriptions

7.3.3.1. External Signals

Table 7- 9. DSPO External Signals

V833 Signal	V831 Signal	Description	Type
VO_D0	VO_D0	Video Output Data0	O
VO_D1	VO_D1	Video Output Data1	O
VO_D2	VO_D2	Video Output Data2	O
VO_D3	VO_D3	Video Output Data3	O
VO_D4	VO_D4	Video Output Data4	O
VO_D5	VO_D5	Video Output Data5	O
VO_D6	VO_D6	Video Output Data6	O
VO_D7	VO_D7	Video Output Data7	O
VO_D8	/	Video Output Data8	O
VO_D9	/	Video Output Data9	O
VO_D10	/	Video Output Data10	O
VO_D11	/	Video Output Data11	O
VO_D12	/	Video Output Data12	O
VO_D13	/	Video Output Data13	O
VO_D14	/	Video Output Data14	O
VO_D15	/	Video Output Data15	O
VO_CLK	VO_CLK	Clock for Video Data Output	O
VO_HSYNC	VO_HSYNC	Horizontal Blanking Signal	O
VO_VSYNC	VO_VSYNC	Vertical Blanking Signal	O
VO_FIELD	VO_FIELD	Field Indicate Signal	O

7.3.3.2. Clock Sources

Table 7- 10. DSPO Clock Sources

Clock Sources	Description
VDPO SCLK	Source CLK from Video PLL

7.3.3.3. Typical Output Data Timing Format

7.3.3.3.1. 1080p@60/50/30/24Hz

Horizontal timing(16-bit mode):

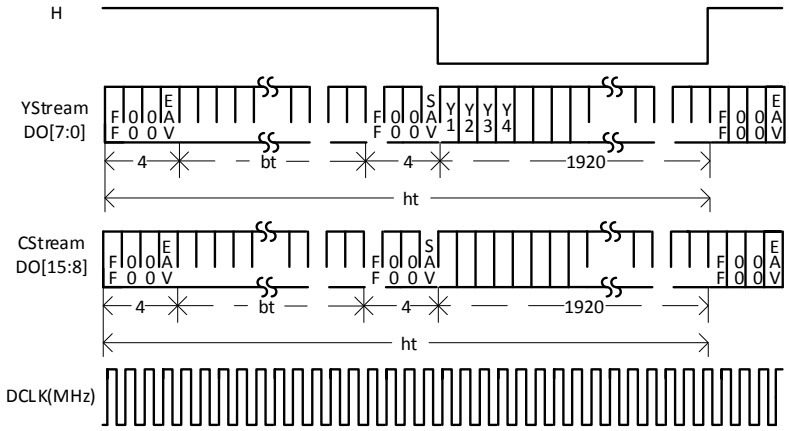

Figure 7- 10. BT.1120 60/50/30/24p YC Channel Mode Horizontal Timing Diagram

Table 7- 11. Relation between Frame Frequency and DCLK in BT.1120 60/50/30/24p Mode

Frame Frequency	ht(DCLK)	DCLK(MHz)
60P	2200	148.5
50P	2640	148.5
30P	2200	74.25
24P	2750	74.25

Vertical timing:

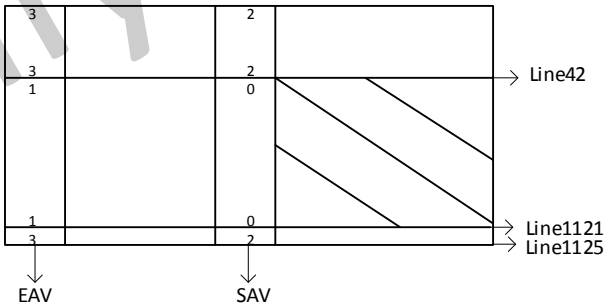

Figure 7- 11. 1080p Vertical Timing Diagram

7.3.3.3.2. 1080I@60/50Hz

Horizontal timing(16-bit mode):

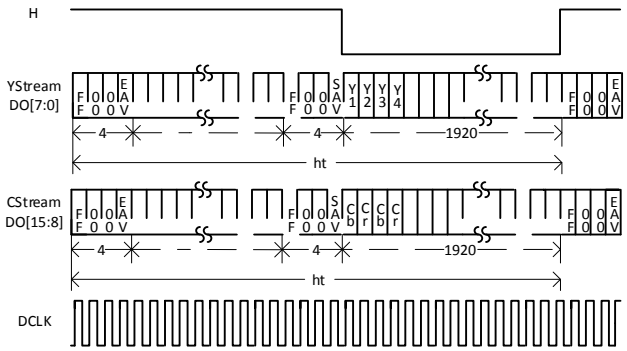

Figure 7- 12. BT.1120 60/50i Horizontal Timing Diagram

Table 7- 12. Relation between Frame Frequency and DCLK in BT.1120 60/50i Mode

Frame Freq	ht(DCLK)	DCLK(MHz)
60I	2200	74.25
50I	2640	74.25

Vertical timing:

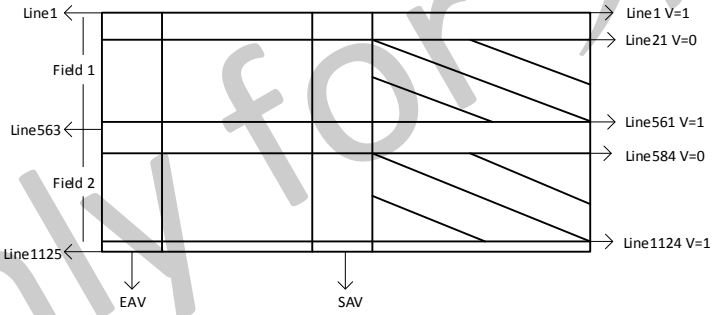

Figure 7- 13. BT.1120 60/50i Vertical Timing Diagram

7.3.3.3.3. 525line@59.94Hz(BT.656)

Horizontal timing(8-bit mode):

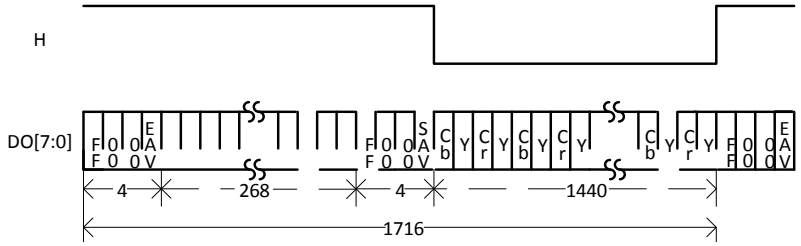

Figure 7- 14. 525line Horizontal Timing Diagram

Table 7- 13. Relation between Frame Frequency and DCLK in BT.656 525line Mode

Frame Frequency	DCLK(MHz)
60I	27

Vertical timing:

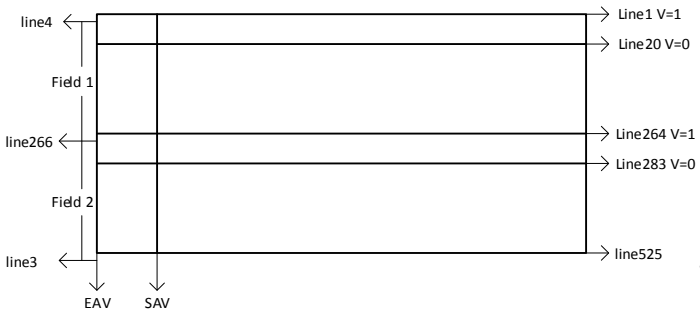

Figure 7- 15. 525line Vertical Timing Diagram

7.3.3.3.4. 625line@50Hz(BT.656)

Horizontal timing(8-bit mode):

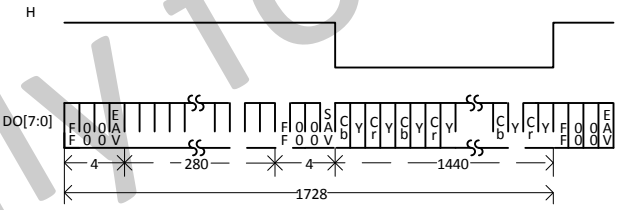

Figure 7- 16. 625line Horizontal Timing Diagram

Table 7- 14. Relation between Frame Frequency and DCLK in BT.656 625line Mode

Frame Freq	DCLK(MHz)
50I	27

Vertical timing:

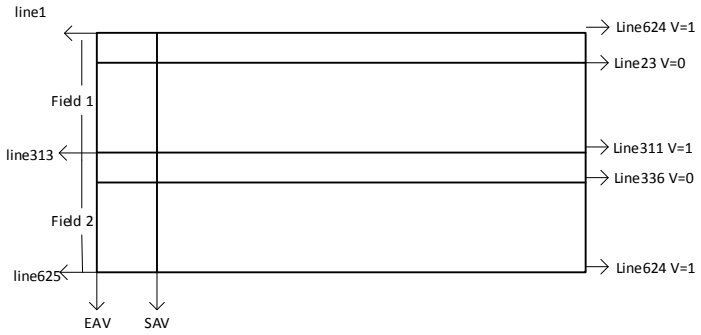

Figure 7- 17. 625line Vertical Timing Diagram

7.3.3.3.5. 720P@60/50/30/24Hz

Horizontal timing(16-bit mode):

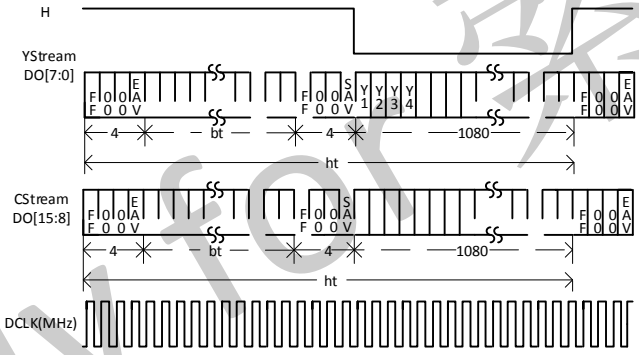

Figure 7- 18. 720p YC Channel Mode Horizontal Timing Diagram

Table 7- 15. Relation between Frame Frequency and DCLK in 720p 16-bit Mode

Frame Frequency	ht(DCLK)	DCLK(MHz)
60P	/	37.125
50P	/	37.125

Horizontal timing(8-bit mode):

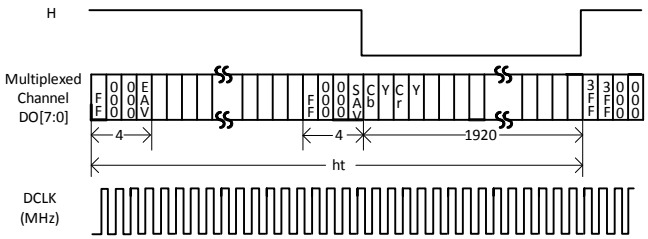

Figure 7- 19. 720P Horizontal Timing Diagram

Table 7- 16. Relation between Frame Frequency and DCLK in 720p 8-bit Mode

Frame Frequency	ht(DCLK)	DCLK(MHz)
60P	/	74.25
50P	/	74.25

Vertical timing:

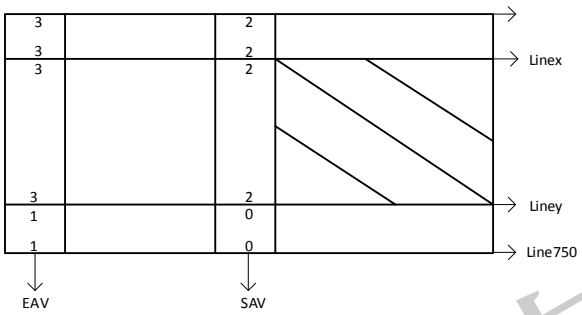

Figure 7- 20. 720p Vertical Timing Diagram

7.3.3.4. BT.656 or BT.1120 SYNC Signal

In BT.656 or BT.1120, in every line, the active video data starts right after a 4-byte sync signal(SAV) and finish with a 4-byte sync signal after the active video data (EAV), the definition of 4-byte sync signal data is shown below.

MSB	SAV/EAV bit status			Protection bit			
Bit 7	Bit 6(F)	Bit 5(V)	Bit 4(H)	Bit 3(P3)	Bit 2(P2)	Bit 1(P1)	Bit 0(P0)
1	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	1
1	0	1	1	0	1	1	0
1	1	0	0	0	1	1	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	0
1	1	1	1	0	0	0	1

F: Field signal

V: vertical blanking signal

H: horizontal blanking signal

P3: P3= V⊕H

P2: P2= F⊕H

P1: P1= F⊕V

P0: P0= F⊕V⊕H

7.3.3.5. Input Data Format

The module supports 10 input formats.

Table 7- 17. DSPO Input Data Format

Color Standard	Mode
RGB	ARGB888
YUV444	YUV444
YUV422	Interleaved YUV422(V0Y1U0Y0)
	Interleaved YUV422(Y1V0Y0U0)
	Interleaved YUV422(U0Y1V0Y0)
	Interleaved YUV422(Y1U0Y0V0)
	Planar YUV422 UV combined(V1U1V0U0)
	Planar YUV422 UV combined(U1V1U0V0)
YUV420	Planar YUV420 UV combined(V1U1V0U0)
	Planar YUV420 UV combined(U1V1U0V0)

The data format of ARGB888 is as follows.

Table 7- 18. ARGB888 Data Format

31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0
A00	R00	G00	B00	A01	R01	G01	B01	A02	R02	G02	B02	A03	R03	G03	B03
A10	R10	G10	B10	A11	R11	G11	B11	A12	R12	G12	B12	A13	R13	G13	B13
A20	R20	G20	B20	A21	R21	G21	B21	A22	R22	G22	B22	A23	R23	G23	B23
A30	R30	G30	B30	A31	R31	G31	B31	A32	R32	G32	B32	A33	R33	G33	B33

The A component in ARGB888 is removed, RGB data is converted to YUV444 through Color Space Converter(CSC), then filter sampling, YUV422 data is obtained. For details, see section 7.3.3.7 and section 7.3.3.8.

Table 7- 19. YUV444 Data Format

31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0
X	Y00	U00	V00	X	Y01	U01	V01	X	Y02	U02	V02
X	Y10	U10	V10	X	Y11	U11	V11	X	Y12	U12	V12
X	Y20	U20	V20	X	Y21	U21	V21	X	Y22	U22	V22
X	Y30	U30	V30	X	Y31	U31	V31	X	Y32	U32	V32

Table 7- 20. Interleaved YUV422(V0Y1U0Y0) Data Format

7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
Y00	U00	Y01	V00	Y02	U01	Y03	V01
Y10	U10	Y11	V10	Y12	U11	Y13	V11
Y20	U20	Y21	V20	Y22	U21	Y23	V21
Y30	U30	Y31	V30	Y32	U31	Y33	V31

Table 7- 21. Interleaved YUV422(Y1V0Y0U0) Data Format

7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
U00	Y00	V00	Y01	U01	Y02	V01	Y03
U10	Y10	V10	Y11	U11	Y12	V11	Y13
U20	Y20	V20	Y21	U21	Y22	V21	Y23
U30	Y30	V30	Y31	U31	Y32	V31	Y33

Table 7- 22. Interleaved YUV422(U0Y1V0Y0) Data Format

7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
Y00	V00	Y01	U00	Y02	V01	Y03	U01
Y10	V10	Y11	U10	Y12	V11	Y13	U11
Y20	V20	Y21	U20	Y22	V21	Y23	U21
Y30	V30	Y31	U30	Y32	V31	Y33	U31

Table 7- 23. Interleaved YUV422(Y1U0Y0V0) Data Format

7:0	15:8	23:16	31:24	7:0	15:8	23:16	31:24
V00	Y00	U00	Y01	V01	Y02	U01	Y03
V10	Y10	U10	Y11	V11	Y12	U11	Y13
V20	Y20	U20	Y21	V21	Y22	U21	Y23
V30	Y30	U30	Y31	V31	Y32	U31	Y33

Table 7- 24. Planar YUV422 UV Combined(V1U1V0U0) Data Format

7:0	15:8	23:16	31:24
Y00	Y01	Y02	Y03
Y10	Y11	Y12	Y13
Y20	Y21	Y22	Y23
Y30	Y31	Y32	Y33
U00	V00	U01	V01
U10	V10	U11	V11
U20	V20	U21	V21
U30	V30	U31	V31

Table 7- 25. Planar YUV422 UV Combined(U1V1U0V0) Data Format

7:0	15:8	23:16	31:24
Y00	Y01	Y02	Y03
Y10	Y11	Y12	Y13
Y20	Y21	Y22	Y23
Y30	Y31	Y32	Y33
V00	U00	V01	U01
V10	U10	V11	U11
V20	U20	V21	U21
V30	U30	V31	U31

Table 7- 26. Planar YUV420 UV Combined(V1U1V0U0) Data Format

7:0	15:8	23:16	31:24
Y00	Y01	Y02	Y03
Y10	Y11	Y12	Y13
Y20	Y21	Y22	Y23
Y30	Y31	Y32	Y33
U00	V10	U01	V11
U20	V30	U21	V31

Table 7- 27. Planar YUV420 UV Combined(U1V1U0V0) Data Format

7:0	15:8	23:16	31:24
Y00	Y01	Y02	Y03
Y10	Y11	Y12	Y13
Y20	Y21	Y22	Y23
Y30	Y31	Y32	Y33
V10	U00	V11	U01
V30	U20	V31	U21

7.3.3.6. DMA Descriptor

The DMA of the module only supports read-operation, and supports chain-structure. Each DMA descriptor points to the only data area and the next descriptor address. Depending on the format of the data source, the component storage area is different, the descriptor reads 3 component information (RGB888, YUV444, YUV422 interleave) at once time. The component2 is only used in YUV422 planar and YUV420 planar.

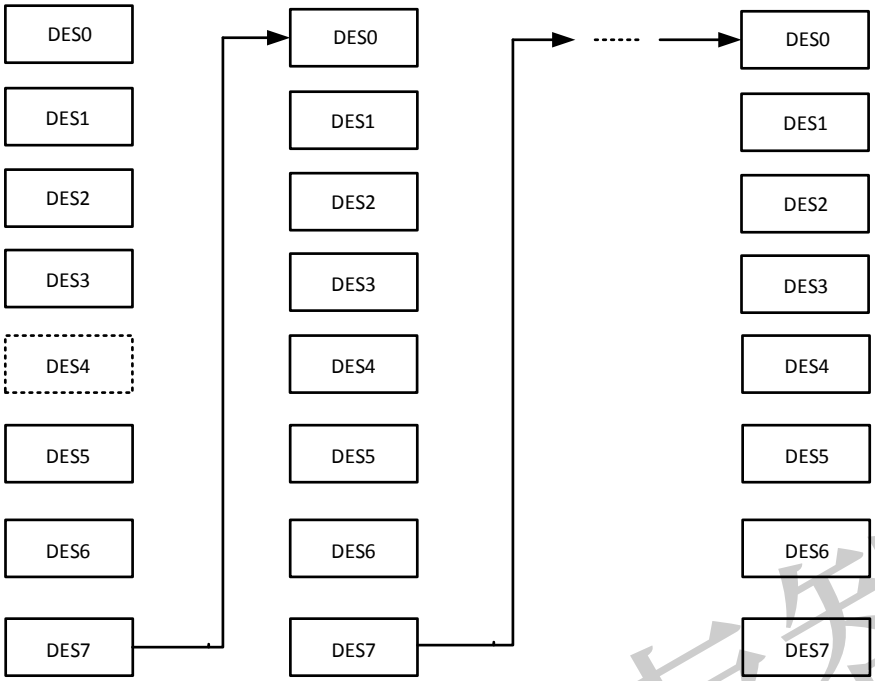

Figure 7- 21. DSPO Descriptor Chain Structure

DESC_0 is used to configure whether the descriptor is chained or non-chained.

DESC_0		
Bits	**Name**	**Descriptor**
31:2	/	/
1	Last descriptor Flag	LAST_FLAG When set, this bit indicates that the buffers pointed by this descriptor are the last data buffer.
0	Chain Flag	CHAIM_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.

DESC_1 is used to configure picture data type.

DESC_1		
Bits	**Name**	**Descriptor**
31:4	/	/
3:0	Video Data Type	0000: ARGB888 0001: YUV444 0100: Interleaved YUV422(V0Y1U0Y0) 0101: Interleaved YUV422(Y1V0Y0U0) 0110: Interleaved YUV422(U0Y1V0Y0) 0111: Interleaved YUV422(Y1U0Y0V0)

		1000: Planar YUV422 UV combined(V1U1V0U0) 1010: Planar YUV422 UV combined(U1V1U0V0) 1100: Planar YUV420 UV combined(V1U1V0U0) 1110: Planar YUV420 UV combined(U1V1U0V0) Others: Reserved

DESC_2 is used to configure the size of the picture, take 320 x 240 as an example: Column Size = 320, Row Size = 240

DESC_2		
Bits	**Name**	**Descriptor**
31:29	/	/
28:16	Column Size	COL_SIZE These bits indicate height of the picture data, unit is pixel clock
15:13	/	/
11:0	Row Size	ROW_SIZE These bits indicate line of the picture data, unit is line

DESC_3 and DESC_4 are used to configure the start address of a frame picture. If picture data type is RGB888/YUV444/YUV422 Interleave, all pixel components store in the same area, only the BUFF0_ADDR of DESC_3 needs be configured. If picture data type is YUV422 Combined/YUV420, Y component and UV component store in different area, the BUFF0_ADDR of DESC_3 and the BUFF1_ADDR of DESC_4 need be configured.

DESC_3		
Bits	**Name**	**Descriptor**
31:0	Buffer 0 address pointer	BUFF0_ADDR The word address indicates the physical address of data buffer for component 0. For data type: RGB888, YUV444, YUV420 Interleave

DESC_4		
Bits	**Name**	**Descriptor**
31:0	Buffer 1 address pointer	BUFF1_ADDR The word address indicates the physical address of data buffer for component 1. For data type : YUV422 combined , YUV420

DESC_5 and DESC_6 are used to configure the increasing address of the read picture data.

DESC_5		
Bits	**Name**	**Descriptor**
31:16	/	/
15:0	Buffer0 Line Stride	BUF0_LINE_STRIDE These bits indicate the actual store size of one line component 0 in

		Buffer 0, unit is byte, always multiple of 8.

DESC_6		
Bits	**Name**	**Descriptor**
31:16	/	/
15:0	Buffer1 Line Stride	BUF1_LINE_STRIDE These bits indicate the actual store size of one line component 1 in Buffer 1, unit is byte, always multiple of 8.

For different data type, the configuration of Buffer0/1 Line Stride is as follows.

Data Type	Configuration
RGB888	BUF0_LINE_STRIDE = Column Size * 4 BUF1_LINE_STRIDE configuration invalid
YUV444	BUF0_LINE_STRIDE = Column Size * 4 BUF1_LINE_STRIDE configuration invalid
YUV422 Interleave	BUF0_LINE_STRIDE = Column Size * 2 BUF1_LINE_STRIDE configuration invalid
YUV422 Combined	BUF0_LINE_STRIDE = Column Size BUF1_LINE_STRIDE = Column Size
YUV420 Combined	BUF0_LINE_STRIDE = Column Size BUF1_LINE_STRIDE = Column Size

DESC_7 is used to configure next descriptor address.

DESC_7		
Bits	**Name**	**Descriptor**
31:0	Next descriptor address	NEXT_DESP_ADDR The word address indicates the pointer to the physical memory where the next descriptor is present. It must be a multiple of 4 bytes.

7.3.3.7. Color Space Converter

Color Space Converter is used to convert RGB data to YUV(R'B'G') color space data. The conversion formula is as follows.

R' = (((Rr*R + Rg*G + Rb*B +8)/16)+ Rc+8)/16
G' = (((Gr*R + Gg*G + Gb*B +8)/16) +Gc+8)/16
B' = (((Br*R + Bg*G + Bb*B +8)/16) + Bc+8)/16

Note:

Rr, Rg, Rb ,Gr, Gg, Gb, Br, Bg, Bb	s13	(-4096,4096)
Rc, Gc, Bc	s19	(-262144, 262144)
R, G, B	u8	[0-255]

R' has the range of [Rmin ,Rmax]
G' has the range of [Rmin ,Rmax]
B' has the range of [Rmin ,Rmax]

7.3.3.8. Video Data Sampling and Clamp

7.3.3.8.1. YCbCr4:4:4 to YCbCr4:2:2 Down-Sampling

In this conversion, horizontal resolution of Cb and Cr component will be down-sampled by 2.
A 8-taps FIR filter will be applied to the input data:
For each line, Cb and Cr are filtered and down-sampled by 2 in horizontal direction:

```
yuv422_width = width >> 1;
for (i = 0;i < yuv422_width; i++)
{
    j = i << 1;
    filtered(i) = (in(j-3)*HCOEF[0] + in(j-2)*HCOEF[1] + in(j-1)*HCOEF[2] + in(j)*HCOEF[3] + in(j+1)*HCOEF[4] +
in(j+2)*HCOEF[5] + in(j+3)*HCOEF[6] + in(j+4)*HCOEF[7] + 0x20) >> 6;
 }
```

NOTE

If (j-n)<0, in(j-n)=in(0), n can be 3/2/1.
If (j+n)> (width-1), in(j+n)=in(width-1), n can be 3/2/1.

Cb and Cr can be selected different COEF_SEL type.

Table 7- 28. HCOEF Value

COEF_SEL TYPE	HCOEF							
	[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]
0	-2	0	18	32	18	0	-2	0
1	0	-2	0	18	32	18	0	-2
2	0	-2	7	27	27	7	-2	0
3	0	0	-2	7	27	27	7	-2
4	0	0	0	64	0	0	0	0
5	0	0	0	0	64	0	0	0
6	0	0	0	32	32	0	0	0
7	0	0	0	0	32	32	0	0

When the COEF_SEL type is 4, it indicates that data is not filtered.

7.3.3.8.2. YCbCr4:2:0 to YCbCr4:2:2 Up-Sampling

For YUV420, 2-lines Y components share 1-line U component, V component, so when reconstructing YUV422 data, the U component, V component per line need be copyed once, then paired with adjacent 2-lines Y component to reconstruct YUV422 data.

Table 7- 29. Planar YUV420 UV Combined(U1V1U0V0) Data Format

Y00	Y01	Y02	Y03
Y10	Y11	Y12	Y13
Y20	Y21	Y22	Y23
Y30	Y31	Y32	Y33
U00	V10	U01	V11
U20	V30	U21	V31

YUV420 is reconstructed to YUV422, the data format is as follows.

Table 7- 30. YUV422 Data Format by YUV420 Reconstructed

Y00	U00	Y01	V10	Y02	U01	Y03	V11
Y10	U00	Y11	V10	Y12	U01	Y13	V11
Y20	U20	Y21	V30	Y22	U21	Y23	V31
Y30	U20	Y31	V30	Y32	U21	Y33	V31

7.3.3.8.3. Video Data Clamp

Video data Clamp module is behind horizontal chrominance down-sampling module, the YCbCr422 video data can be clamped like below:

```
if(video_val < lowlimit)
    return lowlimit;
else if(video_val > uplimit)
    return uplimit;
else
    return val;
```

Y, Cb, Cr can be selected different low limit and up limit.

7.3.3.8.4. Blanking Data

The data words occurring during digital blanking intervals that are not used for the timing reference codes (SAV and

EAV), line number data, the error detection codes or ancillary data (ANC) are filled with words corresponding to the following blanking levels, appropriately placed in the multiplexed data:

64(10)/16(8) for Y signals

512(10)/128(8) for CB ,CR

7.3.3.9. Working Mode

7.3.3.9.1. DMA Register Descriptor

Configure DMA_TCON_CTRL_REG [7] to 1, the DMA will not read descriptor from DRAM, the descriptor should be configured by local register. After completed register descriptor configuration, enable DMA_START.

DMA_START_REG	0x0044
DMA_TCON_CTRL_REG	0x004C
DMA_SIZE_REG	0x0050
DMA_Y_BASE_ADDR_REG	0x0054
DMA_CbCr_BASE_ADDR_REG	0x0058
DMA_BUF_LINE_STRIDE_REG	0x005C

After DMA obtains one frame picture, DMA_DONE interrupt will be triggered. Then update register(configure the address of the next frame), clear DMA_DONE interrupt, enable DMA_START.

7.3.3.9.2. DMA Abnormal Mode Processing

[Symptom]

After DMA interrupt is triggered, the descriptor and DMA_START have not been updated in time because of system, at this time TCON display module can not stop transferring data, Line Buffer can be read empty, which results in display exception.

[Solution]

When VDPO frame stops interrupt trigger, the new DMA descriptor and DMA_START are not triggered within N Hsync cycle, auto reload the descriptor of the previous picture address and enable DMA_START.

Offset: 0x004C			Register Name: DMA_TCON_CTRL_REG
Bit	Read/Write	Default/Hex	Description
18:12	R/W	0x0	dma_start_check Haraware detects automatically VDPO frame interrupt. If dma_start has not been triggered in N HSYNC cycle after interrupt, then dma_start can be triggered automatically to get the previous frame picture. N: 0 ~ 127

11:10	/	/	/
9	R/W	0x0	dma_start_check_en (detect whether dma_start trigger time meets expectation) 0: Disable 1: Enable In register descriptor and non-chain descriptor mode, if CPU does not response DMA interrupt in time, the new descriptor cannot be configured in time, which results in display exception.

7.3.3.9.3. DSPO Trigger Mode

Configure DMA_TCON_CTRL_REG [25] to 1 to set TCON trigger mode, configure DMA_TCON_CTRL_REG [26] to 1, after 10*Pixel_clk cycle(the delay time cannot exceed one frame time), re-configure DMA_TCON_CTRL_REG [26] to 0, then DSPO outputs one frame picture.

Before the first trigger, you need to check whether the Line Buffer caches enough data. When LINE_BUFFER_RANG _REG3 [0] is 1, it indicates the buffer requirement is reached. Then after VDPO frame interrupt is triggered, TCON trigger can be configured.

CAUTION

In trigger mode, after DMA_DONE is triggered, the descriptor needs be updated in time to avoid reading empty Line Buffer.

Offset: 0x004C			Register Name: DMA_TCON_CTRL_REG
Bit	Read/Write	Default/Hex	Description
26	R/W	0x0	TCON Trigger configure the bit to 1, after 10*Pixel_clk cycle(the delay time cannot exceed one frame time), re-configure the bit to 0, then DSPO outputs one frame picture.
25	R/W	0x0	TCON Trigger Mode 0 : Normal Mode 1 : Trigger Mode

7.3.4. Register List

Module Name	Base Address
DSPO	0x06543000

Register Name	Offset	Description

MODULE_CTRL_REG	0x0000	Module Control Register
FMT_CTRL_REG	0x0004	Output Data Format Control Register
SYNC_CTRL_REG	0x0008	Sync Signal Control Register
INT_CTRL_REG	0x000C	Interrupt Control Register
LINE_INT_NUM_REG	0x0010	Line Match Interrupt Register
DEUBG_STATUS_REG	0x0014	Debug Status Register
HOR_CHROMA_SPL _REG	0x0018	Horizontal Chrominance Down-sampling Control Register
CLAMP_CTRL_REG0	0x001C	Clamp Control 0 Register
CLAMP_CTRL_REG1	0x0020	Clamp Control 1 Register
CLAMP_CTRL_REG2	0x0024	Clamp Control 2 Register
INTERLACE_MODE_REG	0x0030	Configured V Total Timing Parameter
H_TIMING_REG0	0x0034	Configured H_FP, HSYNC Timing Parameter
H_TIMING_REG1	0x0038	Configured H_BP, H_ACTIVE Timing Parameter
V_TIMING_REG0	0x003C	Configured V_FP, VSYNC Timing Parameter
V_TIMING_REG1	0x0040	Configured V_BP, V_ACTIVE Timing Parameter
DMA_START_REG	0x0044	DMA Start Register
DMA_TCON_CTRL_REG	0x004C	DMA TCON Control Register
DMA_SIZE_REG	0x0050	DMA Size Register
DMA_Y_BASE_ADDR_REG	0x0054	DMA Y Base Address Register
DMA_CbCr_BASE_ADDR_REG	0x0058	DMA CbCr Base Address Register
DMA_BUF_LINE_STRIDE_REG	0x005C	DMA Buffer Line Stride Register
DMA_DESCRIPTOR_BASE_ADDR_REG	0x0060	DMA Descriptor Base Address Register
CSC_CEU_CTL_REG	0x0064	Color Space Convert Function Enable
CSC_CEU_COEF_MUL_REG	0x0070 + N*0x04	N = 0 ~ 10 Configured Color Space Convert Coefficient
CSC_CEU_COEF_REG	0x00b0 + N*0x04	N = 0 ~ 2 Configured Color Space Convert Coefficient
LINE_BUFFER_RANG_REG0	0x00C0	Configured DMA Line Buffer Y Capacity
LINE_BUFFER_RANG_REG1	0x00C4	Configured DMA Line Buffer UV Capacity
LINE_BUFFER_RANG_REG3	0x00CC	Line Buffer Capacity Attained Aim Value
BIST_CTRL_REG	0x0100	Bist Control Register
BIST_START_ADDR_REG	0x0104	Bist Start Address Register
BIST_END_ADDR_REG	0x0108	Bist End Address Register
BIST_DATA_MASK_REG	0x010C	Bist Data Mask Register

7.3.5. Register Description

7.3.5.1. 0x0000 Module Control Register(Default Value: 0x0000_0004)

Offset: 0x0000			Register Name: MODULE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/

4	R/W	0x0	Bist_Mode 0:disable 1:enable
3	R/W	0x0	Reserved
2	R/W	0x1	Soft_rstn 0: reset 1: invalid It resets all the modules which is exclusive of configuration register
1	R/W	0x0	Separate_Sync_En 0: disable 1: enable
0	R/W	0x0	VDPO_Module_En 0: disable 1: enable

7.3.5.2. 0x0004 Output Data Format Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			**Register Name: FMT_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	Data_Seq_Sel 0x0: Cb->Y->Cr->Y 0x1: Cr->Y->Cb->Y 0x2: Y->Cb->Y->Cr 0x3: Y->Cr->Y->Cb If is dual data channel mode(Output_Data_Width=1), if output sequence q is A->B->C->D, Then D15-D8: A->C D7-D0: B->D If is one data channel mode(Output_Data_Width=0), If output sequence is A->B->C->D, Then D7-D0: A->B->C->D
7:5	/	/	/
4	R/W	0	Embedded_ Sync_Fmt 0: BT.1120 like If data output width is 16 bits, the format is: C channel: FF,00,00,EAV,XX……XX,FF,00,00,SAV Y channel: FF,00,00,EAV,XX……XX,FF,00,00,SAV If data output width is 10 bits, the format is: FF FF 00 00 EAV EAV XX……XX FF FF 00 00 SAV SAV 1: BT.656 like If data output width is 8 bits, the format is: C channel: FF 00 XX……XX FF 00

			Y channel: 00 EAV XX……XX 00 SAV If data output width is 8 bits, the format is: Multiplexed channel: FF 00 00 EAV XX……XX FF 00 00 SAV **Note: For RGB888/YUV444, the bit is 0.**
3	/	/	/
2	R/W	0	Data_Source_Sel 0: YUV444 to Packet Generator 1: YUV422 to Packet Generator
1	R/W	0	Prog_Intl_Mode 0: progress 1: interlace
0	R/W	0	Output_Data_Width 0: 8/10 bit data output(one Y channel) 1: 16/20 bit data output(one Y channel +one C channel)

7.3.5.3. 0x0008 Sync Signal Control Register(Default Value: 0x0000_0003)

Offset: 0x0008			**Register Name: SYNC_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	DCLK_Dly_En 0: disable 1: enable
9:4	R/W	0x0	DCLK_Dly_Num Number= bit[9:4]+1
3	R/W	0x0	DCLK_Invert 0: disable dclk invert 1: enable dclk invert
2	R/W	0x0	Field_Pol Field indicate signal polarity Field_Pol=0: low level respects field 1, high level respects field2. Field_Pol=1: high level respects field 1, low level respects field 2.
1	R/W	0x1	V_Blank_Pol Vertical blanking signal polarity V_Blank_Pol=0: low level respects blanking, high level respects active. V_Blank_Pol=1: high level respects blanking, low level respects active.
0	R/W	0x1	H_Blank_Pol Horizonal blanking signal polarity H_Blank_Pol=0: low level respects blanking, high level respects active. H_Blank_Pol=1: high level respects blanking,

			low level respects active.

7.3.5.4. 0x000C Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: INT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W0C	0x0	Line Buffer Y overflow INT Trigger when Line Buffer Y overflow Write 0 to clear it.
27	R/W0C	0x0	Line Buffer UV overflow INT Trigger when Line Buffer UV overflow Write 0 to clear it.
26	R/W0C	0x0	Line Buffer Y underflow INT Trigger when Line Buffer Y underflow Write 0 to clear it.
25	R/W0C	0x0	Line Buffer UV underflow INT Trigger when Line Buffer UV underflow Write 0 to clear it.
24	R/W0C	0x0	DMA_UV_Line_INT DMA UV obtains one line picture from DRAM, only YUV422 Combine and YUV420 pictures are valid. Write 0 to clear it.
23	R/W0C	0x0	Frame_INT DMA mode: obtain one frame picture from DRAM Write 0 to clear it.
22	R/W0C	0x0	Line_INT DMA mode: DMA Y obtains one line picture from DRAM Write 0 to clear it.
21	R/W0C	0x0	DMA_DONE_INT DMA state machine completes descriptor processing Write 0 to clear it.
20	R/W0C	0x0	DMA_DESC_INT DMA accesses base address and obtains descriptor completely Write 0 to clear it.
19:18	/	/	/
17	R/W0C	0x0	Vb_Int_Flag(VDPO frame interrupt) Trigger when vertical blanking signal asserts Write 0 to clear it.
16	R/W0C	0x0	Line_Match_Int_Flag Trigger when current scan line number match the line number in INT_LINE_NUM_REG. Write 0 to clear it.

15:13	/	/	/
12	R/W	0x0	Line Buffer Y overflow INT EN 0: disable 1: enable
11	R/W	0x0	Line Buffer UV overflow INT EN 0: disable 1: enable
10	R/W	0x0	Line Buffer Y underflow INT EN 0: disable 1: enable
9	R/W	0x0	Line Buffer UV underflow INT EN 0: disable 1: enable
8	R/W	0x0	DMA_UV_Line_INT_EN 0: disable 1: enable
7	R/W	0x0	Frame_INT_EN 0: disable 1: enable
6	R/W	0x0	Line_INT_EN 0: disable 1: enable
5	R/W	0x0	DMA_DONE_INT_EN 0: disable 1: enable
4	R/W	0x0	DMA_DESC_INT_EN 0: disable 1: enable
3:2	/	/	/
1	R/W	0x0	Vb_Int_EN 0: disable 1: enable
0	R/W	0x0	Line_Match_Int_En 0: disable 1: enable

7.3.5.5. 0x0010 Interrupt Control Register(Default Value: 0x0000_0FFF)

Offset: 0x0010			**Register Name: LINE_INT_NUM_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0xFFF	Int_Line_Num(including inactive line) (Can be write only scan line match interrupt disable)

7.3.5.6. 0x0014 Debug Status Register(Default Value: 0x0001_0000)

Offset: 0x0014			Register Name: DEUBG_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R	0x1	Field_Pol_Sta 0: Even field in interlace mode 1: Odd field in interlace mode This bit always be 0 in progress mode.
15:13	/	/	/
12:0	R	0x0	Current _Line

7.3.5.7. 0x0018 Horizontal Chrominance Down-sampling Control Register(Default Value: 0x0000_0044)

Offset: 0x0018			Register Name: HOR_CHROMA_SPL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x4	Cr_Hor_Spl_Type For the detail of down-sampling type, see table7-28.
3	/	/	/
2:0	R/W	0x4	Cb_Hor_Spl_Type For the detail of down-sampling type, see table7-28.

7.3.5.8. 0x001C Clamp Control 0 Register(Default Value: 0x00FF_0000)

Offset: 0x001C			Register Name: CLAMP_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xFF	Y_Val_Range_Max
15:8	/	/	/
7:0	R/W	0x0	Y_Val_Range_Min

7.3.5.9. 0x0020 Clamp Control 1 Register(Default Value: 0x00FF_0000)

Offset: 0x0020			Register Name: CLAMP_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xFF	Cb_Value_Range_Max When data source type is RGB888/YUV444, the field is used to configure

			the maximum value of Cb. When data source type is YUV422/YUV420, the field is used to configure the maximum value of Cr.
15:8	/	/	/
7:0	R/W	0x0	Cb_Val_Range_Min When data source type is RGB888/YUV444, the field is used to configure the minimum value of Cb. When data source type is YUV422/YUV420, the field is used to configure the minimum value of Cr.

7.3.5.10. 0x0024 Clamp Control 2 Register(Default Value: 0x00FF_0000)

Offset: 0x0024			Register Name: CLAMP_CTRL_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xFF	Cr_Val_Range_Max When data source type is RGB888/YUV444, the field is used to configure the maximum value of Cr. When data source type is YUV422/YUV420, the field is used to configure the maximum value of Cb.
15:8	/	/	/
7:0	R/W	0x0	Cr_Val_Range_Min When data source type is RGB888/YUV444, the field is used to configure the minimum value of Cr. When data source type is YUV422/YUV420, the field is used to configure the minimum value of Cb.

7.3.5.11. 0x0030 Configured V Total Timing Parameter(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: INTERLACE_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	Interlace mode option Only valid in interlace mode , if V_Total is odd number: 1: field 1 has more 1 line then field 0, the line adds to field 1 vbp. **Note: bt656 like** 0: field 0 has more 1 line then field 1, the line adds to field 0 vfp. **Note: bt1120 like**
15	R/W	0x0	V_total Configuration Auto 0: Auto 1: Manual
14:13	/	/	/

12:0	R/W	0x0	V_total Parameter When V_total Configuration Auto is 1, the field is valid. Progressive Mode: V_total * 2 Interlaced Mode: V_total

7.3.5.12. 0x0034 Configured H_FP, HSYNC Timing Parameter(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: H_TIMING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	H_FP Horizontal Front Porch width.
15:10	/	/	/
9:0	R/W	0x0	H_SYNC Horizontal Sync pulse width.

7.3.5.13. 0x0038 Configured H_BP, H_ACTIVE Timing Parameter(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: H_TIMING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	H_BP Horizontal Black Porch width
15:13	/	/	/
12:0	R/W	0x0	H_Active Horizontal Active Area width

7.3.5.14. 0x003C Configured V_FP, VSYNC Timing Parameter(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: V_TIMING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	V_FP Vertical Front Porch Area length.
15:10	/	/	/
9:0	R/W	0x0	V_SYNC Vertical sync pulse width.

7.3.5.15. 0x0040 Configured V_BP, V_ACTIVE Timing Parameter(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: V_TIMING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	V_BP Vertical Black Porch width.
15:12	/	/	/
11:0	R/W	0x0	V_Active Vertical Active Area length.

7.3.5.16. 0x0044 DMA Start Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: DMA_START_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	dma_start In the information mode of register configuration descriptor, first must configure Input Data Type, X, Y, Y_BUF_ADDR, CbCr_BUF_ADDR before configuration. 0: disable 1: enable

7.3.5.17. 0x004C DMA TCON Control Register(Default Value: 0x0000_0000)

Configure DMA_TCON_CTRL_REG [25] to 1 to set TCON trigger mode, configure DMA_TCON_CTRL_REG [26] to 1, after 10*Pixel_clk cycle(the delay time cannot exceed one frame time), re-configure DMA_TCON_CTRL_REG [26] to 0, then DSPO outputs one frame picture.

Before the first trigger, you need to check whether the Line Buffer caches enough data. When LINE_BUFFER_RANG _REG3 [0] is 1, it indicates the buffer requirement is reached. Then after VDPO frame interrupt is triggered, TCON trigger can be configured.

CAUTION

In trigger mode, after DMA_DONE is triggered, the descriptor needs be updated in time to avoid reading empty Line Buffer.

Offset: 0x004C			Register Name: DMA_TCON_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28	R/W	0x0	TCON_MANU_EN (TCON manual mode is valid) 0: Disable 1: Enable
27	R/W	0x0	TCON_MANU 0: When the data of Line Buffer reaches the setting threshold, TCON is enabled automatically. 1: Software enables TCON mode.
26	R/W	0x0	TCON Trigger Firstly configure the bit to 1, after 10*Pixel_clk cycle(the delay time cannot exceed one frame time), secondly configure the bit to 0, then DSPO outputs one frame picture.
25	R/W	0x0	TCON Trigger Mode 0 : Normal Mode 1 : Trigger Mode
24:19	/	/	/
18:12	R/W	0x0	dma_start_check The hardware checks automatically VDPO frame interrupt, within N*HSYNC cycle after interrupt, if dma_start is not triggered, then dma_start can be auto-triggered to obtain the previous frame data. N: 0 ~ 127
11:10	/	/	/
9	R/W	0x0	dma_start_check_en Check whether the trigger time of dma_start consistents with expectations. 0: Disable 1: Enable In register descriptor and non-chain descriptor mode, if CPU does not respond in time DMA interrupt, the new descriptor does not configure in time, which causes display exception.
8	/	/	/
7	R/W	0x0	Reg descriptor mode 0: Get back descriptor mode from DRAM 1: Configure descriptor by register
6:5	R/W	0x0	DMA block size select These bits indicates block size for mbus outstanding 00: 256 bytes 01: 512 bytes 10: 1024 bytes 11: 2048 bytes
4	/	/	/
3:0	R/W	0x0	Input Data Type 0000: ARGB888 0001: YUV444 0100: Interleaved YUV422(V0Y1U0Y0)

			0101: Interleaved YUV422(Y1V0Y0U0) 0110: Interleaved YUV422(U0Y1V0Y0) 0111: Interleaved YUV422(Y1U0Y0V0) 1000: Planar YUV422 UV combined(V1U1V0U0) 1010: Planar YUV422 UV combined(U1V1U0V0) 1100: Planar YUV420 UV combined(V1U1V0U0) 1110: Planar YUV420 UV combined(U1V1U0V0) Others: Reserved

7.3.5.18. 0x0050 DMA Size Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: DMA_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	X In DMA descriptor mode, the field is read-only. The field is used to read out descriptor content. In register descriptor mode, the written and read datas are consistent.
15:0	R/W	0x0	Y In DMA descriptor mode, the field is read-only. The field is used to read out descriptor content. In register descriptor mode, the written and read datas are consistent.

7.3.5.19. 0x0054 DMA Y Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: DMA_Y_BASE_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BUF_0_ADDR RGB888/YUV444/YUV420 Interleave image format is stored in the starting address of DRAM. In DMA descriptor mode, the field is read-only. The field is used to read out descriptor content. In register descriptor mode, the written and read datas are consistent.

7.3.5.20. 0x0058 DMA CbCr Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: DMA_CbCr_BASE_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BUF_1_ADDR The UV component of YUV422 combined, YUV420 image format is stored in the starting address of DRAM. In DMA descriptor mode, the field is read-only. The field is used to read out descriptor content.

			In register descriptor mode, the written and read datas are consistent.

7.3.5.21. 0x005C DMA Buffer Line Stride Register(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: DMA_BUF_LINE_STRIDE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	BUF1_LINE_STRIDE In DMA descriptor mode, the field is read-only. The field is used to read out descriptor content. In register descriptor mode, the written and read datas are consistent.
15:0	R/W	0x0	BUF0_LINE_STRIDE In DMA descriptor mode, the field is read-only. The field is used to read out descriptor content. In register descriptor mode, the written and read datas are consistent.

7.3.5.22. 0x0060 DMA Descriptor Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: DMA_DESCRIPTOR_BASE_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Descriptor_ADDR

7.3.5.23. 0x0064 CSC CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: CSC_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CEU_EN 0: bypass 1: enable Enable CEU function

7.3.5.24. 0x0070+N*0x04 CSC CEU COEF MUL Register(Default Value: 0x0000_0000)

Offset: 0x0070+N*0x04			Register Name: CSC_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE N=0 ,offest (0x0070) : Rr N=1 , offest (0x0074): Rg N=2, offest (0x0078): Rb

			N=4, offest (0x0080): Gr N=5, offest (0x0084): Gg N=6, offest (0x0088): Gb N=8, offest (0x0090): Br N=9, offest (0x0094): Bg N=10, offest (0x0098): Bb Signed 13bit value, range of (-16,16).

7.3.5.25. 0x00A0+N*0x04 CSC CEU COEF Register(Default Value: 0x0000_0000)

Offset: 0x00A0+N*0x04			Register Name: CSC_CEU_COEF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE N=0, offest (0x00a0): Rc N=1, offest (0x00a4): Gc N=2, offest (0x00a8): Bc Signed 19bit value, range of (-16384, 16384).

7.3.5.26. 0x00B0+N*0x04 CSC CEU COEF Range Register(Default Value: 0x0000_0000)

Offset: 0x00B0+N*0x04			Register Name: CSC_CEU_COEF_RANG _REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255]. N=0, 0x00b0, (Y) N=1, 0x00b4, (U) N=2, 0x00b8, (V)
15:8	/	/	/
7:0	R/W	0xFF	CEU COEF_RANGE_MAX Unsigned 8bit value, range of [0,255]. N=0, 0x00b0, (Y) N=1, 0x00b4, (U) N=2, 0x00b8, (V)

7.3.5.27. 0x00C0 Line Buffer Range Register0(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: LINE_BUFFER_RANG _REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/

11:0	R/W	0x0	DMA Mode LB_Y Capacity The cached data of Line Buffer Y in DMA mode. (configured by image type and size) RGB888/YUV444: 0~2688 YUV422/YUV420: 0~5376

7.3.5.28. 0x00C4 Line Buffer Range Register1(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: LINE_BUFFER_RANG _REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	DMA Mode LB_UV Capacity The cached data of Line Buffer UV in DMA mode. (configured by image size) The data type is Planar format. YUV422/YUV420: 0~5376

7.3.5.29. 0x00CC Line Buffer Range Register3(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: LINE_BUFFER_RANG _REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	Line Buffer Capacity Ready The cached data of Line Buffer reaches the requirement set by LINE_BUFFER_RANG_REG0 ~ 2.

7.3.5.30. 0x0100 Bist Control Register(Default Value: 0x0000_0200)

Offset: 0x0100			Register Name: BIST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0:NO effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle
9	R	0x1	BIST_STOP BIST STOP

			0:running 1:STOP
8	R	0x0	BIST_BUSY BIST Busy 0:idle 1:busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select
4	R/W	0x0	BIST_ADDR_Mode_SEL BIST Address mode select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write data Pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST Enable A positive will trigger the BIST to start.

7.3.5.31. 0x0104 Bist Start Address Register(Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: BIST_START_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST Start Address BIST Start Address It is 32-bit aligned.

7.3.5.32. 0x0108 Bist End Address Register(Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: BIST_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST END Address BIST END Address It is 32-bit aligned.

7.3.5.33. 0x010C Bist Data Mask Register(Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: BIST_DATA_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0:Unmask 1:Mask

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Chapter 8 Video Input Interfaces

8.1. CSIC

8.1.1. Overview

The CMOS Sensor Interface Controller(CSIC) is an image or video input control module which can receive image or video data via digital camera(DC) interface, BT656 interface, BT601 interface, high speed serial interface like MIPI. The controller can store the data in memory directly.

The CSIC includes the following features:

- Supports 1 serial interface(MIPI) + 1 parallel interface
- Supports image crop function
- Parallel interface:
  - Supports 12-bit DC interface
  - Supports BT656, BT601, BT1120 interface
  - Supports ITU-R BT.656 time-multiplexed format up to 4*720p@30fps in DDR sample mode
  - Supports progress and interleave video input
  - Maximum video capture resolution for parallel interface to 5M@15fps or 1080p@30fps
  - Maximum pixel clock for parallel to 148.5MHz
- MIPI interface:
  - Supports MIPI Version 1.0
  - 1/2/4 Data Lanes configuration
  - Up to 1.0Gbps/Lane
  - **For V833**, maximum video capture resolution for serial interface up to 2592 x 1936@30fps RAW data or 4*1080p@25fps YUV422 data
  - **For V831**, maximum video capture resolution for serial interface up to 1080p@60fps

NOTE

V831 does not support parallel CSI, and V831 only supports 2 data lanes MIPI CSI.

8.1.2. Block Diagram

Figure 8-1 shows a function block diagram of the CSIC. The CSIC consists of Input Parser, ISP, VIPP and DMA Control. In addition, the controller has 2 Input Parsers, 1 ISP(only ISP0), 4 VIPPs and 4 DMAs.

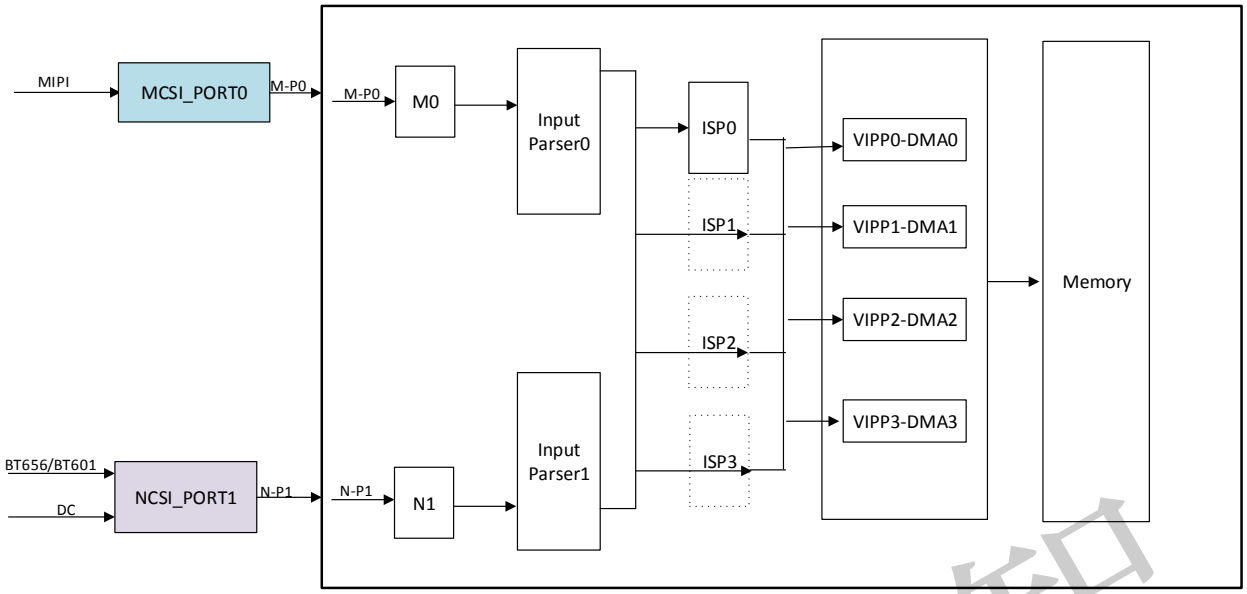

Figure 8- 1. CSIC Block Diagram

8.1.3. Operations and Functional Descriptions

8.1.3.1. External Signals

Table 8- 1. CSIC External Signals

V833 Signal	V831 Signal	Description	Type
MIPI CSI			
CSI_MASTERCLK0	CSI_MASTERCLK0	Master Clock for MIPI Sensor	O
CSI_SM_HS	CSI_SM_HS	MIPI CSI Slave Mode Horizontal SYNC	I
CSI_SM_VS	CSI_SM_VS	MIPI CSI Slave Mode Vertical SYNC	I
MCSI0_CKP	MCSI0_CKP	MIPI Clock Lane Positive Side	I
MCSI0_CKN	MCSI0_CKN	MIPI Clock Lane Negative Side	I
MCSI0_DP[3:0]	MCSI0_DP[1:0]	MIPI Data Lane Positive Side	I
MCSI0_DN[3:0]	MCSI0_DN[1:0]	MIPI Data Lane Negative Side	I
Parallel CSI			
CSI_MASTERCLK1	/	Master Clock for NCSI Sensor	O
NCSI1_PCLK	/	Pixel Clock	I
NCSI1_FIELD	/	FIELD Index Signal	I
NCSI1_VSYNC	/	Vertical SYNC Signal	I
NCSI1_HSYNC	/	Horizontal SYNC Signal	I
NCSI1_D0	/	Video Input Data0	I
NCSI1_D1	/	Video Input Data1	I
NCSI1_D2	/	Video Input Data2	I
NCSI1_D3	/	Video Input Data3	I
NCSI1_D4	/	Video Input Data4	I

NCSI1_D5	/	Video Input Data5	I
NCSI1_D6	/	Video Input Data6	I
NCSI1_D7	/	Video Input Data7	I
NCSI1_D8	/	Video Input Data8	I
NCSI1_D9	/	Video Input Data9	I
NCSI1_D10	/	Video Input Data10	I
NCSI1_D11	/	Video Input Data11	I
NCSI1_D12	/	Video Input Data12	I
NCSI1_D13	/	Video Input Data13	I
NCSI1_D14	/	Video Input Data14	I
NCSI1_D15	/	Video Input Data15	I

8.1.3.2. Parallel CSI Mapping

Table 8- 2. Parallel CSI Mapping

External Signals	8-bit DC Interface	10-bit DC Interface	12-bit DC Interface	16-bit DC Interface
NCSI1_D0	D0	D0	D0	Y0
NCSI1_D1	D1	D1	D1	Y1
NCSI1_D2	D2	D2	D2	Y2
NCSI1_D3	D3	D3	D3	Y3
NCSI1_D4	D4	D4	D4	Y4
NCSI1_D5	D5	D5	D5	Y5
NCSI1_D6	D6	D6	D6	Y6
NCSI1_D7	D7	D7	D7	Y7
NCSI1_D8	-	D8	D8	C0
NCSI1_D9	-	D9	D9	C1
NCSI1_D10	-	-	D10	C2
NCSI1_D11	-	-	D11	C3
NCSI1_D12	-	-	-	C4
NCSI1_D13	-	-	-	C5
NCSI1_D14	-	-	-	C6
NCSI1_D15	-	-	-	C7

8.1.3.3. Typical Application

CSIC module has 2 input ports and 4 DMA, which means CSIC can support 2 port input and 4 video streams output to memory simultaneously at most. This makes the applications very flexible.

CSIC supports following input cases:

- 1 serial input + 1 parallel DC input
- 1 BT656/BT1120 input interleaved 4-channel
- 1 MIPI VC input 4-channel

- 1 BT656/BT1120 input interleaved 2-channel + 1 MIPI VC input 2-channel

8.1.3.4. NCSI Timing

Figure 8-2 shows the timing of 8-bit CMOS sensor interface, in this figure clock active at the rising edge, vsync valid at positive, hsync valid at positive.

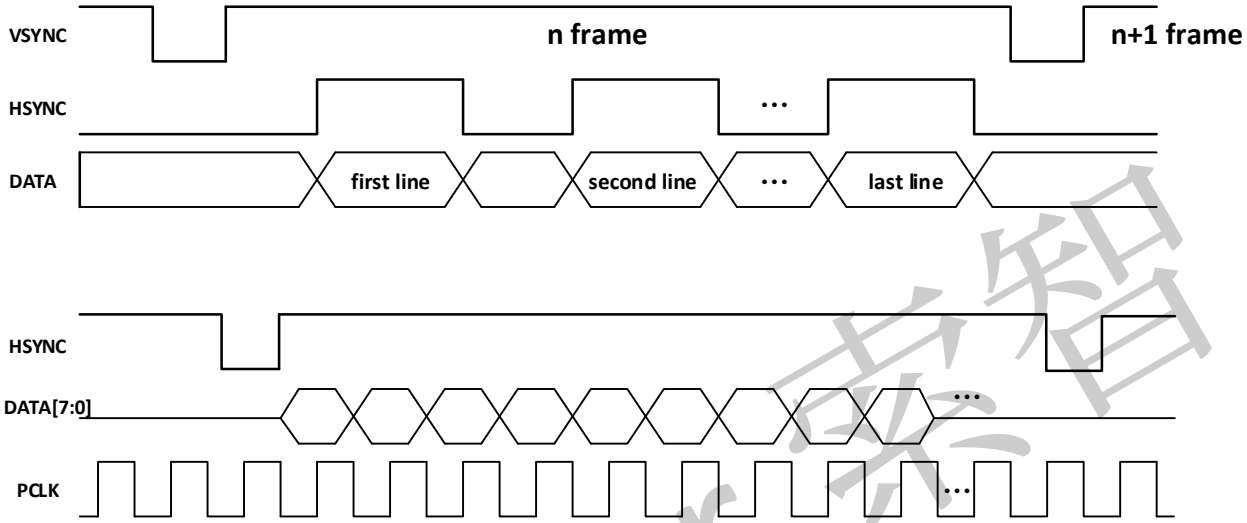

Figure 8- 2. 8-bit DC Sensor Interface Timing

Figure 8-3 shows the timing of 8-bit YCbCr4:2:2 with embedded syncs (BT656).

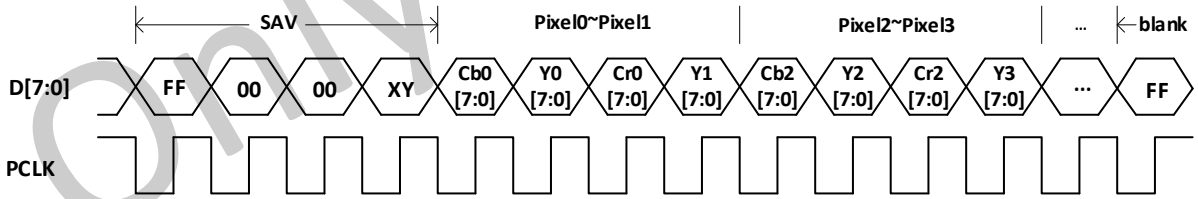

Figure 8- 3. 8-bit YCbCr4:2:2 with Embedded Syncs (BT656)

Figure 8-4 shows the data sample timing of CSI.

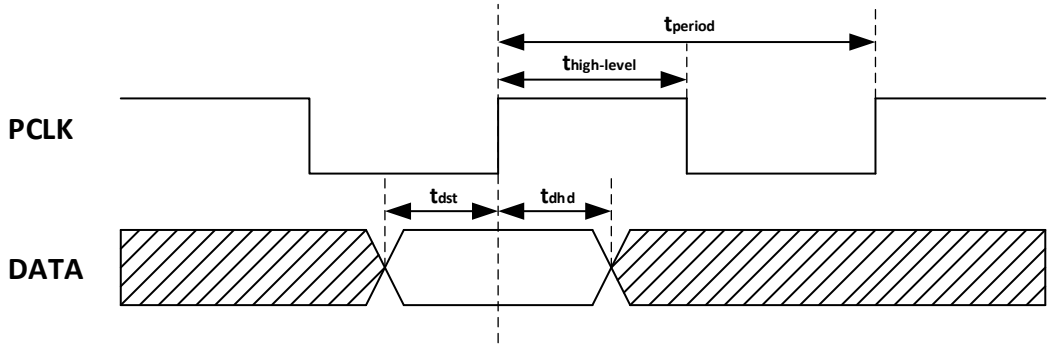

Figure 8- 4. Data Sample Timing

The timing parameter of CSI shows in Table 8-3.

Table 8- 3. CSIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk Period	t_{period}	6.7	-	-	ns
Pclk Frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk Duty	$t_{high\text{-}level}/t_{period}$	40	50	60	%
Data Input Setup Time	t_{dst}	0.6	-	-	ns
Data Input Hold Time	t_{dhd}	0.6	-	-	ns

8.1.3.5. CSIC FIFO Distribution

Table 8- 4. CSIC FIFO Distribution

Interface	YUYV422 Interleaved/Raw			MIPI Interface		
Input format	YUV422		Raw	YUV422		Raw
Output format	Planar	UV combined	Raw/RGB/PRGB	Planar	UV combined	Raw/RGB/PRGB
CH0_FIFO0	Y	Y	All pixels data	Y	Y	All pixels data
CH0_FIFO1	Cb (U)	CbCr (UV)	-	Cb (U)	CbCr (UV)	-
CH0_FIFO2	Cr (V)	-	-	Cr (V)	-	-

Table 8- 5. CSIC FIFO Distribution(Continued)

Interface	BT656 Interface	
Input format	YUV422	
Output format	Planar	UV combined
CH0_FIFO0	Y	Y
CH0_FIFO1	Cb (U)	CbCr (UV)
CH0_FIFO2	Cr (V)	-
CH1_FIFO0	Y	Y
CH1_FIFO1	Cb (U)	CbCr (UV)
CH1_FIFO2	Cr (V)	-
CH2_FIFO0	Y	Y
CH2_FIFO1	Cb (U)	CbCr (UV)
CH2_FIFO2	Cr (V)	-
CH3_FIFO0	Y	Y
CH3_FIFO1	Cb (U)	CbCr (UV)
CH3_FIFO2	Cr (V)	-

8.1.3.6. Pixel Format Arrangement

RAW-10:

Dummy1[5:0]	Raw data 1[9:0]	Dummy 0[5:0]	Raw data 0[9:0]

MSB LSB

Figure 8- 5. RAW-10 Format

RAW-12:

Dummy1[3:0]	Raw data 1[11:0]	Dummy 0[3:0]	Raw data 0[11:0]

MSB LSB

Figure 8- 6. RAW-12 Format

YUV-10:

Dummy1[5:0]	Y1[9:0]	Dummy 0[5:0]	Y 0[9:0]

MSB LSB

Figure 8- 7. Y of YUV-10 Format

Dummy1[5:0]	V/U 0[9:0]	Dummy 0[5:0]	U/V 0[9:0]

MSB LSB

Figure 8- 8. UV Combined of YUV-10 Format

RGB888:

B1[7:0]	R0[7:0]	G0[7:0]	B0[7:0]
G2[7:0]	B2[7:0]	R1[7:0]	G1[7:0]
R3[7:0]	G3[7:0]	B3[7:0]	R2[7:0]

MSB

Figure 8- 9. RGB888 Format

PRGB888:

PAD[7:0]	R0[7:0]	G0[7:0]	B0[7:0]

MSB LSB

Figure 8- 10. PRGB888 Format

RGB565:

R1[4:0]	G1[5:0]	B1[4:0]	R0[4:0]	G0[5:0]	B0[4:0]

MSB LSB

Figure 8- 11. RGB565 Format

8.1.3.7. CCIR656 Head Code

Table 8-6 shows the header code of CCIR656.

Table 8- 6. CCIR656 Header Code

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1
CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

Table 8-7 shows the header data bit definition of CCIR656.

Table 8- 7. CCIR656 Header Data Bit Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

8.1.3.8. Offset Definition

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.
For YUV422 format, pixel unit is a YU/YV combination.
For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.
For Bayer and RAW format, pixel unit is a R/G/B single component.
For RGB565, pixel unit is 2 bytes of RGB565 package.
For RGB888, pixel unit is 3 bytes of RGB combination.

8.1.3.9. Flip Definition

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.
If horizontal flip is enabled, one or more pixels will be taken as a unit:
For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be.
For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.
For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

8.1.4. Register List

Module Name	Base Address
CSIC_BASE	0x06600000
CSIC_CCU	0x06600000
CSIC_TOP	0x06600800
CSIC_PARSER0	0x06601000
CSIC_PARSER1	0x06602000
CSIC_DMA0	0x06609000
CSIC_DMA1	0x06609200
CSIC_DMA2	0x06609400
CSIC_DMA3	0x06609600
CSIC_MIPI0	0x0660C000
CSIC_ISP0	0x02100000
CSIC_VIPP0	0x02104000
CSIC_VIPP1	0x02104400
CSIC_VIPP2	0x02104800
CSIC_VIPP3	0x02104C00

CCU register list:

Register Name	Offset	Register Description
CCU_CLK_MODE_REG	0x0000	CCU Clock Mode Register
CCU_PARSER_CLK_EN_REG	0x0004	CCU Parser Clock Enable Register
CCU_ISP_CLK_EN_REG	0x0008	CCU ISP Clock Enable Register
CCU_POST0_CLK_EN_REG	0x000C	CCU Post0 Clock Enable Register

CSIC TOP register list:

Register Name	Offset	Register Description
CSIC_TOP_EN_REG	0x0000	CSIC TOP Enable Register
CSIC_PTN_GEN_EN_REG	0x0004	CSIC Pattern Generation Enable Register
CSIC_PTN_CTRL_REG	0x0008	CSIC Pattern Control Register

/	0x000C~0x001C	Reserved
CSIC_PTN_LEN_REG	0x0020	CSIC Pattern Generation Length Register
CSIC_PTN_ADDR_REG	0x0024	CSIC Pattern Generation Address Register
CSIC_PTN_ISP_SIZE_REG	0x0028	CSIC Pattern ISP Size Register
CSIC_ISP0_INPUT0_SEL_REG	0x0030	CSIC ISP0 Input0 Select Register
CSIC_ISP0_INPUT1_SEL_REG	0x0034	CSIC ISP0 Input1 Select Register
CSIC_ISP0_INPUT2_SEL_REG	0x0038	CSIC ISP0 Input2 Select Register
CSIC_ISP0_INPUT3_SEL_REG	0x003C	CSIC ISP0 Input3 Select Register
CSIC_ISP1_INPUT0_SEL_REG	0x0040	CSIC ISP1 Input0 Select Register
CSIC_ISP1_INPUT1_SEL_REG	0x0044	CSIC ISP1 Input1 Select Register
CSIC_ISP1_INPUT2_SEL_REG	0x0048	CSIC ISP1 Input2 Select Register
CSIC_ISP1_INPUT3_SEL_REG	0x004C	CSIC ISP1 Input3 Select Register
CSIC_ISP2_INPUT0_SEL_REG	0x0050	CSIC ISP2 Input0 Select Register
CSIC_ISP2_INPUT1_SEL_REG	0x0054	CSIC ISP2 Input1 Select Register
CSIC_ISP2_INPUT2_SEL_REG	0x0058	CSIC ISP2 Input2 Select Register
CSIC_ISP2_INPUT3_SEL_REG	0x005C	CSIC ISP2 Input3 Select Register
CSIC_ISP3_INPUT0_SEL_REG	0x0060	CSIC ISP3 Input0 Select Register
CSIC_ISP3_INPUT1_SEL_REG	0x0064	CSIC ISP3 Input1 Select Register
CSIC_ISP3_INPUT2_SEL_REG	0x0068	CSIC ISP3 Input2 Select Register
CSIC_ISP3_INPUT3_SEL_REG	0x006C	CSIC ISP3 Input3 Select Register
CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG	0x0070	CSIC ISP Bridge Buffer Maxuse Counter Clear Register
CSIC_ISP0_BRG_BUF_MAXUSE_CNT_REG	0x0074	CSIC ISP0 Bridge Buffer Maxuse Counter Register
/	0x0078~0x0080	Reserved
CSIC_ISP0_BRG_INT_EN_REG	0x0084	CSIC ISP0 Bridge Interrupt Enable Register
/	0x0088	Reserved
CSIC_ISP0_BRG_INT_PD_REG	0x008C	CSIC ISP0 Bridge Interrupt Pending Register
/	0x0090~0x009C	Reserved
CSIC_DMA0_INPUT_SEL_REG	0x00A0	CSIC DMA0 Input Select Register
CSIC_DMA1_INPUT_SEL_REG	0x00A4	CSIC DMA1 Input Select Register
CSIC_DMA2_INPUT_SEL_REG	0x00A8	CSIC DMA2 Input Select Register
CSIC_DMA3_INPUT_SEL_REG	0x00AC	CSIC DMA3 Input Select Register
CSIC_BIST_CS_REG	0x00DC	CSIC BIST CS Register
CSIC_BIST_CONTROL_REG	0x00E0	CSIC BIST Control Register
CSIC_BIST_START_REG	0x00E4	CSIC BIST Start Register
CSIC_BIST_END_REG	0x00E8	CSIC BIST End Register
CSIC_BIST_DATA_MASK_REG	0x00EC	CSIC BIST Data Mask Register
CSIC_MBUS_REQ_MAX_REG	0x00F0	CSIC MBUS REQ MAX Register
CSIC_MULF_MOD_REG	0x0100	CSIC Multi-Frame Mode Register
CSIC_MULF_INT_REG	0x0104	CSIC Multi-Frame Interrupt Register
CSIC_FEATURE_LIST_REG	0x01F0	CSIC Feature List Register

PARSER0/1 register list:

Register Name	Offset	Register Description
PRS_EN_REG	0x0000	Parser Enable Register
PRS_NCSIC_IF_CFG_REG	0x0004	Parser NCSIC Interface Configuration Register
PRS_MCSIC_IF_CFG_REG	0x0008	Parser MCSIC Interface Configuration Register
PRS_CAP_REG	0x000C	Parser Capture Register
PRS_SIGNAL_STA_REG	0x0010	Parser Signal Status Register
PRS_NCSIC_BT656_HEAD_CFG_REG	0x0014	Parser NCSIC BT656 Header Configuration Register
/	0x0018~0x0020	Reserved
PRS_C0_INFMT_REG	0x0024	Parser Channel_0 Input Format Register
PRS_C0_OUTPUT_HSIZE_REG	0x0028	Parser Channel_0 Output Horizontal Size Register
PRS_C0_OUTPUT_VSIZE_REG	0x002C	Parser Channel_0 Output Vertical Size Register
PRS_C0_INPUT_PARA0_REG	0x0030	Parser Channel_0 Input Parameter0 Register
PRS_C0_INPUT_PARA1_REG	0x0034	Parser Channel_0 Input Parameter1 Register
PRS_C0_INPUT_PARA2_REG	0x0038	Parser Channel_0 Input Parameter2 Register
PRS_C0_INPUT_PARA3_REG	0x003C	Parser Channel_0 Input Parameter3 Register
PRS_C0_INT_EN_REG	0x0040	Parser Channel_0 Interrupt Enable Register
PRS_C0_INT_STA_REG	0x0044	Parser Channel_0 Interrupt Status Register
PRS_CH0_LINE_TIME_REG	0x0048	Parser Channel_0 Line Time Register
/	0x004C~0x0120	Reserved
PRS_C1_INFMT_REG	0x0124	Parser Channel_1 Input Format Register
PRS_C1_OUTPUT_HSIZE_REG	0x0128	Parser Channel_1 Output Horizontal Size Register
PRS_C1_OUTPUT_VSIZE_REG	0x012C	Parser Channel_1 Output Vertical Size Register
PRS_C1_INPUT_PARA0_REG	0x0130	Parser Channel_1 Input Parameter0 Register
PRS_C1_INPUT_PARA1_REG	0x0134	Parser Channel_1 Input Parameter1 Register
PRS_C1_INPUT_PARA2_REG	0x0138	Parser Channel_1 Input Parameter2 Register
PRS_C1_INPUT_PARA3_REG	0x013C	Parser Channel_1 Input Parameter3 Register
PRS_C1_INT_EN_REG	0x0140	Parser Channel_1 Interrupt Enable Register
PRS_C1_INT_STA_REG	0x0144	Parser Channel_1 Interrupt Status Register
PRS_CH1_LINE_TIME_REG	0x0148	Parser Channel_1 Line Time Register
/	0x014C~0x0220	Reserved
PRS_C2_INFMT_REG	0x0224	Parser Channel_2 Input Format Register
PRS_C2_OUTPUT_HSIZE_REG	0x0228	Parser Channel_2 Output Horizontal Size Register
PRS_C2_OUTPUT_VSIZE_REG	0x022C	Parser Channel_2 Output Vertical Size Register
PRS_C2_INPUT_PARA0_REG	0x0230	Parser Channel_2 Input Parameter0 Register
PRS_C2_INPUT_PARA1_REG	0x0234	Parser Channel_2 Input Parameter1 Register
PRS_C2_INPUT_PARA2_REG	0x0238	Parser Channel_2 Input Parameter2 Register
PRS_C2_INPUT_PARA3_REG	0x023C	Parser Channel_2 Input Parameter3 Register
PRS_C2_INT_EN_REG	0x0240	Parser Channel_2 Interrupt Enable Register
PRS_C2_INT_STA_REG	0x0244	Parser Channel_2 Interrupt Status Register
PRS_CH2_LINE_TIME_REG	0x0248	Parser Channel_2 Line Time Register
/	0x024C~0x0320	Reserved
PRS_C3_INFMT_REG	0x0324	Parser Channel_3 Input Format Register
PRS_C3_OUTPUT_HSIZE_REG	0x0328	Parser Channel_3 Output Horizontal Size Register
PRS_C3_OUTPUT_VSIZE_REG	0x032C	Parser Channel_3 Output Vertical Size Register

PRS_C3_INPUT_PARA0_REG	0x0330	Parser Channel_3 Input Parameter0 Register
PRS_C3_INPUT_PARA1_REG	0x0334	Parser Channel_3 Input Parameter1 Register
PRS_C3_INPUT_PARA2_REG	0x0338	Parser Channel_3 Input Parameter2 Register
PRS_C3_INPUT_PARA3_REG	0x033C	Parser Channel_3 Input Parameter3 Register
PRS_C3_INT_EN_REG	0x0340	Parser Channel_3 Interrupt Enable Register
PRS_C3_INT_STA_REG	0x0344	Parser Channel_3 Interrupt Status Register
PRS_CH3_LINE_TIME_REG	0x0348	Parser Channel_3 Line Time Register
/	0x0348~0x04FC	Reserved
PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG	0x0500	Parser NCSIC RX Signal0 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL1_DLY_ADJ_REG	0x0504	Parser NCSIC RX Signal1 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL2_DLY_ADJ_REG	0x0508	Parser NCSIC RX Signal2 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG	0x050C	Parser NCSIC RX Signal3 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG	0x0510	Parser NCSIC RX Signal4 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG	0x0514	Parser NCSIC RX Signal5 Delay Adjust Register
PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG	0x0518	Parser NCSIC RX Signal6 Delay Adjust Register
PRS_NCSIC_SYNC_EN_REG	0x0520	Parser NCSIC SYNC Enable Register
PRS_NCSIC_SYNC_CFG_REG	0x0524	Parser NCSIC SYNC CFG Register
PRS_NCSIC_SYNC_WAIT_N_REG	0x0528	Parser NCSIC SYNC WAIT N Register
PRS_NCSIC_SYNC_WAIT_M_REG	0x052C	Parser NCSIC SYNC WAIT M Register

DMA0/1/2/3 register list:

CSIC_DMA_EN_REG	0x0000	CSIC DMA Enable Register
CSIC_DMA_CFG_REG	0x0004	CSIC DMA Configuration Register
/	0x0008	Reserved
/	0x000C	Reserved
CSIC_DMA_HSIZE_REG	0x0010	CSIC DMA Horizontal Size Register
CSIC_DMA_VSIZE_REG	0x0014	CSIC DMA Vertical Size Register
/	0x0018	Reserved
/	0x001C	Reserved
CSIC_DMA_F0_BUFA_REG	0x0020	CSIC DMA FIFO 0 Output Buffer-A Address Register
CSIC_DMA_F0_BUFA_RESULT_REG	0x0024	CSIC DMA FIFO 0 Output Buffer-A Address Result Register
CSIC_DMA_F1_BUFA_REG	0x0028	CSIC DMA FIFO 1 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x002C	CSIC DMA FIFO 1 Output Buffer-A Address Result Register
CSIC_DMA_F2_BUFA_REG	0x0030	CSIC DMA FIFO 2 Output Buffer-A Address Register
CSIC_DMA_F1_BUFA_RESULT_REG	0x0034	CSIC DMA FIFO 2 Output Buffer-A Address Result Register
CSIC_DMA_BUF_LEN_REG	0x0038	CSIC DMA Buffer Length Register
CSIC_DMA_FLIP_SIZE_REG	0x003C	CSIC DMA Flip Size Register
CSIC_DMA_VI_TO_TH0_REG	0x0040	CSIC DMA Video Input Timeout Threshold0 Register
CSIC_DMA_VI_TO_TH1_REG	0x0044	CSIC DMA Video Input Timeout Threshold1 Register
CSIC_DMA_VI_TO_CNT_VAL_REG	0x0048	CSIC DMA Video Input Timeout Counter Value Register

CSIC_DMA_CAP_STA_REG	0x004C	CSIC DMA Capture Status Register
CSIC_DMA_INT_EN_REG	0x0050	CSIC DMA Interrupt Enable Register
CSIC_DMA_INT_STA_REG	0x0054	CSIC DMA Interrupt Status Register
CSIC_DMA_LINE_CNT_REG	0x0058	CSIC DMA LINE COUNTER Register
CSIC_DMA_FRM_CNT_REG	0x005C	CSIC DMA Frame Counter Register
CSIC_DMA_FRM_CLK_CNT_REG	0x0060	CSIC DMA Frame Clock Counter Register
CSIC_DMA_ACC_ITNL_CLK_CNT_REG	0x0064	CSIC DMA Accumulated And Internal Clock Counter Register
CSIC_DMA_FIFO_STAT_REG	0x0068	CSIC DMA FIFO Statistic Register
CSIC_DMA_FIFO_THRS_REG	0x006C	CSIC DMA FIFO Threshold Register
CSIC_DMA_PCLK_STAT_REG	0x0070	CSIC DMA PCLK Statistic Register
CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG	0x0080	CSIC DMA BUF Address FIFO0 Entry Register
CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG	0x0084	CSIC DMA BUF Address FIFO1 Entry Register
CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG	0x0088	CSIC DMA BUF Address FIFO2 Entry Register
CSIC_DMA_BUF_TH_REG	0x008C	CSIC DMA BUF Threshold Register
CSIC_DMA_BUF_ADDR_FIFO_CON_REG	0x0090	CSIC DMA BUF Address FIFO Content Register
CSIC_DMA_STORED_FRM_CNT_REG	0x0094	CSIC DMA Stored Frame Counter Register
CSIC_LBC_CONFIG_REG	0x0100	CSIC LBC Configure Register
CSIC_LBC_LINE_TAR_BIT0_REG	0x0104	CSIC LBC Line Target Bit0 Register
CSIC_LBC_LINE_TAR_BIT1_REG	0x0108	CSIC LBC Line Target Bit1 Register
CSIC_LBC_RC_ADV_REG	0x010C	CSIC LBC RC ADV Register
CSIC_LBC_MB_MIN_REG	0x0110	CSIC LBC MB MIN Register
CSIC_FEATURE_REG	0x01F4	CSIC DMA Feature List Register

8.1.5. CCU Register Description

8.1.5.1. 0x0000 CCU Clock Mode Register(Default Value:0x8000_0000)

Offset: 0x0000			Register Name: CCU_CLK_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	CCU_CLK_GATING_DISABLE 0:CCU Clock Gating Registers(0x0004~0x0010) effect 1:CCU Clock Gating Registers(0x0004~0x0010) not effect
30:18	/	/	/
17	R/W	0x0	MIPI_TX_CLK invert
16	R/W	0x0	MIPI_TX_CLK enable
15:5	/	/	/
4	R/W	0x0	MISP_CLK_MODE 0: ISP core clock uses isp_clk2x when there is only 1 isp core working 1: ISP core clock uses isp_clk1x when there is 2 isp core working
3:2	/	/	/
1	R/W	0x0	MCSI_POST_CLK_MODE 0: CSI Post works in isp core clock

			1: CSI Post works in csi clock
0	R/W	0x0	MCSI_PARSER_CLK_MODE 0: CSI Parser works in isp core clock 1: CSI Parser works in csi clock

8.1.5.2. 0x0004 CCU Parser Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CCU_PARSER_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MCSI_MIPI0_CLK_ENABLE 0: MIPI0 clock disable 1: MIPI0 clock enable
15:2	/	/	/
1	R/W	0x0	MCSI_PARSER1_CLK_ENABLE 0: CSI Parser1 clock disable 1: CSI Parser1 clock enable
0	R/W	0x0	MCSI_PARSER0_CLK_ENABLE 0: CSI Parser0 clock disable 1: CSI Parser0 clock enable

8.1.5.3. 0x0008 CCU ISP Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: CCU_ISP_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	MISP0_BRIDGE_CLK_ENABLE 0: ISP0 bridge clock disable 1: ISP0 bridge clock enable
3:1	/	/	/
0	R/W	0x0	MISP0_CLK_ENABLE 0: ISP0 clock disable 1: ISP0 clock enable

8.1.5.4. 0x000C CCU Post0 Clock Enable Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: CCU_POST0_CLK_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	MCSI_POST0_CLK_ENABLE 0: POST0 clock disable

			1: POST0 clock enable
15:12	/	/	/
11	R/W	0x0	MCSI_VIPP3_CLK_ENABLE 0: VIPP3 clock disable 1: VIPP3 clock enable,when MCSI_POST0_CLK_ENABLE is 1
10	R/W	0x0	MCSI_VIPP2_CLK_ENABLE 0: VIPP2 clock disable 1: VIPP2 clock enable,when MCSI_POST0_CLK_ENABLE is 1
9	R/W	0x0	MCSI_VIPP1_CLK_ENABLE 0:VIPP1 clock disable 1: VIPP1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
8	R/W	0x0	MCSI_VIPP0_CLK_ENABLE 0: VIPP0 clock disable 1: VIPP0 clock enable,when MCSI_POST0_CLK_ENABLE is 1
7:4	/	/	/
3	R/W	0x0	MCSI_BK3_CLK_ENABLE 0: BK3 clock disable 1: BK3 clock enable,when MCSI_POST0_CLK_ENABLE is 1
2	R/W	0x0	MCSI_BK2_CLK_ENABLE 0: BK2 clock disable 1: BK2 clock enable,when MCSI_POST0_CLK_ENABLE is 1
1	R/W	0x0	MCSI_BK1_CLK_ENABLE 0: BK1 clock disable 1: BK1 clock enable,when MCSI_POST0_CLK_ENABLE is 1
0	R/W	0x0	MCSI_BK0_CLK_ENABLE 0: BK0 clock disable 1: BK0 clock enable,when MCSI_POST0_CLK_ENABLE is 1

8.1.6. CSIC Top Register Description

8.1.6.1. 0x0000 CSIC TOP Enable Register(Default Value:0x0000_0000)

Offset: 0x0000			**Register Name: CSIC_TOP_EN_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN CSIC Version Register Read Enable 0: Disable 1: Enable
30:7	/	/	/
6:4	R/W	0x0	MCSI_TX_SEL 000:CSI TX from VIPP0 output 001:CSI TX from VIPP1 output 010:CSI TX from VIPP2 output

			011:CSI TX from VIPP3 output Others: Reserved
3	R/W	0x0	ISP_BRIDGE_EN Enable Async Bridge from parser to isp and isp to post, when isp uses different clock source from csi_top_clk 0: disable 1: enable
2	R/W	0x0	BIST_MODE_EN 0: Closed 1: EN BIST TEST
1	R/W	0x0	MCSI_TX_EN 0: Closed 1:EN CSI TX output
0	R/W	0x0	CSIC_TOP_EN 0: Reset and disable the CSIC module 1: Enable the CSIC module

8.1.6.2. 0x0008 CSIC Pattern Control Register(Default Value:0x0000_000F)

Offset: 0x0008			**Register Name: CSIC_PTN_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	PTN_PORT_SEL Pattern Generator output port selection 000:MCSIC0 010:NCSIC0 Others: Reserved
23:22	/	/	/
21:20	R/W	0x0	PTN_GEN_DATA_WIDTH 00:8bit 01:10bit 10:12bit 11:Reserved
19:16	R/W	0x0	PTN_MODE Pattern mode selection 0000~0011:reserved 0100:NCSIC YUV 8 bits width 0101:NCSIC YUV 16 bits width 0110:reserved 0111:reserved 1000:BT656 8 bits width 1001:BT656 16 bits width 1010:reserved 1011:reserved

			1100:BAYER 12 bits for ISPFE 1101:UYVY422 12 bits for ISPFE 1110:UYVY420 12 bits for ISPFE 1111:reserved
15:10	/	/	/
9:8	R/W	0x0	PTN_GEN_CLK_DIV Packet generator clock divider
7:0	R/W	0xF	PTN_GEN_DLY Clocks delayed before pattern generating start.

8.1.6.3. 0x0020 CSIC Pattern Generation Length Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_PTN_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

8.1.6.4. 0x0024 CSIC Pattern Generation Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_PTN_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

8.1.6.5. 0x0028 CSIC Pattern ISP Size Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_PTN_ISP_SIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	Height Vertical size,only valid for ISP mode pattern generation.
15:13	/	/	/
12:0	R/W	0x0	Width Horizontal size,only valid for ISP mode pattern generation.

8.1.6.6. 0x0030 CSIC ISP0 Input0 Select Register(Default Value:0x0000_0000)

Offset :0x0030			Register Name: CSIC_ISP0_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3:0	R/W	0x0	ISP0 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.7. 0x0034 CSIC ISP0 Input1 Select Register(Default Value:0x0000_0001)

Offset :0x0034			Register Name: CSIC_ISP0_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x1	ISP0 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.8. 0x0038 CSIC ISP0 Input2 Select Register(Default Value:0x0000_0002)

Offset :0x0038			Register Name: CSIC_ISP0_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x2	ISP0 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.9. 0x003C CSIC ISP0 Input3 Select Register(Default Value:0x0000_0003)

Offset :0x003C			Register Name: CSIC_ISP0_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	ISP0 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.10. 0x0040 CSIC ISP1 Input0 Select Register(Default Value:0x0000_0004)

Offset :0x0040			Register Name: CSIC_ISP1_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x4	ISP1 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.11. 0x0044 CSIC ISP1 Input1 Select Register(Default Value:0x0000_0005)

Offset :0x0044			Register Name: CSIC_ISP1_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x5	ISP1 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0

			0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.12. 0x0048 CSIC ISP1 Input2 Select Register(Default Value:0x0000_0006)

Offset :0x0048			Register Name: CSIC_ISP1_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x6	ISP1 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.13. 0x004C CSIC ISP1 Input3 Select Register(Default Value:0x0000_0007)

Offset :0x004C			Register Name: CSIC_ISP1_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x7	ISP1 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.14. 0x0050 CSIC ISP2 Input0 Select Register(Default Value:0x0000_0008)

Offset :0x0050			Register Name: CSIC_ISP2_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

3:0	R/W	0x8	ISP2 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.15. 0x0054 CSIC ISP2 Input1 Select Register(Default Value:0x0000_0009)

Offset :0x0054			Register Name: CSIC_ISP2_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x9	ISP2 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.16. 0x0058 CSIC ISP2 Input2 Select Register(Default Value:0x0000_000A)

Offset :0x0058			Register Name: CSIC_ISP2_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xA	ISP2 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.17. 0x005C CSIC ISP2 Input3 Select Register(Default Value:0x0000_000B)

Offset :0x005C			Register Name: CSIC_ISP2_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xB	ISP2 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.18. 0x0060 CSIC ISP3 Input0 Select Register(Default Value:0x0000_000C)

Offset :0x0060			Register Name: CSIC_ISP3_INPUT0_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xC	ISP3 Input0 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.19. 0x0064 CSIC ISP3 Input1 Select Register(Default Value:0x0000_000D)

Offset :0x0064			Register Name: CSIC_ISP3_INPUT1_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xD	ISP3 Input1 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0

			0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.20. 0x0068 CSIC ISP3 Input2 Select Register(Default Value:0x0000_000E)

Offset :0x0068			Register Name: CSIC_ISP3_INPUT2_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xE	ISP3 Input2 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.21. 0x006C CSIC ISP3 Input3 Select Register(Default Value:0x0000_000F)

Offset :0x006C			Register Name: CSIC_ISP3_INPUT3_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0xF	ISP3 Input3 Select 0000: input from Parser0 CH0 0001: input from Parser0 CH1 0010: input from Parser0 CH2 0011: input from Parser0 CH3 0100: input from Parser1 CH0 0101: input from Parser1 CH1 0110: input from Parser1 CH2 0111: input from Parser1 CH3 Others: Reserved

8.1.6.22. 0x0070 CSIC ISP Bridge Buffer Maxuse Counter Clear Register(Default Value:0x0000_0000)

Offset :0x0070			Register Name: CSIC_ISP_BRG_BUF_MAXUSE_CNT_CLR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

1	R/W	0x0	ISP0_BRG1_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear
0	R/W	0x0	ISP0_BRG0_BUF_MAXUSE_CNT_CLR 0: no effect 1: clear

8.1.6.23. 0x0074 CSIC ISP0 Bridge Buffer Maxuse Counter Register(Default Value:0x0000_0000)

Offset :0x0074			Register Name: CSIC_ISP0_BRG_BUF_MAXUSE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	ISP0_BRG1_BUF_MAXUSE_CNT
15:0	RO	0x0	ISP0_BRG0_BUF_MAXUSE_CNT

8.1.6.24. 0x0084 CSIC ISP0 Bridge Interrupt Enable Register(Default Value:0x0000_0000)

Offset :0x0084			Register Name: CSIC_ISP0_BRG_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25	R/W	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:18	/	/	/
17	R/W	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_EN Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:10	/	/	/
9	R/W	0x0	ISP0_BRG1_BUF_OV_INT_EN ISP0 Bridge1 Buffer overflow interrupt enable
8	R/W	0x0	ISP0_BRG0_BUF_OV_INT_EN ISP0 Bridge0 Buffer overflow interrupt enable
7:2	/	/	/
1	R/W	0x0	ISP0_BRG1_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable
0	R/W	0x0	ISP0_BRG0_RS_INT_EN ISP0 Bridge0 Read clock too slow interrupt enable

8.1.6.25. 0x008C CSIC ISP0 Bridge Interrupt Pending Register(Default Value:0x0000_0000)

Offset :0x008C			Register Name: CSIC_ISP0_BRG_INT_PD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25	R/W1C	0x0	ISP0_BRG1_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Slow to Fast Side
24	R/W1C	0x0	ISP0_BRG0_S2F_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Slow to Fast Side
23:18	/	/	/
17	R/W1C	0x0	ISP0_BRG1_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge1 Fast to Slow Side
16	R/W1C	0x0	ISP0_BRG0_F2S_LW_MISMTCH_INT_PD Picture Line Width Mismatch detect in ISP0 Bridge0 Fast to Slow Side
15:10	/	/	/
9	R/W1C	0x0	ISP0_BRG1_BUF_OV_INT_PD ISP0 Bridge1 Buffer overflow interrupt pending
8	R/W1C	0x0	ISP0_BRG0_BUF_OV_INT_PD ISP0 Bridge0 Buffer overflow interrupt pending
7:2	/	/	/
1	R/W1C	0x0	ISP0_BRG1_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending
0	R/W1C	0x0	ISP0_BRG0_RS_INT_PD ISP0 Bridge0 Read clock too slow interrupt pending

8.1.6.26. 0x00A0 CSIC DMA0 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A0			Register Name: CSIC_DMA0_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA0 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.27. 0x00A4 CSIC DMA1 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A4			Register Name: CSIC_DMA1_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA1 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.28. 0x00A8 CSIC DMA2 Input Select Register(Default Value:0x0000_0000)

Offset :0x00A8			Register Name: CSIC_DMA2_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA2 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0 0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.29. 0x00AC CSIC DMA3 Input Select Register(Default Value:0x0000_0000)

Offset :0x00AC			Register Name: CSIC_DMA3_INPUT_SEL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	DMA3 Input Select 0000: input from ISP0 CH0 0001: input from ISP0 CH1 0010: input from ISP0 CH2 0011: input from ISP0 CH3 0100: input from ISP1 CH0

			0101: input from ISP1 CH1 0110: input from ISP1 CH2 0111: input from ISP1 CH3 Others: Reserved

8.1.6.30. 0x00DC CSIC BIST CS Register(Default Value:0x0000_0000)

Offset :0x00DC			Register Name: CSIC_BIST_CS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	BIST_CS 000: Set when BK0 or ISP0_BRIDGE0 memory bist 001: Set when BK1 or ISP0_BRIDGE1 memory bist 010: Set when BK2 or ISP0_BRIDGE2 memory bist 011: Set when BK3 or ISP0_BRIDGE3 memory bist 100: Set when BK4 or ISP1_BRIDGE0 memory bist 101: Set when BK5 or ISP1_BRIDGE1 memory bist Others: Reserved

8.1.6.31. 0x00E0 CSIC BIST Control Register(Default Value:0x0000_0200)

Offset :0x00E0			Register Name: CSIC_BIST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	BIST_ERR_STA BIST Error Status 0:NO effect 1:Error
14:12	R	0x0	BIST_ERR_PAT BIST Error Pattern
11:10	R	0x0	BIST_ERR_CYC BIST Error Cycle
9	R	0x1	BIST_STOP BIST STOP 0:running 1:STOP
8	R	0x0	BIST_BUSY BIST Busy 0:idle 1:busy
7:5	R/W	0x0	BIST_REG_SEL BIST REG select

4	R/W	0x0	BIST_ADDR_Mode_SEL BIST Address mode select
3:1	R/W	0x0	BIST_WDATA_PAT BIST Write data Pattern 000:0x00000000 001:0x55555555 010:0x33333333 011:0x0F0F0F0F 100:0x00FF00FF 101:0x0000FFFF others: reserved
0	R/W	0x0	BIST_EN BIST Enable.A positive will trigger the BIST to start.

8.1.6.32. 0x00E4 CSIC BIST Start Address Register(Default Value:0x0000_0000)

Offset :0x00E4			Register Name: CSIC_BIST_START_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST Start Address BIST Start Address.It is 32-bit aligned.

8.1.6.33. 0x00E8 CSIC BIST End Address Register(Default Value:0x0000_0000)

Offset :0x00E8			Register Name: CSIC_BIST_END_ADDR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST END Address BIST END Address.It is 32-bit aligned.

8.1.6.34. 0x00EC CSIC BIST Data Mask Register(Default Value:0x0000_0000)

Offset :0x00EC			Register Name: CSIC_BIST_DATA_MASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	BIST_DATA_MASK BIST Data Mask 0:Unmask 1:Mask

8.1.6.35. 0x00F0 CSIC MBUS REQ MAX Register(Default Value:0x0000_0000)

Offset: 0x00F0	Register Name: CSIC_MBUS_REQ_MAX_REG

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x00	MISP_MEM_REQ_MAX
15:13	/	/	/
12:8	R/W	0x00	MCSI_MEM_1_REQ_MAX
7:5	/	/	/
4:0	R/W	0x00	MCSI_MEM_REQ_MAX Maxnum of request commands for the master granted in MCSI_MEM arbiter is N+1. Recommended value is 0xF.

8.1.6.36. 0x0100 CSIC Multi-Frame Mode Register(Default Value:0x0000_0000)

Offset: 0x0100			Register Name: CSIC_MULF_MOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	MULF_STATUS
23:16	/	/	/
15:8	R/W	0x0	MULF_CS
7:1	/	/	/
0	R/W	0x0	MULF_EN

8.1.6.37. 0x0104 CSIC Multi-Frame Interrupt Register (Default Value:0x0000_0000)

Offset: 0x0104			Register Name: CSIC_MULF_INT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	MULF_ERR_PD
16	R/W1C	0x0	MULF_DONE_PD
15:2	/	/	/
1	R/W	0x0	MULF_ERR_EN
0	R/W	0x0	MULF_DONE_EN

8.1.6.38. 0x01F0 CSIC Feature List Register(Default Value:0x2111_4400)

Offset: 0x01F0			Register Name: CSIC_FEATURE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R	0x2	VER_SMALL_PARSER_NUM Only can be read when version register read enable is on.
27:24	R	0x1	VER_SMALL_MCSI_NUM Only can be read when version register read enable is on.
23:20	R	0x1	VER_SMALL_NCSI_NUM Only can be read when version register read enable is on.

19:16	R	0x1	VER_SMALL_ISP_NUM Only can be read when version register read enable is on.
15:12	R	0x4	VER_SMALL_VIPP_NUM Only can be read when version register read enable is on.
11:8	R	0x4	VER_SMALL_DMA_NUM Only can be read when version register read enable is on.
7:0	/	/	/

8.1.7. Parser Register Description

8.1.7.1. 0x0000 Parser Enable Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: PRS_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MCSIC_EN 0: Reset and disable the MCSIC module 1: Enable the MCSIC module
30:17	/	/	/
16	R/W	0x0	NCSIC_EN 0: Reset and disable the NCSIC module 1: Enable the NCSIC module
15	R/W	0x0	PCLK_EN 0:Gate pclk input 1:Enable pclk input
14:3	/	/	/
2	R/W	0x0	PRS_CH_MODE 0: Parser output channel 0~3 corresponding from input channel 0~3 1: Parser output channel 0~3 all from input channel 0(MIPI SEHDR)
1	R/W	0x0	PRS_MODE 0: NCSI 1: MCSI
0	R/W	0x0	PRS_EN 0: Reset and disable the parser module 1: Enable the parser module

8.1.7.2. 0x0004 Parser NCSIC Interface Configuration Register(Default Value:0x0105_0080)

Offset: 0x0004			Register Name: PRS_NCSIC_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order

30:28	/	/	/
27:24	R/W	0x1	FIELD_DT_PCLK_SHIFT Only for vsync detected field mode, the odd field permitted pclk shift = 4* FIELD_DT_PCLK_SHIFT
23:22	/	/	/
21	R/W	0x0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	/	/	/
19	R/W	0x0	FIELD For YUV HV timing, Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) For BT656 timing, Field sequence 0: Normal sequence (field 0 first) 1: Inverse sequence (field 1 first)
18	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
17	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not apply to CCIR656 interface.
16	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge
15:14	R/W	0x0	Field_DT_MODE(only valid when CSI_IF is YUV and source type is interlaced) 00:by both field and vsync 01:by field 10:by vsync 11:reserved
13	R/W	0x0	DDR_SAMPLE_ MODE_EN 0:disable 1:enable
12:11	R/W	0x0	SEQ_8PLUS2 When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual CSI data bus according to these sequences: 00: 6'bx+D[9:8], D[7:0] 01: D[9:2], 6'bx+D[1:0]

			10: D[7:0], D[9:8]+6'bx 11: D[7:0], 6'bx+D[9:8]
10:8	R/W	0x0	IF_DATA_WIDTH 000: 8 bit data bus 001: 10 bit data bus 010: 12 bit data bus 011: 8+2bit data bus 100: 2x8bit data bus Others: Reserved
7:6	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	R/W	0x0	CSI_IF YUV(separate syncs): 00000: YUYV422 Interleaved or RAW (All data in one data bus) 00001: 16 bit YUYV422 Interleaved 00010: Reserved 00011: Reserved CCIR656(embedded syncs): 00100: BT656 1 channel 00101: 16bit BT656(BT1120 like) 1 channel 00110: Reserved 00111: Reserved 01100: BT656 2 channels (All data interleaved in one data bus) 01101: 16bit BT656(BT1120 like) 2 channels(All data interleaved in one data bus) 01110: BT656 4 channels (All data interleaved in one data bus) 01111:16bit BT656(BT1120 like) 4 channels(All data interleaved in one data bus) Others: Reserved

8.1.7.3. 0x0008 Parser MCSIC Interface Configuration Register(Default Value:0x0000_0080)

Offset: 0x0008			Register Name: PRS_MCSI_IF_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	YUV420_LINE_ORDER 0: YUV420 input in Y-YC-Y-YC Line Order 1: YUV420 input in YC-Y-YC-Y Line Order
30:8	/	/	/
7:6	R/W	0X2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
5	R/W	0x0	OUTPUT_MODE 0:field mode 1:frame mode
4:0	/	/	/

8.1.7.4. 0x000C Parser Capture Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: PRS_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:26	R/W	0x0	CH3_CAP_MASK Vsync number masked before capture.
25	R/W	0x0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	RC/W	0x0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture 1: Enable still capture

			The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
13:12	/	/	/
21:18	R/W	0x0	CH2_CAP_MASK Vsync number masked before capture.
17	R/W	0x0	CH2_VCAP_ON Video capture control: Capture the video image data stream on channel 2. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
16	RC/W	0x0	CH2_SCAP_ON Still capture control: Capture a single still image frame on channel 2. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
15:14	/	/	/
13:10	R/W	0x0	CH1_CAP_MASK Vsync number masked before capture.
9	R/W	0x0	CH1_VCAP_ON Video capture control: Capture the video image data stream on channel 1. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
8	RC/W	0x0	CH1_SCAP_ON Still capture control: Capture a single still image frame on channel 1. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.
7:6	/	/	/
5:2	R/W	0x0	CH0_CAP_MASK Vsync number masked before capture.
1	R/W	0x0	CH0_VCAP_ON Video capture control: Capture the video image data stream on channel 0. 0: Disable video capture

			If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	RC/W	0x0	CH0_SCAP_ON Still capture control: Capture a single still image frame on channel 0. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

8.1.7.5. 0x0010 Parser Signal Status Register(Default Value:0x0000_0000)

Offset: 0x0010			Register Name: PRS_SIGNAL_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R	0x0	PCLK_STA Indicates the pclk status 0:low 1:high
23:0	R	0x0	DATA_STA Indicates the Dn status(n=0~23),MSB for D23,LSB for D0 0:low 1:high

8.1.7.6. 0x0014 Parser NCSIC BT656 Header Configuration Register (Default Value:0x0302_0100)

Offset: 0x0014			Register Name: PRS_NCSIC_BT656_HEAD_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x3	CH3_ID The low 4bit of BT656 header for channel 3 Only valid in BT656 multi-channel mode
23:20	/	/	/
19:16	R/W	0x2	CH2_ID The low 4bit of BT656 header for channel 2 Only valid in BT656 multi-channel mode
15:12	/	/	/
11:8	R/W	0x1	CH1_ID The low 4bit of BT656 header for channel 1

			Only valid in BT656 multi-channel mode
7:4	/	/	/
3:0	R/W	0x0	CH0_ID The low 4bit of BT656 header for channel 0 Only valid in BT656 multi-channel mode

8.1.7.7. 0x0024 Parser Channel_0 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0024			Register Name: PRS_CH0_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.8. 0x0028 Parser Channel_0 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0028			Register Name: PRS_CH0_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.9. 0x002C Parser Channel_0 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x002C			Register Name: PRS_CH0_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.10. 0x003C Parser Channel_0 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: PRS_CH0_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.11. 0x0034 Parser Channel_0 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0034			Register Name: PRS_CH0_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.12. 0x0038 Parser Channel_0 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0038			Register Name: PRS_CH0_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.13. 0x003C Parser Channel_0 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x003C			Register Name: PRS_CH0_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.14. 0x0040 Parser Channel_0 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0040			Register Name: PRS_CH0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.15. 0x0044 Parser Channel_0 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: PRS_CH0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

8.1.7.16. 0x0048 Parser Channel_0 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0048			Register Name: PRS_CH0_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH0_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH0_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.17. 0x0124 Parser Channel_1 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0124			Register Name: PRS_CH1_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.18. 0x0128 Parser Channel_1 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0128			Register Name: PRS_CH1_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.19. 0x012C Parser Channel_1 Output Vertical Size Register(Default Value:0x02d0_0000)

Offset: 0x012C			Register Name: PRS_CH1_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.20. 0x0130 Parser Channel_1 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0130			Register Name: PRS_CH1_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/

0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.21. 0x0134 Parser Channel_1 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0134			Register Name: PRS_CH1_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.22. 0x0138 Parser Channel_1 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0138			Register Name: PRS_CH1_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.23. 0x013C Parser Channel_1 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x013C			Register Name: PRS_CH1_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.24. 0x0140 Parser Channel_1 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0140			Register Name: PRS_CH1_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error

			Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.25. 0x0144 Parser Channel_1 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0144			Register Name: PRS_CH1_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.26. 0x0148 Parser Channel_1 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0148			Register Name: PRS_CH1_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH1_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH1_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.27. 0x0224 Parser Channel_2 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0224			Register Name: PRS_CH2_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved

			0011: YUV422 0100: YUV420 Others: reserved

8.1.7.28. 0x0228 Parser Channel_2 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0228			Register Name: PRS_CH2_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.29. 0x022C Parser Channel_2 Output Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x022C			Register Name: PRS_CH2_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.30. 0x0230 Parser Channel_2 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0230			Register Name: PRS_CH2_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.31. 0x0234 Parser Channel_2 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0234			Register Name: PRS_CH2_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/

29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.32. 0x0238 Parser Channel_2 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0238			Register Name: PRS_CH2_INPUT_PARA2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.33. 0x023C Parser Channel_2 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x023C			Register Name: PRS_CH2_INPUT_PARA3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.34. 0x0240 Parser Channel_2 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0240			Register Name: PRS_CH2_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.35. 0x0244 Parser Channel_2 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0244			Register Name: PRS_CH2_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1 When the parser input parameter0 register update,this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register,parser input parameter2 register or parser input parameter3 register update,this flag set to 1. Write 1 to clear.

8.1.7.36. 0x0248 Parser Channel_2 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0248			Register Name: PRS_CH2_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH2_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH2_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.37. 0x0324 Parser Channel_3 Input Format Register(Default Value:0x0000_0003)

Offset: 0x0324			Register Name: PRS_CH3_INFMT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	INPUT_FMT Input data format 0000: RAW stream 0001: reserved 0010: reserved 0011: YUV422 0100: YUV420 Others: reserved

8.1.7.38. 0x0328 Parser Channel_3 Output Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0328			Register Name: PRS_CH3_OUTPUT_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel unit length. Valid pixel of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.7.39. 0x032C Parser Channel_3 Output Vertical Size Register(Default Value:0x02d0_0000)

Offset: 0x032C			Register Name: PRS_CH3_OUTPUT_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

8.1.7.40. 0x0330 Parser Channel_3 Input Parameter0 Register(Default Value:0x0000_0000)

Offset: 0x0330			Register Name: PRS_CH3_INPUT_PARA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R	0x0	INPUT_SRC_TYPE 0:Progress 1:Interlace

8.1.7.41. Parser Channel_3 Input Parameter1 Register(Default Value:0x0000_0000)

Offset: 0x0334			Register Name: PRS_CH3_INPUT_PARA1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R	0x0	INPUT_VT INPUT_VT = INPUT_VB+INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_HT INPUT_HT = INPUT_HB+INPUT_X

8.1.7.42. 0x0338 Parser Channel_3 Input Parameter2 Register(Default Value:0x0000_0000)

Offset: 0x0338			Register Name: PRS_CH3_INPUT_PARA2_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_VB
15:14	/	/	/
13:0	R	0x0	INPUT_HB

8.1.7.43. 0x033C Parser Channel_3 Input Parameter3 Register(Default Value:0x0000_0000)

Offset: 0x033C			Register Name: PRS_CH3_INPUT_PARA3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	INPUT_Y
15:14	/	/	/
13:0	R	0x0	INPUT_X

8.1.7.44. 0x0340 Parser Channel_3 Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0340			Register Name: PRS_CH3_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	MUL_ERR_INT_EN Multi-channel writing error Indicates error has been detected for writing data to a wrong channel.
1	R/W	0x0	INPUT_PARA1_INT_EN 0:disable 1:enable
0	R/W	0x0	INPUT_PARA0_INT_EN 0:disable 1:enable

8.1.7.45. 0x0344 Parser Channel_3 Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0344			Register Name: PRS_CH3_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W1C	0x0	MUL_ ERR_PD Multi-channel writing error
1	R/W1C	0x0	INPUT_SRC_PD1

			When the parser input parameter0 register update, this flag set to 1. Write 1 to clear.
0	R/W1C	0x0	INPUT_SRC_PD0 When the parser input parameter1 register, parser input parameter2 register or parser input parameter3 register update, this flag set to 1. Write 1 to clear.

8.1.7.46. 0x0348 Parser Channel_3 Line Time Register(Default Value:0x0000_0000)

Offset: 0x0348			Register Name: PRS_CH3_LINE_TIME_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	RO	0x0	PRS_CH3_HBLK_TIME Time of H Blanking when vsync valid, unit is csi_top_clk cycle
15:0	RO	0x0	PRS_CH3_HSYN_TIME Time of H SYNC when vsync valid, unit is csi_top_clk cycle

8.1.7.47. 0x0500 Parser NCSIC RX Signal0 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0500			Register Name: PRS_NCSIC_RX_SIGNAL0_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	Filed_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	Vsync_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	Hsync_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	Pclk_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.48. 0x0504 Parser NCSIC RX Signal1 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0504			Register Name: PRS_NCSIC_RX_SIGNAL1_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D23_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/

20:16	R/W	0x0	D22_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D21_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D20_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.49. 0x0508 Parser NCSIC RX Signal2 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0508			Register Name: PRS_NCSIC_RX_SIGNAL2_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D19_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D18_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D17_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D16_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.50. 0x050C Parser NCSIC RX Signal3 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x050C			Register Name: PRS_NCSIC_RX_SIGNAL3_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D15_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D14_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D13_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D12_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.51. 0x0510 Parser NCSIC RX Signal4 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0510			Register Name: PRS_NCSIC_RX_SIGNAL4_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D11_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D10_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D9_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D8_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.52. 0x0514 Parser NCSIC RX Signal5 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0514			Register Name: PRS_NCSIC_RX_SIGNAL5_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D7_dly 32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D6_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D5_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D4_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.53. 0x0518 Parser NCSIC RX Signal6 Delay Adjust Register(Default Value:0x0000_0000)

Offset: 0x0518			Register Name: PRS_NCSIC_RX_SIGNAL6_DLY_ADJ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x0	D3_dly

			32 Step for adjust, 1 step = 0.2ns
23:21	/	/	/
20:16	R/W	0x0	D2_dly 32 Step for adjust, 1 step = 0.2ns
15:13	/	/	/
12:8	R/W	0x0	D1_dly 32 Step for adjust, 1 step = 0.2ns
7:5	/	/	/
4:0	R/W	0x0	D0_dly 32 Step for adjust, 1 step = 0.2ns

8.1.7.54. 0x0520 Parser CSIC SYNC EN Register(Default Value:0x0000_0000)

Offset :0x0520			Register Name: CSIC_SYNC_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
19:16	R/W	0x0	Input vsync singal Source select 0: Vsync signals all from 1 parser 1: Vsync signals from 2 parser others:reserved
15:12	/	/	/
11:8	R/W	0x0	Generate sync singal Benchmark select Bit8: USE VSYNC_Input0 Bit9: USE VSYNC_Input1 Bit10: USE VSYNC_Input2 Bit11: USE VSYNC_Input3 Set 1,Use input
7:4	R/W	0x0	Parser input vsync singal enable in sync mode Bit4: VSYNC_Input0 Bit5: VSYNC_Input1 Bit6: VSYNC_Input2 Bit7: VSYNC_Input3 Set 1,enable input
3	/	/	/
2	R/W	0x0	Parser sent sync singal via by 0: FSYNC0 1: Reserved
1	R/W	0x0	Parser sync signal source select 0: From outside 1: Generate by self
0	R/W	0x0	Enable Parser sent sync signal 0: Disable 1: Enable

8.1.7.55. 0x0524 Parser CSIC SYNC CFG Register(Default Value:0x0000_0000)

Offset :0x0524			Register Name: CSIC_PULSE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PUL_WID Sync signal pulse width $N*T_{24M}$, $N*T_{24M} \geq 4*Tpclk$
15:0	R/W	0x0	SYNC_DISTANCE The interval of two sync signal

8.1.7.56. 0x0528 Parser CSIC VS WAIT N Register(Default Value:0x0000_0000)

Offset :0x0528			Register Name: CSIC_SYNC_WAIT_N_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_N When multi-channel vsync all come, the max wait time.

8.1.7.57. 0x052C Parser CSIC VS WAIT M Register(Default Value:0x0000_0000)

Offset :0x052C			Register Name: CSIC_SYNC_WAIT_M_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VS_WAIT_M When in multi-channel mode, vsync comes at the different time, these bits indicate the max wait time.

8.1.8. CSIC DMA Register Description

8.1.8.1. 0x0000 CSIC DMA Enable Register(Default Value:0x7000_0000)

Offset:0x0000			Register Name: CSIC_DMA_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VER_EN
30	R/W	0x1	VFLIP_BUF_ADDR_CFG_MODE Vflip buffer address set by software or calculated by hardware 0: hardware 1: software
29	R/W	0x1	BUF_LENGTH_CFG_MODE Buffer length set by software or calculated by hardware

			0: hardware 1: software
28	R/W	0x1	FLIP_SIZE_CFG_MODE FLIP SIZE set by software or calculated by hardware 0: hardware 1: software
27:9	/	/	/
7	R/W	0x0	BUF_ADDR_MODE 0: Buffer Address Register Mode 1: Buffer Address FIFO Mode
6	R/W	0x0	VI_TO_CNT_EN Enable Video Input Timeout counter, add 1 when there is no effective video input in a 12M clock, clear to 0 when detecting effective video input. 0: disable 1: enable
5	R/W	0x0	FRAME_CNT_EN When BK_TOP_EN enable, this bit is set to 1 to indicate that the Frame counter starts to add. 0: Disable 1: Enable
4	R/W	0x0	DMA_EN When BK_TOP_EN enable, this bit is set to 1 to indicate that module works in DMA mode. 0: Disable 1: Enable
3	R/W	0x0	FBC_EN When BK_TOP_EN enable, this bit is set to 1 indicate that module works in FBC mode. 0: Disable 1: Enable
2	R/W	0x0	CLK_CNT_SPL Sampling time for clk counter per frame 0: Sampling clock counter every frame done 1: Sampling clock counter every vsync
1	R/W	0x0	CLK_CNT_EN clk count per frame enable
0	R/W	0x0	BK_TOP_EN 0: Disable 1: Enable

8.1.8.2. 0x0004 CSIC DMA Configuration Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: CSIC_DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:24	R/W	0x0	PAD_VAL Padding value when OUTPUT_FMT is prgb888 0x00~0xff
23:22	/	/	/
21	R/W	0x0	YUV 10bit input cut to 8bit 0: disable 1: enable
20	R/W	0x0	YUV 10bit store configure 0: YUV 10bit Stored in low 10bit of a 16bit-word 1: YUV 10bit Stored in high 10bit of a 16bit-word
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set to RAW stream 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: reserved 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: reserved When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined(UV sequence) 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111: frame planar YCbCr 422 UV combined(UV sequence) 1000: filed planar YCbCr 422 UV combined(VU sequence) 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011: frame planar YCbCr 422 UV combined(VU sequence) 1100: reserved 1101: field YCbCr 400

			1110: reserved 1111: frame YCbCr 400 When the input format is set YUV420 0000: LBC Mode Output 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: reserved 0100: reserved 0101: field planar YCbCr 420 UV combined(UV sequence) 0110: frame planar YCbCr 420 UV combined(UV sequence) 0111~1000: reserved 1001: field planar YCbCr 420 UV combined(VU sequence) 1010: frame planar YCbCr 420 UV combined(VU sequence) 1011~1100: reserved 1101: field YCbCr 400 1110: reserved 1111: frame YCbCr 400
15:14	/	/	/
13	R/W	0x0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0x0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0x0	FIELD_SEL Field selection. 00: capturing with field 0. 01: capturing with field 1. 10: capturing with either field. 11: reserved
9:6	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames 2: 1/3 fps, only receives the first frame every 3 frames 3: 1/4 fps, only receives the first frame every 4 frames 4: 1/5 fps, only receives the first frame every 4 frames …… 15: 1/16 fps, only receives the first frame every 16 frames
5:2	/	/	/

1:0	R/W	0x0	MIN_SDR_WR_SIZE Minimum size of SDRAM block write 00: 256 bytes (if hflip is enable, always select 256 bytes) 01: 512 bytes 10: 1k bytes 11: 2k bytes

8.1.8.3. 0x0010 CSIC DMA Horizontal Size Register(Default Value:0x0500_0000)

Offset: 0x0010			Register Name: CSIC_DMA_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN When BK_TOP_EN enable, FBC_EN enable, DMA_EN disable, these bits indicate Input width in FBC mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, LBC disable, these bits indicate Horizontal pixel unit length. Valid pixel of a line in DMA mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, LBC enable, these bits indicate Input width in LBC mode.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel unit start. Pixel is valid from this pixel.

8.1.8.4. 0x0014 CSIC DMA Vertical Size Register(Default Value:0x02D0_0000)

Offset: 0x0014			Register Name: CSIC_DMA_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x2D0	VER_LEN When BK_TOP_EN enable, FBC_EN enable, DMA_EN disable, these bits indicate Input height in FBC mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, LBC disable, these bits indicate Valid line number of a frame in DMA mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, LBC enable, these bits indicate Input height in LBC mode.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

8.1.8.5. 0x0020 CSIC DMA FIFO 0 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSIC_DMA_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F0_BUFA When BK_TOP_EN enable, FBC_EN enable, DMA_EN disable, these bits indicate output address of overhead data in FBC mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, LBC_EN disable, these bits indicate FIFO 0 output buffer-A address in DMA mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, LBC_EN enable, these bits indicate the output buffer address in LBC mode.

8.1.8.6. 0x0024 CSIC DMA FIFO 0 Output Buffer-A Address Result Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSIC_DMA_F0_BUFA_RESULT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F0_BUFA_RESULT Indicate the final F0_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.7. 0x0028 CSIC DMA FIFO 1 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSIC_DMA_F1_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	F1_BUFA When BK_TOP_EN enable, FBC_EN enable, DMA_EN disable, these bits indicate output address of compressed data in FBC mode. When BK_TOP_EN enable, FBC_EN disable, DMA_EN enable, these bits indicate FIFO 1 output buffer-A address in DMA mode.

8.1.8.8. 0x002C CSIC DMA FIFO 1 Output Buffer-A Address Result Register(Default Value:0x0000_0000)

Offset: 0x002C			Register Name: CSIC_DMA_F1_BUFA_RESULT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RO	0x0	F1_BUFA_RESULT Indicate the final F1_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.9. 0x0030 CSIC DMA FIFO 2 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0030			Register Name: CSIC_DMA_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	F2_BUFA FIFO 2 output buffer-A address

8.1.8.10. 0x0034 CSIC DMA FIFO 2 Output Buffer-A Address Result Register(Default Value:0x0000_0000)

Offset: 0x0034			Register Name: CSIC_DMA_F2_BUFA_RESULT_REG
Bit	Read/Write	Default/Hex	Description
31:0	RO	0x0	F2_BUFA_RESULT Indicate the final F2_BUFA address used for DMA or FBC after software configuration or hardware calculation from Buffer-A address register or buffer address fifo. Only used for debug.

8.1.8.11. 0x0038 CSIC DMA Buffer Length Register(Default Value:0x0280_0500)

Offset: 0x0038			Register Name: CSIC_DMA_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x280	BUF_LEN_C DMA_MODE:Buffer length of chroma C in a line. Unit is byte. LBC_MODE:Buffer length Stride of luminance Y in ONLY Y line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE is set 0
15:14	/	/	/
13:0	R/W	0x500	BUF_LEN DMA_MODE:Buffer length of luminance Y in a line. Unit is byte. LBC_MODE: Buffer length Stride of luminance Y and chroma C in YC line. Unit is byte. Only Readable when BUF_LENGTH_CFG_MODE is set 0

8.1.8.12. 0x003C CSIC DMA Flip Size Register(Default Value:0x02D0_0500)

Offset: 0x003C			Register Name: CSIC_DMA_FLIP_SIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x2d0	VER_LEN Vertical line number when in VFLIP mode. Unit is line. Only Readable when FLIP_SIZE_CFG_MODE is set 0.
15:14	/	/	/

13:0	R/W	0x500	VALID_LEN Valid components of a line when in HFLIP mode. Unit is pixel component. Only Readable when FLIP_SIZE_CFG_MODE is set 0.

8.1.8.13. 0x0040 CSIC DMA Video Input Timeout Threshold0 Register(Default Value:0x0000_0000)

Offset: 0x0040			Register Name: CSIC_DMA_VI_TO_TH0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold0 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH0 after VI_TO_CNT_EN is set , Time Unit is a 12M clock period.

8.1.8.14. 0x0044 CSIC DMA Video Input Timeout Threshold1 Register(Default Value:0x0000_0000)

Offset: 0x0044			Register Name: CSIC_DMA_VI_TO_TH1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Video Input Timeout Threshold1 Set VIDEO_INPUT_TO_INT_PD when VI Counter reaches TH1 after getting the first frame has been input, Time Unit is a 12M clock period.

8.1.8.15. 0x0048 CSIC DMA Video Input Timeout Counter Value Register(Default Value:0x0000_0000)

Offset: 0x0048			Register Name: CSIC_DMA_VI_TO_CNT_VAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Video Input Timeout Counter Value Indicate the current value of Video Input Timeout Counter.

8.1.8.16. 0x004C CSIC DMA Capture Status Register(Default Value:0x0000_0000)

Offset: 0x004C			Register Name: CSIC_DMA_CAP_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When

			software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

8.1.8.17. 0x0050 CSIC DMA Interrupt Enable Register(Default Value:0x0000_0000)

Offset: 0x0050			Register Name: CSIC_DMA_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	FRM_LOST_INT_EN Set an INT when frame starts with empty Buffer Address FIFO , only use in BUF Address FIFO MODE.
14	R/W	0x0	STORED_FRM_CNT_INT_EN Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE.
13	R/W	0x0	BUF_ADDR_FIFO_INT_EN Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE.
12	R/W	0x0	VIDEO_INPUT_TO_INT_EN Set an INT when no video input exceeds the setting threshold time
11	R/W	0x0	CLR_FRAME_CNT_INT_EN Set a INT When Clear Frame cnt.
10	R/W	0x0	SENT_SYNC_INT_EN Set a INT When sent a SYNC signal.
9	R/W	0x0	FBC_DATA_WRDDR_FULL_EN Error flag of FBC_DATA_WRDDR_FULL.
8	R/W	0x0	FBC_OVHD_WRDDR_FULL_EN Error flag of FBC_OVHD_WRDDR_FULL.
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, changing the buffer address could only effect next frame
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.

5	R/W	0x0	LC_INT_EN Line counter flag The bit is set when the specific line has been written to dram every frame. The line number is set in the line counter register.
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 becomes overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 becomes overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 becomes overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

8.1.8.18. 0x0054 CSIC DMA Interrupt Status Register(Default Value:0x0000_0000)

Offset: 0x0054			Register Name: CSIC_DMA_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W1C	0x0	FRM_LOST_INT_PD Set an INT when frame starts with empty Buffer Address FIFO, only use in BUF Address FIFO MODE
14	R/W1C	0x0	STORED_FRM_CNT_INT_PD Set an INT when the value of CSIC_DMA_STORED_FRM_CNT reaches CSIC_DMA_STORED_FRM_THRESHOLD, only use in BUF Address FIFO MODE
13	R/W1C	0x0	BUF_ADDR_FIFO_INT_PD Set an INT when content in BUF Address FIFO less than CSIC_DMA_BUFA_FIFO_THRESHOLD, only use in BUF Address FIFO MODE
12	R/W1C	0x0	VIDEO_INPUT_TO_INT_PD Set an INT Pending when no video input exceeds the setting threshold time

11	R/W1C	0x0	CLR_FRAME_CNT_INT Set a INT When Clear Frame cnt.
10	R/W1C	0x0	SENT_SYNC_INT Set a INT When sent a SYNC signal.
9	R/W1C	0x0	FBC_DATA_WRDDR_FULL_PD Error flag of FBC_DATA_WRDDR_FULL.
8	R/W1C	0x0	FBC_OVHD_WRDDR_FULL_PD Error flag of FBC_OVHD_WRDDR_FULL.
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	R/W1C	0x0	LC_PD Line counter flag
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

8.1.8.19. 0x0058 CSIC DMA Line Counter Register(Default Value:0x0000_0000)

Offset: 0x0058			Register Name: CSIC_DMA_LINE_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	LINE_CNT_NUM The LINE_CNT_NUM value is set by user,when internal line counter reach the set value,the LC_PD will set.

8.1.8.20. 0x005C CSIC DMA Frame Counter Register(Default Value:0x0001_0000)

Offset: 0x005C			Register Name: CSIC_DMA_FRM_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FRM_CNT_CLR When the bit set to 1, Frame cnt is cleared to 0

30:16	R/W	0x1	PCLK_DMA_CLR_DISTANCE Frame cnt clear cycle $N*T_{SYNC}$
15:0	R	0x0	FRM_CNT Counter value of frame. When frame done comes, the internal counter value add 1, and when the reg full ,it is cleared to 0 . When parser sent a sync signal,it is cleared to 0.

8.1.8.21. 0x0060 CSIC DMA Frame Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0060			Register Name: CSIC_DMA_FRM_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 12MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

8.1.8.22. 0x0064 CSIC DMA Accumulated and Internal Clock Counter Register(Default Value:0x0000_0000)

Offset: 0x0064			Register Name: CSIC_DMA_ACC_ITNL_CLK_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/WC	0x0	ACC_CLK_CNT The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame is done, the software checks this accumulated value and clears it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame. When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing this register.
23:0	R	0x0	ITNL_CLK_CNT The instant value of internal frame clock counter. When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.

8.1.8.23. 0x0068 CSIC DMA FIFO Statistic Register(Default Value:0x0000_0000)

Offset: 0x0068	Register Name: CSIC_DMA_FIFO_STAT_REG

Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R	0x0	Line Index Indicates the line index in current vsync.
15:13	/	/	/
12:0	R	0x0	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.

8.1.8.24. 0x006C CSIC DMA FIFO Threshold Register(Default Value:0x0000_0400)

Offset: 0x006C			Register Name: CSIC_DMA_FIFO_THRS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x400	FIFO_THRS When FIFO occupied memory exceed the threshold, dram frequency can not change.

8.1.8.25. 0x0070 CSIC DMA PCLK Statistic Register(Default Value:0x0000_7FFF)

Offset: 0x0070			Register Name: CSIC_DMA_PCLK_STAT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R	0x0	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:0	R	0x7FFF	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

8.1.8.26. 0x0080 CSIC DMA BUF Address FIFO0 Entry Register(Default Value:0x0000_0000)

Offset: 0x0080			Register Name: CSIC_DMA_BUF_ADDR_FIFO0_ENTRY_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO0_ENTRY FIFO Entry of Buffer Address FIFO0 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.27. 0x0084 CSIC DMA BUF Address FIFO1 Entry Register(Default Value:0x0000_0000)

Offset: 0x0084			Register Name: CSIC_DMA_BUF_ADDR_FIFO1_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO1_ENTRY FIFO Entry of Buffer Address FIFO1 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.28. 0x0088 CSIC DMA BUF Address FIFO2 Entry Register(Default Value:0x0000_0000)

Offset: 0x0088			Register Name: CSIC_DMA_BUF_ADDR_FIFO2_ENTRY_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO2_ENTRY FIFO Entry of Buffer Address FIFO2 for input frames to be stored, only used in Buffer Addr FIFO Mode

8.1.8.29. 0x008C CSIC DMA BUF Threshold Register(Default Value:0x0020_0000)

Offset: 0x008C			Register Name: CSIC_DMA_BUF_TH_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
21:16	R/W	0x20	CSIC_DMA_STORED_FRM_THRESHOLD when stored frame counter value reaches the threshold , counter is cleared to 0 , only used in Buffer Addr FIFO Mode
15:6	/	/	/
5:0	R/W	0x0	CSIC_DMA_BUF_ADDR_FIFO_THRESHOLD when content in Buffer Address FIFO less than the threshold, an interrupt is set, only used in Buffer Addr FIFO Mode

8.1.8.30. 0x0090 CSIC DMA BUF Address FIFO Content Register(Default Value:0x0000_0000)

Offset: 0x0090			Register Name: CSIC_DMA_BUF_ADDR_FIFO_CON_REG
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:16	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO2_CONTENT FIFO Content of address buffered in Buffer Address FIFO2, only used in Buffer Addr FIFO Mode
15:14	/	/	/
13:8	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO1_CONTENT FIFO Content of address buffered in Buffer Address FIFO1, only used in Buffer Addr FIFO Mode

7:6	/	/	/
5:0	RO	0x0	CSIC_DMA_BUF_ADDR_FIFO0_CONTENT FIFO Content of address buffered in Buffer Address FIFO0, only used in Buffer Addr FIFO Mode

8.1.8.31. 0x0094 CSIC DMA Stored Frame Counter Register(Default Value:0x0000_0000)

Offset: 0x0094			Register Name: CSIC_DMA_STORED_FRM_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	RO	0x0	CSIC_DMA_STORED_FRM_CNT Indicates value of stored frames counter, when counter value reaches CSIC_DMA_STORED_FRM_THRESHOLD, counter is cleared to 0, only used in Buffer Addr FIFO Mode

8.1.8.32. 0x0100 CSIC LBC Configure Register(Default Value:0x8F30_0008)

Offset: 0x0100			Register Name: CSIC_LBC_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	Whether lossy compress enable
30:28	/	/	/
27	R/W	0x1	Glb enable
26	R/W	0x1	Dts enable
25	R/W	0x1	Ots enable
24	R/W	0x1	Msq enable
23:22	/	/	/
21	R/W	0x1	Updata advanture enable
20:16	R/W	0x10	Updata advanture ratio
15:4	/	/	/
3	R/W	0x1	Limit qp enable
2:0	R/W	0x0	Limit qp min

8.1.8.33. 0x0104 CSIC LBC Line Target Bit0 Register(Default Value:0x0000_2400)

Offset: 0x0104			Register Name: CSIC_LBC_LINE_TAR_BIT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x2400	Compress target bit for the even line

8.1.8.34. 0x0108 CSIC LBC Line Target Bit1 Register(Default Value:0x0000_3600)

Offset: 0x0108			Register Name: CSIC_LBC_LINE_TAR_BIT1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x3600	Compress target bit for the odd line

8.1.8.35. 0x010C CSIC LBC RC ADV Register(Default Value:0x1010_1010)

Offset: 0x010C			Register Name: CSIC_LBC_RC_ADV_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x10	Rate control advanture 3
23:16	R/W	0x10	Rate control advanture 2
15:8	R/W	0x10	Rate control advanture 1
7:0	R/W	0x10	Rate control advanture 0

8.1.8.36. 0x0110 CSIC LBC MB MIN Register(Default Value:0x006E_0037)

Offset: 0x0110			Register Name: CSIC_LBC_MB_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:16	R/W	0x6E	Macro block min bits1
15:9	/	/	/
8:0	R/W	0x37	Macro block min bits0

8.1.8.37. 0x01F4 CSIC DMA Feature List Register(Default Value:0x0000_0002)

Offset: 0x01F4			Register Name: CSIC_FEATURE_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R	0x1	DMA0_EMBEDDED_LBC 0: No Embedded LBC 1: Embedded LBC
0	R	0x0	DMA0_EMBEDDED_FBC 0: No Embedded DMA 1: Embedded FBC

8.2. MIPI CSI

8.2.1. Overview

- Compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00.00
- 1/2/4 data lane configuration and up to 1Gbps per Lane in HS transmission
- Supports format: YUV422-8bit/10bit, YUV420-8bit/10bit, RAW-8, RAW-10, RAW-12, RGB888, RGB565
- Supports MIPI DOL for WDR
- **For V833**, maximum video capture resolution for serial interface up to 2592 x 1936@30fps RAW data or 4*1080p@25fps YUV422 data
- **For V831**, maximum video capture resolution for serial interface up to 1080p@60fps

NOTE

The MIPI CSI of V833 has 4 data lanes, and the MIPI CSI of V831 only has 2 data lanes.

Contents

Figures

Tables

Chapter 9 Audio

9.1. I2S/PCM

9.1.1. Overview

The I2S/PCM controller is designed to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified mode format, Right-justified mode format, PCM mode format and TDM mode format.

The I2S/PCM controller includes the following features:

- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master/slave mode
- Adjustable interface voltage
- Clock up to 24.576MHz
- Adjustable audio sample resolution from 8-bit to 32-bit
- Up to 16 channel(fs = 48kHz) which has adjustable width from 8-bit to 32-bit
- Sample rate from 8kHz to 384kHz(CHAN = 2)
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width TXFIFO for data transmit, one 64 depth x 32-bit width RXFIFO for data receive
- Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports loop back mode for test

NOTE

V833 supports 2 I2S/PCM interfaces; V831 supports 1 I2S/PCM interface.

9.1.2. Block Diagram

The block diagram of I2S/PCM interface is shown as follows.

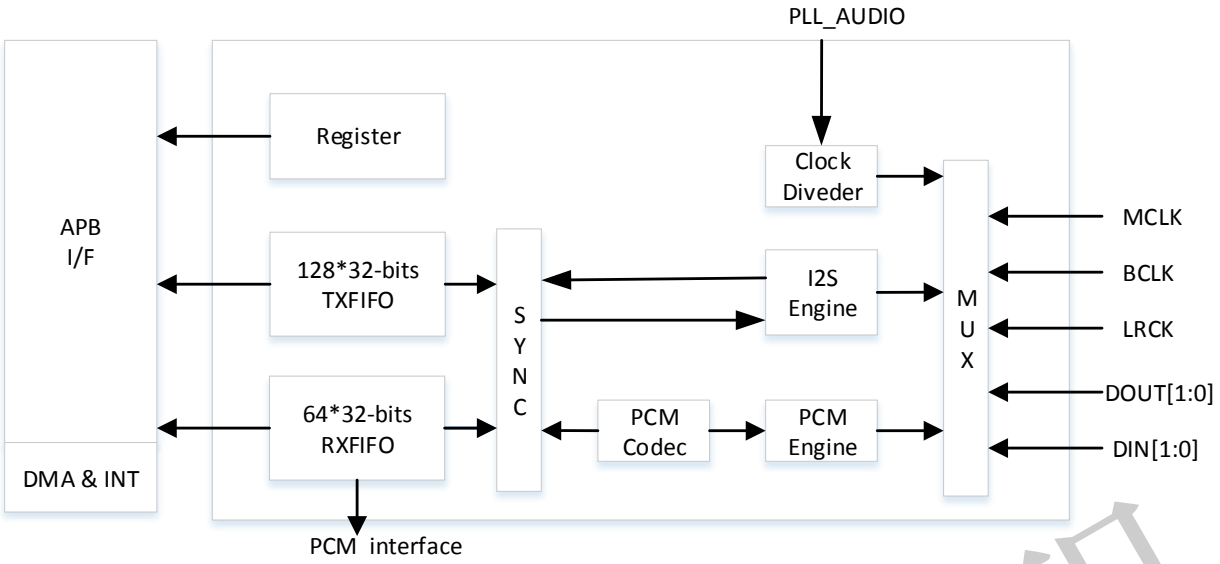

Figure 9- 1. I2S/PCM Interface System Block Diagram

9.1.3. Operations and Functional Descriptions

9.1.3.1. External Signals

Table 9-1 describes the external signals of I2S/PCM interface. LRCK and BCLK are bidirectional I/O, when I2S/PCM interface is configured as Master device, LRCK and BCLK is output pin; when I2S/PCM interface is configured as slave device, LRCK and BCLK is input pin. MCLK is an output pin for external device. DOUT is always the serial data output pin, and DIN is the serial data input pin. For information about General Purpose I/O port, see Port Controller.

Table 9- 1. I2S/PCM External Signals

V833 Signal	V831 Signal	Description	Type
I2S0_MCLK	I2S0_MCLK	I2S0 Master Clock	O
I2S0_BCLK	I2S0_BCLK	I2S0/PCM0 Sample Rate Serial Clock	I/O
I2S0_LRCK	I2S0_LRCK	I2S0 Sample Rate Left and Right Channel Select Clock/PCM0 Sync	I/O
I2S0_DIN	I2S0_DIN	I2S0/PCM0 Serial Data Input	I
I2S0_DOUT	I2S0_DOUT	I2S0/PCM0 Serial Data Output	O
I2S1_MCLK	/	I2S1 Master Clock	O
I2S1_BCLK	/	I2S1/PCM1 Sample Rate Serial Clock	I/O
I2S1_LRCK	/	I2S1 Sample Rate Left and Right Channel Select Clock/PCM1 Sync	I/O
I2S1_DIN[1:0]	/	I2S1/PCM1 Serial Data Input[1:0]	I
I2S1_DOUT[1:0]	/	I2S1/PCM1 Serial Data Output[1:0]	O

9.1.3.2. Clock Sources

Table 9-2 describes the clock sources for I2S/PCM. Users can see **Chapter 3.3.CCU** for clock setting, configuration and gating information.

Table 9- 2. I2S/PCM Clock Sources

Clock Name	Description
PLL_AUDIO	24.576 MHz or 22.5792 MHz generated by PLL_AUDIO to produce 48 kHz or 44.1 kHz sample frequency

9.1.3.3. Timing Diagram

The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode and TDM mode. Software can select any modes by setting the **I2S/PCM Control Register**. Figure 9-2 to Figure 9-6 describe the waveforms for SYNC, BCLK and DOUT, DIN.

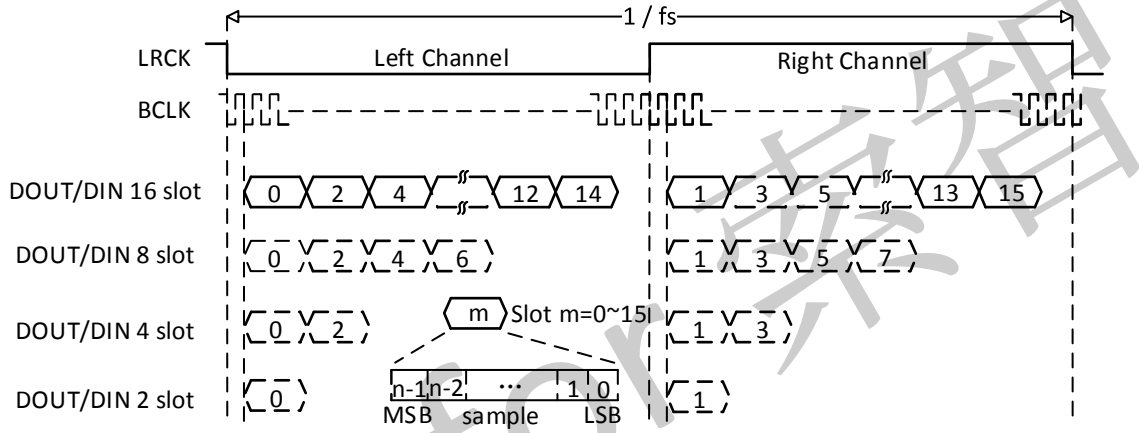

Figure 9- 2. I2S Standard Mode Timing

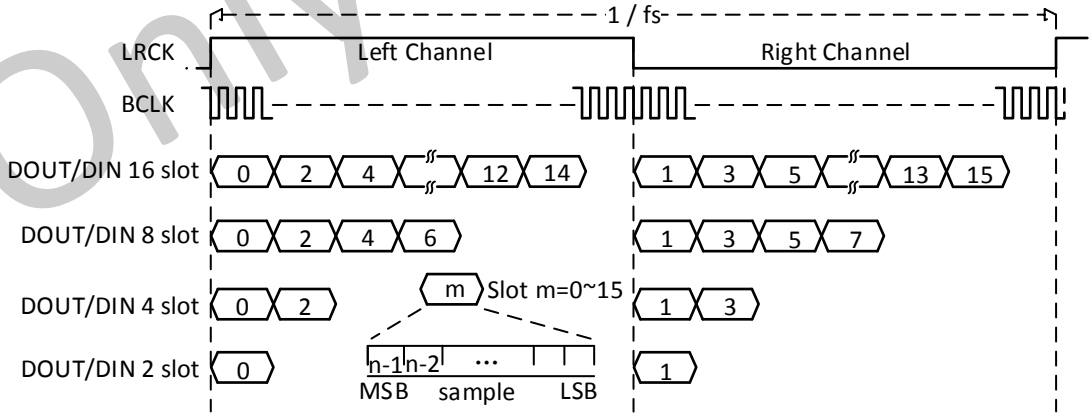

Figure 9- 3. Left-Justified Mode Timing

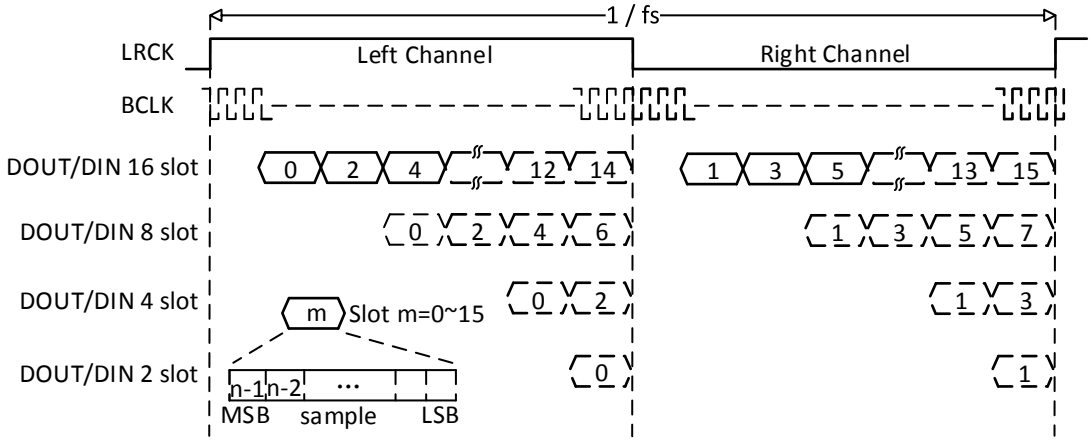

Figure 9- 4. Right-Justified Mode Timing

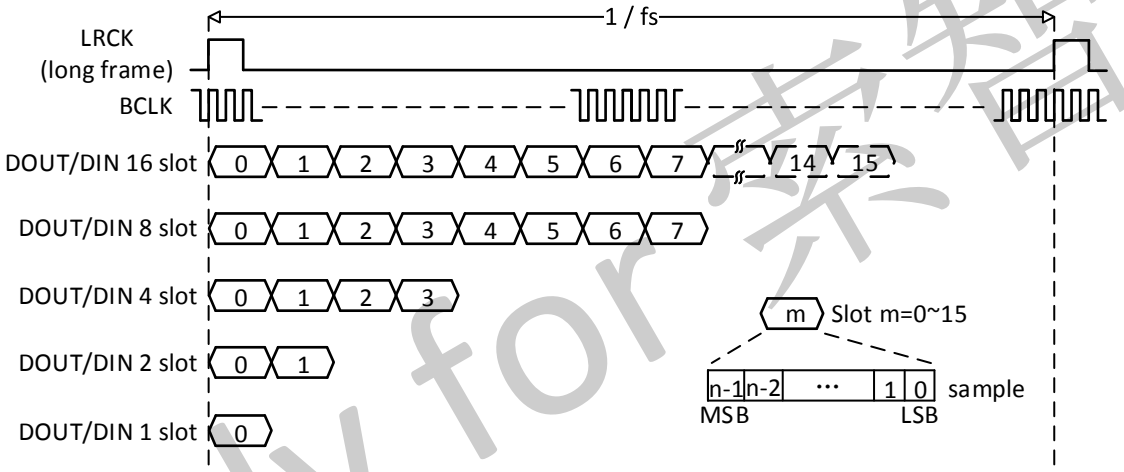

Figure 9- 5. PCM Long Frame Mode Timing

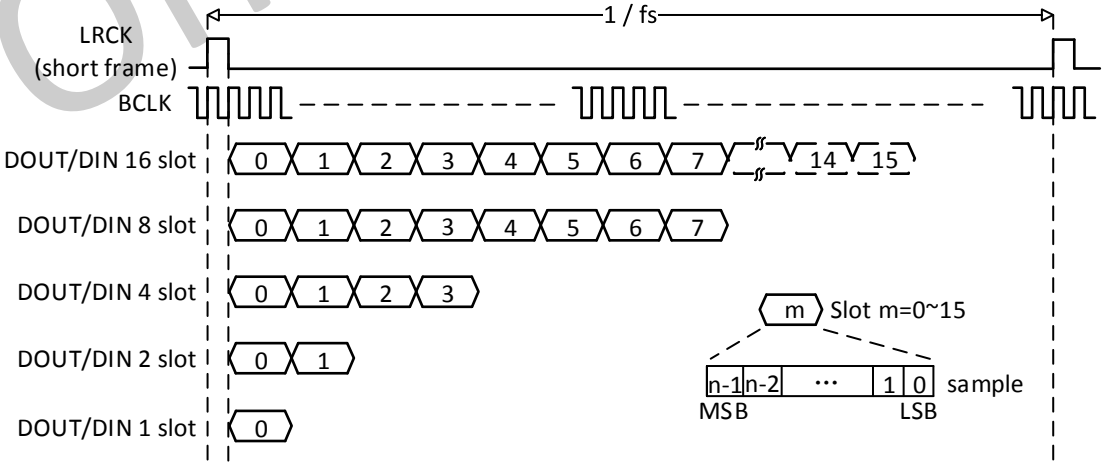

Figure 9- 6. PCM Short Frame Mode Timing

9.1.3.4. DIN Slot Mapping

The 4-wire DIN has 64 slots, each wire DIN has 16 slots, but RX is only 16 channels valid, the relationship between slot id and encoder is as follows.

Table 9- 3. DIN Slot ID and Encoder

DIN0 Slot ID	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DIN1 Slot ID	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DIN2 Slot ID	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
DIN3 Slot ID	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

There are 16 channels mapping configuration, each wire is selected four slots into RX.

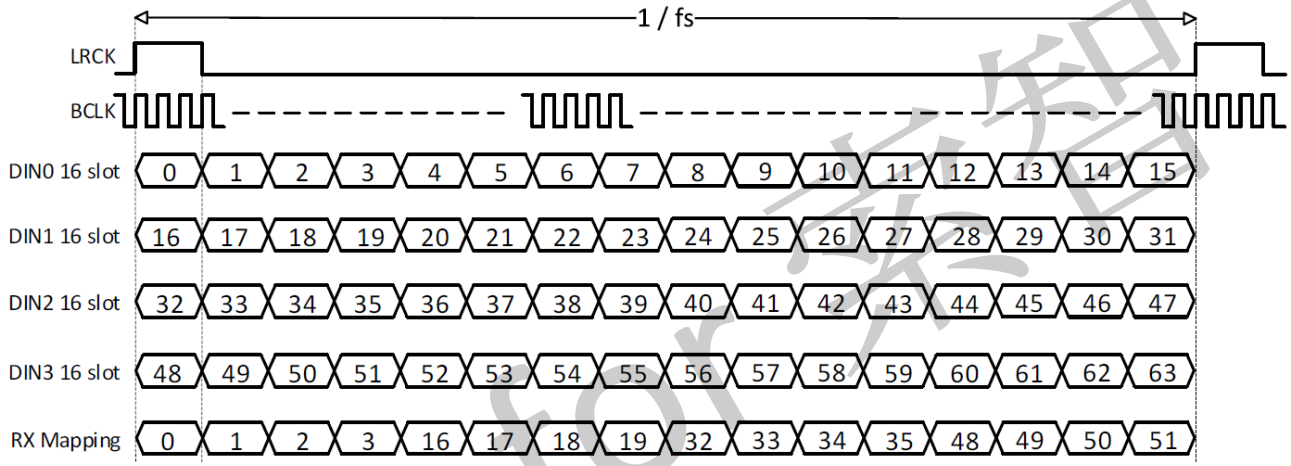

Figure 9- 7. 16 Channels Mapping Configuration

9.1.3.5. RX Slot Mapping

I2S/PCM has maximum 64 slot, but only maximum 16 slot is valid, so slot id needs be re-encoded, as shown in Table 9-4. I2S/PCM has 16 mapping configuration, the corresponding number of each mapping is 0~63, it indicates which slot id the final valid slot corresponds to.

Table 9- 4. RX Mapping Encoding

Valid Slot	0	2	4	6	8	10	12	14	1	3	5	7	9	11	13	15
Slot id	16	18	20	22	24	26	28	30	17	19	21	23	25	27	29	31
Slot id	32	34	36	38	40	42	44	46	33	35	37	39	41	43	45	47
Slot id	48	50	52	54	56	58	60	62	49	51	53	55	57	59	61	63

9.1.3.6. Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

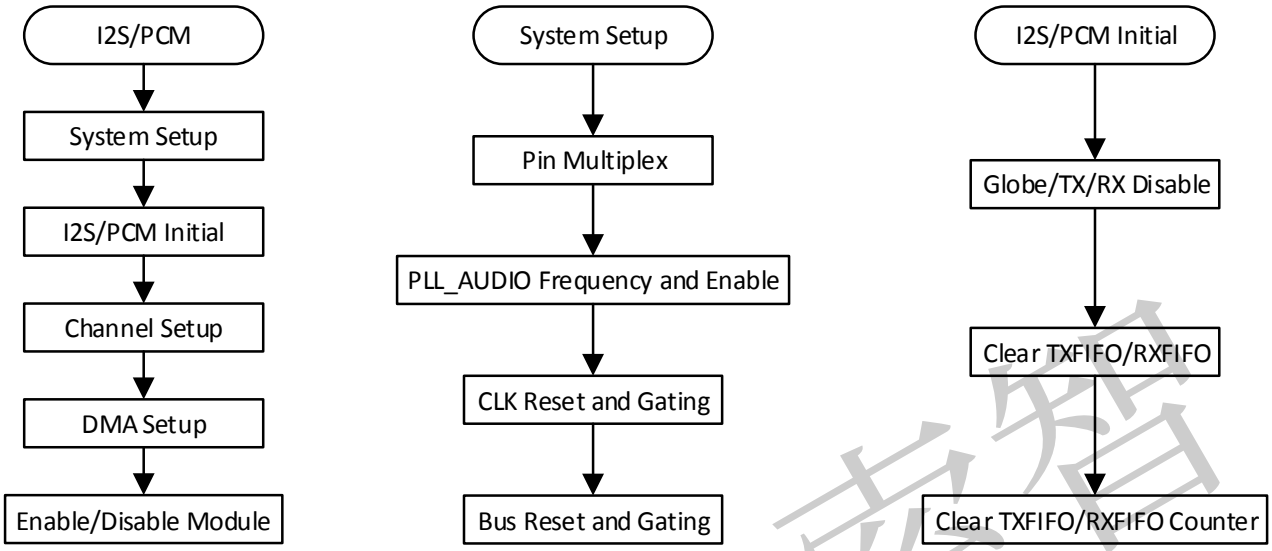

Figure 9- 8. I2S/PCM Operation Flow

(1). System Setup and I2S/PCM Initialization

The clock source for the I2S/PCM should be followed. At first you must disable the PLL_AUDIO through the **PLL_ENABLE** bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must set up the frequency of the PLL_AUDIO in the **PLL_AUDIO_CTRL_REG**. After that, you must open the I2S/PCM gating through the **I2S/PCM_CLK_REG** when you checkout that the LOCK bit of **PLL_AUDIO_CTRL_REG** becomes to 1. At last, you must reset and open the I2S/PCM bus gating in the **CCU_I2S_BGR_REG**.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should close the **Globe Enable** bit(I2S/PCM_CTL[0]), **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit[25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX FIFO and RX FIFO counter by writing 0 to **I2S/PCM_TXCNT** and **I2S/PCM_RXCNT**.

(2). Channel Setup and DMA Setup

First, you can setup the master I2S/PCM and the slave I2S/PCM. The configuration can be referred to the protocol of I2S/PCM. Then, you can set up the translation mode, the sample resolution, the wide of slot, the channel slot number and the trigger level and so on. The setup of register can be found in the specification.

The I2S/PCM supports two methods to transfer the data. The most common way is DMA, the setup of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3). Enable and Disable I2S/PCM

To enable the function, you can enable TX/RX by writing **the I2S/PCM_CT**L[2:1]. After that, you must enable I2S/PCM by writing 1 to the **Globe Enable** bit in the I2S/PCM_CTL. Write 0 to the **Globe Enable** bit to disable I2S/PCM.

9.1.4. Programming Guidelines

The following example assumes that the audio channels are stereo channels in I2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits. The recording and playback processes are as follows.

----------GPIO configuration----------

Step1: Ensure that I2S/PCM0 GPIO has power supply.

Step2: Configure GPIOH0/GPIOH1/GPIOH2/GPIOH3/GPIOH4 as Function3.

----------Clock configuration----------

Step1: Configure PLL_AUDIO as 24.576MHz, that is, set **PLL_AUDIO Control Register** to 0xA90B1701, set **PLL_AUDIO Pattern0 Register** to 0xC00126E9 (If PLL_AUDIO is set as 22.5792MHz, that is, set **PLL_AUDIO Control Register** to 0xA90B1501, set **PLL_AUDIO Pattern0 Register** to 0xC001288D).

Step2: Check whether **PLL_AUDIO Control Register**[PLL_AUDIO_LOCK] is 0x1. If is 1, set **I2S/PCM0 Clock Register** to 0x80000000.

Step3: Write 0x1 to the bit16 of **I2S/PCM0 Bus Gating Reset Register** to dessert I2S/PCM0 reset.

Step4: Write 0x1 to the bit0 of **I2S/PCM0 Bus Gating Reset Register** to open I2S/PCM0 gating.

NOTE

The Step3 and Step4 is set separately.

----------Initialization I2S/PCM----------

Step1: Set the bit[2:0] of **I2S/PCM Control Register** to 0 to close TXEN,RXEN and GEN.

Step2: Set the bit[25:24] of **I2S/PCM FIFO Control Register** to 0x3 to clear TXFIFO and RXFIFO.

Step3: Set **I2S/PCM TX Counter Register** to 0 to clear TX counter, set **I2S/PCM RX Counter Register** to 0 to clear RX counter.

----------Format configuration----------

Step1: Master/slave configuration. In master mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0x3; in slave mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0.

Step2: Configure the[5:4] of **I2S/PCM Control Register** to 0x1 to set standard I2S mode, configure the bit[21:20] of **I2S/PCM TX0 Channel Select Register** to 0x1, configure the bit[21:20] of **I2S/PCM RX Channel Select Register** to 0x1.

Step3: Configure the bit[6:4] of **I2S/PCM Format Register0** to 0x3 to set sample resolution, configure the bit[2:0] of **I2S/PCM Format Register0** to 0x3 to set channel width.

Step4: Configure the bit[7:4] of **I2S/PCM Channel Configuration Register** to 0x1 to set RX channel number, configure the bit[3:0] of **I2S/PCM Channel Configuration Register** to 0x1 to set TX channel number. Configure the bit[19:16] of **I2S/PCM TX0 Channel Select Register** to 0x1, configure the bit[1:0] of **I2S/PCM TX0 Channel Select**

Register to 0x3. Configure the bit[19:16] of **I2S/PCM RX Channel Select Register** to 0x1.

Step5: Configure the bit[7:0] of **I2S/PCM TX0 Channel Mapping Register 1** to 0x10, configure the bit[5:0] of **I2S/PCM RX Channel Mapping Register 3** to 0x0, configure the bit[13:8] of **I2S/PCM RX Channel Mapping Register 3** to 0x1.

----------Clock divider configuration----------

Step1: Set MCLK divider. Configure the bit[3:0] of **I2S/PCM Clock Divide Register** to 0x1, that is, MCLK=24.576MHz. Configure the bit8 of **I2S/PCM Clock Divide Register** to 0x1 to enable MCLK.

Step2: Set BCLK divider. Configure the bit[7:4] of **I2S/PCM Clock Divide Register** to 0xF, that is, BCLK=Sample ratio*Slot_Width*Slot_Num=48K*16*2=1.536MHz.

Step3: Set LRCK divider. Configure the bit[17:8] of **I2S/PCM Format Register** to 0xF, that is, N-1=BCLK/Sample ratio/ Slot_Num =16,N=15.

----------DMA configuration----------

Step1: Set data width of both DMA_SRC and DMA_DEST to 16-bit.

Step2: Set DMA BLOCK SIZE,DMA_SRC BLOCK SIZE and DMA_DEST BLOCK SIZE to 8.

Step3: TX DMA configuration. Set DMA_SRC_DRQ_TYPE to DRAM, set DMA_SRC_ADDR_MODE to Linear Mode, set DMA_DEST_DRQ_TYPE to I2S/PCM0-TX, set DMA_DEST_ADDR_MODE to IO Mode, set DMA_SRC_ADDR to DRAM address of storing data, set DMA_DEST_ADDR to **I2S/PCM TXFIFO**(address: 0x05090020).

Step4: RX DMA configuration. Set DMA_SRC_DRQ_TYPE to I2S/PCM0-RX, set DMA_SRC_ADDR_MODE to IO Mode, set DMA_DEST_DRQ_TYPE to DRAM, set DMA_DEST_ADDR_MODE to Linear Mode, set DMA_SRC_ADDR to **I2S/PCM RXFIFO**(address: 0x05090010), set DMA_DEST_ADDR to DRAM address of storing data.

For more details about DMA, please see the description of DMA in section 3.9.

NOTE

If data is stored in SRAM, then DRAM is modified to SRAM.

----------Recording/playback/pause----------

Step1: Enable globe, set the bit0 of **I2S/PCM Control Register** to 0x1. Enable DOUT0_EN, set the bit8 of **I2S/PCM Control Register** to 0x1.

Step2: Recording start: set the bit1 of **I2S/PCM Control Register** to 0x1, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step3: Playback start: set the bit2 of **I2S/PCM Control Register** to 0x1, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step4: Recording pause: set the bit1 of **I2S/PCM Control Register** to 0, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0.

Step5: Playback pause: set the bit2 of **I2S/PCM Control Register** to 0, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0.

9.1.5. Register List

Module Name	Base Address

I2S/PCM0	0x05090000
I2S/PCM1(only for V833)	0x05091000

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RXFIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register
I2S/PCM_TXFIFO	0x0020	I2S/PCM TXFIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TX0CHCFG	0x0034	I2S/PCM TX0 Channel Configuration Register
I2S/PCM_TX1CHCFG	0x0038	I2S/PCM TX1 Channel Configuration Register
I2S/PCM_TX2CHCFG	0x003C	I2S/PCM TX2 Channel Configuration Register
I2S/PCM_TX3CHCFG	0x0040	I2S/PCM TX3 Channel Configuration Register
I2S/PCM_TX0CHMAP0	0x0044	I2S/PCM TX0 Channel Mapping Register0
I2S/PCM_TX0CHMAP1	0x0048	I2S/PCM TX0 Channel Mapping Register1
I2S/PCM_TX1CHMAP0	0x004C	I2S/PCM TX1 Channel Mapping Register0
I2S/PCM_TX1CHMAP1	0x0050	I2S/PCM TX1 Channel Mapping Register1
I2S/PCM_TX2CHMAP0	0x0054	I2S/PCM TX2 Channel Mapping Register0
I2S/PCM_TX2CHMAP1	0x0058	I2S/PCM TX2 Channel Mapping Register1
I2S/PCM_TX3CHMAP0	0x005C	I2S/PCM TX3 Channel Mapping Register0
I2S/PCM_TX3CHMAP1	0x0060	I2S/PCM TX3 Channel Mapping Register1
I2S/PCM_RXCHSEL	0x0064	I2S/PCM RX Channel Select Register
I2S/PCM_RXCHMAP0	0x0068	I2S/PCM RX Channel Mapping Register0
I2S/PCM_RXCHMAP1	0x006C	I2S/PCM RX Channel Mapping Register1
I2S/PCM_RXCHMAP2	0x0070	I2S/PCM RX Channel Mapping Register2
I2S/PCM_RXCHMAP3	0x0074	I2S/PCM RX Channel Mapping Register3

9.1.6. Register Description

9.1.6.1. 0x0000 I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/

18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	DOUT3_EN 0: Disable, Hi-Z State 1: Enable
10	R/W	0x0	DOUT2_EN 0: Disable, Hi-Z State 1: Enable
9	R/W	0x0	DOUT1_EN 0: Disable, Hi-Z State 1: Enable
8	R/W	0x0	DOUT0_EN 0: Disable, Hi-Z State 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE 0: Normal Transfer 1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM Mode (offset 0: Long Frame; offset 1: Short Frame) 01: Left Mode (offset 0: LJ Mode; offset 1: I2S Mode) 10: Right-Justified Mode 11: Reserved
3	R/W	0x0	LOOP Loop Back Test 0: Normal Mode 1: Loop Back Test When setting to '1' , the bit indicates that the DOUT connects to the DIN.
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN

			Globe Enable 0: Disable 1: Enable

9.1.6.2. 0x0004 I2S/PCM Format Register 0(Default Value: 0x0000_0033)

Offset: 0x0004			Register Name: I2S/PCM_FMT0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH LRCK Width(only apply in PCM mode) 0: LRCK = 1 BCLK Width (Short Frame) 1: LRCK = 2 BCLK Width (Long Frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY In I2S/Left-Justified/Right-Justified mode: 0: Left Channel when LRCK is low 1: Left channel when LRCK is high In PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
18	/	/	/
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follows. **PCM mode**: Number of BCLKs within (Left + Right) channel width. **I2S/Left-Justified/Right-Justified mode**: Number of BCLKs within each individual channel width (Left or Right) . For example: N = 7: 8 BCLKs width … N = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, DOUT drives data at negative edge 1: Invert mode, DOUT drives data at positive edge
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit

			111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: DOUT drives data and DIN sample data at the different BCLK edge 1: DOUT drives data and DIN sample data at the same BCLK edge BCLK_POLARITY = 0, EDGE_TRANSFER = 0, DIN sample data at positive edge; BCLK_POLARITY = 0, EDGE_TRANSFER = 1, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 0, DIN sample data at negative edge; BCLK_POLARITY = 1, EDGE_TRANSFER = 1, DIN sample data at positive edge.
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

9.1.6.3. 0x0008 I2S/PCM Format Register 1(Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	RX MLS MSB/LSB First Select 0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB/LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in Slot [Sample Resolution < Slot Width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each Slot
3:2	R/W	0x0	RX_PDM PCM Data Mode

			00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

9.1.6.4. 0x000C I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: TXFIFO underrun pending interrupt Write '1' to clear this interrupt.
5	R/W1C	0x0	TXO_INT TXFIFO Overrun Pending Interrupt 0: No pending interrupt 1: TXFIFO overrun pending interrupt Write '1' to clear this interrupt.
4	R	0x1	TXE_INT TXFIFO Empty Pending Interrupt 0: No pending IRQ 1: TXFIFO empty pending interrupt when data in TXFIFO are less than TX trigger level
3	/	/	/
2	R/W1C	0x0	RXU_INT RXFIFO Underrun Pending Interrupt 0: No pending interrupt 1: RXFIFO underrun pending interrupt Write '1' to clear this interrupt.
1	R/W1C	0x0	RXO_INT RXFIFO Overrun Pending Interrupt 0: No pending IRQ 1: RXFIFO overrun pending IRQ Write '1' to clear this interrupt.
0	R/W	0x0	RXA_INT RXFIFO Data Available Pending Interrupt

			0: No pending IRQ 1: Data available pending IRQ when data in RXFIFO are more than RX trigger level

9.1.6.5. 0x0010 I2S/PCM RXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

9.1.6.6. 0x0014 I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/WAC	0x0	FTX Write ‘1’ to flush TXFIFO, self clear to ‘0’.
24	R/WAC	0x0	FRX Write ‘1’ to flush RXFIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TXFIFO Empty Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition. Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RXFIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition. Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TXFIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bit transmitted audio sample:

			Mode 0: TXFIFO[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1: TXFIFO[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RXFIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of RXFIFO register 01: Expanding received sample sign bit at MSB of RXFIFO register 10: Truncating received samples at high half-word of RXFIFO register and low half-word of RXFIFO register is filled by '0' 11: Truncating received samples at low half-word of RXFIFO register and high half-word of RXFIFO register is expanded by its sign bit Example for 20-bit received audio sample: Mode 0: APB_RDATA[31:0] = {RXFIFO[31:12], 12'h0} Mode 1: APB_RDATA[31:0] = {12{RXFIFO[31]}, RXFIFO[31:12]} Mode 2: APB_RDATA [31:0] = {RXFIFO[31:16], 16'h0} Mode 3: APB_RDATA[31:0] = {16{RXFIFO[31], RXFIFO[31:16]}

9.1.6.7. 0x0018 I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TXFIFO Empty 0: No room for new sample in TXFIFO 1: More than one room for new sample in TXFIFO (>= 1 Word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TXFIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RXFIFO Available 0: No available data in RXFIFO 1: More than one sample in RXFIFO (>= 1 Word)
7	/	/	/
6:0	R	0x0	RXA_CNT RXFIFO available sample word counter

9.1.6.8. 0x001C I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

7	R/W	0x0	TX_DRQ TXFIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TXFIFO Overrun Interrupt Enable 0: Disable 1: Enable When setting to '1', an interrupt happens when writing new audio data if TXFIFO is full.
4	R/W	0x0	TXEI_EN TXFIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RXFIFO Data Available DRQ Enable 0: Disable 1: Enable When setting to '1', RXFIFO DMA request line is asserted if data is available in RXFIFO.
2	R/W	0x0	RXUI_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RXFIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RXFIFO Data Available Interrupt Enable 0: Disable 1: Enable

9.1.6.9. 0x0020 I2S/PCM TXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written to this

			register one by one. The left channel sample data is first and then the right channel sample.

9.1.6.10. 0x0024 I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **NOTE** **Whether in slave or master mode, when this bit is set to '1', MCLK should be output.**
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24

			1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

9.1.6.11. 0x0028 I2S/PCM TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

9.1.6.12. 0x002C I2S/PCM RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.

9.1.6.13. 0x0030 I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ 0: Normal mode for the last half cycle of BCLK in the slot 1: Turn to Hi-Z state for the last half cycle of BCLK in the slot
8	R/W	0x0	TX_STATE

			0: Transfer level 0 in non-transferring slot 1: Turn to Hi-Z State (TDM) in non-transferring slot
7:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot number between CPU/DMA and RXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
3:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot number between CPU/DMA and TXFIFO 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots

9.1.6.14. 0x0034 I2S/PCM TX0 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TX0CHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX0_OFFSET TX0 Offset Tune(TX0 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX0_CHSEL TX0 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX0_CHEN TX0 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.15. 0x0038 I2S/PCM TX1 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: I2S/PCM_TX1CHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX1_OFFSET TX1 Offset Tune(TX1 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX1_CHSEL TX1 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX1_CHEN TX1 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.16. 0x003C I2S/PCM TX2 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: I2S/PCM_TX2CHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX2_OFFSET TX2 Offset Tune(TX2 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX2_CHSEL TX2 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX2_CHEN TX2 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are)

			disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.17. 0x0040 I2S/PCM TX3 Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: I2S/PCM_TX3CHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	TX3_OFFSET TX3 Offset Tune(TX3 Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	TX3_CHSEL TX3 Channel (Slot) Number Select for Each Output 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	R/W	0x0	TX3_CHEN TX3 Channel (Slot) Enable The bit[15:0] refer to Slot [15:0]. When one or more Slot(s) is(are) disabled, the affected Slot(s) is(are) set to the disable state. 0: Disable 1: Enable

9.1.6.18. 0x0044 I2S/PCM TX0 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TX0CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX0_CH15_MAP TX0 Channel 15 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX0_CH14_MAP TX0 Channel 14 Mapping 0000: 1st Sample

			… 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
23:20	R/W	0x0	TX0_CH13_MAP TX0 Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX0_CH12_MAP TX0 Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX0_CH11_MAP TX0 Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX0_CH10_MAP TX0 Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX0_CH9_MAP TX0 Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

3:0	R/W	0x0	TX0_CH8_MAP TX0 Channel 8 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

9.1.6.19. 0x0048 I2S/PCM TX0 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: I2S/PCM_TX0CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX0_CH7_MAP TX0 Channel 7 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
27:24	R/W	0x0	TX0_CH6_MAP TX0 Channel 6 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
23:20	R/W	0x0	TX0_CH5_MAP TX0 Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX0_CH4_MAP TX0 Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ...

			1111: 16th Sample
15:12	R/W	0x0	TX0_CH3_MAP TX0 Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	TX0_CH2_MAP TX0 Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX0_CH1_MAP TX0 Channel 1 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX0_CH0_MAP TX0 Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.20. 0x004C I2S/PCM TX1 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: I2S/PCM_TX1CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX1_CH15_MAP TX1 Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample

			... 1111: 16th Sample
27:24	R/W	0x0	TX1_CH14_MAP TX1 Channel 14 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
23:20	R/W	0x0	TX1_CH13_MAP TX1 Channel 13 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX1_CH12_MAP TX1 Channel 12 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX1_CH11_MAP TX1 Channel 11 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th sample
11:8	R/W	0x0	TX1_CH10_MAP TX1 Channel 10 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX1_CH9_MAP TX1 Channel 9 Mapping 0000: 1st Sample

			… 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX1_CH8_MAP TX1 Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.21. 0x0050 I2S/PCM TX1 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: I2S/PCM_TX1CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX1_CH7_MAP TX1 Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX1_CH6_MAP TX1 Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	TX1_CH5_MAP TX1 Channel 5 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX1_CH4_MAP TX1 Channel 4 Mapping

			0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX1_CH3_MAP TX1 Channel 3 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
11:8	R/W	0x0	TX1_CH2_MAP TX1 Channel 2 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX1_CH1_MAP TX1 Channel 1 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX1_CH0_MAP TX1 Channel 0 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.22. 0x0054 I2S/PCM TX2 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S/PCM_TX2CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX2_CH15_MAP

			TX2 Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX2_CH14_MAP TX2 Channel 14 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
23:20	R/W	0x0	TX2_CH13_MAP TX2 Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX2_CH12_MAP TX2 Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX2_CH11_MAP TX2 Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX2_CH10_MAP TX2 Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample

			… 1111: 16th Sample
7:4	R/W	0x0	TX2_CH9_MAP TX2 Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX2_CH8_MAP TX2 Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.23. 0x0058 I2S/PCM TX2 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: I2S/PCM_TX2CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX2_CH7_MAP TX2 Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX2_CH6_MAP TX2 Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
23:20	R/W	0x0	TX2_CH5_MAP TX2 Channel 5 Mapping 0000: 1st Sample … 0111: 8th Sample

			1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX2_CH4_MAP TX2 Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX2_CH3_MAP TX2 Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	TX2_CH2_MAP TX2 Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX2_CH1_MAP TX2 Channel 1 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX2_CH0_MAP TX2 Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample

9.1.6.24. 0x005C I2S/PCM TX3 Channel Mapping Register 0(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: I2S/PCM_TX3CHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX3_CH15_MAP TX3 Channel 15 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX3_CH14_MAP TX3 Channel 14 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
23:20	R/W	0x0	TX3_CH13_MAP TX3 Channel 13 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
19:16	R/W	0x0	TX3_CH12_MAP TX3 Channel 12 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
15:12	R/W	0x0	TX3_CH11_MAP TX3 Channel 11 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th sample
11:8	R/W	0x0	TX3_CH10_MAP

			TX3 Channel 10 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
7:4	R/W	0x0	TX3_CH9_MAP TX3 Channel 9 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
3:0	R/W	0x0	TX3_CH8_MAP TX3 Channel 8 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

9.1.6.25. 0x0060 I2S/PCM TX3 Channel Mapping Register 1(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: I2S/PCM_TX3CHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	TX3_CH7_MAP TX3 Channel 7 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample
27:24	R/W	0x0	TX3_CH6_MAP TX3 Channel 6 Mapping 0000: 1st Sample … 0111: 8th Sample 1000: 9th Sample … 1111: 16th Sample

23:20	R/W	0x0	TX3_CH5_MAP TX3 Channel 5 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
19:16	R/W	0x0	TX3_CH4_MAP TX3 Channel 4 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
15:12	R/W	0x0	TX3_CH3_MAP TX3 Channel 3 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
11:8	R/W	0x0	TX3_CH2_MAP TX3 Channel 2 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
7:4	R/W	0x0	TX3_CH1_MAP TX3 Channel 1 Mapping 0000: 1st Sample ... 0111: 8th Sample 1000: 9th Sample ... 1111: 16th Sample
3:0	R/W	0x0	TX3_CH0_MAP TX3 Channel 0 Mapping 0000: 1st Sample ... 0111: 8th Sample

			1000: 9th Sample ... 1111: 16th Sample

9.1.6.26. 0x0064 I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: I2S/PCM_RXCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:20	R/W	0x0	RX_OFFSET RX Offset Tune(RX Data offset to LRCK) 0: No offset n: Data is offset by n BCLKs to LRCK
19:16	R/W	0x0	RX_CHSEL RX Channel (Slot) Number Select for Input 0000: 1 channel or slot ... 0111: 8 channels or slots 1000: 9 channels or slots ... 1111:16 channels or slots
15:0	/	/	/

9.1.6.27. 0x0068 I2S/PCM RX Channel Mapping Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: I2S/PCM_RXCHMAP0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH15_MAP RX Channel 15 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH14_MAP RX Channel 14 Mapping 000000: 1st Sample ... 000111: 8th Sample

			001000: 9th Sample ... 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH13_MAP RX Channel 13 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH12_MAP RX Channel 12 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample

9.1.6.28. 0x006C I2S/PCM RX Channel Mapping Register1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: I2S/PCM_RXCHMAP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH11_MAP RX Channel 11 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH10_MAP RX Channel 10 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample

15:14	/	/	/
13:8	R/W	0x0	RX_CH9_MAP RX Channel 9 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH8_MAP RX Channel 8 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample

9.1.6.29. 0x0070 I2S/PCM RX Channel Mapping Register2(Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: I2S/PCM_RXCHMAP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH7_MAP RX Channel 7 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH6_MAP RX Channel 6 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH5_MAP RX Channel 5 Mapping

			000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH4_MAP RX Channel 4 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample

9.1.6.30. 0x0074 I2S/PCM RX Channel Mapping Register3(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: I2S/PCM_RXCHMAP3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x0	RX_CH3_MAP RX Channel 3 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
23:22	/	/	/
21:16	R/W	0x0	RX_CH2_MAP RX Channel 2 Mapping 000000: 1st Sample … 000111: 8th Sample 001000: 9th Sample … 111111: 64th Sample
15:14	/	/	/
13:8	R/W	0x0	RX_CH1_MAP RX Channel 1 Mapping 000000: 1st Sample … 000111: 8th Sample

			001000: 9th Sample ... 111111: 64th Sample
7:6	/	/	/
5:0	R/W	0x0	RX_CH0_MAP RX Channel 0 Mapping 000000: 1st Sample ... 000111: 8th Sample 001000: 9th Sample ... 111111: 64th Sample

9.2. Audio Codec

9.2.1. Overview

The Audio Codec has 1-ch DAC and 1-ch ADC with a high level of mixed-signal integration which ideal for smart phone and other portable devices. The DRC with integrated hardware DAP engine can be used in record and playback paths.

The Audio Codec has the following features:

- One audio digital-to-analog(DAC) channel
  - Supports 8 kHz to 192 kHz DAC sample rate
  - 95±3dB SNR
  - Supports 16-bit and 20-bit audio sample resolution
- One audio output
  - One differential LINEOUTP/N or single-ended LINEOUTL output (**for V833**)
  - One sing-ended LINEOUTP or LINEOUTL output (**for V831**)
- One audio analog-to-digital(ADC) channel
  - Supports 8 kHz to 48 kHz ADC sample rate
  - 95±3dB SNR
  - Supports 16-bit and 20-bit audio sample resolution
- Two audio inputs
  - One differential microphone input: MICIN1P and MICIN1N
  - One single-ended LINEINL input (**only for V833**)
- Supports Dynamic Range Controller(DRC) adjusting the ADC recording and DAC playback
- One low-noise analog microphone bias output
- One 128x24-bits FIFO for DAC data transmit, one 128x24-bits FIFO for ADC data receive
- Programmable FIFO thresholds
- Interrupt and DMA support

9.2.2. Block Diagram

Figure 9-9 shows the block diagram of Audio Codec.

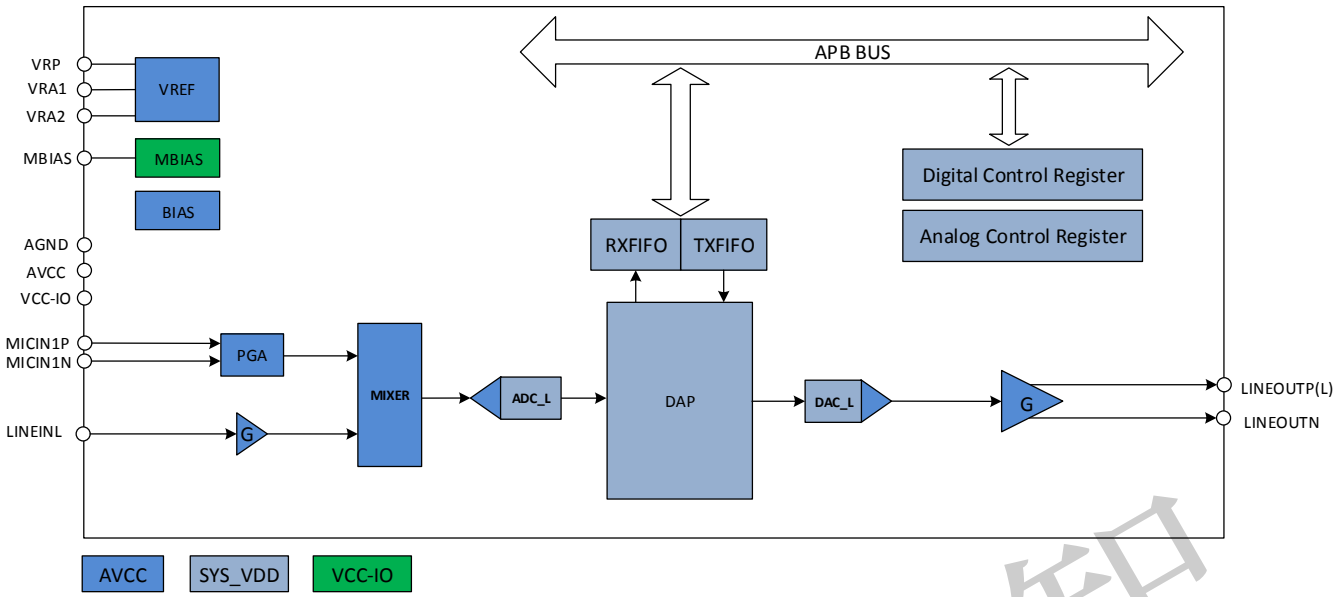

Figure 9- 9. Audio Codec Block Diagram

9.2.3. Operations and Functional Descriptions

9.2.3.1. External Signals

9.2.3.1.1. Analog I/O Pins

V833 Signal	V831 Signal	Type	Description
MICIN1P	MICIN1P	AI	Positive differential input for MIC1
MICIN1N	MICIN1N	AI	Negative differential input for MIC1
LINEINL	/	AI	Left single-end input for Line-in
LINEOUTP(L)	LINEOUTP(L)	AO	Differential mono positive output(or left single-end output for lineout)
LINEOUTN	/	AO	Differential mono negative output

9.2.3.1.2. Reference

V833 Signal	V831 Signal	Type	Description
MBIAS	/	AO	First bias voltage output for main microphone
VRA1	VRA1	AO	Internal reference voltage
VRA2	VRA2	AO	Internal reference voltage

9.2.3.1.3. Power/Ground

V833 Signal	V831 Signal	Type	Description
AVCC	AVCC	P	Analog power
AGND	AGND	G	Analog ground

9.2.3.2. Clock Sources

Figure 9-10 describes the Audio Codec clock source. Users can see ***CCU*** for clock setting, configuration and gating information.

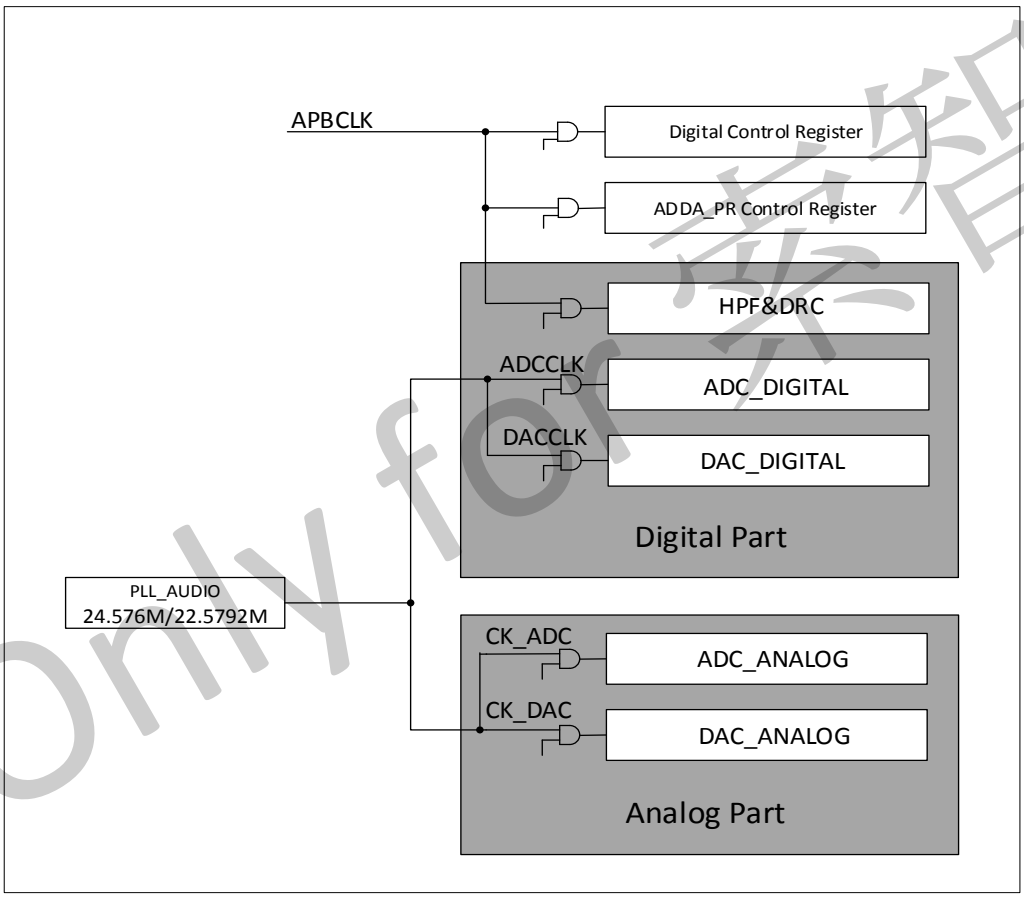

Figure 9- 10. Audio Codec Clock Diagram

The clock of digital part is from PLL_AUDIO(1X). The clock of analog part includes CK_ADC and CK_DAC. CK_ADC and CK_DAC is provided by PLL_AUDIO(1X).

9.2.3.3. Reset System

9.2.3.3.1. Digital Part Reset System

The SYS_RST will be provided by the VDD-SYS domain, which comes from VDD-SYS domain and is produced by RTC domain. Each domain has the de-bounce to confirm that the reset system is strong. The codec register part, MIX will be reset by the SYS_RST during the power on or the system soft writing the reset control logic. The other parts will be reset by the soft configure through writing register.

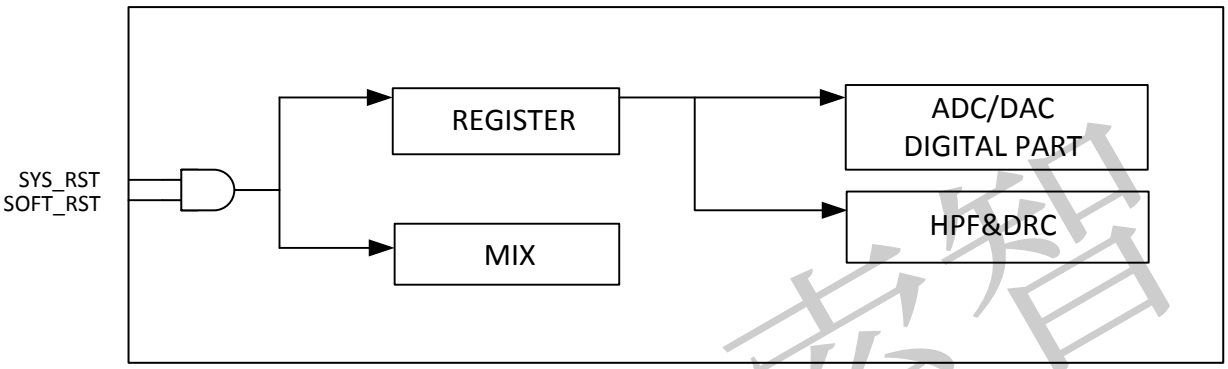

Figure 9- 11. Audio Codec Digital Part Reset System

9.2.3.3.2. Analog Part Reset System

When AVCC is powered on, it will send the AVCC_POR signal. And the AVCC_POR signal passes the level shift and RC filter part to ADDA logic core.

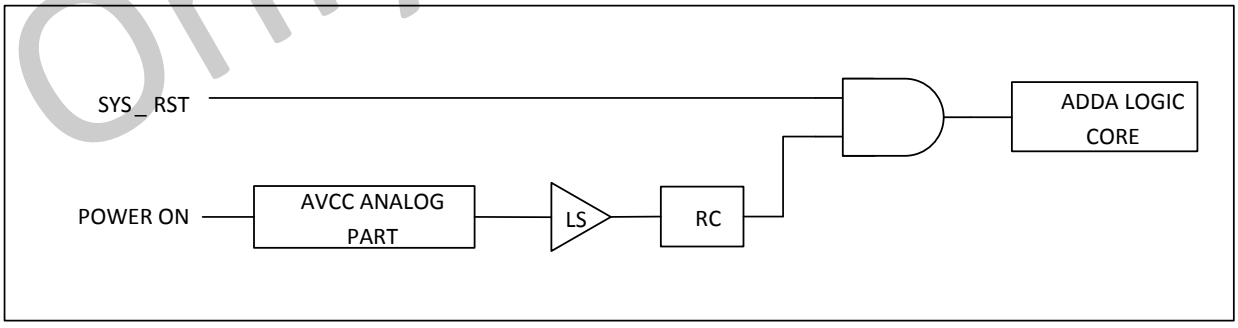

Figure 9- 12. Audio Codec Analog Part Reset System

9.2.3.4. Data Path Diagram

Figure 9-13 shows a data path of the Audio Codec.

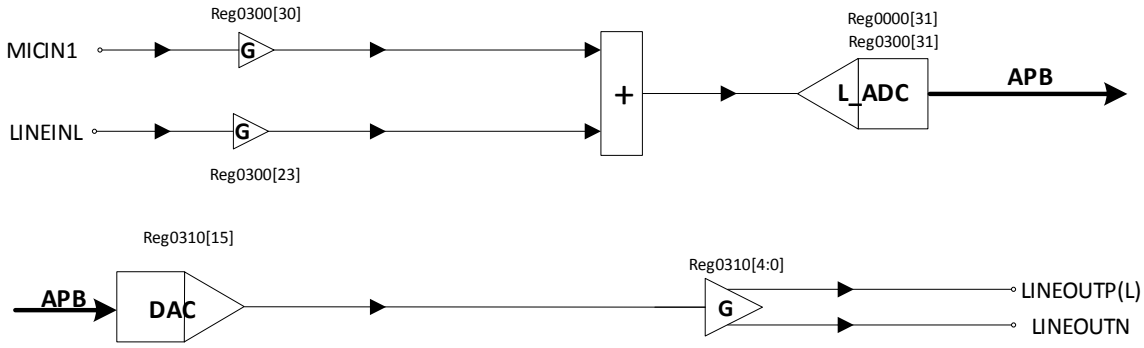

Figure 9- 13. Audio Codec Data Path Diagram

9.2.3.5. Mono ADC

The one ADC is used for recording stereo sound and a reference signal. The sample rate of the three ADC is independent of DAC sample rate. The digital ADC part can be enabled/disabled by the bit28 of the **AC_ADC_FIFOC** register.

9.2.3.6. Mono DAC

The mono DAC sample rate can be configured by setting the register. In order to save power, the DAC can be enabled/disabled by setting the bit[6] of the **MIX_DAC_CTRL** register. The digital DAC part can be enabled/disabled by the bit[31] of the **AC_DAC_DPC** register.

9.2.3.7. Mixer

The Audio Codec supports two mixers for all function requirements:

- 1 channel ADC Record mixers

The ADC record mixer is used to mix analog signals as input to the ADC for recording. The following signals can be mixed into the input mixer.

- MICIN1P/N
- LINEINL
- Mono DAC output

9.2.3.8. Analog Audio Input Path

The Audio Codec supports two analog audio input paths:

- MICIN1P/N
- LINEINL

MICIN1P/N, LINEINL provide differential input that can be mixed into the ADC record mixer. MICIN is high impedance,

low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. The gain for each pre-amplifier can be set independently. MBIAS provides reference voltage for electret condenser type(ECM) microphones.

9.2.3.9. Analog Audio Output Path

The Audio Codec has one type analog output port:

- LINEOUTP/N or LINEOUTL

The LINEOUT provides one differential output to drive line level signals to external audio equipment. The LINEOUTP(L) output source is from DACL. The LINEOUTN output source is from DAC differential output. The volume control is logarithmic with a 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The LINEOUT output buffer is powered up or down by the bit[7:6] of **LINEOUT_CTRL0**.

9.2.3.10. Microphone BIAS

The MBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components.

9.2.3.11. Interrupt

The Audio Codec has two interrupts. Figure 9-14 describes the Audio Codec interrupt system.

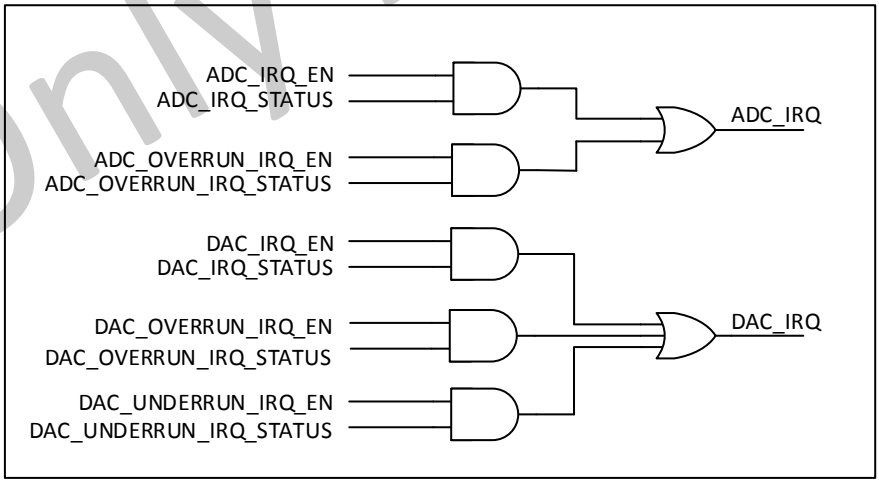

Figure 9- 14. Audio Codec Interrupt System

9.2.3.12. DAP

9.2.3.12.1. DAP Data Flow

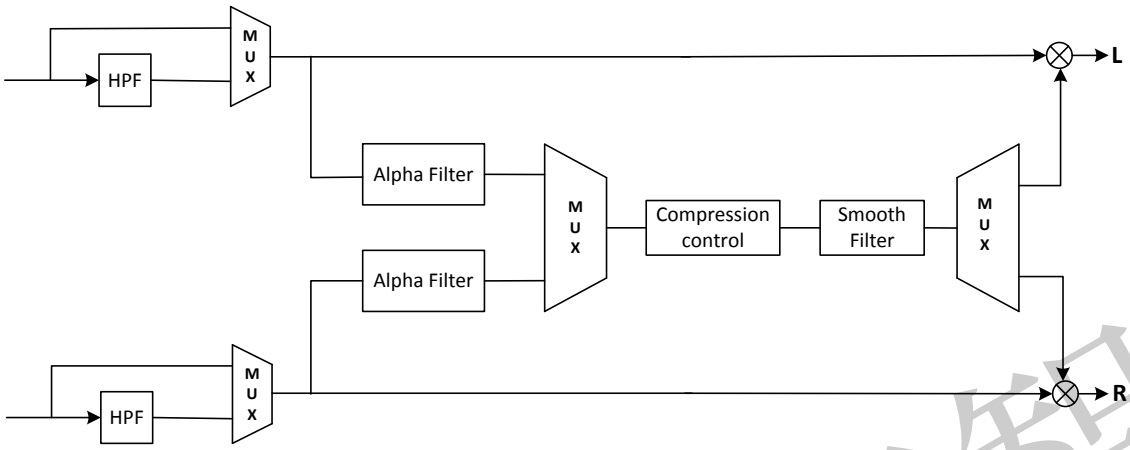

Figure 9- 15. DAP Data Flow

9.2.3.12.2. HPF Function

The DAP has individual channel high pass filter (HPF, -3dB cutoff < 1Hz) that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz that can be removed DC offset from ADC recording. The HPF can also be bypassed.

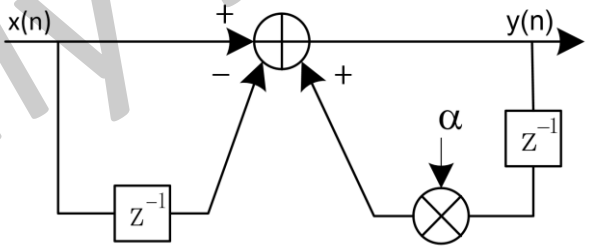

Figure 9- 16. HPF Function

9.2.3.12.3. DRC Function

The DRC scheme has three thresholds, three offset, and four slope (all programmable). There is one ganged DRC for the left/right channels. The diagram of DRC input/output is as follows.

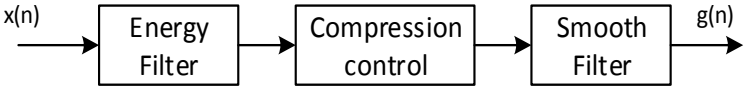

Figure 9- 17. DRC Block Diagram

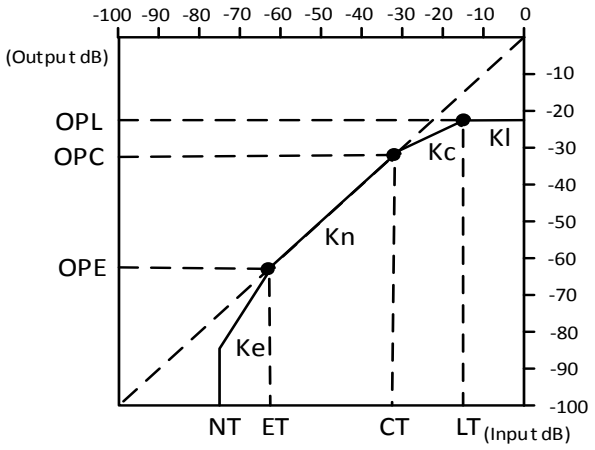

Figure 9- 18. DRC Static Curve Parameters

Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

One DRC is for left/right, and one DRC is for subwoofer.

Each DRC has adjustable threshold, offset, and compression levels, programmable energy, attack, and decay time constants.

Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

Figure 9- 19. DRC Process

DRC parameter setting:

- **Number format**

The Number format is N.M which means there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 9.23 means that there are 9 bits at the left of the decimal point and 23 bits at the right decimal point.

- **Energy Filter**

The Energy Filter is to estimate the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by $\alpha = 1 - e^{-2.2Ts/ta}$.

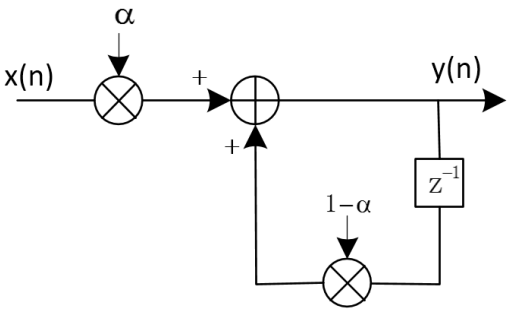

Figure 9- 20. Energy Filter Structure

Compression Control

This element has ten parameters (ET, CT, LT, Ke, Kn, Kc, Kl, OPL, OPC, OPE), which are all programmable, and the computation will be explained as follows.

- **Threshold Parameter Computation(T parameter)**

The threshold is the value that determines the signal to be compressed or not. When the signal's RMS is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by

$$Tin = -\frac{T_{dB}}{6.0206}$$

There, T_{dB} must less than zero, the positive value is illegal.

For example, it is desired to set CT=-40dB, then the Tin require to set CT to -40dB is CT_{in} = - (-40dB)/6.0206 = 6.644, CT_{in} is entered as a 32-bit number in 8.24 format.

Therefore, CT_{in} = 6.644 = 0000 0110.1010 0100 1101 0011 1100 0000 = 0x06A4 D3C0 in 8.24 format.

- **Slope Parameter Computation (K parameter)**

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB is for n dB RMS input. The k input to the coefficient ram is computed by $K = \frac{1}{n}$

There, n is from 1 to 50, and must be integer.

For example, it is desired to set 2:1, then the Kc require to set to 2:1 is Kc = 1/2 = 0.5, Kc is entered as a 32-bit number in 8.24 format.

Therefore, Kc = 0.5 = 0000 0000.1000 0000 0000 0000 0000 0000 = 0x0080 0000 in 8.24 format.

- **Gain Smooth Filter**

The Gain Smooth Filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 9-21. The structure of the Gain Smooth filter is also the Alpha filter, so the rise time computation is the same as the Energy filter which is $\alpha = 1 - e^{-2.2Ts/ta}$.

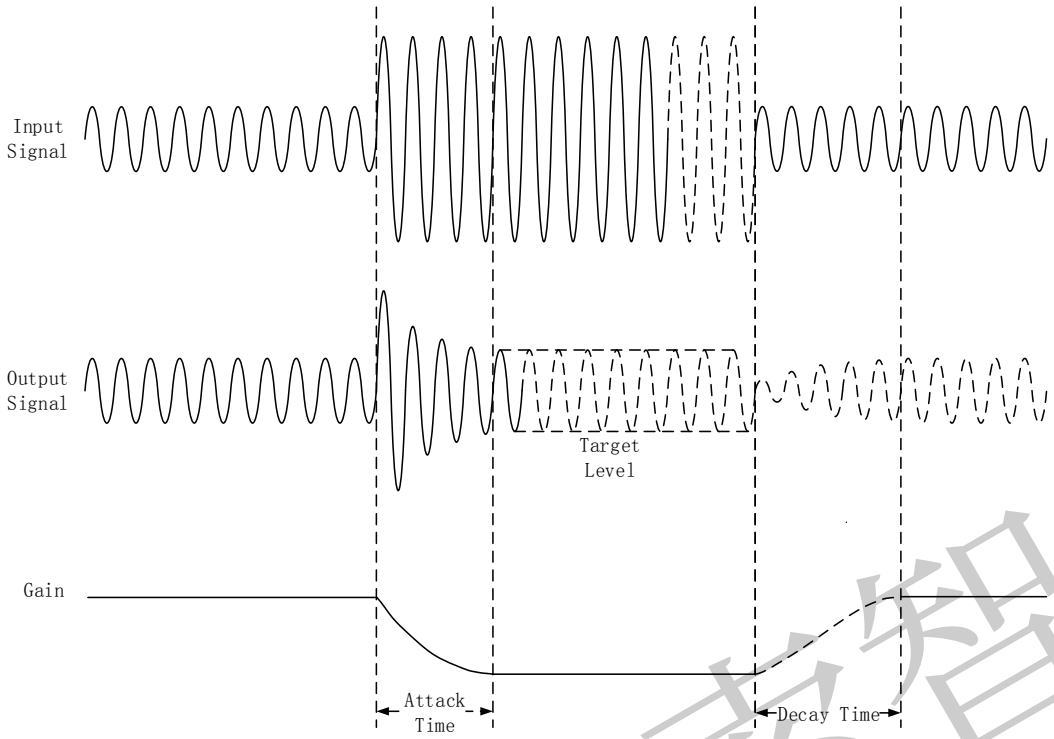

Figure 9- 21. Gain Smooth Filter

9.2.4. Programming Guidelines

9.2.4.1. Playback Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**. Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate, configure data transfer format, enable DAC.
(4) DMA configure and DMA request.
(5) Enable DAC DRQ and DMA.

9.2.4.2. Record Process

(1) Codec initial: Open audio codec bus clock gating and de-assert bus reset through **AUDIO_CODEC_BGR_REG**, configure PLL_Audio frequency and enable PLL_Audio through **PLL_AUDIO_CTRL_REG**. Please refer to CCU in chapter 3.3 about detail.
(2) Configure MIX path.
(3) Set sample rate, configure data transfer format, enable ADC.
(4) DMA configure and DMA request.
(5) Enable ADC DRQ and DMA.

9.2.5. Register List

Module Name	Base Address
Audio Codec	0x05096000

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
AC_DAC_FIFOC	0x0010	DAC FIFO Control Register
AC_DAC_FIFOS	0x0014	DAC FIFO Status Register
AC_DAC_TXDATA	0x0020	DAC TX DATA Register
AC_DAC_CNT	0x0024	DAC TX FIFO Counter Register
AC_DAC_DG	0x0028	DAC Debug Register
AC_ADC_FIFOC	0x0030	ADC FIFO Control Register
AC_ADC_FIFOS	0x0034	ADC FIFO Status Register
AC_ADC_RXDATA	0x0040	ADC RX Data Register
AC_ADC_CNT	0x0044	ADC RX Counter Register
AC_ADC_DG	0x004C	ADC Debug Register
AC_DAC_DAP_CTRL	0x00F0	DAC DAP Control Register
AC_ADC_DAP_CTR	0x00F8	ADC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Threshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Threshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Threshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold

AC_DAC_DRC_HET	0x016C	DAC DRC Expander Threshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Threshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth Filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth Filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth Filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_HPFHGAIN	0x01B8	DAC DRC HPF Gain High Coef Register
AC_DAC_DRC_HPFLGAIN	0x01BC	DAC DRC HPF Gain Low Coef Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Threshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Threshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Threshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold

AC_ADC_DRC_HET	0x026C	ADC DRC Expander Threshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Threshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth filter Gain Low Attack Time Coef Register
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGLS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_HPFHGAIN	0x02B8	ADC DRC HPF Gain High Coef Register
AC_ADC_DRC_HPFLGAIN	0x02BC	ADC DRC HPF Gain Low Coef Register
Analog Domain Register		
ADCL_REG	0x0300	ADCL Analog Control Register
DAC_REG	0x0310	DAC Analog Control Register
MICBIAS_REG	0x0318	MICBIAS Analog Control Register
BIAS_REG	0x0320	BIAS Analog Control Register

9.2.6. Register Description

9.2.6.1. 0x0000 DAC Digital Part Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EN_DA DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA DWA Function Disable

			0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital volume control: DVC, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step
11:1	/	/	/
0	R/W	0x0	HUB_EN Audio Hub Enable 0: Disable 1: Enable

9.2.6.2. 0x0010 DAC FIFO Control Register(Default Value: 0x0000_4000)

Offset: 0x0010			Register Name: AC_DAC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	DAC_FS Sample Rate of DAC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: 192 kHz 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: 96 kHz 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO underrun 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 20-bit transmitted audio sample: 00/10: FIFO_I[19:0] = {TXDATA[31:12]} 01/11: FIFO_I[19:0] = {TXDATA[19:0]}

			For 16-bit transmitted audio sample: 00/10: FIFO_I[19:0] = {TXDATA[31:16], 4'b0} 01/11: FIFO_I[19:0] = {TXDATA[15:0], 4'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO available room is less than or equal N, DRQ Request will be de-asserted. N is defined here: 00: IRQ/DRQ De-asserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ generated when WLEVEL ≤ TXTL **Note: WLEVEL represents the number of valid samples in the TX FIFO.** **Only TXTL[6:0] valid when TXMODE = 0**
7	/	/	/
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data.
5	R/W	0x0	TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Underrun IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/WC	0x0	FIFO_FLUSH

			DAC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

9.2.6.3. 0x0014 DAC FIFO Status Register(Default Value: 0x0080_8008)

Offset: 0x0014			Register Name: AC_DAC_FIFOS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
2	R/W1C	0x0	TXU_INT TX FIFO Underrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Underrun Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

9.2.6.4. 0x0020 DAC TX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

9.2.6.5. 0x0024 DAC TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: AC_DAC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **Note: It is used for Audio/Video Synchronization**

9.2.6.6. 0x0028 DAC Debug Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_DAC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT DAC Pattern Select 00: Normal (Audio Sample from TX FIFO) 01: -6 dB Sin wave 10: -60 dB Sin wave 11: Silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC Clock from PLL 1: CODEC Clock from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC Output Channel Swap Enable 0:Disable 1:Enable
5:3	/	/	/
1:0	R/W	0x0	ADDA_LOOP_MODE ADDA Loop Mode Select 00: Disable 01: ADDA LOOP MODE DACL connect to ADCL 1X:Reserved

9.2.6.7. 0x0030 ADC FIFO Control Register(Default Value: 0x0000_0400)

Offset: 0x0030			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48 kHz 010: 24 kHz 100: 12 kHz 110: Reserved 001: 32 kHz 011: 16 kHz 101: 8 kHz 111: Reserved 44.1 kHz/22.05 kHz/11.025 kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable
27:26	R/W	0x0	ADCFDT ADC FIFO delay time for writing data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms
25	R/W	0x0	ADCDFEN ADC FIFO delay function for writing data after EN_AD 0: Disable 1: Enable
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding ‘0’ at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 20-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[19:0], 12’h0} Mode 1: RXDATA[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0]} For 16-bit received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[19:4], 16’h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[19]}, FIFO_O[19:4]}
23:17	/	/	/
16	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits

15:13	/	/	/
12	R/W	0x0	ADC_CHANNEL_EN ADCL enable
11	/	/	/
10:4	R/W	0x40	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL[5:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ generated when WLEVEL > RXTL[5:0] **Note: WLEVEL represents the number of valid samples in the RX FIFO.**
3	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
0	R/W1C	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'.

9.2.6.8. 0x0038 ADC FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: AC_ADC_FIFOS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:15	/	/	/
14:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W1C	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

2	/	/	/
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

9.2.6.9. 0x0040 ADC RX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

9.2.6.10. 0x0044 ADC RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **Note: It is used for Audio/Video Synchronization.**

9.2.6.11. 0x004C ADC Debug Register (Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	AD_SWP ADC output channel swap enable (for digital filter) 0: Disable 1: Enable
23:0	/	/	/

9.2.6.12. 0x00F0 DAC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: AC_DAC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDAP_EN DAP for DRC Enable 0: Bypass 1: Enable
30	/	/	/
29	R/W	0x0	DDAP_DRC_EN DRC enable control 0: Disable 1: Enable
28	R/W	0x0	DDAP_HPF_EN HPF enable control 0: Disable 1: Enable
27:0	/	/	/

9.2.6.13. 0x00F8 ADC DAP Control Register (Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: AC_ADC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_DAP0_EN DAP for ADC enable(Two DRC can use the same parameter) 0:Bypass 1:Enable
30	/	/	/
29	R/W	0x0	ADC_DRC0_EN ADC DRC0 enable control 0:Disable 1:Enable
28	R/W	0x0	ADC_HPF0_EN ADC HPF0 enable control 0:Disable 1:Enable
27:0	/	/	/

9.2.6.14. 0x0100 DAC DRC High HPF Coef Register (Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**

31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.2.6.15. 0x0104 DAC DRC Low HPF Coef Register (Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

9.2.6.16. 0x0108 DAC DRC Control Register (Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enabled and the drc funciton is disabled. After disabled drc function and this bit goes to 0, the user should write the drc delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc is disabled and the drc buffer data output completely. 0: Don't use the buffer 1: Use the buffer
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable
5	R/W	0x0	DRC gain min limit enable When this function is enabled, it will overwrite the noise detect funciton. 0: Disable 1: Enable

4	R/W	0x0	Control the drc to detect noise when ET enable 0: Disable 1: Enable
3	R/W	0x0	Signal function select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT /AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0: Disable 1: Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0: Disable 1: Enable When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0: Disable 1: Enable When the bit is disabled, Ke and OPE parameter is unused.

9.2.6.17. 0x010C DAC DRC Left Peak Filter High Attack Time Coef Register (Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(The default value is 1ms)

9.2.6.18. 0x0110 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24.(The default value is 1ms)

9.2.6.19. 0x0118 DAC DRC Left Peak Filter Low Attack Time Coef Register (Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

9.2.6.20. 0x011C DAC DRC Left Peak Filter High Release Time Coef Register (Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

9.2.6.21. 0x0120 DAC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

9.2.6.22. 0x012C DAC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.2.6.23. 0x0130 DAC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description

31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.2.6.24. 0x013C DAC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (The default value is -40dB)

9.2.6.25. 0x0140 DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24 (The default value is -40dB)

9.2.6.26. 0x0144 DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0080	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is 2 : 1)

9.2.6.27. 0x0148 DAC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is 2 : 1)

9.2.6.28. 0x014C DAC DRC Compressor High Output at Compressor Threshold Register (Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor, which is determined by the equation -OPC/6.0206. The format is 8.24 (The default value is -40dB)

9.2.6.29. 0x0150 DAC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0150			Register Name: AC_DAC_DRC_LOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor, which is determined by the equation OPC/6.0206. The format is 8.24 (The default value is -40dB)

9.2.6.30. 0x0154 DAC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (The default value is -10dB)

9.2.6.31. 0x0158 DAC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206. The format is 8.24. (The default value is -10dB)

9.2.6.32. 0x015C DAC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0005	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24.

			(The default value is <50 :1>)

9.2.6.33. 0x0160 DAC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.2.6.34. 0x0164 DAC DRC Limiter High Output at Limiter Threshold Register(Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24 (The default value is -25dB)

9.2.6.35. 0x0168 DAC DRC Limiter Low Output at Limiter Threshold Register(Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24 (The default value is -25dB)

9.2.6.36. 0x016C DAC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

9.2.6.37. 0x0170 DAC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

9.2.6.38. 0x0174 DAC DRC Expander Slope High Setting Register(Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.2.6.39. 0x0178 DAC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.2.6.40. 0x017C DAC DRC Expander High Output at Expander Threshold Register(Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24 (The default value is -70dB)

9.2.6.41. 0x0180 DAC DRC Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24 (The default value is -70dB)

9.2.6.42. 0x0184 DAC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (The default value is <1:1>)

9.2.6.43. 0x0188 DAC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (The default value is <1:1>)

9.2.6.44. 0x018C DAC DRC Smooth Filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.2.6.45. 0x0190 DAC DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.2.6.46. 0x0194 DAC DRC Smooth Filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description

31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.2.6.47. 0x0198 DAC DRC Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.2.6.48. 0x019C DAC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (The default value is -10dB)

9.2.6.49. 0x01A0 DAC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (The default value is -10dB)

9.2.6.50. 0x01A4 DAC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.2.6.51. 0x01A8 DAC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting, which is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.2.6.52. 0x01AC DAC DRC Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

9.2.6.53. 0x01B0 DAC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which are determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

9.2.6.54. 0x01B8 DAC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.2.6.55. 0x01BC DAC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.2.6.56. 0x0200 ADC DRC High HPF Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.2.6.57. 0x0204 ADC DRC Low HPF Coef Register(Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

9.2.6.58. 0x0208 ADC DRC Control Register(Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enabled and the drc funciton is disabled. After disabled drc function and this bit goes to 0, the user should write the drc delay function bit to 0. 0: Not completed 1: Completed
14:10	/	/	/
13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disabled, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc is disabled and the drc buffer data output completely. 0: Don't use the buffer 1: Use the buffer
6	R/W	0x0	DRC gain max limit enable 0: Disable 1: Enable

5	R/W	0x0	DRC gain min limit enable. When this fuction is enabled, it will overwrite the noise detect funciton. 0: Disable 1: Enable
4	R/W	0x0	Control the drc to detect noise when ET is enabled 0: Disable 1: Enable
3	R/W	0x0	Signal function select 0: RMS filter 1: Peak filter When signal function selects Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT/AC_DRC_LRMSLAT/AC_DRC_LRMSHAT/AC_DRC_LRMSLAT) When signal function selects RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT/AC_DRC_LPFLAT/AC_DRC_RPFHAT/AC_DRC_RPFLAT /AC_DRC_LPFHRT/AC_DRC_LPFLRT/AC_DRC_RPFHRT/AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0: Disable 1: Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0: Disable 1: Enable When the bit is disabled, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0: Disable 1: Enable When the bit is disabled, Ke and OPE parameter is unused.

9.2.6.59. 0x020C ADC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

9.2.6.60. 0x0210 ADC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (The default value is 1ms)

9.2.6.61. 0x021C ADC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

9.2.6.62. 0x0220 ADC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which is determined by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (The default value is 100ms)

9.2.6.63. 0x022C ADC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.2.6.64. 0x0230 ADC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (The default value is 10ms)

9.2.6.65. 0x023C ADC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

9.2.6.66. 0x0240 ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which is set by the equation that CTin = -CT/6.0206. The format is 8.24. (The default value is -40dB)

9.2.6.67. 0x0244 ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0080	The slope of the compressor which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is <2 : 1>)

9.2.6.68. 0x0248 ADC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor, which is determined by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (The default value is <2 : 1>)

9.2.6.69. 0x024C ADC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor, which is determined by the equation

			-OPC/6.0206 The format is 8.24. (The default value is -40dB)

9.2.6.70. 0x0250 ADC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor, which is determined by the equation OPC/6.0206 The format is 8.24 (The default value is -40dB)

9.2.6.71. 0x0254 ADC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (The default value is -10dB)

9.2.6.72. 0x0258 ADC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which is set by the equation that LTin = -LT/6.0206, The format is 8.24. (The default value is -10dB)

9.2.6.73. 0x025C ADC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.2.6.74. 0x0260 ADC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter, which is determined by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (The default value is <50 :1>)

9.2.6.75. 0x0264 ADC DRC Limiter High Output at Limiter Threshold Register(Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter, which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25dB)

9.2.6.76. 0x0268 ADC DRC Limiter Low Output at Limiter Threshold Register(Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter which is determined by equation OPT/6.0206. The format is 8.24. (The default value is -25dB)

9.2.6.77. 0x026C ADC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

9.2.6.78. 0x0270 ADC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which is set by the equation that ETin = -ET/6.0206, The format is 8.24. (The default value is -70dB)

9.2.6.79. 0x0274 ADC DRC Expander Slope High Setting Register(Default Value:0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0500	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.2.6.80. 0x0278 ADC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander, which is determined by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (The default value is <1:5>)

9.2.6.81. 0x027C ADC DRC Expander High Output at Expander Threshold Register(Default Value:0x0000_F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70dB)

9.2.6.82. 0x0280 ADC DRC Expander Low Output at Expander Threshold Register(Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander, which is determined by equation OPE/6.0206. The format is 8.24. (The default value is -70dB)

9.2.6.83. 0x0284 ADC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0284			Register Name: AC_ADC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0100	The slope of the linear, which is determined by the equation that Kn = 1/R,

			there, R is the ratio of the linear, which always is interger . The format is 8.24. (The default value is <1:1>)

9.2.6.84. 0x0288 ADC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: AC_ADC_DRC_LKN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear, which is determined by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (The default value is <1:1>)

9.2.6.85. 0x028C ADC DRC Smooth Filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x028C			Register Name: AC_ADC_DRC_SFHAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.2.6.86. 0x0290 ADC DRC Smooth Filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0290			Register Name: AC_ADC_DRC_SFLAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which is determined by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 5ms)

9.2.6.87. 0x0294 ADC DRC Smooth Filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: AC_ADC_DRC_SFHRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.2.6.88. 0x0298 ADC DRC Smooth Filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 200ms)

9.2.6.89. 0x029C ADC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (The default value is -10dB)

9.2.6.90. 0x02A0 ADC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (The default value is -10dB)

9.2.6.91. 0x02A4 ADC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting, which is determined by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.2.6.92. 0x02A8 ADC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting, which is determined by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (The default value is -40dB)

9.2.6.93. 0x02AC ADC DAP Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

9.2.6.94. 0x02B0 ADC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which is determined by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (The default value is 30ms)

9.2.6.95. 0x02B8 ADC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting, which format is 3.24.(gain = 1)

9.2.6.96. 0x02BC ADC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting, which format is 3.24.(gain = 1)

9.2.6.97. 0x0300 ADCL Analog Control Register0(Default Value: 0x000C_0055)

Offset: 0x0300			Register Name: ADCL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ADCLEN ADCL Channel Enable

			0: Disable 1: Enable
30	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0:Disable 1:Enable
29	R/W	0x0	Dither Reset 0: New dither off 1: New dither on
28:24	/	/	/
23	R/W	0x0	LINEINLEN LINEINL Enable 0:Disable 1:Enable
22	R/W	0x0	LINEINLG LINEINL Gain 0:0dB 1:6dB
21:20	R/W	0x1	IOPLINE PGA LINEIN Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
19:18	R/W	0x3	PGA_CTRL_RCM PGA Common Mode Input Impedance Control for MIC-IN(The AC coupling capacitor of Mic-in is 100nF, the AC coupling capacitor and common-mode input resistance cooperate to high filter, the corresponding cut-off frequency is 20Hz~80Hz. 00 : 100 kΩ 01 : 75 kΩ 10 : 50 kΩ 11 : 25 kΩ
17:16	R/W	0x0	PGA_IN_VCM_CTRL High gain microphone input common mode voltage control(The gain is greater than or equal to 8dB) 00 : 900mV 01 : 750mV 10 : 800mV 11 : 700mV
15:13	/	/	/
12:8	R/W	0x0	PGA_GAIN_CTRL PGA Gain Setting Control for MICIN 0 : 0 dB 16 : 21 dB 1 : 6 dB 17 : 22 dB

			2 : 6 dB 18 : 23 dB 3 : 6 dB 19 : 24 dB 4 : 9 dB 20 : 25 dB 5 : 10 dB 21 : 26 dB 6 : 11 dB 22 : 27 dB 7 : 12 dB 23 : 28 dB 8 : 13 dB 24 : 29 dB 9 : 14 dB 25 : 30 dB 10 : 15 dB 26 : 31 dB 11 : 16 dB 27 : 32 dB 12 : 17 dB 28 : 33 dB 13 : 18 dB 29 : 34 dB 14 : 19 dB 30 : 35 dB 15 : 20 dB 31 : 36 dB
7:6	R/W	0x1	IOPAAFL ADCL OP AAF Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
5:4	R/W	0x1	IOPSDML1 ADCL OP SDM Bias Current Select1 00: 6uA 01: 7uA 10: 8uA 11: 9uA
3:2	R/W	0x1	IOPSDML2 ADCL OP SDM Bias Current Select2 00: 6uA 01: 7uA 10: 8uA 11: 9uA
1:0	R/W	0x1	IOPMICL PGA OPMIC Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA

9.2.6.98. 0x0310 DAC Analog Control Register(Default Value: 0x0015_0000)

Offset: 0x0310			Register Name: DAC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

23	R/W	0x0	CURRENT_TEST_SELECT Internal Current Sink Test Enable (from LINEOUTL pin) 0: Normal 1: For Debug
22	/	/	/
21:20	R/W	0x1	IOPVRS VRA2 Buffer OP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
19:18	R/W	0x1	ILINEOUTAMPS LINEOUTL/R AMP Bias Current Select 00: 6uA 01: 7uA 10: 8uA 11: 9uA
17:16	R/W	0x1	IOPDACS OPDAC Bias Current Select 00: 7uA 01: 8uA 10: 9uA 11: 10uA
15	R/W	0x0	DACEN DAC Enable 0: Disable 1: Enable
14	/	/	/
13	R/W	0x0	LINEOUTLEN Left Channel LINEOUT Enable 0: Disable 1: Enable
12	R/W	0x0	LMUTE DACL to Left Channel LINEOUT Mute Control 0: Mute 1: Not mute
11:7	/	/	/
6	R/W	0x0	LINEOUTLDIFFEN Left Channel LINEOUT Output Control 0: Single-End 1: Differential
5	/	/	/
4:0	R/W	0x0	LINEOUT Volume Control, Total 30 level from 0x1F to 0x02 with the volume 0dB to -43.5dB, -1.5dB/step, mute when 00000 & 00001.

9.2.6.99. 0x0318 MICBIAS Analog Control Register(Default Value: 0x0000_0030)

Offset: 0x0318			Register Name: MICBIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	MMICBIASEN Master Microphone Bias Enable 0: Disable 1: Enable
6:5	R/W	0x1	MBIASSEL MMICBIAS Voltage Level Select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V
4	R/W	0x1	MMIC BIAS chopper enable 0: Disable 1: Enable
3:2	R/W	0x0	MMIC BIAS chopper clock select 00: 250kHz 01: 500kHz 10: 1MHz 11: 2MHz
1:0	/	/	/

9.2.6.100. 0x0320 BIAS Analog Control Register(Default Value: 0x0000_0080)

Offset: 0x0320			Register Name: BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x80	BIASDATA Bias Current Register Setting Data The field can not be controlled by Audio Codec module, only controlled by system BUS reset.

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Chapter 10 ISP

10.1. Overview

The ISP module supports real time image process for RAW sensor. The main functions are as follows.

- Crop
- Black level correction(BLC)
- Linearity correction
- Digital gain
- WDR stitching
- Defect pixel correction(DPC)
- Crosstalk correction
- Global chromatic aberration correction(GCA)
- 2D denoise filter
- 3D denoise filter
- White balance(WB)
- Lens shading correction(LSC)
- WDR BE
- Pixel-by-pixel local tone mapping(PLTM)
- Bayer interpolation
- Local chromatic aberration correction(LCA)
- Sharpening
- Color matrix
- Chrominance noise reduction(CNR)
- Saturation adjust
- RGB Dynamic range compression(DRC)
- RGB Gamma correction
- RGB2YCbCr
- Color enhance management
- 3A statistic output
- Anti-flick detection statistics
- Histogram statistics
- Line Buffer Compress

The processing capability of the ISP module is as follows.

- Supports 8/10/12 bits RAW data input
- Maximum picture resolution of 2688x2688
- Minimum picture resolution of 256x128
- Maximum frame rate of 2592x1936@30fps
- Minimum horizontal blanking region of 96 pixels
- Minimum vertical blanking region of 40 lines

10.2. Block Diagram

The block diagram of the ISP module is as follows.

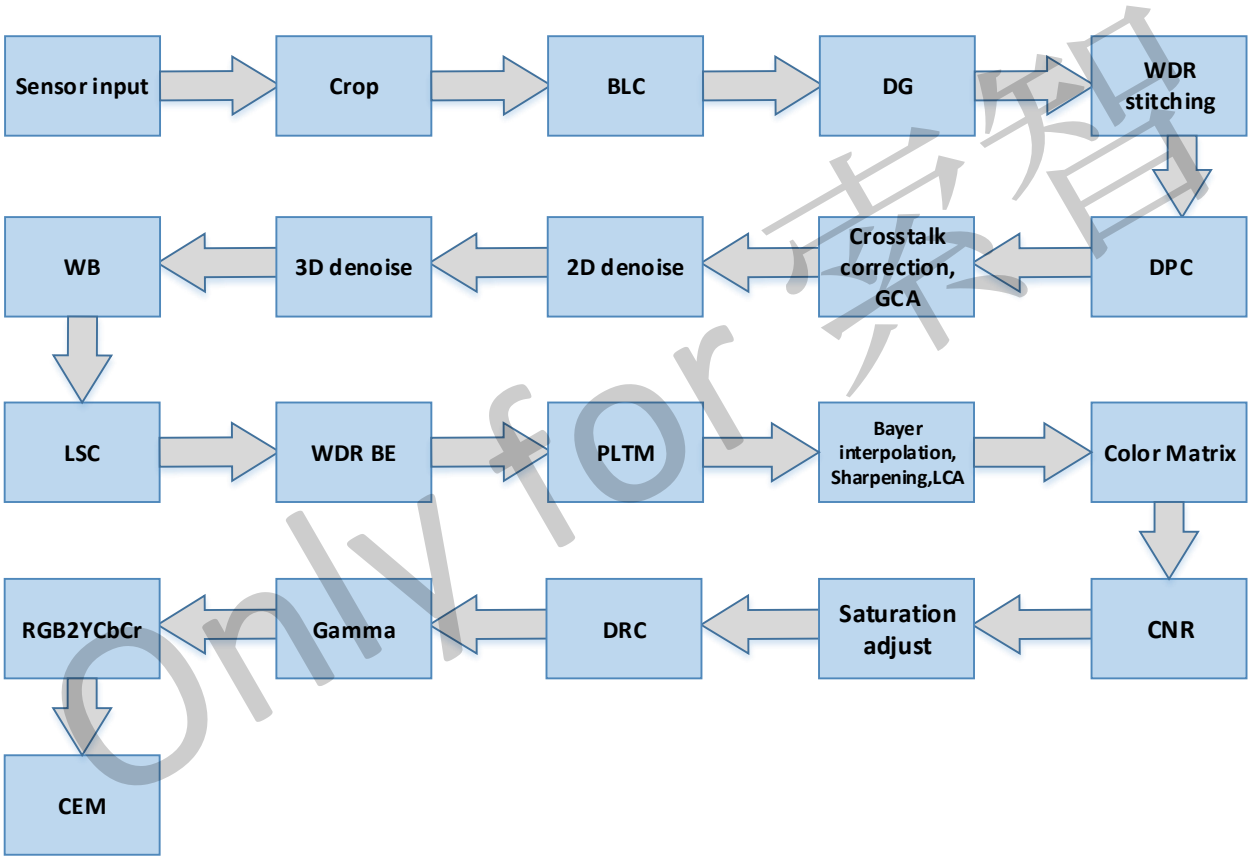

Figure 10- 1. ISP Block Diagram

10.3. Module Functions

10.3.1. Crop

The Crop module, which can crop the input picture, is often used to change the aspect ratio of the input picture or extract the region of interest for a picture. For details about the configuration methods, see the <<*image sensor light guide*>>.

10.3.2. BLC

The BLC module adds respectively offset for four Bayer color channels(R, Gr, Gb, and B), to perform optical black correction. The precision of the offset is S13. The module is usually used for wide dynamic sensor.

10.3.3. Digital Gain

The Digital Gain module provides the digital gain, and supports U16Q10-precision.

10.3.4. WDR

The WDR module supports 2-frame combination WDR function.

10.3.5. DPC

The DPC module is used to correct defect pixels in Bayer field. It supports correct the type of defective pixel: Singlet dead pixel; doublet dead pixel in 5x5 kernel; and other cluster of defect pixel.

10.3.6. Crosstalk Correction

The Crosstalk Correction module is used to remove abnormal picture question when Gr and Gb imbalance. Usually, the module is used when sensor CRA unmatches lens CRA.

10.3.7. GCA

The GCA module is used to correction of Lateral Chromatic Aberration, which is one of the common optical defects of camera lens.

10.3.8. 2D De-noise

The 2D De-noise module restrains sensor noises in the Bayer field to improve picture quality.

10.3.9. 3D De-noise

The 3D De-noise module implements inter-frame filtering for sensor noises in the time domain to improve picture quality.

10.3.10. WB

The WB Correction module adds respectively gain for four channels(R, Gr ,Gb, and B) to implement white balance correction. The precision of the gain is U12Q8.

10.3.11. LSC

The LSC module implements lens shading correction. It supports two way of mesh(MSC) and radio(RSC), which interpolate the shading correction coefficient by the radio distance and pixel block statistics.

10.3.12. WDR BE

Same as WDR.

10.3.13. PLTM

The PLTM module adjusts the dynamic range of picture. The module adjust the luminance and contrast through histogram statistic of picture, to improve picture quality.

10.3.14. Bayer Interpolation

The module interpolates Bayer field pixel to RGB field while holding clear picture edge and restraining pseudo color.

10.3.15. Sharpen

The Sharpen module implements picture edge sharpening to improve picture edge information, while picture contour is much clearer.

10.3.16. LCA

The LCA module is used to correction of Axial Chromatic Aberration, which is one of the common optical defects of camera lens.

10.3.17. Color Matrix

The Color Matrix module applies a 3x3 color gain matrix and a 3x1 offset matrix on the input R/G/B pixels to restore image color. The precision of each value in gain matrix is S12Q8 and the precision of each value in offset matrix is S13.

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} g_{rr} & g_{gr} & g_{br} \\ g_{rg} & g_{gg} & g_{bg} \\ g_{rb} & g_{gb} & g_{bb} \end{pmatrix} \times \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

10.3.18. CNR

The CNR module is used to reduce chroma noise in RGB domain.

10.3.19. SATU

Saturation adjust module is used to adjust the saturation of image.

10.3.20. DRC

The DRC module performs a gamma correction for each color in the RGB color space.

10.3.21. Gamma

The Gamma module applies gamma correction for each color channel(R,G,and B) through looking-up table. Each gamma table has 256 entries and the precision is U12.

10.3.22. RGB2YCrCb

The RGB2YCrCb module convert RGB color space to YCbCr color space using a 3x3 square matrix with an added offset. Each gain range is U10Q10 precision.

10.3.23. CEM

The CEM module adjusts hue and saturation of picture in YUV field, and enhances or restrains specific colors such as blue sky, plant and complexion based on user preference.

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Chapter 11 Interfaces

11.1. TWI

11.1.1. Overview

The TWI is designed as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including slave and master. The communication of the 2-wire bus is carried out by a byte-wise mode based on interrupt or polled handshaking. The TWI can be operated in standard mode (100kbit/s) or fast-mode (400kbit/s). The 10-bit addressing mode is supported for this specified application. General call addressing is also supported in slave mode.

The TWI has the following features:

- Software-programmable for slave or master
- Supports repeated START signal
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Supports speed up to 400kbit/s ('fast mode')
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in master mode

NOTE

V833 supports 5 TWI interfaces; V831 supports 4 TWI interfaces.

11.1.2. Block Diagram

Figure 11-1 shows the block diagram of TWI.

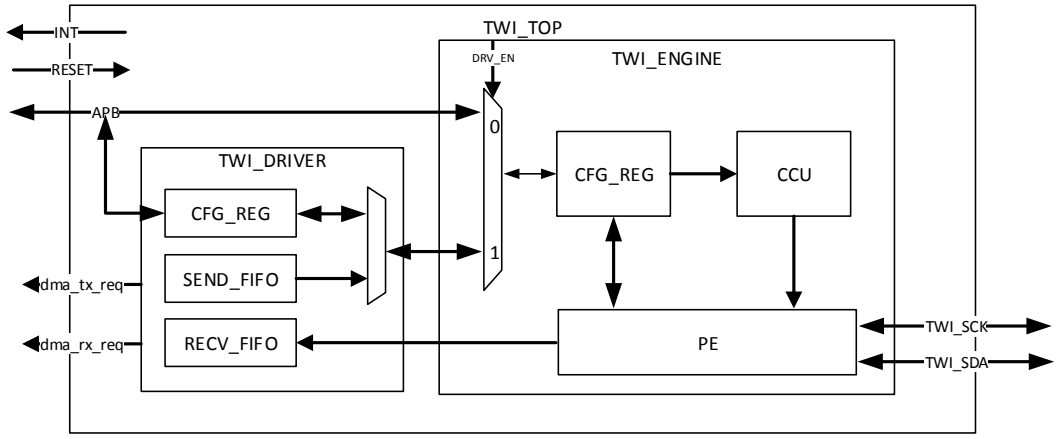

Figure 11- 1. TWI Block Diagram

RESET: Module reset signal

INT: Module output interrupt signal

CFG_REG: Module configuration register in TWI

PE: Packet encoding/decoding

CCU: Module clock controller unit

11.1.3. Operations and Functional Descriptions

11.1.3.1. External Signals

The TWI controller has 5 TWIs. Table 11-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O, when TWI is configured as master device, TWI_SCK is output pin; when TWI is configurable as slave device, TWI_SCK is input pin. The unused TWI ports are used as General Purpose I/O ports. For information about General Purpose I/O ports, see **Port Controller** in chapter11.

Table 11- 1. TWI External Signals

V833 Signal	V831 Signal	Description	Type
TWI0_SCK	TWI0_SCK	TWI0 Clock Signal	I/O,OD
TWI0_SDA	TWI0_SDA	TWI0 Serial Data	I/O,OD
TWI1_SCK	TWI1_SCK	TWI1 Clock Signal	I/O,OD
TWI1_SDA	TWI1_SDA	TWI1 Serial Data	I/O,OD
TWI2_SCK	TWI2_SCK	TWI2 Clock Signal	I/O,OD
TWI2_SDA	TWI2_SDA	TWI2 Serial Data	I/O,OD
TWI3_SCK	TWI3_SCK	TWI3 Clock Signal	I/O,OD
TWI3_SDA	TWI3_SDA	TWI3 Serial Data	I/O,OD
S_TWI0_SCK	/	TWI0 Clock Signal in CPUS	I/O,OD
S_TWI0_SDA	/	TWI0 Serial Data in CPUS	I/O,OD

11.1.3.2. Clock Sources

Each TWI controller has a fixed clock source. Table 11-2 describes the clock source for TWI. Users can see **Clock Controller Unit(CCU)** in chapter3 and **Power Reset Clock Management(PRCM)** for clock setting, configuration and gating information.

Table 11- 2. TWI Clock Sources

Clock Sources	Description
APB2_CLK	TWI clock source in CPUX, for details on APB2 refer to CCU
APBS2_CLK	R-TWI clock in CPUS, for details on APBS2 refer to PRCM

After selected a proper clock, for using the TWI in CPUX, user must open the gating of TWI and release the reset bit. For using the TWI in CPUS, user also needs to open the gating of R-TWI and release the reset bit.

For more details on the gating/reset register, see CCU and PRCM specification**.**

11.1.3.3. Write/Read Timing in Standard and Extended Address Mode

Figure 11-2 describes the write timing in 7-bit standard address mode.

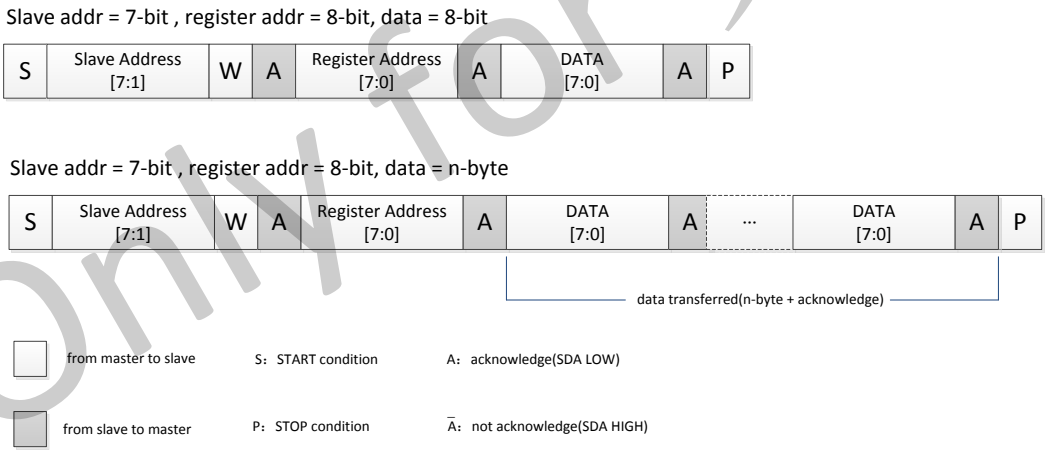

Figure 11- 2. 7-bit Standard Address Write Timing

Figure 11-3 describes the read timing in 7-bit standard address mode.

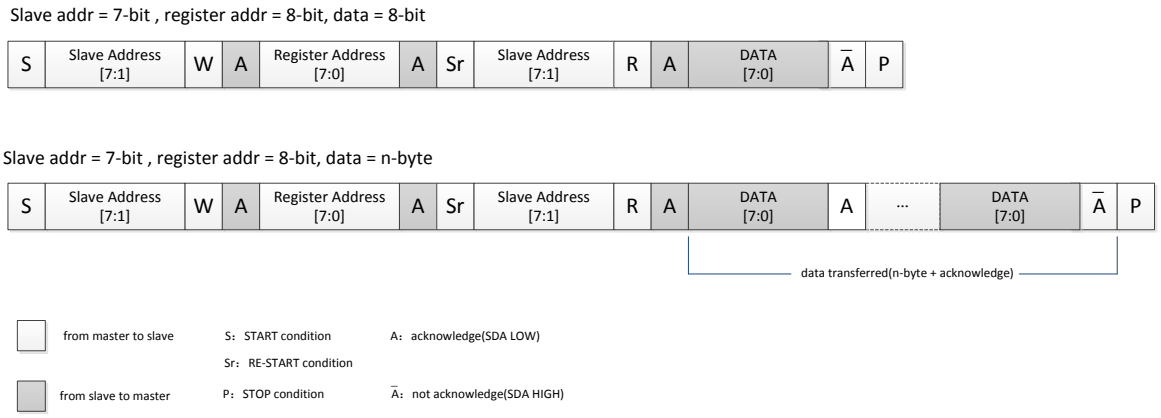

Figure 11- 3. 7-bit Standard Address Read Timing

Figure 11-4 describes the write timing in 10-bit extended address mode.

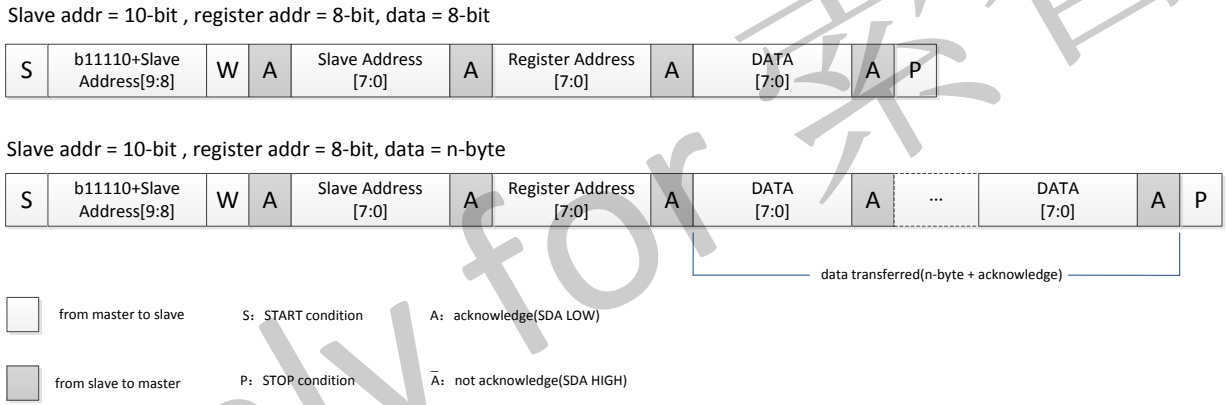

Figure 11- 4. 10-bit Extended Address Write Timing

Figure 11-5 describes the read timing in 10-bit extended address mode.

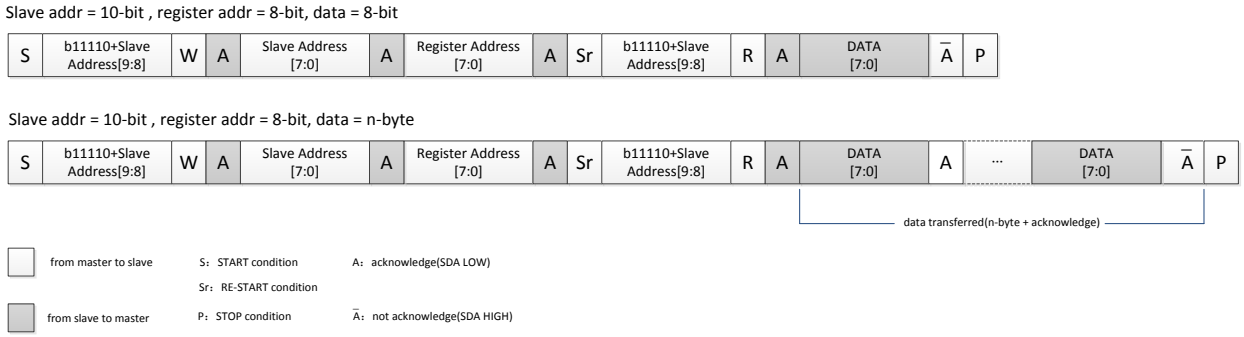

Figure 11- 5. 10-bit Extended Address Read Timing

11.1.3.4. Programming State Diagram

Figure 11-6 shows the TWI programming state diagram. For the value between two states, see TWI_STAT register in section 11.1.6.5.

M_SEND_S: master sends START signal;

M_SEND_ADDR: master sends slave address;

M_SEND_XADD: master sends slave extended address;

M_SEND_SR: master repeated start;

M_SEND_DATA: master sends data;

M_SEND_P: master sends STOP signal;

M_RECV_DATA: master receives data;

ARB_LOST: Arbitration lost;

C_IDLE: Idle;

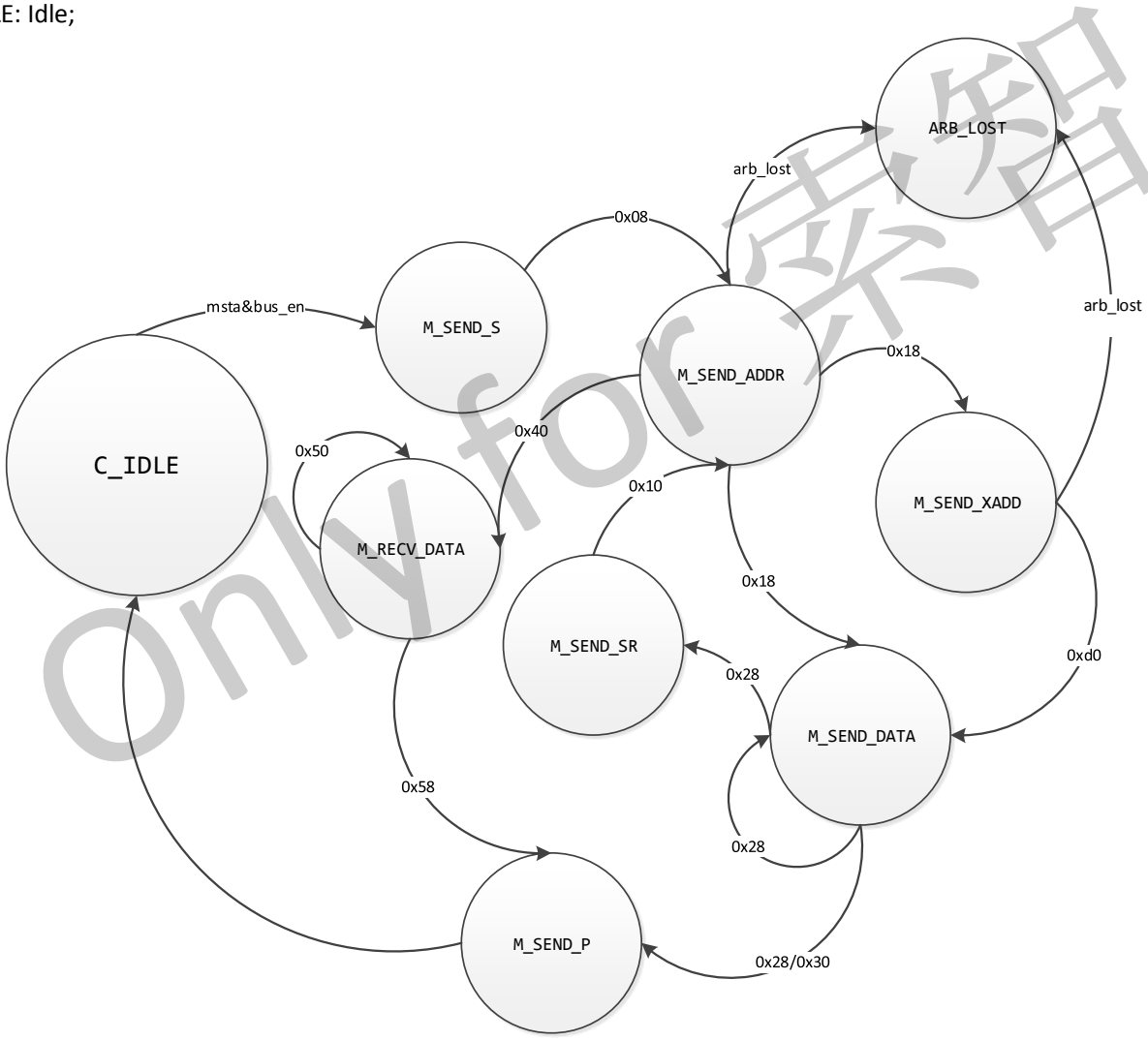

Figure 11- 6. TWI Programming State Diagram

11.1.3.5. TWI Engine Master and Slave Mode

There are four operation modes on the TWI bus. They are Master Transmit, Master Receive, Slave Transmit and Slave

Receive. In general, CPU host controls TWI engine by writing command and data to its registers. TWI engine transmits an interrupt to CPU when each time a byte transfer is done or a START/STOP command is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit of the TWI_CNTR register to high (before it must be low). The TWI engine will assert INT line and INT_FLAG to indicate a completion for the START command and each consequent byte transfer. At each interrupt, the micro-processor needs to check the TWI_STAT register for current status. A transfer has to be concluded with STOP command by setting M_STP bit to high.

In Slave mode, the TWI engine also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write TWI_DATA data register, and set the TWI_CNTR control register. After each byte transfer, a slave device always stop the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START command.

11.1.4. Programming Guidelines

The TWI controller operates in 8-bit data format. The data on the TWI_SDA line is always 8 bits long. At first, the TWI controller will sent a start condition. When in the addressing formats of 7-bit, TWI sends out one 8 bits message which includes 7 MSB slave address and 1 LSB read/write flag. The least significant of the salve address indicates the direction of transmission. When TWI works in 10-bit slave address mode, the operation will be divided into two steps, for details on the operation, see the register description in Section 11.1.6.1 and 11.1.6.2.

11.1.4.1. Initialization

To initialize the TWI, perform the following steps:

Step1 Configure corresponding GPIO multiplex function as TWI mode.

Step2 For TWIx, set TWI_BGR_REG[TWIx_GATING] in CCU module to 0 to close TWIx clock;
For R_TWIx, set R_TWI_BGR_REG[R_TWIx_GATING] in PRCM module to 0 to close R_TWIx clock.

Step3 For TWIx, set TWI_BGR_REG[TWIx_RST] in CCU module to 0, then set to 1 to reset TWIx;
For R_TWIx, set R_TWI_BGR_REG[R_TWIx_RST] in PRCM module to 0, then set to 1 to reset R_TWIx.

Step4 For TWIx, set TWI_BGR_REG[TWIx_GATING] in CCU module to 1 to open TWIx clock;
For R_TWIx, set R_TWI_BGR_REG[R_TWIx_GATING] in PRCM module to 1 to open R_TWIx clock.

Step5 Configure TWI_CCR[CLK_M] and TWI_CCR[CLK_N] to get the needed rate(The clock source of TWI is from APB2 or APBS2).

Step6 Configure TWI_CNTR[BUS_EN] and TWI_CNTR[A_ACK], when using interrupt, set TWI_CNTR[BUS_EN] to 1, and register system interrupt through GIC module. In slave mode, configure TWI_ADDR and TWI_XADDR registers to finish TWI initialization configuration.

For PRCM, see the description in ***V833/V831_PRCM_Specification***.

Figure 11-7 shows the process of TWI initialization.

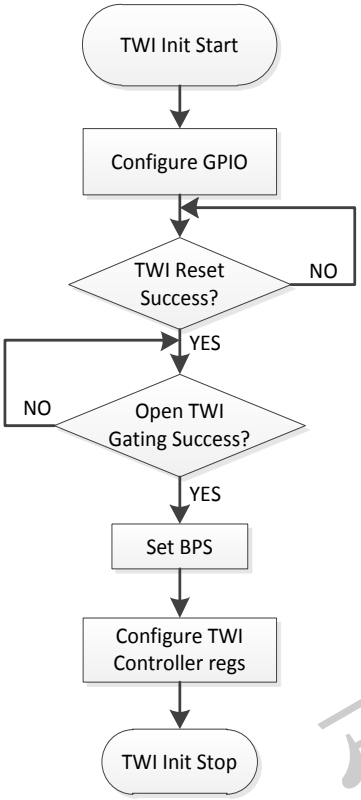

Figure 11- 7. TWI Initialization Process

11.1.4.2. Data Write Operation

To write data to device, perform the following steps:

Step1 Clear TWI_EFR register, and configure TWI_CNTR[M_STA] to 1 to transmit START signal.

Step2 After START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA(For 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step3 Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA(For 16-bit address, firstly write the first byte address, secondly write the second byte address).

Step4 Interrupt is triggered after data address transmission completes, write data to be transmitted to TWI_DATA(For consecutive write data operation, every byte transmission completion triggers interrupt, during interrupt write the next byte data to TWI_DATA).

Step5 After transmission completes, write TWI_CNTR[M_STP] to 1 to transmit STOP signal and end this write-operation.

Figure 11-8 shows the process of TWI write to device.

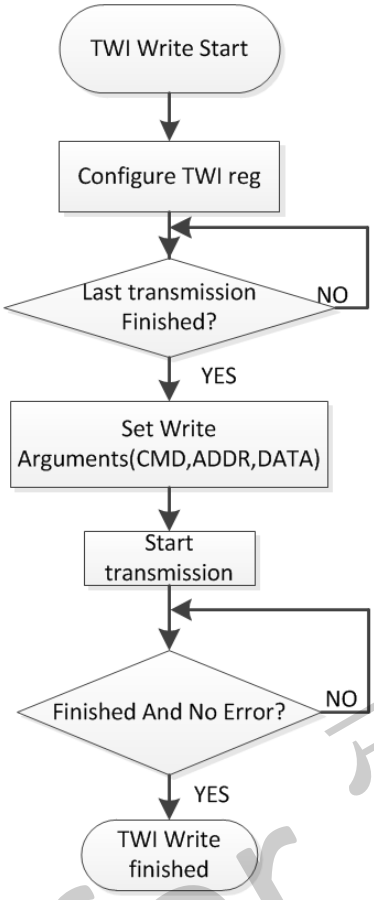

Figure 11- 8. TWI Write Data Process

11.1.4.3. Data Read Operation

To read data from device, perform the following steps:

Step1 Clear TWI_EFR register, set TWI_CNTR[A_ACK] to 1, and configure TWI_CNTR[M_STA] to 1 to transmit START signal.

Step2 After START signal is transmitted, the first interrupt is triggered, then write device ID to TWI_DATA(For 10-bit device ID, firstly write the first byte ID, secondly write the second byte ID in the next interrupt).

Step3 Interrupt is triggered again after device ID transmission completes, write device data address to be read to TWI_DATA(For 16-bit address, firstly write the first byte address, secondly write the second byte address).

Step4 Interrupt is triggered after data address transmission completes, write TWI_CNTR[M_STA] to 1 to transmit new START signal, and after interrupt triggers, write device ID to TWI_DATA to start read-operation.

Step5 After device address transmission completes, each receive completion will trigger interrupt, in turn, read TWI_DATA to get data, when receiving the previous interrupt of the last byte data, clear TWI_CNTR[A_ACK] to stop acknowledge signal of the last byte.

Step6 Write TWI_CNTR[M_STP] to 1 to transmit STOP signal and end this read-operation.

Figure 11-9 shows the process of TWI read from device.

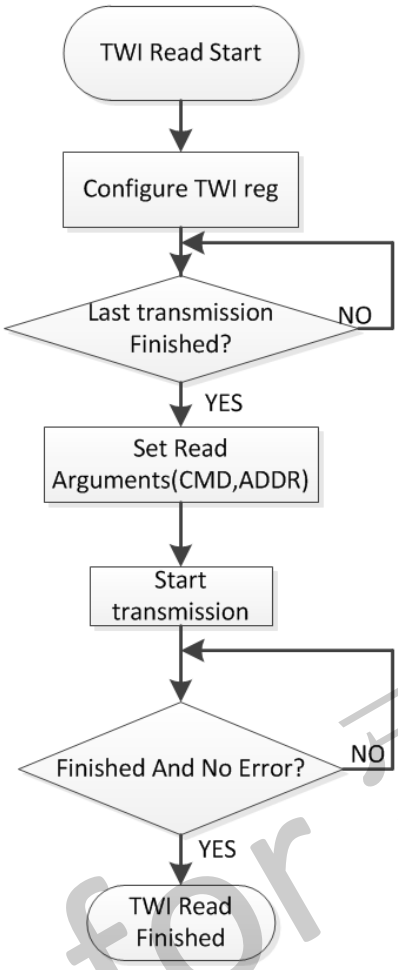

Figure 11- 9. TWI Read Data Process

11.1.4.4. Packet Transmission Operation

Figure 11-10 shows a software operation flow for packet transmission by TWI driver.

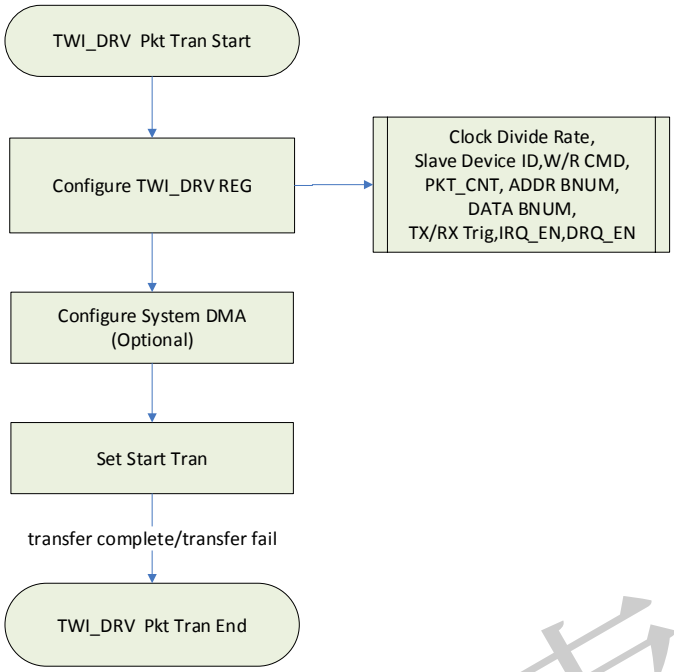

Figure 11- 10. TWI Driver Packet Transmission Process

11.1.5. Register List

Module Name	Base Address
TWI0	0x05002000
TWI1	0x05002400
TWI2	0x05002800
TWI3	0x05002C00
R-TWI0(only for V833)	0x07081400

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address
TWI_XADDR	0x0004	TWI Extended Slave Address
TWI_DATA	0x0008	TWI Data Byte
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register
TWI_DRV_CTRL	0x0200	TWI_DRV Control Register
TWI_DRV_CFG	0x0204	TWI_DRV Transmission Configuration Register

TWI_DRV_SLV	0x0208	TWI_DRV Slave ID Register
TWI_DRV_FMT	0x020C	TWI_DRV Packet Format Register
TWI_DRV_BUS_CTRL	0x0210	TWI_DRV Bus Control Register
TWI_DRV_INT_CTRL	0x0214	TWI_DRV Interrupt Control Register
TWI_DRV_DMA_CFG	0x0218	TWI_DRV DMA Configure Register
TWI_DRV_FIFO_CON	0x021C	TWI_DRV FIFO Content Register
TWI_DRV_SEND_FIFO_ACC	0x0300	TWI_DRV Send Data FIFO Access Register
TWI_DRV_RECV_FIFO_ACC	0x0304	TWI_DRV Receive Data FIFO Access Register

11.1.6. Register Description

11.1.6.1. 0x0000 TWI Slave Address Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:1	R/W	0x0	SLA Slave Address 7-bit addressing: SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing: 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General Call Address Enable 0: Disable 1: Enable

NOTE

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

11.1.6.2. 0x0004 TWI Extend Address Register(Default Value:0x0000_0000)

Offset: 0x0004	Register Name: TWI_XADDR

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

11.1.6.3. 0x0008 TWI Data Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte transmitted or received

11.1.6.4. 0x000C TWI Control Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus ISDA/ISCL is ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to call to its slave address – and to the general call address if the GCE bit in the ADDR register is set. **Note: In master operation mode, this bit should be set to '1'.**
5	R/WAC	0x0	M_STA Master Mode Start When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition has been sent. Writing a '0' to this bit has no effect.

4	R/W1C	0x0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will indicate if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the GCE bit in the ADDR register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

11.1.6.5. 0x0010 TWI Status Register(Default Value:0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

11.1.6.6. 0x0014 TWI Clock Register(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: TWI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N

			The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48 MHz (APB clock input) For 400 kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48 MHz/2^2=12 MHz, F1= F0/(10*(2+1)) = 0.4 MHz For 100 kHz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48 MHz/2^2=12 MHz, F1=F0/(10*(11+1)) = 0.1 MHz

11.1.6.7. 0x0018 TWI Soft Reset Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write ‘1’ to this bit to reset the TWI and clear to ‘0’ when completing Soft Reset operation.

11.1.6.8. 0x001C TWI Enhance Feature Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	DBN Data Byte Number Follow Read Command Control 00 : No data byte can be written after read command 01 : Only 1 byte data can be written after read command 10 : 2 bytes data can be written after read command 11 : 3 bytes data can be written after read command

11.1.6.9. 0x0020 TWI Line Control Register(Default Value:0x0000_003A)

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**

31:6	/	/	/
5	R	0x1	SCL_STATE Current State of TWI_SCL 0 : Low 1 : High
4	R	0x1	SDA_STATE Current State of TWI_SDA 0 : Low 1 : High
3	R/W	0x1	SCL_CTL TWI_SCL Line State Control Bit When line control mode is enabled (bit[2] set), this bit decides the output level of TWI_SCL. 0 : Output low level 1 : Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL Line State Control Enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0 : Disable TWI_SCL line control mode 1 : Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA Line State Control Bit When line control mode is enabled (bit[0] set), this bit decides the output level of TWI_SDA. 0 : Output low level 1 : Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA Line State Control Enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0 : Disable TWI_SDA line control mode 1 : Enable TWI_SDA line control mode

11.1.6.10. 0x0200 TWI_DRV Control Register(Default Value:0x00F8_1000)

Offset: 0x0200			**Register Name: TWI_DRV_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	START_TRAN 0: Transmission idle 1: Start transmission Automatically cleared to '0' when finished. If slave does not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. All format setting and data will be loaded from registers and FIFO when transmission start.

30	/	/	/
29	R/W	0x0	RESTART_MODE 0: RESTART 1: STOP+START Define the TWI_DRV action after sending register address.
28	R/W	0x0	READ_TRAN_MODE 0: send slave_id+W 1: do not send slave_id+W **Setting this bit to 1 if reading from a slave which register width is equal to 0**.
27:24	R	0x0	TRAN_RESULT 000: OK 001: FAIL Other: Reserved
23:16	R	0xf8	TWI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9th SCL clk Other: Reserved
15:8	R/W	0x10	TIMEOUT_N When sending the 9th clock, assert fail signal when slave device does not response after **N*F_{SCL}** cycles. And software must do a reset to TWI_DRV module and send a stop condition to slave.
7:2	/	/	/
1	R/W	0x0	SOFT_RESET 0: normal 1: reset
0	R/W	0x0	TWI_DRV_EN 0: Module disable 1: Module enable (only use in TWI Master Mode)

11.1.6.11. 0x0204 TWI_DRV Transmission Configuration Register(Default Value:0x0000_0001)

Offset: 0x0204	Register Name: TWI_DRV_CFG

Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	PKT_INTERVAL Define the interval between each packet for PKT_INTERVAL F_{SCL} cycles.
15:0	R/W	0x1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format.

11.1.6.12. 0x0208 TWI_DRV Slave ID Register(Default Value:0x0000_0000)

Offset: 0x0208			Register Name: TWI_DRV_SLV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:9	R/W	0x0	SLV_ID Slave device ID • 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 • 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
8	R/W	0x0	CMD R/W operation to slave device 0: write 1: read
7:0	R/W	0x0	SLV_ID_X SLAX[7:0], low 8 bits for slave device ID with 10-bit address

11.1.6.13. 0x020C TWI_DRV Packet Format Register(Default Value:0x0001_0001)

Offset: 0x020C			Register Name: TWI_DRV_FMT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x1	ADDR_BYTE How many bytes be sent as slave device reg address 0~255
15:0	R/W	0x1	DATA_BYTE How many bytes be sent/received as data 1~65535

11.1.6.14. 0x0210 TWI_DRV Bus Control Register(Default Value:0x0000_00C0)

Offset: 0x0210			Register Name: TWI_DRV_BUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/

14:12	R/W	0x0	CLK_N TWI_DRV bus sampling clock F0=24MHz/2^CLK_N
11:8	R/W	0x0	CLK_M TWI_DRV output SCL frequency is F_{SCL}=F1/10=(F0/(CLK_M+1))/10
7	R	0x1	SCL_STA SCL current status
6	R	0x1	SDA_STA SDA current status
5:4	/	/	/
3	R/W	0x0	SCL_MOV SCL manual output value
2	R/W	0x0	SDA_MOV SDA manual output value
1	R/W	0x0	SCL_MOE SCL manual output en
0	R/W	0x0	SDA_MOE SDA manual output en

11.1.6.15. 0x0214 TWI_DRV Interrupt Control Register(Default Value:0x0000_0000)

Offset: 0x0214			**Register Name: TWI_DRV_INT_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
19	R/W	0x0	RX_REQ_INT_EN
18	R/W	0x0	TX_REQ_INT_EN
17	R/W	0x0	TRAN_ERR_INT_EN
16	R/W	0x0	TRAN_COM_INT_EN
15:4	/	/	/
3	R/W1C	0x0	RX_REQ_PD Set when the data byte number in RECV_FIFO reaches RX_TRIG
2	R/W1C	0x0	TX_REQ_PD Set when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO
1	R/W1C	0x0	TRAN_ERR_PD Packet transmission failed pending
0	R/W1C	0x0	TRAN_COM_PD Packet transmission completed pending

11.1.6.16. 0x0218 TWI_DRV DMA Configure Register(Default Value:0x0010_0010)

Offset: 0x0218			**Register Name: TWI_DRV_DMA_CFG**
Bit	**Read/Write**	**Default/Hex**	**Description**

31:25	/	/	/
24	R/W	0x0	DMA_RX_EN
23:22	/	/	/
21:16	R/W	0x10	RX_TRIG When DMA_RX_EN set, send DMA RX Req when the data byte number in RECV_FIFO reaches RX_TRIG or Read Packet Transmission completed with RECV_FIFO not empty
15:9	/	/	/
8	R/W	0x0	DMA_TX_EN
7:6	/	/	/
5:0	R/W	0x10	TX_TRIG When DMA_TX_EN set, send DMA TX Req when there is no less than DMA_TX_TRIG empty byte number in SEND_FIFO

11.1.6.17. 0x021C TWI_DRV FIFO Content Register(Default Value:0x0000_0000)

Offset: 0x021C			**Register Name: TWI_DRV_FIFO_CON**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/WAC	0x0	RECV_FIFO_CLEAR Set this bit to clear RECV_FIFO pointer, and this bit is cleared automatically
21:16	R	0x0	RECV_FIFO_CONTENT The number of data in RECV_FIFO
15:7	/	/	/
6	R/WAC	0x0	SEND_FIFO_CLEAR Set this bit to clear SEND_FIFO pointer, and this bit is cleared automatically
5:0	R	0x0	SEND_FIFO_CONTENT The number of data in SEND_FIFO

11.1.6.18. 0x0300 TWI_DRV Send Data FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0300			**Register Name: TWI_DRV_SEND_FIFO_ACC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	SEND_DATA_FIFO Address of a 32x8 SEND_FIFO ,which stores reg address and data sending to slave device

11.1.6.19. 0x0304 TWI_DRV Receive Data FIFO Access Register(Default Value:0x0000_0000)

Offset: 0x0304	**Register Name: TWI_DRV_RECV_FIFO_ACC**

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RECV_DATA_FIFO Address of a 32x8 RECV_FIFO ,which stores data received from slave device

11.2. UART

11.2.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in system where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART has the following features:

- Compatible with industry-standard 16550 UARTs
- 256 bytes transmit and receive data FIFOs
- Capable of speed up to 5Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

11.2.2. Block Diagram

Figure 11-11 shows a block diagram of the UART.

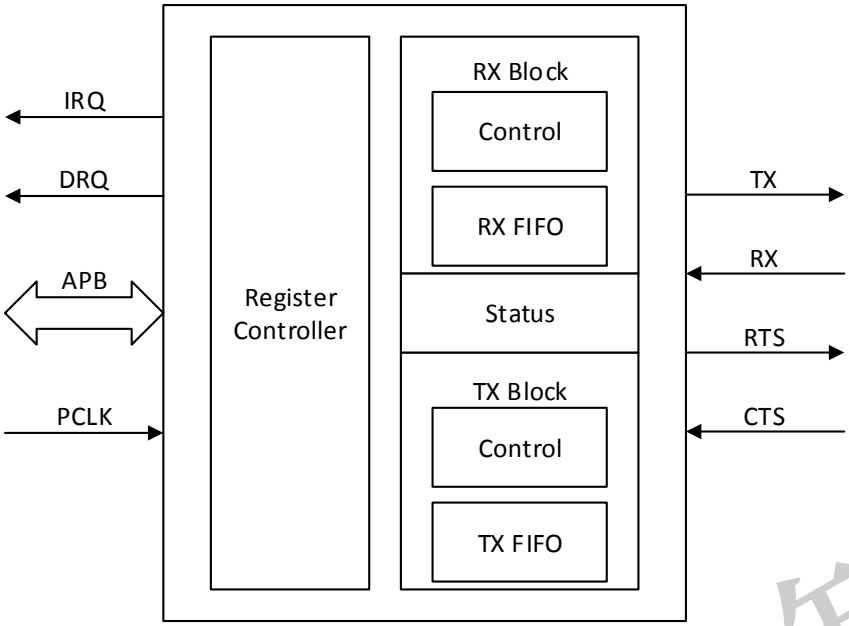

Figure 11- 11. UART Block Diagram

11.2.3. Operations and Functional Descriptions

11.2.3.1. External Signals

Table 11-3 describes the external signals of UART.

Table 11- 3. UART External Signals

Signal	Type	Description
UART0_TX	O	UART0 Data Transmit
UART0_RX	I	UART0 Data Receive
UART1_TX	O	UART1 Data Transmit
UART1_RX	I	UART1 Data Receive
UART1_CTS	I	UART1 Data Clear to Send
UART1_RTS	O	UART1 Data Request to Send
UART2_TX	O	UART2 Data Transmit
UART2_RX	I	UART2 Data Receive
UART2_CTS	I	UART2 Data Clear to Send
UART2_RTS	O	UART2 Data Request to Send
UART3_TX	O	UART3 Data Transmit
UART3_RX	I	UART3 Data Receive
UART3_CTS	I	UART3 Data Clear to Send
UART3_RTS	O	UART3 Data Request to Send

11.2.3.2. Clock Sources

Table 11-4 describes the clock sources of UART.

Table 11- 4. UART Clock Sources

Clock Sources	Description
APB2_CLK	Clock of APB2

11.2.3.3. Typical Application

Figure 11-12 shows the application block diagram of UART.

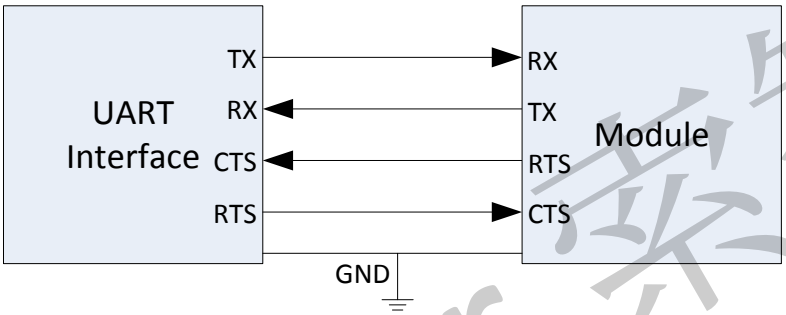

Figure 11- 12. UART Application Diagram

11.2.3.4. UART Timing Diagram

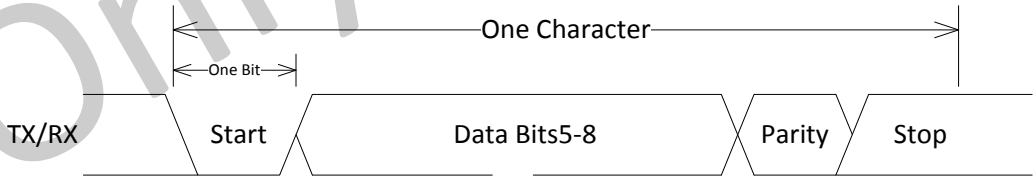

Figure 11- 13. UART Serial Data Format

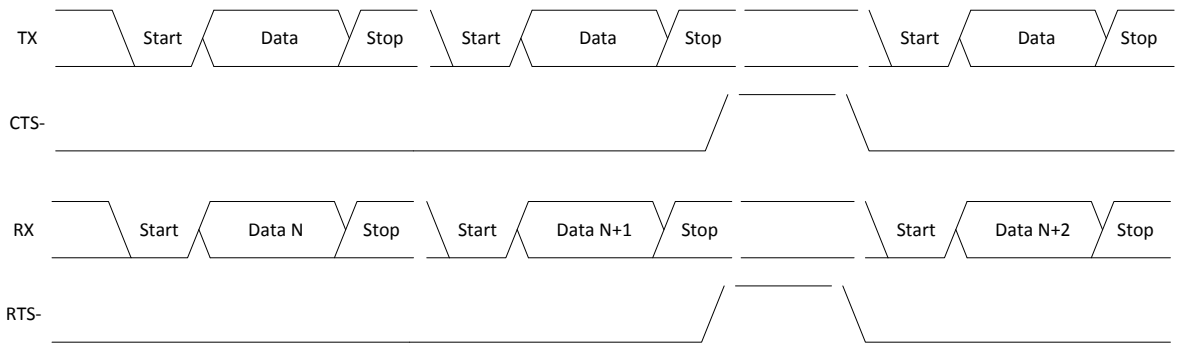

Figure 11- 14. RTS/CTS Autoflow Control Timing

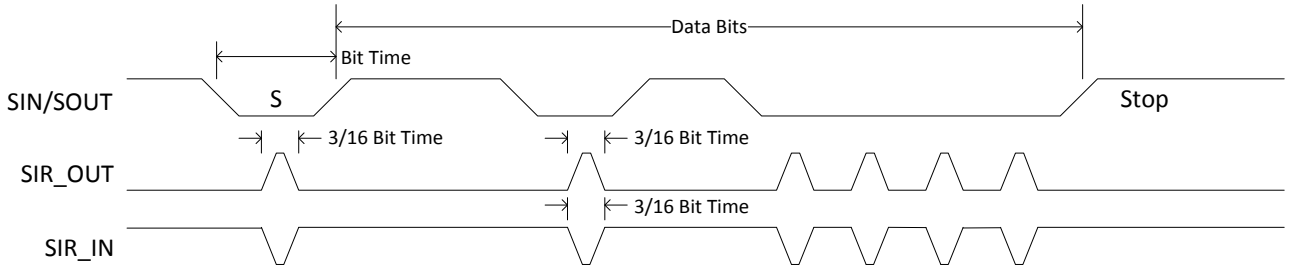

Figure 11- 15. Serial IrDA Data Format

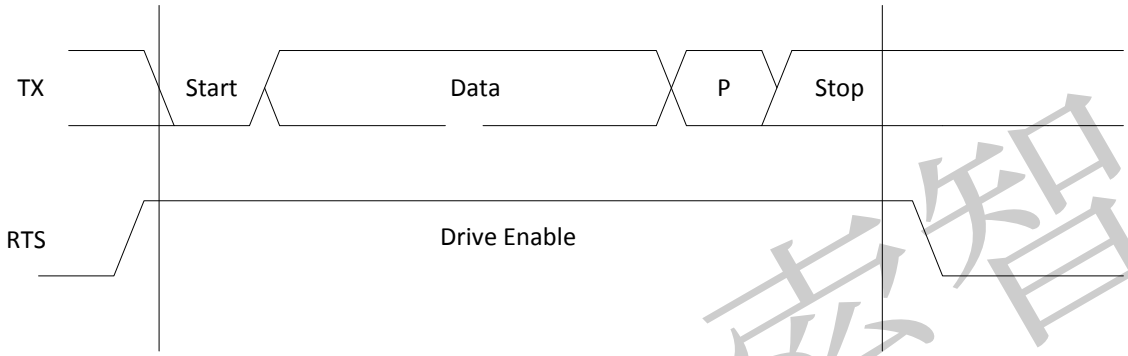

Figure 11- 16. RS-485 Timing

11.2.3.5. UART Operating Mode

11.2.3.5.1. Basic Mode Setting

The **UART_LCR** register can set basic parameter of a data frame: data width(5 to 8 bits), stop bit number(1/1.5/2), parity type.

A frame transfer of the UART includes the start signal, data signal, parity bit and stop signal. The LSB is transmitted first.

- Start signal(start bit): It is the start flag of a data frame. According to UART protocol, the low level of TXD signal indicates the start of a data frame. When the UART transmits data, the level need hold high.
- Data signal(data bit): The data bit width can be configured as 5-bit,6-bit,7-bit,8-bit through different applications.
- Parity bit: It is 1-bit error correction signal. Parity bit includes odd parity, even parity. The UART can enable and disable the parity bit by setting the **UART_LCR** register.
- Stop Signal(stop bit): It is the stop bit of a data frame. The stop bit can be set to 1-bit, 1.5-bit and 2-bit by the **UART_LCR** register. The high level of TXD signal indicates the end of a data frame.

11.2.3.5.2. Baud Rate Setting

The baud rate is calculated as follows: Baud rate = SCLK /(16 * divisor). SCLK is usually APB2 and can be set in CCU. Divisor is frequency divider of UART. The frequency divider has 16-bit, the low 8-bit is in the UART_DLL register, the

high 8-bit is in the UART_DLH register.

The relationship between different UART mode and error rate is as follows.

Table 11- 5. UART Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Over sampling	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0
24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16
48000000	13	230400	16	0.16
64000000	7	576000	16	-0.794
75000000	5	921600	16	1.725
48000000	3	1000000	16	0
24000000	1	1500000	16	0
48000000	1	3000000	16	0
64000000	1	4000000	16	0

Table 11- 6. IrDA Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	3/16	0
24000000	2500	600	3/16	0
24000000	1250	1200	3/16	0
24000000	625	2400	3/16	0
24000000	313	4800	3/16	-0.16
24000000	156	9600	3/16	0.16
24000000	78	19200	3/16	0.16
24000000	39	38400	3/16	0.16
24000000	26	57600	3/16	0.16
24000000	13	115200	3/16	0.16

Table 11- 7. RS485 Mode Baud and Error Rates

Clock source	Divisor	Baud rate	Encoding	Error(%)
24000000	5000	300	16	0
24000000	2500	600	16	0
24000000	1250	1200	16	0
24000000	625	2400	16	0

24000000	313	4800	16	-0.16
24000000	156	9600	16	0.16
24000000	78	19200	16	0.16
24000000	39	38400	16	0.16
24000000	26	57600	16	0.16
24000000	13	115200	16	0.16

11.2.3.5.3. DLAB Setting

DLAB control bit (**UART_LCR[7]**) is the access control bit of divisor Latch register.
If DLAB is 0, then 0x00 offset address is **TX/RX FIFO** register, 0x04 offset address is **IER** register.
If DLAB is 1, then 0x00 offset address is **DLL** register, 0x04 offset address is **DLH** register.
When UART initial, divisor need be set. That is, writing 1 to DLAB can access the **DLL** and **DLH** register, after finished setting, writing 0 to DLAB can access the **TX/RX FIFO** register.

11.2.3.5.4. CHCFG_AT_BUSY Setting

The function of **CHCFG_AT_BUSY**(UART_HALT[1]) and **CHANGE_UPDATE**(UART_HALT[2]) are as follows.
CHCFG_AT_BUSY(configure at busy): Enable the bit, software can also set UART controller when UART is busy, such as the LCR,DLH,DLL register.
CHANGE_UPDATE(change update): If **CHCFG_AT_BUSY** is enabled, and **CHANGE_UPDATE** is written to 1, the configuration of UART controller can be updated. After completed update, the bit is cleared to 0 automatically.

Setting divisor, performs the following steps:
Step1 Write 1 to **CHCFG_AT_BUSY** to enable “configure at busy”.
Step2 Write 1 to **DLAB** , and set **DLH** and **DLL**.
Step3 Write 1 to **CHANGE_UPDATE** to update configuration. The bit is cleared to 0 automatically after completed update.

11.2.3.5.5. UART Busy

UART_USR[0] is a busy flag of UART controller or not.
When TX transmits data, or RX receives data, or TX FIFO is not empty, or RX FIFO is not empty, then the BUSY flag bit can be set to 1 by hardware, which indicates the UART controller is busy.

11.2.4. Programming Guidelines

11.2.4.1. Initialization

Step1 System Initialization

- Configure APB2_CFG_REG in CCU module to set APB2 bus clock(The clock is 24MHz by default).
- Set UART_BGR_REG[UARTx_GATING] to 1 to enable the module clock, and set UART_BGR_REG[UARTx_RST] to 1 to de-assert the module.

Step2 UART Controller Initialization

- IO configuration: Configure GPIO multiplex as UART function, and set UART pins to internal pull-up mode(For detail, see the description in Port Controller).
- Baud-rate configuration:
  - Set UART baud-rate(refer to section 11.2.3.5.2);
  - Write UART_FCR[FIFOE] to 1 to enable TX/RX FIFO;
  - Write UART_HALT[HALT_TX] to 1 to disable TX transfer;
  - Set UART_LCR[DLAB] to 1, remain default configuration for other bits; set 0x00 offset address to UART_DLL register, set 0x04 offset address to UART_DLH register;
  - Write the high 8-bit of divisor to UART_DLH, and write the low 8-bit of divisor to UART_DLL;
  - Set UART_LCR[DLAB] to 0, remain default configuration for other bits; set 0x00 offset address to UART_RBR/UART_THR register, set 0x04 offset address to UART_IER register;
  - Set UART_HALT[HALT_TX] to 0 to enable TX transfer.

Step3 Controller Parameter Configuration

- Set data width, stop bits and even/odd parity type by writing UART_LCR register.
- Reset, enable FIFO and set FIFO trigger condition by writing UART_FCR register.
- Set flow control parameter by writing UART_MCR register.

Step4 Interrupt Configuration

- Configure UART interrupt vector number to request UART interrupt(please refer to GIC module for interrupt vector number).
- In DMA mode, write UART_IER to 0 to disable interrupt; write UART_HSK[Handshake configuration] to 0xE5 to set DMA handshake mode; write UART_FCR[DMAM] to 1 to set DMA transmission/reception mode; set DMA parameter and request DMA interrupt according to DMA configuration process.
- In Interrupt mode, configure UART_IER to enable corresponding interrupt according to requirements: such as transmit(TX) interrupt, receive(RX) interrupt, receive line status interrupt, RS48 interrupt, etc. (Here TX/RX Interrupt is usually used).

11.2.4.2. Data Transfer/Receive in Query Mode

Data transfer

Step1 Write data to UART_THR to start data transfer.

Step2 Check TX_FIFO status by reading UART_USR[TFNF]. If the bit is 1, data can continue to be written; if the bit is 0, wait data transfer, and data cannot continue to write until FIFO is not full.

Data receive

Step1 Check RX_FIFO status by reading UART_USR[RFNE].

Step2 Read data from UART_RBR if RX_FIFO is not empty.

Step3 If UART_USR[RFNE] is 0, data is received completely.

11.2.4.3. Data Transfer/Receive in Interrupt Mode

Data transfer

Step1 Set UART_IER[ETBEI] to 1 to enable UART transfer interrupt.

Step2 Write data to be transmitted to UART_THR.

Step3 When the data of TX_FIFO meets trigger condition(such as FIFO/2, FIFO/4), UART transfer interrupt is generated.

Step4 Check UART_USR[TFE] and determine whether TX_FIFO is empty. If UART_USR[TFE] is 1, it indicates that the data in TX_FIFO is transmitted completely.

Step5 Clear UART_IER[ETBEI] to 0 to disable transfer interrupt.

Data receive

Step1 Set UART_IER[ERBFI] to 1 to enable UART receive interrupt.

Step2 When the received data from RX_FIFO meets trigger condition(such as FIFO/2, FIFO/4), UART receive interrupt is generated.

Step3 Read data from UART_RBR.

Step4 Check RX_FIFO status by reading UART_USR[RFNE] and determine whether to read data. If the bit is 1, continue to read data from UART_RBR until UART_USR[RFNE] is cleared to 0, which indicates data is received completely.

Figure 11-17 shows the process of UART transmitting and receiving data in interrupt mode.

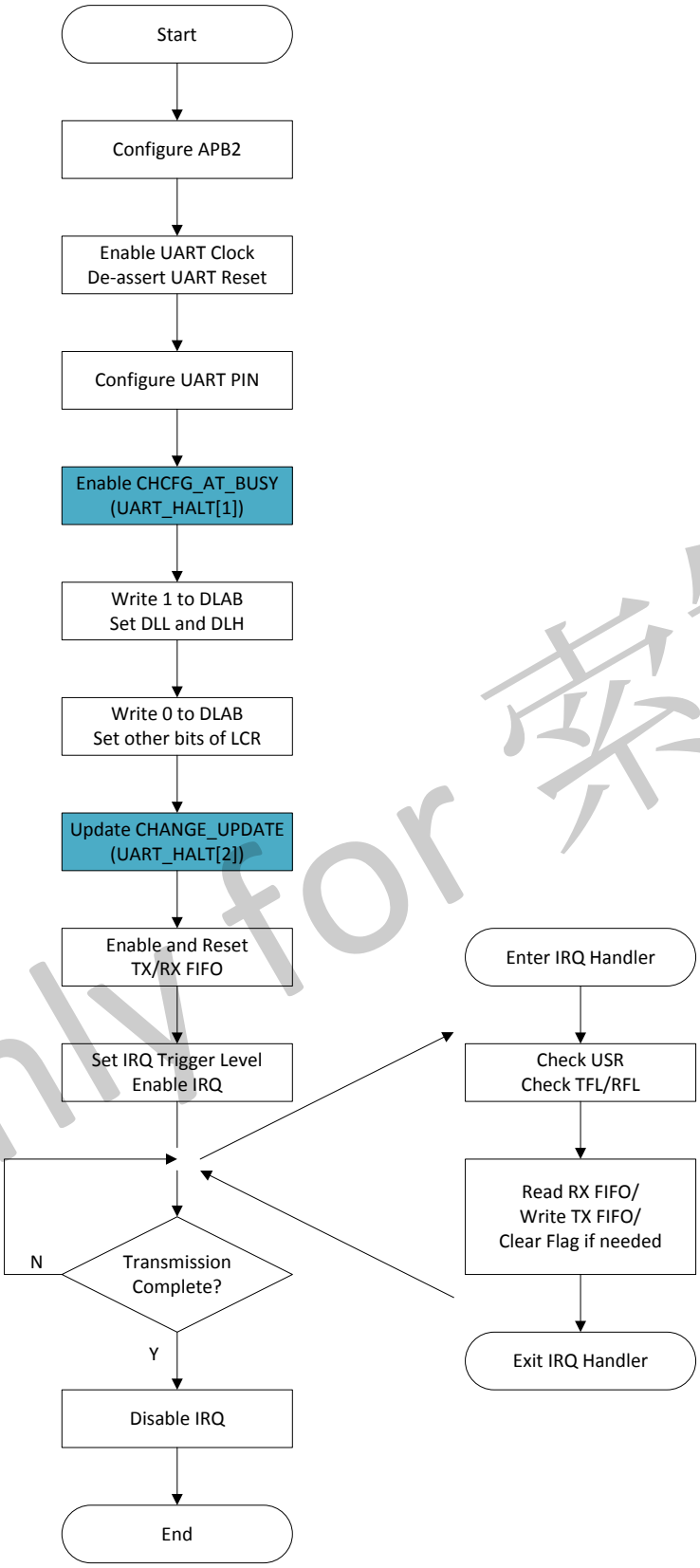

Figure 11- 17. Process of UART Transmitting/Receiving Data in Interrupt Mode

11.2.4.4. Data Transfer/Receive in DMA Mode

Data transfer

Step1 Configure UART DMA interrupt according to initialization process.

Step2 Configure DMA data channel, including transfer source address, transfer destination address, number of data to be transferred, and transfer type, etc(For details, see the description in DMA module).

Step3 Enable DMA transfer function of the UART by setting the register of DMA module.

Step4 Determine whether UART data is transferred completely based on DMA status. If all data is transferred completely, disable DMA transfer function of the UART.

Data receive

Step1 Configure DMA data channel, including transfer source address, transfer destination address, number of data to be transferred, and transfer type, etc(For details, see the description in DMA module).

Step2 Enable DMA receive function of the UART by setting the register of DMA module.

Step3 Determine whether UART data is received completely based on DMA status. If all data is received completely, disable DMA receive function of the UART.

Figure 11-18 shows the process of UART transmitting data in DMA mode.

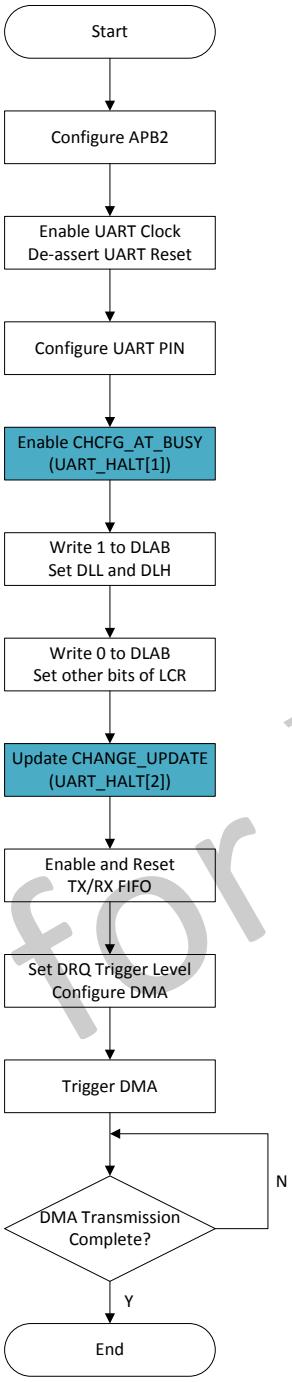

Figure 11- 18. Process of DMA Transmitting Data in DMA Mode

11.2.5. Register List

Module Name	Base Address
UART0	0x05000000
UART1	0x05000400
UART2	0x05000800
UART3	0x05000C00

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level Register
UART_RFL	0x0084	UART Receive FIFO Level Register
UART_HSK	0x0088	UART DMA Handshake Configuration Register
UART_HALT	0x00A4	UART Halt TX Register
UART_DBG_DLL	0x00B0	UART Debug DLL Register
UART_DBG_DLH	0x00B4	UART Debug DLH Register
UART_485_CTL	0x00C0	UART RS485 Control and Status Register
RS485_ADDR_MATCH	0x00C4	UART RS485 Address Match Register
BUS_IDLE_CHK	0x00C8	UART RS485 Bus Idle Check Register
TX_DLY	0x00CC	UART TX Delay Register

11.2.6. Register Description

11.2.6.1. 0x0000 UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register can not read before the next data character arrives, then the data

			already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

11.2.6.2. 0x0000 UART Transmit Holding Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters data may be written to the THR before the FIFO is full. When the FIFO is full, any write data results in the write data being lost.

11.2.6.3. 0x0000 UART Divisor Latch Low Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that when the Divisor Latch Registers (DLL and DLH) are set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

11.2.6.4. 0x0004 UART Divisor Latch High Register(Default Value: 0x0000_0000)

Offset: 0x0004	Register Name: UART_DLH

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16 bits, read/write, Divisor Latch Register contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that when the Divisor Latch Registers (DLL and DLH) is set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

11.2.6.5. 0x0004 UART Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RS485_INT_EN RS485 Interrupt Enable 0:Disable 1:Enable
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable

1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupt. 0: Disable 1: Enable

11.2.6.6. 0x0008 UART Interrupt Identity Register(Default Value: 0x0000_0001)

Offset: 0x0008			**Register Name: UART_IIR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0011:RS485 Interrupt 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout The bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset**
0001	-	None	None	-
0110	Highest	Receiver	Overrun/parity/framing errors or	Reading the line status register

		line status	break interrupt	
0011	Second	RS485 Interrupt	In RS485 mode, receives address data and match setting address	Writes 1 to addr flag to reset
0100	Third	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Fourth	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Fifth	Transmit holding register empty	Transmitter holding register empty (Program THRE mode disabled) or XMIT FIFO at or below threshold (Program THRE mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE mode selected and enabled).
0000	Sixth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status register
0111	Seventh	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

11.2.6.7. 0x0008 UART FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO when the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full

5:4	W	0x0	TFT TX Empty Trigger This is used to select the empty threshold level when the THRE Interrupts are generated and the mode is active. It also determines when the dma_tx_req_n signal is asserted in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 In this mode, if PTE is high and TX FIFO is enabled, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is high and TX FIFO is disabled, the TX DMA request will send when THRE is empty. If PTE is low, the TX DMA request will send when the TX FIFO is empty. If dma_pte_rx is high and RX FIFO is enabled, the rx drq will send when RFL is equal to or more than FIFO Trigger Level. 1: Mode 1 In this mode, if TX FIFO is enabled and the PTE is high, the TX DMA request will send when TFL is less than or equal to FIFO Trigger Level. If PTE is low, the TX DMA request will send when TX FIFO is empty and the request stops only when TX FIFO is full. If RFL is equal to or more than FIFO Trigger Level, the rx drq will be set to 1, in otherwise, it will be set to 0.
2	W	0x0	XFIFOR XMIT FIFO Reset The bit resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset The bit resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs The bit enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller portion of FIFOs is reset.

11.2.6.8. 0x000C UART Line Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If setting to 0, the serial output is forced to the spacing (logic 0) state. When not in Loopback mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE is enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0x0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable/readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is unset to reverse the LCR[4]. 00: Odd Parity 01: Even Parity 1X: Reverse LCR[4] In RS485 mode, it is the 9th bit--address bit. 11:9th bit = 0, indicates that this is a data byte. 10:9th bit = 1, indicates that this is an address byte. **Note: When using this function, PEN(LCR[3]) must set to 1.**
3	R/W	0x0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: Parity disabled 1: Parity enabled
2	R/W	0x0	STOP Number of stop bits

			It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If setting to 0, one stop bit is transmitted in the serial data. If setting to 1 and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

11.2.6.9. 0x0010 UART Modem Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x0	UART_FUNCTION Select IrDA or RS485 00:UART Mode 01:IrDA SIR Mode 10:RS485 Mode 11:Reserved
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control mode disabled 1: Auto Flow Control mode enabled
4	R/W	0x0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] is set to zero), data on the sout line is held high, while serial data output is looped

			back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] is set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The RTS (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] is set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] is set to one) and FIFOs enable (FCR[0] is set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] is set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0: dtr_n de-asserted (logic 1) 1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] is set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

11.2.6.10. 0x0014 UART Line Status Register(Default Value: 0x0000_0060)

Offset:0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this

			bit is set to “1” when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided, there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sir_in, is held in a logic '0' state for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of *start time* + *data bits* + *parity* + *stop bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RC	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data,

			and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	RC	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	RC	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

11.2.6.11. 0x0018 UART Modem Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD

			Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] is set to 1), DSR is the same as MCR[0] (DTR).
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RC	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. **Note: If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.**
2	RC	0x0	TERI Trailing Edge Ring Indicator

			This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	RC	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). **Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.**
0	RC	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). **Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.**

11.2.6.12. 0x001C UART Scratch Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: UART_SCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

11.2.6.13. 0x007C UART Status Register(Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/

4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO in not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

11.2.6.14. 0x0080 UART Transmit FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:0	R	0x0	TFL Transmit FIFO Level The bit indicates the number of data entries in the transmit FIFO.

11.2.6.15. 0x0084 UART Receive FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/

8:0	R	0x0	RFL Receive FIFO Level The bit indicates the number of data entries in the receive FIFO.

11.2.6.16. 0x0088 UART DMA Handshake Configuration Register(Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: UART_HSK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xE5	Handshake configuration 0xA5: DMA wait cycle mode 0xE5: DMA handshake mode

11.2.6.17. 0x00A4 UART Halt TX Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTE The sending of TX_REQ. In DMA1 mode (FIFO on), if PTE is set to 1, when TFL is less than trig, send the DMA request. If PTE is set to 0, when FIFO is empty, send the DMA request. The DMA request will stop when FIFO is full. In DMA0 mode, if PTE is set to 1 and FIFO is on, when TFL is less than trig, send DMA request. If PTE is set to 1 and FIFO is off, when THRE is empty, send DMA request. If PTE is set to 0, when FIFO is empty, send DMA request.
6	R/W	0x0	DMA_PTE_RX The sending of RX_DRQ. In DMA1 mode, when RFL is more than or equal to trig or receive timeout, send DRQ. In DMA0 mode, if DMA_PTE_RX is 1 and FIFO is on, when RFL is more than trig, send DRQ. In other cases, once the receive data is valid, send DRQ.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse

3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user uses HALT[1] to change the baud rate or LCR configuration, write 1 to update the configuration and wait this bit to self-clear to 0 to finish update process. Writing 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change LCR register configuration and baud rate register (DLH and DLL) when the UART is busy. 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled **Note: If FIFOs are not enabled, the setting has no effect on operation.**

11.2.6.18. 0x00B0 UART DBG DLL Register(Default Value: 0x0000_0000)

Offset: 0x00B0			**Register Name: UART_DBG_DLL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLL

11.2.6.19. 0x00B4 UART DBG DLH Register(Default Value: 0x0000_0000)

Offset: 0x00B4			**Register Name: UART_DBG_DLH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DEBUG DLH

11.2.6.20. 0x00C0 UART RS485 Control and Status Register(Default Value: 0x0000_0000)

Offset: 0x00C0			**Register Name: UART_485_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	Reserved
6	R/W1C	0x0	AAD_ADDR_F In AAD mode, when UART receives an address byte and the byte is the same as RS485_ADDR_MATCH, this bit will be set to 1. If RS485 interrupt is enabled, the RS485 interrupt will arrive.

			Write 1 to clear this bit and reset the RS485 interrupt.
5	R/W1C	0x0	RS485_ADDR_DET_F This is a flag of the detecting of address bytes. When UART receives an address byte, this bit will be set to 1. If the RS485 Interrupt is enabled, the RS485 interrupt will arrive. 1:An address byte is detected 0:No address byte is detected Write 1 to clear this bit and reset the RS485 interrupt.
4	/	/	/
3	R/W	0x0	RX_BF_ADDR In NMM mode, If setting this bit to 1, UART will receive all the bytes into FIFO before receiving an address byte. If setting to 0, it will not. 1:Receive 0:Not Receive
2	R/W	0x0	RX_AF_ADDR In NMM mode, if setting this bit to 1, UART will receive all the bytes into FIFO after receiving an address byte. If setting to 0, it will not. 1:Receive 0:Not Receive
1:0	R/W	0x0	RS485_SLAVE_MODE_SEL RS485 Slave Mode 00: Normal Multidrop Operation(NMM) 01: Auto Address Detection Operation(AAD) 10: Reserved 11: Reserved

11.2.6.21. 0x00C4 UART RS485 Address Match Register(Default Value: 0x0000_0000)

Offset: 0x00C4			**Register Name: RS485_ADDR_MATCH**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	ADDR_MATCH The matching address uses in AAD mode. **Note: It is only available for AAD.**

11.2.6.22. 0x00C8 UART RS485 Bus Idle Check Register(Default Value: 0x0000_0000)

Offset: 0x00C8			**Register Name: BUS_IDLE_CHK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	BUS_IDLE_CHK_EN 0: Disable bus idle check function 1: Enable bus idle check function

6	R	0x0	BUS_STATUS The Flag of Bus Status 0:Idle 1:Busy
5:0	R	0x0	ADJ_TIME Bus Idle Time The unit is 8*16*Tclk.

11.2.6.23. 0x00CC UART TX Delay Register(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: TX_DLY
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLY The delay time between the last stop bit and the next start bit. The unit is 16*Tclk. It is used to control the space between two bytes in TX.

11.3. SPI

11.3.1. Overview

The SPI is a full-duplex, synchronous, serial communication interface which allows rapid data communication with fewer software interrupts. The SPI controller contains one 64x8 bits receiver buffer (RXFIFO) and one 64x8 bits transmit buffer (TXFIFO). It can work at master mode and slave mode.

The SPI has the following features:

- Full-duplex synchronous serial interface
- Master/slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA support
- Supports mode0, mode1, mode2 and mode3
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1 bit to 32 bits
- Supports the SPI NAND flash and SPI NOR flash
- Supports standard SPI, dual-output/dual-input SPI, dual I/O SPI, quad-output/quad-input SPI
- Supports maximum IO rate: 100MHz

NOTE

V833 has three SPI controllers, and V831 has two SPI controllers.

11.3.2. Block Diagram

Figure 11-19 shows a block diagram of the SPI.

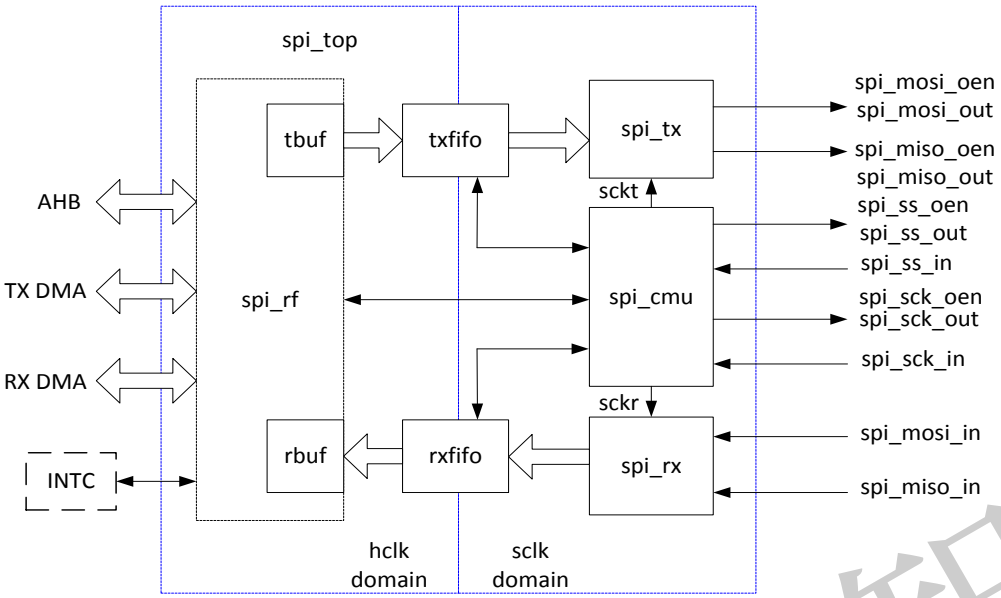

Figure 11- 19. SPI Block Diagram

The SPI comprises with:

spi_rf: Responsible for implementing the internal register, interrupt and DMA Request.

spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8bits, then the data is written into the rxfifo.

spi_rbuf: The block is used to convert the rxfifo data into read data length of AHB.

txfifo, rxfifo: For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the txfifo; data received from the external serial device into SPI is pushed into the rxfifo.

spi_cmu: Responsible for implementing SPI bus clock, chip select, internal sample and the generation of transfer clock.

spi_tx: Responsible for implementing SPI data transfer, the interface of the internal txfifo and status register.

spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

11.3.3. Operations and Functional Descriptions

11.3.3.1. External Signals

Table 11-8 describes the external signals of SPI. MOSI and MISO are bidirectional I/O, when SPI is configured as master device, CLK and CS is output pin; when SPI is configurable as slave device, CLK and CS is input pin. The unused SPI ports are used as General Purpose I/O ports.

Table 11- 8. SPI External Signals

V833 Signal	V831 Signal	Description	Type
SPI0_CS0	SPI0_CS0	SPI0 Chip Select Signal0, Low Active	I/O
SPI0_CS1	/	SPI0 Chip Select Signal1, Low Active	I/O
SPI0_CLK	SPI0_CLK	SPI0 Clock Signal	I/O

SPI0_MOSI	SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0_WP	SPI0_WP	Write protection and active low or Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0_HOLD	SPI0_HOLD	The HOLD pin is used to temporarily pause serial communication without deselecting or resetting the device. While the HOLD pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, or Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1_CS0	SPI1_CS0	SPI1 Chip Select Signal0, Low Active	I/O
SPI1_CS1	SPI1_CS1	SPI1 Chip Select Signal1, Low Active	I/O
SPI1_CLK	SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI2_CS0	/	SPI2 Chip Select Signal0, Low Active	I/O
SPI2_CLK	/	SPI2 Clock Signal	I/O
SPI2_MOSI	/	SPI2 Master Data Out, Slave Data In	I/O
SPI2_MISO	/	SPI2 Master Data In, Slave Data Out	I/O

11.3.3.2. Clock Sources

The SPI controller get 5 different clock sources, users can select one of them to make SPI clock source. Table 11-9 describes the clock sources for SPI.

Table 11- 9. SPI Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_UNI(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1200MHz
PLL_UNI(2X)	Peripheral Clock, default value is 1200MHz

11.3.3.3. Typical Application

Figure 11-20 shows the application block diagram when the SPI master device is connected to a slave device.

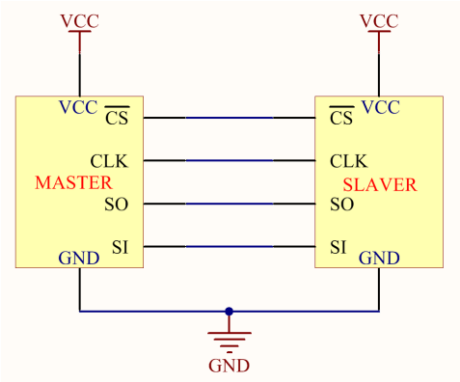

Figure 11- 20. SPI Application Block Diagram

11.3.3.4. SPI Transmit Format

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 11-10.

Table 11- 10. SPI Transmit Format

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 11-21 and Figure 11-22 describe four waveforms for SPI_SCLK.

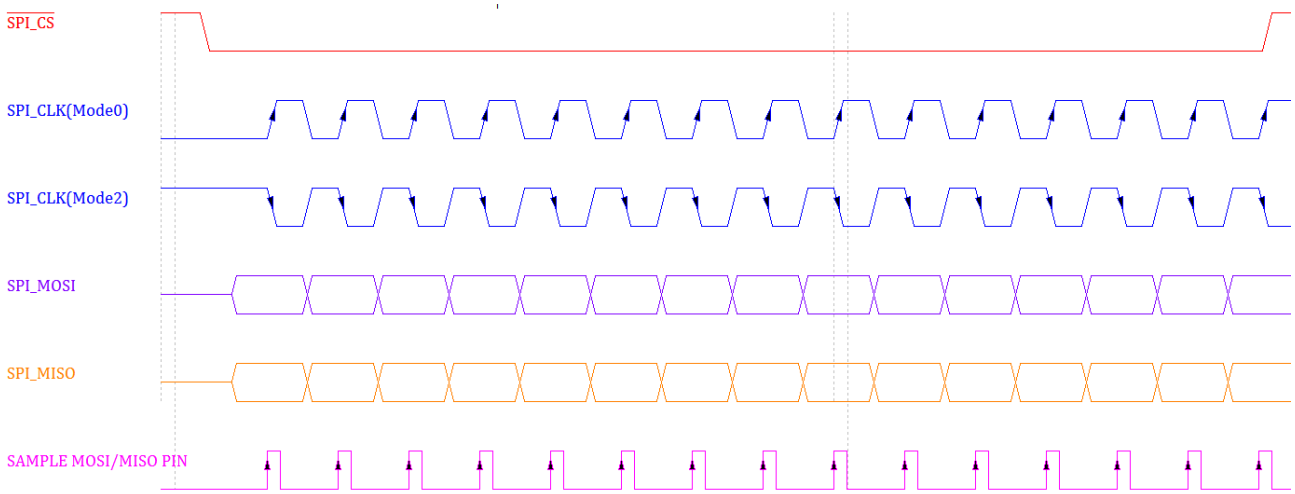

Figure 11- 21. SPI Phase 0 Timing Diagram

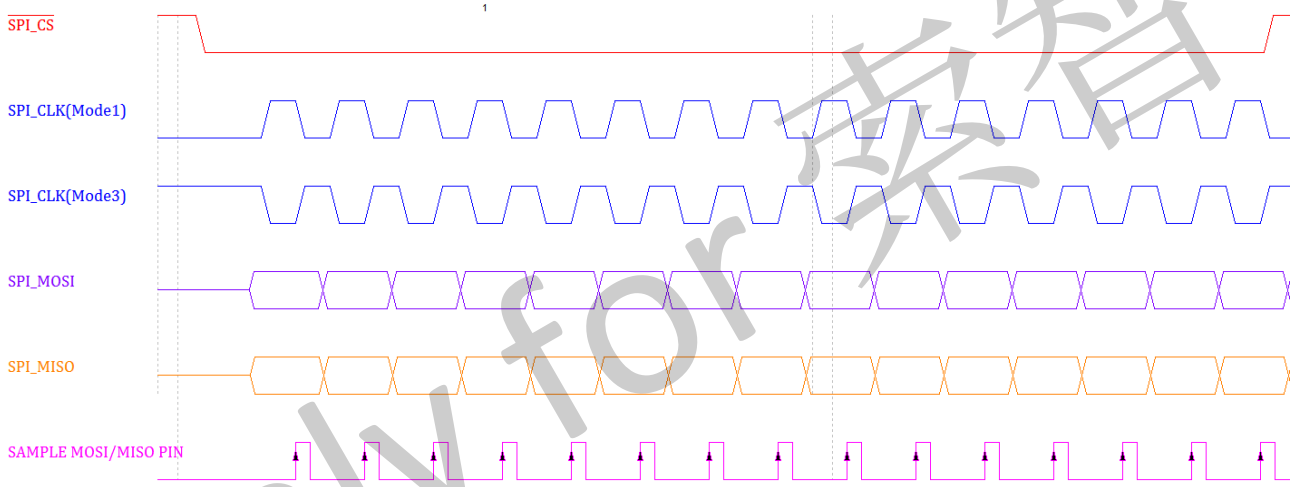

Figure 11- 22. SPI Phase 1 Timing Diagram

11.3.3.5. SPI Master and Slave Mode

The SPI controller can be configured to a master or slave device. Master mode is selected by setting the **MODE** bit in the **SPI Global Control Register;** slave mode is selected by clearing the **MODE** bit in the **SPI Global Control Register**.

In master mode, SPI_CLK is generated and transmitted to external device, and data from the TX FIFO is transmitted on the MOSI pin, the data from slave is received on the MISO pin and sent to RX FIFO. Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received. SPI_SS can be selected SPI auto control or software manual control. When using auto control, **SS_OWNER**(the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control, **SS_OWNER** must be set, Chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In slave mode, after software selects the **MODE** bit to '0', it waits for master initiate a transaction. When the master asserts SPI_SS and SPI_CLK is transmitted to the slave, the slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

11.3.3.6. SPI 3-Wire Mode

The SPI 3-wire mode is only valid when the SPI controller work in master mode, and is selected when the **Work Mode Select(bit[1:0])** is equal to 0x2 in the **SPI Bit-Aligned Transfer Configure Register**. And in the 3-wire mode, the input data and the output data use the same single data line. The following figure describes this mode.

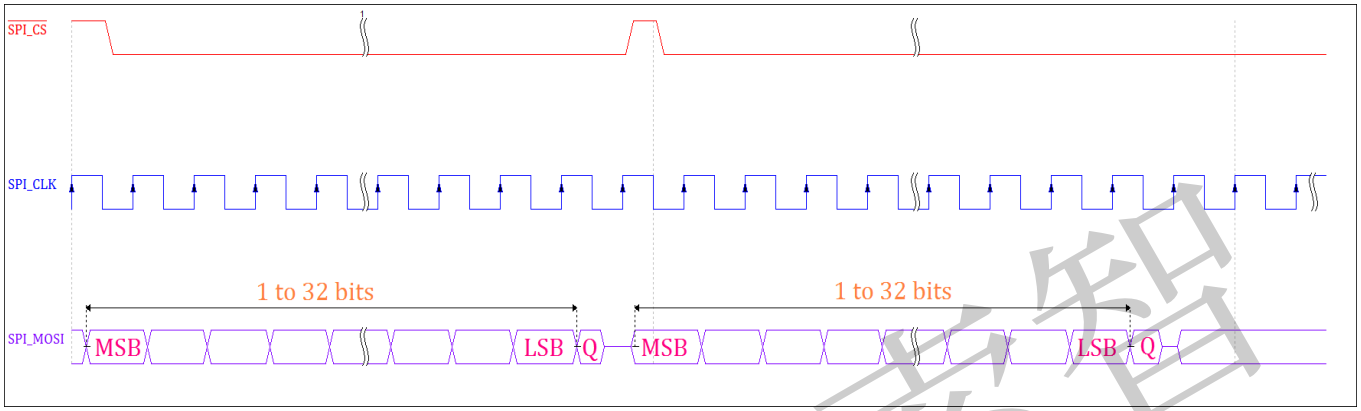

Figure 11- 23. SPI 3-Wire Mode

11.3.3.7. SPI Dual-Input/Dual-Output and Dual I/O Mode

The dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**. Using the dual mode allows data to be transferred to or from the device at double the rate of standard single mode SPI devices, data can be read at fast speed using two data bits(MOSI and MISO) at a time. The following figure describes the dual-input/dual-output SPI(Figure 11-24) and the dual I/O SPI(Figure 11-25).

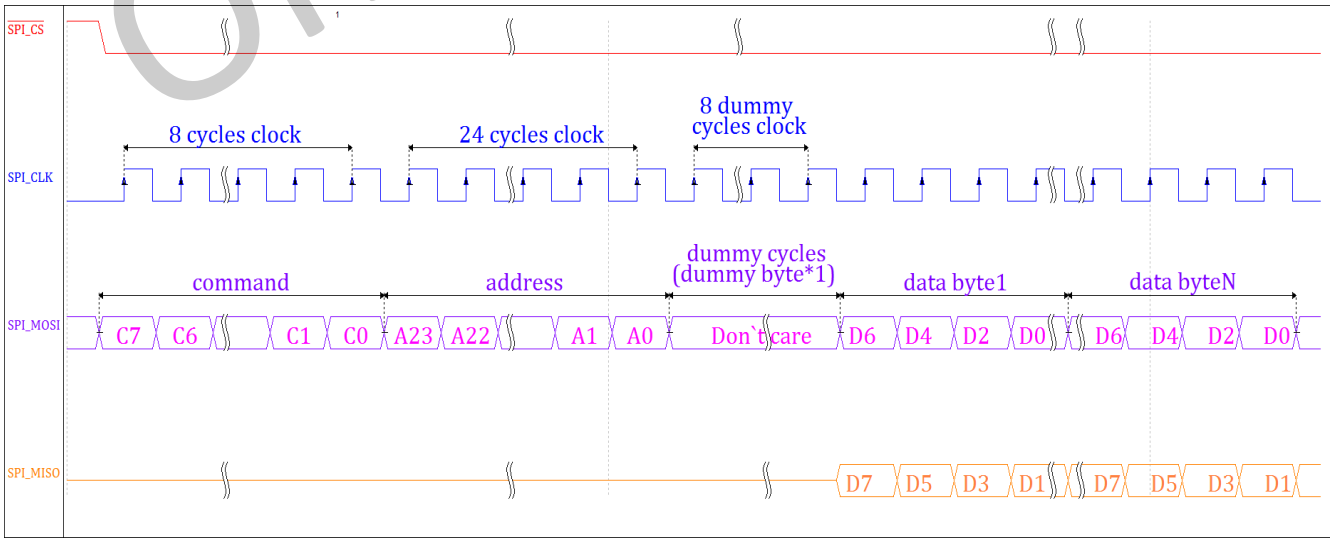

Figure 11- 24. SPI Dual-Input/Dual-Output Mode

In the dual-input/dual-output SPI, the command, address, and the dummy bytes output in unit of a single bit in serial mode through SPI_MOSI line, only the data bytes are output(write) and input(read) in unit of dual bits through the

SPI_MOSI and SPI_MISO.

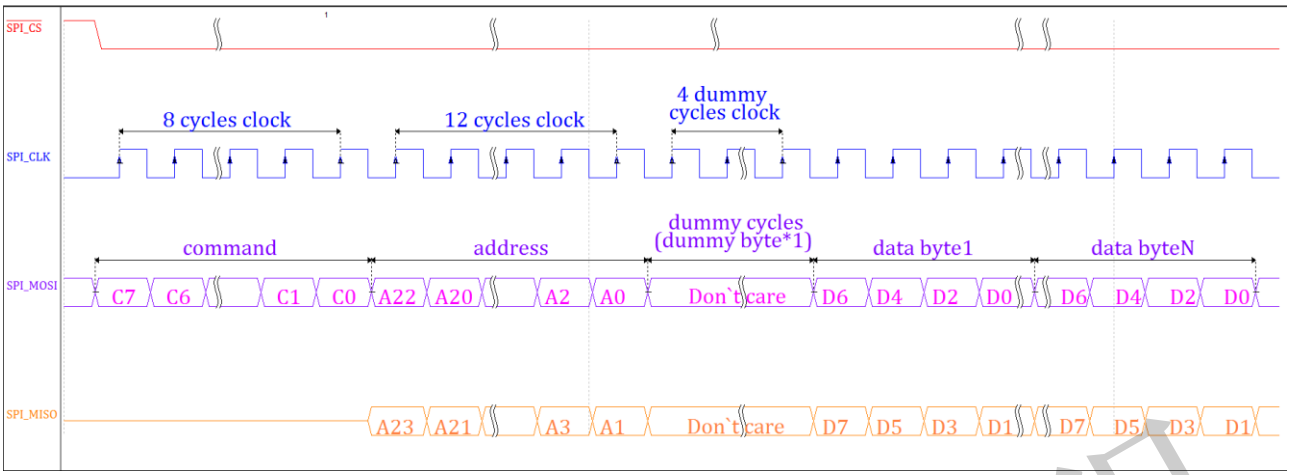

Figure 11- 25. SPI Dual I/O Mode

In the dual I/O SPI, only the command bytes are output in unit of a single bit in serial mode through SPI_MOSI line. The address bytes and the dummy bytes are output in unit of dual bits through the SPI_MOSI and SPI_MISO. And the data bytes are output(write) and input(read) in unit of dual bits through the SPI_MOSI and SPI_MISO.

11.3.3.8. SPI Quad-Input/Quad-Output Mode

The quad read mode(SPI x4) is selected when the **Quad_EN**(bit29) is set in the **SPI Master Burst Control Counter Register**. Using the quad mode allows data to be transferred to or from the device at 4 times the rate of standard single mode SPI devices, data can be read at fast speed using four data bits(MOSI, MISO, IO2(WP#)and IO3(HOLD#)) at the same time. The following figure describes the quad-input/quad-output SPI.

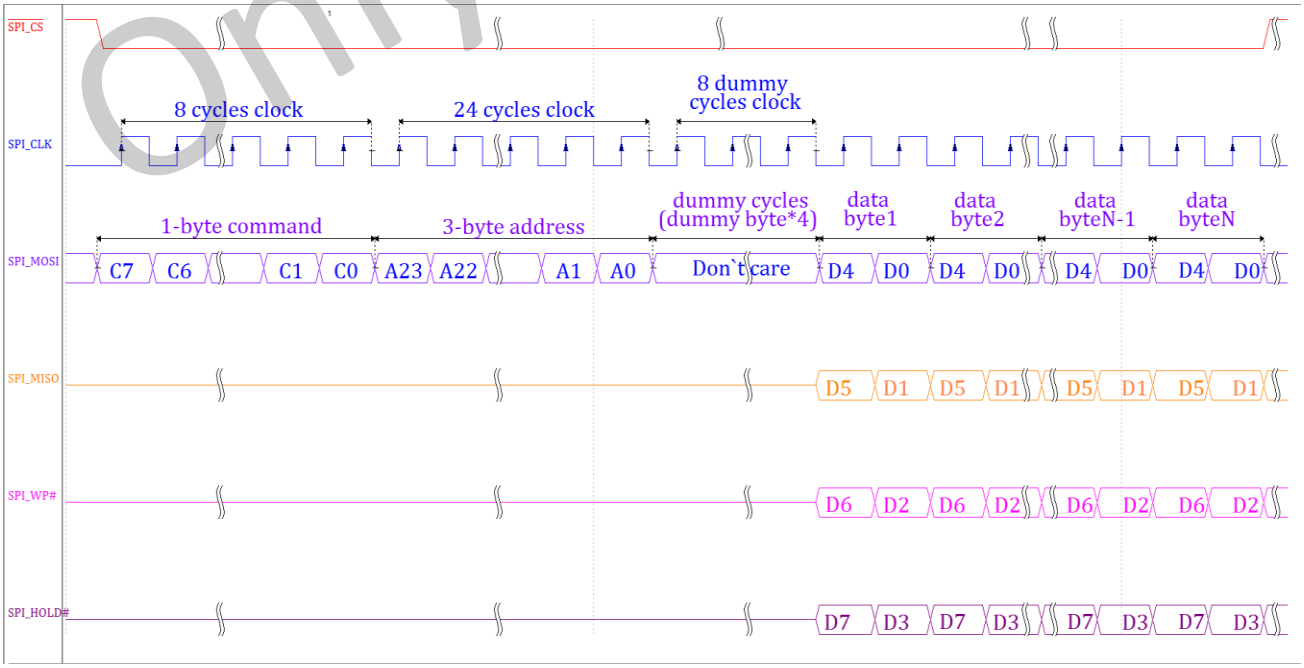

Figure 11- 26. SPI Quad-Input/Quad-Output Mode

In the quad-input/quad-output SPI, the command, address, and the dummy bytes are output in unit of a single bit in serial mode through SPI_MOSI line. Only the data bytes are output(write) and input(read) in unit of quad bits through the SPI_MOSI, SPI_MISO, SPI_WP# and SPI_HOLD#.

11.3.3.9. Transmit/Receive Burst in Master Mode

In SPI master mode, the transmit and receive burst(byte in unit) are configured before the SPI transfers serial data between the processor and external device. The transmit bursts are written in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** The transmit bursts in single mode before automatically sending dummy burst are written in STC(bit[23:0]) of **SPI Master Burst Control Counter Register.** For dummy data, SPI controller can automatically sent before receiving by writing DBC(bit[27:24]) in **SPI Master Burst Control Counter Register**. If users do not use SPI controller to sent dummy data automatically, then the dummy bursts are used as the transmit counters to write together in MWTC(bit[23:0]) of **SPI Master Transmit Counter Register.** In master mode, the total burst numbers are written in MBC(bit[23:0]) of **SPI Master Burst Counter Register.** When all transmit burst and receive burst are transferred, SPI controller will send an completed interrupt, at the same time, SPI controller will clear DBC,MWTC and MBC.

11.3.3.10. SPI Sample Mode and Run Clock Configuration

The SPI controller runs at 3kHz~100MHz at its interface to external SPI devices. The internal SPI clock should run at the same frequency as the outgoing clock in master mode. The SPI clock is selected different clock sources, SPI must configure different work mode. There are three work mode: normal sample mode, delay half cycle sample mode, delay one cycle sample mode. Delay half cycle sample mode is the default mode of SPI controller. When SPI runs at 40 MHz or below 40 MHz, SPI can work at normal sample mode or delay half cycle sample mode. When SPI runs over 60 MHz,setting the **SDC** bit in **SPI Transfer Control Register** to '1' makes the internal read sample point with a half cycle delay of SPI_CLK, which is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. The different configuration of SPI sample mode shows in Table 11-11.

Table 11- 11. SPI Sample Mode and Run Clock

SPI Sample Mode	SDM(bit13)	SDC(bit11)	Run Clock
normal sample	1	0	<=24MHz
delay half cycle sample	0	0	<=40MHz
delay one cycle sample	0	1	>=60MHz

CAUTION

The remaining spectrum is not recommended. Because when the output delay of SPI flash (refer to the datasheet of the manufactures for the specific delay time) is the same with the half cycle of SPI working clock, the variable edge of the device's output data bumps into the clock sampling edge of the controller, so setting 1 cycle of sampling delay would cause stability problem.

11.3.3.11. SPI Error Conditions

If any error conditions occur, hardware will set the corresponding status bits in the **SPI Interrupt Status Register** and stop the transfer. For the SPI controller, the following error scenarios can happen.

(1) TX_FIFO Underrun

TX_FIFO underrun happens when the CPU/DMA reads from TX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_UDF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(2) TX_FIFO Overflow

TX_FIFO overflow happens when the CPU/DMA writes into the TX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the TF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the TF_OVF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(3) RX_FIFO Underrun

RX_FIFO underrun happens when the CPU/DMA reads from RX FIFO when it is empty. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_UDF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_UDF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

(4) RX_FIFO Overflow

RX_FIFO overflow happens when the CPU/DMA writes into the RX FIFO when it is full. In the case, the SPI controller will end the transaction and flag the error bit along with the RF_OVF bit in the **SPI Interrupt Status Register**. The SPI controller will generate an interrupt if interrupts are enabled. Software has to clear the error bit and the RF_OVF bit. To start a new transaction, software has to reset the FIFO by writing to the SRST(soft reset) bit in the **SPI Global Controller Register.**

11.3.4. Programming Guidelines

11.3.4.1. CPU or DMA Operation

The SPI transfers serial data between the processor and external device. CPU and DMA are the two main operational modes for SPI. For each SPI, data is simultaneously transmitted(shifted out serially) and received (shifted in serially).SPI has 2 channels, TX channel and RX channel. TX channel has the path from TX FIFO to external device. RX channel has the path from external device to RX FIFO.

Write Data: CPU or DMA must write data on the register SPI_TXD, data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO, CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends an completed interrupt(the TC bit in SPI Interrupt Status Register) to the processor at the end of each transfer.

(1).CPU Mode

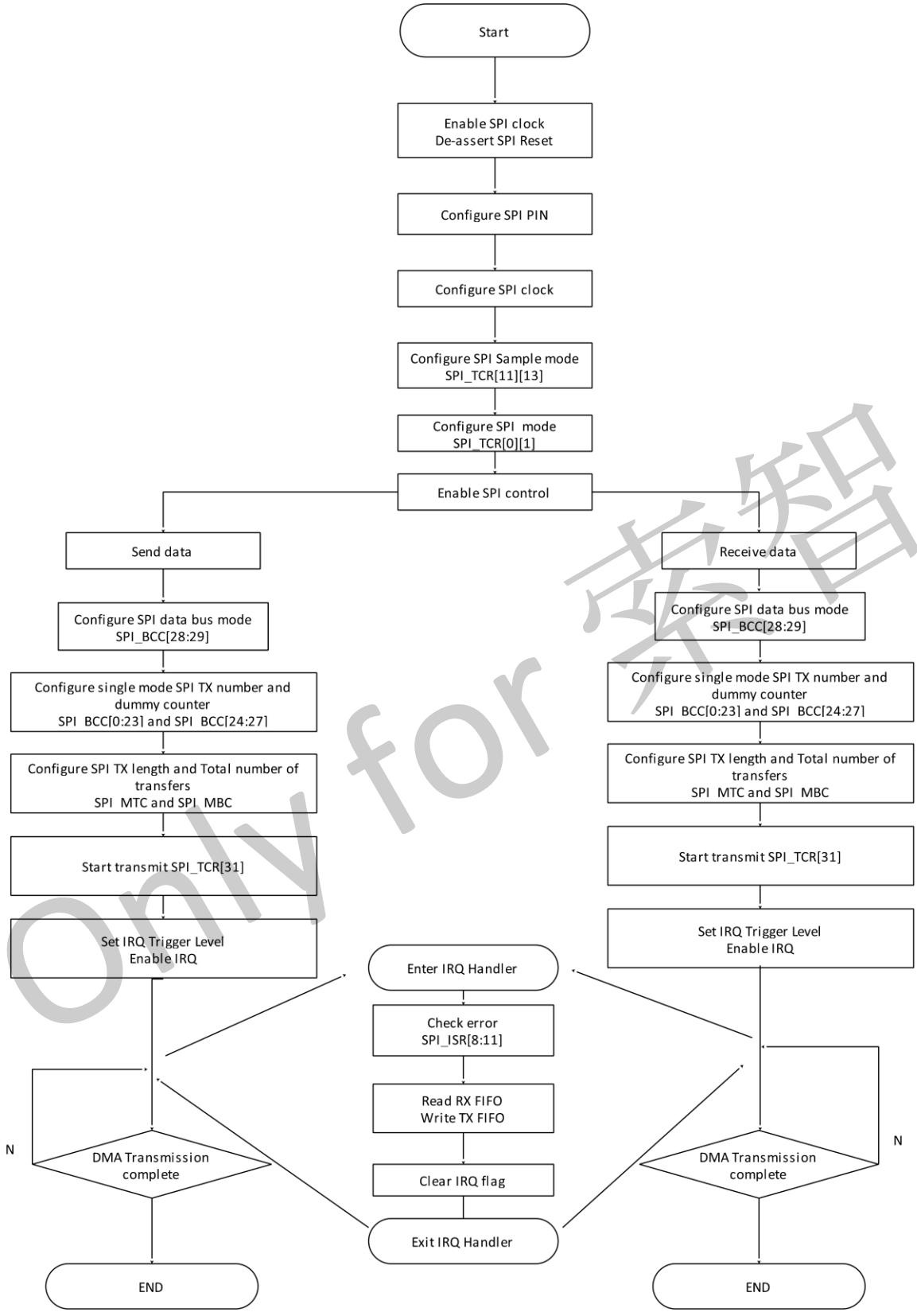

Figure 11- 27. SPI Write/Read Data in CPU Mode

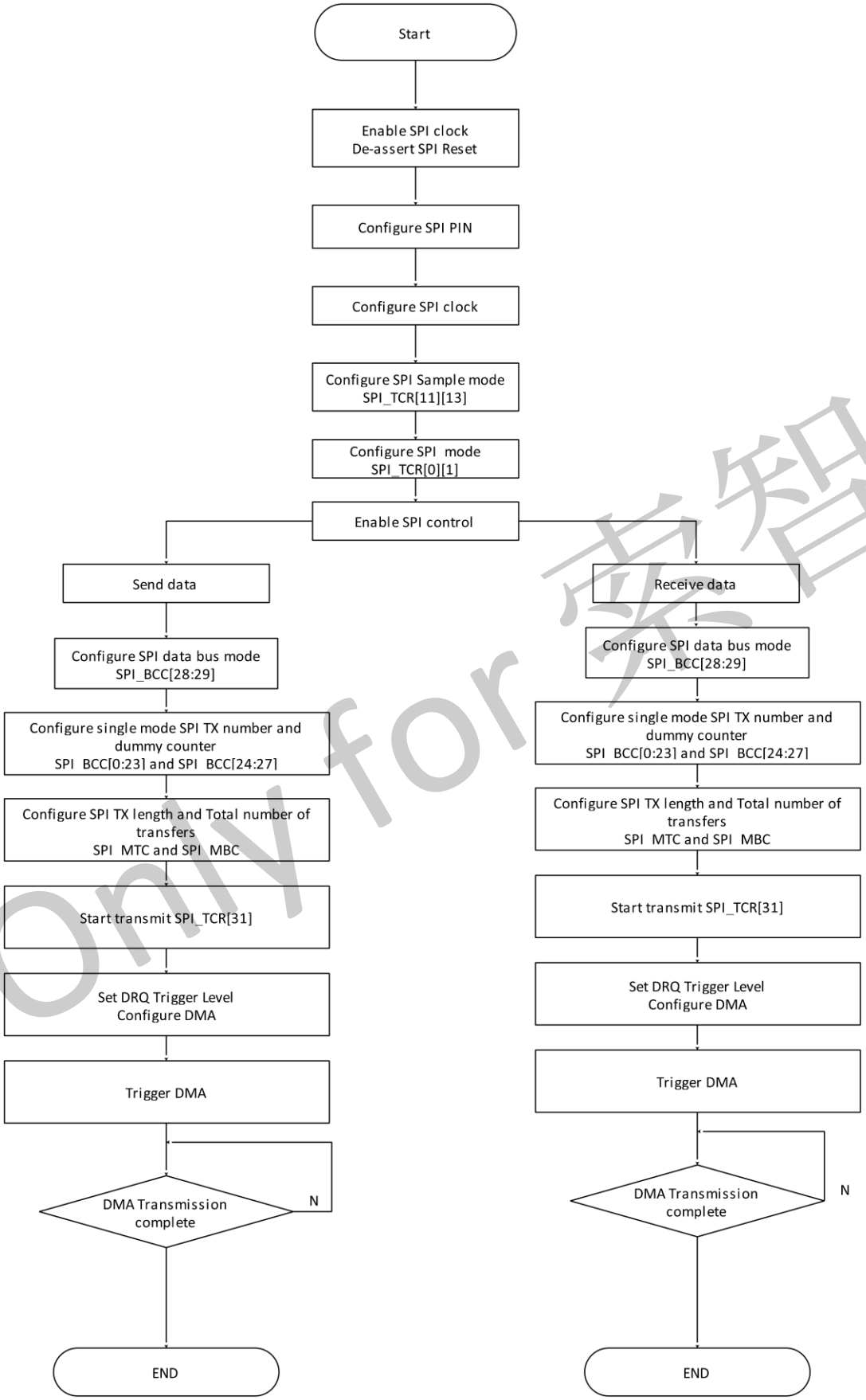

Figure 11- 28. SPI Write/Read Data in DMA Mode

11.3.4.2. Calibrate Delay Chain

The SPI has one delay chain, which is used to generate delay to make proper timing between internal SPI clock signal and data signals. Delay chain is made up with 64 delay cells. The delay time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SPI. In order to calibrate delay chain by operation registers in SPI, the SPI must be enabled through AHB reset and AHB clock gating control registers.

Step2: Configure a proper clock for SPI. Calibration delay chain is based on the clock for SPI from CCU.

Step3: Set proper initial delay value. Write 0xA0 to delay control register to set initial delay value 0x20 to delay chain. Then write 0x0 to delay control register to clear this value.

Step4: Write 0x8000 to delay control register to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in delay control register) of calibration done is set. The number of delay cells is shown at Bit8~Bit14 in delay control register. The delay time generated by these delay cells is equal to the cycle of SPI's clock nearly. This value is the result of calibration.

Step6: Calculate the delay time of one delay cell according to the cycle of SPI's clock and the result of calibration.

11.3.5. Register List

Module Name	Base Address
SPI0	0x05010000
SPI1	0x05011000
SPI2(only for V833)	0x05012000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control Register
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Counter Register
SPI_CCR	0x0024	SPI Clock Rate Control Register
SPI_MBC	0x0030	SPI Burst Counter Register

SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control Register
SPI_BATCR	0x0040	SPI Bit-Aligned Transfer Configure Register
SPI_BA_CCR	0x0044	SPI Bit-Aligned Clock Configuration Register
SPI_TBR	0x0048	SPI TX Bit Register
SPI_RBR	0x004C	SPI RX Bit Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

11.3.6. Register Description

11.3.6.1. 0x0004 SPI Global Control Register(Default Value: 0x0000_0080)

Offset:0x0004			**Register Name: SPI_GCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing ‘1’ to this bit will clear the SPI controller, and auto clear to ‘0’ when reset operation completes. Writing ‘0’ has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 0: Normal operation, ignore RXFIFO status 1: Stop transmit data when RXFIFO full Cannot be written when XCH=1
6:2	/	/	/
1	R/W	0x0	MODE SPI Function Mode Select 0: Slave mode 1: Master mode Cannot be written when XCH=1
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable After transforming from bit_mode to byte_mode, it must enable the SPI module again.

11.3.6.2. 0x0008 SPI Transfer Control Register(Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Writing “1” to SRST will also clear this bit. Writing ‘0’ to this bit has no effect. Cannot be written when XCH=1.
30:15	/	/	/
14	R/W	0x0	SDDM Sending Data Delay Mode 0:Normal sending 1:Delay sending Set the bit to "1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode 0. Cannot be written when XCH=1.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay sample mode 1: Normal sample mode In normal sample mode, SPI master samples the data at the correct edge for each SPI mode; In delay sample mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode. Cannot be written when XCH=1.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first Cannot be written when XCH=1.
11	R/W	0x0	SDC Master Sample Data Control Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point Cannot be written when XCH=1.
10	R/W	0x0	RPSM Rapids Mode Select

			Select rapid mode for high speed write. 0: Normal write mode 1: Rapid write mode Cannot be written when XCH=1.
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one Cannot be written when XCH=1.
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC. Cannot be written when XCH=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 0: set SS to low 1: set SS to high Cannot be written when XCH=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software Cannot be written when XCH=1.
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Cannot be written when XCH=1.
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Cannot be written when XCH=1.
2	R/W	0x1	SPOL

			SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Cannot be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Cannot be written when XCH=1.

11.3.6.3. 0x0010 SPI Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip select signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable

			1: Enable
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

11.3.6.4. 0x0014 SPI Interrupt Status Register(Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC have been exchanged. In other condition, When set, this bit indicates that all the datas in TXFIFO have been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy

			1: Transfer completed
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available 1: RXFIFO is overflowed
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. TX_WL is the water level of TXFIFO.
3	/	/	/
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP

			RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. RX_WL is the water level of RXFIFO.

11.3.6.5. 0x0018 SPI FIFO Control Register(Default Value: 0x0040_0001)

Offset: 0x0018			**Register Name: SPI_FCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and auto clear to ‘0’ when completing reset operation, writing to ‘0’ has no effect.
30	R/W	0x0	TF_TEST_ENB TX Test Mode Enable 0: Disable 1: Enable **Note: In normal mode, TX FIFO can only be read by SPI controller, writing ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.**
29:25	/	/	/
24	R/W	0x0	TF_DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, writing ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable **Note: In normal mode, RX FIFO can only be written by SPI controller, writing**

			'1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, donot set in normal operation and donot set RF_TEST and TF_TEST at the same time.
13:9	/	/	/
8	R/W	0x0	RF_DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

11.3.6.6. 0x001C SPI FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			**Register Name: SPI_FSR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO … 64: 64 bytes in TX FIFO other: Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO … 64: 64 bytes in RX FIFO other: Reserved

11.3.6.7. 0x0020 SPI Wait Clock Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). Cannot be written when XCH=1. 0: No wait states inserted n: n SPI_SCLK wait states inserted **Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer.**
15:0	R/W	0x0	WCC Wait Clock Counter (In master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted

11.3.6.8. 0x0024 SPI Clock Control Register(Default Value: 0x0000_0002)

Offset: 0x0024			Register Name: SPI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2 Can’t be written when XCH=1.
11:8	R/W	0x0	CDR1_M Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2^CDR1_M). Can’t be written when XCH=1.
7:0	R/W	0x2	CDR2_N Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR2_N + 1)). Can’t be written when XCH=1.

11.3.6.9. 0x0030 SPI Master Burst Counter Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_MBC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts **Note: Total transfer data, includes the TXD, RXD and dummy burst.** **Can't be written when XCH=1.**

11.3.6.10. 0x0034 SPI Master Transmit Counter Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_MTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts Can't be written when XCH=1.

11.3.6.11. 0x0038 SPI Master Burst Control Counter Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	Quad_EN Quad_Mode_EN 0: Quad mode disable 1: Quad mode enable Cannot be written when XCH=1. **Note: Quad mode includes Quad-Input and Quad-Output.**

28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode Cannot be written when XCH=1. It is only valid when Quad_Mode_EN=0.
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data does not care by the device. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts. 0: 0 burst 1: 1 burst … N: N bursts Cannot be written when XCH=1.

11.3.6.12. 0x0040 SPI Bit-Aligned Transfer Configure Register(Default Value: 0x0000_00A0)

Offset: 0x0040			**Register Name: SPI_BATC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TCE Transfer Control Enable In master mode, it is used to start to transfer the serial bits frame, it is only valid when ***Work Mode Select==0x10/0x11.*** 0: Idle 1: Initiates transfer Writing “1” to this bit will start to transfer serial bits frame(the value comes from the ***SPI TX Bit Register*** or ***SPI RX Bit Register***), and will auto clear after the bursts transfer completely. Writing ‘0’ to this bit has no effect.
30	R/W	0x0	MSMS Master Sample Standard 0: Delay Sample Mode 1: Standard Sample Mode In Standard Sample Mode, SPI master samples the data at the standard

			rising edge of SCLK for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the standard rising edge of SCLK defined in respective SPI mode.
29:26	/	/	/
25	R/W1C	0x0	TBC Transfer Bits Completed When set, this bit indicates that the last bit of the serial data frame in ***SPI TX Bit Register****(or* ***SPI RX Bit Register****)* has been transferred completely. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed It is only valid when ***Work Mode Select==0x10/0x11.***
24	R/W	0x0	TBC_INT_EN Transfer Bits Completed Interrupt Enable 0: Disable 1: Enable It is only valid when ***Work Mode Select==0x10/0x11.***
23:22	/	/	/
21:16	R/W	0x00	Configure the length of serial data frame(burst) of RX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
15:14	/	/	/
13:8	R/W	0x00	Configure the length of serial data frame(burst) of TX 000000: 0bit 000001: 1bit … 100000: 32bits Other values: reserved It is only valid when ***Work Mode Select==0x10/0x11,*** and cannot be written when TCE=1.
7	R/W	0x1	SS_LEVEL When control SS signal manually , set this bit to ‘1’ or ‘0’ to control the level of SS signal. 0: Set SS to low 1: Set SS to high It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this

			bit is set to 1, software must manually write SPI_CTL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
5	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) It is only valid when ***Work Mode Select==0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
4	/	/	/
3:2	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted It is only valid when ***Work Mode Select= =0x10/0x11,*** and only ***work in Mode0***, cannot be written when TCE=1.
1:0	R/W	0x0	Work Mode Select 00: Data frame is byte aligned in standard SPI, dual-output/dual input SPI, dual IO SPI and quad-output/quad-input SPI. 01: Reserved 10: Data frame is bit aligned in 3-wire SPI 11: Data frame is bit aligned in standard SPI

11.3.6.13. 0x0044 SPI Bit-Aligned CLOCK Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0044			**Register Name: SPI_BA_CCR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CDR_N Clock Divide Rate (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(CDR_N + 1)).

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

11.3.6.14. 0x0048 SPI TX Bit Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SPI_TBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VTB The Value of the Transmit Bits This register is used to store the value of the transmitted serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

11.3.6.15. 0x004C SPI RX Bit Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SPI_RBR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	VRB The Value of the Receive Bits This register is used to store the value of the received serial data frame. In the process of transmission, the LSB is transmitted first.

NOTE

This register is only valid when *Work Mode Select==0x10/0x11*.

11.3.6.16. 0x0088 SPI Normal DMA Mode Control Register(Default Value: 0x0000_00E5)

Offset: 0x0088			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R/W	0x11	00:dma_active is low 01:dma_active is high 10:dma_active is controlled by dma_request(DRQ) 11:dma_active is controlled by controller
5	R/W	0x1	0: active fall do not care ack 1: active fall must after detect ack is high
4:0	R/W	0x05	Delay Cycles The counts of hold cycles from DMA last signal high to dma_active high

11.3.6.17. 0x0200 SPI TX Data Register(Default Value: 0x0000_0000)

Offset: 0x0200	Register Name: SPI_TXD

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in TXFIFO, one burst data is written to TXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increased by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **NOTE** **This address is writable-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

11.3.6.18. 0x0300 SPI RX Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decreased by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **NOTE** **This address is readable-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

11.4. USB2.0 OTG

11.4.1. Overview

The USB2.0 OTG is a dual-role device controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB2.0 Specification. It can support high-speed (HS, 480 Mbit/s), full-speed (FS, 12 Mbit/s), and low-speed (LS, 1.5 Mbit/s) transfers in Host mode. It can support high-speed (HS, 480 Mbit/s), and full-speed (FS, 12 Mbit/s) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB-OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB-OTG FIFO. The USB-OTG core also supports USB power saving functions.

The USB2.0 OTG has the following features:

- Complies with USB2.0 Specification
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s) in Host mode
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 8 User-Configurable Endpoints for Bulk, Isochronousl and Interrupt bi-directional transfer
- Supports up to (4KB+64Bytes) FIFO for all EPs (including EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power optimization and power management capabilities
- Includes interface to an external normal DMA controller for every EPs

11.4.2. Block Diagram

Figure 11-29 shows the block diagram of USB2.0 OTG Controller.

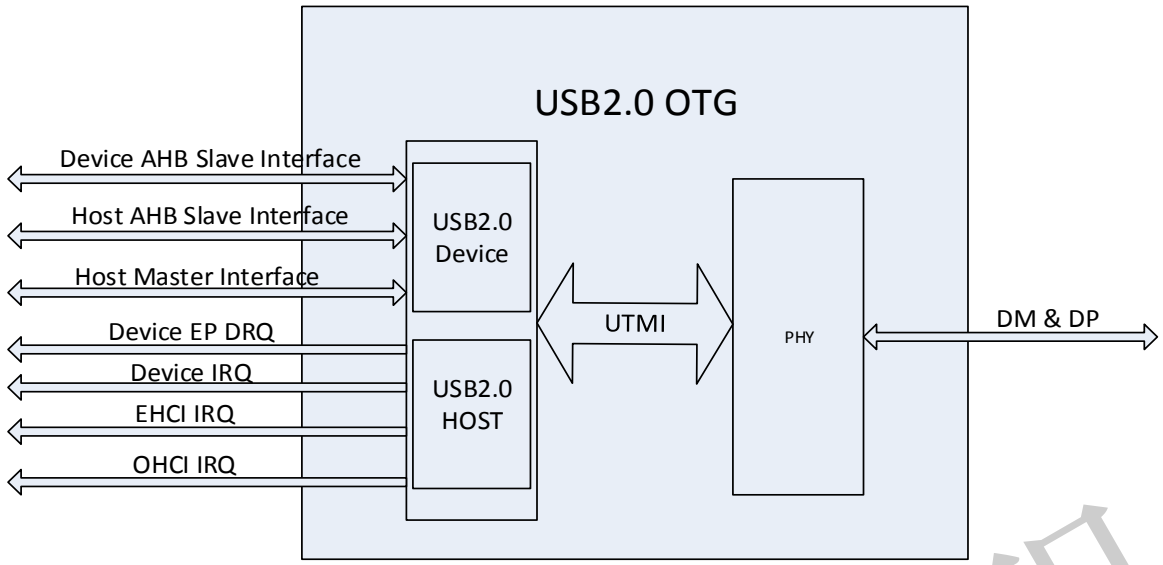

Figure 11- 29. USB2.0 OTG Controller Block Diagram

11.4.3. Operations and Functional Descriptions

11.4.3.1. External Signals

Table 11- 12. USB2.0 OTG External Signals

Signal	Description	Type
USB0_DP	USB2.0 OTG differential signal positive	AI/O
USB0_DM	USB2.0 OTG differential signal negative	AI/O

11.4.3.2. Controller and PHY Connection Diagram

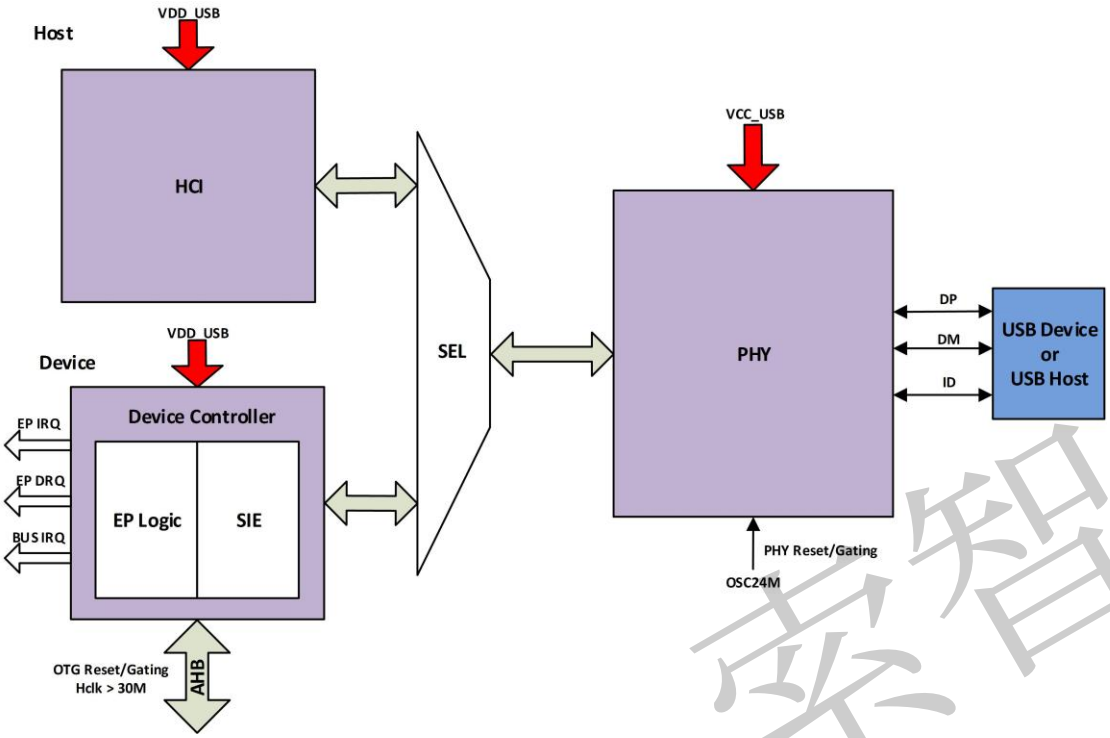

Figure 11- 30. USB2.0 OTG Controller and PHY Connection Diagram

11.4.3.3. USB2.0 OTG-Host Clock and Reset System

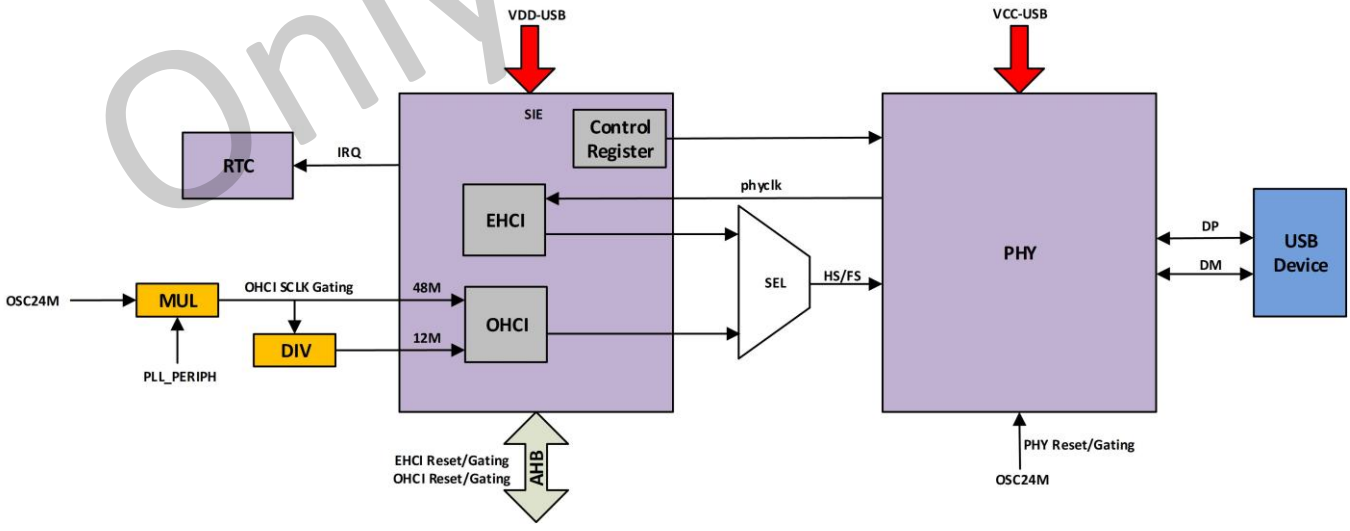

Figure 11- 31. USB2.0 OTG-Host Clock and Reset System

11.5. One Wire Interface

11.5.1. Overview

The One Wire Interface implements the hardware protocol of the Master function of the 1-Wire protocol, which uses a single wire for communication between the Master (1-Wire controller) and the Slave (1-Wire external compliant devices).

The One Wire Interface is implemented as an open-drain output at the device level. Therefore, an external pull-up resistance is required and protocol use the return-to-1 mechanism (that is, after any command by any of the connected devices, the line is pulled to a logical high level).

The One Wire Interface can work at simple mode or standard mode at one time.

The One Wire Interface has the following features:

- Hardware implement of 1-Wire protocol
- Supports master function
- Supports simple mode and standard mode

11.5.2. Block Diagram

The block diagram of the One Wire Interface is shown below.

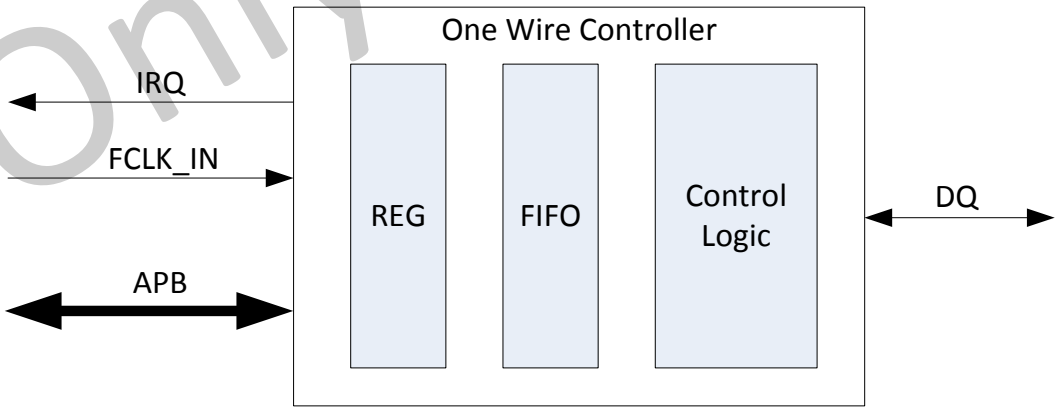

Figure 11- 32. One Wire Interface Block Diagram

11.5.3. Operations and Functional Descriptions

11.5.3.1. External Signals

Table 11-13 describes the external signals of One Wire Interface.

Table 11- 13. One Wire Interface External Signals

Signal Name	Description	Type
ONEWIRE	Data In/Out of One Wire Interface	I/O

11.5.3.2. Clock and Reset

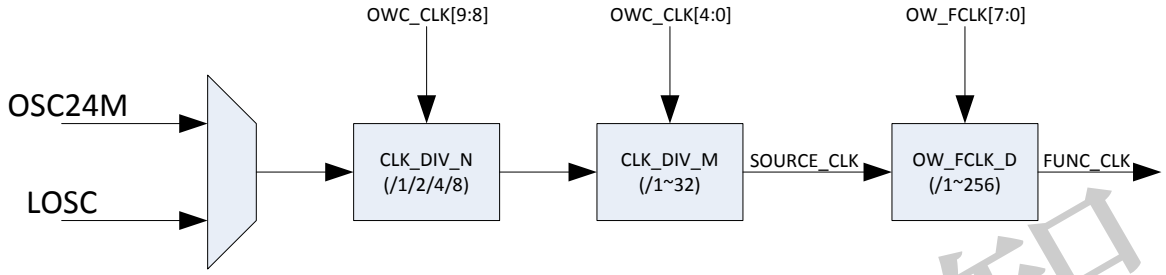

Figure 11- 33. One Wire Interface Clock Description

11.5.3.3. Typical Application

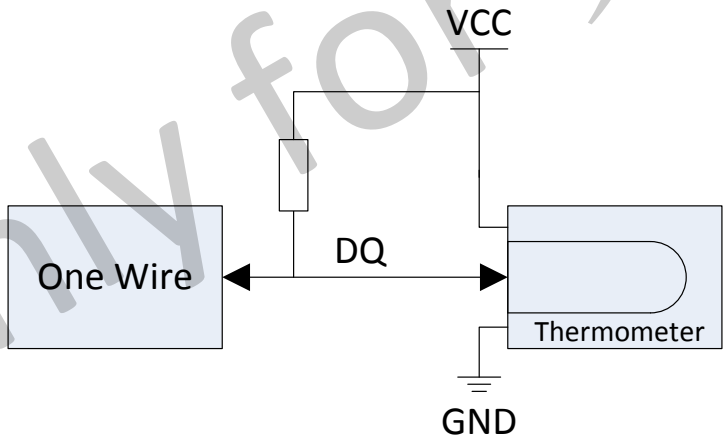

Figure 11- 34. One Wire Interface Typical Application

11.5.3.4. Function Implementation

11.5.3.4.1. Simple Mode

The bus of Simple mode is a master-slave bus system using a simple one-wire, asynchronous, bi-directional, serial interface with a maximum bit-rate of about 5kbit/s.

It is a command-based protocol in which the host sends a command byte to the slave. The command directs the slave

either to store the next eight bits of data received to a register specified by the command byte (Write command), or to output the eight bits of data from a register specified by the command byte (Read command). Command and data bytes consist of a stream of bits where the least-significant bit of a command or data byte is transmitted first. The first 7 bits of the command word are the register address and the last command bit transmitted is the read/write (R/W) bit. The following figure illustrates a typical read cycle.

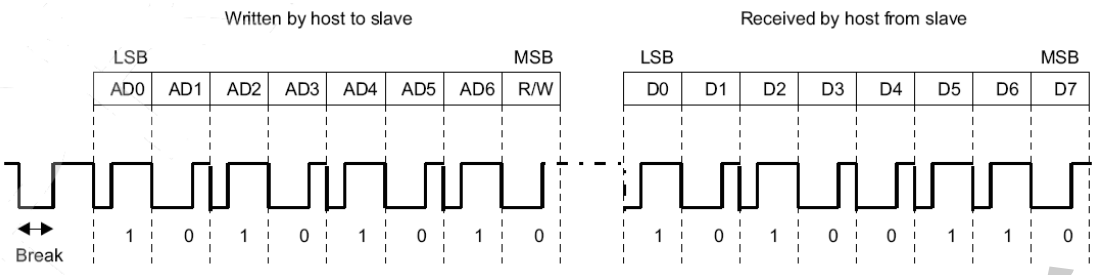

Figure 11- 35. Typical Read Cycle

In the figure, the 1 of the R/W bit indicates a write command where the 0 indicates the read command.

In Simple mode, the slave can be reset by using the break pulse. If the host does not get an expected response from the slave or if the host needs to restart a communication before it is complete, the host can hold the line low and generate a break to reset the communication engine. The break timing is illustrated as follow.

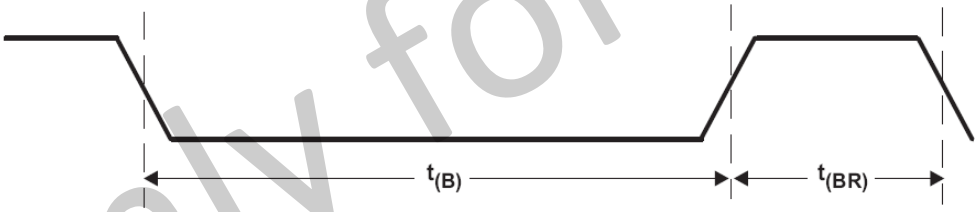

Figure 11- 36. Break Timing

Table 11- 14. Break Timing Parameters

Timing Parameter	For Device	Minimum	Maximum
t(B)	All	190us	
t(BR)	All	40us	

It is not required, but it is recommended to precede each communication with a break for the reliable communication.

After a successful break pulse (if have), the host and slave are ready for bit transmission. Each bit to transmit (either from the host to the slave or from the slave to the host) is preceded by a low-going edge on the line.

The host transmitted bit timing is shown in Figure 11-37.

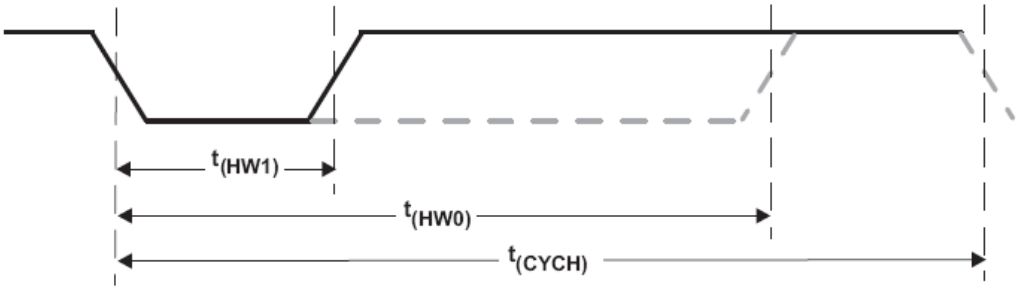

Figure 11- 37. Host Bit Timing

And the slave transmitted bit timing is shown in Figure 11-38.

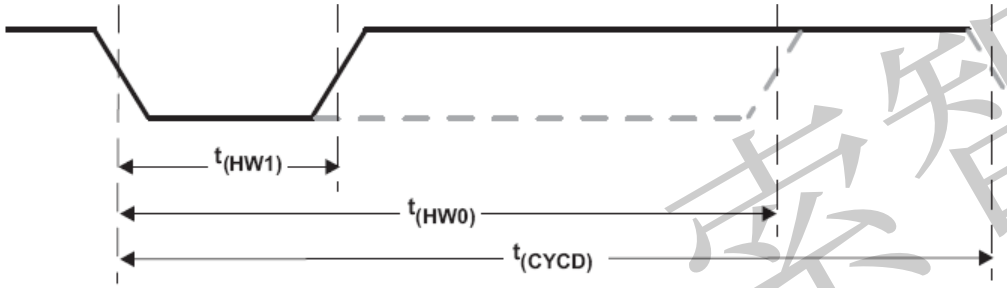

Figure 11- 38. Slave Bit Timing

After the last bit of address is sent on a read cycle, the slave starts outputting the data after the specified response time, t(RSPS). The response time is measured from the fall time of the command R/W bit to the fall time of the first data bit returned by the slave and therefore includes the entire bit time for the R/W bit. Because the minimum response time equal to the minimum bit cycle time, this means that the first data bit may begin as soon as the command R/W bit time ends. The timing is shown as follows.

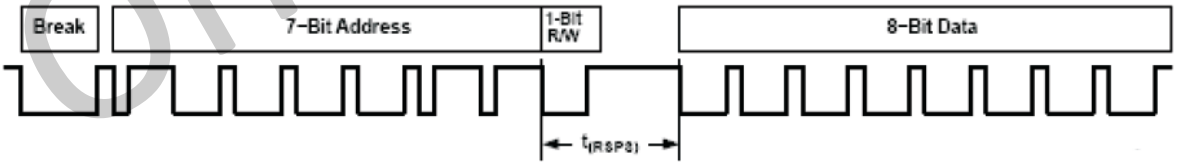

Figure 11- 39. t(RSPS) Requirement

Table 11- 15. Response Time Parameters

Timing Parameter	For Device	Minimum	Maximum
t(RSPS)	All	190us	320us

Also, to avoid short noise spike coupled onto the HDQ line, some filtering may be prudent.

11.5.3.4.2. Standard Mode

The Standard mode consists of 4 types of signaling on the data line, which are Initialization Sequence, Write Zero, Write One and Read Data.

The host first sends an initialization pulse and then waits for the slave to respond with a presence pulse before enabling any communication sequence. The initialization pulse and presence pulse are shown as follows.

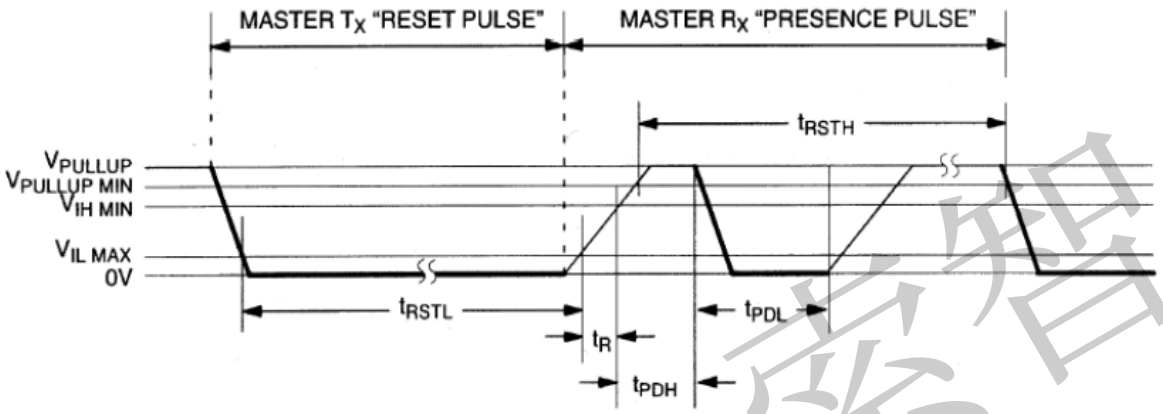

Figure 11- 40. Initialization Pulse and Presence Pulse

Table 11- 16. Initialization Pulse and Presence Pulse Timing Parameters

Timing Parameter	Minimum	Maximum
t(RSTL)	480us	-
t(RSTH)	480us	-
t(PDH)	15us	60us
t(PDL)	60us	240us

The other two types of signal are Writing Zero and Writing One. Both writing time slots must be a minimum of 60us in duration with a minimum of a 1us recovery time between individual write cycles. The slave device samples the data line in a window of 15us to 60us after the data line falls. If the line is high, a Write One occurs. If the line is low, a Write Zero occurs.

The Writing Zero time slot is shown as follows.

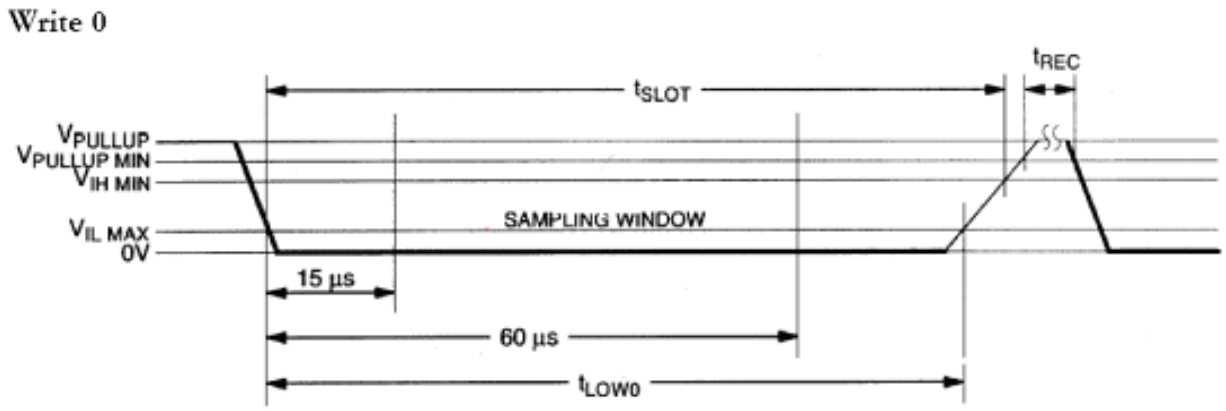

Figure 11- 41. Writing 0 Time Slot

Table 11- 17. Writing 0 Time Slot Timing Parameters

Timing Parameter	Minimum	Maximum
T(LOW0)	60us	t(SLOT)
t(SLOT)	T(LOW0)	120 us
t(REC)	1us	

When Writing One occurs, the data line must be pulled to a logic low level and then released, allowing the data line to pull up to a high level within 15us after the start of the writing time slot. The Writing One time slot is shown as follows.

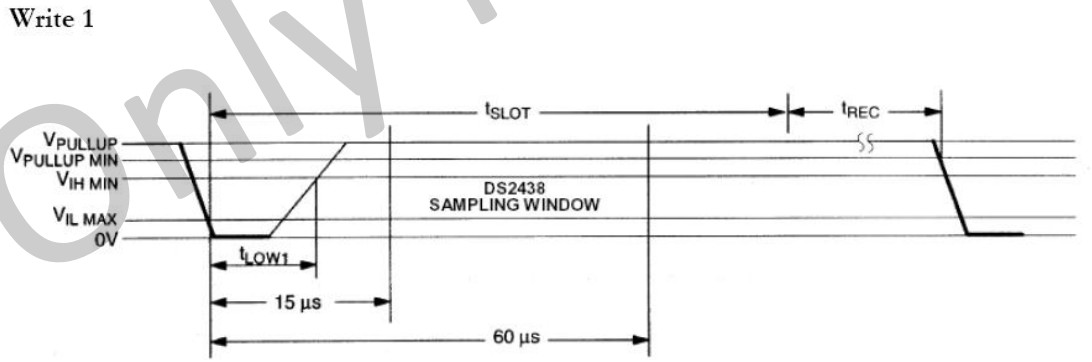

Figure 11- 42. Writing 1 Time Slot

Table 11- 18. Writing 1 Time Slot Timing Parameters

Timing Parameter	Minimum	Maximum
t(SLOT)	60us	120 us
t(LOW1)	1us	15us
t(REC)	1us	

The last signal type is Read Data. A reading time slot is initiated when the bus master pulls the data line from a logic high level to logic low level. The data line must remain at a low logic level for a minimum of 1 us; output data from the slave is valid within the next maximum 14us.

The bus master therefore must stop driving the data line low in order to read its state 15us from the start of the read slot. All read time slots must be a minimum of 60us in duration with a minimum of a 1us recovery time between individual read slots. The Read Data slot is shown as follows.

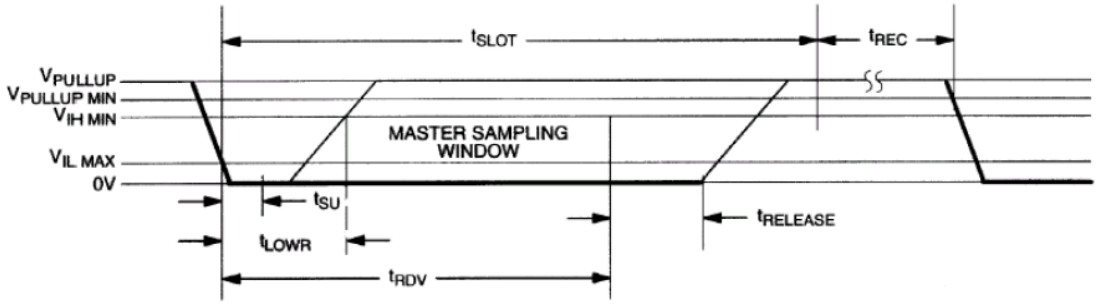

Figure 11- 43. Read Data Slot

Table 11- 19. Read Data Slot Timing Parameters

Timing Parameter	Minimum	Maximum
t(SU)		1us
t(LOWR)	1us	15us
t(RDV)	(= 15us)	
t(RELEASE)	0us	45us
t(SLOT)	60 us	120 us
t(REC)	1us	

Cyclic Redundancy Check (CRC) is used by One Wire devices to ensure data integrity. Two different CRC are commonly found in Standard mode. There are one 8 bit CRC and one 16 bit CRC. CRC8 is used in the ROM section of all devices. CRC8 is also in some devices used to verify other data, like commands issued on the bus. CRC16 is used by some devices to check for errors on larger data sets.

11.5.4. Programming Guidelines

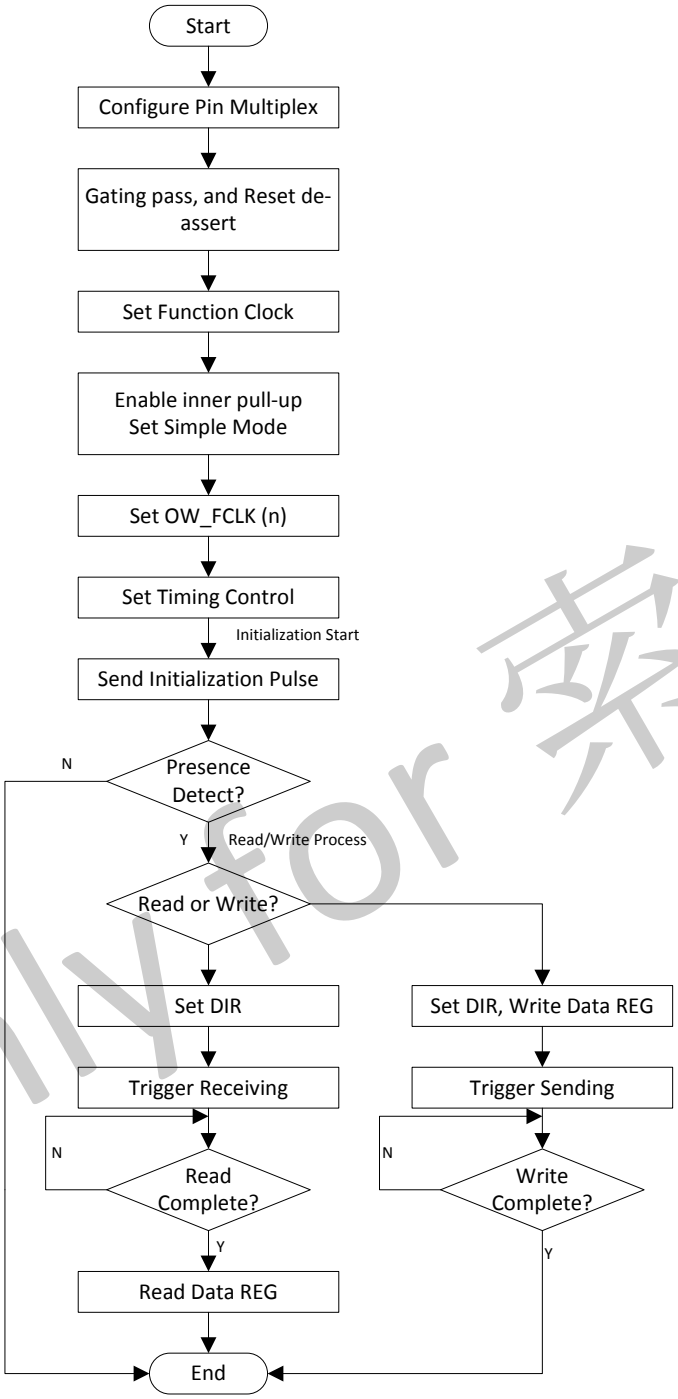

Figure 11- 44. One Wire Interface Write/Read Process

11.5.5. Register List

Module Name	Base Address
R_OWC	0x07040400

Register Name	Offset	Description
OW_DATA	0x0000	One Wire Data Register
OW_CTL	0x0004	One Wire Control Register
OW_SMSC	0x0008	One Wire Standard Mode Special Control Register
OW_SMCRC	0x000C	One Wire Standard Mode CRC Register
OW_INT_STATUS	0x0010	One Wire Interrupt Status Register
OW_INT_MASK	0x0014	One Wire Interrupt Mask Register
OW_FCLK	0x0018	One Wire Function Clock Register
OW_LC	0x001C	One Wire Line Control Register
SM_WR_RD_TCTL	0x0020	Standard Mode Write Read Timing Control Register
SM_RST_PRESENCE_TCTL	0x0024	Standard Mode Reset Presence Timing Control Register
SP_WR_RD_TCTL	0x0028	Simple Mode Timing Control Register
SP_BR_TCTL	0x002C	Simple Mode Break Timing Control Register

11.5.6. Register Description

11.5.6.1. 0x0000 One Wire Data Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: OW_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	SM_DATA These fields are for Simple mode data send or receive in a one wire transmission. After this byte data transfer finishing, a transmission complete interrupt will generate.
15:8	/	/	/
7:0	R/W	0x0	OW_DATA Data byte for transmitting or received In Simple mode, these fields are for the command byte transmission. When GO bit is set (the INITIALIZATION/BREAK bit is not set at the same time), these fields will be sent as the address and command for a Simple mode transfer. After the command byte transmission finished, the controller in Simple mode will send next 8-bit data from SM_DATA when the DIR bit is 1 or receive one byte data to SM_DATA when the DIR bit is 0. In Standard mode, if the INITIALIZATION/BREAK bit is not set, the controller samples/sends data to/from these fields determining by the DIR bit when the Go bit is set. When the ONE_WIRE_SINGLE_BIT is enabled, only the first bit of these fields is available.

11.5.6.2. 0x0004 One Wire Control Register(Default Value: 0x0003_0000)

Offset: 0x0004	Register Name: OW_CTL

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	/	/	/
19:16	R/W	0x3	SAMPLE_TIME These fields determine the sample times in digital circuit.
15:10	/	/	/
9	R/W	0x0	INNER_PULL_UP_ENABLE When this bit is set, the inner pull up for one wire bus is determined by inner output (pull up is off when bus is drive 0) 0: Inner pull up is on 1: Inner pull up is off when bus is drive 0
8	R/W	0x0	AUTOIDLE Auto Idle 0: Module clock is free-running 1: Module clock is in power saving mode: the function clock is running only when module is accessed or inside logic is in function to process events.
7	/	/	/
6	R	0x0	PRESENCEDETECT Slave Presence Indicator This read-only flag is only used in Standard mode. The value of this field indicates whether there is Presence Pulse responding to the host initialization pulse. The flag is updated when the OW_INT_STATUS[0] Presence Detect Interrupt Flag is set.
5	R/W	0x0	STANDARD_MODE_SINGLE_BIT The single-bit mode is only supported for Standard mode. After the bit is transferred, Tx-complete or Rx-complete interrupt will generate for corresponding transfer operation. 0: Disabled 1: Enabled
4	R/W	0x0	Go Go Bit Write 1 to start the appropriate operation. If the INITIALIZATION/BREAK bit is set, the controller generates the initialization or break pulse. If the INITIALIZATION/BREAK bit is not set, the controller in Standard mode samples/sends data to/from the OW_DATA fields determining by the DIR bit, or controller in Simple mode begins a transfer sequence with the command byte in OW_DATA. Bit returns to 0 after the operation is complete.
3	R/W	0x0	INITIALIZATION/BREAK Initialization/Break Bit Write 1 to send initialization pulse for the Standard mode or break pulse for the Simple mode. The OW_DATA register will be flushed when initialization or the break situation is generating. Bit returns to 0 after pulse is sent.

			The pulse generates after the Go bit is set.
2	R/W	0x0	DIR Direction Bit In Standard mode, this field determines if next operation (byte operation or bit operation) is read or write. In Simple mode, this field determines if the current transfer sequence is read or write. 0 : Read 1: Write The operation starts after the Go bit is set.
1	R/W	0x0	MS Mode Selection Bit 0: Standard Mode 1: Simple Mode
0	R/W	0x0	GEN Global Enable This field is used to enable or disable the One Wire Controller. A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

11.5.6.3. 0x0008 One Wire Standard Mode Special Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: OW_SMSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:6	/	/	/
5	R/W	0x0	CRC_ERROR_STATUS These fields indicate the result of the CRC comparing. 0: CRC comparing right 1: CRC comparing wrong
4	/	/	/
3	R/W	0x0	MEM_CRC_COMPARE This field is only used in Standard mode. When this field is set, the controller will compare the value in the CRC_RECEV field with the data read from the CRC_CALC_INDICATE field, and then returns corresponding result in the CRC_ERROR_STATUS field and generates CRC finish interrupt. The CRC shift register and CRC_CALC_INDICATE field will be cleared to 0. This field will be automatically cleared when the CRC compare is finished.
2	R/W	0x0	CRC_16BIT_EN This field is only used in Standard mode. and is set to 1 to select 16-bit CRC, else the 8-bit CRC is selected. 0: CRC_8BIT_EN

			1: CRC_16BIT_EN
1	R/W	0x0	WR_MEM_CRC_REQ This field is only used in One Wire mode. When this bit is set, the bit send to the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleared. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.
0	R/W	0x0	RD_MEM_CRC_REQ This field is only used in Standard Mode. When this bit is set, the bit received from the device will be took into calculate the CRC value (CRC8 or CRC16). The calculation will stop when this bit is cleared. The value will be preserved in the corresponding CRC (CRC8 or CRC16) shift register then.

11.5.6.4. 0x000C One Wire Standard Mode CRC Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: OW_SMCRC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	CRC_CALC_INDICATE This field indicates the CRC value calculated by the CRC shift register.
15:0	R/W	0x0	CRC_RECEV The data CRC value (CRC8 or CRC16) will be written to these fields by software for CRC comparing.

11.5.6.5. 0x0010 One Wire Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: OW_INT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	Deglitch Detected Interrupt Flag This flag indicates a deglitch in the bus. The controller looks for any glitch in the sample window for at least 1us. If the Deglitch Interrupt is enabled, an interrupt will issue when any deglitch occurs in the bus. The interrupt condition is cleared by writing “1” to this field.
4	R/W1C	0x0	CRC Comparing Complete Interrupt Flag This flag is used in Standard mode, and is used to indicate the CRC comparing has finished. The interrupt condition is cleared by writing “1” to this field.
3	R/W1C	0x0	Transmission Complete Interrupt Flag In Standard mode, the flag is set when a write operation of one byte or one bit in single-bit mode was completed. The interrupt is generated. In Simple mode, the flag is set when a write operation of one byte was completed. The interrupt is generated. The interrupt condition is cleared by writing “1” to this field.

2	R/W1C	0x0	Read Complete Interrupt Flag In Standard mode, the flag is set when a byte or a bit in single-bit mode has been successfully read. The interrupt is generated. In Simple mode, the flag is set when a byte has been successfully read. The interrupt is generated. The interrupt condition is cleared by writing “1” to this field.
1	R/W1C	0x0	Time-out Interrupt Flag This flag is only used in Simple mode. The flag is set when two event happened. The one event is that after a read command initiated by the host, the slave did not pull the line low within the specified time(512us). The other event is that another bit transfer does not begin after a specified time (512us) from the pre-bit beginning. When the above situation occurs, the interrupt generates and the value of this field is set. The interrupt condition is cleared by writing “1” to this field.
0	R/W1C	0x0	Presence Detect Interrupt Flag In Standard mode, this interrupt status is set when the Initialization Pulse is completed. The interrupt is generated then and the PRESENCEDETECT bit is updated. In Simple mode, the flag is set when the successful completion of a break pulse. The interrupt is generated. The interrupt condition is cleared by writing “1” to this field.

11.5.6.6. 0x0014 One Wire Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0014			**Register Name: OW_INT_MASK**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	Deglitch Detected Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	CRC Comparing Complete Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	Transmission Complete Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	Read Complete Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	Time-out Interrupt Enable 0: Disable 1: Enable

0	R/W	0x0	Presence Detect Interrupt Enable 0: Disable 1: Enable

11.5.6.7. 0x0018 HDQ/One Wire Function Clock Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: OW_FCLK
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	OW_FCLK (n) n-MHz clock is needed to use as a time reference by the machine. Transitions between the states of the state machine as well as actions triggered at precise time deadlines are expressed using the n-MHz clock.
15:8	/	/	/
7:0	R/W	0x0	OW_FCLK_D OW_FCLK = SOURCE_CLK/OW_FCLK_D

11.5.6.8. 0x001C One Wire Line Control Register(Default Value: 0x0000_0004)

Offset: 0x001C			Register Name: OW_LC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x1	Current state of One Wire line 0: Low 1: High
1	R/W	0x0	One Wire line state control bit When the line control mode is enabled (bit [0] set), value of this bit decides the output level of the One Wire line. 0: Output low level 1: Output high level
0	R/W	0x0	One Wire line state control enable When this bit is set, the state of One Wire line is controlled by the value of bit [1]. 0: Disable line control mode 1: Enable line control mode

11.5.6.9. 0x0020 Standard Mode Write Read Timing Control Register(Default Value: 0x213D_E0BC)

Offset: 0x0020			Register Name: OW_SMSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

30:29	R/W	0x1	TSU Read Data Setup. In standard speed, range: t(SU) < 1 00: 0.5us 01: 1us 10: 2us 11: 4us
28	/	/	/
27:24	R/W	0x1	REC Recovery Time, t(recovery) = N us. In standard speed, range: 1us <= t(recovery)
23	/	/	/
22:18	R/W	0xF	TRDV Read data valid time, t(rdv) = N us. In standard speed, range: Exactly 15
17:11	R/W	0x3C	TLOW0 Write Zero time low, Tlow0 = N us. The range setting for TLOW0 is from 0x3c to 0x77. In standard mode, range:60<= t(low0) < t(tslot) <120
10:7	R/W	0x1	TLOW1 Write One time low, or TLOWR both are same. t(low1) = N us. The range setting for TLOW1 and TLOWR here is from 0x1 to 0xf. In standard speed, range:1 <= t(low1) < 15. t(lowR) = N owr clks. In standard speed, rang = 1 <= t(lowR) <15
6:0	R/W	0x3C	TSLOT Active time slot for write and read data, t(slot) = N us. The range setting for TSLOT is from 0x3c to 0x78. In standard mode, range:60 <= t(slot) <120

11.5.6.10. 0x0024 Standard Mode Reset Presence Timing Control Register(Default Value: 0x3C3F_C1E0)

Offset: 0x0024			**Register Name: SM_RST_PRESENCE_TCTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x3c	TPDL PRESENCE_DETECT_LOW t(pdl) = N us. The range setting for TPDL in these fields is from 0 to 0xf0. In standard speed, Range: 60 <= t(pdl) <240.
23:18	R/W	0xf	TPDH PRESENCE_DETECT_HIGH t(pdh) = N us. The range setting for TPDH in these fields is from 0xf to 0x3c. In standard speed, range: 15 <= t(pdh) < 60 .
17:9	R/W	0x1e0	TRSTL RESET_TIME_LOW t(rstl) = N us. The range setting for TRSTL in these fields is from 0 to 0xff. In standard speed, Range: 480 <= t(rstl) < infinity
8:0	R/W	0x1e0	TRSTH RESET_TIME_HIGH, t(rsth) = N us. The range setting for TRSTH in these fields is from 0 to 0xff. In standard speed, Range : 480 <= t(rsth) < infinity

11.5.6.11. 0x0028 Simple Mode Write Read Timing Control Register(Default Value: 0x0A01_58BE)

Offset: 0x0028			Register Name: SP_WR_RD_TCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	RD_SAMPLE_POINT When controller of the Simple mode read, the default sample point is at the middle of the THW1 point and the THW0 point, named S(middle). When these fields are set, the corresponding new sample point will be determined. 0000 S(middle) / 1000 S(middle)-30us 0001 S(middle)+5us / 1001 S(middle)+40us 0010 S(middle)-5us / 1010 S(middle)-40us 0011 S(middle)+10us / 1011 S(middle)+50us 0100 S(middle)-10us / 1100 S(middle)-50us 0101 S(middle)+20us / 1101 S(middle)+60us 0110 S(middle)-20us / 1110 S(middle)-60us 0111 S(middle)+30us / 1111 reserve
27:22	R/W	0x28	THW1_INT t(HW1_INT) = N us. The range setting for THW1_INT in these fields is from 0 to 0x3f, which is the integer part of the THW1. In HDQ mode, Range: t(HW0) <= 50us.
21:18	R/W	0x0	THW1_DEC THW1_DEC is the decimal part of the THW1. t(HW1_DEC) = N ow_clks. The value for the THW1 = THW1_INT + THW1_DEC.
17:10	R/W	0x56	THW0 t(HW0) = N us. The range setting for THW0 in these fields is from 0 to 0xff. In HDQ mode, Range: t(HW0) <= 145us.
9:0	R/W	0xbe	TCYCH t(CYCH) = N us. The range setting for TCYCH in these fields is from 0 to 0x3ff. In HDQ mode, Rang: 190 us <= t(CYCH) <= infinity.

11.5.6.12. 0x002C Simple Mode Break Timing Control Register(Default Value: 0x00BE_0028)

Offset: 0x002C			Register Name: HDQ_ BR_TCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0xbe	TB t(B) = N us. The range setting for TB in these fields is from 0 to 0x 3ff. In HDQ mode, Rang: 190 us <= t(B) <= infinity.
15:10	/	/	/
9:0	R/W	0x28	TBR t(BR) = N us. The range setting for TBR in these fields is from 0 to 0xff. In HDQ mode, Rang: 40 us <= t(BR) <= infinity.

11.6. Port Controller

11.6.1. Overview

The Port Controller can be configured with multi-functional input/output pins. All these ports can be configured as GPIO only if multiplexed functions are not used. The total 8 group external PIO interrupt sources are supported and interrupt mode can be configured by software.

The Port Controller has the following features:

- 8 ports(PC,PD,PE,PF,PG,PH,PI,PL)
- Software control for each signal pin
- GPIO peripheral can produce interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 99 interrupts
- Configurable interrupt edges

11.6.2. Block Diagram

The block diagram of port controller is shown in Figure 11-45.

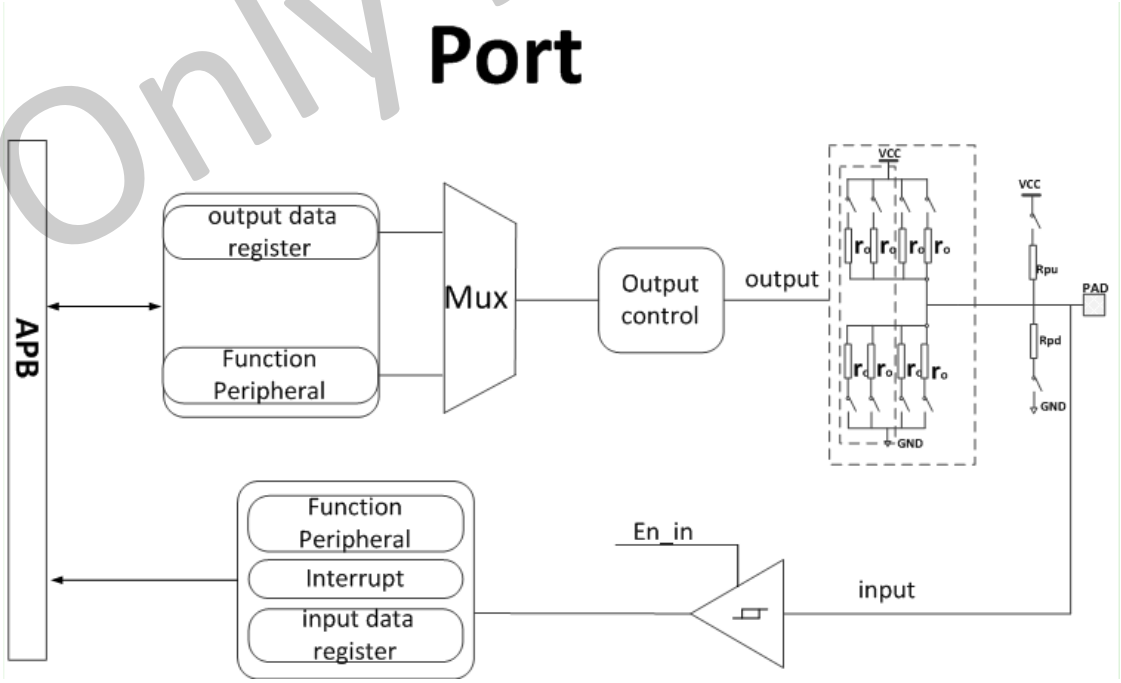

Figure 11- 45. Port Controller Block Diagram

Port controller consists of digital part(GPIO, external interface) and IO analog part(output buffer, dual pull down, pad, etc). Digital part can select output interface by MUX switch; analog part can configure pull up/down, buffer strength.

When executing GPIO read state, the port controller reads the current level of pin into internal register bus. When not executing GPIO read state, external pin and internal register bus is off-status, that is high-impedance.

11.6.3. Operations and Functional Descriptions

11.6.3.1. Multi-function Port Table

The V833 includes 99 multi-functional input/output port pins. There are 8 ports as listed below:

Table 11- 20. V833 Multi-function Port Table

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PC	12	Schmitt	CMOS	SPI/SDC/PC-EINT	1.8V/3.3V
PD	23	Schmitt	CMOS	LCD/PWM/I2S/RMII/DSPO/PD-EINT	1.8V/3.3V
PE	22	Schmitt	CMOS	NCSI/RGMII/RMII/SPI/TWI/UART/PE-EINT	1.8V/2.8V/ 3.3V
PF	7	Schmitt	CMOS	SDC/JTAG/UART/PF-EINT	1.8V
PG	8	Schmitt	CMOS	SDC/UART/PG-EINT	1.8V/3.3V
PH	16	Schmitt	CMOS	PWM/JTAG/I2S/RMII/SPI/TWI/UART/ONEWIRE/ PH-EINT	3.3V
PI	5	Schmitt	CMOS	CSI/SPI/TWI/PI-EINT	1.8V/2.8V/ 3.3V
PL	6	Schmitt	CMOS	RSB/TWI/PL-EINT	1.8V/3.3V

The V831 includes 53 multi-functional input/output port pins. There are 7 ports as listed below:

Table 11- 21. V831 Multi-function Port Table

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PC	6	Schmitt	CMOS	SPI/PC-EINT	3.3V
PD	12	Schmitt	CMOS	LCD/PWM/I2S/RMII/DSPO/PD-EINT	3.3V
PE	2	Schmitt	CMOS	TWI	3.3V/1.8V
PF	7	Schmitt	CMOS	SDC/JTAG/UART/PF-EINT	3.3V
PG	8	Schmitt	CMOS	SDC/UART/PG-EINT	3.3V
PH	15	Schmitt	CMOS	PWM/JTAG/I2S/RMII/SPI/TWI/UART/ONEWIRE/ PH-EINT	3.3V
PI	3	Schmitt	CMOS	CSI/TWI/PI-EINT	1.8V

The multiplex function pins between V833 and V831 are shown in Table 11-22 to Table 11-29 .

Table 11- 22. PC Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	Support	PC0	-	SDC2_DS	SPI0_CLK	-	PC_EINT0

Support	Support	PC1	-	SDC2_RST	SPI0_CS0	-	PC_EINT1
Support	Support	PC2	-	SDC2_CLK	SPI0_MOSI	-	PC_EINT2
Support	Support	PC3	-	SDC2_CMD	SPI0_MISO	-	PC_EINT3
Support	Support	PC4	-	SDC2_D3	SPI0_WP	-	PC_EINT4
Support	Support	PC5	-	SDC2_D4	SPI0_HOLD	-	PC_EINT5
Support	No Support	PC6	-	SDC2_D0	SPI0_CS1	-	PC_EINT6
Support	No Support	PC7	-	SDC2_D5	-	-	PC_EINT7
Support	No Support	PC8	-	SDC2_D1	-	-	PC_EINT8
Support	No Support	PC9	-	SDC2_D6	-	-	PC_EINT9
Support	No Support	PC10	-	SDC2_D2	-	-	PC_EINT10
Support	No Support	PC11	-	SDC2_D7	-	-	PC_EINT11

Table 11- 23. PD Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	No Support	PD0	LCD_D2	-	-	-	PD_EINT0
Support	Support	PD1	LCD_D3	PWM_0	VO_D0	RMII_RXD1	PD_EINT1
Support	Support	PD2	LCD_D4	PWM_1	VO_D1	RMII_RXD0	PD_EINT2
Support	Support	PD3	LCD_D5	PWM_2	VO_D2	RMII_CRS_DV	PD_EINT3
Support	Support	PD4	LCD_D6	PWM_3	VO_D3	RMII_RXER	PD_EINT4
Support	Support	PD5	LCD_D7	PWM_4	VO_D4	RMII_TXD1	PD_EINT5
Support	Support	PD6	LCD_D10	PWM_5	VO_D5	RMII_TXD0	PD_EINT6
Support	Support	PD7	LCD_D11	PWM_6	VO_D6	RMII_TXCK	PD_EINT7
Support	Support	PD8	LCD_D12	PWM_7	VO_D7	RMII_TXEN	PD_EINT8
Support	No Support	PD9	LCD_D13	PWM_8	-	-	PD_EINT9
Support	No Support	PD10	LCD_D14	I2S1_MCLK	VO_D8	-	PD_EINT10
Support	No Support	PD11	LCD_D15	I2S1_BCLK	VO_D9	-	PD_EINT11
Support	No Support	PD12	LCD_D18	I2S1_LRCK	VO_D10	-	PD_EINT12
Support	No Support	PD13	LCD_D19	I2S1_DOUT0	VO_D11	-	PD_EINT13
Support	No Support	PD14	LCD_D20	I2S1_DOUT1	VO_D12	I2S1_DIN1	PD_EINT14
Support	No Support	PD15	LCD_D21	I2S1_DOUT2	VO_D13	I2S1_DIN2	PD_EINT15
Support	No Support	PD16	LCD_D22	I2S1_DOUT3	VO_D14	I2S1_DIN3	PD_EINT16
Support	No Support	PD17	LCD_D23	I2S1_DIN0	VO_D15	-	PD_EINT17
Support	Support	PD18	LCD_CLK	-	VO_CLK	EPHY_25M	PD_EINT18
Support	Support	PD19	LCD_DE	PWM_9	VO_FIELD	TCON_TRIG	PD_EINT19
Support	Support	PD20	LCD_HSYNC	-	VO_HSYNC	MDC	PD_EINT20
Support	Support	PD21	LCD_VSYNC	-	VO_VSYNC	MDIO	PD_EINT21
Support	No Support	PD22	PWM_9	-	-	-	PD_EINT22

Table 11- 24. PE Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	No Support	PE0	NCSI1_PCLK	RGMII_RXD3			PE_EINT0
Support	No Support	PE1	CSI_MASTERCL	RGMII_RXD2			PE_EINT1

			K1				
Support	No Support	PE2	NCSI1_HSYNC	RGMII_RXD1/ RMII_RXD1			PE_EINT2
Support	No Support	PE3	NCSI1_VSYNC	RGMII_RXD0/ RMII_RXD0			PE_EINT3
Support	No Support	PE4	NCSI1_D0	RGMII_RXCK			PE_EINT4
Support	No Support	PE5	NCSI1_D1	RGMII_RXCTL /RMII_CRS_D V			PE_EINT5
Support	No Support	PE6	NCSI1_D2	RGMII_CLKIN /RMII_RXER			PE_EINT6
Support	No Support	PE7	NCSI1_D3	RGMII_TXD3			PE_EINT7
Support	No Support	PE8	NCSI1_D4	RGMII_TXD2			PE_EINT8
Support	No Support	PE9	NCSI1_D5	RGMII_TXD1/ RMII_TXD1			PE_EINT9
Support	No Support	PE10	NCSI1_D6	RGMII_TXD0/ RMII_TXD0			PE_EINT10
Support	No Support	PE11	NCSI1_D7	RGMII_TXCK/ RMII_TXCK			PE_EINT11
Support	No Support	PE12	NCSI1_D8	RGMII_TXCTL /RMII_TXEN			PE_EINT12
Support	No Support	PE13	NCSI1_D9	MDC		TWI1_CLK	PE_EINT13
Support	No Support	PE14	NCSI1_D10	MDIO		TWI1_SDA	PE_EINT14
Support	No Support	PE15	NCSI1_D11	EPHY_25M		NCSI1_FIEL D	PE_EINT15
Support	Support	PE16		LCD_D0		TWI0_SCK	PE_EINT16
Support	Support	PE17		LCD_D1		TWI0_SDA	PE_EINT17
Support	No Support	PE18	NCSI1_D12	LCD_D8	SPI2_CLK	UART2_TX	PE_EINT18
Support	No Support	PE19	NCSI1_D13	LCD_D9	SPI2_MOSI	UART2_RX	PE_EINT19
Support	No Support	PE20	NCSI1_D14	LCD_D16	SPI2_MISO	UART2_RTS	PE_EINT20
Support	No Support	PE21	NCSI1_D15	LCD_D17	SPI2_CS0	UART2_CTS	PE_EINT21

Table 11- 25. PF Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	Support	PF0	SDC0_D1	JTAG_MS	-	CPU_BIST0	PF_EINT0
Support	Support	PF1	SDC0_D0	JTAG_DI	-	CPU_BIST1	PF_EINT1
Support	Support	PF2	SDC0_CLK	UART0_TX	-	-	PF_EINT2
Support	Support	PF3	SDC0_CMD	JTAG_DO	-	-	PF_EINT3
Support	Support	PF4	SDC0_D3	UART0_RX	-	-	PF_EINT4
Support	Support	PF5	SDC0_D2	JTAG_CK	-	-	PF_EINT5
Support	Support	PF6	-	-	-	-	PF_EINT6

Table 11- 26. PG Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	Support	PG0	SDC1_CLK	-	-	UART3_TX	PG_EINT0
Support	Support	PG1	SDC1_CMD	-	-	UART3_RX	PG_EINT1
Support	Support	PG2	SDC1_D0	-	-	UART3_CTS	PG_EINT2
Support	Support	PG3	SDC1_D1	-	-	UART3_RTS	PG_EINT3
Support	Support	PG4	SDC1_D2	-	-	UART1_RTS	PG_EINT4
Support	Support	PG5	SDC1_D3	-	-	UART1_CTS	PG_EINT5
Support	Support	PG6	-	-	-	UART1_TX	PG_EINT6
Support	Support	PG7	-	-	-	UART1_RX	PG_EINT7

Table 11- 27. PH Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	Support	PH0	PWM_0	I2S0_MCLK	SPI1_CLK	UART3_TX	PH_EINT0
Support	Support	PH1	PWM_1	I2S0_BCLK	SPI1_MOSI	UART3_RX	PH_EINT1
Support	Support	PH2	PWM_2	I2S0_LRCK	SPI1_MISO	UART3_CTS	PH_EINT2
Support	Support	PH3	PWM_3	I2S0_DOUT	SPI1_CS0	UART3_RTS	PH_EINT3
Support	Support	PH4	PWM_4	I2S0_DIN	SPI1_CS1	ONEWIRE	PH_EINT4
Support	Support	PH5	PWM_5	RMII_RXD1	TWI2_SCK	UART2_TX	PH_EINT5
Support	Support	PH6	PWM_6	RMII_RXD0	TWI2_SDA	UART2_RX	PH_EINT6
Support	Support	PH7	PWM_7	RMII_CRS_DV	UART0_TX	UART2_RTS	PH_EINT7
Support	Support	PH8	PWM_8	RMII_RXER	UART0_RX	UART2_CTS	PH_EINT8
Support	Support	PH9	PWM_9	RMII_TXD1	TWI3_SCK	UART0_TX	PH_EINT9
Support	Support	PH10	-	RMII_TXD0	TWI3_SDA	UART0_RX	PH_EINT10
Support	Support	PH11	JTAG_MS	RMII_TXCK	SPI1_CLK	TWI2_SCK	PH_EINT11
Support	Support	PH12	JTAG_CK	RMII_TXEN	SPI1_MOSI	TWI2_SDA	PH_EINT12
Support	Support	PH13	JTAG_DO	MDC	SPI1_MISO	TWI3_SCK	PH_EINT13
Support	Support	PH14	JTAG_DI	MDIO	SPI1_CS0	TWI3_SDA	PH_EINT14
Support	No Support	PH15	-	EPHY_25M	SPI1_CS1	-	PH_EINT15

Table 11- 28. PI Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	Support	PI0	CSI_MASTERCLK0	-	-	-	PI_EINT0
Support	Support	PI1	CSI_SM_HS	-	SPI2_CLK	TWI1_SCK	PI_EINT1
Support	Support	PI2	CSI_SM_VS	TCON_TRIG	SPI2_MOSI	TWI1_SDA	PI_EINT2
Support	No Support	PI3	-	-	SPI2_MISO	TWI0_SCK	PI_EINT3
Support	No Support	PI4	-	-	SPI2_CS0	TWI0_SDA	PI_EINT4

Table 11- 29. PL Multiplex Function Select

V833	V831	GPIO Port	Function2	Function3	Function4	Function5	Function6
Support	No Support	PL0	S_RSB_SCK	S_TWI0_SCK	-	-	S_PL_EINT0
Support	No Support	PL1	S_RSB_SCK	S_TWI0_SDA	-	-	S_PL_EINT1
Support	No Support	PL2	-	-	-	-	S_PL_EINT2
Support	No Support	PL3	-	-	-	-	S_PL_EINT3
Support	No Support	PL4	-	-	-	-	S_PL_EINT4
Support	No Support	PL5	-	-	-	-	S_PL_EINT5

11.6.3.2. Port Function

Port Controller supports 8 GPIOs, every GPIO can configure as Input, Output, Functional Peripheral, IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 11- 30. Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/: non-configure, configuration is invalid

Y: configure

X: Select configuration according to actual situation

N: Forbid to configure

11.6.3.3. Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

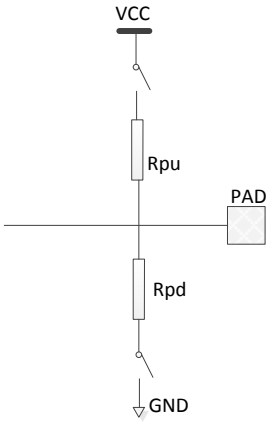

Figure 11- 46. Pull up/down Logic

High-impedance, the output is float state, all buffers are off, the level is decided by external high/low level. When

high-impedance, software configures the switch on Rpu and Rpd as off, and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by a resistance, the resistance has current-limiting function. When pulling up, the switch on Rpu is breakover by software configuration, IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is breakover by software configuration, IO is pulled down to GND by Rpd.

The pull-up/down of each IO is weak pull-up/down, the pull-up/down resistance contains three kinds of resistance values : 4.7 kΩ, 15 kΩ and 100 kΩ.

The setting of pull-down, pull-up, high-impledance is decided by external circuit.

11.6.3.4. Buffer Strength

Each IO can be set as different buffer strength. The IO buffer diagram is as follows.

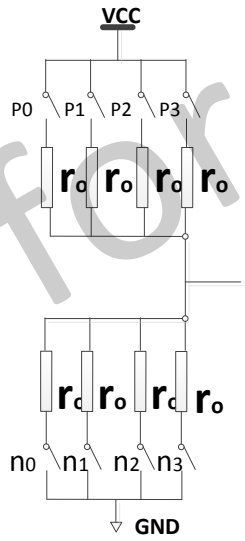

Figure 11- 47. IO Buffer Strength Diagram

When output high level, the n0,n1,n2,n3 of NMOS are off, the p0,p1,p2,p3 of PMOS are on. When buffer strength is set to 0(buffer strength is weakest), only p0 is on, the output impedance is maximum, the impedance value is r0 (on-resistance). When buffer strength is set to 1, only p0 and p1 are on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only p0,p1 and p2 are on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, p0,p1,p2 and p3 are on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0,p1,p2,p3 of PMOS is off, the n0,n1,n2,n3 of NMOS is on. When buffer strength is set to 0(buffer strength is weakest), only n0 is on, the output impedance is maximum, the impedance value is r0. When buffer strength is set to 1, only n0 and n1 are on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only n0,n1 and n2 are on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, n0,n1,n2 and n3 are on, the output

impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between output driver circuit and port is unconnected, driver configuration is invalid.

NOTE

The typical value of r0 is 200Ω.

11.6.3.5. Interrupt

Each group IO has independent interrupt number. IO within group uses one interrupt number, when one IO generates interrupt, Port Controller sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

Interrupt trigger of GPIO supports the following trigger types.

- Positive Edge : When low level changes to high level, the interrupt will generate. No matter how long high level keeps, the interrupt generates only once.
- Negative Edge: When high level changes to low level, the interrupt will generate. No matter how long low level keeps, the interrupt generates only once.
- High Level : Just keep high level and the interrupt will always generate.
- Low Level : Just keep low level and the interrupt will always generate.
- Double Edge : Positive and negative edge.

External Interrupt Configure Register is used to configure trigger type.

GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using lower sample clock, to reach the debounce effect because of the dither frequency of signal is higher than sample frequency.

Set sample clock source by PIO_INT_CLK_SELECT and prescale factor by DEB_CLK_PRE_SCALE.

11.6.4. Register List

Module Name	Base Address
GPIO(PC,PD,PE,PF,PG,PH,PI)	0x0300B000

Register Name	Offset	Description
Pn_CFG0	n*0x0024+0x00	Port n Configure Register 0 (n =2,3,4,5,6,7,8)
Pn_CFG1	n*0x0024+0x04	Port n Configure Register 1 (n =2,3,4,5,6,7,8)
Pn_CFG2	n*0x0024+0x08	Port n Configure Register 2 (n =2,3,4,5,6,7,8)
Pn_CFG3	n*0x0024+0x0C	Port n Configure Register 3 (n =2,3,4,5,6,7,8)

Pn_DAT	n*0x0024+0x10	Port n Data Register (n =2,3,4,5,6,7,8)
Pn_DRV0	n*0x0024+0x14	Port n Multi-Driving Register 0 (n =2,3,4,5,6,7,8)
Pn_DRV1	n*0x0024+0x18	Port n Multi-Driving Register 1 (n =2,3,4,5,6,7,8)
Pn_PUL0	n*0x0024+0x1C	Port n Pull Register 0 (n =2,3,4,5,6,7,8)
Pn_PUL1	n*0x0024+0x20	Port n Pull Register 1 (n =2,3,4,5,6,7,8)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0 (n =2,3,4,5,6,7,8)
Pn_INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1 (n =2,3,4,5,6,7,8)
Pn_INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2 (n =2,3,4,5,6,7,8)
Pn_INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3 (n =2,3,4,5,6,7,8)
Pn_INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register (n =2,3,4,5,6,7,8)
Pn_INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register (n =2,3,4,5,6,7,8)
Pn_INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register (n =2,3,4,5,6,7,8)
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_MS_CTL	0x0344	PIO Group Withstand Voltage Mode Select Control Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register

Module Name	**Base Address**
GPIO(PL)	0x07022000

Register Name	**Offset**	**Description**
PL_CFG0	0x0000	Port L Configure Register 0
PL_DAT	0x0010	Port L Data Register
PL_DRV0	0x0014	Port L Multi-Driving Register 0
PL_PUL0	0x001C	Port L Pull Register 0
PL_INT_CFG0	0x0200	PIO Interrupt Configure Register 0
PL_INT_CTL	0x0210	PIO Interrupt Control Register
PL_INT_STA	0x0214	PIO Interrupt Status Register
PL_INT_DEB	0x0218	PIO Interrupt Debounce Register
PIO_POW_MOD_SEL	0x0340	PIO Group Withstand Voltage Mode Select Register
PIO_POW_MS_CTL	0x0344	PIO Group Withstand Voltage Mode Select Control Register
PIO_POW_VAL	0x0348	PIO Group Power Value Register

11.6.5. V833 GPIO(PC,PD,PE,PF,PG,PH,PI) Register Description

11.6.5.1. 0x0048 PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			**Register Name: PC_CFG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

30:28	R/W	0x7	PC7_SELECT 000:Input 010:Reserved 100:Reserved 110:PC_EINT7	 001:Output 011:SDC2_D5 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PC6_SELECT 000:Input 010:Reserved 100:SPI0_CS1 110:PC_EINT6	 001:Output 011:SDC2_D0 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PC5_SELECT 000:Input 010:Reserved 100:SPI0_HOLD 110:PC_EINT5	 001:Output 011:SDC2_D4 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000:Input 010:Reserved 100:SPI0_WP 110:PC_EINT4	 001:Output 011:SDC2_D3 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000:Input 010:Reserved 100:SPI0_MISO 110:PC_EINT3	 001:Output 011:SDC2_CMD 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000:Input 010:Reserved 100:SPI0_MOSI 110:PC_EINT2	 001:Output 011:SDC2_CLK 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000:Input 010:Reserved 100:SPI0_CS0 110:PC_EINT1	 001:Output 011:SDC2_RST 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000:Input	 001:Output

			010:Reserved	011:SDC2_DS
			100:SPI0_CLK	101:Reserved
			110:PC_EINT0	111:IO Disable

11.6.5.2. 0x004C PC Configure Register 1 (Default Value: 0x0000_7777)

Offset: 0x004C			Register Name: PC_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:15	/	/	/	
14:12	R/W	0x7	PC11_SELECT 000:Input 010:Reserved 100:Reserved 110:PC_EINT11	 001:Output 011:SDC2_D7 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC10_SELECT 000:Input 010:Reserved 100:Reserved 110:PC_EINT10	 001:Output 011:SDC2_D2 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC9_SELECT 000:Input 010:Reserved 100:Reserved 110:PC_EINT9	 001:Output 011:SDC2_D6 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC8_SELECT 000:Input 010:Reserved 100:Reserved 110:PC_EINT8	 001:Output 011:SDC2_D1 101:Reserved 111:IO Disable

11.6.5.3. 0x0058 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is

			configured as functional pin, the undefined value will be read.

11.6.5.4. 0x005C PC Multi-Driving Register 0 (Default Value: 0x0055_5555)

Offset: 0x005C			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x1	PC11_DRV PC11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PC10_DRV PC10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PC9_DRV PC9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PC8_DRV PC8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PC7_DRV PC7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PC6_DRV PC6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PC5_DRV PC5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PC4_DRV PC4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PC3_DRV PC3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PC2_DRV

			PC2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PC1_DRV PC1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PC0_DRV PC0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.5. 0x0064 PC Pull Register 0 (Default Value: 0x0000_1054)

Offset: 0x0064			Register Name: PC_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x0	PC11_PULL PC11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PC10_PULL PC10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PC9_PULL PC9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PC8_PULL PC8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PC7_PULL PC7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x1	PC6_PULL PC6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PC5_PULL PC5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

			10: Pull-down	11: Reserved
9:8	R/W	0x0	PC4_PULL PC4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x1	PC2_PULL PC2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x1	PC1_PULL PC Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.5.6. 0x006C PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD7_SELECT 000:Input 010:LCD_D11 100:VO_D6 110:PD_EINT7	 001:Output 011:PWM_6 101:RMII_TXCK 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PD6_SELECT 000:Input 010:LCD_D10 100:VO_D5 110:PD_EINT6	 001:Output 011:PWM_5 101:RMII_TXD0 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD5_SELECT 000:Input 010:LCD_D7 100:VO_D4	 001:Output 011:PWM_4 101:RMII_TXD1

			110:PD_EINT5	111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD4_SELECT 000:Input 010:LCD_D6 100:VO_D3 110:PD_EINT4	 001:Output 011:PWM_3 101:RMII_RXER 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD3_SELECT 000:Input 010:LCD_D5 100:VO_D2 110:PD_EINT3	 001:Output 011:PWM_2 101:RMII_CRS_DV 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000:Input 010:LCD_D4 100:VO_D1 110:PD_EINT2	 001:Output 011:PWM_1 101:RMII_RXD0 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000:Input 010:LCD_D3 100:VO_D0 110:PD_EINT1	 001:Output 011:PWM_0 101:RMII_RXD1 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD0_SELECT 000:Input 010:LCD_D2 100:Reserved 110:PD_EINT0	 001:Output 011:Reserved 101:Reserved 111:IO Disable

11.6.5.7. 0x0070 PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD15_SELECT 000:Input 010:LCD_D21 100:VO_D13 110:PD_EINT15	 001:Output 011:I2S1_DOUT2 101:I2S1_DIN2 111:IO Disable
27	/	/	/	

26:24	R/W	0x7	PD14_SELECT 000:Input 010:LCD_D20 100:VO_D12 110:PD_EINT14	001:Output 011:I2S1_DOUT1 101:I2S1_DIN1 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD13_SELECT 000:Input 010:LCD_D19 100:VO_D11 110:PD_EINT13	001:Output 011:I2S1_DOUT0 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD12_SELECT 000:Input 010:LCD_D18 100:VO_D10 110:PD_EINT12	001:Output 011:I2S1_LRCK 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD11_SELECT 000:Input 010:LCD_D15 100:VO_D9 110:PD_EINT11	001:Output 011:I2S1_BCLK 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD10_SELECT 000:Input 010:LCD_D14 100:VO_D8 110:PD_EINT10	001:Output 011:I2S1_MCLK 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD9_SELECT 000:Input 010:LCD_D13 100:Reserved 110:PD_EINT9	001:Output 011:PWM_8 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD8_SELECT 000:Input 010:LCD_D12 100:VO_D7 110:PD_EINT8	001:Output 011:PWM_7 101:RMII_TXEN 111:IO Disable

11.6.5.8. 0x0074 PD Configure Register 2 (Default Value: 0x0777_7777)

Offset: 0x0074			Register Name: PD_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PD22_SELECT 000:Input 010:PWM_9 100:Reserved 110:PD_EINT22	 001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT 000:Input 010:LCD_VSYNC 100:VO_VSYNC 110:PD_EINT21	 001:Output 011:Reserved 101:MDIO 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000:Input 010:LCD_HSYNC 100:VO_HSYNC 110:PD_EINT20	 001:Output 011:Reserved 101:MDC 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000:Input 010:LCD_DE 100:VO_FIELD 110:PD_EINT19	 001:Output 011:PWM_9 101: TCON_TRIG 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000:Input 010:LCD_CLK 100:VO_CLK 110:PD_EINT18	 001:Output 011:Reserved 101:EPHY_25M 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD17_SELECT 000:Input 010:LCD_D23 100:VO_D15 110:PD_EINT17	 001:Output 011:I2S1_DIN0 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PD16_SELECT 000:Input 010:LCD_D22	 001:Output 011:I2S1_DOUT3

			100:VO_D14	101:I2S1_DIN3
			110:PD_EINT16	111:IO Disable

11.6.5.9. 0x007C PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:0	R/W	0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.5.10. 0x0080 PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PD15_DRV PD15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PD14_DRV PD14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PD13_DRV PD13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PD12_DRV PD12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PD11_DRV PD11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PD10_DRV PD10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

19:18	R/W	0x1	PD9_DRV PD9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PD8_DRV PD8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PD7_DRV PD7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PD6_DRV PD6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD5_DRV PD5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD4_DRV PD4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD3_DRV PD3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD2_DRV PD2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD1_DRV PD1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD0_DRV PD0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.11. 0x0084 PD Multi-Driving Register 1 (Default Value: 0x0000_1555)

Offset: 0x0084	Register Name: PD_DRV1

Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x1	PD22_DRV PD22 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD21_DRV PD21 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD20_DRV PD20 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD19_DRV PD19 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD18_DRV PD18 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD17_DRV PD17 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PD16_DRV PD16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.12. 0x0088 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PD15_PULL PD15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PD14_PULL PD14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PD13_PULL

			PD13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PD12_PULL PD12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PD11_PULL PD11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PD10_PULL PD10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PD9_PULL PD9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PD8_PULL PD8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull-up/down Select

			00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD0_PULL PD0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

11.6.5.13. 0x008C PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PD22_PULL PD22 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD21_PULL PD21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD20_PULL PD20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD17_PULL PD17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PD16_PULL PD16 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

11.6.5.14. 0x090 PE Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: PE_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE7_SELECT 000:Input 010:NCSI1_D3 100:Reserved 110:PE_EINT7	 001:Output 011:RGMII_TXD3 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PE6_SELECT 000:Input 010:NCSI1_D2 100:Reserved 110:PE_EINT6	 001:Output 011:RGMII_CLKIN/RMII_RXER 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PE5_SELECT 000:Input 010:NCSI1_D1 100:Reserved 110:PE_EINT5	 001:Output 011:RGMII_RXCTL/RMII_CRS_DV 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PE4_SELECT 000:Input 010:NCSI1_D0 100:Reserved 110:PE_EINT4	 001:Output 011:RGMII_RXCK 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PE3_SELECT 000:Input 010:NCSI1_VSYNC 100:Reserved 110:PE_EINT3	 001:Output 011:RGMII_RXD0/RMII_RXD0 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PE2_SELECT 000:Input 010:NCSI1_HSYNC 100:Reserved 110:PE_EINT2	 001:Output 011:RGMII_RXD1/RMII_RXD1 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PE1_SELECT	

			000:Input 010:CSI_MASTERCLK1 100:Reserved 110:PE_EINT1	001:Output 011:RGMII_RXD2 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PE0_SELECT 000:Input 010:NCSI1_PCLK 100:Reserved 110:PE_EINT0	 001:Output 011:RGMII_RXD3 101:Reserved 111:IO Disable

11.6.5.15. 0x0094 PE Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0094			Register Name: PE_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PE15_SELECT 000:Input 010:NCSI1_D11 100:Reserved 110:PE_EINT15	 001:Output 011:EPHY_25M 101:NCSIC1_FIELD 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PE14_SELECT 000:Input 010:NCSI1_D10 100:Reserved 110:PE_EINT14	 001:Output 011:MDIO 101:TWI1_SDA 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PE13_SELECT 000:Input 010:NCSI1_D9 100:Reserved 110:PE_EINT13	 001:Output 011:MDC 101:TWI1_SCK 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PE12_SELECT 000:Input 010:NCSI1_D8 100:Reserved 110:PE_EINT12	 001:Output 011:RGMII_TXCTL/RMII_TXEN 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PE11_SELECT 000:Input 010:NCSI1_D7	 001:Output 011:RGMII_TXCK/RMII_TXCK

			100:Reserved	101:Reserved
			110:PE_EINT11	111:IO Disable
11	/	/	/	
			PE10_SELECT	
			000:Input	001:Output
			010:NCSI1_D6	011:RGMII_TXD0/RMII_TXD0
			100:Reserved	101:Reserved
10:8	R/W	0x7	110:PE_EINT10	111:IO Disable
7	/	/	/	
			PE9_SELECT	
			000:Input	001:Output
			010:NCSI1_D5	011:RGMII_TXD1/RMII_TXD1
			100:Reserved	101:Reserved
6:4	R/W	0x7	110:PE_EINT9	111:IO Disable
3	/	/	/	
			PE8_SELECT	
			000:Input	001:Output
			010:NCSI1_D4	011:RGMII_TXD2
			100:Reserved	101:Reserved
2:0	R/W	0x7	110:PE_EINT8	111:IO Disable

11.6.5.16. 0x0098 PE Configure Register 2 (Default Value: 0x0077_7777)

Offset: 0x0098			Register Name: PE_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:23	/	/	/	
			PE21_SELECT	
			000:Input	001:Output
22:20	R/W	0x7	010:NSCI1_D15	011:LCD_D17
			100:SPI2_CS0	101:UART2_CTS
			110:PE_EINT21	111:IO Disable
19	/	/	/	
			PE20_SELECT	
			000:Input	001:Output
18:16	R/W	0x7	010:NSCI1_D14	011:LCD_D16
			100:SPI2_MISO	101:UART2_RTS
			110:PE_EINT20	111:IO Disable
15	/	/	/	
			PE19_SELECT	
			000:Input	001:Output
14:12	R/W	0x7	010:NSCI1_D13	011:LCD_D9
			100:SPI2_MOSI	101:UART2_RX
			110:PE_EINT19	111:IO Disable

11	/	/	/
10:8	R/W	0x7	PE18_SELECT 000:Input 001:Output 010:NSCI0_D12 011:LCD_D8 100:SPI2_CLK 101:UART2_TX 110:PE_EINT18 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PE17_SELECT 000:Input 001:Output 010:Reserved 011:LCD_D1 100:Reserved 101:TWI0_SDA 110:PE_EINT17 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE16_SELECT 000:Input 001:Output 010:Reserved 011:LCD_D0 100:Reserved 101:TWI0_SCK 110:PE_EINT16 111:IO Disable

11.6.5.17. 0x00A0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PE_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.5.18. 0x00A4 PE Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x00A4			Register Name: PE_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PE15_DRV PE15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PE14_DRV PE14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

27:26	R/W	0x1	PE13_DRV PE13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PE12_DRV PE12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PE11_DRV PE11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PE10_DRV PE10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PE9_DRV PE9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PE8_DRV PE8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PE7_DRV PE7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PE6_DRV PE6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PE5_DRV PE5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PE4_DRV PE4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PE3_DRV PE3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PE2_DRV

			PE2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PE1_DRV PE1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PE0_DRV PE0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.19. 0x00A8 PE Multi-Driving Register 1 (Default Value: 0x0000_0555)

Offset: 0x00A8			Register Name: PE_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x1	PE21_DRV PE21 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PE20_DRV PE20 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PE19_DRV PE19 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PE18_DRV PE18 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PE17_DRV PE17 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PE16_DRV PE16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.20. 0x00AC PE Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: PE_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	PE15_PULL PE15 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
29:28	R/W	0x0	PE14_PULL PE14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PE13_PULL PE13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PE12_PULL PE12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PE11_PULL PE11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PE10_PULL PE10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PE9_PULL PE9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PE8_PULL PE8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PE7_PULL PE7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PE6_PULL PE6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PE5_PULL

			PE5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PE4_PULL PE4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PE3_PULL PE3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE2_PULL PE2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PE1_PULL PE1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE0_PULL PE0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

11.6.5.21. 0x00B0 PE Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PE_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PE21_PULL PE21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PE20_PULL PE20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PE19_PULL PE19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PE18_PULL PE18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

			10: Pull-down	11: Reserved
3:2	R/W	0x0	PE17_PULL PE17 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PE16_PULL PE16 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.5.22. 0x00B4 PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PF6_SELECT 000:Input 010:Reserved 100:Reserved 110:PF_EINT6	 001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PF5_SELECT 000:Input 010:SDC0_D2 100:Reserved 110:PF_EINT5	 001:Output 011:JTAG_CK 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PF4_SELECT 000:Input 010:SDC0_D3 100:Reserved 110:PF_EINT4	 001:Output 011:UART0_RX 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PF3_SELECT 000:Input 010:SDC0_CMD 100:Reserved 110:PF_EINT3	 001:Output 011:JTAG_DO 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PF2_SELECT 000:Input 010:SDC0_CLK 100:Reserved	 001:Output 011:UART0_TX 101:Reserved

			110:PF_EINT2	111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PF1_SELECT 000:Input 010:SDC0_D0 100:Reserved 110:PF_EINT1	 001:Output 011:JTAG_DI 101:CPU_BIST1 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PF0_SELECT 000:Input 010:SDC0_D1 100:Reserved 110:PF_EINT0	 001:Output 011:JTAG_MS 101:CPU_BIST0 111:IO Disable

11.6.5.23. 0x00C4 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.5.24. 0x00C8 PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:14	/	/	/	
13:12	R/W	0x1	PF6_DRV PF6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PF5_DRV PF5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PF4_DRV PF4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

7:6	R/W	0x1	PF3_DRV PF3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PF2_DRV PF2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PF1_DRV PF1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PF0_DRV PF0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.25. 0x00D0 PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	PF6_PULL PF6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull-up/down Select

			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.5.26. 0x00D8 PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PG7_SELECT 000:Input 010:Reserved 100:Reserved 110:PG_EINT7	 001:Output 011:Reserved 101:UART1_RX 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PG6_SELECT 000:Input 010:Reserved 100:Reserved 110:PG_EINT6	 001:Output 011:Reserved 101:UART1_TX 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PG5_SELECT 000:Input 010:SDC1_D3 100:Reserved 110:PG_EINT5	 001:Output 011:Reserved 101:UART1_CTS 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PG4_SELECT 000:Input 010:SDC1_D2 100:Reserved 110:PG_EINT4	 001:Output 011:Reserved 101: UART1_RTS 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PG3_SELECT 000:Input 010:SDC1_D1 100:Reserved 110:PG_EINT3	 001:Output 011:Reserved 101: UART3_RTS 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PG2_SELECT	

			000:Input 010:SDC1_D0 100:Reserved 110:PG_EINT2	001:Output 011:Reserved 101:UART3_CTS 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PG1_SELECT 000:Input 010:SDC1_CMD 100:Reserved 110:PG_EINT1	 001:Output 011:Reserved 101:UART3_RX 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000:Input 010:SDC1_CLK 100:Reserved 110:PG_EINT0	 001:Output 011:Reserved 101:UART3_TX 111:IO Disable

11.6.5.27. 0x00E8 PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.5.28. 0x00EC PG Multi-Driving Register 0 (Default Value: 0x0000_5555)

Offset: 0x00EC			Register Name: PG_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0x1	PG7_DRV PG7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PG6_DRV PG6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PG5_DRV

			PG5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PG4_DRV PG4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PG3_DRV PG3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PG2_DRV PG2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PG1_DRV PG1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PG0_DRV PG0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.29. 0x00F4 PG Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0x0	PG7_PULL PG7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PG5_PULL PG5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PG4_PULL PG4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

			10: Pull-down	11: Reserved
7:6	R/W	0x0	PG3_PULL PG3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PG2_PULL PG2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PG1_PULL PG1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.5.30. 0x00FC PH Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00FC			Register Name: PH_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH7_SELECT 000:Input 010:PWM_7 100:UART0_TX 110:PH_EINT7	 001:Output 011:RMII_CRS_DV 101:UART2_RTS 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH6_SELECT 000:Input 010:PWM_6 100:TWI2_SDA 110:PH_EINT6	 001:Output 011:RMII_RXD0 101:UART2_RX 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH5_SELECT 000:Input 010:PWM_5 100:TWI2_SCK 110:PH_EINT5	 001:Output 011:RMII_RXD1 101:UART2_TX 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH4_SELECT 000:Input	 001:Output

			010:PWM_4 100:SPI1_CS1 110:PH_EINT4	011:I2S0_DIN 101:ONEWIRE 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH3_SELECT 000:Input 010:PWM_3 100:SPI1_CS0 110:PH_EINT3	 001:Output 011:I2S0_DOUT 101:UART3_RTS 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH2_SELECT 000:Input 010: PWM_2 100:SPI1_MISO 110:PH_EINT2	 001:Output 011:I2S0_LRCK 101:UART3_CTS 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH1_SELECT 000:Input 010:PWM_1 100:SPI1_MOSI 110:PH_EINT1	 001:Output 011:I2S0_BCLK 101:UART3_RX 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000:Input 010:PWM_0 100:SPI1_CLK 110:PH_EINT0	 001:Output 011:I2S0_MCLK 101:UART3_TX 111:IO Disable

11.6.5.31. 0x0100 PH Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0100			Register Name: PH_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH15_SELECT 000:Input 010:Reserved 100:SPI1_CS1 110:PH_EINT15	 001:Output 011:EPHY_25M 101:Reserved 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH14_SELECT 000:Input 010:JTAG_DI 100:SPI1_CS0	 001:Output 011:MDIO 101:TWI3_SDA

			110:PH_EINT14	111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH13_SELECT 000:Input 010:JTAG_DO 100:SPI1_MISO 110:PH_EINT13	 001:Output 011:MDC 101:TWI3_SCK 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH12_SELECT 000:Input 010:JTAG_CK 100:SPI1_MOSI 110:PH_EINT12	 001:Output 011:RMII_TXEN 101:TWI2_SDA 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH11_SELECT 000:Input 010:JTAG_MS 100:SPI1_CLK 110:PH_EINT11	 001:Output 011:RMII_TXCK 101:TWI2_SCK 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH10_SELECT 000:Input 010:Reserved 100:TWI3_SDA 110:PH_EINT10	 001:Output 011:RMII_TXD0 101:UART0_RX 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000:Input 010:PWM_9 100:TWI3_SCK 110:PH_EINT9	 001:Output 011:RMII_TXD1 101:UART0_TX 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000:Input 010:PWM_8 100:UART0_RX 110:PH_EINT8	 001:Output 011:RMII_RXER 101:UART2_CTS 111:IO Disable

11.6.5.32. 0x010C PH Data Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

15:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.5.33. 0x0110 PH Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0110			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	PH15_DRV PH15 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
29:28	R/W	0x1	PH14_DRV PH14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PH13_DRV PH13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PH12_DRV PH12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PH11_DRV PH11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PH10_DRV PH10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PH9_DRV PH9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PH8_DRV PH8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PH7_DRV PH7 Multi-Driving Select

			00: Level 0 10: Level 2	01: Level 1 11: Level 3
13:12	R/W	0x1	PH6_DRV PH6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PH5_DRV PH5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PH4_DRV PH4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PH3_DRV PH3 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
5:4	R/W	0x1	PH2_DRV PH2 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
3:2	R/W	0x1	PH1_DRV PH1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PH0_DRV PH0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

11.6.5.34. 0x0118 PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PH_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:30	R/W	0x0	PH15_PULL PH15 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
27:26	R/W	0x0	PH13_PULL	

			PH13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull-up/down Select

			00: Pull-up/down disable 10: Pull-down	01: Pull-up 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.5.35. 0x0120 PI Configure Register 0 (Default Value: 0x0007_7777)

Offset: 0x0120			Register Name: PI_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:19	/	/	/	
18:16	R/W	0x7	PI4_SELECT 000:Input 010:Reserved 100:SPI2_CS0 110:PI_EINT4	 001:Output 011:Reserved 101:TWI0_SDA 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PI3_SELECT 000:Input 010:Reserved 100:SPI2_MISO 110:PI_EINT3	 001:Output 011:Reserved 101:TWI0_SCK 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PI2_SELECT 000:Input 010:CSI_SM_VS 100:SPI2_MOSI 110:PI_EINT2	 001:Output 011:TCON_TRIG 101:TWI1_SDA 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PI1_SELECT 000:Input 010:CSI_SM_HS 100:SPI2_CLK 110:PI_EINT1	 001:Output 011:Reserved 101:TWI1_SCK 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PI0_SELECT 000:Input	 001:Output

			010:CSI_MASTERCLK0	011:Reserved
			100:Reserved	101:Reserved
			110:PI_EINT0	111:IO Disable

11.6.5.36. 0x0130 PI Data Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PI_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0x0	PI_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.5.37. 0x0134 PI Multi-Driving Register 0 (Default Value: 0x0000_0155)

Offset: 0x0134			Register Name: PI_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x1	PI4_DRV PI4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PI3_DRV PI3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PI2_DRV PI2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PI1_DRV PI1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PI0_DRV PI0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.5.38. 0x013C PI Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PI_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	PI4_PULL PI4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PI3_PULL PI3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PI2_PULL PI2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PI1_PULL PI1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PI0_PULL PI0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

11.6.5.39. 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

			0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.40. 0x0244 PC External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0244			Register Name: PC_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.41. 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable

1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.5.42. 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.43. 0x0258 PC External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.44. 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: PD_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative)

			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

11.6.5.45. 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0264			**Register Name: PD_EINT_CFG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

			0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

11.6.5.46. 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: PD_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT22_CFG External INT22 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG

			External INT18 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

11.6.5.47. 0x0270 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	EINT22_CTL External INT22 Enable 0: Disable 1: Enable
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable

			1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable

7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.5.48. 0x0274 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: PD_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W1C	0x0	EINT22_STATUS External INT22 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
21	R/W1C	0x0	EINT21_STATUS

			External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
20	R/W1C	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
19	R/W1C	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
12	R/W1C	0x0	EINT12_STATUS

			External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS

			External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.49. 0x0278 PD External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: PD_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.50. 0x0280 PE External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PE_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge

			0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG

			External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.51. 0x0284 PE External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PE_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.52. 0x0288 PE External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0288	Register Name: PE_EINT_CFG2

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG External INT19 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.53. 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL

			External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable

			0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.5.54. 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21	R/W1C	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W1C	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W1C	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.55. 0x0298 PE External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE

			Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.56. 0x02A0 PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative)

			Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

11.6.5.57. 0x0280 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			**Register Name: PF_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL

			External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.5.58. 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			**Register Name: PF_EINT_STATUS**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.59. 0x02B8 PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02B8			Register Name: PF_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.60. 0x02C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.61. 0x02D0 PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable

			0: Disable 1: Enable

11.6.5.62. 0x02D4 PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS

			External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.63. 0x02D8 PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PG_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.64. 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name:PH_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.65. 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT15_CFG External INT15 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative)

			Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.66. 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			**Register Name: PH_EINT_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	EINT15_CTL External INT15 Enable 0: Disable 1: Enable
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL

			External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable

			0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.5.67. 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W1C	0x0	EINT15_STATUS External INT15 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit

			0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.68. 0x02F8 PH External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.69. 0x0300 PI External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: PI_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.5.70. 0x0310 PI External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: PI_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL

			External INT0 Enable 0: Disable 1: Enable

11.6.5.71. 0x0314 PI External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: PI_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.5.72. 0x0318 PI External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: PI_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n

			The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.5.73. 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC-IO&PH_Port POWER MODE Select 0: 3.3V 1: 1.8V
11:9	/	/	/
8	R/W	0x0	PI_POWER MODE Select 0: 3.3V 1: 1.8V
7	/	/	/
6	R/W	0x0	PG_POWER MODE Select 0: 3.3V 1: 1.8V
5	R/W	0x0	PF_POWER MODE Select 0: 3.3V 1: 1.8V
4	R/W	0x0	PE_POWER MODE Select 0: 3.3V 1: 1.8V
3	R/W	0x0	PD_POWER MODE Select 0: 3.3V 1: 1.8V
2	R/W	0x0	PC_POWER MODE Select 0: 3.3V 1: 1.8V
1:0	/	/	/

NOTE

When the power domain of GPIO is larger than 1.8V, the withstand voltage is set to 3.3V mode, the corresponding value in 0x0340 register is set to 0.

When the power domain of GPIO is 1.8V, the withstand voltage is set to 1.8V mode, the corresponding value in 0x0340 register is set to 1.

11.6.5.74. 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC-IO&PH_Port Withstand Voltage Mode Select Control 0: Enable 1: Disable
11:9	/	/	/
8	R/W	0x0	VCC-PI Withstand Voltage Mode Select Control 0: Enable 1: Disable
7	/	/	/
6	R/W	0x0	VCC-PG Withstand Voltage Mode Select Control 0: Enable 1: Disable
5	R/W	0x0	VCC-PF Withstand Voltage Mode Select Control 0: Enable 1: Disable
4	R/W	0x0	VCC-PE Withstand Voltage Mode Select Control 0: Enable 1: Disable
3	R/W	0x0	VCC-PD Withstand Voltage Mode Select Control 0: Enable 1: Disable
2	R/W	0x0	VCC-PC Withstand Voltage Mode Select Control 0: Enable 1: Disable
1	/	/	/

NOTE

For 1.8V and 3.3V power, the withstand function is enabled by default, the corresponding bit in 0x0344 register is set to 0.

For 2.5V power, the withstand function is disabled, the corresponding bit in 0x0344 register is set to 1, and the withstand mode in 0x0340 register needs be set to 3.3V.

11.6.5.75. 0x0348 PIO Group Power Value Register

Offset: 0x0348		Register Name: PIO_POW_Val
Bit	**Read/Write**	**Description**
31:17	/	/
16	R	VCC-IO&PH_Port Power Value

15:9	/	/
8	R	PI_Port Power Value
7	/	/
6	R	PG_Port Power Value
5	R	PF_Port Power Value
4	R	PE_Port Power Value
3	R	PD_Port Power Value
2	R	PC_Port Power Value
1:0	/	/

NOTE

When the reading value of the 0x0348 register is 0, it indicates that IO power voltage is greater than 2.5V.
When the reading value of the 0x0348 register is 1, it indicates that IO power voltage is less than 2.0V.

11.6.5.76. 0x0350 PIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: PIO_PV_SEL_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	VCC-PF Power Voltage Select Control 0: 1.8V 1: 3.3V

11.6.6. V831 GPIO(PC,PD,PE,PF,PG,PH,PI) Register Description

11.6.6.1. 0x0048 PC Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	Reserved
27	/	/	/
26:24	R/W	0x7	Reserved
23	/	/	/
22:20	R/W	0x7	PC5_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:SPI0_HOLD 101:Reserved 110:PC_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PC4_SELECT

			000:Input 010:Reserved 100:SPI0_WP 110:PC_EINT4	001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000:Input 010:Reserved 100:SPI0_MISO 110:PC_EINT3	 001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000:Input 010:Reserved 100:SPI0_MOSI 110:PC_EINT2	 001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000:Input 010:Reserved 100:SPI0_CS0 110:PC_EINT1	 001:Output 011:Reserved 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000:Input 010:Reserved 100:SPI0_CLK 110:PC_EINT0	 001:Output 011:Reserved 101:Reserved 111:IO Disable

11.6.6.2. 0x0058 PC Data Register (Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
4:0	R/W	0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.6.3. 0x005C PC Multi-Driving Register 0 (Default Value: 0x0055_5555)

Offset: 0x005C			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:22	R/W	0x1	Reserved
21:20	R/W	0x1	Reserved
19:18	R/W	0x1	Reserved
17:16	R/W	0x1	Reserved
15:14	R/W	0x1	Reserved
13:12	R/W	0x1	Reserved
11:10	R/W	0x1	Reserved
9:8	R/W	0x1	PC4_DRV PC4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PC3_DRV PC3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PC2_DRV PC2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PC1_DRV PC1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PC0_DRV PC0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.6.4. 0x0064 PC Pull Register 0 (Default Value: 0x0000_1054)

Offset: 0x0064			Register Name: PC_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	Reserved
11:10	R/W	0x0	Reserved
9:8	R/W	0x0	PC4_PULL PC4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

			10: Pull-down	11: Reserved
7:6	R/W	0x1	PC3_PULL PC3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x1	PC2_PULL PC2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x1	PC1_PULL PC Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PC0_PULL PC0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.6.5. 0x006C PD Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD7_SELECT 000:Input 010:LCD_D11 100:VO_D6 110:PD_EINT7	 001:Output 011:PWM_6 101:RMII_TXCK 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PD6_SELECT 000:Input 010:LCD_D10 100:VO_D5 110:PD_EINT6	 001:Output 011:PWM_5 101:RMII_TXD0 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PD5_SELECT 000:Input 010:LCD_D7 100:VO_D4 110:PD_EINT5	 001:Output 011:PWM_4 101:RMII_TXD1 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD4_SELECT 000:Input	 001:Output

			010:LCD_D6 100:VO_D3 110:PD_EINT4	011:PWM_3 101:RMII_RXER 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD3_SELECT 000:Input 010:LCD_D5 100:VO_D2 110:PD_EINT3	 001:Output 011:PWM_2 101:RMII_CRS_DV 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000:Input 010:LCD_D4 100:VO_D1 110:PD_EINT2	 001:Output 011:PWM_1 101:RMII_RXD0 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000:Input 010:LCD_D3 100:VO_D0 110:PD_EINT1	 001:Output 011:PWM_0 101:RMII_RXD1 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	Reserved	

11.6.6.6. 0x0070 PD Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	Reserved
27	/	/	/
26:24	R/W	0x7	Reserved
23	/	/	/
22:20	R/W	0x7	Reserved
19	/	/	/
18:16	R/W	0x7	Reserved
15	/	/	/
14:12	R/W	0x7	Reserved
11	/	/	/
10:8	R/W	0x7	Reserved
7	/	/	/
6:4	R/W	0x7	Reserved
3	/	/	/

2:0	R/W	0x7	PD8_SELECT 000:Input 010:LCD_D12 100:VO_D7 110:PD_EINT8	 001:Output 011:PWM_7 101:RMII_TXEN 111:IO Disable

11.6.6.7. 0x0074 PD Configure Register 2 (Default Value: 0x0777_7777)

Offset: 0x0074			Register Name: PD_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	Reserved	
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT 000:Input 010:LCD_VSYNC 100:VO_VSYNC 110:PD_EINT21	 001:Output 011:Reserved 101:MDIO 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000:Input 010:LCD_HSYNC 100:VO_HSYNC 110:PD_EINT20	 001:Output 011:Reserved 101:MDC 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000:Input 010:LCD_DE 100:VO_FIELD 110:PD_EINT19	 001:Output 011:PWM_9 101: TCON_TRIG 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000:Input 010:LCD_CLK 100:VO_CLK 110:PD_EINT18	 001:Output 011:Reserved 101:EPHY_25M 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	Reserved	
3	/	/	/	
2:0	R/W	0x7	Reserved	

11.6.6.8. 0x007C PD Data Register (Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
21:0	R/W	0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.6.9. 0x0080 PD Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	Reserved
29:28	R/W	0x1	Reserved
27:26	R/W	0x1	Reserved
25:24	R/W	0x1	Reserved
23:22	R/W	0x1	Reserved
21:20	R/W	0x1	Reserved
19:18	R/W	0x1	Reserved
17:16	R/W	0x1	PD8_DRV PD8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PD7_DRV PD7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PD6_DRV PD6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PD5_DRV PD5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD4_DRV PD4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD3_DRV

			PD3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD2_DRV PD2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PD1_DRV PD1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	Reserved

11.6.6.10. 0x0084 PD Multi-Driving Register 1 (Default Value: 0x0000_1555)

Offset: 0x0084			Register Name: PD_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	Reserved
11:10	R/W	0x1	PD21_DRV PD21 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PD20_DRV PD20 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PD19_DRV PD19 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PD18_DRV PD18 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	Reserved
1:0	R/W	0x1	Reserved

11.6.6.11. 0x0088 PD Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**

31:18	/	/	/
17:16	R/W	0x0	PD8_PULL PD8 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
15:14	R/W	0x0	PD7_PULL PD7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PD6_PULL PD6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PD5_PULL PD5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PD4_PULL PD4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD3_PULL PD3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD2_PULL PD2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PD1_PULL PD1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	Reserved

11.6.6.12. 0x008C PD Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PD21_PULL PD21 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

9:8	R/W	0x0	PD20_PULL PD20 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PD19_PULL PD19 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PD18_PULL PD18 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:0	/	/	/

11.6.6.13. 0x0098 PE Configure Register 2 (Default Value: 0x0077_7777)

Offset: 0x0098			Register Name: PE_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x7	Reserved
19	/	/	/
18:16	R/W	0x7	Reserved
15	/	/	/
14:12	R/W	0x7	Reserved
11	/	/	/
10:8	R/W	0x7	Reserved
7	/	/	/
6:4	R/W	0x7	PE17_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:TWI0_SDA 110:PE_EINT17 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PE16_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:TWI0_SCK 110:PE_EINT16 111:IO Disable

11.6.6.14. 0x00A0 PE Data Register (Default Value: 0x0000_0000)

Offset: 0x00A0	Register Name: PE_DAT

Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
17:16	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.
15:0	/	/	/

11.6.6.15. 0x00A8 PE Multi-Driving Register 1 (Default Value: 0x0000_0555)

Offset: 0x00A8			Register Name: PE_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x1	Reserved
9:8	R/W	0x1	Reserved
7:6	R/W	0x1	Reserved
5:4	R/W	0x1	Reserved
3:2	R/W	0x1	PE17_DRV PE17 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PE16_DRV PE16 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.6.16. 0x00B0 PE Pull Register 1 (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PE_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	Reserved
9:8	R/W	0x0	Reserved
7:6	R/W	0x0	Reserved
5:4	R/W	0x0	Reserved
3:2	R/W	0x0	PE17_PULL PE17 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PE16_PULL PE16 Pull-up/down Select

			00: Pull-up/down disable	01: Pull-up
			10: Pull-down	11: Reserved

11.6.6.17. 0x00B4 PF Configure Register 0 (Default Value: 0x0777_7777)

Offset: 0x00B4			Register Name: PF_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:27	/	/	/	
26:24	R/W	0x7	PF6_SELECT 000:Input 010:Reserved 100:Reserved 110:PF_EINT6	 001:Output 011:Reserved 101:Reserved 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PF5_SELECT 000:Input 010:SDC0_D2 100:Reserved 110:PF_EINT5	 001:Output 011:JTAG_CK 101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PF4_SELECT 000:Input 010:SDC0_D3 100:Reserved 110:PF_EINT4	 001:Output 011:UART0_RX 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PF3_SELECT 000:Input 010:SDC0_CMD 100:Reserved 110:PF_EINT3	 001:Output 011:JTAG_DO 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PF2_SELECT 000:Input 010:SDC0_CLK 100:Reserved 110:PF_EINT2	 001:Output 011:UART0_TX 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PF1_SELECT 000:Input 010:SDC0_D0 100:Reserved 110:PF_EINT1	 001:Output 011:JTAG_DI 101:CPU_BIST1 111:IO Disable

3	/	/	/
2:0	R/W	0x7	PF0_SELECT 000:Input 001:Output 010:SDC0_D1 011:JTAG_MS 100:Reserved 101:CPU_BIST0 110:PF_EINT0 111:IO Disable

11.6.6.18. 0x00C4 PF Data Register (Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.6.19. 0x00C8 PF Multi-Driving Register 0 (Default Value: 0x0000_1555)

Offset: 0x00C8			Register Name: PF_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	PF6_DRV PF6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PF5_DRV PF5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PF4_DRV PF4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PF3_DRV PF3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PF2_DRV PF2 Multi-Driving Select 00: Level 0 01: Level 1

			10: Level 2	11: Level 3
3:2	R/W	0x1	PF1_DRV PF1 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
1:0	R/W	0x1	PF0_DRV PF0 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3

11.6.6.20. 0x00D0 PF Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:14	/	/	/	
13:12	R/W	0x0	PF6_PULL PF6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PF5_PULL PF5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PF4_PULL PF4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PF3_PULL PF3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PF2_PULL PF2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PF1_PULL PF1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PF0_PULL PF0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.6.21. 0x00D8 PG Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:UART1_RX 110:PG_EINT7 111:IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000:Input 001:Output 010:Reserved 011:Reserved 100:Reserved 101:UART1_TX 110:PG_EINT6 111:IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000:Input 001:Output 010:SDC1_D3 011:Reserved 100:Reserved 101:UART1_CTS 110:PG_EINT5 111:IO Disable
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000:Input 001:Output 010:SDC1_D2 011:Reserved 100:Reserved 101:UART1_RTS 110:PG_EINT4 111:IO Disable
15	/	/	/
14:12	R/W	0x7	PG3_SELECT 000:Input 001:Output 010:SDC1_D1 011:Reserved 100:Reserved 101:UART3_RTS 110:PG_EINT3 111:IO Disable
11	/	/	/
10:8	R/W	0x7	PG2_SELECT 000:Input 001:Output 010:SDC1_D0 011:Reserved 100:Reserved 101:UART3_CTS 110:PG_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PG1_SELECT 000:Input 001:Output 010:SDC1_CMD 011:Reserved

			100:Reserved 110:PG_EINT1	101:UART3_RX 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PG0_SELECT 000:Input 010:SDC1_CLK 100:Reserved 110:PG_EINT0	 001:Output 011:Reserved 101:UART3_TX 111:IO Disable

11.6.6.22. 0x00E8 PG Data Register (Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.6.23. 0x00EC PG Multi-Driving Register 0 (Default Value: 0x0000_5555)

Offset: 0x00EC			Register Name: PG_DRV0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:16	/	/	/	
15:14	R/W	0x1	PG7_DRV PG7 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
13:12	R/W	0x1	PG6_DRV PG6 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
11:10	R/W	0x1	PG5_DRV PG5 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
9:8	R/W	0x1	PG4_DRV PG4 Multi-Driving Select 00: Level 0 10: Level 2	 01: Level 1 11: Level 3
7:6	R/W	0x1	PG3_DRV	

			PG3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PG2_DRV PG2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PG1_DRV PG1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PG0_DRV PG0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.6.24. 0x00F4 PG Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0x0	PG7_PULL PG7 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
13:12	R/W	0x0	PG6_PULL PG6 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
11:10	R/W	0x0	PG5_PULL PG5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PG4_PULL PG4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PG3_PULL PG3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PG2_PULL PG2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

			10: Pull-down	11: Reserved
3:2	R/W	0x0	PG1_PULL PG1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PG0_PULL PG0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.6.25. 0x00FC PH Configure Register 0 (Default Value: 0x7777_7777)

Offset: 0x00FC			Register Name: PH_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PH7_SELECT 000:Input 010:PWM_7 100:UART0_TX 110:PH_EINT7	 001:Output 011:RMII_CRS_DV 101:UART2_RTS 111:IO Disable
27	/	/	/	
26:24	R/W	0x7	PH6_SELECT 000:Input 010:PWM_6 100:TWI2_SDA 110:PH_EINT6	 001:Output 011:RMII_RXD0 101:UART2_RX 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH5_SELECT 000:Input 010:PWM_5 100:TWI2_SCK 110:PH_EINT5	 001:Output 011:RMII_RXD1 101:UART2_TX 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH4_SELECT 000:Input 010:PWM_4 100:SPI1_CS1 110:PH_EINT4	 001:Output 011:I2S0_DIN 101:ONEWIRE 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH3_SELECT 000:Input 010:PWM_3 100:SPI1_CS0	 001:Output 011:I2S0_DOUT 101:UART3_RTS

			110:PH_EINT3	111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH2_SELECT 000:Input 010:PWM_2 100:SPI1_MISO 110:PH_EINT2	 001:Output 011:I2S0_LRCK 101:UART3_CTS 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH1_SELECT 000:Input 010:PWM_1 100:SPI1_MOSI 110:PH_EINT1	 001:Output 011:I2S0_BCLK 101:UART3_RX 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000:Input 010:PWM_0 100:SPI1_CLK 110:PH_EINT0	 001:Output 011:I2S0_MCLK 101:UART3_TX 111:IO Disable

11.6.6.26. 0x0100 PH Configure Register 1 (Default Value: 0x7777_7777)

Offset: 0x0100			Register Name: PH_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	Reserved	
27	/	/	/	
26:24	R/W	0x7	PH14_SELECT 000:Input 010:JTAG_DI 100:SPI1_CS0 110:PH_EINT14	 001:Output 011:MDIO 101:TWI3_SDA 111:IO Disable
23	/	/	/	
22:20	R/W	0x7	PH13_SELECT 000:Input 010:JTAG_DO 100:SPI1_MISO 110:PH_EINT13	 001:Output 011:MDC 101:TWI3_SCK 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PH12_SELECT 000:Input 010:JTAG_CK 100:SPI1_MOSI	 001:Output 011:RMII_TXEN 101:TWI2_SDA

			110:PH_EINT12	111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PH11_SELECT 000:Input 010:JTAG_MS 100:SPI1_CLK 110:PH_EINT11	 001:Output 011:RMII_TXCK 101:TWI2_SCK 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PH10_SELECT 000:Input 010:Reserved 100:TWI3_SDA 110:PH_EINT10	 001:Output 011:RMII_TXD0 101:UART0_RX 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000:Input 010:PWM_9 100:TWI3_SCK 110:PH_EINT9	 001:Output 011:RMII_TXD1 101:UART0_TX 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000:Input 010:PWM_8 100:UART0_RX 110:PH_EINT8	 001:Output 011:RMII_RXER 101:UART2_CTS 111:IO Disable

11.6.6.27. 0x010C PH Data Register (Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
14:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.6.28. 0x0110 PH Multi-Driving Register 0 (Default Value: 0x5555_5555)

Offset: 0x0110			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x1	Reserved

29:28	R/W	0x1	PH14_DRV PH14 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
27:26	R/W	0x1	PH13_DRV PH13 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
25:24	R/W	0x1	PH12_DRV PH12 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
23:22	R/W	0x1	PH11_DRV PH11 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
21:20	R/W	0x1	PH10_DRV PH10 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
19:18	R/W	0x1	PH9_DRV PH9 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
17:16	R/W	0x1	PH8_DRV PH8 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
15:14	R/W	0x1	PH7_DRV PH7 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
13:12	R/W	0x1	PH6_DRV PH6 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
11:10	R/W	0x1	PH5_DRV PH5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PH4_DRV PH4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PH3_DRV

			PH3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PH2_DRV PH2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PH1_DRV PH1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PH0_DRV PH0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.6.29. 0x0118 PH Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x0118			**Register Name: PH_PULL0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	Reserved
29:28	R/W	0x0	PH14_PULL PH14 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
27:26	R/W	0x0	PH13_PULL PH13 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
25:24	R/W	0x0	PH12_PULL PH12 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
23:22	R/W	0x0	PH11_PULL PH11 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
21:20	R/W	0x0	PH10_PULL PH10 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
19:18	R/W	0x0	PH9_PULL PH9 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up

			10: Pull-down	11: Reserved
17:16	R/W	0x0	PH8_PULL PH8 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
15:14	R/W	0x0	PH7_PULL PH7 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
13:12	R/W	0x0	PH6_PULL PH6 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
11:10	R/W	0x0	PH5_PULL PH5 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
9:8	R/W	0x0	PH4_PULL PH4 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
7:6	R/W	0x0	PH3_PULL PH3 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
5:4	R/W	0x0	PH2_PULL PH2 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
3:2	R/W	0x0	PH1_PULL PH1 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved
1:0	R/W	0x0	PH0_PULL PH0 Pull-up/down Select 00: Pull-up/down disable 10: Pull-down	 01: Pull-up 11: Reserved

11.6.6.30. 0x0120 PI Configure Register 0 (Default Value: 0x0007_7777)

Offset: 0x0120			Register Name: PI_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/

18:16	R/W	0x7	
15	/	/	/
14:12	R/W	0x7	
11	/	/	/
10:8	R/W	0x7	PI2_SELECT 000:Input 001:Output 010:CSI_SM_VS 011:TCON_TRIG 100:Reserved 101:TWI1_SDA 110:PI_EINT2 111:IO Disable
7	/	/	/
6:4	R/W	0x7	PI1_SELECT 000:Input 001:Output 010:CSI_SM_HS 011:Reserved 100:Reserved 101:TWI1_SCK 110:PI_EINT1 111:IO Disable
3	/	/	/
2:0	R/W	0x7	PI0_SELECT 000:Input 001:Output 010:CSI_MASTERCLK0 011:Reserved 100:Reserved 101:Reserved 110:PI_EINT0 111:IO Disable

11.6.6.31. 0x0130 PI Data Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PI_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4:0	R/W	0x0	PI_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.6.32. 0x0134 PI Multi-Driving Register 0 (Default Value: 0x0000_0155)

Offset: 0x0134			Register Name: PI_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x1	PI4_DRV PI4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

7:6	R/W	0x1	PI3_DRV PI3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PI2_DRV PI2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PI1_DRV PI1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PI0_DRV PI0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.6.33. 0x013C PI Pull Register 0 (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PI_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	PI4_PULL PI4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
7:6	R/W	0x0	PI3_PULL PI3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PI2_PULL PI2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x0	PI1_PULL PI1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x0	PI0_PULL PI0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

11.6.6.34. 0x0240 PC External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0240			Register Name: PC_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.6.35. 0x0250 PC External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0250			Register Name: PC_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.6.36. 0x0254 PC External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0254			Register Name: PC_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.6.37. 0x0258 PC External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0258			Register Name: PC_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.6.38. 0x0260 PD External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0260			Register Name: PD_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level

			0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
3:0	R/W	0x0	Reserved

11.6.6.39. 0x0264 PD External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x0264			Register Name: PD_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	R/W	0x0	Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

11.6.6.40. 0x0268 PD External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0268			Register Name: PD_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	Reserved
23:20	R/W	0x0	EINT21_CFG External INT21 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT20_CFG External INT20 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT19_CFG

			External INT19 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT18_CFG External INT18 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	Reserved
3:0	R/W	0x0	Reserved

11.6.6.41. 0x0270 PD External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0270			Register Name: PD_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W	0x0	Reserved
21	R/W	0x0	EINT21_CTL External INT21 Enable 0: Disable 1: Enable
20	R/W	0x0	EINT20_CTL External INT20 Enable 0: Disable 1: Enable
19	R/W	0x0	EINT19_CTL External INT19 Enable 0: Disable 1: Enable
18	R/W	0x0	EINT18_CTL External INT18 Enable 0: Disable 1: Enable
17	R/W	0x0	Reserved
16	R/W	0x0	Reserved
15	R/W	0x0	Reserved

14	R/W	0x0	Reserved
13	R/W	0x0	Reserved
12	R/W	0x0	Reserved
11	R/W	0x0	Reserved
10	R/W	0x0	Reserved
9	R/W	0x0	Reserved
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.6.42. 0x0274 PD External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0274			Register Name: PD_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22	R/W1C	0x0	Reserved
21	R/W1C	0x0	EINT21_STATUS External INT21 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
20	R/W1C	0x0	EINT20_STATUS External INT20 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
19	R/W1C	0x0	EINT19_STATUS External INT19 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
18	R/W1C	0x0	EINT18_STATUS External INT18 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
17	R/W1C	0x0	Reserved
16	R/W1C	0x0	Reserved
15	R/W1C	0x0	Reserved
14	R/W1C	0x0	Reserved
13	R/W1C	0x0	Reserved
12	R/W1C	0x0	Reserved
11	R/W1C	0x0	Reserved
10	R/W1C	0x0	Reserved
9	R/W1C	0x0	Reserved
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending

			Write ‘1’ to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

11.6.6.43. 0x0278 PD External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: PD_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n

			The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.6.44. 0x0288 PE External Interrupt Configure Register 2 (Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: PE_EINT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	EINT17_CFG External INT17 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT16_CFG External INT16 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.6.45. 0x0290 PE External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PE_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	EINT17_CTL External INT17 Enable 0: Disable 1: Enable
16	R/W	0x0	EINT16_CTL External INT16 Enable 0: Disable 1: Enable

15:0	/	/	/

11.6.6.46. 0x0294 PE External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0294			Register Name: PE_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	EINT17_STATUS External INT17 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
16	R/W1C	0x0	EINT16_STATUS External INT16 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
15:0	/	/	/

11.6.6.47. 0x0298 PE External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PE_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.6.48. 0x02A0 PF External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PF_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge

			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

11.6.6.49. 0x0280 PF External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PF_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.6.50. 0x02B4 PF External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: PF_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.6.51. 0x02B8 PF External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02B8	Register Name: PF_EINT_DEB

Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.6.52. 0x02C0 PG External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name:PG_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level

			0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.6.53. 0x02D0 PG External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: PG_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable

			1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.6.54. 0x02D4 PG External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02D4			Register Name: PG_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending

			Write ‘1’ to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear

11.6.6.55. 0x02D8 PG External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: PG_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz

			1: HOSC 24MHz

11.6.6.56. 0x02E0 PH External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x02E0			Register Name:PH_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	EINT7_CFG External INT7 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
27:24	R/W	0x0	EINT6_CFG External INT6 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

			0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.6.57. 0x02E4 PH External Interrupt Configure Register 1 (Default Value: 0x0000_0000)

Offset: 0x02E4			Register Name: PH_EINT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	EINT14_CFG External INT14 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
23:20	R/W	0x0	EINT13_CFG External INT13 Mode 0000: Positive Edge 0001: Negative Edge

			0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT12_CFG External INT12 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT11_CFG External INT11 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT10_CFG External INT10 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT9_CFG External INT9 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT8_CFG External INT8 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.6.58. 0x02F0 PH External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x02F0			Register Name: PH_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EINT14_CTL External INT14 Enable 0: Disable 1: Enable
13	R/W	0x0	EINT13_CTL External INT13 Enable 0: Disable 1: Enable
12	R/W	0x0	EINT12_CTL External INT12 Enable 0: Disable 1: Enable
11	R/W	0x0	EINT11_CTL External INT11 Enable 0: Disable 1: Enable
10	R/W	0x0	EINT10_CTL External INT10 Enable 0: Disable 1: Enable
9	R/W	0x0	EINT9_CTL External INT9 Enable 0: Disable 1: Enable
8	R/W	0x0	EINT8_CTL External INT8 Enable 0: Disable 1: Enable
7	R/W	0x0	EINT7_CTL External INT7 Enable 0: Disable 1: Enable
6	R/W	0x0	EINT6_CTL External INT6 Enable 0: Disable 1: Enable
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable

4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable
2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.6.59. 0x02F4 PH External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x02F4			Register Name: PH_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W1C	0x0	EINT14_STATUS External INT14 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
13	R/W1C	0x0	EINT13_STATUS External INT13 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
12	R/W1C	0x0	EINT12_STATUS External INT12 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
11	R/W1C	0x0	EINT11_STATUS External INT11 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
10	R/W1C	0x0	EINT10_STATUS External INT10 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
9	R/W1C	0x0	EINT9_STATUS External INT9 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
8	R/W1C	0x0	EINT8_STATUS External INT8 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
7	R/W1C	0x0	EINT7_STATUS External INT7 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
6	R/W1C	0x0	EINT6_STATUS External INT6 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending

			1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.6.60. 0x02F8 PH External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x02F8			Register Name: PH_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.6.61. 0x0300 PI External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: PI_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode

			0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.6.62. 0x0310 PI External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0310			Register Name: PI_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable

2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.6.63. 0x0314 PI External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: PI_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.6.64. 0x0318 PI External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0318			Register Name: PI_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.6.65. 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC-IO&PH_Port POWER MODE Select 0: 3.3V 1: 1.8V
11:9	/	/	/
8	R/W	0x0	PI_POWER MODE Select 0: 3.3V 1: 1.8V
7	/	/	/
6	R/W	0x0	PG_POWER MODE Select 0: 3.3V 1: 1.8V
5	R/W	0x0	PF_POWER MODE Select 0: 3.3V 1: 1.8V
4	R/W	0x0	PE_POWER MODE Select 0: 3.3V 1: 1.8V
3	R/W	0x0	PD_POWER MODE Select 0: 3.3V 1: 1.8V
2	R/W	0x0	PC_POWER MODE Select 0: 3.3V 1: 1.8V
1:0	/	/	/

NOTE

When the power domain of GPIO is larger than 1.8V, the withstand voltage is set to 3.3V mode, the corresponding value in 0x0340 register is set to 0.

When the power domain of GPIO is 1.8V, the withstand voltage is set to 1.8V mode, the corresponding value in 0x0340 register is set to 1.

11.6.6.66. 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	VCC-IO&PH_Port Withstand Voltage Mode Select Control 0: Enable 1: Disable
11:9	/	/	/
8	R/W	0x0	VCC-PI Withstand Voltage Mode Select Control 0: Enable 1: Disable
7	/	/	/
6	R/W	0x0	VCC-PG Withstand Voltage Mode Select Control 0: Enable 1: Disable
5	R/W	0x0	VCC-PF Withstand Voltage Mode Select Control 0: Enable 1: Disable
4	R/W	0x0	VCC-PE Withstand Voltage Mode Select Control 0: Enable 1: Disable
3	R/W	0x0	VCC-PD Withstand Voltage Mode Select Control 0: Enable 1: Disable
2	R/W	0x0	VCC-PC Withstand Voltage Mode Select Control 0: Enable 1: Disable
1	/	/	/

NOTE

For 1.8V and 3.3V power, the withstand function is enabled by default, the corresponding bit in 0x0344 register is set to 0.

For 2.5V power, the withstand function is disabled, the corresponding bit in 0x0344 register is set to 1, and the withstand mode in 0x0340 register needs be set to 3.3V.

11.6.6.67. 0x0348 PIO Group Power Value Register

Offset: 0x0348		Register Name: PIO_POW_Val
Bit	**Read/Write**	**Description**
31:17	/	/
16	R	VCC-IO&PH_Port Power Value
15:9	/	/
8	R	PI_Port Power Value
7	/	/
6	R	PG_Port Power Value
5	R	PF_Port Power Value
4	R	PE_Port Power Value
3	R	PD_Port Power Value
2	R	PC_Port Power Value
1:0	/	/

NOTE

When the reading value of the 0x0348 register is 0, it indicates that IO power voltage is greater than 2.5V.
When the reading value of the 0x0348 register is 1, it indicates that IO power voltage is less than 2.0V.

11.6.6.68. 0x0350 PIO Group Power Voltage Select Control Register (Default Value: 0x0000_0001)

Offset: 0x0350			Register Name: PIO_PV_SEL_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	VCC-PF Power Voltage Select Control 0: 1.8V 1: 3.3V

11.6.7. V833 GPIO(PL) Register Description

11.6.7.1. 0x0000 PL Configure Register 0 (Default Value: 0x0077_7777)

Offset: 0x0000			Register Name: PL_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x7	PL5_SELECT 000:Input 001:Output 010:Reserved 011:Reserved

			100:Reserved 110:S_PL_EINT5	101:Reserved 111:IO Disable
19	/	/	/	
18:16	R/W	0x7	PL4_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT4	001:Output 011:Reserved 101:Reserved 111:IO Disable
15	/	/	/	
14:12	R/W	0x7	PL3_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT3	001:Output 011:Reserved 101:Reserved 111:IO Disable
11	/	/	/	
10:8	R/W	0x7	PL2_SELECT 000:Input 010:Reserved 100:Reserved 110:S_PL_EINT2	001:Output 011:Reserved 101:Reserved 111:IO Disable
7	/	/	/	
6:4	R/W	0x7	PL1_SELECT 000:Input 010:S_RSB_SDA 100:Reserved 110:S_PL_EINT1	001:Output 011:S_TWI0_SDA 101:Reserved 111:IO Disable
3	/	/	/	
2:0	R/W	0x7	PL0_SELECT 000:Input 010:S_RSB_SCK 100:Reserved 110:S_PL_EINT0	001:Output 011:S_TWI0_SCK 101:Reserved 111:IO Disable

11.6.7.2. 0x0010 PL Data Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PL_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	PL_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

11.6.7.3. 0x0014 PL Multi-Driving Register 0 (Default Value: 0x0000_0555)

Offset: 0x0014			Register Name: PL_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x1	PL5_DRV PL5 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
9:8	R/W	0x1	PL4_DRV PL4 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
7:6	R/W	0x1	PL3_DRV PL3 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
5:4	R/W	0x1	PL2_DRV PL2 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
3:2	R/W	0x1	PL1_DRV PL1 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3
1:0	R/W	0x1	PL0_DRV PL0 Multi-Driving Select 00: Level 0 01: Level 1 10: Level 2 11: Level 3

11.6.7.4. 0x001C PL Pull Register 0 (Default Value: 0x0000_0005)

Offset: 0x001C			Register Name: PL_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:10	R/W	0x0	PL5_PULL PL5 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
9:8	R/W	0x0	PL4_PULL PL4 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

7:6	R/W	0x0	PL3_PULL PL3 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
5:4	R/W	0x0	PL2_PULL PL2 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
3:2	R/W	0x1	PL1_PULL PL1 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved
1:0	R/W	0x1	PL0_PULL PL0 Pull-up/down Select 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

11.6.7.5. 0x0200 PL External Interrupt Configure Register 0 (Default Value: 0x0000_0000)

Offset: 0x0200			Register Name:PL_EINT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R/W	0x0	EINT5_CFG External INT5 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
19:16	R/W	0x0	EINT4_CFG External INT4 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
15:12	R/W	0x0	EINT3_CFG External INT3 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level

			0100: Double Edge (Positive/Negative) Others: Reserved
11:8	R/W	0x0	EINT2_CFG External INT2 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
7:4	R/W	0x0	EINT1_CFG External INT1 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved
3:0	R/W	0x0	EINT0_CFG External INT0 Mode 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/Negative) Others: Reserved

11.6.7.6. 0x0210 PL External Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0210			Register Name: PL_EINT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	EINT5_CTL External INT5 Enable 0: Disable 1: Enable
4	R/W	0x0	EINT4_CTL External INT4 Enable 0: Disable 1: Enable
3	R/W	0x0	EINT3_CTL External INT3 Enable 0: Disable 1: Enable

2	R/W	0x0	EINT2_CTL External INT2 Enable 0: Disable 1: Enable
1	R/W	0x0	EINT1_CTL External INT1 Enable 0: Disable 1: Enable
0	R/W	0x0	EINT0_CTL External INT0 Enable 0: Disable 1: Enable

11.6.7.7. 0x0214 PL External Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0214			Register Name: PL_EINT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W1C	0x0	EINT5_STATUS External INT5 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
4	R/W1C	0x0	EINT4_STATUS External INT4 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
3	R/W1C	0x0	EINT3_STATUS External INT3 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
2	R/W1C	0x0	EINT2_STATUS External INT2 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
1	R/W1C	0x0	EINT1_STATUS External INT1 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear
0	R/W1C	0x0	EINT0_STATUS

			External INT0 Pending Bit 0: No IRQ pending 1: IRQ pending Write '1' to clear

11.6.7.8. 0x0218 PL External Interrupt Debounce Register (Default Value: 0x0000_0000)

Offset: 0x0218			Register Name: PL_EINT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

11.6.7.9. 0x0340 PIO Group Withstand Voltage Mode Select Register (Default Value: 0x0000_0000)

Offset: 0x0340			Register Name: PIO_POW_MOD_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	PL_POWER MODE Select 0: 3.3V 1: 1.8V

NOTE

When the power domain of GPIO is larger than 1.8V, the withstand voltage is set to 3.3V mode, the corresponding value in 0x0340 register is set to 0.

When the power domain of GPIO is 1.8V, the withstand voltage is set to 1.8V mode, the corresponding value in 0x0340 register is set to 1.

11.6.7.10. 0x0344 PIO Group Withstand Voltage Mode Select Control Register (Default Value: 0x0000_0000)

Offset: 0x0344			Register Name: PIO_POW_MS_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	VCC-PL Withstand Voltage Mode Select Control

			0：Enable 1：Disable

NOTE

For 1.8V and 3.3V power, the withstand function is enabled by default, the corresponding bit in 0x0344 register is set to 0.

For 2.5V power, the withstand function is disabled, the corresponding bit in 0x0344 register is set to 1, and the withstand mode in 0x0340 register needs be set to 3.3V.

11.6.7.11. 0x0348 PIO Group Power Value Register

Offset: 0x0348		Register Name: PIO_POW_Val
Bit	**Read/Write**	**Description**
31:1	/	/
0	R	PL_Port Power Value **When the reading value is 0, it indicates that IO power voltage is greater than 2.5V.** **When the reading value is 1, it indicates that IO power voltage is less than 2.0V.**

11.7. GPADC

11.7.1. Overview

The General Purpose ADC(GPADC) is one analog to digital converter with 12-bit sampling resolution. This ADC is a type of successive approximation register (SAR) converter.

The GPADC has the following features:

- 12-bit resolution
- 8-bit effective SAR type A/D converter
- 64 FIFO depth of data register
- Power reference voltage: 1.8V, analog input voltage range: 0 to 1.8V
- Maximum sampling frequency: 1MHz
- Supports data compare and interrupt
- Supports DMA transport
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

NOTE

V833 has two GPADC channels. V831 has only one GPADC channel.

11.7.2. Block Diagram

Figure 11-48 shows the block diagram of the GPADC.

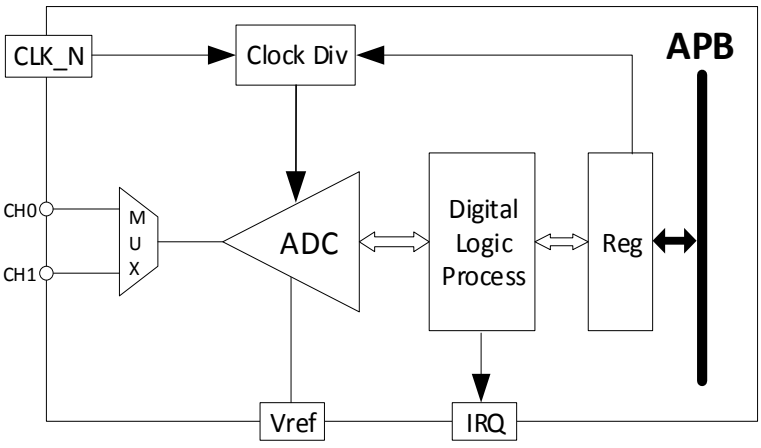

Figure 11- 48. GPADC Block Diagram

11.7.3. Operations and Functional Descriptions

11.7.3.1. External Signals

Table 11-31 describes the external signals of GPADC.

Table 11- 31. GPADC External Signals

V833 Signal	V831 Signal	Description	Type
GPADC0	GPADC0	ADC Input Channel0	AI
GPADC1	/	ADC Input Channel1	AI

11.7.3.2. Clock Sources

GPADC has one clock source. Table 11-32 describes the clock source for GPADC. Users can see **Clock Controller Unit(CCU)** for clock setting, configuration and gating information.

Table 11- 32. GPADC Clock Sources

Clock Sources	Description
OSC24M	24MHz

11.7.3.3. GPADC Work Mode

(1).Single conversion mode

GPADC completes one conversion in specified channel, the converted data is updated at the data register of corresponding channel.

(2).Continuous conversion mode

GPADC has continuous conversion in specified channel until the software stops, the converted data is updated at the data register of corresponding channel.

(3).Burst conversion mode

GPADC samples and converts in the specified channel, and sequentially stores the results in FIFO.

11.7.3.4. Clock and Timing Requirements

CLK_IN = 24MHz

CONV_TIME(Conversion Time) = 1/(24MHz/14Cycles) =0.583 (us)

TACQ> 10RC (R is output impedance of ADC sample circuit, C= 6.4pF)

ADC Sample Frequency > TACQ+CONV_TIME

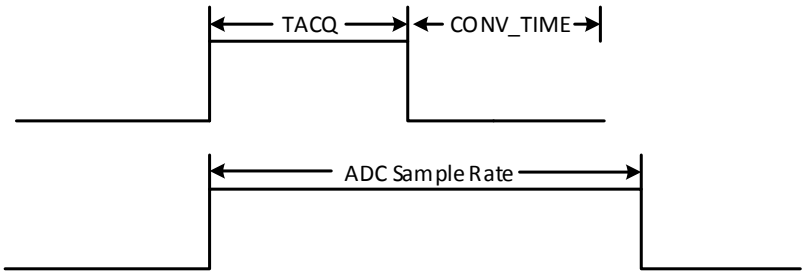

Figure 11- 49. GPADC Clock and Timing Requirement

11.7.3.5. GPADC Calculate Formula

GPADC calculate formula: GPADC_DATA = Vin/V_{REF}*4096
Where:
V_{REF}=1.8V

11.7.4. Programming Guidelines

The GPADC initial process is as follows.

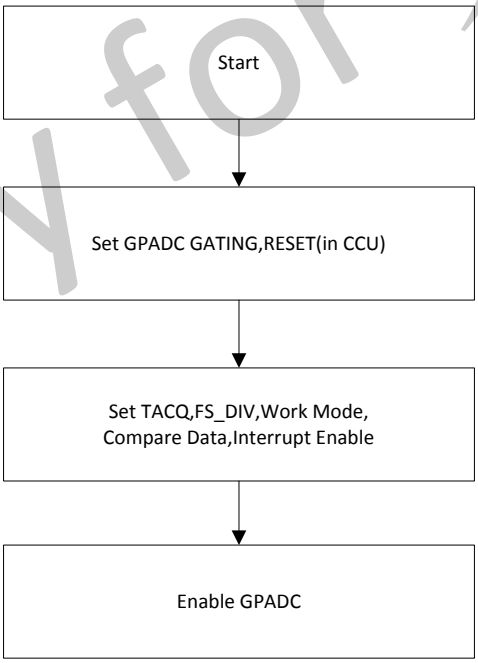

Figure 11- 50. GPADC Initial Process

11.7.5. Register List

Module Name	Base Address
GPADC	0x05070000

Register Name	Offset	Description
GP_SR_CON	0x0000	GPADC Sample Rate Configure Register
GP_CTRL	0x0004	GPADC Control Register
GP_CS_EN	0x0008	GPADC Compare and Select Enable Register
GP_FIFO_INTC	0x000C	GPADC FIFO Interrupt Control Register
GP_FIFO_INTS	0x0010	GPADC FIFO Interrupt Status Register
GP_FIFO_DATA	0x0014	GPADC FIFO Data Register
GP_CDATA	0x0018	GPADC Calibration Data Register
GP_DATAL_INTC	0x0020	GPADC Data Low Interrupt Configure Register
GP_DATAH_INTC	0x0024	GPADC Data High Interrupt Configure Register
GP_DATA_INTC	0x0028	GPADC Data Interrupt Configure Register
GP_DATAL_INTS	0x0030	GPADC Data Low Interrupt Status Register
GP_DATAH_INTS	0x0034	GPADC Data High Interrupt Status Register
GP_DATA_INTS	0x0038	GPADC Data Interrupt Status Register
GP_CH0_CMP_DATA	0x0040	GPADC CH0 Compare Data Register
GP_CH1_CMP_DATA	0x0044	GPADC CH1 Compare Data Register
GP_CH0_DATA	0x0080	GPADC CH0 Data Register
GP_CH1_DATA	0x0084	GPADC CH1 Data Register

11.7.6. Register Description

11.7.6.1. 0x0000 GPADC Sample Rate Configure Register (Default Value: 0x01DF_002F)

Offset: 0x0000			Register Name: GP_SR_CON
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 16	R/W	0x1DF	FS_DIV ADC sample frequency divider CLK_IN/(n+1) Default value: 50K
15:0	R/W	0x2F	TACQ ADC acquire time CLK_IN/(N+1) Default value: 2us

11.7.6.2. 0x0004 GPADC Control Register (Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: GP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/ W	0x0	ADC_FIRST_DLY ADC First Convert Delay Setting ADC conversion of each channel is delayed by N samples.

23	R/ W	0x1	ADC_AUTOCALI_EN ADC Auto Calibration
22	/	/	/
21:20	R/W	0x0	ADC_OP_BIAS ADC OP Bias Adjust the bandwidth of the ADC amplifier
19:18	R/W	0x0	GPADC Work Mode 00: Single conversion mode 01: Reserved 10: Continuous conversion mode 11: Burst conversion mode
17	R/W	0x0	ADC_CALI_EN ADC Calibration 1: Start Calibration, it is cleared to 0 after calibration
16	R/W	0x0	ADC_EN ADC Function Enable Before the bit is enabled, configure ADC parameters including the work mode and channel number,etc. 0: Disable 1: Enable
15:0	/	/	/

11.7.6.3. 0x0008 GPADC Compare and Select Enable Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GP_CS_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	ADC_CH1_CMP_EN Channel 1 Compare Enable 0: Disable 1: Enable
16	R/W	0x0	ADC_CH0_CMP_EN Channel 0 Compare Enable 0: Disable 1: Enable
15:2	/	/	/
1	R/W	0x0	ADC_CH1_SELECT Analog input channel 1 Select 0: Disable 1: Enable
0	R/W	0x0	ADC_CH0_SELECT Analog input channel 0 Select 0: Disable

			1: Enable

11.7.6.4. 0x000C GPADC FIFO Interrupt Control Register (Default Value: 0x0000_1F00)

Offset: 0x000C			Register Name: GP_FIFO_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	FIFO_OVERRUN_IRQ_EN ADC FIFO Overrun IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	FIFO_DATA_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13:8	R/W	0x1F	FIFO_TRIG_LEVEL Interrupt trigger level for ADC Trigger Level = TXTL + 1
7:5	/	/	/
4	R/WAC	0x0	FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, clear automatically to '0'.
3:0	/	/	/

11.7.6.5. 0x0010 GPADC FIFO Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: GP_FIFO_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	FIFO_OVERRUN_PENDING ADC FIFO Overrun IRQ Pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
16	R/W1C	0x0	FIFO_DATA_PENDING ADC FIFO Data Available Pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

15:14	/	/	/
13:8	R	0x0	RXA_CNT ADC FIFO available sample word counter
7:0	/	/	/

11.7.6.6. 0x0014 GPADC FIFO Data Register

Offset: 0x0014			Register Name: GP_FIFO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	UDF	GP_FIFO_DATA GPADC Data in FIFO

11.7.6.7. 0x0018 GPADC Calibration Data Register (Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: GP_CDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	GP_CDATA GPADC Calibration Data

11.7.6.8. 0x0020 GPADC Low Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GP_DATAL_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CH1_LOW_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_LOW_IRQ_EN 0: Disable 1: Enable

11.7.6.9. 0x0024 GPADC High Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GP_DATAH_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CH1_HIG_IRQ_EN 0: Disable

			1: Enable
0	R/W	0x0	CH0_HIG_IRQ_EN 0: Disable 1: Enable

11.7.6.10. 0x0028 GPADC DATA Interrupt Configure Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: GP_DATA_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CH1_DATA_IRQ_EN 0: Disable 1: Enable
0	R/W	0x0	CH0_DATA_IRQ_EN 0: Disable 1: Enable

11.7.6.11. 0x0030 GPADC Low Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: GP_DATAL_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	CH1_LOW_PENGDING 1: Channel 1 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_LOW_PENGDING 1: Channel 0 Voltage Low Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

11.7.6.12. 0x0034 GPADC High Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GP_DATAH_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	CH1_HIG_PENGDING 0: No Pending IRQ 1: Channel 1 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

0	R/W1C	0x0	CH0_HIG_PENGDING 0: No Pending IRQ 1: Channel 0 Voltage High Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

11.7.6.13. 0x0038 GPADC Data Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GP_DATA_INTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	CH1_DATA_PENGDING 0: No Pending IRQ 1: Channel 1 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	CH0_DATA_PENGDING 0: No Pending IRQ 1: Channel 0 Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

11.7.6.14. 0x0040 GPADC CH0 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0040			Register Name: GP_CH0_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH0_CMP_HIG_DATA Channel 0 Voltage High Value
15:12	/	/	/
11:0	R/W	0x400	CH0_CMP_LOW_DATA Channel 0 Voltage Low Value

11.7.6.15. 0x0044 GPADC CH1 Compare Data Register (Default Value: 0x0BFF_0400)

Offset: 0x0044			Register Name: GP_CH1_CMP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0xBFF	CH1_CMP_HIG_DATA Channel 1 Voltage High Value
15:12	/	/	/

11:0	R/W	0x400	CH1_CMP_LOW_DATA Channel 1 Voltage Low Value

11.7.6.16. 0x0080 GPADC CH0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: GP_CH0_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH0_DATA Channel 0 Data

11.7.6.17. 0x0084 GPADC CH1 Data Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: GP_CH1_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x000	GP_CH1_DATA Channel 1 Data

11.8. PWM

11.8.1. Overview

The PWM controller has 10 PWM channels(PWM0,PWM1,PWM2,PWM3,PWM4,PWM5,PWM6,PWM7,PWM8,PWM9), and divides to 5 PWM pairs:PWM01 pair,PWM23 pair,PWM45 pair,PWM67 pair,PWM89 pair. PWM01 pair consists of PWM0 and PWM1, PWM23 pair consists of PWM2 and PWM3, PWM45 pair consists of PWM4 and PWM5, PWM67 pair consists of PWM6 and PWM7, PWM89 pair consists of PWM8 and PWM9.

Each PWM channel supports two functions including PWM output and capture input. The clock sources of PWM channel have OSC24M and APB1. PWM channel can output single-pulse waveform or long-period waveform, the frequency range of the output waveform is from 0Hz to 24/100MHz. PWM also can capture input waveform. PWM channel captures the current value of 16-bit adding-counter at the external rising edge, and loads it to Capture Rise Lock Register, PWM channel captures the current value of 16-bit adding-counter at the external falling edge, and loads it to Capture Fall Lock Register, then the frequency of the external clock can be calculated accurately by the value of Capture Rise Lock Register and Capture Fall Lock Register.

PWM pair can output complementary waveform pair or dead-time PWM pair. When the two channels at a PWM pair have the same prescale, the same period register and opposite active state, then the PWM pair outputs a complementary waveform pair; when the programmable dead-time generator of PWM pair is enabled, then the PWM pair outputs the waveform pair with dead-time, and the dead-time is controllable.

PWM channel can configure to generate interrupt. PWM is as output function, when 16-bit adding-counter is equal to the value of entire cycle, PWM channel can be enabled to generate interrupt. PWM is as input function, when PWM channel captures the external rising edge, PWM channel can be enabled to generate one interrupt; when PWM channel captures the external falling edge, PWM channel can be enabled to generated one interrupt; when PWM channel captures rising edge or falling edge, PWM can trigger interrupt.

The PWM has the following features:

- 10 PWM channels(5 PWM pairs)
- Supports pulse(configurable pulse number),cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0 ~ 24MHz/100MHz
- Various duty-cycle: 0% ~100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input
- The PWM start/stop phase is controllable

11.8.2. Block Diagram

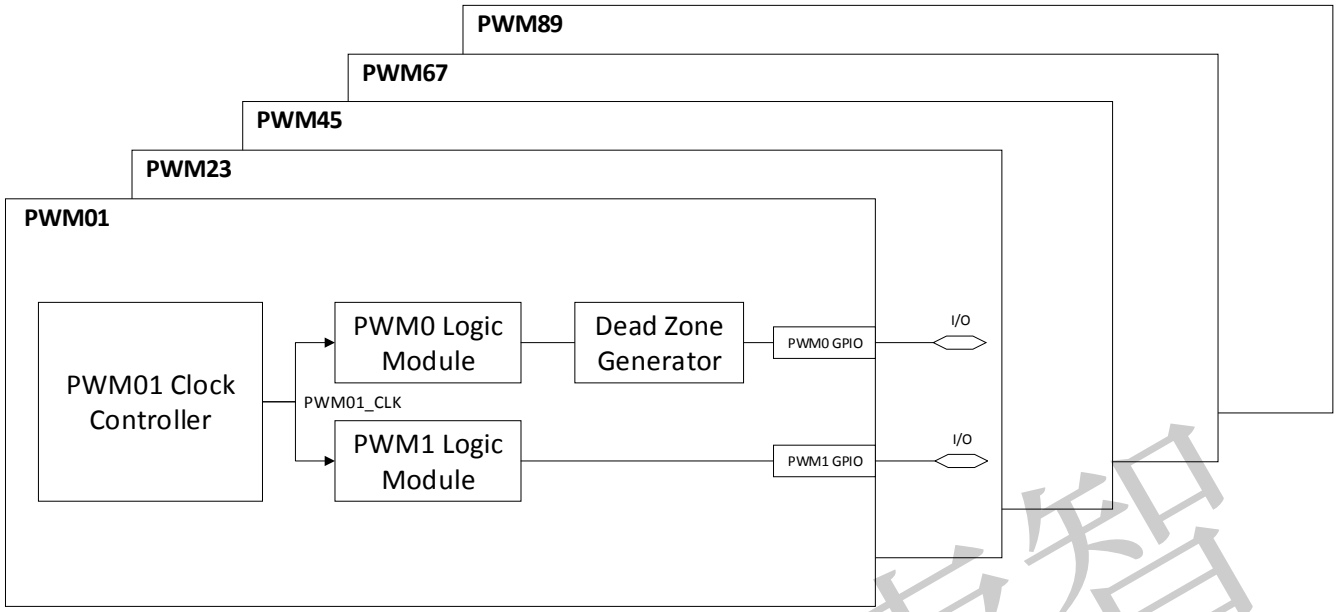

Figure 11- 51. PWM Block Diagram

Each PWM pair consists of 1 clock module, 2 timer logic module and 1 programmable dead-time generator.

11.8.3. Operations and Functional Descriptions

11.8.3.1. External Signals

Table 11-33 describes the external signals of the PWM.

Table 11- 33. PWM External Signals

Signal	Description	Type
PWM0	Pulse Width Module Channel0	I/O
PWM1	Pulse Width Module Channel1	I/O
PWM2	Pulse Width Module Channel2	I/O
PWM3	Pulse Width Module Channel3	I/O
PWM4	Pulse Width Module Channel4	I/O
PWM5	Pulse Width Module Channel5	I/O
PWM6	Pulse Width Module Channel6	I/O
PWM7	Pulse Width Module Channel7	I/O
PWM8	Pulse Width Module Channel8	I/O
PWM9	Pulse Width Module Channel9	I/O

11.8.3.2. Typical Application

- Suitable for display device, such as LCD

- Suitable for electric motor control

11.8.3.3. Clock Controller

Using PWM01 as an example, the clock controller diagram is as follows. Other PWM pairs(PWM23, PWM45, PWM67, PWM89) clock controller diagrams are the same as PWM01.

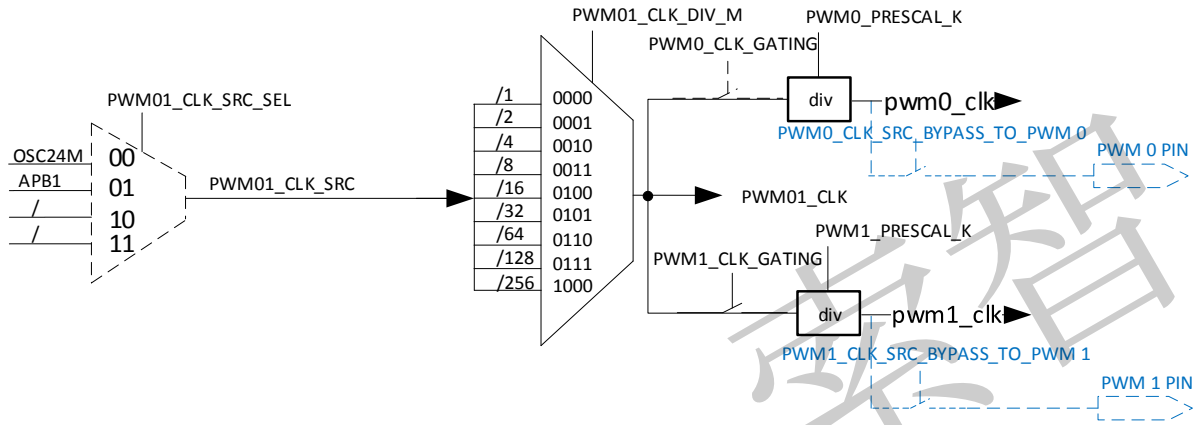

Figure 11- 52. PWM01 Clock Controller Diagram

The clock controller of each PWM pair(for example: PWM01) includes clock source select(PWM01_CLK_SRC_SEL), the first-level exponent divider (PWM01_CLK_DIV_M), the second-level count divider(PRESCAL_K), clock source bypass(CLK_SRC_BYPASS) and clock switch(PWM01_CLK_GATING).

The clock sources of PWM have OSC24M and APB1 Bus. OSC24M comes from external high frequency oscillator, APB1 is APB1 bus clock, usually is 100MHz.

The clock source bypass function is that clock source directly accesses PWM output, the PWM output waveform is the waveform of clock controller output. The BYPASS gridlines in the above figure indicates clock source bypass function, the details about implement, please see Figure 11-52.

11.8.3.4. PWM Output

Using PWM01 as an example, Figure 11-52 indicates PWM01 output logic module diagram. Other PWM pairs(PWM23, PWM45, PWM67, PWM89) logic module diagrams are the same as PWM01.

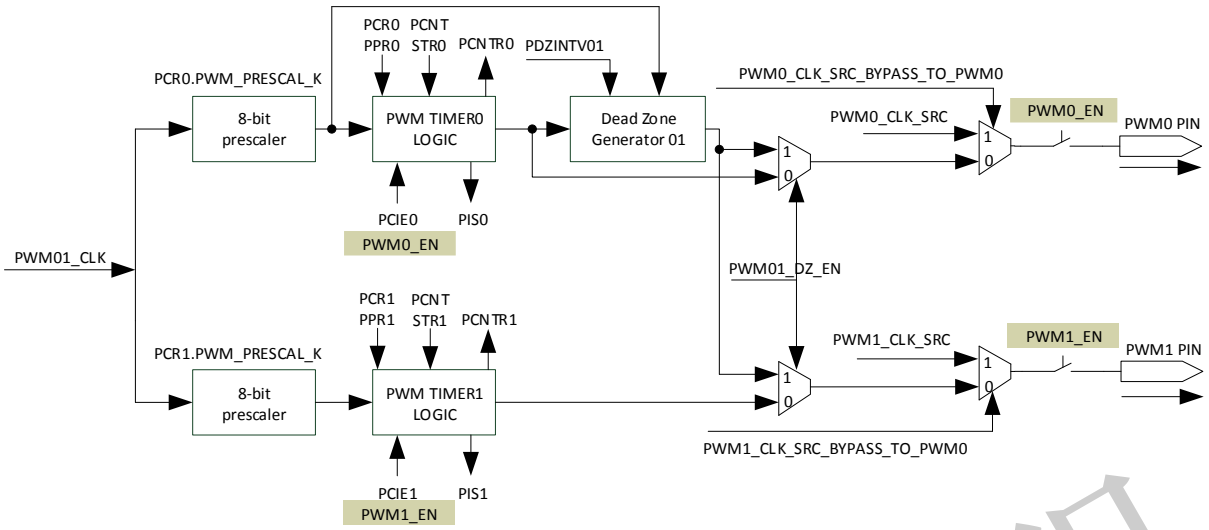

Figure 11- 53. PWM01 Output Logic Module Diagram

PWM Timer Logic module(PWM_TIMER_LOGIC) consists of one 16-bit up-counter(PCNTR) and three 16-bit parameters(PWM_ENTIRE_CYCLE, PWM_ACTIVE_CYCLE and PWM_CNTSTART).

The PWM_ENTIRE_CYCLE is used for PWM period control, the PWM_ACTIVE_CYCLE is used for duty-cycle control, the PWM_CNTSTART is used for phase output control(multi-channel synchronous work requirement).

The PWM_ENTIRE_CYCLE and PWM_ACTIVE_CYCLE support cache loading, after PWM output is enabled, the register values of PWM_ENTIRE_CYCLE and PWM_ACTIVE_CYCLE can be changed anytime, the changed value caches into the cache register. When PCNTR count outputs a period of PWM waveform, the value of the cache register can be updated for PCNTR controlling. Cache-loading is good to avoid unstable PWM output waveform with burred feature when updating PWM_ENTIRE_CYCLE and PWM_ACTIVE_CYCLE.

PWM_CNTSTART does support cache loading, only can be configured before PWM output enable.

PWM supports cycle and pulse waveform output.
Cycle mode: PWM repeatedly outputs the setting waveform, that is, a continuous square wave.
Pulse mode: After the PWM_PUL_CNT is pre-set, PWM outputs (PWM_PULNUM+1) cycles of PWM waveform, that is, the waveform of several pulses.

11.8.3.5. PWM Output Period, Duty-Cycle and Phase

The period, duty-cycle and phase of PWM output waveform are decided by the PCNTR, PWM_ENTIRE_CYCLE, PWM_ACT_CYCLE and PWM_CNTSTART. The rule of the comparator is as follows.

- PCNTR = (PCNTR==PWM_ENTIRE_CYCLE)? 0 : PCNTR + 1
- The PCNTR is started to count by PWM_CNTSTART, the (PWM_ENTIRE_CYCLE+1) is 1 PWM period.
- PCNTR >= (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “active state”
- PCNTR < (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “~ (active state)”

11.8.3.5.1. Period and Duty-Cycle

Active state can be programmatic controlled at the PCR of each PWM channel. Using PWM0 as an example:

(1) Active state of PWM0 channel is high level (PCR0. PWM_ACT_STA = 1)

When PCNTR0 > (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1(high level).

When PCNTR0 <= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0(low level).

The formula of PWM output period and duty-cycle is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0. PWM_ENTIRE_CYCLE + 1)

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE + 1 - PPR0.PWM_ACT_CYCLE)

Duty-cycle = (high level time) / (1 period time)

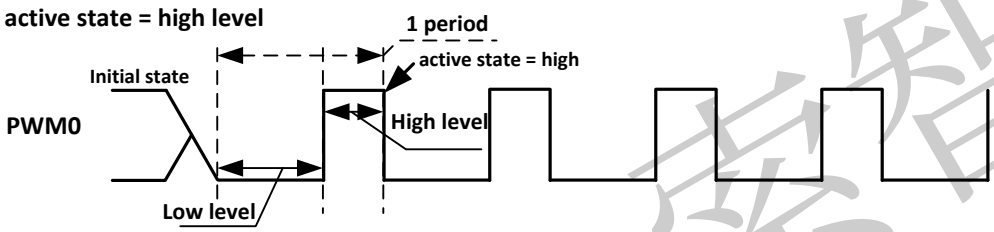

Figure 11- 54. Period and Duty-Cycle in PWM0 High Level Active State

(2) Active state of PWM0 channel is low level (PCR0. PWM_ACT_STA = 0)

When PCNTR0 > (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 0.

When PCNTR0 <= (PPR0. PWM_ENTIRE_CYCLE - PPR0.PWM_ACT_CYCLE), then PWM0 outputs 1.

The formula of PWM output period and duty-cycle is as follows.

T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0. PWM_ENTIRE_CYCLE + 1)

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE + 1 - PPR0.PWM_ACT_CYCLE)

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE

Duty-cycle = (low level time) / (1 period time)

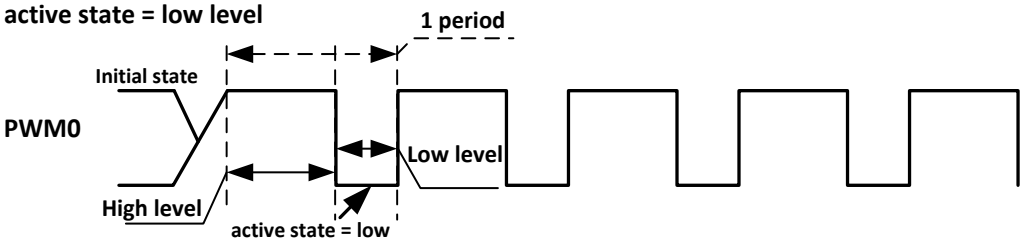

Figure 11- 55. Period and Duty-Cycle in PWM0 Low Level Active State

11.8.3.5.2. Phase

PCNTR count starts from 0 by default. Configure PWM_CNTSTART to realize the phase control of the output waveform.

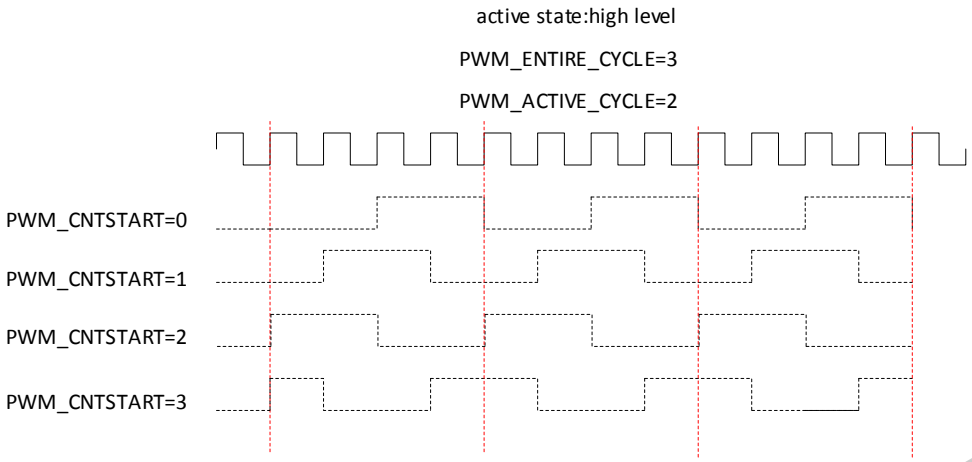

Figure 11- 56. Phase in PWM0 High Level Active State

11.8.3.6. Cache Loading, Cycle Mode, Pulse Mode and Active State

The PWM output supports cycle mode and pulse mode. The PWM in cycle mode outputs continuous waveform, PWM in pulse mode outputs several pulse waveform. Figure 11-57 shows the cache loading, cycle mode, pulse mode and active state for PWM0 channel of PWM01 pair.

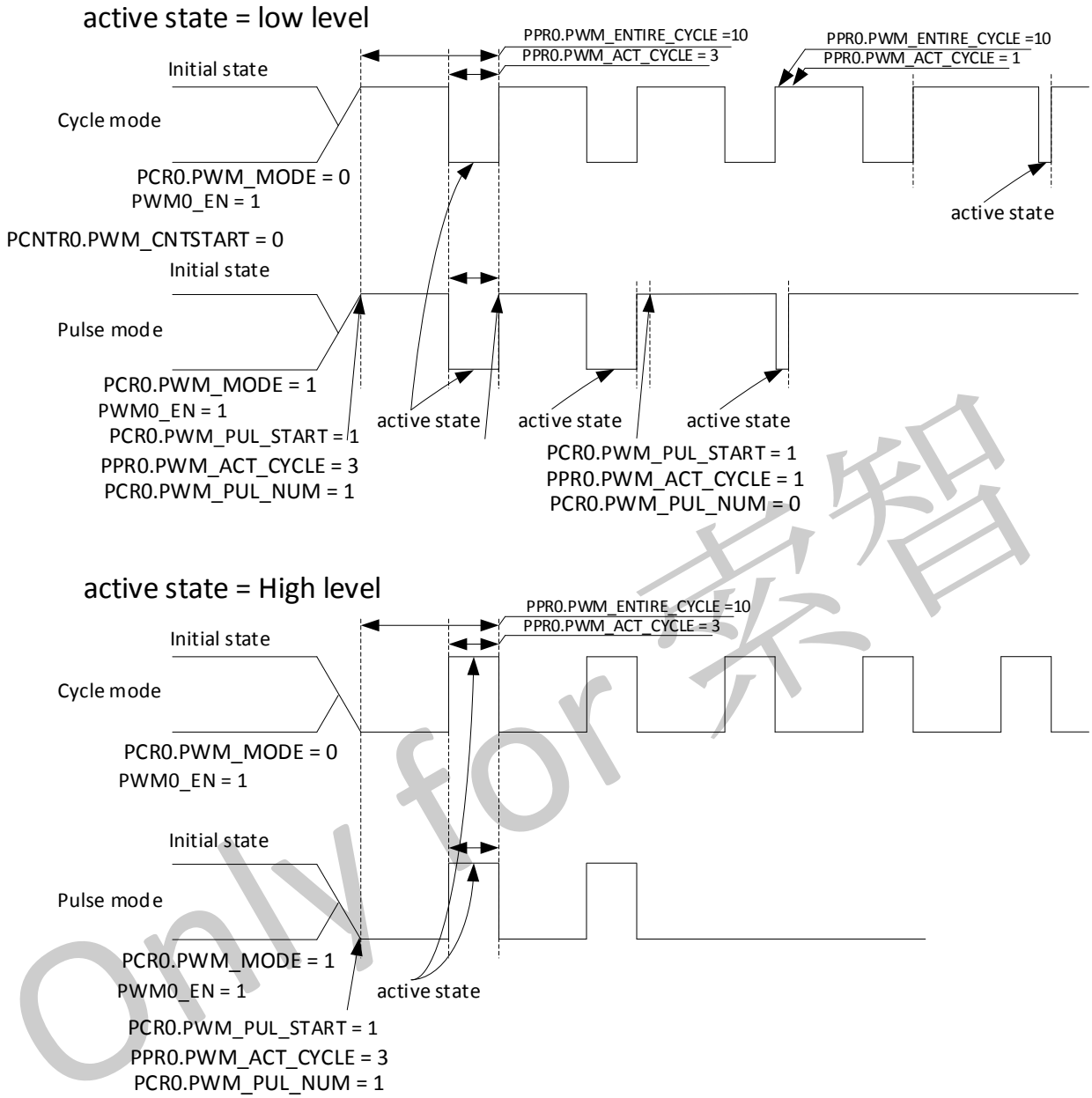

Figure 11- 57. Cache Loading, Cycle Mode, Pulse Mode and Active State for PWM0 Channel

The active state of PWM output waveform is configurable.

When PCR0.PWM_MODE is 0, PWM0 outputs cycle waveform.

When PCR0.PWM_MODE is 1, PWM0 outputs pulse waveform. In pulse mode, after PWM0 channel is enabled, the PCR0. PWM_PUL_START is sets to 1, after setting 1, PWM0 outputs PWM_PULNUM pulse waveform, the PCR0. PWM_PUL_START is cleared by hardware after output completed.

11.8.3.7. Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time. Figure 11-58 shows the complementary pair output of PWM01.

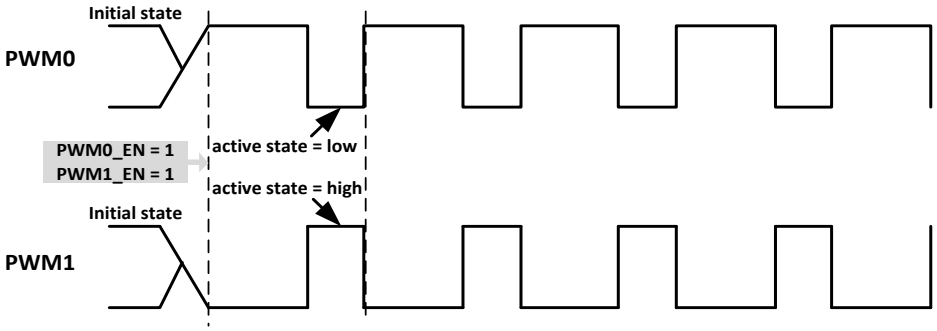

Figure 11- 58. PWM01 Complementary Pair Output

The complementary pair output need satisfy the following three conditions:

- PWM0 and PWM1 have the same frequency, duty-cycle, phase.
- PWM0 and PWM1 have opposite active state.
- Enable PWM0 and PWM1 at the same time.

11.8.3.8. Dead-time Generator

Every PWM pair has a programmable dead-time generator. When the dead-time function of PWM pair enabled, PWM01 pair outputs a pair of PWM waveforms that insert dead-time, PWM01 pair output waveform is decided by PWM0 timer logic module and DeadZone Generator01. Figure 11-59 shows the output waveform.

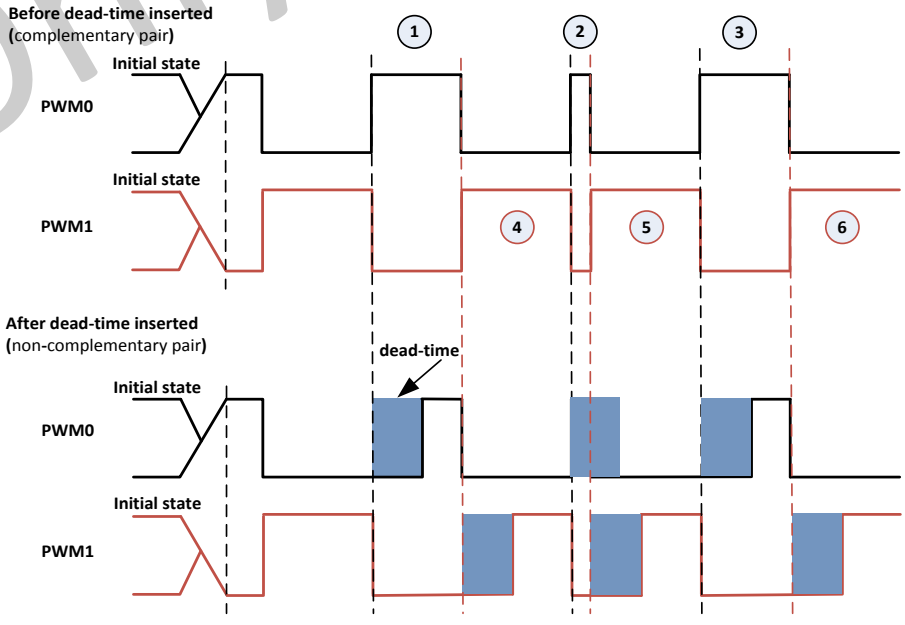

Figure 11- 59. PWM01 Pair Waveform Before/After Insert Dead-time

The PWM waveform before the insertion of dead-time indicates a complementary waveform pair of non-inserted dead-time in Dead Zone Generator 01.
The PWM waveform after the insertion of dead-time indicates a non-complementary PWM waveform pair inserted dead-time in a complementary waveform pair of Dead Zone Generator 01. The PWM waveform pair at last outputs to PWM0 pin and PWM1 pin.

For complementary pair of Dead Zone Generator 01, the principle of inserting dead-time is that to insert dead-time as soon as the rising edge came. If high level time for mark② in the above figure is less than dead-time, then dead-time will override the high level. The setting of dead-time need consider the period and duty-cycle of output waveform. Dead-time formula is defined as follows:
Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PDZINTV01

11.8.3.9. PWM Group Mode

Using PWM Group0 as an example. The same group of PWM channel is selected to work by PGR0.CS; the same PWM_ENTIRE_CYCLE, PWM_ACTIVE_CYCLE are set by the same clock configuration; the different PWM_CNTSTART can output PWM group signals with same duty-cycle, different phase.

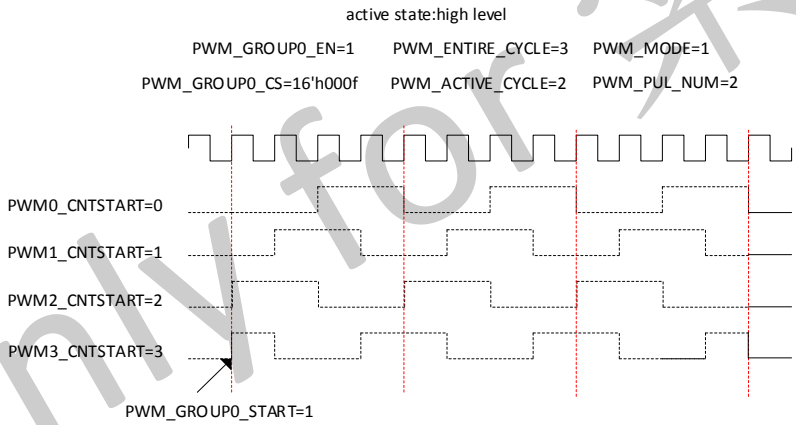

Figure 11- 60. Group 0~3 PWM Signal Output

11.8.3.10. Capture Input

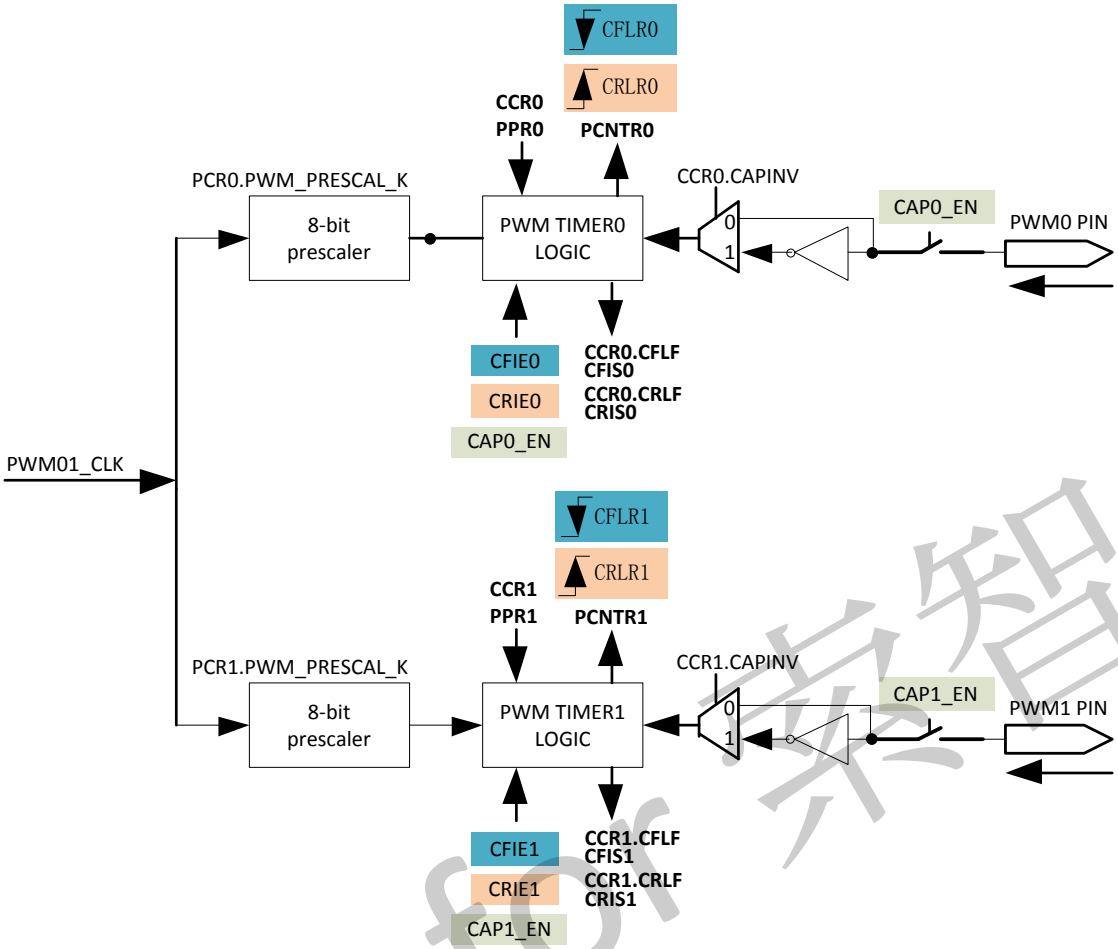

Figure 11- 61. PWM01 Capture Logic Module Diagram

Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture rising edge and falling edge of the external clock. Using PWM0 channel as an example, PWM0 channel has one **CFLR0** and one **CRLR0** for capturing up-counter value in falling edge and rising edge, respectively. You can calculate the period of external clock by **CFLR0** and **CRLR0**.

$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CRLR0

$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * CFLR0

$T_{period} = T_{high\text{-}level} + T_{low\text{-}level}$

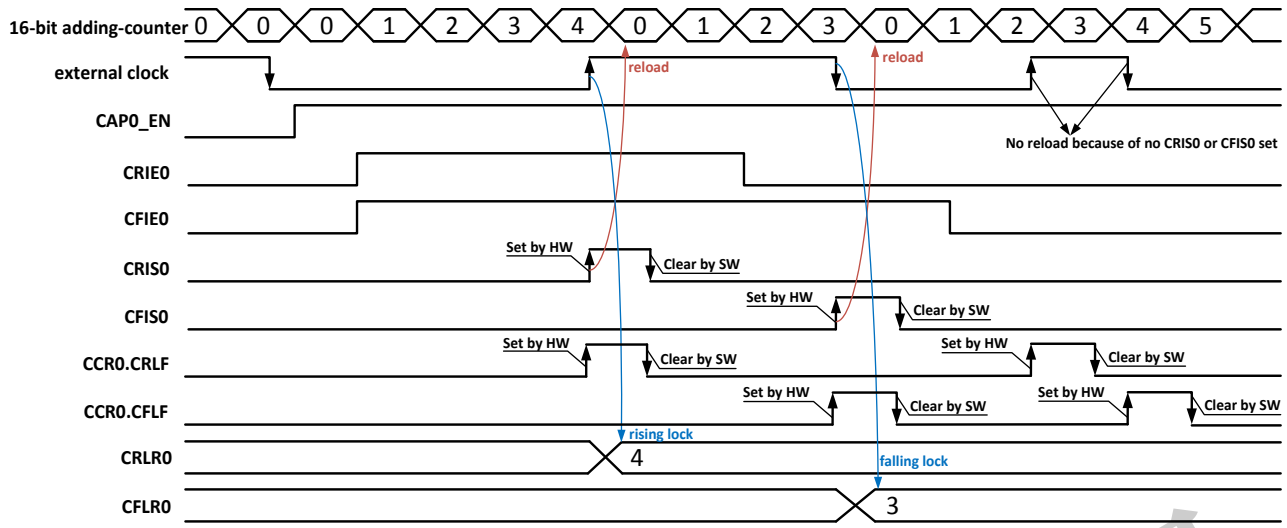

Figure 11- 62. PWM0 Channel Capture Timing

When the capture input function of PWM0 channel is enabled, the PCNTR of PWM0 channel starts to work.

When the timer logic module of PWM0 captures one rising edge, the current value of up-counter is locked to **CRLR0**, and **CCR0.CRLF** is set to 1. If **CRIE0** is 1, then **CRIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CRIE0** is 0, the timer logic module of PWM0 captures rising edge, **CRIS0** can not be set to 1, the up-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of **PCNTR** is locked to **CFLR0**, and **CCR0.CFLF** is set to 1 . If **CFIE0** is 1, then **CFIS0** is set to 1, PWM0 channel sends interrupt request, and the up-counter is loaded to 0 and continues to count. If **CFIE0** is 0, the timer logic module of PWM0 captures falling edge, **CFIS0** can not be set to 1, the up-counter is not loaded to 0.

11.8.3.11. Interrupt

PWM supports interrupt generation when PWM channel is configured to PWM output or capture input .

For PWM output function, when 1 cycle of PWM waveform is output in cycle mode, the PIS of the corresponding PWM channel is set to 1; when (PWM_PULNUM+1) cycle of PWM waveform is output in pulse mode, the PIS of the corresponding PWM channel is set to 1.

NOTE

The PIS bit is set to 1 automatically by hardware and cleared by software.

For capture input function, when the timer logic module of the capture channel0 captures rising edge, and **CRIE0** is 1, then **CRIS0** is set to 1; when the timer logic module of the capture channel0 captures falling edge, and **CFIE0** is 1, then **CFIS0** is set to 1.

11.8.4. Working Mode

The following working mode takes PWM01 as an example, other PWM pairs and PWM01 are consistent.

11.8.4.1. Clock Configuration

(1) PWM gating: When using PWM, write 1 to PCGR[PWMx_CLK_GATING].
(2) PWM clock source select: Set PCCR01[PWM01_CLK_SRC] to select OSC24M or APB1 clock.
(3) PWM clock divider: Set PCCR01[PWM01_CLK_DIV_M] to select different frequency division coefficient (1/2/4/8/16/32/64/128/256).
(4) PWM clock bypass: Set PCGR[PWM_CLK_SRC_BYPASS_TO_PWM] to 1, outputting the PWM clock after the secondary frequency division to the corresponding PWM output pin.
(5) PWM internal clock configuration: Set PCR[PWM_PRESCAL_K] to select any frequency division coefficient from 1 to 256.

11.8.4.2. PWM Configuration

(1) PWM mode: Set PCR[PWM_MODE] to select cycle mode or pulse mode, if pulse mode, PWM_PUL_NUM needs be configured.
(2) PWM valid level: Set PCR[PWM_ACT_STA] to select low level or high level.
(3) PWM duty-cycle: Configure PPR[PWM_ENTIRE_CYCLE] and PPR[PWM _ACT_CYCLE] after clock gating is opened.
(4) PWM starting phase: Configure PCNTR[PWM_COUNTER_START] after clock gating is opened and before PWM is enabled, read PCNTR[PWM_COUNTER_STATUS] to ensure whether the starting phase is configured successful.
(5) Enable PWM: Configure PER to select the corresponding PWM enable bit; when selecting pulse mode, PCR[PWM_PUL_START] needs be enabled.

11.8.4.3. Deadzone Control

(1) Deadzone initial value: Set PDZCR01[PDZINTV01].
(2) Deaszone enable: Set PDZCR01[PWM01_DZ_CN].

11.8.4.4. Capture

(1) Capture enable: Configure CER to enable the corresponding channel.
(2) Capture mode: Configure CCR[CRLF] and CCR[CFLF] to select rising edge capture or falling edge capture, configure CCR[CAPINV] to select whether the input signal does reverse processing.

11.8.5. Register List

Module Name	Base Address
PWM	0x0300A000

Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register
PCCR23	0x0024	PWM23 Clock Configuration Register
PCCR45	0x0028	PWM45 Clock Configuration Register
PCCR67	0x002C	PWM67 Clock Configuration Register
PCCR89	0x0030	PWM89 Clock Configuration Register
PCGR	0x0040	PWM Clock Gating Register
PDZCR01	0x0060	PWM01 Dead Zone Control Register
PDZCR23	0x0064	PWM23 Dead Zone Control Register
PDZCR45	0x0068	PWM45 Dead Zone Control Register
PDZCR67	0x006C	PWM67 Dead Zone Control Register
PDZCR89	0x0070	PWM89 Dead Zone Control Register
PER	0x0080	PWM Enable Register
PGR0	0x0090	PWM Group0 Register
PGR1	0x0094	PWM Group1 Register
CER	0x00C0	Capture Enable Register
PCR	0x0100+0x0000+N*0x0020(N= 0~9)	PWM Control Register
PPR	0x0100+0x0004+N*0x0020(N= 0~9)	PWM Period Register
PCNTR	0x0100+0x0008+N*0x0020(N= 0~9)	PWM Count Register
PPCNTR	0x0100+0x000C+N*0x0020(N= 0~9)	PWM Pulse Count Register
CCR	0x0100+0x0010+N*0x0020(N= 0~9)	Capture Control Register
CRLR	0x0100+0x0014+N*0x0020(N= 0~9)	Capture Rise Lock Register
CFLR	0x0100+0x0018+N*0x0020(N= 0~9)	Capture Fall Lock Register

11.8.6. Register Description

11.8.6.1. 0x0000 PWM IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0000			Register Name: PIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	PGIE1 PWM group 1 Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	PGIE0 PWM group 0 Interrupt Enable 0: Disable

			1: Enable
15:10	/	/	/
9	R/W	0x0	PCIE9 PWM Channel 9 Interrupt Enable 0: PWM channel 9 Interrupt Disable; 1: PWM channel 9 Interrupt Enable.
8	R/W	0x0	PCIE8 PWM Channel 8 Interrupt Enable 0: PWM channel 8 Interrupt Disable; 1: PWM channel 8 Interrupt Enable.
7	R/W	0x0	PCIE7 PWM Channel 7 Interrupt Enable 0: PWM channel 7 interrupt disable 1: PWM channel 7 interrupt enable
6	R/W	0x0	PCIE6 PWM Channel 6 Interrupt Enable 0: PWM channel 6 interrupt disable 1: PWM channel 6 interrupt enable
5	R/W	0x0	PCIE5 PWM Channel 5 Interrupt Enable 0: PWM channel 5 interrupt disable 1: PWM channel 5 interrupt enable
4	R/W	0x0	PCIE4 PWM Channel 4 Interrupt Enable 0: PWM channel 4 interrupt disable 1: PWM channel 4 interrupt enable
3	R/W	0x0	PCIE3 PWM Channel 3 Interrupt Enable 0: PWM channel 3 interrupt disable 1: PWM channel 3 interrupt enable
2	R/W	0x0	PCIE2 PWM Channel 2 Interrupt Enable 0: PWM channel 2 interrupt disable 1: PWM channel 2 interrupt enable
1	R/W	0x0	PCIE1 PWM Channel 1 Interrupt Enable 0: PWM channel 1 interrupt disable 1: PWM channel 1 interrupt enable
0	R/W	0x0	PCIE0 PWM Channel 0 Interrupt Enable 0: PWM channel 0 interrupt disable 1: PWM channel 0 interrupt enable

11.8.6.2. 0x0004 PWM IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0004			Register Name: PISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W1C	0x0	PGIS1 PWM Group 1 Interrupt Status
16	R/W1C	0x0	PGIS0 PWM Group 0 Interrupt Status
15:10	/	/	/
9	R/W1C	0x0	PIS9 PWM Channel 9 Interrupt Status When PWM channel 9 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 9 interrupt is not pending. Reads 1: PWM channel 9 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 9 interrupt status.
8	R/W1C	0x0	PIS8 PWM Channel 8 Interrupt Status When PWM channel 8 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 8 interrupt is not pending. Reads 1: PWM channel 8 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 8 interrupt status.
7	R/W1C	0x0	PIS7 PWM Channel 7 Interrupt Status When PWM channel 7 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. Reads 1: PWM channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6 PWM Channel 6 Interrupt Status When PWM channel 6 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. Reads 1: PWM channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5 PWM Channel 5 Interrupt Status When PWM channel 5 counter reaches Entire Cycle Value, this bit is set 1 by

			hardware. Writing 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. Reads 1: PWM channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4 PWM Channel 4 Interrupt Status When PWM channel 4 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. Reads 1: PWM channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3 PWM Channel 3 Interrupt Status When PWM channel 3 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. Reads 1: PWM channel 3 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2 PWM Channel 2 Interrupt Status When PWM channel 2 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending. Reads 1: PWM channel 2 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1 PWM Channel 1 Interrupt Status When PWM channel 1 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. Reads 1: PWM channel 1 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0 PWM Channel 0 Interrupt Status When PWM channel 0 counter reaches Entire Cycle Value, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. Reads 1: PWM channel 0 interrupt is pending. Writes 0: No effect. Writes 1: Clear PWM channel 0 interrupt status.

11.8.6.3. 0x0010 PWM Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset:0x0010			Register Name: CIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	CFIE9 If the bit is set 1, when capture channel 9 captures falling edge, it generates a capture channel 9 pending. 0: Capture channel 9 fall lock interrupt disable 1: Capture channel 9 fall lock interrupt enable
18	R/W	0x0	CRIE9 If the bit is set 1, when capture channel 9 captures rising edge, it generates a capture channel 9 pending. 0: Capture channel 9 rise lock interrupt disable 1: Capture channel 9 rise lock interrupt enable
17	R/W	0x0	CFIE8 If the bit is set 1, when capture channel 8 captures falling edge, it generates a capture channel 8 pending. 0: Capture channel 8 fall lock interrupt disable 1: Capture channel 8 fall lock interrupt enable
16	R/W	0x0	CRIE8 If the bit is set 1, when capture channel 8 captures rising edge, it generates a capture channel 8 pending. 0: Capture channel 8 rise lock interrupt disable 1: Capture channel 8 rise lock interrupt enable
15	R/W	0x0	CFIE7 If the bit is set 1, when capturing channel 7 captures falling edge, it generates a capturing channel 7 pending. 0: Capturing channel 7 fall lock interrupt disable 1: Capturing channel 7 fall lock interrupt enable
14	R/W	0x0	CRIE7 If the bit is set 1, when capturing channel 7 captures rising edge, it generates a capturing channel 7 pending. 0: Capturing channel 7 rise lock interrupt disable 1: Capturing channel 7 rise lock interrupt enable
13	R/W	0x0	CFIE6 If the bit is set 1, when capturing channel 6 captures falling edge, it generates a capturing channel 6 pending. 0: Capturing channel 6 fall lock interrupt disable 1: Capturing channel 6 fall lock interrupt enable
12	R/W	0x0	CRIE6 If the bit is set 1, when capturing channel 6 captures rising edge, it generates a capturing channel 6 pending.

			0: Capturing channel 6 rise lock interrupt disable 1: Capturing channel 6 rise lock interrupt enable
11	R/W	0x0	CFIE5 If the bit is set 1, when capturing channel 5 captures falling edge, it generates a capturing channel 5 pending. 0: Capturing channel 5 fall lock interrupt disable 1: Capturing channel 5 fall lock interrupt enable
10	R/W	0x0	CRIE5 If the bit is set 1, when capturing channel 5 captures rising edge, it generates a capturing channel 5 pending. 0: Capturing channel 5 rise lock interrupt disable 1: Capturing channel 5 rise lock interrupt enable
9	R/W	0x0	CFIE4 If the bit is set 1, when capturing channel 4 captures falling edge, it generates a capturing channel 4 pending. 0: Capture channel 4 fall lock interrupt disable 1: Capture channel 4 fall lock interrupt enable
8	R/W	0x0	CRIE4 If the bit is set 1, when capturing channel 4 captures rising edge, it generates a capturing channel 4 pending. 0: Capturing channel 4 rise lock interrupt disable 1: Capturing channel 4 rise lock interrupt enable
7	R/W	0x0	CFIE3 If the bit is set 1, when capturing channel 3 captures falling edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 fall lock interrupt disable 1: Capturing channel 3 fall lock interrupt enable
6	R/W	0x0	CRIE3 If the bit is set 1, when capturing channel 3 captures rising edge, it generates a capturing channel 3 pending. 0: Capturing channel 3 rise lock interrupt disable 1: Capturing channel 3 rise lock interrupt enable
5	R/W	0x0	CFIE2 If the bit is set 1, when capturing channel 2 captures falling edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 fall lock interrupt disable 1: Capturing channel 2 fall lock interrupt enable
4	R/W	0x0	CRIE2 If the bit is set 1, when capturing channel 2 captures rising edge, it generates a capturing channel 2 pending. 0: Capturing channel 2 rise lock interrupt disable 1: Capturing channel 2 rise lock interrupt enable
3	R/W	0x0	CFIE1 If the bit is set 1, when capturing channel 1 captures falling edge, it generates a capturing channel 1 pending.

			0: Capturing channel 1 fall lock interrupt disable 1: Capturing channel 1 fall lock interrupt enable
2	R/W	0x0	CRIE1 If the bit is set 1, when capturing channel 1 captures rising edge, it generates a capturing channel 1 pending. 0: Capturing channel 1 rise lock interrupt disable 1: Capturing channel 1 rise lock interrupt enable
1	R/W	0x0	CFIE0 If the bit is set 1, when capturing channel 0 captures falling edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 fall lock interrupt disable 1: Capturing channel 0 fall lock interrupt enable
0	R/W	0x0	CRIE0 If the bit is set 1, when capturing channel 0 captures rising edge, it generates a capturing channel 0 pending. 0: Capturing channel 0 rise lock interrupt disable 1: Capturing channel 0 rise lock interrupt enable

11.8.6.4. 0x0014 PWM Capture IRQ Status Register (Default Value: 0x0000_0000)

Offset:0x0014			Register Name: CISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W1C	0x0	CFIS9 Capture channel 9 falling lock interrupt status When capture channel 9 captures falling edge, if capture channel 9 fall lock interrupt (**CFIE9**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. Reads 1: Capture channel 9 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 9 interrupt status.
18	R/W1C	0x0	CRIS9 Capture channel 9 rising lock interrupt status When capture channel 9 captures rising edge, if capture channel 9 rise lock interrupt (**CRIE9**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 9 interrupt is not pending. Reads 1: Capture channel 9 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 9 interrupt status.
17	R/W1C	0x0	CFIS8 Capture channel 8 falling lock interrupt status When capture channel 8 captures falling edge, if capture channel 8 fall lock

			interrupt (**CFIE8**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. Reads 1: Capture channel 8 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 8 interrupt status.
16	R/W1C	0x0	CRIS8 Capture channel 8 rising lock interrupt status When capture channel 8 captures rising edge, if capture channel 8 rise lock interrupt (**CRIE8**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 8 interrupt is not pending. Reads 1: Capture channel 8 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 8 interrupt status.
15	R/W1C	0x0	CFIS7 Capturing channel 7 falling lock interrupt status. When capturing channel 7 captures falling edge, if capturing channel 7 fall lock interrupt (**CFIE7**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 7 interrupt is not pending. Reads 1: Capturing channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 7 interrupt status.
14	R/W1C	0x0	CRIS7 Capturing channel 7 rising lock interrupt status. When capturing channel 7 captures rising edge, if capturing channel 7 rise lock interrupt (**CRIE7**) is enabled, this bit is set 1 by hardware. Write 1 to clear this bit. Reads 0: Capturing channel 7 interrupt is not pending. Reads 1: Capturing channel 7 interrupt is pending. Writes 0: No effect. Writes 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6 Capturing channel 6 falling lock interrupt status. When capturing channel 6 captures falling edge, if capturing channel 6 fall lock interrupt (**CFIE6**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 6 interrupt is not pending. Reads 1: Capturing channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 6 interrupt status.
12	R/W1C	0x0	CRIS6 Capturing channel 6 rising lock interrupt status. When capturing channel 6 captures rising edge, if capturing channel 6 rise

			lock interrupt (**CRIE6**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 6 interrupt is not pending. Reads 1: Capturing channel 6 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 6 interrupt status.
11	R/W1C	0x0	CFIS5 Capturing channel 5 falling lock interrupt status. When capturing channel 5 captures falling edge, if capturing channel 5 fall lock interrupt (**CFIE5**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 5 interrupt is not pending. Reads 1: Capturing channel 5 interrupt is pending. Writes 0: No effect. Reads 1: Clear capturing channel 5 interrupt status.
10	R/W1C	0x0	CRIS5 Capturing channel 5 rising lock interrupt status. When capturing channel 5 captures rising edge, if capturing channel 5 rise lock interrupt (**CRIE5**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 5 interrupt is not pending. Reads 1: Capturing channel 5 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 5 interrupt status.
9	R/W1C	0x0	CFIS4 Capturing channel 4 falling lock interrupt status. When capturing channel 4 captures falling edge, if capturing channel 4 fall lock interrupt (**CFIE4**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capturing channel 4 interrupt is not pending. Reads 1: Capturing channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 4 interrupt status.
8	R/W1C	0x0	CRIS4 Capturing channel 4 rising lock interrupt status. When capturing channel 4 captures rising edge, if capturing channel 4 rise lock interrupt (**CRIE4**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capturing channel 4 interrupt is not pending. Reads 1: Capturing channel 4 interrupt is pending. Writes 0: No effect. Writes 1: Clear capturing channel 4 interrupt status.
7	R/W1C	0x0	CFIS3 Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock

			interrupt (**CFIE3**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3 Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (**CRIE3**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. Reads 1: Capture channel 3 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2 Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (**CFIE2**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2 Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (**CRIE2**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. Reads 1: Capture channel 2 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1 Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (**CFIE1**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1 Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock

			interrupt (**CRIE1**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. Reads 1: Capture channel 1 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0 Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (**CFIE0**) is enabled, this bit is set 1 by hardware.Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0 Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (**CRIE0**) is enabled, this bit is set 1 by hardware. Writing 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. Reads 1: Capture channel 0 interrupt is pending. Writes 0: no effect. Writes 1: Clear capture channel 0 interrupt status.

11.8.6.5. 0x0020 PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0020			**Register Name: PCCR01**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM01_CLK_SRC Select PWM01 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM01_CLK_DIV_M PWM01 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32

			0110: /64 0111: /128 1000: /256 others: Reserved

11.8.6.6. 0x0024 PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0024			Register Name: PCCR23
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM23_CLK_SRC_SEL Select PWM23 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM23_CLK_DIV_M PWM23 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

11.8.6.7. 0x0028 PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0028			Register Name: PCCR45
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM45_CLK_SRC_SEL Select PWM45 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM45_CLK_DIV_M PWM45 Clock Divide M 0000: /1

			0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

11.8.6.8. 0x002C PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x002C			Register Name: PCCR67
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM67_CLK_SRC_SEL Select PWM67 Clock Source 00: OSC24M 01: APB1 Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM67_CLK_DIV_M PWM67 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

11.8.6.9. 0x0030 PWM89 Clock Configuration Register (Default Value: 0x0000_0000)

Offset:0x0030			Register Name: PCCR89
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM89_CLK_SRC_SEL Select PWM89 Clock Source 00: OSC24M 01: APB1

			Others: Reserved
6:4	/	/	/
3:0	R/W	0x0	PWM89_CLK_DIV_M PWM89 Clock Divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: Reserved

11.8.6.10. 0x0040 PWM Clock Gating Register (Default Value: 0x0000_0000)

Offset:0x0040			Register Name: PCGR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25	R/W	0x0	PWM9_CLK_BYPASS Bypass clock source(after pre-scale) to PWM9 output 0: not bypass 1: bypass
24	R/W	0x0	PWM8_CLK_BYPASS Bypass clock source(after pre-scale) to PWM8 output 0: not bypass 1: bypass
23	R/W	0x0	PWM7_CLK_BYPASS Bypass clock source(after pre-scale) to PWM7 output 0: not bypass 1: bypass
22	R/W	0x0	PWM6_CLK_BYPASS Bypass clock source(after pre-scale) to PWM6 output 0: not bypass 1: bypass
21	R/W	0x0	PWM5_CLK_BYPASS Bypass clock source(after pre-scale) to PWM5 output 0: not bypass 1: bypass
20	R/W	0x0	PWM4_CLK_BYPASS Bypass clock source(after pre-scale) to PWM4 output 0: not bypass 1: bypass

19	R/W	0x0	PWM3_CLK_BYPASS Bypass clock source(after pre-scale) to PWM3 output 0: not bypass 1: bypass
18	R/W	0x0	PWM2_CLK_BYPASS Bypass clock source(after pre-scale) to PWM2 output 0: not bypass 1: bypass
17	R/W	0x0	PWM1_CLK_BYPASS Bypass clock source(after pre-scale) to PWM1 output 0: not bypass 1: bypass
16	R/W	0x0	PWM0_CLK_BYPASS Bypass clock source(after pre-scale) to PWM0 output 0: not bypass 1: bypass
15:10	/	/	/
9	R/W	0x0	PWM9_CLK_GATING Gating clock for PWM9 0: Mask 1: Pass
8	R/W	0x0	PWM8_CLK_GATING Gating clock for PWM8 0: Mask 1: Pass
7	R/W	0x0	PWM7_CLK_GATING Gating clock for PWM7 0: Mask 1: Pass
6	R/W	0x0	PWM6_CLK_GATING Gating clock for PWM6 0: Mask 1: Pass
5	R/W	0x0	PWM5_CLK_GATING Gating clock for PWM5 0: Mask 1: Pass
4	R/W	0x0	PWM4_CLK_GATING Gating clock for PWM4 0: Mask 1: Pass
3	R/W	0x0	PWM3_CLK_GATING Gating clock for PWM3 0: Mask 1: Pass

2	R/W	0x0	PWM2_CLK_GATING Gating clock for PWM2 0: Mask 1: Pass
1	R/W	0x0	PWM1_CLK_GATING Gating clock for PWM1 0: Mask 1: Pass
0	R/W	0x0	PWM0_CLK_GATING Gating clock for PWM0 0: Mask 1: Pass

11.8.6.11. 0x0060 PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0060			Register Name: PDZCR01
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01 PWM01 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN PWM01 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

11.8.6.12. 0x0064 PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0064			Register Name: PDZCR23
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV PWM23 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN PWM23 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

11.8.6.13. 0x0068 PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0068			Register Name: PDZCR45
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM45_DZ_INTV PWM45 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN PWM45 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

11.8.6.14. 0x006C PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x006C			Register Name: PDZCR67
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM67_DZ_INTV PWM67 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN PWM67 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

11.8.6.15. 0x0070 PWM89 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset:0x0070			Register Name: PDZCR89
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM89_DZ_INTV PWM89 Dead Zone interval value
7:1	/	/	/
0	R/W	0x0	PWM89_DZ_EN PWM89 Dead Zone enable 0: Dead Zone disable 1: Dead Zone enable

11.8.6.16. 0x0080 PWM Enable Register (Default Value: 0x0000_0000)

Offset:0x0080			Register Name: PER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	PWM9_EN 0: PWM disable 1: PWM enable
8	R/W	0x0	PWM8_EN 0: PWM disable 1: PWM enable
7	R/W	0x0	PWM7_EN 0: PWM disable 1: PWM enable
6	R/W	0x0	PWM6_EN 0: PWM disable 1: PWM enable
5	R/W	0x0	PWM5_EN 0: PWM disable 1: PWM enable
4	R/W	0x0	PWM4_EN 0: PWM disable 1: PWM enable
3	R/W	0x0	PWM3_EN 0: PWM disable 1: PWM enable
2	R/W	0x0	PWM2_EN 0: PWM disable 1: PWM enable
1	R/W	0x0	PWM1_EN 0: PWM disable 1: PWM enable
0	R/W	0x0	PWM0_EN 0: PWM disable 1: PWM enable

11.8.6.17. 0x0090 PWM Group0 Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: PGR0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	PWMG0_START PWM channels selected in PWMG0_CS start to output PWM waveform at

			the same time.
16	R/W	0x0	PWMG0_EN PWM Group0 Enable
15:0	R/W	0x0	PWMG0_CS If bit[i] is set, PWM i is selected as one channel of PWM Group0

11.8.6.18. 0x0094 PWM Group1 Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: PGR1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	PWMG1_START PWM channels selected in PWMG1_CS start to output PWM waveform at the same time.
16	R/W	0x0	PWMG1_EN PWM Group1 Enable
15:0	R/W	0x0	PWMG1_CS If bit[i] is set, PWM i is selected as one channel of PWM Group1

11.8.6.19. 0x00C0 Capture Enable Register (Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: CER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	CAP8_EN When enable capture function, the 16-bit up-counter starts working and capture channel8 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
7	R/W	0x0	CAP7_EN When enable capture function, the 16-bit up-counter starts working and capture channel7 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
6	R/W	0x0	CAP6_EN When enable capture function, the 16-bit up-counter starts working and capture channel6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
5	R/W	0x0	CAP5_EN When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge.

			0: Capture disable 1: Capture enable
4	R/W	0x0	CAP4_EN When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
3	R/W	0x0	CAP3_EN When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
2	R/W	0x0	CAP2_EN When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
1	R/W	0x0	CAP1_EN When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable
0	R/W	0x0	CAP0_EN When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable

11.8.6.20. 0x0100 + N*0x20 PWM Control Register (Default Value: 0x0000_0000)

Offset:0x0100+0x0+N*0x20(N=0~9)			Register Name: PCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_PUL_NUM In pulse mode, PWM output pulse for PWM_CYCLE_NUM+1 times and then stop.
15:12	/	/	/
11	R	0x0	PWM_PERIOD_RDY PWM Period Register Ready 0: PWM period register is ready to write 1: PWM period register is busy
10	R/W1S	0x0	PWM_PUL_START PWM Pulse Output Start 0: No effect 1: Output pulse for PWM_CYCLE_NUM+1.

			After finishing configuration for outputting pulse, set this bit once and then PWM would output waveform. After the waveform is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE PWM Output Mode Select 0: Cycle mode 1: Pulse mode
8	R/W	0x0	PWM_ACT_STA PWM Active State 0: Low Level 1: High Level
7:0	R/W	0x0	PWM_PRESCAL_K PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 ..... K = 255, actual pre-scale: 256

11.8.6.21. 0x0104 + N*0x20 PWM Period Register (Default Value: 0x0000_0000)

Offset:0x0100+0x04+N*0x20(N=0~9)			Register Name: PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_ENTIRE_CYCLE Number of the entire cycles in the PWM clock. 0: 1 cycle 1: 2 cycles … N: N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK.
15:0	R/W	0x0	PWM_ACT_CYCLE Number of the active cycles in the PWM clock. 0: 0 cycle 1: 1 cycle … N: N cycles

11.8.6.22. 0x0108 + N*0x20 PWM Counter Register (Default Value: 0x0000_0000)

Offset:0x0100+0x08+N*0x20(N=0~9)			Register Name: PCNTR
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0x0	PWM_COUNTER_START PWM counter value is set for phase control.
15:0	R	0x0	PWM_COUNTER_STATUS On PWM output or capture input, reading this register could get the current value of the PWM 16bit up-counter.

11.8.6.23. 0x010C + N*0x20 PWM Pulse Counter Register (Default Value: 0x0000_0000)

Offset:0x0100+0x0C+N*0x20(N=0~9)			Register Name: PPCNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	PWM_PUL_COUNTER_STATUS On PWM output , reading this register could get the current value of the PWM pulse counter.

11.8.6.24. 0x0110 + N*0x20 PWM Capture Control Register (Default Value: 0x0000_0000)

Offset:0x0100+0x10+N*0x20(N=0~9)			Register Name: CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W1C	0x0	CRLF When capture channel captures rising edge, the 16-bit up-counter’s current value is latched to CRLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
3	R/W1C	0x0	CFLF When capture channel captures falling edge, the 16-bit up-counter’s current value is latched to CFLR and then this bit is set 1 by hardware. Write 1 to clear this bit.
2	R/W	0x0	CRTE Rising edge capture trigger enable
1	R/W	0x0	CFTE Falling edge capture trigger enable
0	R/W	0x0	CAPINV Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: not inverse 1: inverse

11.8.6.25. 0x0114 + N*0x20 PWM Capture Rise Lock Register (Default Value: 0x0000_0000)

Offset:0x0100+0x14+N*0x20(N=0~9)	Register Name: CRLR

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	When capture channel captures rising edge, the 16-bit up-counter's current value is latched to this register.

11.8.6.26. 0x0118 + N*0x20 PWM Capture Fall Lock Register (Default Value: 0x0000_0000)

Offset:0x0100+0x18+N*0x20(N=0~9)			Register Name: CFLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	CFLR When the capturing channel captures the falling edge, the current value of the 16-bit up-counter is latched to the register.

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Chapter 12 Security System

12.1. Crypto Engine

12.1.1. Overview

The Crypto Engine(CE) module is one encryption/decryption algorithm accelerator. It supports kinds of symmetric, asymmetric, Hash, and RNG algorithms. The software interface is simple for configuration, only setting interrupt control, task description address and load tag. Algorithm control information is written in memory by task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels, and has an internal DMA controller to transfer data between CE and memory.

The CE has the following features:

- Symmetrical algorithm: AES, DES, 3DES, XTS
  - 128-, 192-, 256-bit key size for AES
  - ECB, CBC, CTR, CTS, OFB, CFB, CBC-MAC modes for AES
  - AES-CFB mode support CFB1, CFB8, CFB64, CFB128
  - AES-CTR supports CTR16, CTR32, CTR64, CTR128
  - ECB, CBC, CTR, CBC-MAC modes for DES/3DES
  - DES-CTR mode supports CTR16, CTR32, CTR64
  - 256-bit, 512-bit key for XTS
- Hash algorithm: MD5, SHA1, SHA224, SHA256, SHA384, SHA512, HMAC-SHA1, HMAC-SHA256
  - MD5, SHA, HMAC are padded using hardware, if not last package, input should aligned with computation block, namely 512bits or 1024bits
- Asymmetrical algorithm: RSA512/1024/2048/4096-bit, ECC160/224/256/384/521-bit
- 160-bit hardware PRNG with 175-bit seed. Output aligns with 5 words
- 256-bit hardware TRNG. Output aligns with 8 words
- Support task chain mode for each request. Task or task chain are executed at request order
- Symmetric, asymmetric, HASH ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time
- 8 scatter group(sg) are supported for both input and output data. sg size is input/output word number. DMA reads and write at word aligned
- DMA has multiple channel, each channel corresponds to one suit of algorithms

12.1.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

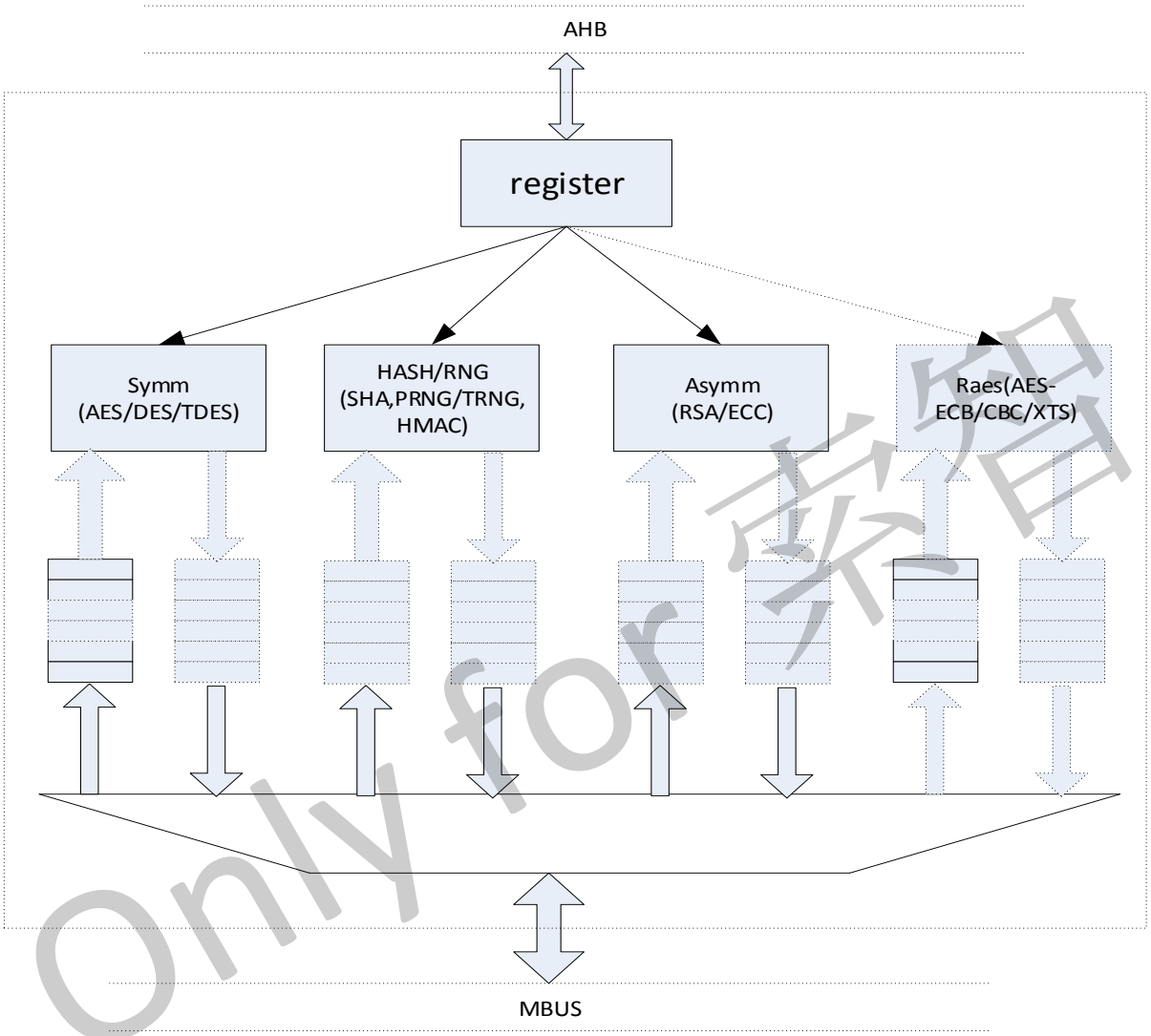

Figure 12- 1. CE Block Diagram

12.1.3. Operations and Functional Descriptions

12.1.3.1. Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

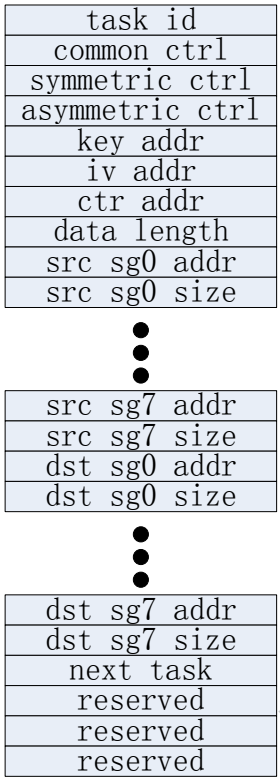

Figure 12- 2. Task Chaining

Task chaining id supports 0~3.

The key addr field is address for each algorithm's key, and for HASH's total length address when last package, also for extension feature micro codes address. When indicate HASH's total length address, it must be 64-bit data length with 64-bit address align.

The iv addr field is address for IV or modulus, or tweak value address for XTS.

The ctr addr is address for next block's IV, and for HMAC K1 address.

The src/dst sgX addr field indicates 32-bit address for source and destination data.

The src/dst sgX size field indicates size for each sg respectively.

The next task field should be set to 0 when no next task, else set to next task's descriptor.

12.1.3.2. Task Descriptor Queue Common Control

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	Interrupt enable for current task 0: disable interrupt 1: enable interrupt
30:25	/	/	/
24:17	R/W	0	cbc_mac_len the outcome bit length of CBC-MAC when in CBC-MAC mode.
16	R/W	0x0	IV mode IV mode for SHA1/SHA224/SHA256/SHA384/SHA512/MD5 or constants 0: use initial constants defined in FIPS-180

			1: use input iv
15	R/W	0x0	Last HMAC plaintext 0: not the last HMAC plaintext package. Padding is not required. 1: the last HMAC plaintext package.Padding is required
14:9	/	/	/
8	R/W	0x0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0x0	Algorithm Type 0x0: AES 0x1: DES 0x2: Triple DES (3DES) 0x10: MD5 0x11: SHA-1 0x12: SHA-224 0x13: SHA-256 0x14: SHA-384 0x15: SHA-512 0x16: HMAC-SHA1 0x17: HMAC-SHA256 0x1C: TRNG 0x1D: PRNG 0x20: RSA 0x21: ECC 0x30: RAES Others: Reserved

12.1.3.3. Task Descriptor Queue Symmetric Control

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	KEY_SELECT key select for AES 0000: Select input CE_KEYx (Normal Mode) 0001: Select {SSK} 0010: Select {HUK} 0011: Select {RSSK} 0100-0111: Reserved 1000-1111: Select internal Key n (n from 0 to 7)
19:18	R/W	0x0	CFB_WIDTH For AES-CFB width 00: CFB1

			01: CFB8 10: CFB64 11: CFB128
17	R/W	0x0	PRNG_LD Load new 15bits key into lfsr for PRNG
16	R/W	0x0	AES CTS last package flag When setting to '1', it means this is the last package for AES-CTS mode(the size of the last package >128bit).
15:14	/	/	/
13	R/W	0x0	xts_last 0: not last block for XTS 1: last block for XTS
12	R/W	0x0	xts_first 0: not first block for XTS 1: first block for XTS
11:8	R/W	0x0	Operation Mode for Symmetric AES/DES/3DES/RAES Modes DES/3DES only supports ECB/CBC/CTR. RAES only supports ECB/CBC/XTS. 0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: CipherText Stealing (CTS) mode 0100: Output feedback (OFB)mode 0101: Cipher feedback (CFB)mode 0110: CBC-MAC mode 1001: XTS mode Other: Reserved
7:4	/	/	/
3:2	R/W	0x0	CTR WIDTH Counter width for CTR mode 00: 16-bit Counter 01: 32-bit Counter 10: 64-bit Counter 11: 128-bit Counter
1:0	R/W	0x0	AES KEY SIZE 00: 128-bit 01: 192-bit 10: 256-bit 11: Reserved

12.1.3.4. Task Descriptor Queue Asymmetric Control

Bit	Read/Write	Default/Hex	Description
31:21	/	/	/

20:16	R/W	0	PKC algorithm mode For modular computation: 00000: modular exponent(RSA) 00001: modular add 00010: modular minus 00011: modular multiplication others: reserved For ECC: 00000: point add 00001: point double 00010: point multiplication 00011: point verification 00100: encryption 00101: decryption 00110: sign 00111: sign verify others: reserved
15:8	/	/	/
7:0	R/W	0	Asymmetric algorithms operation width field It indicates how much width this request apply, as words.

12.1.3.5. Task Request

Basically, there are 4 steps for one task handling from software.

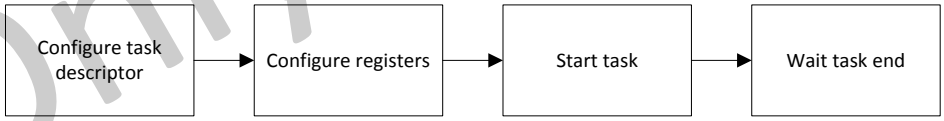

Figure 12- 3. Task Request Process

Step1: Software should configure task descriptor in memory, including all fields in descriptor. Channel id corresponds to one channel in CE. According to algorithm type, software should set the fields in common control, symmetric control, asymmetric control, then provide key/iv/ctr address and the data length of this task. Source and destination sg address and size are set based on upper application. If there is another task concatenating after this task, then set its descriptor address at next descriptor field.

Step 2: Software should set registers, including task descriptor address, interrupt control.

Step 3: Software reads load register to ensure that the bit0 is zero, then starts request by pulling up the bit0 of the load register.

Step 4: Wait task end.

12.1.3.6. Data Length Setting

Data length field in task descriptor has different meaning for different algorithms.
For HASH algorithm, data length field indicates valid source data bit number, for others indicates source data byte number. The data length of HASH should be 512/1024-bit aligned if current request is not the last data block, because of hardware padding.
For PRNG, data length should be 5 words aligned.
For TRNG, data length should be 8 words aligned.
Data size in source and destination sg is as words, whose value should corresponds with data length field, or else CE will report error and stop execution.

12.1.3.7. Task Parallel

Algorithms are divided into 3 types: symmetric, HASH/RNG, asymmetric. Each type has a task queue with 8 elements for requests. Tasks in each queue are handled in sequence. Among these 3 types, task request and complete time are not sure. If one type uses the outcome of another type, software should make sure that start one type after another type is finished.

CE supports 4 channels in each world, and 3 suits algorithm type which can run in parallel. When software issues request, it first checks if load bit is low, which means software can request. If load bit is high, which means last request is not registered by CE, software should wait until load bit is low. If software makes several requests with the same type, these tasks will be executed in request sequence. If software makes several requests with different types, these tasks will be executed in parallel. Because parallel tasks would finish out of order, software should make different type request with different channel id, which results in generating different interrupt status bit.

12.1.3.8. PKC Microcode

PKC module supports RSA, ECC asymmetric algorithms in the form of microcode. It implements basic modular add, minus, multiplication, point add, point double, and logic computing, etc. Complete RSA/ECC encryption, decryption, sign, verify are implemented with these microcode.

Asymmetric algorithms RSA/ECC are implemented as microcode in PKC module. Asymmetric encryption, decryption, sign, verify operations are composed with certain fixed microcode with hardware.

12.1.3.9. PKC Configuration

Before starting PKC, task description must be configured. Parameters to PKC are assigned to source sg, outcome is put to destination sg.
For RSA, parameters should be at the order of key, modulus, plaintext.
For ECC point add P2 = P0 + P1, parameters should be at the order of p, P0x, P0y, P1x, P1y. Output is at the order of P2x, P2y.
For ECC point double P2 = 2*P0, parameters should be at the order of p, a, P0x, P0y. Output is at the order of P2x, P2y.

For ECC point multiplication P2 = k*P0, parameters should be at the order of p, k, a, P0x, P0y. Output is at the order of P2x, P2y.
For ECC point verification, parameters should be at the order of p, a, P0x, P0y, b. Output is 1 or 0.
For ECC encryption, parameters should be at the order of random k, p, a, Gx, Gy, Qx, Qy, m. Output is at the order of Rx, Ry, c.
For ECC decryption, parameters should be at the order of random k, p, a, Rx, Ry, c. Output is m.
For ECC signature, parameters should be at the order of random k, p, a, Gx, Gy, n, d, e. Output is at the order of r, s.
For ECC signature verification, parameters should be at the order of n, s, e, r, p, a, Gx, Gy, Qx, Qy, n, r. Output is 1 or 0.

12.1.3.10. Error Check

CE module includes error detection for task configuration, data computing error, and authentication invalid. When algorithm type in task description is read into module, CE will check if this type is supported through checking algorithm type field in common control. If type value is out of scope, CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting task descriptor, input size and output size configuration will be checked to avoid size error. If size configuration is wrong, CE will issue interrupt signal and set error state.

12.1.3.11. Clock Requirement

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	24MHz ~ 200MHz
m_clk	MBUS clk	24MHz ~ 400MHz
ce_clk	CE work clock	24MHz ~ 300MHz

12.1.4. Register List

Module Name	Base Address
CE_NS	0x01904000
CE_S	0x01904800

Register Name	Offset	Description
CE_TDA	0x0000	Task Descriptor Address
CE_ICR	0x0008	Interrupt Control Register
CE_ISR	0x000C	Interrupt Status Register
CE_TLR	0x0010	Task Load Register
CE_TSR	0x0014	Task Status Register
CE_ESR	0x0018	Error Status Register
CE_SCSA	0x0024	Symmetric Algorithm DMA Current Source Address
CE_SCDA	0x0028	Symmetric Algorithm DMA Current Destination Address
CE_HCSA	0x0034	HASH Algorithm DMA Current Source Address

CE_HCDA	0x0038	HASH Algorithm DMA Current Destination Address
CE_ACSA	0x0044	Asymmetric Algorithm DMA Current Source Address
CE_ACDA	0x0048	Asymmetric Algorithm DMA Current Destination Address
CE_XCSA	0x0054	XTS Algorithm DMA Current Source Address
CE_XCDA	0x0058	XTS Algorithm DMA Current Destination Address

12.1.5. Register Description

12.1.5.1. 0x0000 CE Task Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Task Descriptor Address

12.1.5.2. 0x0008 CE Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	Task Channel3~0 Interrupt Enable 0: Disable 1: Enable

12.1.5.3. 0x000C CE Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W1C	0x0	Task Channel3~0 End Pending 0: Not finished 1: Finished It indicates if task has been completed . Write '1' to clear it.

12.1.5.4. 0x0010 CE Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:8	R/W	0x0	Algorithm type, the same with type field in description common control.

7:1	/	/	/
0	R/W	0x0	Task Load When setting, CE can load the descriptor of task if task FIFO is not full.

12.1.5.5. 0x0014 CE Task Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R	0x0	indicate which channel in run for XTS 00: task channel0 01: task channel1 10: task channel2 11: task channel3
23:18	/	/	/
17:16	R	0x0	indicate which channel in run for asymmetric 00: task channel0 01: task channel1 10: task channel2 11: task channel3
15:10	/	/	/
9:8	R	0x0	indicate which channel in run for digest 00: task channel0 01: task channel1 10: task channel2 11: task channel3
7:2	/	/	/
1:0	R	0x0	indicate which channel in run for symmetric 00: task channel0 01: task channel1 10: task channel2 11: task channel3

12.1.5.6. 0x0018 CE Error Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W1C	0x0	Task channel 3 error type. (the same for other channels) Bit 24: algorithm not support Bit 25: data length error Bit 26: keysram access error. Write '1' to clear. Bit 29: address invalid

			other: reserved
23:16	R/W1C	0x0	Task channel 2 error type. Bit 16: algorithm not support Bit 17: data length error Bit 18: keysram access error. Write '1' to clear. Bit 21: address invalid other: reserved
15:8	R/W1C	0x0	Task channel 1 error type. Bit 8: algorithm not support Bit 9: data length error Bit 10: keysram access error. Write '1' to clear. Bit 13: address invalid other: reserved
7:0	R/W1C	0x0	Task channel 0 error type. Bit 0: algorithm not support Bit 1: data length error Bit 2: keysram access error. Write '1' to clear. Bit 5: address invalid other: reserved

12.1.5.7. 0x0024 CE Symmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_SCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current source address read by DMA.

12.1.5.8. 0x0028 CE Symmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_SCDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	Symmetric algorithm current destination address written by DMA.

12.1.5.9. 0x0034 CE HASH Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CE_HCSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HASH algorithm current source address read by DMA.

12.1.5.10. 0x0038 CE HASH Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: CE_HCDA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	HASH algorithm current destination address written by DMA.

12.1.5.11. 0x0044 CE Asymmetric Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CE_ACSA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	Asymmetric algorithm current source address read by DMA.

12.1.5.12. 0x0048 CE Asymmetric Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CE_ACDA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	Asymmetric algorithm current destination address written by DMA.

12.1.5.13. 0x0054 CE XTS Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: CE_XCSA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	XTS algorithm current source address read by DMA.

12.1.5.14. 0x0058 CE XTS Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: CE_XCDA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	XTS algorithm current destination address written by DMA.

12.2. Security ID

The Security ID(SID) is 1Kbit(0x0000~0x007F) electrical efuse for saving key, which includes chip ID, thermal sensor, etc.

The SID module has the following features:

- A fuse only can program one time
- Supports a SRAM to backup fuse information

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Chapter 13 Carrier, Storage and Baking Information

13.1. Carrier

13.1.1. V833 Matrix Tray Information

Table 13-1 shows the V833 matrix tray carrier information.

Table 13- 1. V833 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315mm x 136mm x 7.62mm	168 Qty/Tray
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm	Surface impedance:$10^9\Omega$ Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm	
Inner Box	White	396mm x 196mm x 96mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420mm x 410mm x 320mm	6 Inner box/Carton

Table 13-2 shows the V833 packing quantity.

Table 13- 2. V833 Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V833	12 x 12	168	10	1680	6	10080

Figure 13-1 shows tray dimension drawing of the V833.

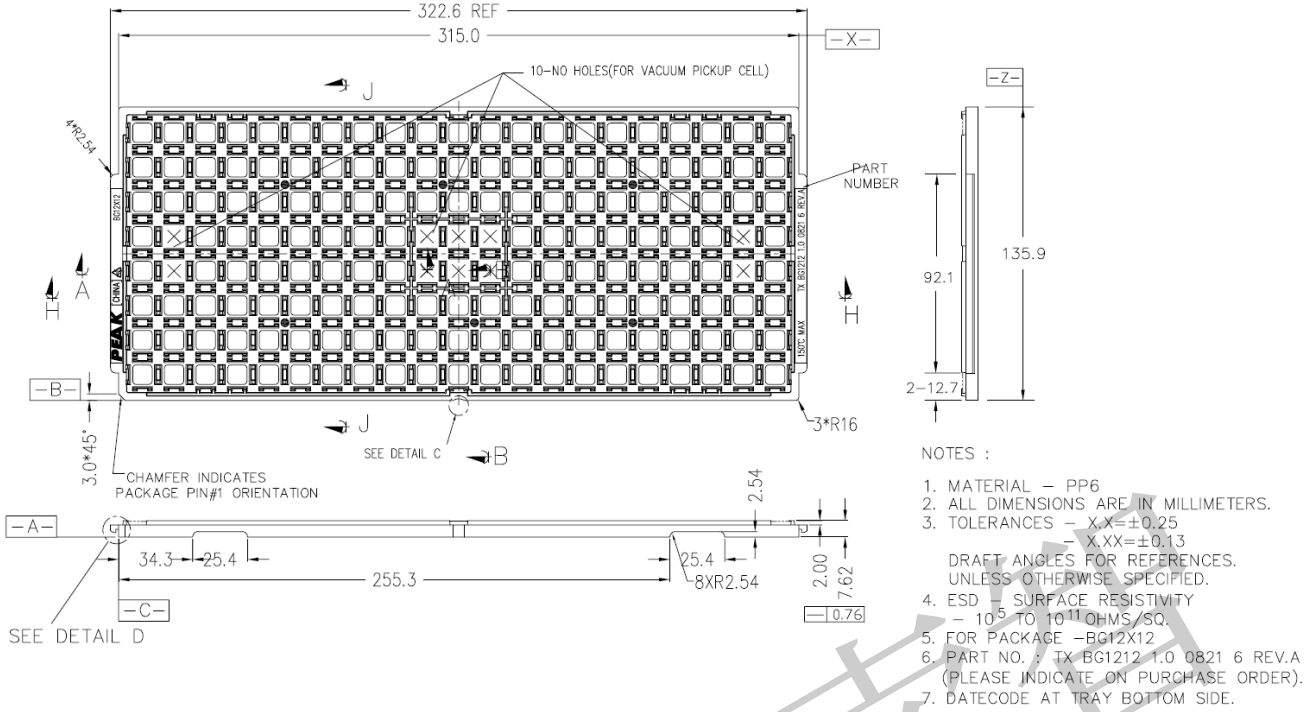


Figure 13- 1. V833 Tray Dimension

13.1.2. V831 Matrix Tray Information

Table 13- 3. V831 Matrix Tray Information

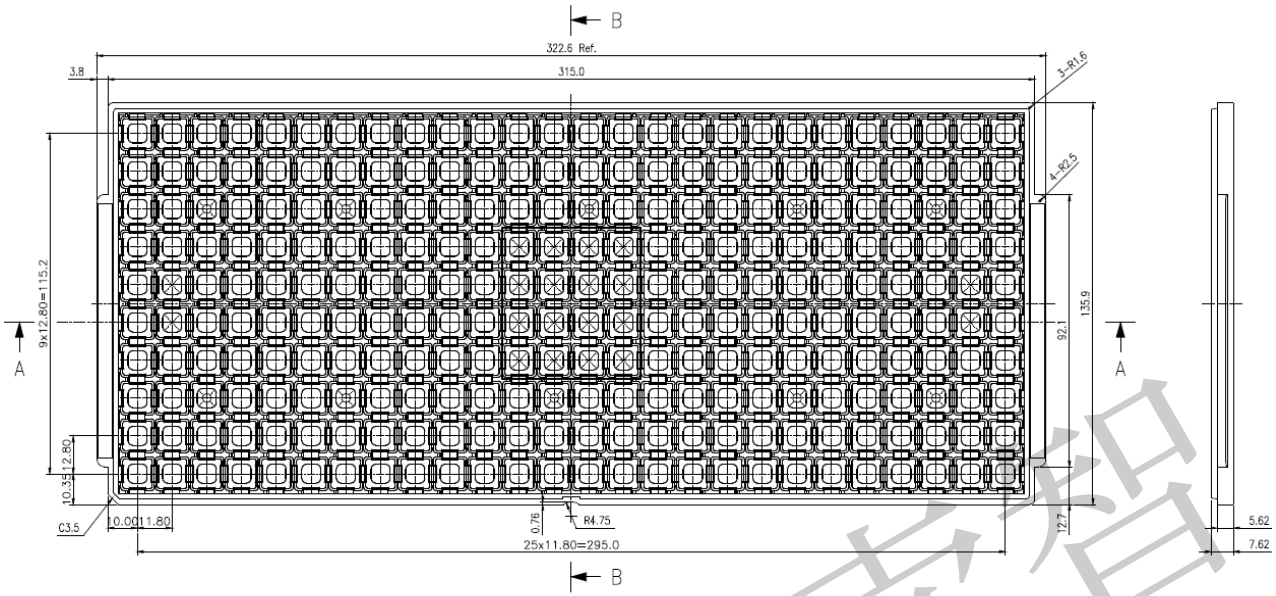
Item	Color	Size	Note
Tray	Black	315mm x 136mm x 7.62mm	260 Qty/Tray
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm	Surface impedance:$10^9\Omega$ Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm	
Inner Box	White	396mm x 196mm x 96mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420mm x 410mm x 320mm	6 Inner box/Carton

Table 13-4 shows the V831 packing quantity.

Table 13- 4. V831 Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty

V831	9 x 9	260	10	2600	6	15600



NOTE :
1. SURFACE RESISTIVITY $10^5 \sim 10^9$ Ω/sq
2. WARPAGE IS WITHIN 0.76mm.
3. FORBID USING THE FIRST CLASS ENVIRONMENT RESTRICTS SUBSTANCES MATERIAL
4. Matrix: 10X26=260

Figure 13- 2. V831 Tray Dimension

13.2. Storage

Reliability is affected if any condition specified in Section 13.2.2 and Section 13.2.3 has been exceeded.

13.2.1. Moisture Sensitivity Level(MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in Table 13-5.

Table 13- 5. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH

2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The V833/V831 device samples are classified as MSL3.

13.2.2. Bagged Storage Conditions

The shelf life of the V833/V831 device samples are defined in Table 13-6.

Table 13- 6. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

13.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the V833/V831 are as follows.

Table 13- 7. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

13.3. Baking

It is not necessary to bake the V833/V831 if the conditions specified in Section 13.2.2 and Section 13.2.3 have not been exceeded. It is necessary to bake the V833/V831 if any condition specified in Section 13.2.2 and Section 13.2.3 has been exceeded.

It is necessary to bake the V833/V831 if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

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Chapter 14 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The lead-free reflow profile conditions are given in Table 14-1. The table is for reference only.

Table 14- 1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

Figure 14-1 shows the typical lead-free reflow profile.

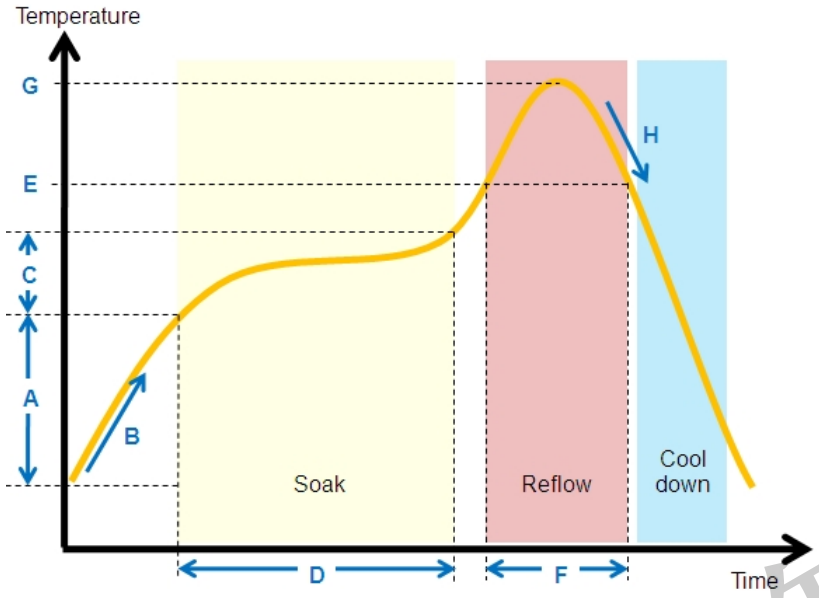

Figure 14- 1. Typical Lead-free Reflow Profile

NOTE

The above reflow profile is solder joint testing result, it is for reference only, please adjust depending on actual production conditions.

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 14-2.

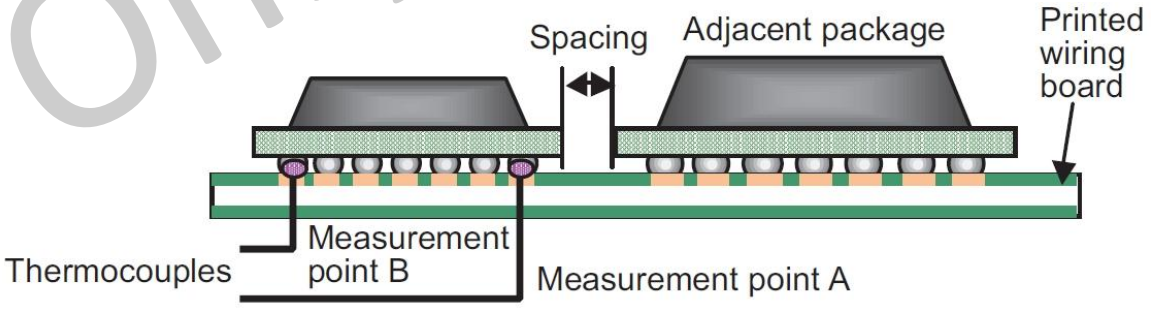

Figure 14- 2. Measuring the Reflow Solding Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

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Chapter 15 Part Marking

15.1. V833

Figure 15-1 shows the V833 package marking.

Figure 15- 1. V833 Package Marking

Table 15-1 describes the V833 package marking definitions.

Table 15- 1. V833 Package Marking Definitions

NO.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V833	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

15.2. V831

Figure 15-2 shows the V831 package marking.

Figure 15- 2. V831 Package Marking

Table 15-2 describes the V831 package marking definitions.

Table 15- 2. V831 Package Marking Definitions

NO.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V831	Product name	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX2	Date code	Dynamic

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