Allwinner Technology

Allwinner UltraOcta A80 Datasheet

UltraOcta Application Processor

Revision 1.0

Mar 17, 2014

Declaration

Revision History

Revision	Date	Description
1.0	Mar 17, 2014	initial version for public release

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1 OVERVIEW

Allwinner's latest flagship octa-core application processor is a revolutionary advance in mobile processor technology. The A80 packs octa-core big.LITTLE Cortex™-A15/7 in a 28nm process to deliver an outstanding combination of both computing power and efficiency.

Fast, smooth, and fluid graphics drive the user experience on premium devices. A80 features the lightning-fast PowerVR 64-core G6230 GPU from Imagination Technologies, delivering industry-leading graphics performance and enabling console-class performance even on the most graphics-intensive games. In addition to superior graphics performance, the A80 excels in multimedia with an advanced HawkView™ ISP supporting cameras up to 16M, innovative video engine technology with 4Kx2K video encoding/decoding, high resolution displays up to 2560x1600, advanced HD DRM support, and low power LTE connectivity.

Application usage is extremely diverse on tablets and smartphones: users listen to music, watch movies, browse the web, share photos, play games, send emails, and more. Each application requires different levels of processing power, and that means different applications run more efficiently on different cores. To deliver optimal efficiency, the Allwinner A80 features all-new CoolFlex™ technology that enables devices to seamlessly run different applications on different CPU cores - saving power by giving applications just the right amount of juice that they need.

2 FEATURES

2.1. CPU Architecture

The A80 platform is based on octa-core big. LITTLE Cortex™-A15/7 CPU architecture.

- ARMv7 ISA standard instruction set plus Thumb-2 and Jazeller RCT
- NEON with SIMD and VFPv4 support
- Support LPAE
- Support 32KB I-cache and 32KB D-cache per CPU
- Support 2MB+512KB L2 cache

2.2. GPU

- PowerVR 64-core G6230 GPU
- Support OpenGL ES 1.1/2.0/3.0, OpenCL 1.1, DirectX 9.3 standards
- Geometry ability up to 133M/s
- Effective pixel ability up to 5.33G/s
- Support up to 85 GFLOPs

2.3. Memory Subsystem

This section consists of:

- Boot ROM
- SDRAM
- NAND Flash
- SD/MMC interface

Boot ROM

- Support system boot from Raw NAND, eMMC NAND, SPI NOR Flash, and SD/TF card
- Support system code download through USB DRD

SDRAM

- Support 8GB address space
- Support dual-channel 64-bit bus width
- Support LPDDR2/LPDDR3/DDR3/DDR3L SDRAM

NAND Flash

- Support 8-bit data BUS width
- Support 72-bit ECC per 1024 bytes
- Support 4 flash chips
- Support 1024, 2048, 4096, 8192, 16K, 32K bytes size per page
- Support SDR, ONFI NV-DDR/NV-DDR2 and Toggle DDR/DDR2

SD/MMC Interface

- Comply to eMMC standard specification V4.5, SD physical layer specification V3.0, SDIO card specification V2.0
- Support 4/8-bit bus width
- Support data rate up to 100Mbps
- Support four SD/MMC controllers
- Support SDIO interrupt detection
- Support 3.3V/1.8V IO voltage

2.4. System Peripheral

This section includes:

- Timer
- High Speed Timer
- GIC
- DMA
- CCU
- PWM
- Security System
- Security ID
- Trustzone
- CPU Configuration
- Power Management

Timer

- Support eight timers
- Support 33-bit AVS counter
- Support 2 watchdogs to generate reset signal or interrupts

High Speed Timer

- Support 5 high speed timers, support five counters up to 56 bits

OSC24M

- Support 1.8v oscillator
- Support internal RC oscillator

GIC

- Support 16 SGIs, 16 PPIs and 192 SPIs

DMA

- 16-channel DMA
- Support data width of 8/16/32 bits
- Support linear and IO address modes

CCU

- 12 PLLs
- Support a 24MHz oscillator and an on-chip RC oscillator
- Support clock configuration for corresponding modules
- Support software-controlled clock gating and software-controlled reset for corresponding modules

PWM

- Support four PWM outputs

Security System

- Support AES, DES, 3DES, SHA1/224/256, MD5
- Support ECB, CBC, CTR, CTS modes for AES/DES/3DES
- 128-bit, 192-bit and 256-bit key size for AES
- 160-bit hardware PRNG with 192-bit seed
- 512/1024/2048-bits RSA
- 32bits hardware CRC
- 256bit TRNG

Security ID

- Support 4Kb EFUSE for chip ID and security application

Trustzone

- Support trustzone technology
- Support 256KB secure SRAM

CPU Configuration

- Support power clamp
- Support flexible CPU configuration

Power Management

- Support DVFS for CPU frequency and voltage adjustment
- Support flexible clock gate and module reset
- Support dynamic frequency adjustment for external DRAM
- Support multiple power domains

2.5. Display Subsystem

This section includes:

- Display engine
- Video output

Display Engine

- Four movable layers, each layer size up to 8192x8192 pixels
- Ultra-Scaling engine
  - –Support 8-tap anti-aliasing filter in horizontal and 4-tap in vertical
  - –Support input and output size up to 4096x4096 pixels
  - –16/32bpp ARGB/YUV444/420/422/411
  - –resize ratio from 1/16x to 32x
- Support multiple image input formats: 16/24/32bpp RGB,Planar YUV444/420/422/411
- Support alpha blending / color key
- Support Color Management Unit (CMU) and Dynamic Range Controller (DRC)
- Support realtime write back function
- Support hardware cursor

Video Output

- Support three independent display channels
- Support 3D function
- Support parallel LCD port up to 2048x1536@60Hz resolution
- Support dual-channel LVDS up to 1920x1080@60Hz resolution
- Support 4-lane MIPI DSI (V1.0) up to 1920x1200@60Hz resolution
- Support 4-lane eDP (V1.2) up to 2560x1600@60Hz resolution
- Support HDMI V1.4 output

2.6. Video Engine

Video Decoding

- Support video playback up to 4096x2048@30fps
- Support multi-format video playback, including MPEG1/2, MPEG4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP8, WMV9/VC-1, JPEG/MJPEG, etc

Video Encoding

- Support H.264/VP8 video encoding up to 4096x2048@30fps, 1080p@120fps, 720p@240fps
- JPEG baseline: picture size up to 8192x8192
- Support input picture size up to 4800x4800
- Support input format: tiled /YUV planner/YUV semi-planner/ARGB/YUYV/UYVY
- Support Alpha blending
- Support thumb generation
- Support 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio
- Support rotated input

2.7. Image Subsystem

CSI

- Support 12-bit parallel camera sensor
- Support up to 5M pixel camera sensor
- Support video shot up to 720p@30fps

MIPI CSI

- Support 4-lane MIPI CSI-2
- Support up to 16M pixel camera sensor
- Support video shot up to 1080p@60fps

2.8. ISP

- Supported input formats: 8/10/12-bit RAW RGB, 8/10-bit YCbCr
- Supported output formats: YCbCr420 semi-planar, YCrCb420 semi-planar, YCbCr422 semi-planar, YCrCb422 semi-planar, YUV420 planar, YUV422 planar.
- Support image mirror flip and rotation
- Support thumb image generation
- Support two output channels
- Support valid picture size up to 4800x4800
- Support speed up to 400M pixels

2.9. Face Detection

- Support up to 900 faces per frame
- Support up to 15 frames per second, with up to 15 faces on each frame
- Support 15 ROI region (size up to 320 x 320 per ROI)
- Support front-view face and side-view face: -90/-45/0/45/90 degree
- Support 0/90/180/270 degree detection
- Support input image resize

2.10. External Peripherals

This section includes:

- USB
- Ethernet MAC
- ADC
- Digital Audio Interface
- Transport Stream
- CIR
- UART
- SPI
- TWI
- One Wire
- RSB™

USB

- USB 3.0 DRD SIE with both USB 2.0 and USB 3.0 PHY
- Three EHCI/OHCI compliant Host SIE multiplexed with two USB 2.0 analog PHYs, one HSIC PHY

Ethernet MAC

- Support 10/100/1000 Mbps data transfer rate
- Support MII/RGMII PHY interface

ADC

- KeyADC with 6-bit resolution
- GPADC with 12-bit resolution

Digital Audio Interface

- Two I2S/PCM compliant digital audio interfaces

Transport Stream

- Support both Synchronous Parallel Interface (SPI) and Synchronous Serial Interface (SSI)
- Support speed up to 150Mbps for both SPI and SSI interface
- Support 32-channel PID filter

CIR

- Support a flexible receiver for IR remote

UART

- Support seven UART controllers

SPI

- Support four SPI controllers
- Master/Slave configurable

TWI

- Support seven TWI controllers

One Wire

- Support an one-wire controller for single wire communication

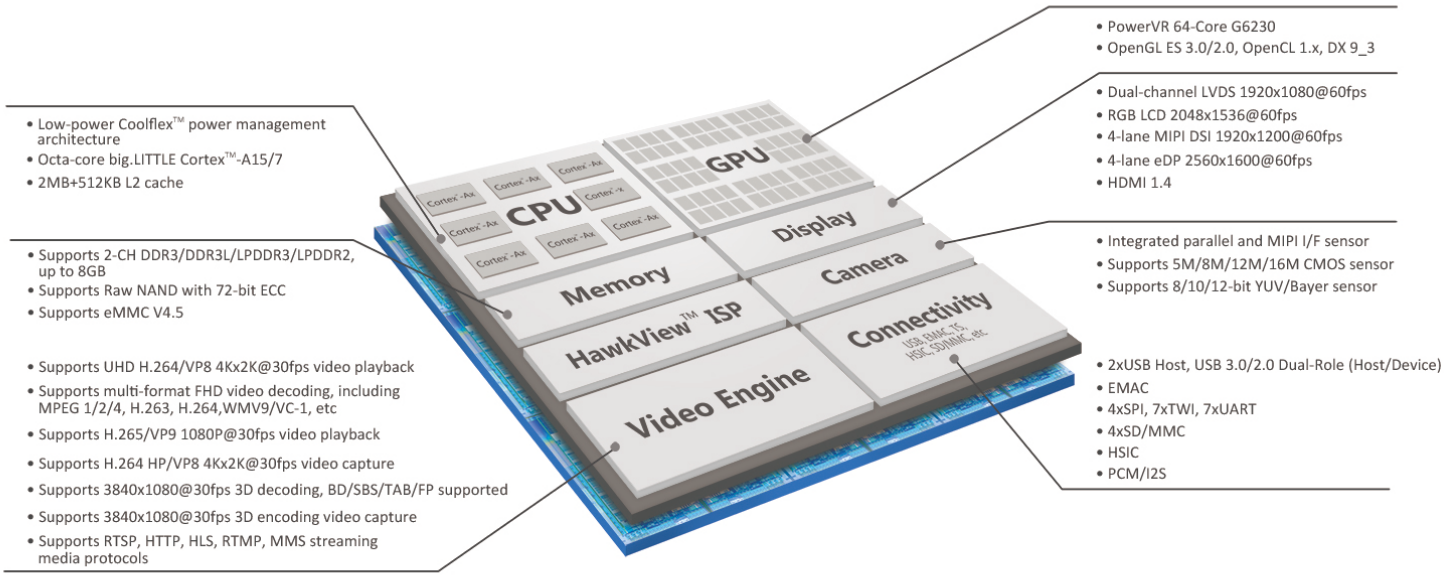
RSB™ (Reduced Serial Bus)

- Support transfer speed up to 20Mbps

2.11. Process and Package

- 28nm process
- FCBGA 636 balls, 0.65mm ball pitch, 19mm x 19mm

3 BLOCK DIAGRAM



A80 Block Diagram

4 PIN DESCRIPTION

4.1. PIN CHARACTERISTICS

Following table describes the A80 pin characteristics from seven aspects: ***BALL#, Pin Name, Default Function[1], Type[2], Reset State[3], Default Pull Up/Down[4], and Buffer Strength[5]***.

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
SDRAM						
V1	S0DQ0	DRAM	I/O	Z	-	-
V2	S0DQ1	DRAM	I/O	Z	-	-
U1	S0DQ2	DRAM	I/O	Z	-	-
U2	S0DQ3	DRAM	I/O	Z	-	-
R1	S0DQ4	DRAM	I/O	Z	-	-
R2	S0DQ5	DRAM	I/O	Z	-	-
P1	S0DQ6	DRAM	I/O	Z	-	-
P2	S0DQ7	DRAM	I/O	Z	-	-
L2	S0DQ8	DRAM	I/O	Z	-	-
K2	S0DQ9	DRAM	I/O	Z	-	-
K1	S0DQ10	DRAM	I/O	Z	-	-
J1	S0DQ11	DRAM	I/O	Z	-	-
H2	S0DQ12	DRAM	I/O	Z	-	-
G1	S0DQ13	DRAM	I/O	Z	-	-
G2	S0DQ14	DRAM	I/O	Z	-	-
F1	S0DQ15	DRAM	I/O	Z	-	-
AD2	S0DQ16	DRAM	I/O	Z	-	-
AC1	S0DQ17	DRAM	I/O	Z	-	-
AC2	S0DQ18	DRAM	I/O	Z	-	-
AB1	S0DQ19	DRAM	I/O	Z	-	-
AA2	S0DQ20	DRAM	I/O	Z	-	-
Y1	S0DQ21	DRAM	I/O	Z	-	-
Y2	S0DQ22	DRAM	I/O	Z	-	-

Note:

1 ***Default function*** defines the default function of each pin, especially for pins with multiplexing functions;

2 There are five ***pin types*** here: O for output, I for input, I/O for input/output, A for analog,OD for Open-Drain, P for power and G for ground;

3 ***Reset state*** defines the state of the terminal at reset: Z for high-impedance.

4 ***Default Pull up/down*** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;

5 ***Buffer strength*** defines the driver strength of the associated output buffer. It is tested in the condition that VCC= 3.0V, strength=MAX;

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
W1	S0DQ23	DRAM	I/O	Z	-	-
E1	S0DQ24	DRAM	I/O	Z	-	-
E2	S0DQ25	DRAM	I/O	Z	-	-
D1	S0DQ26	DRAM	I/O	Z	-	-
D2	S0DQ27	DRAM	I/O	Z	-	-
B1	S0DQ28	DRAM	I/O	Z	-	-
B2	S0DQ29	DRAM	I/O	Z	-	-
A2	S0DQ30	DRAM	I/O	Z	-	-
A3	S0DQ31	DRAM	I/O	Z	-	-
M3	S0VREF	DRAM	P	-	-	-
C2	S0DQS3	DRAM	I/O	Z	-	-
AA1	S0DQS2	DRAM	I/O	Z	-	-
H1	S0DQS1	DRAM	I/O	Z	-	-
T2	S0DQS0	DRAM	I/O	Z	-	-
C1	S0DQS3B	DRAM	I/O	Z	-	-
AB2	S0DQS2B	DRAM	I/O	Z	-	-
J2	S0DQS1B	DRAM	I/O	Z	-	-
T1	S0DQS0B	DRAM	I/O	Z	-	-
F2	S0DQM3	DRAM	O	Z	-	-
AD1	S0DQM2	DRAM	O	Z	-	-
L1	S0DQM1	DRAM	O	Z	-	-
W2	S0DQM0	DRAM	O	Z	-	-
N1	S0CK	DRAM	O	Z	-	-
M1	S0CK1	DRAM	O	Z	-	-
N2	S0CKB	DRAM	O	Z	-	-
M2	S0CK1B	DRAM	O	Z	-	-
U4	S0CKE	DRAM	O	Z	-	-
U5	S0CKE1	DRAM	O	Z	-	-
R3	S0A0	DRAM	O	Z	-	-
R6	S0A1	DRAM	O	Z	-	-
U7	S0A2	DRAM	O	Z	-	-
P5	S0A3	DRAM	O	Z	-	-
M4	S0A4	DRAM	O	Z	-	-
J3	S0A5	DRAM	O	Z	-	-
F3	S0A6	DRAM	O	Z	-	-
L4	S0A7	DRAM	O	Z	-	-
L5	S0A8	DRAM	O	Z	-	-
F4	S0A9	DRAM	O	Z	-	-
R4	S0A10	DRAM	O	Z	-	-
R7	S0A11	DRAM	O	Z	-	-
P8	S0A12	DRAM	O	Z	-	-
J4	S0A13	DRAM	O	Z	-	-
P7	S0A14	DRAM	O	Z	-	-
P4	S0A15	DRAM	O	Z	-	-
E4	S0BA0	DRAM	O	Z	-	-
U8	S0BA1	DRAM	O	Z	-	-
H4	S0BA2	DRAM	O	Z	-	-
H5	S0WE	DRAM	O	Z	-	-
L7	S0CAS	DRAM	O	Z	-	-
H7	S0RAS	DRAM	O	Z	-	-
M7	S0CS	DRAM	O	Z	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
M6	S0CS1	DRAM	O	Z	-	-
J7	S0ODT	DRAM	O	Z	-	-
J6	S0ODT1	DRAM	O	Z	-	-
B3	S0ZQ	DRAM	A	Z	-	-
L8	S0RST	DRAM	O	Z	-	-
AG16	S1DQ0	DRAM	I/O	Z	-	-
AG17	S1DQ1	DRAM	I/O	Z	-	-
AH16	S1DQ2	DRAM	I/O	Z	-	-
AH15	S1DQ3	DRAM	I/O	Z	-	-
AH13	S1DQ4	DRAM	I/O	Z	-	-
AG13	S1DQ5	DRAM	I/O	Z	-	-
AH12	S1DQ6	DRAM	I/O	Z	-	-
AG14	S1DQ7	DRAM	I/O	Z	-	-
AH9	S1DQ8	DRAM	I/O	Z	-	-
AG9	S1DQ9	DRAM	I/O	Z	-	-
AH8	S1DQ10	DRAM	I/O	Z	-	-
AG8	S1DQ11	DRAM	I/O	Z	-	-
AH6	S1DQ12	DRAM	I/O	Z	-	-
AG6	S1DQ13	DRAM	I/O	Z	-	-
AG5	S1DQ14	DRAM	I/O	Z	-	-
AH5	S1DQ15	DRAM	I/O	Z	-	-
AB12	S1DQ16	DRAM	I/O	Z	-	-
AD15	S1DQ17	DRAM	I/O	Z	-	-
AD12	S1DQ18	DRAM	I/O	Z	-	-
AC17	S1DQ19	DRAM	I/O	Z	-	-
AE12	S1DQ20	DRAM	I/O	Z	-	-
AE17	S1DQ21	DRAM	I/O	Z	-	-
AF17	S1DQ22	DRAM	I/O	Z	-	-
AF14	S1DQ23	DRAM	I/O	Z	-	-
AG4	S1DQ24	DRAM	I/O	Z	-	-
AH3	S1DQ25	DRAM	I/O	Z	-	-
AG3	S1DQ26	DRAM	I/O	Z	-	-
AH2	S1DQ27	DRAM	I/O	Z	-	-
AF1	S1DQ28	DRAM	I/O	Z	-	-
AF2	S1DQ29	DRAM	I/O	Z	-	-
AE1	S1DQ30	DRAM	I/O	Z	-	-
AE2	S1DQ31	DRAM	I/O	Z	-	-
AD3	S1VREF	DRAM	P	-	-	-
AG1	S1DQS3	DRAM	I/O	Z	-	-
AE15	S1DQS2	DRAM	I/O	Z	-	-
AG7	S1DQS1	DRAM	I/O	Z	-	-
AH14	S1DQS0	DRAM	I/O	Z	-	-
AG2	S1DQS3B	DRAM	I/O	Z	-	-
AF15	S1DQS2B	DRAM	I/O	Z	-	-
AH7	S1DQS1B	DRAM	I/O	Z	-	-
AG15	S1DQS0B	DRAM	I/O	Z	-	-
AH4	S1DQM3	DRAM	O	Z	-	-
AB17	S1DQM2	DRAM	O	Z	-	-
AG10	S1DQM1	DRAM	O	Z	-	-
AH17	S1DQM0	DRAM	O	Z	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
AH11	S1CK	DRAM	O	Z	-	-
AH10	S1CK1	DRAM	O	Z	-	-
AG12	S1CKB	DRAM	O	Z	-	-
AG11	S1CK1B	DRAM	O	Z	-	-
AD6	S1CKE	DRAM	O	Z	-	-
AE6	S1CKE1	DRAM	O	Z	-	-
AE11	S1A0	DRAM	O	Z	-	-
AF11	S1A1	DRAM	O	Z	-	-
AD9	S1A2	DRAM	O	Z	-	-
AE9	S1A3	DRAM	O	Z	-	-
AC8	S1A4	DRAM	O	Z	-	-
AF5	S1A5	DRAM	O	Z	-	-
AE5	S1A6	DRAM	O	Z	-	-
AD4	S1A7	DRAM	O	Z	-	-
AC5	S1A8	DRAM	O	Z	-	-
AC4	S1A9	DRAM	O	Z	-	-
AE14	S1A10	DRAM	O	Z	-	-
AB11	S1A11	DRAM	O	Z	-	-
AC11	S1A12	DRAM	O	Z	-	-
AA6	S1A13	DRAM	O	Z	-	-
AA12	S1A14	DRAM	O	Z	-	-
AC14	S1A15	DRAM	O	Z	-	-
AA3	S1BA0	DRAM	O	Z	-	-
AB14	S1BA1	DRAM	O	Z	-	-
AA4	S1BA2	DRAM	O	Z	-	-
Y5	S1WE	DRAM	O	Z	-	-
Y4	S1CAS	DRAM	O	Z	-	-
V7	S1RAS	DRAM	O	Z	-	-
AF8	S1CS	DRAM	O	Z	-	-
AE8	S1CS1	DRAM	O	Z	-	-
V6	S1ODT	DRAM	O	Z	-	-
V4	S1ODT1	DRAM	O	Z	-	-
V3	S1ZQ	DRAM	A	Z	-	-
AA15	S1RST	DRAM	O	Z	-	-
Y8,Y9,AA9,AB8	VDD18-DLL	POWER	P	-	-	-
F5,J5,M5,R5,V5, AD17,H6,L6,P6,U6, Y6,AB6,AC7,AD8, AC9,AD11,AC12, AD14,AC15,AA5	VCC-DRAM	POWER	P	-	-	-
GPIO A						
AE23	PA0	GPIO	I/O	Z	NO PULL	20
AF23	PA1	GPIO	I/O	Z	NO PULL	20
AG23	PA2	GPIO	I/O	Z	NO PULL	20
AH23	PA3	GPIO	I/O	Z	NO PULL	20
AD23	PA4	GPIO	I/O	Z	NO PULL	20
AB23	PA5	GPIO	I/O	Z	NO PULL	20
AG22	PA6	GPIO	I/O	Z	NO PULL	20
AH22	PA7	GPIO	I/O	Z	NO PULL	20
AC21	PA8	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
AD21	PA9	GPIO	I/O	Z	NO PULL	20
AE21	PA10	GPIO	I/O	Z	NO PULL	20
AG21	PA11	GPIO	I/O	Z	NO PULL	20
AH21	PA12	GPIO	I/O	Z	NO PULL	20
AE20	PA13	GPIO	I/O	Z	NO PULL	20
AF20	PA14	GPIO	I/O	Z	NO PULL	20
AG20	PA15	GPIO	I/O	Z	NO PULL	20
AH20	PA16	GPIO	I/O	Z	NO PULL	20
AC20	PA17	GPIO	I/O	Z	NO PULL	20
AD20,AC22	VCC-PA	POWER	P	-	-	-
GPIO B						
AD18	PB5	GPIO	I/O	Z	NO PULL	20
AG18	PB6	GPIO	I/O	Z	NO PULL	20
AH18	PB14	GPIO	I/O	Z	NO PULL	20
AB18	PB15	GPIO	I/O	Z	NO PULL	20
AA18	PB16	GPIO	I/O	Z	NO PULL	20
AC18	VCC-PB	POWER	P	-	-	-
GPIO C						
H11	PC0	GPIO	I/O	Z	NO PULL	20
H9	PC1	GPIO	I/O	Z	NO PULL	20
G9	PC2	GPIO	I/O	Z	NO PULL	20
E9	PC3	GPIO	I/O	Z	PULL UP	20
D9	PC4	GPIO	I/O	Z	PULL UP	20
C9	PC5	GPIO	I/O	Z	NO PULL	20
B9	PC6	GPIO	I/O	Z	PULL UP	20
G11	PC7	GPIO	I/O	Z	NO PULL	20
A8	PC8	GPIO	I/O	Z	NO PULL	20
A9	PC9	GPIO	I/O	Z	NO PULL	20
B10	PC10	GPIO	I/O	Z	NO PULL	20
A10	PC11	GPIO	I/O	Z	NO PULL	20
H12	PC12	GPIO	I/O	Z	NO PULL	20
G12	PC13	GPIO	I/O	Z	NO PULL	20
E11	PC14	GPIO	I/O	Z	NO PULL	20
D11	PC15	GPIO	I/O	Z	NO PULL	20
B11	PC16	GPIO	I/O	Z	NO PULL	20
A11	PC17	GPIO	I/O	Z	NO PULL	20
H14	PC18	GPIO	I/O	Z	NO PULL	20
G14	PC19	GPIO	I/O	Z	NO PULL	20
F9,F11	VCC-PC	POWER	P	-	-	-
GPIO D						
D12	PD0	GPIO	I/O	Z	NO PULL	20
E12	PD1	GPIO	I/O	Z	NO PULL	20
B12	PD2	GPIO	I/O	Z	NO PULL	20
A12	PD3	GPIO	I/O	Z	NO PULL	20
B13	PD4	GPIO	I/O	Z	NO PULL	20
A13	PD5	GPIO	I/O	Z	NO PULL	20
E14	PD6	GPIO	I/O	Z	NO PULL	20
D14	PD7	GPIO	I/O	Z	NO PULL	20
B14	PD8	GPIO	I/O	Z	NO PULL	20
A14	PD9	GPIO	I/O	Z	NO PULL	20
G15	PD10	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
H15	PD11	GPIO	I/O	Z	NO PULL	20
D15	PD12	GPIO	I/O	Z	NO PULL	20
E15	PD13	GPIO	I/O	Z	NO PULL	20
B15	PD14	GPIO	I/O	Z	NO PULL	20
A15	PD15	GPIO	I/O	Z	NO PULL	20
B16	PD16	GPIO	I/O	Z	NO PULL	20
A16	PD17	GPIO	I/O	Z	NO PULL	20
B17	PD18	GPIO	I/O	Z	NO PULL	20
A17	PD19	GPIO	I/O	Z	NO PULL	20
C17	PD20	GPIO	I/O	Z	NO PULL	20
D17	PD21	GPIO	I/O	Z	NO PULL	20
F17	PD22	GPIO	I/O	Z	NO PULL	20
G17	PD23	GPIO	I/O	Z	NO PULL	20
H17	PD24	GPIO	I/O	Z	NO PULL	20
F18	PD25	GPIO	I/O	Z	NO PULL	20
G18	PD26	GPIO	I/O	Z	NO PULL	20
H18	PD27	GPIO	I/O	Z	NO PULL	20
C15	VCC18-LVDS	POWER	P	-	-	-
F12,F14,F15	VCC-PD	POWER	P	-	-	-
GPIO E						
AA27	PE0	GPIO	I/O	Z	NO PULL	20
AA28	PE1	GPIO	I/O	Z	NO PULL	20
V26	PE2	GPIO	I/O	Z	NO PULL	20
Y26	PE3	GPIO	I/O	Z	NO PULL	20
V25	PE4	GPIO	I/O	Z	NO PULL	20
Y25	PE5	GPIO	I/O	Z	NO PULL	20
AA25	PE6	GPIO	I/O	Z	NO PULL	20
V24	PE7	GPIO	I/O	Z	NO PULL	20
V23	PE8	GPIO	I/O	Z	NO PULL	20
R22	PE9	GPIO	I/O	Z	NO PULL	20
Y23	PE10	GPIO	I/O	Z	NO PULL	20
AA23	PE11	GPIO	I/O	Z	NO PULL	20
V22	PE12	GPIO	I/O	Z	NO PULL	20
R21	PE13	GPIO	I/O	Z	NO PULL	20
AA22	PE14	GPIO	I/O	Z	NO PULL	20
Y22	PE15	GPIO	I/O	Z	NO PULL	20
U21	PE16	GPIO	I/O	Z	NO PULL	20
V21	PE17	GPIO	I/O	Z	NO PULL	20
Y24,AA24	VCC-PE	POWER	P	-	-	-
GPIO F						
AB21	PF0	GPIO	I/O	Z	NO PULL	20
AB20	PF1	GPIO	I/O	Z	NO PULL	20
AA20	PF2	GPIO	I/O	Z	NO PULL	20
Y21	PF3	GPIO	I/O	Z	NO PULL	20
AG19	PF4	GPIO	I/O	Z	NO PULL	20
AH19	PF5	GPIO	I/O	Z	NO PULL	20
AE18	VCC-PF	POWER	P	-	-	-
GPIO G						
B4	PG0	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
A4	PG1	GPIO	I/O	Z	NO PULL	20
D6	PG2	GPIO	I/O	Z	NO PULL	20
C5	PG3	GPIO	I/O	Z	NO PULL	20
B5	PG4	GPIO	I/O	Z	NO PULL	20
A5	PG5	GPIO	I/O	Z	NO PULL	20
E6	PG6	GPIO	I/O	Z	NO PULL	20
D5	PG7	GPIO	I/O	Z	NO PULL	20
B6	PG8	GPIO	I/O	Z	NO PULL	20
A6	PG9	GPIO	I/O	Z	NO PULL	20
B7	PG10	GPIO	I/O	Z	NO PULL	20
A7	PG11	GPIO	I/O	Z	NO PULL	20
G8	PG12	GPIO	I/O	Z	NO PULL	20
E8	PG13	GPIO	I/O	Z	NO PULL	20
D8	PG14	GPIO	I/O	Z	NO PULL	20
B8	PG15	GPIO	I/O	Z	NO PULL	20
F7,F8	VCC-PG	POWER	P	-	-	-
GPIO H						
AB28	PH0	GPIO	I/O	Z	NO PULL	20
AB27	PH1	GPIO	I/O	Z	NO PULL	20
AC28	PH2	GPIO	I/O	Z	NO PULL	20
AC27	PH3	GPIO	I/O	Z	NO PULL	20
AC26	PH4	GPIO	I/O	Z	NO PULL	20
AC25	PH5	GPIO	I/O	Z	NO PULL	20
AD28	PH6	GPIO	I/O	Z	NO PULL	20
AD27	PH8	GPIO	I/O	Z	NO PULL	20
AD26	PH9	GPIO	I/O	Z	NO PULL	20
AE28	PH10	GPIO	I/O	Z	NO PULL	20
AE27	PH11	GPIO	I/O	Z	NO PULL	20
AF28	PH12	GPIO	I/O	Z	NO PULL	20
AF27	PH13	GPIO	I/O	Z	NO PULL	20
AG28	PH14	GPIO	I/O	Z	NO PULL	20
AG27	PH15	GPIO	I/O	Z	NO PULL	20
AH27	PH16	GPIO	I/O	Z	NO PULL	20
AG26	PH17	GPIO	I/O	Z	NO PULL	20
AH26	PH18	GPIO	I/O	Z	NO PULL	20
AG25	PH19	GPIO	I/O	Z	NO PULL	20
AH25	PH20	GPIO	I/O	Z	NO PULL	20
AF24	PH21	GPIO	I/O	Z	NO PULL	20
AD25,AE24	VCC-PH	POWER	P	-	-	-
GPIO L						
E28	PL0	GPIO	I/O	Z		20
E27	PL1	GPIO	I/O	Z		20
E26	PL2	GPIO	I/O	Z	NO PULL	20
E23	PL3	GPIO	I/O	Z	NO PULL	20
F25	PL4	GPIO	I/O	Z	NO PULL	20
F26	PL5	GPIO	I/O	Z	NO PULL	20
F27	PL6	GPIO	I/O	Z	NO PULL	20
F28	PL7	GPIO	I/O	Z	NO PULL	20
F22	PL8	GPIO	I/O	Z	NO PULL	20
G23	PL9	GPIO	I/O	Z	NO PULL	20
F24	VCC-PL	POWER	P	-	-	-
GPIO M						
B24	PM0	GPIO	I/O	Z		20
A25	PM1	GPIO	I/O	Z		20
B25	PM2	GPIO	I/O	Z	NO PULL	20
A26	PM3	GPIO	I/O	Z	NO PULL	20
E25	PM4	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
B26	PM8	GPIO	I/O	Z	NO PULL	20
B27	PM9	GPIO	I/O	Z	NO PULL	20
A27	PM10	GPIO	I/O	Z		20
B28	PM11	GPIO	I/O	Z		20
C27	PM12	GPIO	I/O	Z	NO PULL	20
C28	PM13	GPIO	I/O	Z	NO PULL	20
D27	PM14	GPIO	I/O	Z	NO PULL	20
D28	PM15	GPIO	I/O	Z	NO PULL	20
D24	VCC-PM	POWER	P	-	-	-
GPIO N						
B23	PN0	GPIO	I/O	Z	PULL UP	20
A23	PN1	GPIO	I/O	Z	PULL UP	20
SYSTEM CONTROL						
A21	UBOOT	-	I	-	PULL UP	-
H23	JTAGSEL0	-	I	-	PULL UP	-
H22	JTAGSEL1	-	I	-	PULL UP	-
AG24	BOOTSEL0	-	I	-	PULL UP	-
AH24	BOOTSEL1	-	I	-	PULL UP	-
J20	VCC18-EFUSE	-	P	-	-	-
C24	NMI	-	I	Z	NO PULL	-
C26	RESET	-	I	Z	NO PULL	-
USB						
R27	USB0-DM	-	A	-	-	-
R28	USB0-DP	-	A	-	-	-
P22	USB0-ID	-	A	-	-	-
P21	USB0-VBUS	-	A	-	-	-
P27	USB0-SSTXN	-	A	-	-	-
P28	USB0-SSTXP	-	A	-	-	-
N27	USB0-SSRXN	-	A	-	-	-
N28	USB0-SSRXP	-	A	-	-	-
M26	VCC33-USB0	-	P	-	-	-
M24	VDD09-USB0	-	P	-	-	-
P26	GND-USB0	-	G	-	-	-
R25	USB1-DM	-	A	-	-	-
R24	USB1-DP	-	A	-	-	-
P24	USB2-DM	-	A	-	-	-
P25	USB2-DP	-	A	-	-	-
R26	VCC33-USBH	-	P	-	-	-
P23,R23	VDD09-USBH	-	P	-	-	-
HSIC						
T27	HSIC-STRB	-	A	-	-	-
T28	HSIC-DATA	-	A	-	-	-
U22	VCC12-HSIC	-	P	-	-	-
ADC						
G20	GPADC0	-	A	-	-	-
H20	GPADC1	-	A	-	-	-
E21	KeyADC0	-	A	-	-	-
B21	KeyADC1	-	A	-	-	-
D21	VCC18-ADC	-	P	-	-	-
C21	GND-ADC	-	G	-	-	-
HDMI						
J28	HTX0P	-	A	-	-	-
J27	HTX0N	-	A	-	-	-
H28	HTX1P	-	A	-	-	-
H27	HTX1N	-	A	-	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
G28	HTX2P	-	A	-	-	-
G27	HTX2N	-	A	-	-	-
K28	HTXCP	-	A	-	-	-
K27	HTXCN	-	A	-	-	-
L25	HHPD	-	A	-	-	-
J24	VCC18-HDMI	-	P	-	-	-
L24	VDD09-HDMI	-	P	-	-	-
H24	GND-HDMI	-	G	-	-	-
eDP						
D18	EDPD0P	-	A	-	-	-
C18	EDPD0N	-	A	-	-	-
A18	EDPD1P	-	A	-	-	-
B18	EDPD1N	-	A	-	-	-
A19	EDPD2P	-	A	-	-	-
B19	EDPD2N	-	A	-	-	-
D20	EDPD3P	-	A	-	-	-
E20	EDPD3N	-	A	-	-	-
A20	EDPAUXP	-	A	-	-	-
B20	EDPAUXN	-	A	-	-	-
F20	EDPHPD	-	A	-	-	-
E18	VCC18-EDP	-	P	-	-	-
E17	GND-EDP	-	G	-	-	-
MIPI DSI						
M21	MDSI-DM0	-	A	-	-	-
M22	MDSI-DP0	-	A	-	-	-
J25	MDSI-DM1	-	A	-	-	-
J26	MDSI-DP1	-	A	-	-	-
L22	MDSI-DM2	-	A	-	-	-
L21	MDSI-DP2	-	A	-	-	-
J21	MDSI-DM3	-	A	-	-	-
J22	MDSI-DP3	-	A	-	-	-
H26	MDSI-CKN	-	A	-	-	-
H25	MDSI-CKP	-	A	-	-	-
J23	VCC18-MDSI	-	P	-	-	-
L23	GND-MDSI	-	G	-	-	-
MIPI CSI						
Y28	MCSI-DM0	-	A	-	-	-
Y27	MCSI-DP0	-	A	-	-	-
W28	MCSI-DM1	-	A	-	-	-
W27	MCSI-DP1	-	A	-	-	-
U28	MCSI-DM2	-	A	-	-	-
U27	MCSI-DP2	-	A	-	-	-
U25	MCSI-DM3	-	A	-	-	-
U24	MCSI-DP3	-	A	-	-	-
V28	MCSI-CKN	-	A	-	-	-
V27	MCSI-CKP	-	A	-	-	-
U23	VCC18-MCSI	-	P	-	-	-
U26	GND-MCSI	-	G	-	-	-
CLOCK						
F21	REXT	-	A	-	-	-
G21	VIO-RTC	-	A	-	-	-
A24	X32KI	-	A	-	-	-
A22	X24MI	-	A	-	-	-
B22	X24MO	-	A	-	-	-
D23	VCC18-PLL	-	P	-	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/ Down	Buffer Strength (mA)
C23	GND-PLL	-	G	-	-	-
POWER						
M20,N20,P20	VDD18	-	P	-	-	-
K19,K20,L20	VDD-CPUS	-	P	-	-	-
K11,K12,K13,K15, L10,L11,L12,L13, L14,L15,M10,M13, M14,M15,N10, N11,N12,N13,N14, N15,P11,P12,P13, P14	VDD-CPUB	-	P	-	-	-
R17,R18,T16,T17, T18,T19,U16,U17, U18,U19	VDD-CPUA	-	P	-	-	-
J14	VDDFB-CPUB	-	P	-	-	-
K14	GNDFB-CPUB	-	P	-	-	-
T20	VDDFB-CPUA	-	P	-	-	-
T11,T12,T13,T14, U11,U12,U14,V11, V12,V13,V14	VDD-GPU	-	P	-	-	-
T9	VDDFB-GPU	-	P	-	-	-
J16,J17,J18,K17, L17,L18,M17,M18, N17,N18	VDD-SYS	-	P	-	-	-
W16,W17,W18, W19,W20	VDD-VPU	-	P	-	-	-
A1, AH1, C3, E3, H3, L3, P3, U3, Y3, AC3, AF3, C6, G6, AF6, Y7, AA7, J8, M8, R8, V8, C8, J9, K9, L9, M9, N9, P9, R9, U9, V9, W9, AB9, AF9, J10, K10, P10, R10, T10, U10, V10, W10, Y10, J11, M11, R11, W11, Y11, AA11, C11, C12, J12, M12, R12, W12, Y12, AF12, J13, R13, U13, W13, Y13, R14, W14, Y14, AA14, J15, C14, P15, R15, T15, U15, V15, W15, Y15, K16, L16, M16, N16, P16, R16, V16, AA17, P17, V17, Y17, K18, P18, V18, Y18, AF18, J19, L19, M19, N19, P19, R19, V19, Y19, C20, R20, U20, V20, Y20, AF21, AC24, AF26, AA26, L26, A28, AH28	GND	-	P	-	-	-
L28, L27, M28, M27, M25, M23	NC	-	-	-	-	-

4.2. GPIO MULTIPLEXING FUNCTIONS

Following table provides a description of the GPIO multiplexing functions of A80.

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multiplexing Function 2	Multiplexing Function 3	Multiplexing Function 4	Multiplexing Function 5	Multiplexing Function 6
PA0	GPIO	I/O	DIS	Z	RGMII-RXD3/ MII-RXD3		UART1_TX		PA_EINT0
PA1	GPIO	I/O	DIS	Z	RGMII-RXD2/ MII-RXD2		UART1_RX		PA_EINT1
PA2	GPIO	I/O	DIS	Z	RGMII-RXD1/ MII-RXD1		UART1_RTS		PA_EINT2
PA3	GPIO	I/O	DIS	Z	RGMII-RXD0/ MII-RXD0		UART1_CTS		PA_EINT3
PA4	GPIO	I/O	DIS	Z	RGMII-RXCK/ MII-RXCK		UART1_DTR		PA_EINT4
PA5	GPIO	I/O	DIS	Z	RGMII-RXCTL/ MII-RXDV		UART1_DSR		PA_EINT5
PA6	GPIO	I/O	DIS	Z	MII-RXERR		UART1_DCD		PA_EINT6
PA7	GPIO	I/O	DIS	Z	RGMII-TXD3/ MII-TXD3		UART1_RING		PA_EINT7
PA8	GPIO	I/O	DIS	Z	RGMII-TXD2/ MII-TXD2		ECLK_IN0		PA_EINT8
PA9	GPIO	I/O	DIS	Z	RGMII-TXD1/ MII-TXD1		ECLK_IN1		PA_EINT9
PA10	GPIO	I/O	DIS	Z	RGMII-TXD0/ MII-TXD0		CLKA_OUT		PA_EINT10
PA11	GPIO	I/O	DIS	Z	MII-CRS		CLKB_OUT		PA_EINT11
PA12	GPIO	I/O	DIS	Z	RGMII-TXCK/ MII-TXCK		PWM3_P		PA_EINT12
PA13	GPIO	I/O	DIS	Z	RGMII-TXCTL/ MII-TXEN		PWM3_N		PA_EINT13
PA14	GPIO	I/O	DIS	Z	MII-TXERR		SPI1_CS0		PA_EINT14
PA15	GPIO	I/O	DIS	Z	RGMII-CLKIN/ MII-COL		SPI1_CLK		PA_EINT15
PA16	GPIO	I/O	DIS	Z	EMDC		SPI1_MOSI		PA_EINT16
PA17	GPIO	I/O	DIS	Z	EMDIO		SPI1_MISO		PA_EINT17
VCC-PA	GPIO	P							
PB5	GPIO	I/O	DIS	Z		UART3_TX			PB_EINT5
PB6	GPIO	I/O	DIS	Z		UART3_RX			PB_EINT6
PB14	GPIO	I/O	DIS	Z		MCSI_MCLK			PB_EINT14
PB15	GPIO	I/O	DIS	Z		MCSI_SCK	TWI4_SCK		PB_EINT15
PB16	GPIO	I/O	DIS	Z		MCSI_SDA	TWI4_SDA		PB_EINT16
VCC-PB	GPIO	P							
PC0	GPIO	I/O	DIS	Z	NAND0_WE	SPI0_MOSI			
PC1	GPIO	I/O	DIS	Z	NAND0_ALE	SPI0_MISO			

PC2	GPIO	I/O	DIS	Z	NAND0_CLE	SPI0_CLK			
PC3	GPIO	I/O	DIS	PULL-UP	NAND0_CE1				
PC4	GPIO	I/O	DIS	PULL-UP	NAND0_CE0				
PC5	GPIO	I/O	DIS	Z	NAND0_RE				
PC6	GPIO	I/O	DIS	PULL-UP	NAND0_RB0	SDC2_CMD			
PC7	GPIO	I/O	DIS	PULL-UP	NAND0_RB1	SDC2_CLK			
PC8	GPIO	I/O	DIS	Z	NAND0_DQ0	SDC2_D0			
PC9	GPIO	I/O	DIS	Z	NAND0_DQ1	SDC2_D1			
PC10	GPIO	I/O	DIS	Z	NAND0_DQ2	SDC2_D2			
PC11	GPIO	I/O	DIS	Z	NAND0_DQ3	SDC2_D3			
PC12	GPIO	I/O	DIS	Z	NAND0_DQ4	SDC2_D4			
PC13	GPIO	I/O	DIS	Z	NAND0_DQ5	SDC2_D5			
PC14	GPIO	I/O	DIS	Z	NAND0_DQ6	SDC2_D6			
PC15	GPIO	I/O	DIS	Z	NAND0_DQ7	SDC2_D7			
PC16	GPIO	I/O	DIS	Z	NAND0_DQS	SDC2_RST			
PC17	GPIO	I/O	DIS	PULL-UP	NAND0_CE2	NAND0_RE_B			
PC18	GPIO	I/O	DIS	PULL-UP	NAND0_CE3	NAND0_DQS_B			
PC19	GPIO	I/O	DIS	PULL-UP		SPI0_CS0			
VCC-PC	GPIO	P							
PD0	GPIO	I/O	DIS	Z	LCD_D0	LVDS0_VP0			
PD1	GPIO	I/O	DIS	Z	LCD_D1	LVDS0_VN0			
PD2	GPIO	I/O	DIS	Z	LCD_D2	LVDS0_VP1			
PD3	GPIO	I/O	DIS	Z	LCD_D3	LVDS0_VN1			
PD4	GPIO	I/O	DIS	Z	LCD_D4	LVDS0_VP2			
PD5	GPIO	I/O	DIS	Z	LCD_D5	LVDS0_VN2			
PD6	GPIO	I/O	DIS	Z	LCD_D6	LVDS0_VPC			
PD7	GPIO	I/O	DIS	Z	LCD_D7	LVDS0_VNC			
PD8	GPIO	I/O	DIS	Z	LCD_D8	LVDS0_VP3			
PD9	GPIO	I/O	DIS	Z	LCD_D9	LVDS0_VN3			
PD10	GPIO	I/O	DIS	Z	LCD_D10	LVDS1_VP0			
PD11	GPIO	I/O	DIS	Z	LCD_D11	LVDS1_VN0			
PD12	GPIO	I/O	DIS	Z	LCD_D12	LVDS1_VP1			
PD13	GPIO	I/O	DIS	Z	LCD_D13	LVDS1_VN1			
PD14	GPIO	I/O	DIS	Z	LCD_D14	LVDS1_VP2			
PD15	GPIO	I/O	DIS	Z	LCD_D15	LVDS1_VN2			
PD16	GPIO	I/O	DIS	Z	LCD_D16	LVDS1_VPC			
PD17	GPIO	I/O	DIS	Z	LCD_D17	LVDS1_VNC			
PD18	GPIO	I/O	DIS	Z	LCD_D18	LVDS1_VP3			
PD19	GPIO	I/O	DIS	Z	LCD_D19	LVDS1_VN3			
PD20	GPIO	I/O	DIS	Z	LCD_D20				
PD21	GPIO	I/O	DIS	Z	LCD_D21				
PD22	GPIO	I/O	DIS	Z	LCD_D22				
PD23	GPIO	I/O	DIS	Z	LCD_D23				
PD24	GPIO	I/O	DIS	Z	LCD_CLK				
PD25	GPIO	I/O	DIS	Z	LCD_DE				
PD26	GPIO	I/O	DIS	Z	LCD_HSYNC				
PD27	GPIO	I/O	DIS	Z	LCD_VSYNC				

VCC18-LVDS	GPIO	P							
VCC-PD	GPIO	P							
PE0	GPIO	I/O	DIS	Z	CSI_PCLK	TS_CLK			PE_EINT0
PE1	GPIO	I/O	DIS	Z	CSI_MCLK	TS_ERR			PE_EINT1
PE2	GPIO	I/O	DIS	Z	CSI_HSYNC	TS_SYNC			PE_EINT2
PE3	GPIO	I/O	DIS	Z	CSI_VSYNC	TS_DVLD			PE_EINT3
PE4	GPIO	I/O	DIS	Z	CSI_D0	SPI2_CS0	UART5_TX		PE_EINT4
PE5	GPIO	I/O	DIS	Z	CSI_D1	SPI2_CLK	UART5_RX		PE_EINT5
PE6	GPIO	I/O	DIS	Z	CSI_D2	SPI2_MOSI	UART5_RTS		PE_EINT6
PE7	GPIO	I/O	DIS	Z	CSI_D3	SPI2_MISO	UART5_CTS		PE_EINT7
PE8	GPIO	I/O	DIS	Z	CSI_D4	TS_D0			PE_EINT8
PE9	GPIO	I/O	DIS	Z	CSI_D5	TS_D1			PE_EINT9
PE10	GPIO	I/O	DIS	Z	CSI_D6	TS_D2			PE_EINT10
PE11	GPIO	I/O	DIS	Z	CSI_D7	TS_D3			PE_EINT11
PE12	GPIO	I/O	DIS	Z	CSI_D8	TS_D4			PE_EINT12
PE13	GPIO	I/O	DIS	Z	CSI_D9	TS_D5			PE_EINT13
PE14	GPIO	I/O	DIS	Z	CSI_D10	TS_D6			PE_EINT14
PE15	GPIO	I/O	DIS	Z	CSI_D11	TS_D7			PE_EINT15
PE16	GPIO	I/O	DIS	Z	CSI_SCK	TWI4_SCK			PE_EINT16
PE17	GPIO	I/O	DIS	Z	CSI_SDA	TWI4_SDA			PE_EINT17
VCC-PE	GPIO	P							
PF0	GPIO	I/O	DIS	Z	SDC0_D1				
PF1	GPIO	I/O	DIS	Z	SDC0_D0				
PF2	GPIO	I/O	DIS	Z	SDC0_CLK		UART0_TX		
PF3	GPIO	I/O	DIS	Z	SDC0_CMD				
PF4	GPIO	I/O	DIS	Z	SDC0_D3		UART0_RX		
PF5	GPIO	I/O	DIS	Z	SDC0_D2				
VCC-PF	GPIO	P							
PG0	GPIO	I/O	DIS	Z	SDC1_CLK				PG_EINT0
PG1	GPIO	I/O	DIS	Z	SDC1_CMD				PG_EINT1
PG2	GPIO	I/O	DIS	Z	SDC1_D0				PG_EINT2
PG3	GPIO	I/O	DIS	Z	SDC1_D1				PG_EINT3
PG4	GPIO	I/O	DIS	Z	SDC1_D2				PG_EINT4
PG5	GPIO	I/O	DIS	Z	SDC1_D3				PG_EINT5
PG6	GPIO	I/O	DIS	Z	UART2_TX				PG_EINT6
PG7	GPIO	I/O	DIS	Z	UART2_RX				PG_EINT7
PG8	GPIO	I/O	DIS	Z	UART2_RTS				PG_EINT8
PG9	GPIO	I/O	DIS	Z	UART2_CTS				PG_EINT9
PG10	GPIO	I/O	DIS	Z	TWI3_SCK				PG_EINT10
PG11	GPIO	I/O	DIS	Z	TWI3_SDA				PG_EINT11
PG12	GPIO	I/O	DIS	Z	UART4_TX				PG_EINT12
PG13	GPIO	I/O	DIS	Z	UART4_RX				PG_EINT13
PG14	GPIO	I/O	DIS	Z	UART4_RTS				PG_EINT14
PG15	GPIO	I/O	DIS	Z	UART4_CTS				PG_EINT15
VCC-PG	GPIO	P							
PH0	GPIO	I/O	DIS	Z	TWI0_SCK				

PH1	GPIO	I/O	DIS	Z	TWI0_SDA				
PH2	GPIO	I/O	DIS	Z	TWI1_SCK				
PH3	GPIO	I/O	DIS	Z	TWI1_SDA				
PH4	GPIO	I/O	DIS	Z	TWI2_SCK				
PH5	GPIO	I/O	DIS	Z	TWI2_SDA				
PH6	GPIO	I/O	DIS	Z	PWM0				
PH8	GPIO	I/O	DIS	Z		PWM1_P			PH_EINT8
PH9	GPIO	I/O	DIS	Z		PWM1_N			PH_EINT9
PH10	GPIO	I/O	DIS	Z		PWM2_P			PH_EINT10
PH11	GPIO	I/O	DIS	Z		PWM2_N			PH_EINT11
PH12	GPIO	I/O	DIS	Z	UART0_TX	SPI3_CS2			PH_EINT12
PH13	GPIO	I/O	DIS	Z	UART0_RX	SPI3_CS3			PH_EINT13
PH14	GPIO	I/O	DIS	Z	SPI3_CLK				PH_EINT14
PH15	GPIO	I/O	DIS	Z	SPI3_MOSI				PH_EINT15
PH16	GPIO	I/O	DIS	Z	SPI3_MISO				PH_EINT16
PH17	GPIO	I/O	DIS	Z	SPI3_CS0				PH_EINT17
PH18	GPIO	I/O	DIS	Z	SPI3_CS1				PH_EINT18
PH19	GPIO	I/O	DIS	Z	HSCL				
PH20	GPIO	I/O	DIS	Z	HSDA				
PH21	GPIO	I/O	DIS	Z	HCEC				
VCC-PH	GPIO	P							
PL0	GPIO	I/O	DIS	Z		S_UART_TX			S_PL_EINT0
PL1	GPIO	I/O	DIS	Z		S_UART_RX			S_PL_EINT1
PL2	GPIO	I/O	DIS	Z					S_PL_EINT2
PL3	GPIO	I/O	DIS	Z					S_PL_EINT3
PL4	GPIO	I/O	DIS	Z					S_PL_EINT4
PL5	GPIO	I/O	DIS	Z					S_PL_EINT5
PL6	GPIO	I/O	DIS	Z		S_CIR_RX			S_PL_EINT6
PL7	GPIO	I/O	DIS	Z		1WIRE			S_PL_EINT7
PL8	GPIO	I/O	DIS	Z		S_PS2_SCK1			S_PL_EINT8
PL9	GPIO	I/O	DIS	Z		S_PS2_SDA1			S_PL_EINT9
VCC-PL	GPIO	P							
PM0	GPIO	I/O	DIS	Z					S_PM_EINT0
PM1	GPIO	I/O	DIS	Z					S_PM_EINT1
PM2	GPIO	I/O	DIS	Z					S_PM_EINT2
PM3	GPIO	I/O	DIS	Z					S_PM_EINT3
PM4	GPIO	I/O	DIS	Z		S_I2S1_LRCKR			S_PM_EINT4
PM8	GPIO	I/O	DIS	Z		S_TWI1_SCK			S_PM_EINT8
PM9	GPIO	I/O	DIS	Z		S_TWI1_SDA			S_PM_EINT9
PM10	GPIO	I/O	DIS	Z	S_I2S_MCLK	S_I2S1_MCLK			
PM11	GPIO	I/O	DIS	Z	S_I2S_BCLK	S_I2S1_BCLK			
PM12	GPIO	I/O	DIS	Z	S_I2S_LRCK	S_I2S1_LRCK			
PM13	GPIO	I/O	DIS	Z	S_I2S_DIN	S_I2S1_DIN			
PM14	GPIO	I/O	DIS	Z	S_I2S_DOUT	S_I2S1_DOUT0			
PM15	GPIO	I/O	DIS	Z					S_PM_EINT15
VCC-PM	GPIO	P							
PN0	GPIO	I/O	DIS	PULL-UP	S_TWI0_SCK	S_RSB_SCK			

PN1	GPIO	I/O	DIS	PULL-UP	S_TWI0_SDA	S_RSB_SDA			

4.3. DETAILED PIN/SIGNAL DESCRIPTION

Pin/Signal	Description	Type
DRAM (x=0/1)		
SxDQ[31:0]	DRAM Data Bit [31:0]	I/O
SxVREF	DRAM Reference Input	P
SxDQS[3:0]	DRAM Data Strobe [3:0]	I/O
SxDQSB[3:0]	DRAM Data Strobe Negative [3:0]	I/O
SxDQM[3:0]	DRAM DQ Mask[3:0]	O
SxCK	DRAM Clock Positive	O
SxCKB	DRAM Clock Negative	O
SxCKE	DRAM Clock Enable	O
SxA[15:0]	DRAM Address[15:0]	O
SxBA[2:0]	DRAM Bank Address[2:0]	O
SxWE	DRAM Write Enable	O
SxCAS	DRAM Column Address Strobe	O
SxRAS	DRAM Row Address Strobe	O
SxCS	DRAM Chip Select	O
SxODT	DRAM ODT Control	O
SxZQ	DRAM ZQ Calibration	A
SxRST	DRAM Reset	O
VDD18-DLL	DLL Power Supply	P
VCC-DRAM	DRAM Power Supply	P
SYSTEM CONTROL		
NMI	Non-Maskable Interrupt Input	I
RESET	Reset Input	I
UBOOT	USB Boot Mode Enable	I
JTAGSEL[1:0]	JTAG Mode Select	I
BOOTSEL[1:0]	Boot Mode Select	I
VCC18-EFUSE	eFUSE power supply	P
INTERRUPT		
EINT	External Interrupt	I
PWM(x=0/1/2/3)		
PWM-P	PWM Output Positive	I
PWM-N	PWM Output Negative	I
CLOCK		
REXT	External Reference Resistor	A

Pin/Signal	Description	Type
VIO-RTC	Internal LDO Output	P
X32KI	Clock Input of 32768Hz Oscillator	A
X24MI	Clock Input of 24MHz Crystal	A
X24MO	Clock Output of 24MHz Crystal	A
VCC18-PLL	PLL Power Supply	P
GND-PLL	PLL Ground	G
CLK-OUT	Internal Clock Output	O
ECLK-IN[1:0]	External Clock Input	I
NAND FLASH		
NAND-DQ[7:0]	NAND Flash Data Bit[7:0]	I/O
NAND-CE[3:0]	NAND Flash Chip Select[3:0]	O
NAND-WE	NAND Flash Write Enable	O
NAND-ALE	NAND Flash Address Latch Enable	O
NAND-CLE	NAND Flash Command Latch Enable	O
NAND-RE	NAND Flash Read Enable	O
NAND-RB[1:0]	NAND Flash Ready/Busy Bit	I
NAND-DQS	NAND Flash Data Strobe	I/O
NAND-RE-B	NAND Flash RE Complementary Signal	O
NAND-DQS-B	NAND DQS Complementary Signal	I/O
LCD		
LCD-D[23:0]	LCD Data Bit[23:0]	O
LCD-CLK	LCD Clock Signal	O
LCD-DE	LCD Data Enable	O
LCD-HSYNC	LCD Horizontal SYNC	O
LCD-VSYNC	LCD Vertical SYNC	O
LVDS (x=0/1)		
LVDSx-VP[3:0]	LVDS Data Positive Signal Output[3:0]	A
LVDSx-VN[3:0]	LVDS Data Negative Signal Output[3:0]	A
LVDSx-VPC	LVDS Clock Positive Output	A
LVDSx-VNC	LVDS Clock Negative Output	A
MIPI		
MDSI-DN[3:0]	DSI Data Negative	A
DSI-DP[3:0]	DSI Data Positive	A
DSI-CKN	DSI Clock Negative	A
DSI-CKP	DSI Clock Positive	A
VCC18-MDSI	DSI Power Supply	P
GND-MDSI	MIPI DSI Ground	G
MCSI-DN[3:0]	CSI Data Negative	A
MCSI-DP[3:0]	CSI Data Positive	A
MCSI-CKN	CSI Clock Negative	A
MCSI-CKP	CSI Clock Positive	A
VCC18-MCSI	MIPI CSI Power Supply	P
GND-MCSI	MIPI CSI Ground	G
eDP		
EDPTXP[3:0]	eDP Data Transmit Positive [3:0]	A
EDPTXN[3:0]	eDP Data Transmit Negative [3:0]	A
EDPAUXP	eDP Auxiliary Positive	
EDPAUXN	eDP Auxiliary Negative	
EDPHPD	eDP Hot Plug Detection	
VCC18-EDP	eDP Power Supply	P
GND-EDP	eDP Ground	G
HDMI		
HTXP[2:0]	TMSD Data Positive	A
HTXN[2:0]	TMSD Data Negative	A
HTXCP	TMSD Clock Positive	A
HTXCN	TMSD Clock Negative	A

Pin/Signal	Description	Type
HHPD	HDMI Hot Plug Detection Signal	A
HSCL	HDMI DDC Clock	IO
HSDA	HDMI DDC Data	IO
HCEC	HDMI CEC	IO
VCC18-HDMI	HDMI Power Supply	P
VDD09-HDMI	HDMI Power Supply	p
GND-HDMI	HDMI Ground	G
CSI		
CSI-D[11:0]	CSI0 Data Bit[11:0]	I
CSI-PCLK	CSI Pixel Clock	I
CSI-MCLK	CSI Master Clock	O
CSI-SCK	CSI Command Serial Clock Signal	O
CSI-SDA	CSI Command Serial Data Signal	IO
CSI-HSYNC	CSI Horizontal SYNC	I
CSI-VSYNC	CSI Vertical SYNC	I
TRANSPORT STREAM		
TS-D[7:0]	Transport Stream Data[7:0]	I/O
TS-CLK	Transport Stream Clock	I/O
TS-ERR	Transport Stream Error Indicate	I/O
TS-SYNC	Transport Stream Sync	I/O
TS-DVLD	Transport Stream Valid Signal	I/O
USB		
USB0-DM	USB DM Signal	A
USB0-DP	USB DP Signal	A
USB0-ID	USB ID Signal	A
USB0-SSTXN	USB Super Speed Transmit Negative	A
USB0-SSTXP	USB Super Speed Transmit Positive	A
USB0-SSRXN	USB Super Speed Receive Negative	A
USB0-SSRXP	USB Super Speed Receive Positive	A
VCC33-USB0	USB Power Supply	P
VDD09-USB0	USB Power Supply	P
GND-USB0	USB Ground	G
USB0-VBUS	USB Power Detect Input	A
USB1-DM	USB DM Signal	A
USB1-DP	USB DP Signal	A
USB2-DM	USB DM Signal	A
USB2-DP	USB DP Signal	A
VCC33-USBH	USB Power Supply	P
VDD09-USBH	USB Power Supply	P
HSIC		
VCC12-HSIC	HSIC Power Supply	P
HSIC-STRB	USB HSIC Signal	A
HSIC-DATA	USB HSIC Data Signal	A
ADC		
GPADC[1:0]	GPADC Input	A
KEYADC[1:0]	Key ADC Input	A
VCC18-ADC	ADC Power Supply	P
GND-ADC	ADC Ground	G
I2S (x=0/1)		
S-I2Sx-LRCK	I2S Left/Right Channel Select Clock	I/O
S-I2Sx-MCLK	I2S Master Clock	I/O
S-I2Sx-BCLK	I2S Bit Clock	I/O
S-I2Sx-LRCKR	S-I2S-LRCK only for S-I2S-DIN	I/O
S-I2Sx-DIN	I2S Data Input	I/O
S-I2Sx-DOUT	I2S Data Output	I/O
SPI		

Pin/Signal	Description	Type
SPI-CS	SPI Chip Select Signal	I/O
SPI-CLK	SPI Clock Signal	I/O
SPI-MOSI	SPI Master Data Out, Slave Data In	I/O
SPI-MISO	SPI Master Data In, Slave Data Out	I/O
UART (x=0/1/2/3/4/5)		
UARTx-TX	UART Data Transmit	O
UARTx-RX	UART Data Receive	I
UARTx-RTS	UART Data Request to Send	O
UARTx-CTS	UART Data Clear to Send	I
UART1-DTR	UART Data Terminal Ready	O
UART1-DSR	UART Data Set Ready	I
UART1-DCD	UART Data Carrier Detect	I
UART1-RING	UART RING Indicator	I
1 WIRE		
1 WIRE	One Wire Signal	I/O
IR		
S-CIR-RX	CIR Signal Receive	I
PS2		
S-PS2-SCLK	PS2 Clock Signal	I/O
S-PS2-SDA	PS2 Data Signal	I/O
TWI (x=0/1/2/3/4)(Open-Drain)		
TWIx-SCK	TWI Clock Signal	I/O
TWIx-SDA	TWI Data Signal	I/O
SD/MMC (x=0/1/2)		
SDCx-D[3:0]	SD/MMC/SDIO Data Bit	I/O
SDCx-CLK	SD/MMC/SDIO Clock	O
SDCx-CMD	SD/MMC/SDIO Command Signal	I/O
ETHERNET MAC		
RGMII-RXD[3:0]	MII Receive Data Nible Data Bit [3:0]	I
RGMII-RXCK	MII Receive Clock	I
RGMII-RXCTL/MII-RXDV	MII Receive Control / EMAC Receive Data Valid	I
MII-RXERR	MII Receive Error	I
RGMII-TXD[3:0]	MII Transmit Data Nible Data Bit [3:0]	O
MII-CRS	MII Carrier Sense	I
RGMII-TXCK/MII-TXCK	MII Transmit Clock	O
RGMII-TXCTL/MII-TXEN	MII Transmit Control / MII Transmit Enable	O
MII-TXERR	MII Transmit Error	O
RGMII-CLKIN/MII-COL	MII Clock Input / EMAC Collision Detect	I
EMDC	MII Management Data Clock	O
EMDIO	MII Management Data Input/Output	I/O
RSB		
S-RSB-SCK	RSB Clock	O
S-RSB-SDA	RSB Data	I/O
POWER		
VDD18	Power	P
VDD-CPUS	Power Supply for CPUS	P
VDD-CPUB	Power Supply for Cluster B	P
VDD-CPUA	Power Supply for Cluster A	P
VDD-GPU	Power Supply for GPU	P
VDD-SYS	Power Supply for System	P
VDD-VPU	Power Supply for VPU	P
GND-IO	IO Ground	G
GND	Ground	G

5 ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

SYMBOL	PARAMETER		MIN	MAX	UNIT
T_g	Storage Temperature		-65	150	°C
$I_{I/O}$	In/Out current for input and output		-	-	mA
V_{ESD}	ESD stress voltage	HBM(human body model)	-	-	V_{ESD}
		CDM(charged device model)	NA	NA	
T_J	Junction Temperature		-	125	°C
VCC-DRAM	Power Supply for DRAM		-0.3	1.65	V
VDD18-DLL	Power Supply for DLL		-0.3	1.98	V
VCC-PA	Power Supply for GPIO Port A		-0.3	3.6	V
VCC-PB	Power Supply for GPIO Port B		-0.3	3.6	V
VCC-PC	Power Supply for GPIO Port C		-0.3	3.6	V
VCC-PD	Power Supply for GPIO Port D		-0.3	3.6	V
VCC-PE	Power Supply for GPIO Port E		-0.3	3.6	V
VCC-PF	Power Supply for GPIO Port F		-0.3	3.6	V
VCC-PG	Power Supply for GPIO Port G		-0.3	3.6	V
VCC-PH	Power Supply for GPIO Port H		-0.3	3.6	V
VCC-PL	Power Supply for GPIO Port L		-0.3	3.6	V
VCC-PM	Power Supply for GPIO Port M		-0.3	3.6	V
VCC18-EFUSE	Power Supply for EFUSE		-0.3	1.98	V
VCC33-USB0	Power Supply for USB		-0.3	3.6	V
VDD09-USB0	Power Supply for USB		-0.3	1.1	V
VCC33-USBH	Power Supply for USB		-0.3	3.6	V
VDD09-USBH	Power Supply for USB		-0.3	1.1	V
VCC12-HSIC	Power Supply for HSIC		-0.3	1.32	V
VCC18-ADC	Power Supply for ADC		-0.3	1.98	V
VCC18-HDMI	Power Supply for HDMI		-0.3	1.98	V
VDD09-HDMI	Power Supply for HDMI		-0.3	1.1	V
VCC18-EDP	Power Supply for EDP		-0.3	1.98	V
VCC18-MDSI	Power Supply for MDSI		-0.3	1.98	V

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC18-MCSI	Power Supply for MCSI	-0.3	1.98	V
VCC18-LVDS	Power Supply for LVDS	-0.3	1.98	V
VCC18-PLL	Power Supply for PLL	-0.3	1.98	V
VDD18	Power Supply	-0.3	1.98	V
VDD-CPUS	Power Supply for CPUS	-0.3	1.1	V
VDD-CPUB	Power Supply for CPUB	-0.3	1.1	V
VDD-CPUA	Power Supply for CPUA	-0.3	1.1	V
VDD-GPU	Power Supply for GPU	-0.3	1.1	V
VDD-SYS	Power Supply for System	-0.3	1.1	V
VDD-VPU	Power Supply for VPU	-0.3	1.1	V

5.2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_a	Ambient Operating Temperature[Commercial]	-20	-	70	°C
GND	Ground	0	0	0	V
VCC-DRAM	Power Supply for DRAM	1.2	NA	1.65	V
VDD18-DLL	Power Supply for DLL	1.62	1.8	1.98	V
VCC-PA	Power Supply for Port A	1.8	NA	3.6	V
VCC-PB	Power Supply for Port B	1.8	NA	3.6	V
VCC-PC	Power Supply for Port C	1.8	NA	3.6	V
VCC-PD	Power Supply for Port D	1.8	NA	3.6	V
VCC-PE	Power Supply for Port E	1.8	NA	3.6	V
VCC-PF	Power Supply for Port F	1.8	NA	3.6	V
VCC-PG	Power Supply for Port G	1.8	NA	3.6	V
VCC-PH	Power Supply for Port H	1.8	NA	3.6	V
VCC-PL	Power Supply for Port L	1.8	NA	3.6	V
VCC-PM	Power Supply for Port M	1.8	NA	3.6	V
VCC18-EFUSE	Power Supply for EFUSE	1.62	1.8	1.98	V
VCC33-USB0	Power Supply for USB	3.0	-	3.6	V
VDD09-USB0	Power Supply for USB	0.8	0.9	1.1	V
VCC33-USBH	Power Supply for USB	3.0	-	3.6	V
VDD09-USBH	Power Supply for USB	0.8	0.9	1.1	V
VCC12-HSIC	Power Supply for HSIC	1.08	1.2	1.32	V
VCC18-ADC	Power Supply for ADC	1.62	1.8	1.98	V
VCC18-HDMI	Power Supply for HDMI	1.62	1.8	1.98	V
VDD09-HDMI	Power Supply for HDMI	0.8	0.9	1.1	V
VCC18-EDP	Power Supply for eDP	1.62	1.8	1.98	V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC18-MDSI	Power Supply for MDSI	1.62	1.8	1.98	V
VCC18-MCSI	Power Supply for MCSI	1.62	1.8	1.98	V
VCC18-LVDS	Power Supply for LVDS	1.62	1.8	1.98	V
VCC18-PLL	Power Supply for PLL	1.62	1.8	1.98	V
VDD18	Power Supply	1.62	1.8	1.98	V
VDD-CPUS	Power Supply for CPUS	0.8	0.9	1.1	V
VDD-CPUB	Power Supply for Cluster B	0.8	0.9	1.1	V
VDD-CPUA	Power Supply for Cluster A	0.8	0.9	1.1	V
VDD-GPU	Power Supply for GPU	0.8	0.9	1.1	V
VDD-SYS	Power Supply for System	0.8	0.9	1.1	V
VDD-VPU	Power Supply for VPU	0.8	0.9	1.1	V

5.3. DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage	VCC-IO[1]=3.0V	2.4	-	3.6	V
		VCC-IO = 1.8V	1.1	-	1.98	V
V_{IL}	Low-Level Input Voltage	VCC-IO=3.0V	-0.3	-	0.7	V
		VCC-IO = 1.8V	-0.3	-	0.7	V
V_{HYS}	Hysteresis Voltage	-	-	-	-	mV
I_{IH}	High-Level Input Current	VCC-IO=3.0V, VI=3.0V	TBD	TBD	TBD	uA
		VCC-IO = 1.8V	TBD	TBD	TBD	uA
I_{IL}	Low-Level Input Current	VCC-IO=3.0V, VI=0V	TBD	TBD	TBD	uA
		VCC-IO = 1.8V	TBD	TBD	TBD	uA
V_{OH}	High-Level Output Voltage	VCC-IO=3.0V	2.7	-	NA	V
		VCC-IO = 1.8V	1.5	-	NA	V
V_{OL}	Low-Level Output Voltage	VCC-IO=3.0V	NA	-	0.4	V
		VCC-IO = 1.8V	NA	-	0.4	V
I_{OZ}	Tri-State Output Leakage Current	VCC-IO=3.0V	TBD	TBD	TBD	uA
		VCC-IO = 1.8V	TBD	TBD	TBD	uA
C_{IN}	Input Capacitance	-	NA	NA	5	pF
C_{OUT}	Output Capacitance	-	NA	NA	5	pF

Notes: VCC-IO here refers to the power supply for all GPIOs, including VCC-PA, VCC-PB, VCC-PC, VCC-PD, VCC-PE, VCC-PF, VCC-PG, VCC-PH, VCC-PL, VCC-PM.

5.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

The A80 contains a 24MHz oscillator and a 32K clock input.

5.4.1. 24MHz OSCILLATOR CHARACTERISTICS

The 24MHz crystal is connected between the X24MI and X24MO.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
1/(tCPMAIN)	Crystal Oscillator Frequency Range	-	24	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25°C	-50	-	50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	50	ppm
PON	Drive Level	-	-	50	uW
CL	Equivalent Load Capacitance	-	-	-	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	-	-	-	pF
RS	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
CM	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

5.4.2. 32KHZ CLOCK CHARACTERISTICS

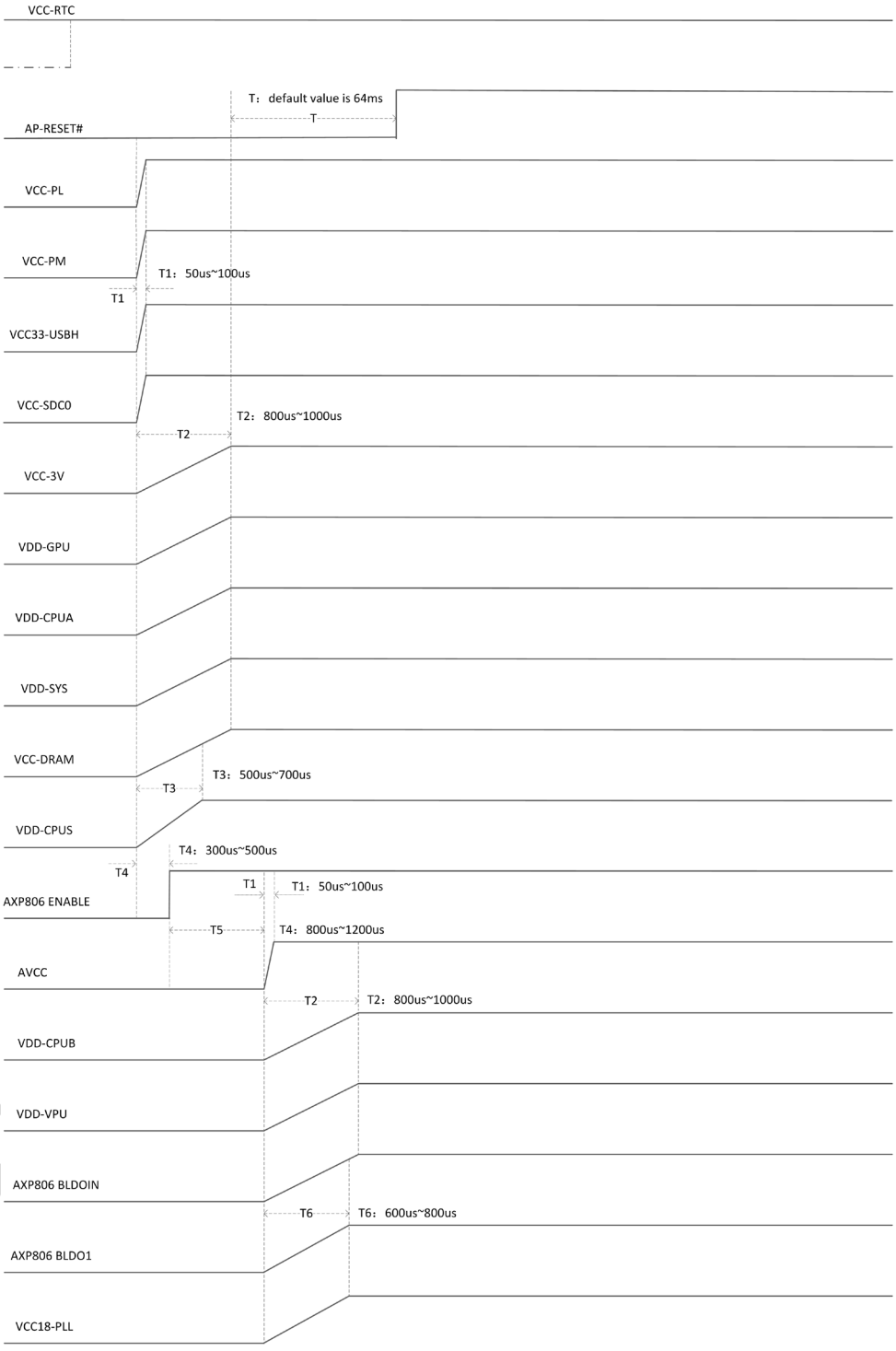
The 32KHz clock is connected to X32KI (input).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Voltage Input	1.2	-	1.8	V
V_{IL}	Low-Level Voltage Input	0	-	0.4	V
	Frequency Range	20	32	50	kHz
	Duty Cycle	30	50	70	%

5.5. POWER UP/DOWN SEQUENCE

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.

Power On Timing

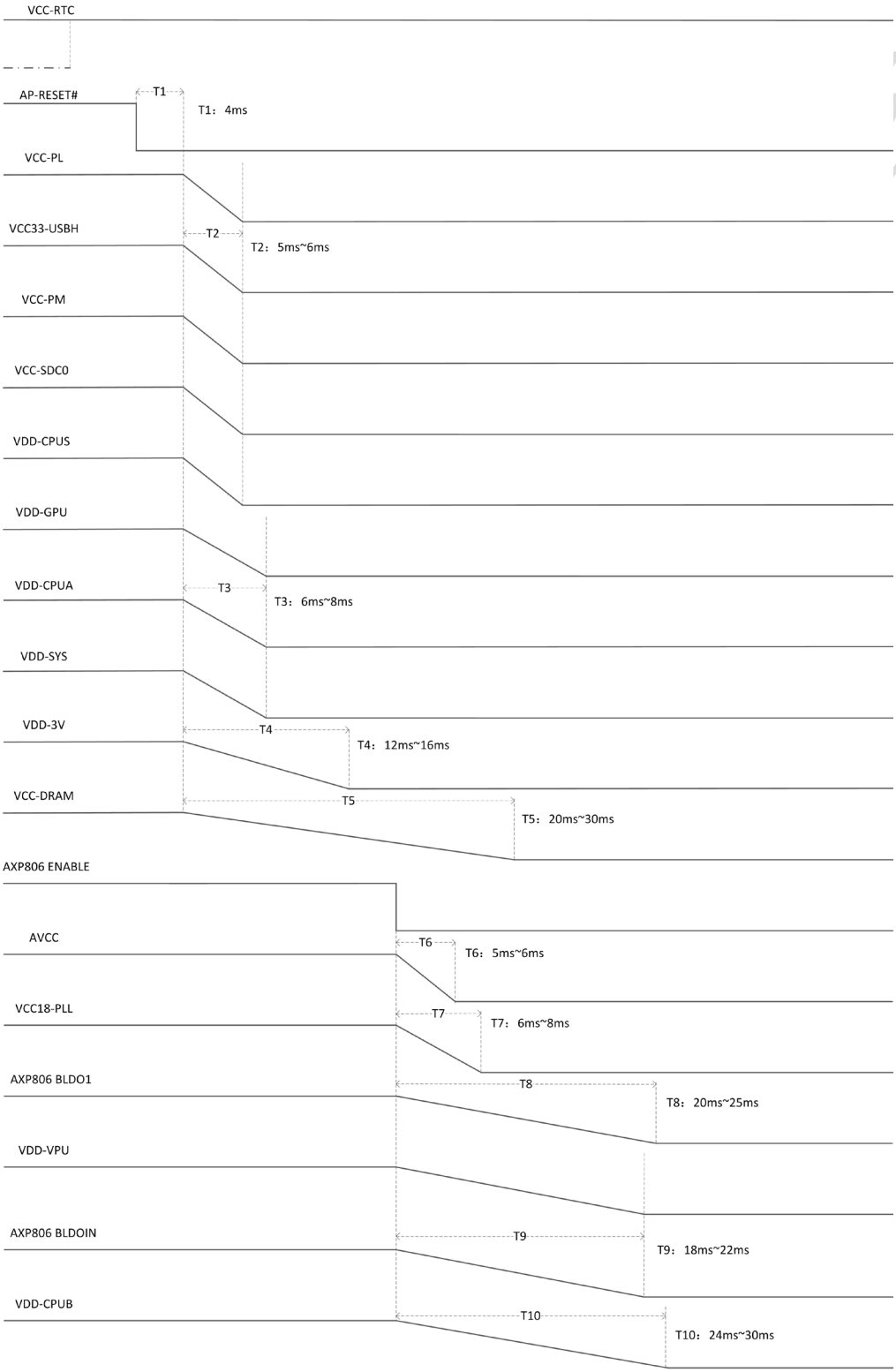


1) when VCC-DRAM is above 0.6V, AXP806 enable signal is valid.

2) AXP806 BLDO1 is for VCC18-EFUSE/VCC18-ADC/VCC18-EDP/VCC18-HDMI/VCC18-DSI/VCC18-CSI2/VCC18-LVDS/VCC18-NAND

3)T is deFault to be 64ms, which can also be modified into 8ms, 16ms, 32ms, 64ms after system power on. The default value is recommended.

Power Down Timing



1） when AXP809 receives the power off source, the AP-REET# will be pulled down through PWROK pin, and all AXP809 outputs will be disabled after 4mS delay；

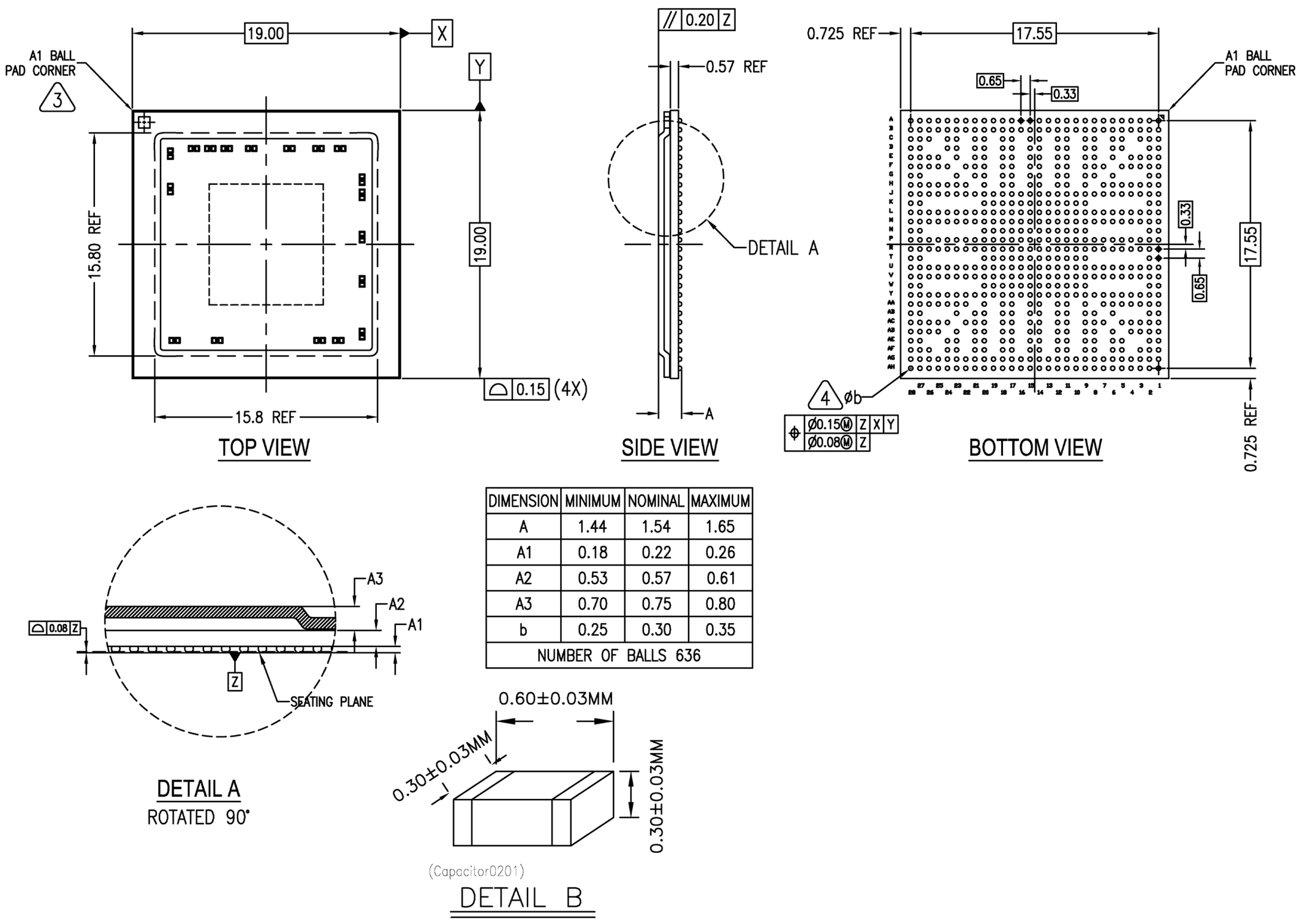
2) when VCC-DRAM is lower than 0.5V, AXP806 will detect power off signal from EN/PWRON pin, and then disable each output.

6 PIN ASSIGNMENT

6.1. PIN MAP

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	GND	S0DQ30	S0DQ31	PG1	PG5	PG9	PG11	PC8	PC9	PC11	PC17	PD3	PD5	PD9	PD15	PD17	PD19	EDPD1P	EDPD2P	EDPAUXP	UBOOT	X24MI	PN1	X32KI	PM1	PM3	PM10	GND	A
B	S0DQ28	S0DQ29	S0ZQ	PG0	PG4	PG8	PG10	PG15	PC6	PC10	PC16	PD2	PD4	PD8	PD14	PD16	PD18	EDPD1N	EDPD2N	EDPAUXN	KeyADC1	X24MO	PN0	PM0	PM2	PM8	PM9	PM11	B
C	S0DQS3B	S0DQS3	GND		PG3	GND		GND	PC5		GND	GND		GND	VCC18-LVDS		PD20	EDPD0N		GND	GND-ADC		GND-PLL	NMI		RESET	PM12	PM13	C
D	S0DQ26	S0DQ27			PG7	PG2		PG14	PC4		PC15	PD0		PD7	PD12		PD21	EDPD0P		EDPD3P	VCC18-ADC		VCC18-PLL	VCC-PM			PM14	PM15	D
E	S0DQ24	S0DQ25	GND	S0BA0		PG6		PG13	PC3		PC14	PD1		PD6	PD13		GND-EDP	VCC18-EDP		EDPD3N	KeyADC0		PL3		PM4	PL2	PL1	PL0	E
F	S0DQ15	S0DQM3	S0A6	S0A9	VCC-DRAM		VCC-PG	VCC-PG	VCC-PC		VCC-PC	VCC-PD		VCC-PD	VCC-PD		PD22	PD25		EDPHPD	REXT	PL8		VCC-PL	PL4	PL5	PL6	PL7	F
G	S0DQ13	S0DQ14				GND		PG12	PC2		PC7	PC13		PC19	PD10		PD23	PD26		GPADC0	VIO-RTC		PL9				HTX2N	HTX2P	G
H	S0DQS1	S0DQ12	GND	S0BA2	S0WE	VCC-DRAM	S0RAS		PC1		PC0	PC12		PC18	PD11		PD24	PD27		GPADC1		JTAGSEL1	JTAGSEL0	GND-HDMI	MDSI-CKP	MDSI-CKN	HTX1N	HTX1P	H
J	S0DQ11	S0DQS1B	S0A5	S0A13	VCC-DRAM	S0ODT1	S0ODT	GND	GND	GND	GND	GND	GND	VDDFB-CPUB	GND	VDD-SYS	VDD-SYS	VDD-SYS	GND	VCC18-EFUSE	MDSI-DM3	MDSI-DP3	VCC18-MDSI	VCC18-HDMI	MDSI-DM1	MDSI-DP1	HTX0N	HTX0P	J
K	S0DQ10	S0DQ9							GND	GND	VDD-CPUB	VDD-CPUB	VDD-CPUB	GNDFB-CPUB	VDD-CPUB	GND	VDD-SYS	GND	VDD-CPUS	VDD-CPUS							HTXCN	HTXCP	K
L	S0DQM1	S0DQ8	GND	S0A7	S0A8	VCC-DRAM	S0CAS	S0RST	GND	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	GND	VDD-SYS	VDD-SYS	GND	VDD-CPUS	MDSI-DP2	MDSI-DM2	GND-MDSI	VDD09-HDMI	HHPD	GND	NC	NC	L
M	S0CK1	S0CK1B	S0VREF	S0A4	VCC-DRAM	S0CS1	S0CS	GND	GND	VDD-CPUB	GND	GND	VDD-CPUB	VDD-CPUB	VDD-CPUB	GND	VDD-SYS	VDD-SYS	GND	VDD18	MDSI-DM0	MDSI-DP0	NC	VDD09-USB0	NC	VCC33-USB0	NC	NC	M
N	S0CK	S0CKB							GND	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	GND	VDD-SYS	VDD-SYS	GND	VDD18							USB0-SSRXN	USB0-SSRXP	N
P	S0DQ6	S0DQ7	GND	S0A15	S0A3	VCC-DRAM	S0A14	S0A12	GND	GND	VDD-CPUB	VDD-CPUB	VDD-CPUB	VDD-CPUB	GND	GND	GND	GND	GND	VDD18	USB0-VBUS	USB0-ID	VDD09-USBH	USB2-DM	USB2-DP	GND-USB0	USB0-SSTXN	USB0-SSTXP	P
R	S0DQ4	S0DQ5	S0A0	S0A10	VCC-DRAM	S0A1	S0A11	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD-CPUA	VDD-CPUA	GND	GND	PE13	PE9	VDD09-USBH	USB1-DP	USB1-DM	VCC33-USBH	USB0-DM	USB0-DP	R
T	S0DQS0B	S0DQS0							VDDFB-GPU	GND	VDD-GPU	VDD-GPU	VDD-GPU	VDD-GPU	GND	VDD-CPUA	VDD-CPUA	VDD-CPUA	VDD-CPUA	VDDFB-CPUA							HSIC-STRB	HSIC-DATA	T
U	S0DQ2	S0DQ3	GND	S0CKE	S0CKE1	VCC-DRAM	S0A2	S0BA1	GND	GND	VDD-GPU	VDD-GPU	GND	VDD-GPU	GND	VDD-CPUA	VDD-CPUA	VDD-CPUA	VDD-CPUA	GND	PE16	VCC12-HSIC	VCC18-MCSI	MCSI-DP3	MCSI-DM3	GND-MCSI	MCSI-DP2	MCSI-DM2	U
V	S0DQ0	S0DQ1	S1ZQ	S1ODT1	VCC-DRAM	S1ODT	S1RAS	GND	GND	GND	VDD-GPU	VDD-GPU	VDD-GPU	VDD-GPU	GND	GND	GND	GND	GND	GND	PE17	PE12	PE8	PE7	PE4	PE2	MCSI-CKP	MCSI-CKN	V
W	S0DQ23	S0DQM0							GND	GND	GND	GND	GND	GND	GND	VDD-VPU	VDD-VPU	VDD-VPU	VDD-VPU	VDD-VPU							MCSI-DP1	MCSI-DM1	W
Y	S0DQ21	S0DQ22	GND	S1CAS	S1WE	VCC-DRAM	GND	VDD18-DLL	VDD18-DLL	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PF3	PE15	PE10	VCC-PE	PE5	PE3	MCSI-DP0	MCSI-DM0	Y
AA	S0DQS2	S0DQ20	S1BA0	S1BA2	VCC-DRAM	S1A13	GND		VDD18-DLL		GND	S1A14		GND	S1RST		GND	PB16		PF2		PE14	PE11	VCC-PE	PE6	GND	PE0	PE1	AA
AB	S0DQ19	S0DQS2B				VCC-DRAM		VDD18-DLL	GND		S1A11	S1DQ16		S1BA1	GND		S1DQM2	PB15		PF1	PF0		PA5				PH1	PH0	AB
AC	S0DQ17	S0DQ18	GND	S1A9	S1A8		VCC-DRAM	S1A4	VCC-DRAM		S1A12	VCC-DRAM		S1A15	VCC-DRAM		S1DQ19	VCC-PB		PA17	PA8	VCC-PA		GND	PH5	PH4	PH3	PH2	AC
AD	S0DQM2	S0DQ16	S1VREF	S1A7		S1CKE		VCC-DRAM	S1A2		VCC-DRAM	S1DQ18		VCC-DRAM	S1DQ17		VCC-DRAM	PB5		VCC-PA	PA9		PA4		VCC-PH	PH9	PH8	PH6	AD
AE	S1DQ30	S1DQ31			S1A6	S1CKE1		S1CS1	S1A3		S1A0	S1DQ20		S1A10	S1DQS2		S1DQ21	VCC-PF		PA13	PA10		PA0	VCC-PH			PH11	PH10	AE
AF	S1DQ28	S1DQ29	GND		S1A5	GND		S1CS	GND		S1A1	GND		S1DQ23	S1DQS2B		S1DQ22	GND		PA14	GND		PA1	PH21		GND	PH13	PH12	AF
AG	S1DQS3	S1DQS3B	S1DQ26	S1DQ24	S1DQ14	S1DQ13	S1DQS1	S1DQ11	S1DQ9	S1DQM1	S1CK1B	S1CKB	S1DQ5	S1DQ7	S1DQS0B	S1DQ0	S1DQ1	PB6	PF4	PA15	PA11	PA6	PA2	BOOTSEL0	PH19	PH17	PH15	PH14	AG
AH	GND	S1DQ27	S1DQ25	S1DQM3	S1DQ15	S1DQ12	S1DQS1B	S1DQ10	S1DQ8	S1CK1	S1CK	S1DQ6	S1DQ4	S1DQS0	S1DQ3	S1DQ2	S1DQM0	PB14	PF5	PA16	PA12	PA7	PA3	BOOTSEL1	PH20	PH18	PH16	GND	AH
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

6.2. PACKAGE DIMENSION



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.44	1.54	1.65
A1	0.18	0.22	0.26
A2	0.53	0.57	0.61
A3	0.70	0.75	0.80
b	0.25	0.30	0.35
NUMBER OF BALLS 636			

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