A33 Nand Flash Controller Specification

Revision 1.0

Feb.28,2014

DECLARATION

Revision History

Version	Date	Author	Reviewer	Description
1.0	Feb.28, 2014			

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1. NAND Flash Controller

1.1. NDFC Overview

The NDFC is the NAND Flash Controller which supports all NAND/MLC flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kinds of modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NDFC includes the following features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Supports 8-bit data bus width
- Supports 1024, 2048, 4096, 8192, 16384 bytes size per page
- Supports 3.3V voltage supply Flash
- Supports conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code can correct up to 64 bits per 512 or 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NDFC status information is reported by its' registers and interrupt is supported
- One Command FIFO
- External DMA is supported for transferring data
- Two 256x32-bit RAM for Pipeline procession
- Supports SDR, DDR and Toggle NAND
- Supports self –debug for NDFC debug

The system block diagram of the NDFC is shown as follows.

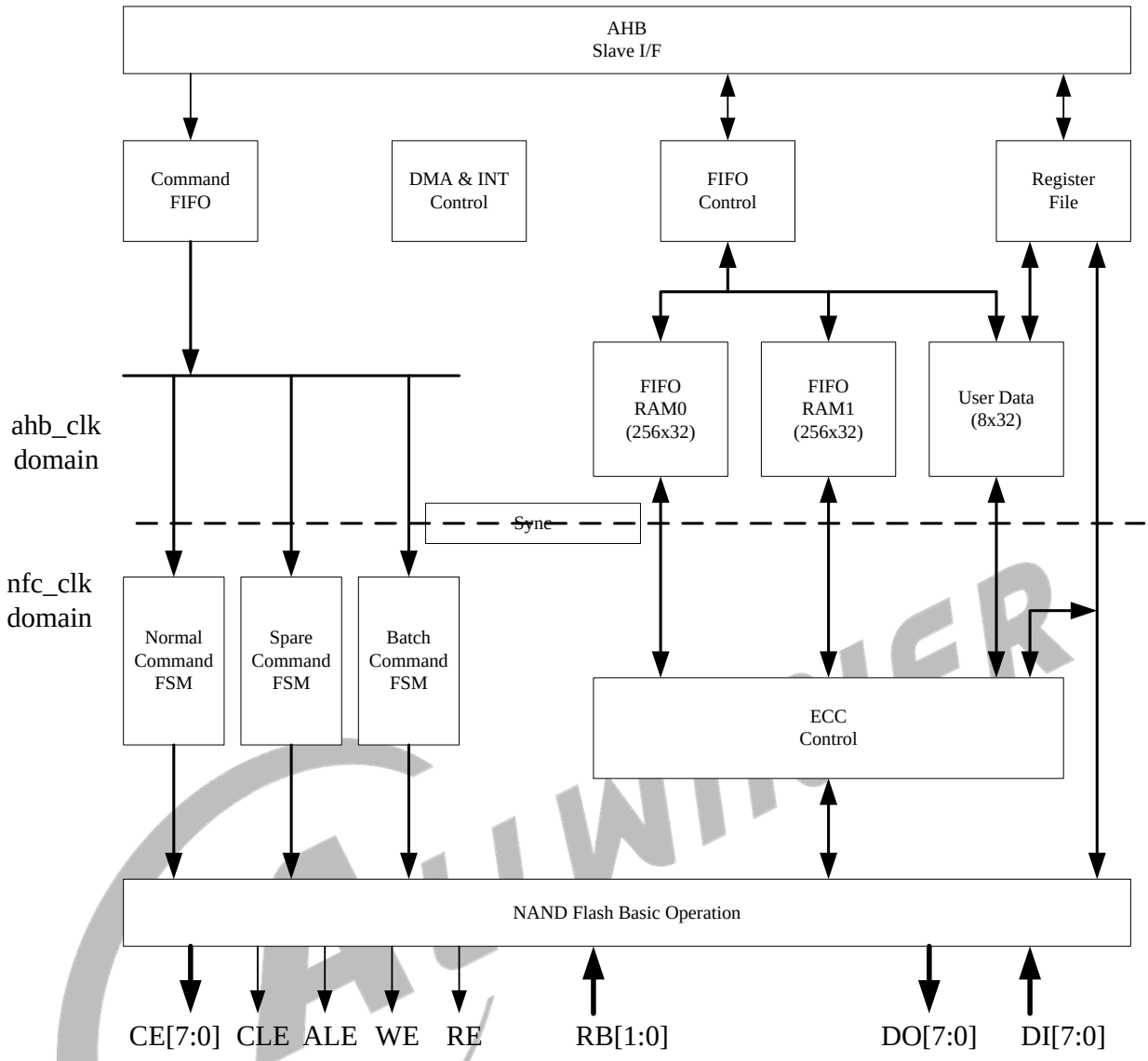

Figure 1. NDFC Block Diagram

1.2. NDFC Timing Diagram

Typically, there are two kinds of serial access method. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.

Conventional Serial Access after Read Cycle (SAM0):

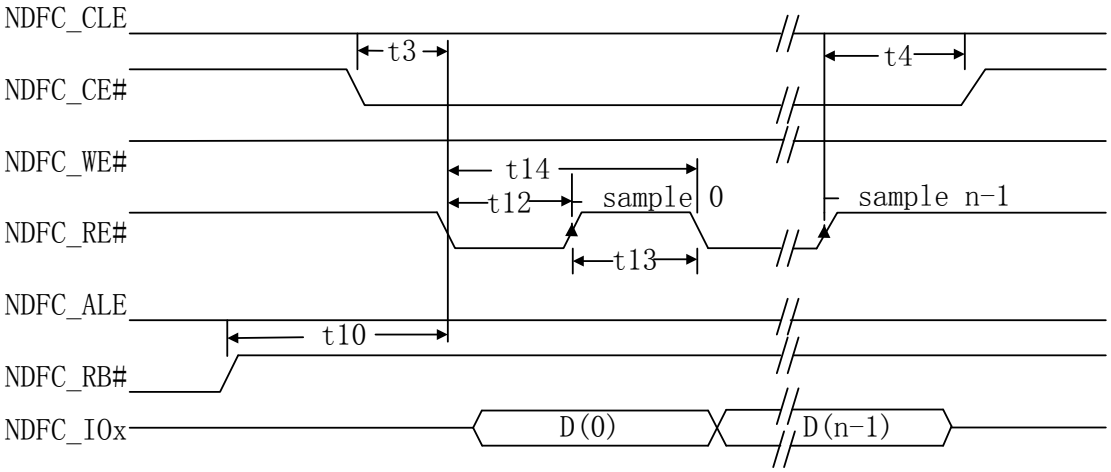

Figure 2. Conventional Serial Access Cycle Diagram (SAM0)

EDO type Serial Access after Read Cycle (SAM1):

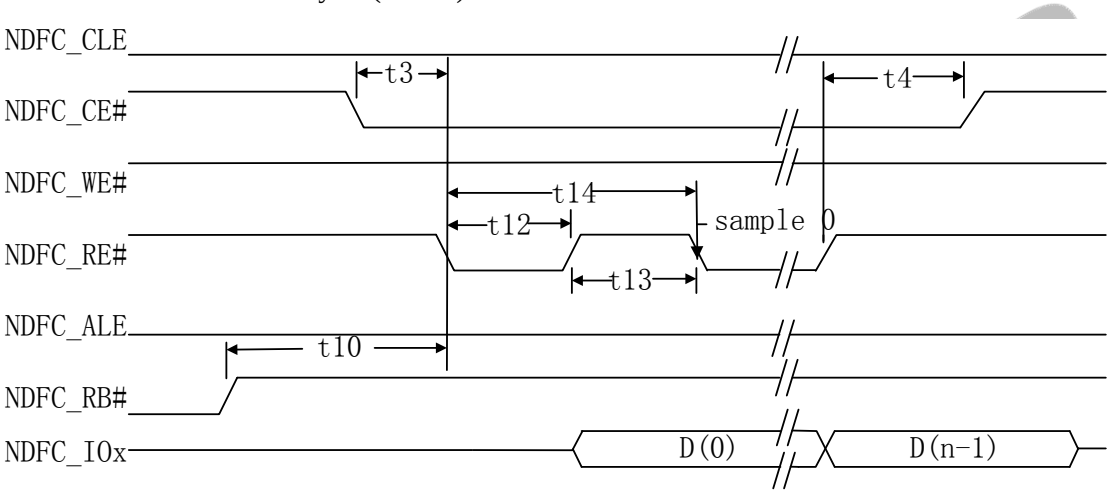

Figure 3. EDO type Serial Access after Read Cycle (SAM1)

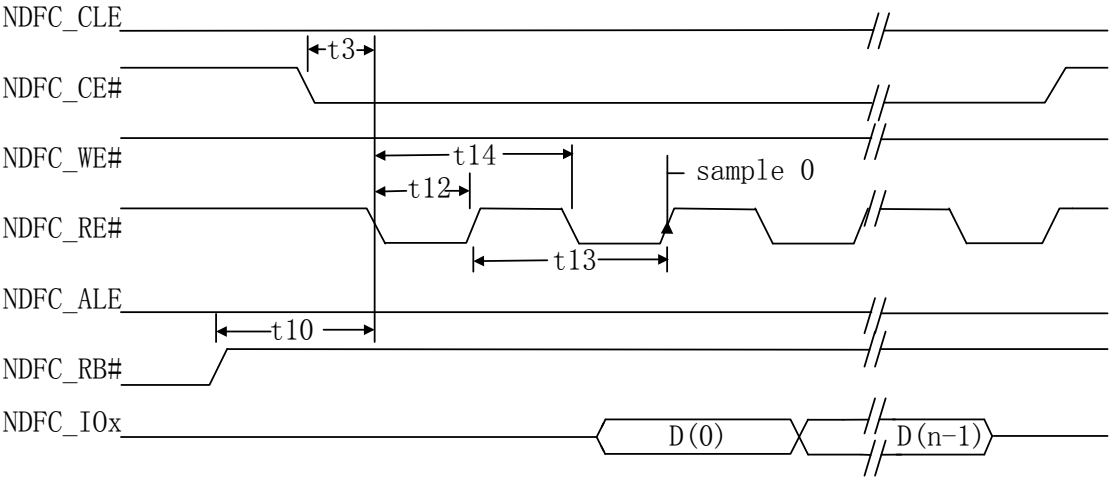

Figure 4. Extending EDO type Serial Access Mode (SAM2)

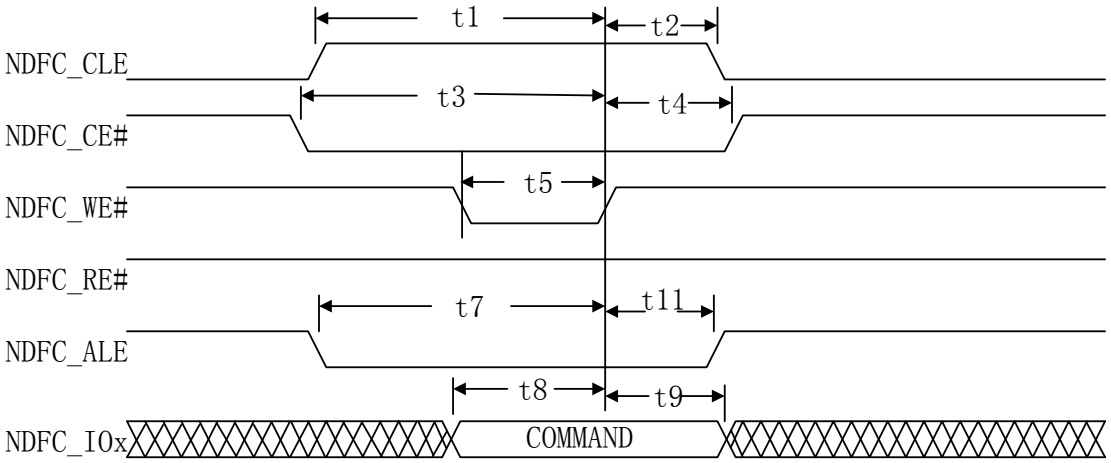

Figure 5. Command Latch Cycle

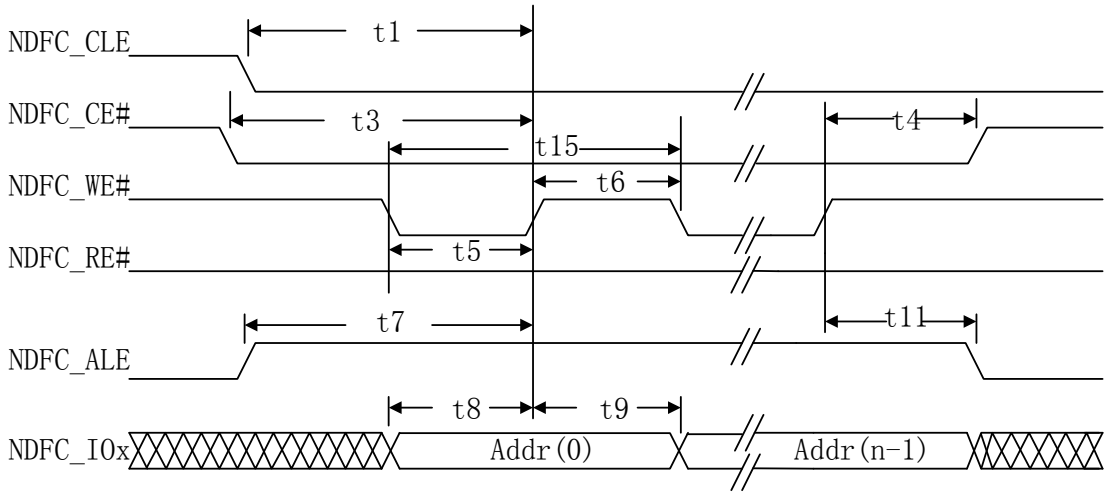

Figure 6. Address Latch Cycle

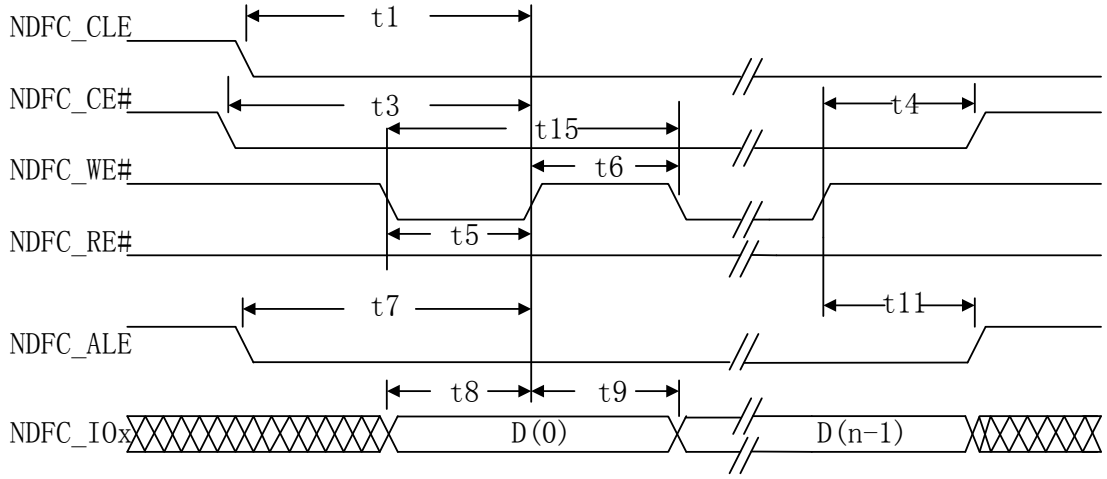

Figure 7. Write Data to Flash Cycle

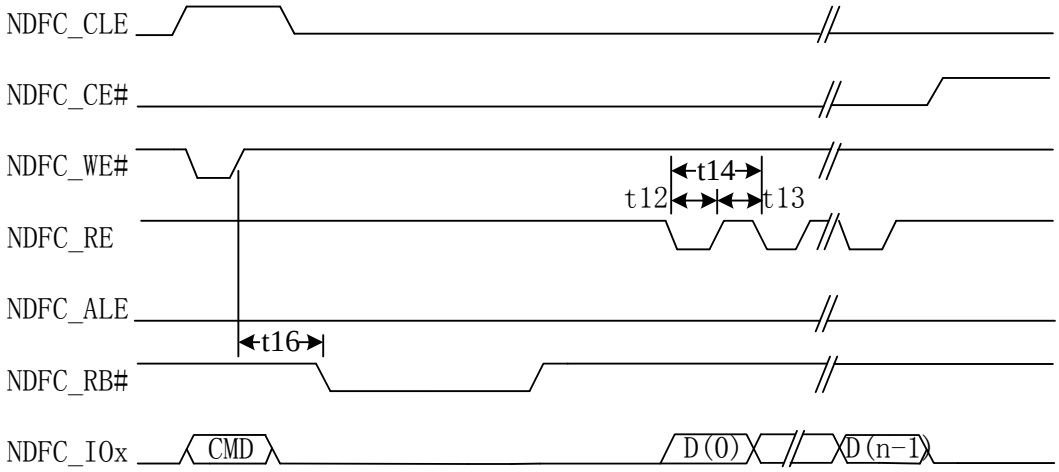

Figure 8. Waiting R/B# ready Diagram

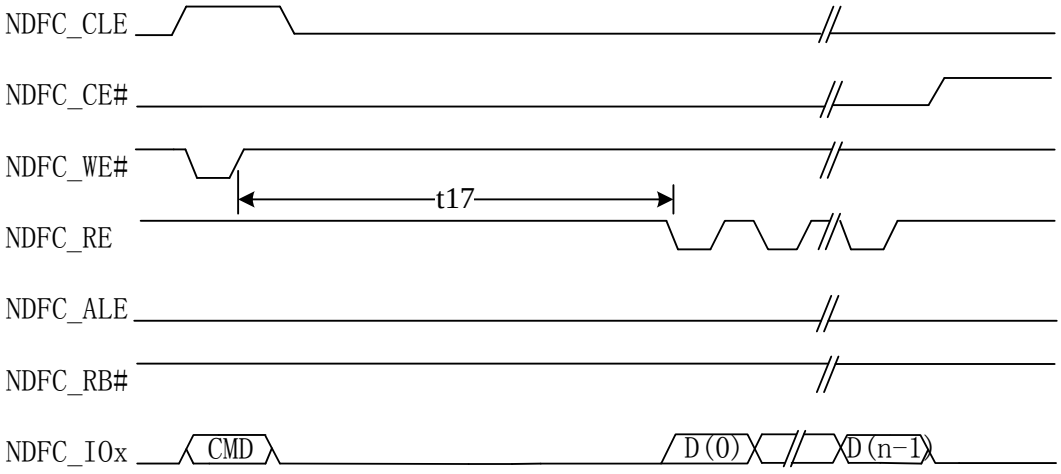

Figure 9. WE# high to RE# low Timing Diagram

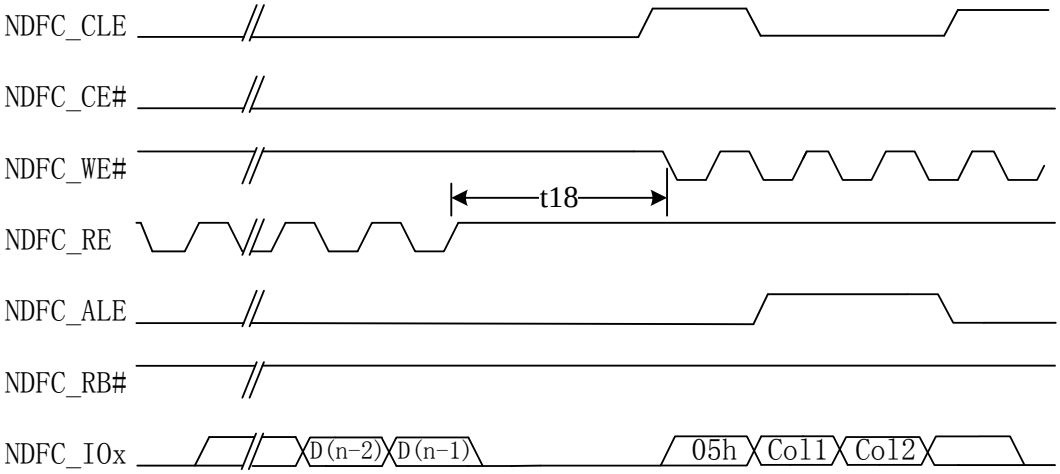

Figure 10. RE# high to WE# low Timing Diagram

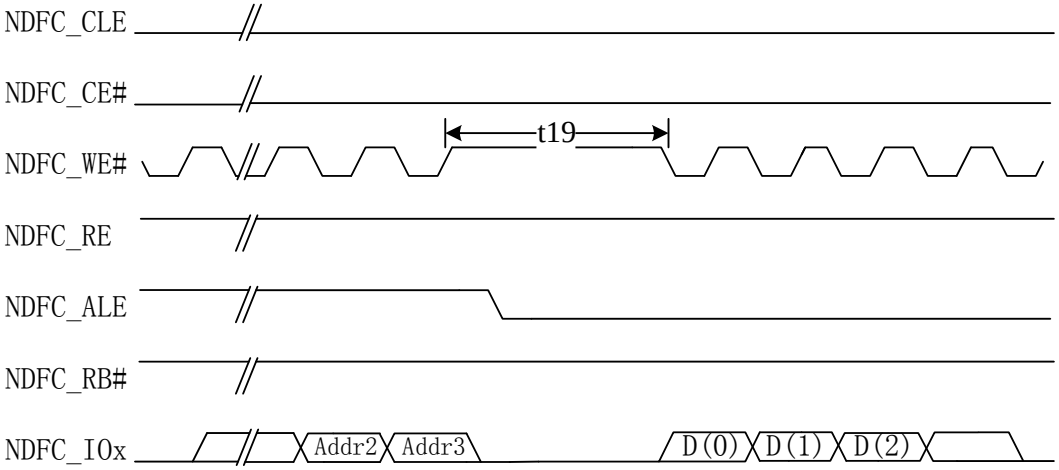

Figure 11. Address to Data Loading Timing Diagram

Timing cycle list:

ID	Parameter	Timing	Notes
T1	NDFC_CLE setup time	2T	
T2	NDFC_CLE hold time	2T	
T3	NDFC_CE setup time	2T	
T4	NDFC_CE hold time	2T	
T5	NDFC_WE# pulse width	T	
T6	NDFC_WE# hold time	T	
T7	NDFC_ALE setup time	2T	
T8	Data setup time	T	
T9	Data hold time	T	
T10	Ready to NDFC_RE# low	3T	
T11	NDFC_ALE hold time	2T	
T12	NDFC_RE# pulse width	T	
T13	NDFC_RE# hold time	T	
T14	Read cycle time	2T	
T15	Write cycle time	2T	
T16	NDFC_WE# high to R/B# busy	tWB	Specified by timing configure register (NDFC_TIMING_CFG)
T17	NDFC_WE# high to NDFC_RE# low	tWHR	Specified by timing configure register (NDFC_TIMING_CFG)
T18	NDFC_RE# high to NDFC_WE# low	tRHW	Specified by timing configure register (NDFC_TIMING_CFG)
T19	Address to Data Loading time	tADL	Specified by timing configure register (NDFC_TIMING_CFG)

Notes: T is the cycle of internal clock.

1.3. NDFC Register List

Module Name	Base Address
NDFC	0x01C03000

Register Name	Offset	Description
NDFC_CTL	0x00	NDFC Configure and Control
NDFC_ST	0x04	NDFC Status Information
NDFC_INT	0x08	NDFC Interrupt Control
NDFC_TIMING_CTL	0x0C	NDFC Timing Control
NDFC_TIMING_CFG	0x10	NDFC Timing Configure
NDFC_ADDR_LOW	0x14	NDFC Low Word Address
NDFC_ADDR_HIGH	0x18	NDFC High Word Address
NDFC_BLOCK_NUM	0x1C	NDFC Data Block Number
NDFC_CNT	0x20	NDFC Data Counter for Data Transfer
NDFC_CMD	0x24	Set up NDFC Commands
NDFC_RCMD_SET	0x28	Read Command Set for Vendor's NAND Memory
NDFC_WCMD_SET	0x2C	Write Command Set for Vendor's NAND Memory
NDFC_ECC_CTL	0x34	ECC Configure and Control
NDFC_ECC_ST	0x38	ECC Status and Operation Information
NDFC_EFR	0x3C	Enhanced Feature Register
NDFC_ERR_CNT0	0x40	Corrected Error Bit Counter0
NDFC_ERR_CNT1	0x44	Corrected Error Bit Counter1
NDFC_USER_DATAn	0x50+4*n	User Data Field Register n (n from 0 to 15)
NDFC_EFNAND_STA	0x90	EFNAND Status Register
NDFC_SPARE_AREA	0xA0	Spare Area Configure Register
NDFC_PAT_ID	0xA4	Pattern ID Register
NDFC_RDATA_STA_CTL	0xA8	Read Data Status Control Register
NDFC_RDATA_STA_0	0xAC	Read Data Status Register0
NDFC_RDATA_STA_1	0xB0	Read Data Status Register1
NDFC_MDMA_ADDR	0xC0	MBUS DMA Address Register
NDFC_MDMA_CNT	0xC4	MBUS DMA Data Counter Register
NDFC_IO_DATA	0x300	Data Input/Output Port
RAM0_BASE	0x400	1024 Bytes RAM0 Base
RAM1_BASE	0x800	1024 Bytes RAM1 Base

1.4. NDFC Register Description

1.4.1. NDFC Control Register

Offset: 0x00			Register Name: NDFC_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:28	/	/	/
27:24	R/W	0	NDFC_CE_SEL Chip Select for 8 NAND Flash Chips 0 -7: NDFC Chip Select Signal 0-7 is selected 8-15: NDFC CS[7:0] not selected. GPIO pins can be used for CS. NDFC can support up to 16 CS.
23:22	/	/	/
21	R/W	0	NDFC_DDR_RM DDR Repeat Data Mode 0: Lower byte 1: Higher byte
20	R/W	0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0	NF_TYPE NAND Flash Type 00: Normal SDR NAND 01: Reserved 10: ONFI DDR NAND 11: Toggle DDR NAND
17	R/W	0	NDFC_CLE_POL NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0	NDFC_RAM_METHOD Access internal RAM method 0: Access internal RAM by AHB bus

			1: Access internal RAM by DMA bus
13:12	/	/	/
11:8	R/W	0	NDFC_PAGE_SIZE 0x0: 1024 bytes 0x1: 2048 bytes 0x2: 4096 bytes 0x3: 8192 bytes 0x4: 16384 bytes Notes: The page size is for main field data.
7	/	/	/
6	R/W	0	NDFC_CE_ACT Chip Select Signal CE# Control during NAND Operation 0: De-active Chip Select Signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatic control Chip Select Signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled.
5	/	/	/
4:3	R/W	0	NDFC_RB_SEL NDFC External R/B Signal Select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus
1	R/W	0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset.
0	R/W	0	NDFC_EN NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

1.4.2. NDFC Status Register

Offset: 0x04			**Register Name: NDFC_ST** **Default Value: 0x0000_0000**
Bit	**Read/Write**	**Default**	**Description**
31:14	/	/	/
13	R	/	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is greater than threshold value. 1: The number of bit 1 during current read operation is less than or equal

			to threshold value. This field is only valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
12	R	/	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is greater than threshold value. 1: The number of bit 0 during current read operation is less than or equal to threshold value. This field is only valid when NDFC_RDATA_STA_EN is 1. The threshold value is configured in NDFC_RDATA_STA_TH.
11	R	/	NDFC_RB_STATE3 NAND Flash R/B 3 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	/	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	/	NDFC_RB_STATE1 NAND Flash R/B 1 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	/	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0	NDFC_STA 0: NDFC FSM in IDLE state 1: NDFC FSM in BUSY state When NDFC_STA is 0, NDFC can accept new command and process command.
3	R	0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W	0	NDFC_DMA_INT_FLAG When it is 1, it means that a pending DMA is completed. It will be clear after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
1	R/W	0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command

			Mode or one Batch Command Work Mode. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
0	R/W	0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be cleared after writing 1 to this bit.

1.4.3. NDFC Interrupt and DMA Enable Register

Offset: 0x08			Register Name: NDFC_INT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:3	/	/	/
2	R/W	0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.
1	R/W	0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a single command in Normal Command Work Mode or one Batch Command Work Mode. 0: Disable 1: Enable
0	R/W	0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state. 0: Disable 1: Enable

1.4.4. NDFC Timing Control Register

Offset: 0x0C			Register Name: NDFC_TIMING_CTL Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:12	/	/	/
11:8	R/W	0	NDFC_READ_PIPE In SDR mode: 0000: Normal 0001: EDO 0010: E-EDO Others : Reserved

			In DDR mode: 0000~1111 is valid(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0	NDFC_DC_CTL NDFC Delay Chain Control These bits are only valid in DDR data interface, and configure the relative phase between DQS and DQ[0:7].

1.4.5. NDFC Timing Configure Register

Offset: 0x10			**Register Name: NDFC_TIMING_CFG** **Default Value: 0x0000_0095**
Bit	**Read/Write**	**Default**	**Description**
31:20	/	/	/
19:18	R/W	0	tWC Write Cycle Time 00: 1*2T 01: 2*2T 10: 3*2T 11: 4*2T
17:16	R/W	0	tCCS Change Column Setup Time 00: 12*2T 01: 20*2T 10: 28*2T 11: 60*2T
15:14	R/W	0	tCLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0	tCS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0	T_CDQSS DQS Setup Time for data input start 0: 4*2T

			1: 20*2T
10:8	R/W	0	T_CAD Command, Address, Data Delay 000: 2*2T 001: 6*2T 010: 10*2T 011: 14*2T 100: 22*2T 101: 30*2T 110/111: 62*2T
7:6	R/W	0x2	T_RHW RE# high to WE# low cycle number 00: 4*2T 01: 12*2T 10: 20*2T 11: 28*2T
5:4	R/W	0x1	T_WHR WE# high to RE# low cycle number 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
3:2	R/W	0x1	T_ADL Address to data loading cycle number 00: 0*2T 01: 6*2T 10: 14*2T 11: 22*2T
1:0	R/W	0x1	T_WB WE# high to busy cycle number 00: 14*2T 01: 22*2T 10: 30*2T 11: 38*2T

1.4.6. NDFC Address Low Word Register

Offset: 0x14			Register Name: NDFC_ADDR_LOW Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	R/W	0	ADDR_DATA4 NAND Flash 4th Cycle Address Data

23:16	R/W	0	ADDR_DATA3 NAND Flash 3rd Cycle Address Data
15:8	R/W	0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0	ADDR_DATA1 NAND Flash 1st Cycle Address Data

1.4.7. NDFC Address High Word Register

Offset: 0x18			Register Name: NDFC_ADDR_HIGH Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:24	R/W	0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0	ADDR_DATA7 NAND Flash 7th Cycle Address Data
15:8	R/W	0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

1.4.8. NDFC Data Block Number Register

Offset: 0x1C			Register Name: NDFC_DATA_BLOCK_NUM Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:6	/	/	/
4:0	R/W	0	NDFC_DATA_BLOCK_NUM DATA BLOCK Number It is used for batch command procession. 0: no data 1: 1 data blocks 2: 2 data blocks … 16: 16 data blocks Others: Reserved Notes: 1 data block = 512 or 1024 bytes main field data

1.4.9. NDFC Data Counter Register

Offset: 0x20			Register Name: NDFC_CNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:10	/	/	/
9:0	R/W	0	NDFC_DATA_CNT Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

1.4.10. NDFC Command IO Register

Offset: 0x24			Register Name: NDFC_CMD Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:30	R/W	0	NDFC_CMD_TYPE 00: Common command for normal operation 01: Special command for Flash spare field operation 10: Page command for batch process operation 11: Reserved
29	R/W	0	NDFC_SEND_FOURTH_CMD 0: Don't send third set command 1: Send it on the external memory's bus Notes： It is used for EF-NAND page read.
28	R/W	0	NDFC_SEND_THIRD_CMD 0: Don't send third set command 1: Send it on the external memory's bus Notes： It is used for EF-NAND page read.
27	R/W	0	NDFC_ROW_ADDR_AUTO Row address auto increase for page command 0: Normal operation 1: Row address increasing automatically
26	R/W	0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for common command and special command. 0: No action 1: DMA transfer automatically It only is active when NDFC_RAM_METHOD is 1. If this bit is set to 1, NDFC should setup DRQ to fetching data before output to Flash or NDFC should setup DRQ to sending out to system memory after fetching data from Flash.

			If this bit is set to 0, NDFC output the data in internal RAM or do nothing after fetching data from Flash.
25	R/W	0	NDFC_SEQ User data & BCH check word position. It only is active for Page Command, don't care about this bit for other two commands 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0	NDFC_SEND_SECOND_CMD 0: Don't send second set command 1: Send it on the external memory's bus
23	R/W	0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY; otherwise it can't when the internal NDFC_RB wire is BUSY.
22	R/W	0	NDFC_SEND_FIRST_CMD 0: Don't send first set command 1: Send it on the external memory's bus
21	R/W	0	NDFC_DATA_TRANS 0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field NDFC_ACCESS_DIR
20	R/W	0	NDFC_ACCESS_DIR 0: Read NAND Flash 1: Write NAND Flash
19	R/W	0	NDFC_SEND_ADR 0: Don't send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by NDFC_ADR_NUM field
18:16	R/W	0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field 111: 8 cycles address field
15:8	R/W	0	NDFC_CMD_HIGH_BYTE NDFC Command high byte data If 8-bit command is supported, the high byte should be zero for 16-bit bus width NAND Flash. For 8-bit bus width NAND Flash, high byte command is discarded.
7:0	R/W	0	NDFC_CMD_LOW_BYTE

			NDFC Command low byte data This command will be sent to external Flash by NDFC.

1.4.11. NDFC Command Set Register 0

Offset: 0x28			Register Name: NDFC_CMD_SET0 Default Value: 0x00E0_0530
Bit	**Read/Write**	**Default**	**Description**
31:24	/	/	/
23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1 Used for Batch Read Operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for Batch Read Operation
7:0	R/W	0x30	NDFC_READ_CMD Used for Batch Read Operation

1.4.12. NDFC Command Set Register 1

Offset: 0x2C			Register Name: NDFC_CMD_SET1 Default Value: 0x7000_8510
Bit	**Read/Write**	**Default**	**Description**
31:16	R/W	0x70	NDFC_READ_CMD0 Used for EF-NAND Page Read operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND Page Read operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for Batch Write Operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for Batch Write Operation

1.4.13. NDFC IO Data Register

Offset: 0x30			Register Name: NDFC_IO_DATA Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	NDFC_IO_DATA Read/ Write data into internal RAM Access unit is 32-bit.

1.4.14. NDFC ECC Control Register

Offset: 0x34			Register Name: NDFC_ECC_CTL Default Value: 0x4a80_0008
Bit	**Read/Write**	**Default**	**Description**
31	/	/	/
30:16	R/W	0x4a80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when NDFC_RANDOM_EN is set to '1'.
15:12	R/W	0	NDFC_ECC_MODE 0x0: BCH-16 for one ECC Data Block 0x1: BCH-24 for one ECC Data Block 0x2: BCH-28 for one ECC Data Block 0x3: BCH-32 for one ECC Data Block 0x4: BCH-40 for one ECC Data Block 0x5: BCH-48 for one ECC Data Block 0x6: BCH-56 for one ECC Data Block 0x7: BCH-60 for one ECC Data Block 0x8: BCH-64 for one ECC Data Block Others: Reserved
11	R/W	0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size
10	R/W	0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
9	R/W	0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
8:6	/	/	/
5	R/W	0	NDFC_ECC_BLOCK_SIZE 0: 1024 bytes of one ECC data block 1: 512 bytes of one ECC data block
4	R/W	0	NDFC_ECC_EXCEPTION 0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. Notes: It is only active when ECC is ON
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error correction function no pipeline with next block operation 1: Error correction pipeline

2:1	/	/	/
0	R/W	0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

1.4.15. NDFC ECC Status Register

Offset: 0x38			Register Name: NDFC_ECC_ST Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:16	R	0	NDFC_PAT_FOUND Special pattern (all 0x00 or all 0xff) Found Flag for 16 Data Blocks 0: No Found 1: Special pattern is found When this field is '1', this means that the special data is found for reading external nand flash. The register of NDFC_PAT_ID would indicate which pattern is found.
15:0	R	0	NDFC_ECC_ERR Error information bit of 16 Data Blocks 0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can't correct them Notes: The LSB of this register corresponds the 1st ECC data block. 1 ECC Data Block = 512 or 1024 bytes.

1.4.16. NDFC Enhanced Feature Register

Offset: 0x3C			Register Name: NDFC_EFR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:9	R/W	0	/
8	R/W	0	NDFC_WP_CTRL NAND Flash Write Protect Control Bit 0: Write Protect is active 1: Write Protect is not active Notes: When this bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, special bits error is inserted before writing external Flash Memory.

			0: No error is inserted (ECC Normal Operation) n: N bits error is inserted

1.4.17. NDFC Error Counter Register 0

Offset: 0x40			Register Name: NDFC_ERR_CNT0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[8i+7:8i] (i=0~3)	R	0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 0 to 3) 0: No corrected bits 1: 1 corrected bit 2: 2 corrected bits … 64: 64 corrected bits Others: Reserved Notes: 1 ECC Data Block = 512 or 1024 bytes

1.4.18. NDFC Error Counter Register 1

Offset: 0x44			Register Name: NDFC_ERR_CNT1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[8i+7:8i] (i=0~3)	R	0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 4 to 7) 0: No corrected bits 1: 1 corrected bit 2: 2 corrected bits … 64: 64 corrected bits Others: Reserved Notes: 1 ECC Data Block = 512 or 1024 bytes

1.4.19. NDFC Error Counter Register 2

Offset: 0x48			Register Name: NDFC_ERR_CNT2 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[8i+7:8i] (i=0~3)	R	0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 8 to 11)

			0: No corrected bits 1: 1 corrected bit 2: 2 corrected bits … 64: 64 corrected bits Others: Reserved Notes: 1 ECC Data Block = 512 or 1024 bytes

1.4.20. NDFC Error Counter Register 3

Offset: 0x4C			Register Name: NDFC_ERR_CNT3 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[8i+7:8i] (i=0~3)	R	0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 12 to 15) 0: No corrected bits 1: 1 corrected bit 2: 2 corrected bits … 64: 64 corrected bits Others: Reserved Notes: 1 ECC Data Block = 512 or 1024 bytes

1.4.21. NDFC User Data Register [n]

Offset: 0x50 + 0x4*n			Register Name: NDFC_USER_DATAn Default Value: 0xffff_ffff
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0xffffffff	USER_DATA User Data for ECC Data Block[n] (n from 0 to 15) Notes: 1 ECC Data Block = 512 or 1024 bytes

Notes: n from 0 to 15

1.4.22. NDFC EFNAND STATUS Register

Offset: 0x90			Register Name: NDFC_EFNAND_STATUS Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:8	/	/	/

7:0	R	0x0	EF_NAND_STATUS The Status Value for EF-NAND Page Read operation

1.4.23. NDFC Spare Area Register

Offset: 0xA0			Register Name: NDFC_SPARE_AREA Default Value: 0x0000_0400
Bit	**Read/Write**	**Default**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the spare area first byte address for NDFC interleave page operation.

1.4.24. NDFC Pattern ID Register

Offset: 0xA4			Register Name: NDFC_PAT_ID Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
[2i+1:2i] (i=0~15)	R	0	PAT_ID Special Pattern ID for 16 ECC data block 0: All 0x00 is found 1: All 0xFF is found Others: Reserved

1.4.25. NDFC Read Data Status Register

Offset: 0xA8			Register Name: NDFC_RDATA_STA Default Value: 0x0100_0000
Bit	**Read/Write**	**Default**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN 0: Disable the counting number of bit 1 and bit 0 during current read operation. 1: Enable the counting number of bit 1 and bit 0 during current read operation. The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:18	/	/	/
17:0	R/W	0	NDFC_RDATA_STA_TH

			The threshold value to generate data status. If the number of bit 1 during current read operation is less than or equal to threshold value, the bit 13 of NDFC_ST register will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, the bit 12 of NDFC_ST register will be set.

1.4.26. NDFC Read Data Status Register 0

Offset: 0xAC			Register Name: NDFC_RDATA_STA_0 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when the next command is executed.

1.4.27. NDFC Read Data Status Register 1

Offset: 0xB0			Register Name: NDFC_RDATA_STA_1 Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R	0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when the next command is executed.

1.4.28. NDFC MBUS DMA Address Register

Offset: 0xC0			Register Name: NDFC_MDMA_ADDR Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0	MDMA_ADDR MBUS DMA address

1.4.29. NDFC MBUS DMA Byte Counter Register

Offset: 0xC4			Register Name: NDFC_MDMA_CNT Default Value: 0x0000_0000
Bit	**Read/Write**	**Default**	**Description**
14:0	R/W	0	MDMA_CNT

			MBUS DMA data counter

1.5. NDFC Operation Diagram

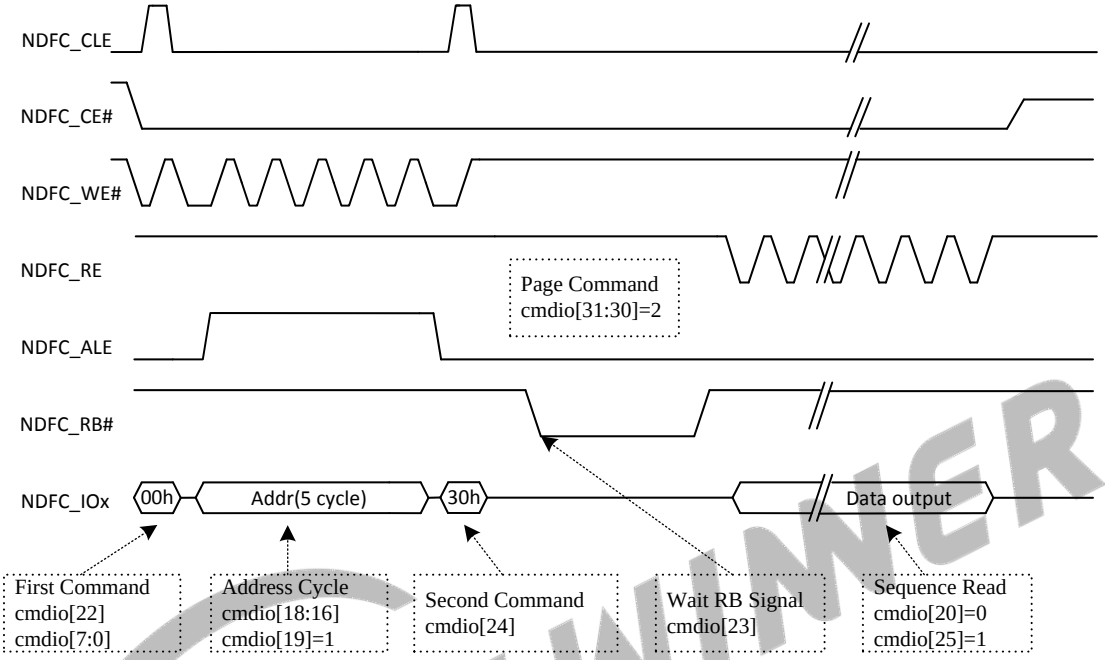

Figure 12. Page Read Command Diagram

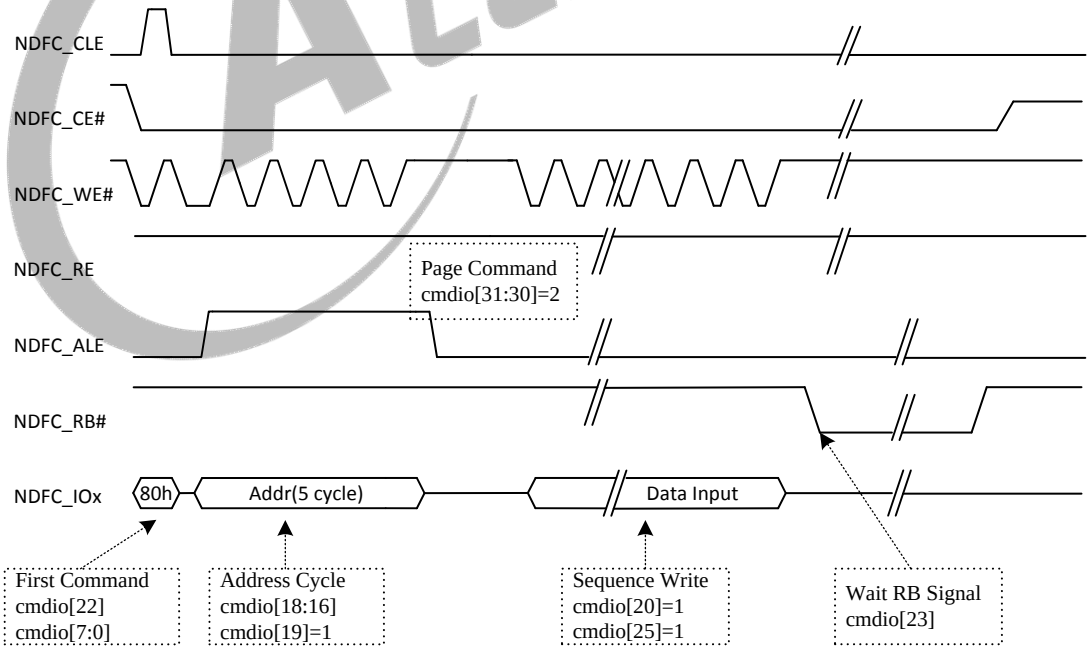

Figure 13. Page Program Diagram

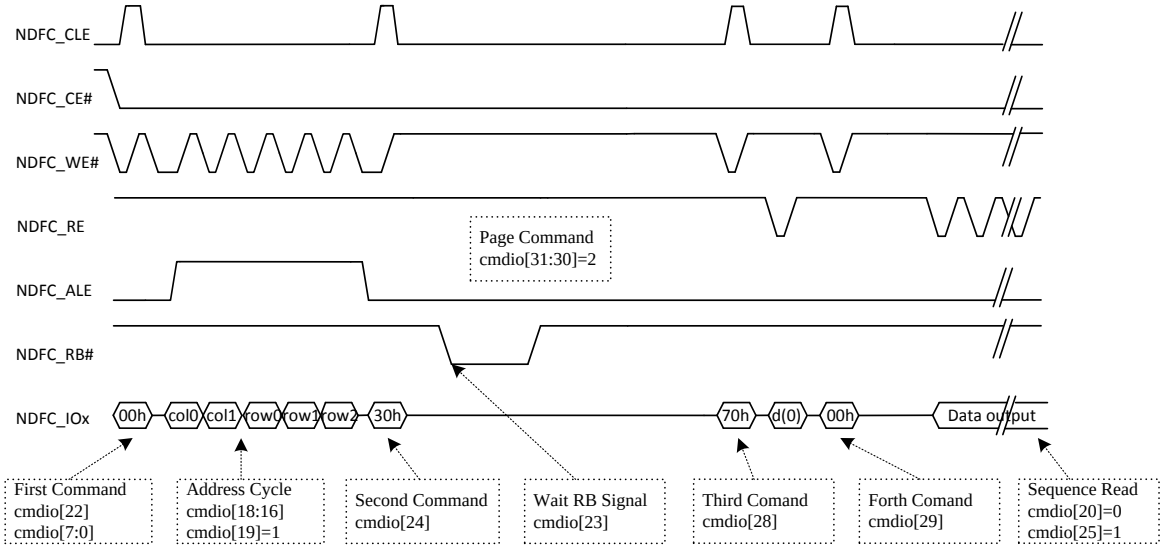

Figure 14. EF-NAND Page Read Diagram

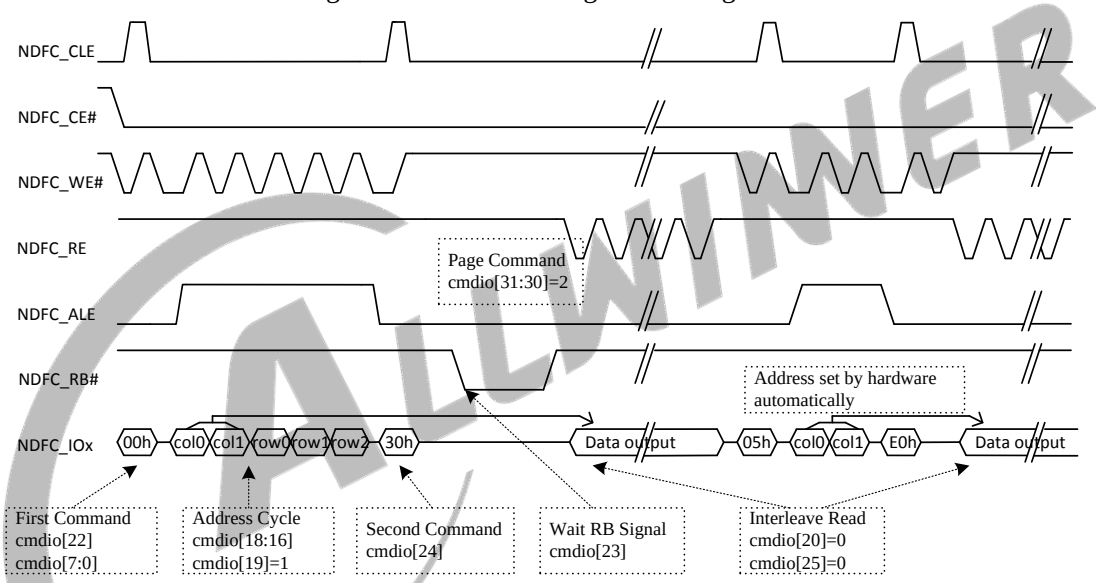

Figure 15. Interleave Page Read Diagram