DesignWare Cores LPDDR4x multiPHY Utility Block (PUB)

Databook

DWC LPDDR4x multiPHY PUB

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Revision History

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Note Links and references to section, table, figure, and page numbers in this table are only assured to be valid for the most current version.

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PUB Version	Databook Version	Date	Description
2.20a	2.00	June 1, 2018	Updated: • "Product Overview" on page 19 • "Interrupt Implementation" on page 169 • "DFI Update Timing Parameters" on page 115 • "Signal Mapping" on page 67 • "Additional/Optional Customer Defines" on page 182 • "Encoding for dfi_init_freq[] bus" on page 150 • "DFI Low Power Control Timing Parameters" on page 117 • "Encoding for dfi_init_freq[] bus" on page 150 • "LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1" on page 76 • "DQS Input Differential Voltage Testing (Vindiff_DQS)" on page 216 • "Functional Overview" on page 38 • "DFI PHY MASTER Timing Parameters" on page 118 • "APB Interface Access Rules" on page 158 • "PHY Initialization Engine" on page 148 s Added: • "dwc_ddrphy_dqs_vix_setup.txt" on page 217
2.20a	1.90	March 26, 2018	Updated: • "LP3 / IO Retention Enter" on page 143 • "[W2R] Write to Rank[i] ; Read from Rank[j]" on page 234 Removed: • Section 9.3.1 Interface between dwc_ddrphy_pub and wc_ddrphydbyte_top/dwc_ddrphyacx4_top - Reason: Outdated information

PUB Version	Databook Version	Date	Description
2.20a	1.80	January 25, 2018	Updated: • "Collisions Between PHY Update and DFI LP" on page 241 • "Supported System Configurations" on page 30 • "Rank-to-Rank Spacing" on page 232 • "Register Description" on page 225
2.11a	1.70	December 4, 2017	Updated: • "BypassPclk" on page 127 (
2.11a	1.60	November 13, 2017	Updated: • "Supported System Configurations" on page 30 • "DFI Pin List and Pin Mapping" on page 68 • "DFI Frequency Change Parameters" on page 119 • "Example Step 4 (above)" on page 215 • "Example Step 4 (above)" on page 222 • "2T Timing and Control Gear Down Support" on page 162 "2T Timing and Control Gear Down Support" on page 162 • "TDR Signals" on page 57 • "DQS Input Differential Voltage Testing (Vindiff_DQS)" on page 216 S • "Standby Power State (LP3/IO Retention)" on page 141 (• "SoC Digital Observation Pin" on page 203 • "DFI Control Timing Parameters" on page 112 • "DFI DRAM Clock Disable Parameters" on page 119 • "PHY Low Power State Modes" on page 137 • Replaced "DfiClk" with "DfiCtlClk*" Added: • "Measuring ODT Impedance" on page 224
2.11a	1.50	September 20, 2017	Updated: • "DFI Miscellaneous Parameters" on page 120 • "Mapping of ICCM and DCCM in CSR Address Spaces" on page 171 • "DFI Frequency Change Parameters" on page 119 Mantis 24576 • "Example Step 4 (above)" on page 215 Mantis 24075 • "Example Step 4 (above)" on page 222 Mantis 24075 • "2T Timing and Control Gear Down Support" on page 162 Mantis 23852 - Added a note • "2T Timing and Control Gear Down Support" on page 162 Mantis 24729 -
2.11a	1.40	September 18, 2017	Updated: • PUBREV in "Register Description" on page 225

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PUB Version	Databook Version	Date	Description
2.10a	1.30	July 26, 2017	Updated: • "Register Description" on page 225 - Added the MTestDtoCtrl register
2.00b	1.20	July 24, 2017	Updated: • "SoC Digital Observation Pin" on page 203 • "Bypass/Flyover Mapping from the Bypass Signal to the Bumps" on page 205 • "Signal Descriptions" on page 45 - New chapter formatting - no technical change • "Bypass/Flyover Controls" on page 209 • "Delay Cell Parametric Characterization and Test" on page 185 • "Supported System Configurations" on page 30 • "DFI Pin List and Pin Mapping" on page 68 - Changed dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[16*DBYTE+15:16*DBYTE] to dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)] throughout chapter • "DfiCtlClk" on page 123 • "DFI Low Power Control Timing Parameters" on page 117 • "SRAM Interface" on page 172 • "DFI Frequency Change" on page 148 • "DFI Control Timing Parameters" on page 112 • "AC Loopback" on page 192 • "Data Loopback" on page 193 • "LP3 / IO Retention Exit" on page 145 • Added: • "Analog Observability" on page 204 • "Signal Mapping" on page 67 - No technical change, a formatting change to create a new chapter from existing information formerly in the "Signal Descriptions" on page 45
2.00b	1.10	June 21, 2017	Updated: • PUB version number - no technical change
2.00a	1.00	May 8, 2017	Initial release

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Preface

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This databook describes the LPDDR4x multiPHY Utility Block (PUB). The PUB is compatible with the following Synopsys DWC DDR PHYs:

- DWC LPDDR4x multiPHY

Databook Organization

The chapters of this databook are organized as follows:

- Chapter 1, "Product Overview," provides an overview of the PUB, and key features
- Chapter 2, "Functional Overview," provides a functional description and signal description.
- Chapter 3, "Signal Descriptions"provides signal descriptions.
- Chapter 4, "Signal Mapping"provides signal mapping.
- Chapter 5, "Parameter Description"provides design parameters descriptions.
- Chapter 6, "Programming Model: Clocks, Resets, Initialization, and Power Management," provides clocking, reset, initialization and power management of the PUB
- Chapter 7, "Architecture," describes the architecture of the PUB.
- Chapter 8, "System Integration," provides information for integrating the DDR PHY with either the Synopsys DesignWare Cores Protocol or Memory Controllers or a non-Synopsys memory controller.
- Chapter 9, "Design for Test," provides information about the boundary scan register, including its signals and cell structures.
- Chapter 10, "Timing," describes all the detailed timing for the interface between the controller and the PUB.
- Chapter 11, "Register Description" describes a brief overview of the functional verification.

Reference Documentation

- *DesignWare Cores DWC LPDDR4x multiPHY Databook*, Synopsys, Inc.
- *DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Release Notes*, Synopsys, Inc.

Web Resources

- DesignWare IP product information: http://www.designware.com
- Your custom DesignWare IP page: http://www.mydesignware.com
- Documentation through SolvNet: http://solvnet.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): http://www.synopsys.com/keys

Customer Support

For customer support:

- Enter a call through SolvNet.
  - Go to https://solvnet.synopsys.com/EnterACall and provide the requested information, including:
    - Product: DesignWare Cores
    - Sub Product: Memory – DDRn SDRAM PHY
    - Version: PUB Version: 2.20a
    - Subject: (Fill in as appropriate to your case)
- Send an e-mail message to support_center@synopsys.com.
  - Include the Product Name, Sub Product name, and Version (product release number) in your e-mail so it can be routed correctly.
  - Provide the following additional information, if applicable:
    - For environment setup problems, run the debug_info command in the coreConsultant GUI and include the text file generated.
    - For configuration failures, include the error messages that appear in the coreConsultant GUI console pane.
    - For simulation failures, include a text file with your specific configuration. Generate this text file using the coreConsultant GUI's write_batch_script command. Also include the log file from the *workspace*/simulation/ directory, the log file for the specific test, and a VPD/VCD waveform dump file.
    - For synthesis failures, include the log file from *workspace*/syn/ directory.
- Telephone your local support center:
  - United States:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - Canada:

    Call 1-650-584-4200 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - All other countries:

    http://www.synopsys.com/Support/GlobalSupportCenters

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1 Product Overview

1.1 System Overview

The DWC LPDDR4x multiPHY PUB SDRAM interface solution is a combination of hard and soft IP that is used to provide a physical interface to JEDEC standard DDR4/LPDDR4/LPDDR4x SDRAM memories. This solution provides logical support for all JEDEC DRAM devices compatible with the system design and PHY hard macro components.

The full PHY IP solution consists of both hard IP components and soft IP components. The hard IP components include:

- A PHY macro for the data lane, DDRPHYDBYTE (referred to as DBYTE),
- A PHY macro for the address/command lane, DDRPHYACX4 (referred to as ACX4)
- The PHY MASTER block, which includes the high-speed PLL.

Note All of these macros contain integrated I/O functionality.

The soft IP consists of a single soft macro, the PHY Utility Block (DDRPHY_PUB or PUB), which provides configuration and control for all the PHY hard macros.

Note An SDRAM system would normally instantiate multiple ACX4 components, multiple DBYTE components and a MASTER PHY component in order to build an 8 to 72-bit system.

The following figure shows how the PHY is used in a typical SDRAM system.

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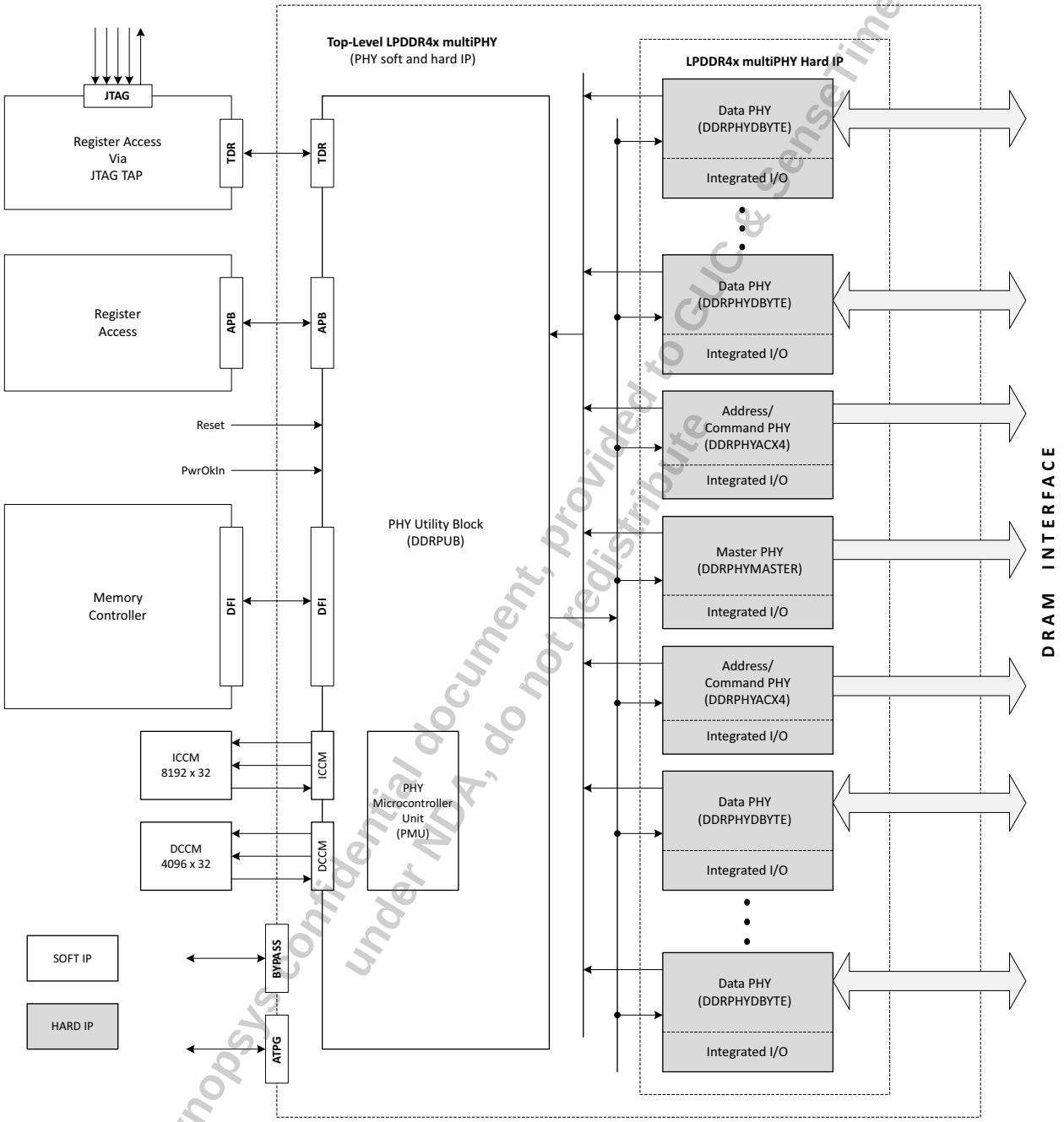
Figure 1-1 System Overview



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The DWC PHY Utility Block (PUB) is an IP component to be used with the DWC PHY. It provides control features to ease the customer implementation of digitally controlled functions of the PHY such as initialization, DRAM interface training, delay line calibration and VT compensation, impedance calibration and VT compensation, and programmable configuration controls. It also provides a DFI interface to the PHY.The PUB includes configuration registers that are accessible through a configuration port. The configuration port is compatible with an APB interface.

1.1.1 System Components

The full DWC LPDDR4x multiPHY PUB IP solution consists of multiple components, including a combination of the following :

- DDRPHYACX4: The AC is the PHY component for the address/command lane. Features of the AC include:
  - High-speed digital logic pipeline for transmitting address/command to the SDRAM
  - Loop-back test mode and PRBS checkers to help verify the integrity of the internal datapath of all AC I/O lanes
  - I/O component that includes PVT-compensated and output impedance
  - For more information, refer to *DWC LPDDR4x multiPHY Databook*
- DDRPHYDBYTE: The DBYTE is the data receive (RX)/ transmit (TX) building component for the DDR PHY (statically configurable as either two nibble-wide lanes or one byte-wide data lane). Features of the DBYTE include:
  - High speed digital logic pipeline for transmit datapaths to the SDRAM
  - High speed digital logic pipeline for receive datapaths from the SDRAM
  - Drivers and receivers for the DQ and DQS signals as well as all the necessary high voltage analog macros to interface off chip
  - I/O component that includes PVT-compensated on-die termination (ODT) and output impedance
  - For more information, refer to the *DWC LPDDR4x multiPHY Databook*
- MASTER PHY- The MASTER PHY is the location of the high speed PLL used to generate the high speed clock for data transmit and high speed digital pipelines. The PLL has the following modes of operation:
  - The PLL block generates the DRAM bit-rate clock
  - Other features of the MASTER include:
    - Power on reset (POR) circuit, I/O macros for DRAM reset, DRAM alert, and PHY debug
    - A global voltage reference generation and observation circuit
    - Impedance calibration circuits

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- PHY Utility Block (PUB)— provides configuration, control, and other utility functions for all PHY hard components. This block handles a variety of functions for the PHY, including driving initialization sequences, providing all training functions, implementing the DFI protocol, and implementing registers and a register access bus.

Note Using the latest available version of a PHY with the latest PUB is recommended. Refer to the Release Notes and DWC LPDDR4x multiPHY Databook for details.

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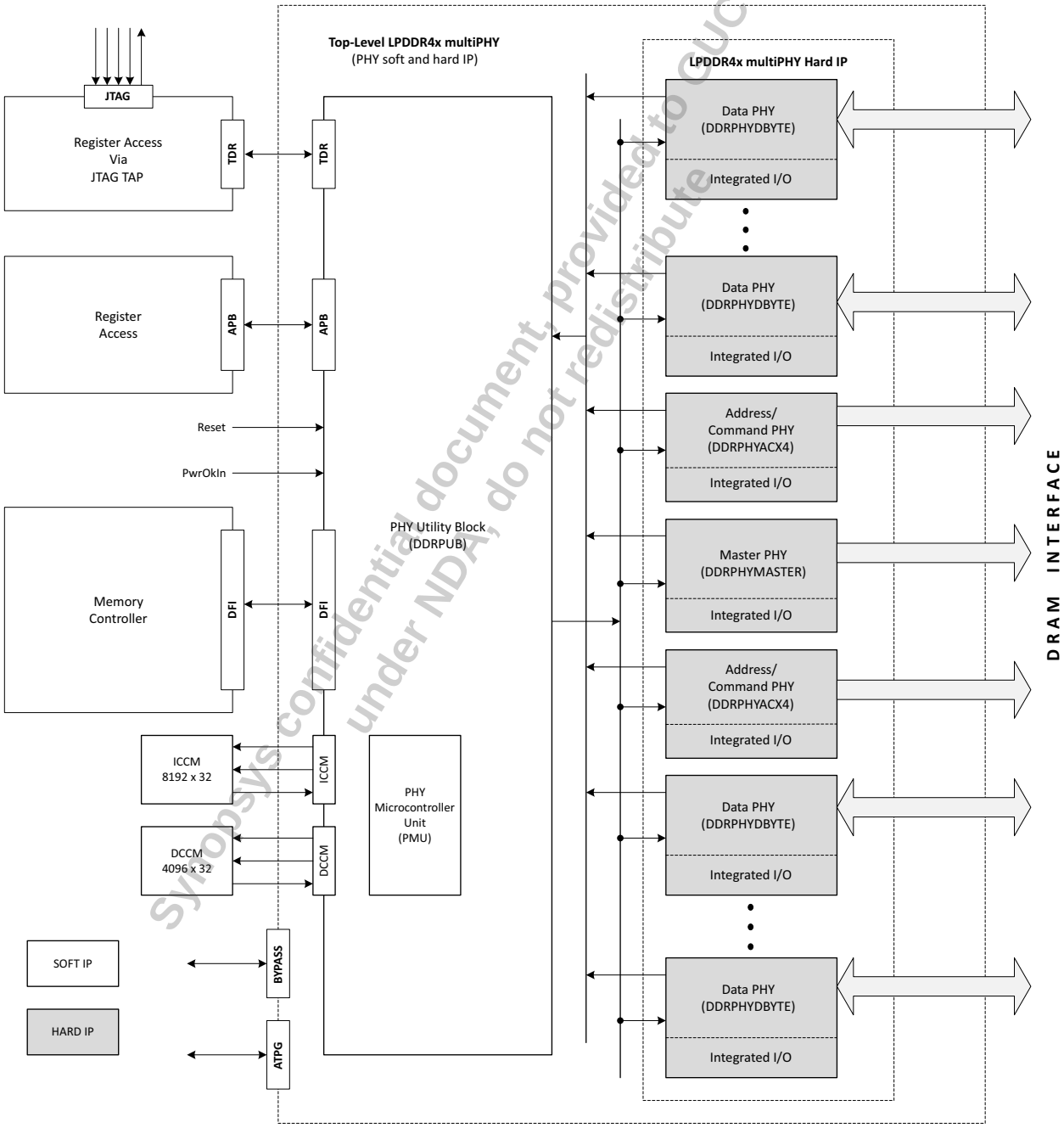
1.1.2 Memory Controller Solution

A memory controller solution is required for PHY applications. The solution uses the PUB's DFI interface to connect between the PHY and the memory controller (see Figure 1-2 on page 23).

Note For minimum latency, the PHY should be placed within close proximity to the memory controller.

Figure 1-2 Memory Controller Implementation of DDR Interface and Control Solution



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1.2 The DWC LPDDR4x multiPHY Features

1.2.1 Highlights

- Supports JEDEC standard LPDDR4x, LPDDR4,and DDR4 SDRAMs
- High-performance DDR PHY (see PHY databook for supported data rates)
- Flexible two channel architecture
- Low Standby and VDDQ signaling power down to 1.1V and VDDQLP signaling power down to 0.6V operation
- In LPDDR4 and DDR4 operation, SOC must connect VDDQLP to VDDQ=1.1V
- LPDDR4 has the option of using either the PMOS pull-up or the NMOS pull-up (slightly lower power)
- LPDDR4x only SOC must connect to both VDDQ (1.1V supply) and VDDQLP(0.6V supply) for ESD purposes, but full decap is not needed
- 40, 60, 120 ohm drive and termination only (9 segments each at 120 ohm: 3 PMOS pull-up to VDDQ, 3 NMOS pull-up to VDDQLP, 3 NMOS pull-down to VSS)
- PHY independent, firmware-based training using an embedded calibration processor
- Supports up to 4 trained states/frequencies with < 5µs switching time
- VT compensated delay lines for DQS centering, read/write leveling, and per bit deskew DFI 4.0 version 2-compliant controller interface with option for dual DFI Channels
- Designed for rapid integration with Synopsys memory or protocol controllers for a complete DDR interface solution
- Flexible implementation to support Package-On-Package (PoP) style SoCs
- Built-in anti-aging features to prevent effects of NBTI & HCI

1.2.2 Target Applications

- Smart phones
- Tablets
- Embedded mobile computing
- Ultraportable laptops

1.2.3 Technology

- 28-nm, 16-nm, 14-nm, 10-nm and below

1.2.4 PHY Key Features

- Low latency, small area, low power
- Compatible with JEDEC standard LPDDR4 and DDR4 SDRAMs
  - Refer to the PHY Databook for supported speed information
- DFI 4.0 Version 2 compliant interface to the memory controller
  - 1:1, 1:2, and 1:4 clock modes supported

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- Optional dual channel DFI for independent 2-channel memories
- Flexible channel architecture
  - Support for 2 or 4 independent LPDDR4x 16-bit channels
  - Support for 2 or 4 independent LPDDR4 16-bit channels
  - Support for one DDR4 interface
- PHY supports:
  - 8-bit, 16-bit and 32-bit wide SDRAMs
    - 8-bit and 16-bit DDR4 supported
    - 16-bit per channel LPDDR4 supported
  - Many DRAM packaging options supported:
    - SDRAM components soldered directly to PCB
    - LPDDR4 PoP devices supported
    - DDR4 UDIMMs and SODIMM
- 8- to 72-bit data path widths in 8-bit increments
- Partially populated interfaces where allowed by protocol
- Up to 16 memory ranks with DDR4 3DS devices
- Flexible configuration options:
  - LPDDR4x: Up to 2 DQ loads, 8 CA loads, and 4 CS loads
  - LPDDR4: Up to 2 DQ loads, 8 CA loads, and 4 CS loads
  - DDR4: Up to 4 DQ loads and 4 ranks of CA loading
  - Shared AC mode that permits one address and command channel to be time division multiplexed between two independent data channels
- PHY independent, firmware-based training using an embedded calibration processor
  - Utilizes specialized hardware acceleration engines
  - Automatic periodic retraining through PHY MASTER Interface
  - Support for:
    - LPDDR4 Command Bus eye training relative to CK
    - Write Leveling to compensate for CK-DQS timing skew
    - Write Training: DQS to DQ:Two modes of training are available in LPDDR4:

      Command-based FIFO WR/RD with user patterns

      An internal DQS clock?tree oscillator, to determine the need for, and the magnitude of, required periodic training
    - Data bus VREFDQ training
    - Read training:

      DQ bit deskew training using DRAM mode registers

      DQS to DQ eye centering training using DRAM array
  - LVSTL IO calibration and ODT calibration

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- Can be trained for up to four distinct states/frequencies to permit fast frequency changes between the four frequencies
  - Each trained state can have unique frequency and I/O drive and ODT impedance settings
  - Each trained state is maintained across voltage and temperature variation
  - Frequency changes are initiated by the DFI interface without software involvement
- Three inactive idle states:
  - DFI_LP Mode: most clocks and delay lines gated
  - PHY Inactive: leakage only
  - PHY Retention: Core power removed, most I/Os powered down, SDRAMs held in self-refresh
- Voltage and temperature compensated delay lines used for:
  - Centering the clock in the address/command window
  - Centering the strobes in the data eyes
  - Read/write leveling
  - Per-bit deskew
- Includes a low-jitter PLL for both PHY clock generation and SDRAM clock generation
  - Only one PLL is required per DDR PHY
  - Integrated PLL bypass to support 50 to 666 MT/s
- Flexible pre and postamble
  - Support for 1 or 2 clock write preamble
  - Support for static or toggling read preamble of 1 or 2 tCK
  - Support for 0.5 or 1.5 tCK read postamble
- Support for a SW controllable DQ bit and AC bit swizzling
- Supports PHYs that go around a die corner and support for both East-West and North-South orientations
- Support for 28-nm and below poly orientation rules
  - Macrocells can be instantiated on orthogonal sides
- Includes the PHY Utility Block (PUB)
  - Soft IP Verilog design that includes PHY control features, such as read/write leveling and data eye training
  - APB and JTAG interfaces for register access
- Test support:
  - At-speed loopback testing on both the address and data channels
  - Delay line BIST
  - MUX-scan ATPG (stuck-at SCAN)
  - RX and TX asynchronous paths support a maximum bit rate of 400 Mb/s (200MHz)
  - PLL lock test

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- ZQ calibration test
- JTAG register interface for easy test access
- Firmware-based 2D eye mapping diagnostic tool allows measuring 2D eye for every bit of the bus at both DRAM and host receivers
- Direct override programming available for all VREF, ODT, drive strength, and timing delays to facilitate debug and characterization

1.2.5 LPDDR4x-Specific Features

- CBT to train address/command bus timing and set user calculated DRAM CA VREF
- Write leveling
- DRAM addressing up to 16Gb
- MRR reads and MPC write/read
- Data bus inversion
- Automatic training of DQ VREF level setting separately for PHY per bit and SDRAM per device
- Write/Read Eye Centering per rank per byte
- Programmable write postamble (0.5 tCK or 1.5 tCK)
- Mode register readout
- Periodic retraining for DRAM write (tDQS2DQ) and read (tDQSCK) drift

1.2.6 LPDDR4-Specific Features

- CBT to train address/command bus timing and set user calculated DRAM CA VREF
- Write leveling
- DRAM addressing up to 16Gb
- MRR reads and MPC write/read
- Data bus inversion
- Automatic training of DQ VREF level setting separately for PHY per bit and SDRAM per device
- Write/Read Eye Centering per rank per byte
- Programmable write postamble (0.5 tCK or 1.5 tCK)
- Mode register readout
- Periodic retraining for DRAM write (tDQS2DQ) and read (tDQSCK) drift

1.2.7 DDR4-Specific Features

- Write leveling
- DRAM addressing up to 16Gb
- MPR writes/reads
- Data bus inversion
- Automatic training of DQ VREF level setting separately for PHY per bit and SDRAM per device

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- Write/Read Eye Centering per rank per byte
- Command/Address (CA) parity
- Per DRAM addressability
- Programmable write preamble (1 tCK or 2 tCK)
- Mode register readout
- Gear down mode
- DDR4 3DS

1.2.8 I/O Features

- LPDDR4x, LPDDR4, and DDR4 operating modes
- I/Os are integrated within the PHY Macrocells
- Programmable input on-die termination (ODT)
- Programmable output impedance
- PVT-compensated ODT and output impedance
- Supports ability to group sections of I/O cells that have different input termination and/or output impedance settings per section
- Termination support:
  - VSS termination for LPDDR4x address/command and data channels
  - VSS termination for LPDDR4 address/command and data channels
  - Mid-rail termination for DDR4 address/command channels
  - VDDQ termination for DDR4 data channels
- Separate driver and receiver I/O power-down control
- Embedded boundary scan support logic and bypass with secondary input & output ports
- PAD and internal loopback modes
- Supports flip chip packaging
- Retention feature keeps SDRAMs in self-refresh during VDD power down
- Power on clear (POC) function renders library power supply sequence-agnostic
- Embedded VDDQ-VSS and VDDLP-VSS decoupling capacitance plus optional “SnapCap” cells to add additional VDDQ-VSS decoupling capacitance

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Note

Features and System Configurations

- Not all system configurations listed here are supported in every release of the PHY. Please consult your release notes or Synopsys support to determine which configuration is enabled for a particular release
- Features implied through CSR or other low-level descriptions are not supported unless indicated in “PHY Key Features” on page 24 and the release notes.

1.3 Compatible Standards

The following standards are compatible with the DWC LPDDR4x multiPHY PUB design.

Standard	Compatible Version
JEDEC DDR4 SDRAM Specification	JESD79-4A, November 2013
JEDEC DDR4 UDIMM Specification	Rev 1.2, June 2016
JEDEC DDR4 SDRAM SODIMM Specification	Rev 1.2, Jun 2016
JEDEC 3D Stacked SDRAM Addendum to JESD79-4	DDR4-3DS Rev 0.95, Nov 2015
DFI Specification	v4.0 Addendum 2, January 2015
AMBA APB Protocol	v2.0, April 2010
JEDEC LPDDR4 Specification	JESD209-4B, February 2017
JEDEC LPDDR4X Addendum No. 1 to JESD209-4-1	Addendum No. 1 to JESD209-4-1 - Low Power Double Data Rate 4X (LPDDR4X) , January 2017

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1.4 Supported System Configurations

The supported configurations for the PUB are dependent on the following programmed parameters:

- DWC_DDRPHY_NUM_ANIB: Number of ACX4 macrocells
- DWC_DDRPHY_NUM_DBYTES: Number of DBYTE macrocells
- DWC_DDRPHY_DFI1_EXISTS: Whether or not the second DFI interface (DFI1) is enabled

For more information on parameter programming refer to "Functional Overview" on page 37.

Note For the configurations related to the LPDDR4 protocol, the same configurations apply to the LPDDR4x protocol

1.4.1 PHY Configurations Supporting Two Channels Per PHY

1.4.1.1 PHY Configuration: NUM_ANIB=12 / NUM_DBYTES=K / DFI1_EXISTS=Y

Table 1-1 PHY Configuration: NUM_ANIB=12 / NUM_DBYTES=K / DFI1_EXISTS=Y

DRAM Type	Channel A [DFI0]		Channel B [DFI1]		Supported Device Types
	Supported Number of Ranks	Data Bytes	Supported Number of Ranks	Data Bytes	
DDR4	1, 2, 3, 4	K=1,2,3,4,5,6,8,9	-	-	x8, x16
LPDDR4/ LPDDR4x	1, 2	K=2, 4	0,1,2	K=2,4	x16

1.4.1.1.1 Legal Options

- 12 ANIBS / 4 DBYTES / 2 CHANNEL
  - Supports 32b LPDDR4/LPDDR4X: Two 16b LPDDR4 channels can be independent or in lockstep
  - Supports {8, 16, 24, 32}b DDR4:
    - DFI0 status: Only DFI0 option (Configured by CSR)
  - Supports {8, 16, 24, 32}b DDR4/3:
    - DFI0 status: Only DFI0 option (Configured by CSR)
- 12 ANIBS / 8 DBYTES / 2 CHANNEL
  - Supports 2x32b LPDDR4/LPDDR4X: Two 16b LPDDR4 channels can be independent or in lockstep
  - Supports 2x16b LPDDR4/LPDDR4X: User may choose to use only half of instantiated DBYTEs
  - Supports 1x32b LPDDR4/LPDDR4X: Two 16b LPDDR4 channels can be independent or in lockstep
  - Supports 1x16b LPDDR4/LPDDR4X: One 16b LPDDR4 channel

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- Supports {8:48, 64, 72}b DDR4:
  - DFI0 status: Only DFI0 option (Configured by CSR
- A supported number of ranks value of 0 in channel B means that the ranks are not populated

1.4.1.2 PHY Configuration: NUM_ANIB=10 / NUM_DBYTES=K / DFI1_EXISTS=Y

Table 1-2 PHY Configuration: NUM_ANIB=10 / NUM_DBYTES=K / DFI1_EXISTS=Y

DRAM Type	Channel A [DFI0]		Channel B [DFI1]		Supported Device Types
	Supported Number of Ranks	Data Bytes	Supported Number of Ranks	Data Bytes	
DDR4	1, 2	K=1,2,3,4,5,6,8,9	-	-	x8, x16
LPDDR4/ LPDDR4x	1, 2	K=2,4	0,1,2	K=2,4	x16

1.4.1.2.1 Legal Options

- 10 ANIBS / 4 DBYTES / 2 CHANNEL
  - Supports 32b LPDDR4: LPDDR4 channels can be independent or in lockstep
  - Supports {8,16,24,32}b DDR4: Only DFI0 option (Configured by CSR)
- 10 ANIBS / 8 DBYTES / 2 CHANNEL
  - Supports 2x32b LPDDR4: LPDDR4 channels can be independent or in lockstep
  - Supports 2x16b LPDDR4: User may choose to use only half of instantiated DBYTEs
  - Supports 1x32b LPDDR4
  - Supports 1x16b LPDDR4
  - Supports {8:48,64,72}b DDR4: Only DFI0 option (Configured by CSR)

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1.4.1.3 PHY Configuration: NUM_ANIB=6 / NUM_DBYTES=K / DFI1_EXISTS=Y

Table 1-3 HY Configuration: NUM_ANIB=6 / NUM_DBYTES=K / DFI1_EXISTS=Y

DRAM Type	Channel A [DFI0]		Channel B [DFI1]		Supported Device Types
	Supported Number of Ranks	Data Bytes	Supported Number of Ranks	Data Bytes	
DDR4	-	-	-	-	-
LPDDR4/ LPDDR4x	1, 2	K=2	0,1,2	K=2	x16

1.4.1.3.1 Legal Options

- 6 ANIBS/4DBYTES/2Channel
  - Supports 2x16b LPDDR4: LPDDR4 channels can be independent or in lockstep
  - Supports 1x16b LPDDR4: DF1 can be depopulated. This option is not recommended

1.4.2 PHY Configurations Supporting One Channel Per PHY

1.4.2.1 PHY Configuration: NUM_ANIB=12 / NUM_DBYTES=K / DFI1_EXISTS=N

Table 1-4 PHY Configuration for DRAM on PCB: NUM_ANIB=12 / NUM_DBYTES=K / DFI1_EXISTS=N

DRAM Type	Channel A [DFI0]		Supported Device Types
	Supported Number of Ranks	Data Bytes	
DDR4	1, 2, 3,4	K=1, 2, 3, 4, 5, 6, 8, 9	x8, x16
LPDDR4/ LPDDR4x	1, 2	K=2	x16

1.4.2.1.1 Legal Options

- 12 ANIBS/KDBYTES/1Channel
  - Not recommended for LPDDR4. The recommendation is to use DFI1_EXISTS=Y
  - Supports 16b LPDDR4

Table 1-5 PHY Configuration: NUM_ANIB=10 / NUM_DBYTES=K / DFI1_EXISTS=N[1]

DRAM Type	Channel A [DFI0]		Supported Device Types
	Supported Number of Ranks	Data Bytes	

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Table 1-5 PHY Configuration: NUM_ANIB=10 / NUM_DBYTES=K / DFI1_EXISTS=N[1]

DDR4	1, 2	K=1,2,3,4,5,6,8,9	x8, x16
LPDDR4/ LPDDR4x	1, 2	K=2	x8, x16

1. The values of K* are the maximum number of usable DBYTEs in LPDDR4 mode

1.4.2.1.2 Legal Options

- 10 ANIBS/K DBYTES/1Channel
  - Not recommended for LPDDR4. The recommendation is to use DFI1_EXISTS=Y
  - Supports 16b LPDDR4

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1.4.2.2 PHY Configuration: NUM_ANIB=6 / NUM_DBYTES=K / DFI1_EXISTS=N

Table 1-6 PHY Configuration: NUM_ANIB=6 / NUM_DBYTES=K / DFI1_EXISTS=N

DRAM Type	Channel A [DFI0]		Supported Device Types
	Supported Number of Ranks	Data Bytes	
DDR4	-	-	-
LPDDR4/ LPDDR4X	1, 2	K=2	x8, x16

1.4.2.2.1 Legal Options

- 6 ANIBS/4 DBYTES/1 Channel
  - Not recommended for LPDDR4.The recommendation is to use DFI1_EXISTS=Y

1.4.2.3 PHY Configuration: NUM_ANIB=3 / NUM_DBYTES=K / DFI1_EXISTS=N

Table 1-7 PHY Configuration: NUM_ANIB=3 / NUM_DBYTES=K / DFI1_EXISTS=N

DRAM Type	Channel A [DFI0]		Supported Device Types
	Supported Number of Ranks	Data Bytes	
DDR4	-	-	-
LPDDR4/ LPDDR4x	1, 2	K=2,4	x8, x16

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1.5 Process Information

The PUB is RTL-based soft IP, which can be paired with the PHY and a DFI-compliant memory controller to form a complete solution. For the supported PHY process information, refer to the *DWC LPDDR4x multiPHY Databook*.

1.5.1 PUB Area

The following table reflects approximate area estimates for the PUB. Actual cell counts vary based on clock frequency, technology, standard cell library, physical design constraints, synthesis/physical design tools, and methodology.

Table 1-8 PUB Area

Configuration	Number of Registers	Number of Placeable Components	Number of Equivalent 2-Input NAND Gates
16b Data, 12b Address/Command (2 DBYTE, 3 ACX4, 1 MASTER)	35.5K	237K	566K
32b Data, 24b Address/Command (4 DBYTE, 6 ACX4, 1 MASTER)	52.1K	372K	866K
72b Data, 48b Address/Command (9 DBYTE, 12 ACX4, 1 MASTER)	92.9K	699K	1596K

1.6 Timing Closure

The PHY can accommodate a wide variety of compile options to allow the user to set the desired configuration and functionality. The DDR PHY also permits the user to implement various floor plan styles. This DDR PHY is designed for very high data rates and the maximum attainable performance may be affected by the user's selected floor plan and PUB compile options. Enabling both a wide interface and many optional features simultaneously may result in timing closure difficulties. A non-optimal floor plan, especially for a very wide interface, may also impact timing closure capability.

It is strongly recommended the user perform preliminary physical-based synthesis using such EDA tools as Synopsys' Design Compiler Graphical to estimate the timing closure capability of both the estimated floor plan and the selected DDR PHY configuration at the start of the project before deciding on the desired floor plan and compile options for the DDR PHY. Furthermore, in order to vet in advance possible timing closure issues, margining should be imposed during synthesis so as to emulate non-ideal circumstances (e.g., clock skew, parasitics that vary from those described in wire models, path length-dependent derates, etc.) that will likely be encountered during downstream construction activities.

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1.7 Definition of Terms and Acronyms

Table 1-9 Definition of Terms and Acronyms

Term	Description
AC	Address/command
ACX4	The four-lane address/command hard IP unit
ACSM	Address Command State Machine
ANIB	Address Nibble, equivalent to ACX4
CSR	Control and Status Registers
DBYTE	The eight-lane data IO unit
DFI	DDR PHY Interface
DFICLK	DDR PHY Interface Clock Clock reference for all mission mode interface signals.
DTSM	Data Training State Machine
HME	Hard Macro Family E
MC	Memory Controller – Interfaces with the PHY to provide operational commands, address and data.
PMU	PHY microcontroller unit, same as uCtl
PUB	DWC PHY Utility Block
PRBS	Pseudo Random Binary Sequence
PState	The PHY supports multiple power states, both Active and Standby. A power state (or PState) is a combination of memory clock frequency, driver strengths, termination and timing. The PHY supports 4 active power states, labelled PS0, PS1, PS2, and PS3. The PHY also supports 3 standby (inactive) power states, labelled DFI LP, Fast Standby, and IO Retention. Active power states are changed by utilizing the DFI Frequency Change protocol, throughthe "dfi_init_start", "dfi_freq[]", and "dfi_init_complete" signals.
uCtl	Micro-Controller

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2
Functional Overview

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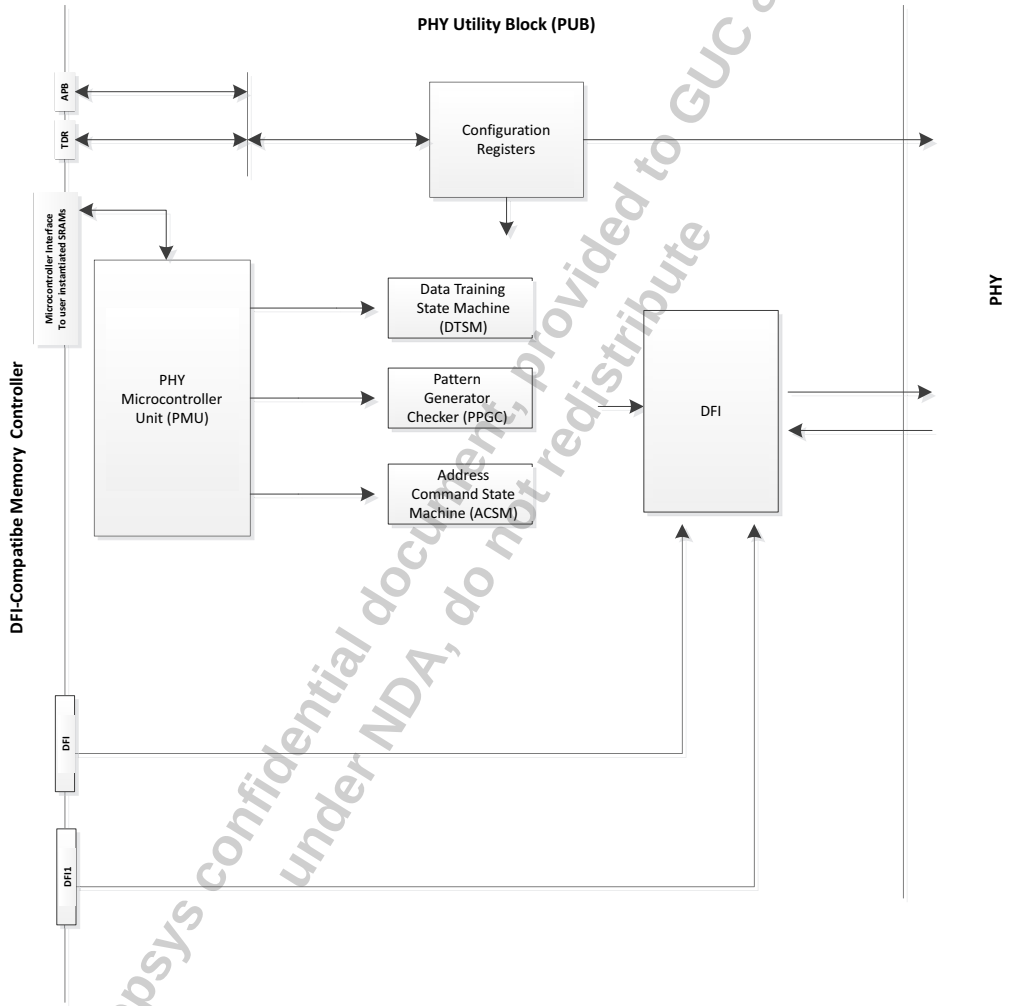
This chapter describes the following:

- "Functional Overview" on page 38

2.1 Functional Overview

The DWC PHY Utility Block (PUB) is a IP block that is used with the DesignWare Cores PHY. It provides control features to ease the customer implementation of digitally controlled DDR PHY features such as read DQS training, data eye training, output impedance calibration. It also provides a DFI interface to the PHY. The PUB performs, in sequence, various tasks required by the PHY before it can commence normal DDR operations. Figure 2-1 on page 38 shows a block diagram of the PUB.

Figure 2-1 PHY Utility Block (PUB)



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SDRAM memory read/write access through the PHY is primarily through a DFI interface on the PUB.

Note The memory controller used with the PHY must be DFI compatible.

Access to the PUB internal control features and registers is through a dedicated configuration port, the APB. A TDR interface is included as an additional second configuration port to co-exist with the APB configuration ports

The PUB is driven off two clocks, the DFI clock (DFICLK) and the configuration clock (APBCLK for APB interface). The DFICLK is the half the frequency of the SDRAM clock (ck). The APBCLK drives the APB interface logic; all internal configuration registers, training and initialization logic, and DRAM address and data path are driven from the DFICLK.

The following is an overview of the different design blocks and functionality of the PUB:

- Configuration Registers
  - Includes all registers required to configure, control, train and self-test the PHY. The configuration block also contains registers required to initialize the DRAM.
- PHY Microcontroller Unit (uCtrl)
  - Initialization
    - Used to initialize the PHY, including locking of the PLL, delay line calibration and calibration of I/O impedances.
  - Data Training
    - Used to train the PHY for optimum timing margins. This includes finding the best positioning of the DQS gating window during reads, write leveling, data bit deskew, and optimizing the read and write data eye.
- DFI Interface Block
  - Implements a DFI-compliant interface between the external controller and the PHY.

Note The Synopsys DFI signal naming convention is DFIx_FREQ instead of DFI_FREQUENCY as shown in the DFI Specification.

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2.2 DFI Connections and System Memory Configurations

The PHY supports multiple configurations of system memory. The memory type, width, and number of channels used in the LP configuration determines the controller connections to and usage of the DFI bus. The following figures show examples of several memory configurations and their connections.

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Figure 2-2 LPDDRx DRAM Channel A

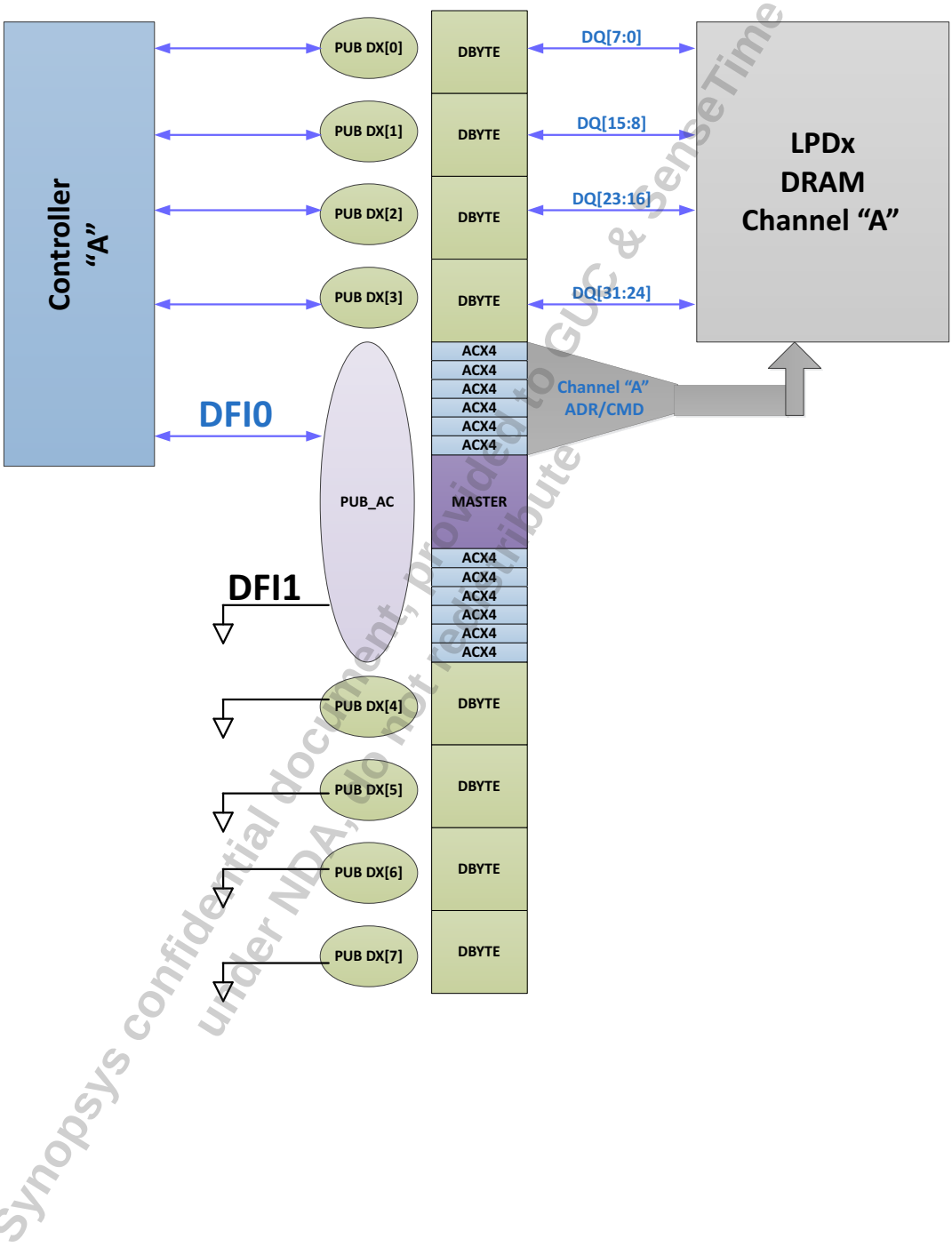

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Figure 2-3 LPDDRx DRAM Channel A and Channel B

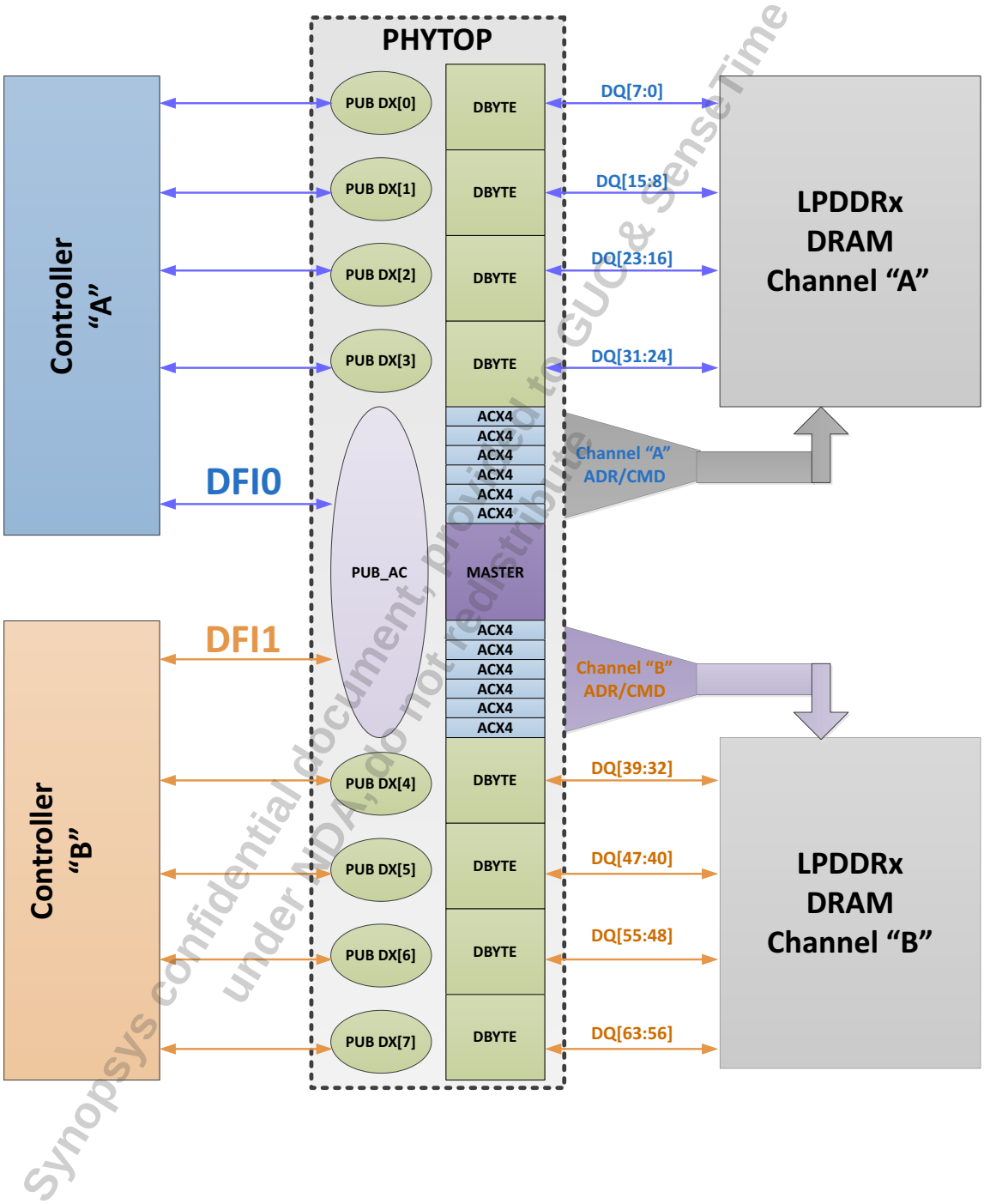

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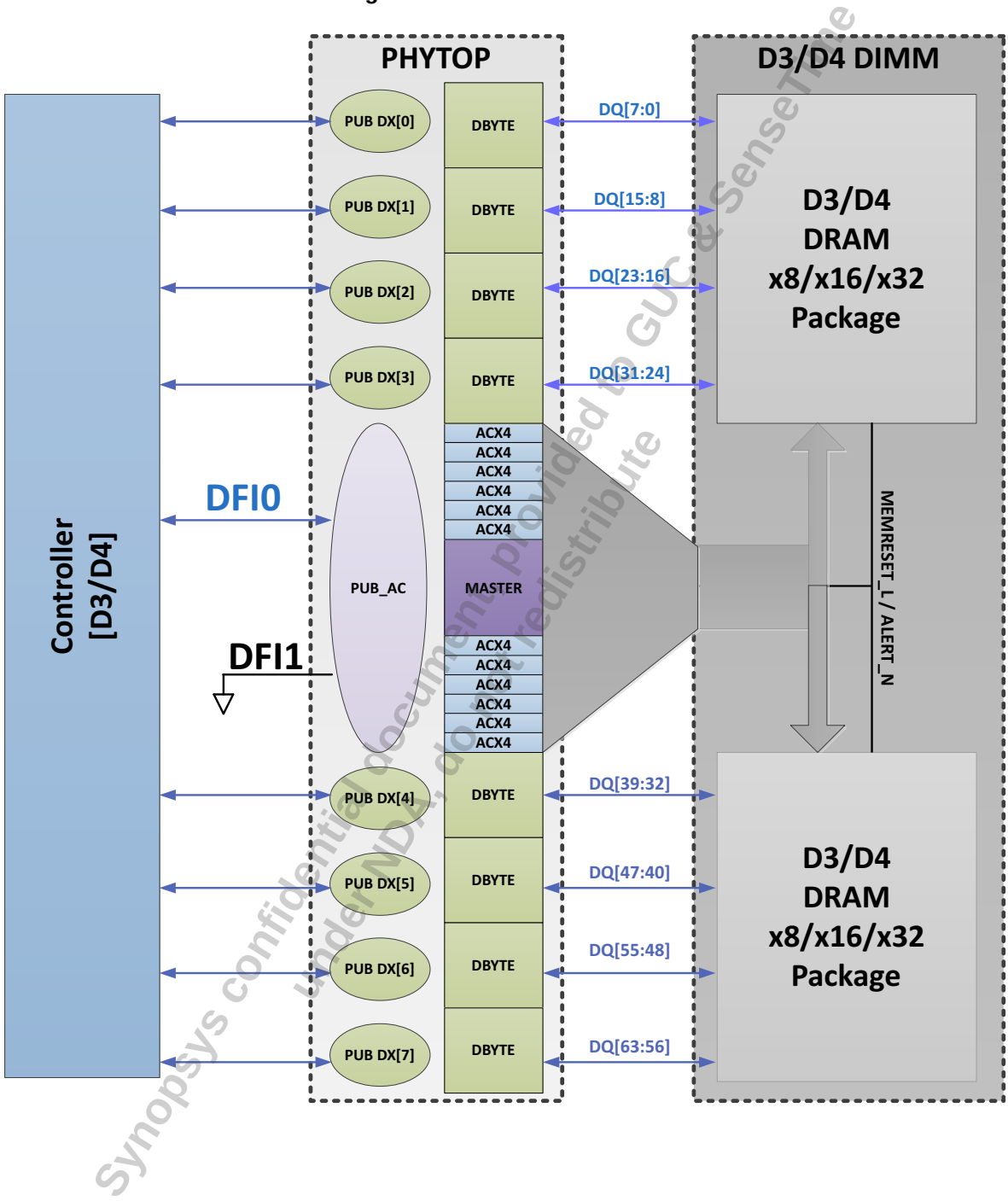
Figure 2-4 DDR4/3 DRAM x8/x16/x32 Package



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3
Signal Descriptions

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This chapter details all possible I/O signals in the PHY. Inputs are on the left of the signal diagrams; outputs are on the right.

In addition to describing the function of each signal, the signal descriptions in this chapter include the following information:

- **Active State:** Indicates whether the signal is active high or active low. When a signal is not intended to be used in a particular application, then this signal needs to be tied or driven to the in-active state (opposite of the active state).
- **Registered:** Indicates whether or not the signal is registered directly inside the IP boundary without intervening logic (excluding simple buffers). A value of No does not imply that the signal is not synchronous, only that there is some combinatorial logic between the signal's origin or destination register and the boundary of the controller. A value of N/A indicates that this information is not provided for this IP title.
- **Synchronous to:** Indicates which clock(s) in the IP sample this input (drive for an output) when considering all possible configurations. A particular configuration might not have all of the clocks listed. This clock might not be the same as the clock that your application logic should use to clock (sample/drive) this pin. For more details, consult the clock section in the databook.
- **Exists:** Name of configuration parameter(s) that populates this signal in your configuration.
- **Validated by:** Assertion or de-assertion of signal(s) that validates the signal being described.

The I/O signals are grouped as follows:

- DFI on page 47
- Reset on page 54
- Boundary Scan / Flyover Interface SignalsBypass Mode on page 55
- TDR on page 57
- Misc. on page 59
- ATPG on page 60
- APB on page 61
- SRAM on page 63
- Bump on page 65

3.1 DFI Signals

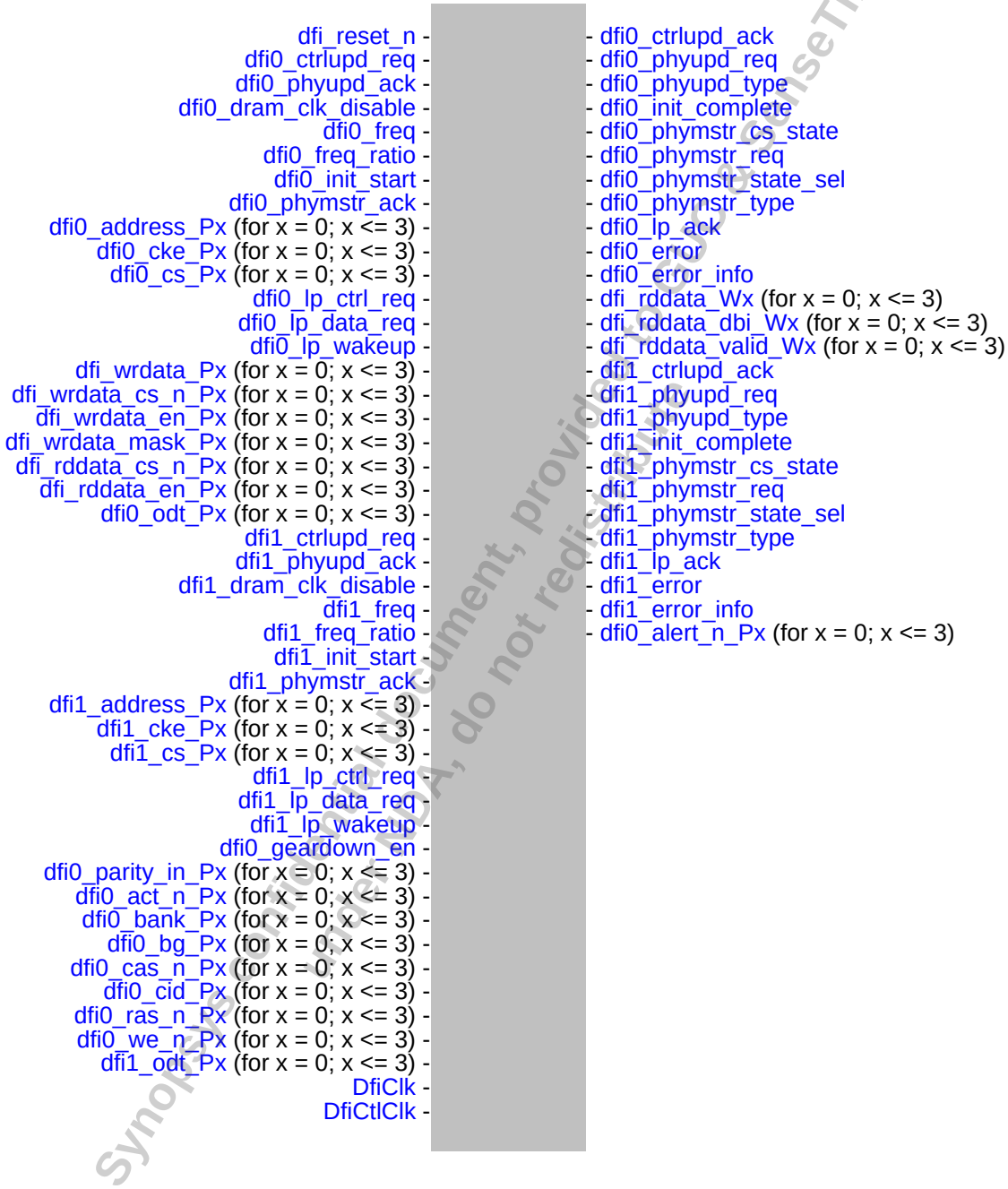

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Table 3-1 DFI Signals

Port Name	I/O	Description
dfi_reset_n	I	DFI reset bus **Exists:** Always **Synchronous To:** DfiClk
dfi0_ctrlupd_ack	O	DFI memory controller initiated update acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi0_ctrlupd_req	I	DFI memory controller initiated update request **Exists:** Always **Synchronous To:** DfiClk
dfi0_phyupd_ack	I	DFI PHY initiated update acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi0_phyupd_req	O	DFI PHY initiated update request **Exists:** Always **Synchronous To:** DfiClk
dfi0_phyupd_type[1:0]	O	DFI PHY initiated update select **Exists:** Always **Synchronous To:** DfiClk
dfi0_dram_clk_disable[3:0]	I	DFI DRAM clock disable **Exists:** Always **Synchronous To:** DfiClk
dfi0_freq[4:0]	I	DFI frequency **Exists:** Always **Synchronous To:** DfiClk
dfi0_freq_ratio[1:0]	I	DFI frequency ratio indicator **Exists:** Always **Synchronous To:** DfiClk
dfi0_init_complete	O	DFI PHY initialization complete **Exists:** Always **Synchronous To:** DfiClk
dfi0_init_start	I	DFI setup stabilization or frequency change **Exists:** Always **Synchronous To:** DfiClk

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Table 3-1 DFI Signals (Continued)

Port Name	I/O	Description
dfi0_phymstr_ack	I	DFI PHY Master Acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi0_phymstr_cs_state[1:0]	O	DFI PHY Master CS State **Exists:** Always **Synchronous To:** DfiClk
dfi0_phymstr_req	O	DFI PHY Master Request **Exists:** Always **Synchronous To:** DfiClk
dfi0_phymstr_state_sel	O	DFI PHY Master State Select **Exists:** Always **Synchronous To:** DfiClk
dfi0_phymstr_type[1:0]	O	DFI PHY Master Type **Exists:** Always **Synchronous To:** DfiClk
dfi0_address_Px[19:0] (for x = 0; x <= 3)	I	DFI address bus **Exists:** Always **Synchronous To:** DfiClk
dfi0_cke_Px[3:0] (for x = 0; x <= 3)	I	DFI clock enable **Exists:** Always **Synchronous To:** DfiClk
dfi0_cs_Px[3:0] (for x = 0; x <= 3)	I	DFI chip select **Exists:** Always **Synchronous To:** DfiClk
dfi0_lp_ack	O	DFI low power port acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi0_lp_ctrl_req	I	DFI low power port control request **Exists:** Always **Synchronous To:** DfiClk
dfi0_lp_data_req	I	DFI low power port data reqeust **Exists:** Always **Synchronous To:** DfiClk
dfi0_lp_wakeup[3:0]	I	DFI wakeup from low power **Exists:** Always **Synchronous To:** DfiClk

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Table 3-1 DFI Signals (Continued)

Port Name	I/O	Description
dfi0_error	O	DFI error **Exists:** Always **Synchronous To:** DfiClk
dfi0_error_info[3:0]	O	DFI error Info **Exists:** Always **Synchronous To:** DfiClk
dfi_wrdata_Px[(((1*DWC_DDRPHY_NUM_DBYTES)*16)-1):0] (for x = 0; x <= 3)	I	DFI write data **Exists:** Always **Synchronous To:** DfiClk
dfi_wrdata_cs_n_Px[(((4*DWC_DDRPHY_NUM_DBYTES)*1)-1):0] (for x = 0; x <= 3)	I	DFI write data chip select **Exists:** Always **Synchronous To:** DfiClk
dfi_wrdata_en_Px[(((1*DWC_DDRPHY_NUM_DBYTES)*1)-1):0] (for x = 0; x <= 3)	I	DFI write data and data mask enable **Exists:** Always **Synchronous To:** DfiClk
dfi_wrdata_mask_Px[(((1*DWC_DDRPHY_NUM_DBYTES)*2)-1):0] (for x = 0; x <= 3)	I	DFI write data byte mask **Exists:** Always **Synchronous To:** DfiClk
dfi_rddata_Wx[(((1*DWC_DDRPHY_NUM_DBYTES)*16)-1):0] (for x = 0; x <= 3)	O	DFI read data bus **Exists:** Always **Synchronous To:** DfiClk
dfi_rddata_cs_n_Px[(((4*DWC_DDRPHY_NUM_DBYTES)*1)-1):0] (for x = 0; x <= 3)	I	DFI read data chip select **Exists:** Always **Synchronous To:** DfiClk
dfi_rddata_dbi_Wx[(((1*DWC_DDRPHY_NUM_DBYTES)*2)-1):0] (for x = 0; x <= 3)	O	DFI read data DBI **Exists:** Always **Synchronous To:** DfiClk
dfi_rddata_en_Px[(((1*DWC_DDRPHY_NUM_DBYTES)*1)-1):0] (for x = 0; x <= 3)	I	DFI read data enable **Exists:** Always **Synchronous To:** DfiClk
dfi_rddata_valid_Wx[(((1*DWC_DDRPHY_NUM_DBYTES)*1)-1):0] (for x = 0; x <= 3)	O	DFI read data valid indicator **Exists:** Always **Synchronous To:** DfiClk
dfi0_odt_Px[3:0] (for x = 0; x <= 3)	I	DFI on-die termination control bus **Exists:** Always **Synchronous To:** DfiClk

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Table 3-1 DFI Signals (Continued)

Port Name	I/O	Description
dfi1_ctrlupd_ack	O	DFI memory controller initiated update acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi1_ctrlupd_req	I	DFI memory controller initiated update request **Exists:** Always **Synchronous To:** DfiClk
dfi1_phyupd_ack	I	DFI PHY initiated update acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi1_phyupd_req	O	DFI PHY initiated update request **Exists:** Always **Synchronous To:** DfiClk
dfi1_phyupd_type[1:0]	O	DFI PHY initiated update select **Exists:** Always **Synchronous To:** DfiClk
dfi1_dram_clk_disable	I	DFI DRAM clock disable **Exists:** Always **Synchronous To:** DfiClk
dfi1_freq[4:0]	I	DFI frequency **Exists:** Always **Synchronous To:** DfiClk
dfi1_freq_ratio[1:0]	I	DFI frequency ratio indicator **Exists:** Always **Synchronous To:** DfiClk
dfi1_init_complete	O	DFI PHY initialization complete **Exists:** Always **Synchronous To:** DfiClk
dfi1_init_start	I	DFI setup stabilization or frequency change **Exists:** Always **Synchronous To:** DfiClk
dfi1_phymstr_ack	I	DFI PHY Master Acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi1_phymstr_cs_state[1:0]	O	DFI PHY Master CS State **Exists:** Always **Synchronous To:** DfiClk

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Table 3-1 DFI Signals (Continued)

Port Name	I/O	Description
dfi1_phymstr_req	O	DFI PHY Master Request **Exists:** Always **Synchronous To:** DfiClk
dfi1_phymstr_state_sel	O	DFI PHY Master State Select **Exists:** Always **Synchronous To:** DfiClk
dfi1_phymstr_type[1:0]	O	DFI PHY Master Type **Exists:** Always **Synchronous To:** DfiClk
dfi1_address_Px[19:0] (for x = 0; x <= 3)	I	DFI address bus **Exists:** Always **Synchronous To:** DfiClk
dfi1_cke_Px[1:0] (for x = 0; x <= 3)	I	DFI clock enable **Exists:** Always **Synchronous To:** DfiClk
dfi1_cs_Px[1:0] (for x = 0; x <= 3)	I	DFI column address strobe **Exists:** Always **Synchronous To:** DfiClk
dfi1_lp_ack	O	DFI low power port acknowledge **Exists:** Always **Synchronous To:** DfiClk
dfi1_lp_ctrl_req	I	DFI low power port control request **Exists:** Always **Synchronous To:** DfiClk
dfi1_lp_data_req	I	DFI low power port data reqeust **Exists:** Always **Synchronous To:** DfiClk
dfi1_lp_wakeup[3:0]	I	DFI wakeup from low power **Exists:** Always **Synchronous To:** DfiClk
dfi1_error	O	DFI error **Exists:** Always **Synchronous To:** DfiClk
dfi1_error_info[3:0]	O	DFI error Info **Exists:** Always **Synchronous To:** DfiClk

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Table 3-1 DFI Signals (Continued)

Port Name	I/O	Description
dfi0_alert_n_Px (for x = 0; x <= 3)	O	DFI CRC or parity error indicator **Exists:** Always **Synchronous To:** DfiClk
dfi0_geardown_en	I	DFI geardown enable **Exists:** Always **Synchronous To:** DfiClk
dfi0_parity_in_Px (for x = 0; x <= 3)	I	DFI Parity value **Exists:** Always **Synchronous To:** DfiClk
dfi0_act_n_Px (for x = 0; x <= 3)	I	DFI activate signal **Exists:** Always **Synchronous To:** DfiClk
dfi0_bank_Px[2:0] (for x = 0; x <= 3)	I	DFI bank bs **Exists:** Always **Synchronous To:** DfiClk
dfi0_bg_Px[1:0] (for x = 0; x <= 3)	I	DFI bank group **Exists:** Always **Synchronous To:** DfiClk
dfi0_cas_n_Px (for x = 0; x <= 3)	I	DFI column address strobe **Exists:** Always **Synchronous To:** DfiClk
dfi0_cid_Px[2:0] (for x = 0; x <= 3)	I	DFI chip ID **Exists:** Always **Synchronous To:** DfiClk
dfi0_ras_n_Px (for x = 0; x <= 3)	I	DFI row address strobe **Exists:** Always **Synchronous To:** DfiClk
dfi0_we_n_Px (for x = 0; x <= 3)	I	DFI write enable signal **Exists:** Always **Synchronous To:** DfiClk
dfi1_odt_Px (for x = 0; x <= 3)	I	DFI on-die termination control bus **Exists:** Always **Synchronous To:** DfiClk
DfiClk	I	Internal DDR PHY Interface Clock. Depending on the value of the data-rate of the DRAM bus **Exists:** Always **Synchronous To:** DfiClk

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Table 3-1 DFI Signals (Continued)

Port Name	I/O	Description
DfiCtlClk	I	External DDR PHY Interface Clock. Depending on the value of the data-rate of the DRAM controller **Exists:** Always **Synchronous To:** DfiCtlClk

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3.2 Reset Signals

Table 3-2 Reset Signals

Port Name	I/O	Description
Reset	I	PHY warm reset **Exists:** Always **Synchronous To:** DfiClk
PwrOkIn	I	used to indicate coldreset as well as Retention mode (s3) entry **Exists:** Always **Synchronous To:** Async

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3.3 Boundary Scan / Flyover Interface SignalsBypass Mode

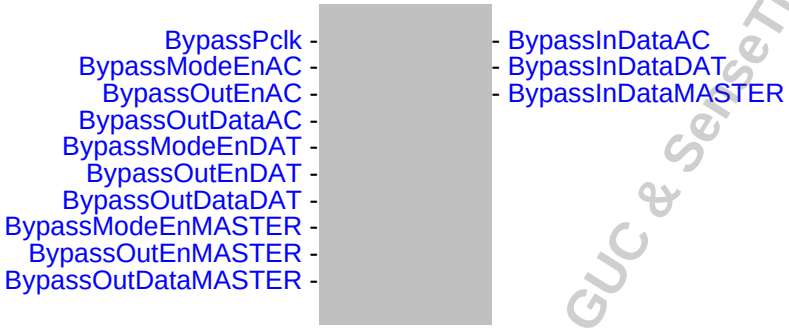

Table 3-3 Boundary Scan / Flyover Interface SignalsBypass Mode

Port Name	I/O	Description
BypassPclk	I	clock override **Exists:** Always **Synchronous To:** Pclk
BypassModeEnAC	I	asynchronous Bypass mode enable **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassOutEnAC[((DWC_DDRPHY_NUM_ANIBS*4)-1):0]	I	per lane asynchronous input enable for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassOutDataAC[((DWC_DDRPHY_NUM_ANIBS*4)-1):0]	I	per lane asynchronous input data for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassInDataAC[((DWC_DDRPHY_NUM_ANIBS*4)-1):0]	O	per lane asynchronous output data for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassModeEnDAT	I	asynchronous Bypass mode enable **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassOutEnDAT[((DWC_DDRPHY_NUM_DBYTES*12)-1):0]	I	per lane asynchronous input enable for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassOutDataDAT[((DWC_DDRPHY_NUM_DBYTES*12)-1):0]	I	per lane asynchronous input data for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk

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Table 3-3 Boundary Scan / Flyover Interface SignalsBypass Mode (Continued)

Port Name	I/O	Description
BypassInDataDAT[((DWC_DDRPHY_NUM_DBYTES*12)-1):0]	O	per lane asynchronous output data for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassModeEnMASTER	I	asynchronous Bypass mode enable **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassOutEnMASTER[1:0]	I	per lane asynchronous input enable for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassOutDataMASTER[1:0]	I	per lane asynchronous input data for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk
BypassInDataMASTER[1:0]	O	per lane asynchronous output data for Bypass mode **Exists:** Always **Synchronous To:** atpg_TxDllClk

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3.4 TDR Signals

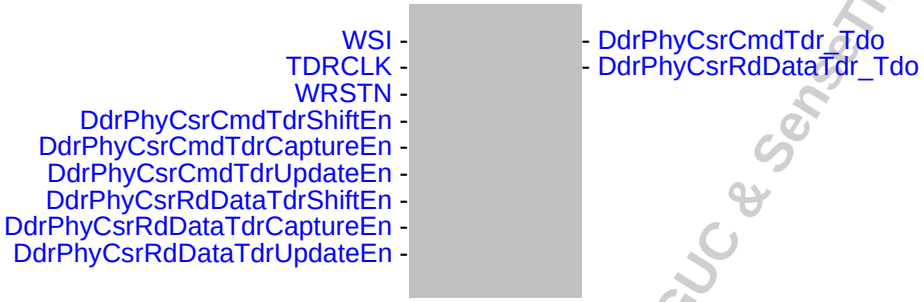

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Table 3-4 TDR Signals

Port Name	I/O	Description
WSI	I	TDR Serial Data In **Exists:** Always **Synchronous To:** TDRCLK
TDRCLK	I	TDR clock **Exists:** Always **Synchronous To:** TDRCLK
WRSTN	I	Active Low Reset to TDR Please see IEEE 1149 specification for full rules regarding WRSTN relationship to TDRCLK/TCK **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrCmdTdrShiftEn	I	TDR register control signals used to have TDR set up CfgCmd for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrCmdTdrCaptureEn	I	TDR capture enable for TDR CfgCmd for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrCmdTdrUpdateEn	I	TDR update enable for TDR CfgCmd for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrCmdTdr_Tdo	O	TDR output data for TDR CfgCmd for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK

Table 3-4 TDR Signals (Continued)

Port Name	I/O	Description
DdrPhyCsrRdDataTdrShiftEn	I	TDR register control signals used to have TDR read data back from Cfg bus to access CSRs **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrRdDataTdrCaptureEn	I	TDR capture enable for TDR Cfg for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrRdDataTdrUpdateEn	I	TDR update enable for TDR Cfg for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK
DdrPhyCsrRdDataTdr_Tdo	O	TDR output data for TDR Cfg for reads and writes of CSRs **Exists:** Always **Synchronous To:** TDRCLK

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3.5 Misc. Signals

- dwc_ddrphy_int_n
- dwc_ddrphy_dto

Table 3-5 Misc. Signals

Port Name	I/O	Description
dwc_ddrphy_int_n	O	Interrupt Output **Exists:** Always **Synchronous To:** DfiClk
dwc_ddrphy_dto	O	Digital test observation **Exists:** Always **Synchronous To:** Async

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3.6 ATPG Signals

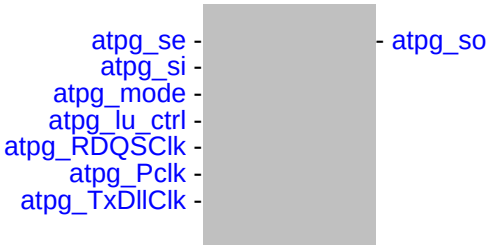

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Table 3-6 ATPG Signals

Port Name	I/O	Description
atpg_se[5:0]	I	ATPG Scan Shift Enable **Exists:** Always **Synchronous To:** DfiClk
atpg_si[(DWC_DDRPHY_NUM_TOP_SCAN_CHAINS-1):0]	I	ATPG Scan Chain Input **Exists:** Always **Synchronous To:** DfiClk
atpg_so[(DWC_DDRPHY_NUM_TOP_SCAN_CHAINS-1):0]	O	ATPG Scan Chain Output **Exists:** Always **Synchronous To:** DfiClk
atpg_mode	I	ATPG Scan Mode Enable **Exists:** Always **Synchronous To:** DfiClk
atpg_lu_ctrl[5:0]	I	ATPG Lockup Latch Enables **Exists:** Always **Synchronous To:** DfiClk
atpg_RDQSClk	I	atpg clock for DQS clk **Exists:** Always **Synchronous To:** RDQSClk
atpg_Pclk	I	atpg clock for Pclk **Exists:** Always **Synchronous To:** Pclk
atpg_TxDllClk	I	atpg clock for TxDllClk clk **Exists:** Always **Synchronous To:** TxDllClk

3.7 APB Signals

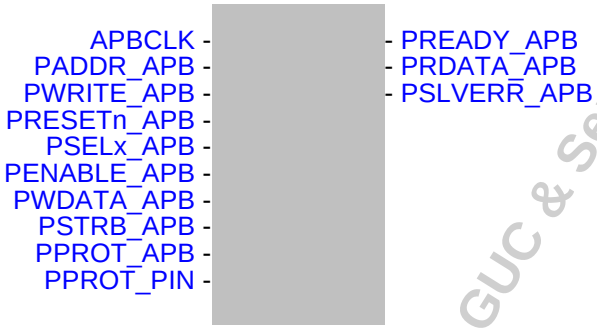

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Table 3-7 APB Signals

Port Name	I/O	Description
APBCLK	I	clock for APB interface **Exists:** Always **Synchronous To:** APBCLK
PADDR_APB[31:0]	I	Interface z Address. This is the APB address bus. **Exists:** Always **Synchronous To:** APBCLK
PWRITE_APB	I	APB write access when HIGH and an APB read access when LOW **Exists:** Always **Synchronous To:** APBCLK
PRESETn_APB	I	APB Reset **Exists:** Always **Synchronous To:** APBCLK
PSELx_APB	I	indicates that the slave device is selected **Exists:** Always **Synchronous To:** APBCLK
PENABLE_APB	I	signal indicates the second and subsequent cycles of an APB transfer **Exists:** Always **Synchronous To:** APBCLK
PWDATA_APB[15:0]	I	APB write data **Exists:** Always **Synchronous To:** APBCLK
PSTRB_APB[1:0]	I	APB write strobe **Exists:** Always **Synchronous To:** APBCLK

Table 3-7 APB Signals (Continued)

Port Name	I/O	Description
PPROT_APB[2:0]	I	APB protect type **Exists:** Always **Synchronous To:** APBCLK
PREADY_APB	O	APB ready **Exists:** Always **Synchronous To:** APBCLK
PRDATA_APB[15:0]	O	APB read data **Exists:** Always **Synchronous To:** APBCLK
PSLVERR_APB	O	APB transfer failure **Exists:** Always **Synchronous To:** APBCLK
PPROT_PIN[2:0]	I	signal indicates the second and subsequent cycles of an APB transfer **Exists:** Always **Synchronous To:** APBCLK

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3.8 SRAM Signals

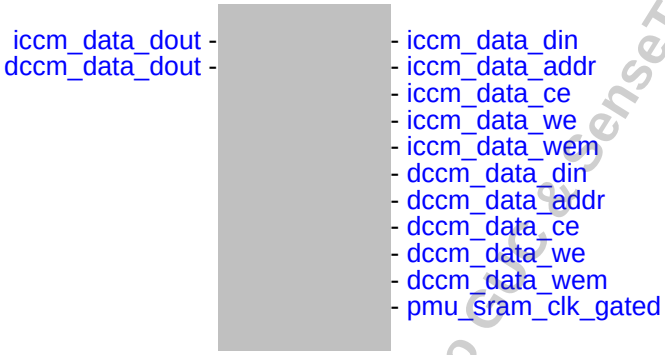

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Table 3-8 SRAM Signals

Port Name	I/O	Description
iccm_data_dout[31:0]	I	Instruction memory read data from SRAM **Exists:** Always **Synchronous To:** DfiClk
iccm_data_din[31:0]	O	Instruction memory write data to SRAM **Exists:** Always **Synchronous To:** DfiClk
iccm_data_addr[14:2]	O	Instruction memory address **Exists:** Always **Synchronous To:** DfiClk
iccm_data_ce	O	Instruction memory chip enable **Exists:** Always **Synchronous To:** DfiClk
iccm_data_we	O	Instruction memory write enable **Exists:** Always **Synchronous To:** DfiClk
iccm_data_wem[3:0]	O	Instruction memory write enable mask **Exists:** Always **Synchronous To:** DfiClk
dccm_data_dout[31:0]	I	Data Memory Read Data from SRAM **Exists:** Always **Synchronous To:** DfiClk
dccm_data_din[31:0]	O	Data memory write data to SRAM **Exists:** Always **Synchronous To:** DfiClk

Table 3-8 SRAM Signals (Continued)

Port Name	I/O	Description
dccm_data_addr[14:2]	O	Data memory address **Exists:** Always **Synchronous To:** DfiClk
dccm_data_ce	O	Data memory chip nable **Exists:** Always **Synchronous To:** DfiClk
dccm_data_we	O	Data memory write enable **Exists:** Always **Synchronous To:** DfiClk
dccm_data_wem[3:0]	O	Data memory write enable mask **Exists:** Always **Synchronous To:** DfiClk
pmu_sram_clk_gated	O	Clock from microcontroller to SRAM (gates off when processor is in Halt mode) **Exists:** Always **Synchronous To:** DfiClk

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3.9 Bump Signals

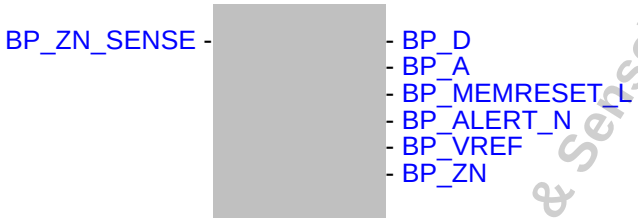

Table 3-9 Bump Signals

Port Name	I/O	Description
BP_D[((DWC_DDRPHY_NUM_DBYTES *12)-1):0]	IO	DRAM data bits and strobes **Exists:** Always **Synchronous To:** Async
BP_A[((DWC_DDRPHY_NUM_ANIBS*4)-1):0]	IO	DRAM Address and Command bits **Exists:** Always **Synchronous To:** Async
BP_MEMRESET_L	O	DRAM reset **Exists:** Always **Synchronous To:** Async
BP_ALERT_N	IO	DDR4 alert or DDR3 register error **Exists:** Always **Synchronous To:** Async
BP_VREF	IO	voltage reference for receivers and analog test point for debug **Exists:** Always **Synchronous To:** Async
BP_ZN_SENSE	I	sense bump for external resistor **Exists:** Always **Synchronous To:** Async
BP_ZN	O	calibration external reference resistor **Exists:** Always **Synchronous To:** Async

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4
Signal Mapping

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This chapter describes the following:

- "DFI Pin List and Pin Mapping" on page 68
- "DFI Interface Implementation Details" on page 107
- "Phase Bits and Chip Selects" on page 108
- "Command Phase Timing" on page 109

4.1 DFI Pin List and Pin Mapping

The DFI pin list is different based on the defines chosen. The following sections show the different DFI pins based on the following parameters/defines:

- "DWC_DDRPHY_NUM_ANIBS = 3 Defined Configuration(s)" on page 68
- "DWC_DDRPHY_NUM_ANIBS = 6 Defined Configuration(s)" on page 71
- "DWC_DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1 Defined Configuration(s)" on page 73
- "DWC_DDRPHY_NUM_ANIBS = 10 Defined Configuration(s)" on page 78
- "DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 Defined Configuration(s)" on page 83
- "DWC_DDRPHY_NUM_ANIBS = 12 Defined Configuration(s)" on page 90
- "DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1 Defined Configuration(s)" on page 97

4.1.1 DBYTE Definitions

- DBYTES assigned to CH1 (DFI0) are DBYTES{NUM_DBYTES/2 -1 … 0}
- DBYTES assigned to CH2 (DFI1) are DBYTES{(NUM_DBYTES-1) … (NUM_DBYTES/2)}

4.1.2 DWC_DDRPHY_NUM_ANIBS = 3 Defined Configuration(s)

4.1.2.1 DFI Pin List

Table 4-1 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 3

Pin Name	Direction	Description	Clock
dfi0_address_P{0..3}[5:0]	input	DFI address bus	DfiCtlClk
dfi0_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[1:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]

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Table 4-1 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 3 (Continued)

Pin Name	Direction	Description	Clock
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3}[(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]

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4.1.2.2 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 3

Table 4-2 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 3

DFI Signal	RTL Bump Name	LPDDR4 CH1 (DFI0)
dfi0_address_P{0-3}[0]	BP_A[2]	CAA0
dfi0_address_P{0-3}[1]	BP_A[3]	CAA1
dfi0_address_P{0-3}[2]	BP_A[8]	CAA2
dfi0_address_P{0-3}[3]	BP_A[9]	CAA3
dfi0_address_P{0-3}[4]	BP_A[10]	CAA4
dfi0_address_P{0-3}[5]	BP_A[11]	CAA5
dfi0_cke_P{0-3}[0]	BP_A[0]	CKEA0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKEA1
dfi0_cs_P{0-3}[0]	BP_A[6]	CSA0
dfi0_cs_P{0-3}[1]	BP_A[7]	CSA1
dfi0_dram_clk_disable[0]	BP_A[4]	CLKA_T
dfi0_dram_clk_disable[0]	BP_A[5]	CLKA_C
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQA{(8*DBYTE)+7} - DQA{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/ dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIA{DBYTE}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSA_T[DBYTE]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSA_C[DBYTE]

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4.1.3 DWC_DDRPHY_NUM_ANIBS = 6 Defined Configuration(s)

4.1.3.1 DFI Pin List

Table 4-3 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 6

Pin Name	Direction	Description	Clock
dfi0_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi0_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[1:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi0_odt_P{0..3}	input	DFI on-die termination control bus	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]

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Table 4-3 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 6 (Continued)

Pin Name	Direction	Description	Clock
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3}[(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]
dfi_wrdata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI write data and data mask enable	DfiCtlClk[1]
dfi_wrdata_mask_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data byte mask	DfiCtlClk[1]

1. when DFICTLCLK:MEMCLK = 1:2, DfiCtlClk = DfiClk

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4.1.4 DWC_DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1 Defined Configuration(s)

4.1.4.1 DFI Pin List

Table 4-4 DFI Pin List: DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1

Pin Name	Direction	Description	Clock
dfi0_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi0_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[1:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi0_odt_P{0..3}	input	DFI on-die termination control bus	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]

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Table 4-4 DFI Pin List: DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

Pin Name	Direction	Description	Clock
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi1_address_P{0..3}[5:0]	input	DFI address bus	DfiCtlClk[1]
dfi1_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi1_cs_P{0..3}[1:0]	input	DFI column address strobe	DfiCtlClk[1]
dfi1_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi1_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi1_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi1_error	output	DFI error	DfiCtlClk[1]
dfi1_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi1_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi1_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi1_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi1_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi1_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi1_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi1_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi1_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi1_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi1_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi1_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi1_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi1_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi1_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]

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Table 4-4 DFI Pin List: DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

Pin Name	Direction	Description	Clock
dfi1_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi1_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3}[(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTESNUM_ DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]
dfi_wrdata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI write data and data mask enable	DfiCtlClk[1]
dfi_wrdata_mask_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data byte mask	DfiCtlClk[1]

1. when DFICTLCLK:MEMCLK = 1:2, DfiCtlClk = DfiClk

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4.1.4.2 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1

Note

- DBYTES assigned to CH1 (DFI0) are DBYTES{floor(NUM_DBYTES/2) -1 … 0 }
- DBYTES assigned to CH2 (DFI1) are DBYTES{ (NUM_DBYTES-x) … (floor(NUM_DBYTES/2)) }
  - Where x = 1 for an even NUM_DBYTES, and x=2 for odd NUM_DBYTES
- For odd NUM_DBYTES, the most-significant DBYTE is unassigned

Table 4-5 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1

DFI Signal	RTL Bump Name	LPDDR4CHx(DFIx)
DFI Signal	**RTL Bump Name**	**LPDDR4CH1 (DFI0)**
dfi0_address_P{0-3}[0]	BP_A[2]	CAA0
dfi0_address_P{0-3}[1]	BP_A[3]	CAA1
dfi0_address_P{0-3}[2]	BP_A[8]	CAA2
dfi0_address_P{0-3}[3]	BP_A[9]	CAA3
dfi0_address_P{0-3}[4]	BP_A[10]	CAA4
dfi0_address_P{0-3}[5]	BP_A[11]	CAA5
dfi0_cke_P{0-3}[0]	BP_A[0]	CKEA0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKEA1
dfi0_cs_P{0-3}[0]	BP_A[6]	CSA0
dfi0_cs_P{0-3}[1]	BP_A[7]	CSA1
dfi0_dram_clk_disable[0]	BP_A[4]	CLKA_T
dfi0_dram_clk_disable[0]	BP_A[5]	CLKA_C
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQA{(8*DBYTE)+7} - DQA{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/ dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIA{DBYTE}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSA_T[DBYTE]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSA_C[DBYTE]
DFI Signal	**RTL Bump Name**	**LPDDR4 CH2 (DFI1)**

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Table 4-5 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 6 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

DFI Signal	RTL Bump Name	LPDDR4CHx(DFIx)
dfi1_address_P{0-3}[0]	BP_A[14]	CAB0
dfi1_address_P{0-3}[1]	BP_A[15]	CAB1
dfi1_address_P{0-3}[2]	BP_A[20]	CAB2
dfi1_address_P{0-3}[3]	BP_A[21]	CAB3
dfi1_address_P{0-3}[4]	BP_A[22]	CAB4
dfi1_address_P{0-3}[5]	BP_A[23]	CAB5
dfi1_cke_P{0-3}[0]	BP_A[12]	CKEB0
dfi1_cke_P{0-3}[1]	BP_A[13]	CKEB1
dfi1_cs_P{0-3}[0]	BP_A[18]	CSB0
dfi1_cs_P{0-3}[1]	BP_A[19]	CSB1
dfi1_dram_clk_disable[0]	BP_A[16]	CLKB_T
dfi1_dram_clk_disable[0]	BP_A[17]	CLKB_C
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQB{(8*(DBYTE-2)+7} - DQB{(8*(DBYTE-2))}
dfi_wrdata_mask_P{0-3}/ dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIB{(DBYTE-2)}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSB_T[(DBYTE-2)]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSB_C[(DBYTE-2)]

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4.1.5 DWC_DDRPHY_NUM_ANIBS = 10 Defined Configuration(s)

4.1.5.1 DFI Pin List

Table 4-6 DFI Pin List: WC_DDRPHY_NUM_ANIBS = 10

Pin Name	Direction	Description	Clock
dfi0_act_n_P{0..3}	input	DFI activate signal	DfiCtlClk[1]
dfi0_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi0_alert_n_P{0..3}	output	DFI CRC or parity error indicator	DfiCtlClk[1]
dfi0_bank_P{0..3}[2:0]	input	DFI bank bs	DfiCtlClk[1]
dfi0_bg_P{0..3}[1:0]	input	DFI bank group	DfiCtlClk[1]
dfi0_cas_n_P{0..3}	input	DFI column address strobe	DfiCtlClk[1]
dfi0_cid_P{0..3}[2:0]	input	DFI chip ID	DfiCtlClk[1]
dfi0_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[1:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi0_odt_P{0..3}[1:0]	input	DFI on-die termination control bus	DfiCtlClk[1]

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Table 4-6 DFI Pin List: WC_DDRPHY_NUM_ANIBS = 10 (Continued)

Pin Name	Direction	Description	Clock
dfi0_parity_in_P{0..3}	input	DFI Parity value	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi0_ras_n_P{0..3}	input	DFI row address strobe	DfiCtlClk[1]
dfi0_we_n_P{0..3}	input	DFI write enable signal	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3}[(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]
dfi_wrdata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI write data and data mask enable	DfiCtlClk[1]
dfi_wrdata_mask_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data byte mask	DfiCtlClk[1]

1. when DFICTLCLK:MEMCLK = 1:2, DfiCtlClk = DfiClk

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4.1.5.2 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10

Table 4-7 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_act_n_P{0-3}[0]	BP_A[6]	ACT_N
dfi0_address_P{0-3}[0]	BP_A[31]	A0
dfi0_address_P{0-3}[1]	BP_A[25]	A1
dfi0_address_P{0-3}[2]	BP_A[24]	A2
dfi0_address_P{0-3}[3]	BP_A[15]	A3
dfi0_address_P{0-3}[4]	BP_A[14]	A4
dfi0_address_P{0-3}[5]	BP_A[13]	A5
dfi0_address_P{0-3}[6]	BP_A[12]	A6
dfi0_address_P{0-3}[7]	BP_A[10]	A7
dfi0_address_P{0-3}[8]	BP_A[11]	A8
dfi0_address_P{0-3}[9]	BP_A[7]	A9
dfi0_address_P{0-3}[10]	BP_A[30]	A10
dfi0_address_P{0-3}[11]	BP_A[9]	A11
dfi0_address_P{0-3}[12]	BP_A[8]	A12
dfi0_address_P{0-3}[13]	BP_A[28]	A13
dfi0_alert_n_P{0-3}[0]	BP_ALERT_L	ALERT_N
dfi0_bank_P{0-3}[0]	BP_A[29]	BA0
dfi0_bank_P{0-3}[1]	BP_A[26]	BA1
dfi0_bg_P{0-3}[0]	BP_A[4]	BG0
dfi0_bg_P{0-3}[1]	BP_A[5]	BG1
dfi0_cas_n_P{0-3}[0]	BP_A[33]	CAS_N
dfi0_cid_P{0-3}[0]	BP_A[3]	C0
dfi0_cid_P{0-3}[1]	BP_A[39]	C1
dfi0_cid_P{0-3}[2]	BP_A[32]	C2
dfi0_cke_P{0-3}[0]	BP_A[0]	CKE0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKE1

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Table 4-7 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 (Continued)

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_cs_P{0-3}[0]	BP_A[2]	CS_N0
dfi0_cs_P{0-3}[1]	BP_A[38]	CS_N1
dfi0_dram_clk_disable[0]	BP_A[16]	CLK0_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLK0_C
dfi0_dram_clk_disable[1]	BP_A[20]	CLK1_T
dfi0_dram_clk_disable[1]	BP_A[21]	CLK1_C
dfi0_odt_P{0-3}[0]	BP_A[36]	ODT0
dfi0_odt_P{0-3}[1]	BP_A[37]	ODT1
dfi0_parity_in_P{0-3}[0]	BP_A[27]	PAR
dfi0_ras_n_P{0-3}[0]	BP_A[35]	RAS_N
dfi0_we_n_P{0-3}[0]	BP_A[34]	WE_N
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQ{(8*DBYTE)+7} - DQ{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBI{DBYTE}
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+10,(DBYTE*12)+9]	DQS_C[DBYTE],DQS_T[DBYTE]

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4.1.5.3 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10

Table 4-8 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10

DFI Signal	RTL Bump Name	LPDDR4 CH1 (DFI0)
dfi0_address_P{0-3}[0]	BP_A[8]	CAA0
dfi0_address_P{0-3}[1]	BP_A[9]	CAA1
dfi0_address_P{0-3}[2]	BP_A[10]	CAA2
dfi0_address_P{0-3}[3]	BP_A[11]	CAA3
dfi0_address_P{0-3}[4]	BP_A[12]	CAA4
dfi0_address_P{0-3}[5]	BP_A[13]	CAA5
dfi0_cke_P{0-3}[0]	BP_A[0]	CKEA0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKEA1
dfi0_cs_P{0-3}[0]	BP_A[2]	CSA0
dfi0_cs_P{0-3}[1]	BP_A[3]	CSA1
dfi0_dram_clk_disable[0]	BP_A[4]	CLKA_T
dfi0_dram_clk_disable[0]	BP_A[5]	CLKA_C
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQA{(8*DBYTE)+7} - DQA{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIA{DBYTE}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSA_T[DBYTE]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSA_C[DBYTE]

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4.1.6 DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 Defined Configuration(s)

4.1.6.1 DFI Pin List

Table 4-9 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1

Pin Name	Direction	Description	Clock
dfi0_act_n_P{0..3}	input	DFI activate signal	DfiCtlClk
dfi0_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi0_alert_n_P{0..3}	output	DFI CRC or parity error indicator	DfiCtlClk[1]
dfi0_bank_P{0..3}[2:0]	input	DFI bank bs	DfiCtlClk[1]
dfi0_bg_P{0..3}[1:0]	input	DFI bank group	DfiCtlClk[1]
dfi0_cas_n_P{0..3}	input	DFI column address strobe	DfiCtlClk[1]
dfi0_cid_P{0..3}[2:0]	input	DFI chip ID	DfiCtlClk[1]
dfi0_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[1:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable[3:0]	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]

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Table 4-9 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

Pin Name	Direction	Description	Clock
dfi0_odt_P{0..3}[1:0]	input	DFI on-die termination control bus	DfiCtlClk[1]
dfi0_parity_in_P{0..3}	input	DFI Parity value	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi0_ras_n_P{0..3}	input	DFI row address strobe	DfiCtlClk[1]
dfi0_we_n_P{0..3}	input	DFI write enable signal	DfiCtlClk[1]
dfi1_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi1_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi1_cs_P{0..3}[1:0]	input	DFI column address strobe	DfiCtlClk[1]
dfi1_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi1_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi1_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi1_error	output	DFI error	DfiCtlClk[1]
dfi1_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi1_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi1_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi1_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi1_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi1_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi1_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]

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Table 4-9 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

Pin Name	Direction	Description	Clock
dfi1_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi1_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi1_odt_P{0..3}	input	DFI on-die termination control bus	DfiCtlClk[1]
dfi1_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi1_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi1_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi1_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi1_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi1_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi1_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi1_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3}[(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]
dfi_wrdata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI write data and data mask enable	DfiCtlClk[1]
dfi_wrdata_mask_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data byte mask	DfiCtlClk[1]

1. when DFICTLCLK:MEMCLK = 1:2, DfiCtlClk = DfiClk

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4.1.6.2 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1

Table 4-10 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 for DDR4 Mode

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_act_n_P{0-3}[0]	BP_A[6]	ACT_N
dfi0_address_P{0-3}[0]	BP_A[31]	A0
dfi0_address_P{0-3}[1]	BP_A[25]	A1
dfi0_address_P{0-3}[2]	BP_A[24]	A2
dfi0_address_P{0-3}[3]	BP_A[15]	A3
dfi0_address_P{0-3}[4]	BP_A[14]	A4
dfi0_address_P{0-3}[5]	BP_A[13]	A5
dfi0_address_P{0-3}[6]	BP_A[12]	A6
dfi0_address_P{0-3}[7]	BP_A[10]	A7
dfi0_address_P{0-3}[8]	BP_A[11]	A8
dfi0_address_P{0-3}[9]	BP_A[7]	A9
dfi0_address_P{0-3}[10]	BP_A[30]	A10
dfi0_address_P{0-3}[11]	BP_A[9]	A11
dfi0_address_P{0-3}[12]	BP_A[8]	A12
dfi0_address_P{0-3}[13]	BP_A[28]	A13
dfi0_alert_n_P{0-3}[0]	BP_ALERT_L	ALERT_N
dfi0_bank_P{0-3}[0]	BP_A[29]	BA0
dfi0_bank_P{0-3}[1]	BP_A[26]	BA1
dfi0_bg_P{0-3}[0]	BP_A[4]	BG0
dfi0_bg_P{0-3}[1]	BP_A[5]	BG1
dfi0_cas_n_P{0-3}[0]	BP_A[33]	CAS_N
dfi0_cid_P{0-3}[0]	BP_A[3]	C0
dfi0_cid_P{0-3}[1]	BP_A[39]	C1
dfi0_cid_P{0-3}[2]	BP_A[32]	C2
dfi0_cke_P{0-3}[0]	BP_A[0]	CKE0

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Table 4-10 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 for DDR4 Mode (Continued)

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_cke_P{0-3}[1]	BP_A[1]	CKE1
dfi0_cs_P{0-3}[0]	BP_A[2]	CS_N0
dfi0_cs_P{0-3}[1]	BP_A[38]	CS_N1
dfi0_dram_clk_disable[0]	BP_A[16]	CLK0_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLK0_C
dfi0_dram_clk_disable[1]	BP_A[20]	CLK1_T
dfi0_dram_clk_disable[1]	BP_A[21]	CLK1_C
dfi0_odt_P{0-3}[0]	BP_A[36]	ODT0
dfi0_odt_P{0-3}[1]	BP_A[37]	ODT1
dfi0_parity_in_P{0-3}[0]	BP_A[27]	PAR
dfi0_ras_n_P{0-3}[0]	BP_A[35]	RAS_N
dfi0_we_n_P{0-3}[0]	BP_A[34]	WE_N
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQ{(8*DBYTE)+7} - DQ{(8*DBYTE)}

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4.1.6.3 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1

Note

- DBYTES assigned to CH1 (DFI0) are DBYTES{floor(NUM_DBYTES/2) -1 … 0 }
- DBYTES assigned to CH2 (DFI1) are DBYTES{ (NUM_DBYTES-x) … (floor(NUM_DBYTES/2)) }
  - Where x = 1 for an even NUM_DBYTES, and x=2 for odd NUM_DBYTES
- For odd NUM_DBYTES, the most-significant DBYTE is unassigned

Table 4-11 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1

DFI Signal	RTL Bump Name	LPDDR4CHx (DFIx)
DFI Signal	**RTL Bump Name**	**LPDDR4CH1 (DFI0)**
dfi0_address_P{0-3}[0]	BP_A[8]	CAA0
dfi0_address_P{0-3}[1]	BP_A[9]	CAA1
dfi0_address_P{0-3}[2]	BP_A[10]	CAA2
dfi0_address_P{0-3}[3]	BP_A[11]	CAA3
dfi0_address_P{0-3}[4]	BP_A[12]	CAA4
dfi0_address_P{0-3}[5]	BP_A[13]	CAA5
dfi0_cke_P{0-3}[0]	BP_A[0]	CKEA0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKEA1
dfi0_cs_P{0-3}[0]	BP_A[2]	CSA0
dfi0_cs_P{0-3}[1]	BP_A[3]	CSA1
dfi0_dram_clk_disable[0]	BP_A[4]	CLKA_T
dfi0_dram_clk_disable[0]	BP_A[5]	CLKA_C
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQA{(8*DBYTE)+7} - DQA{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIA{DBYTE}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSA_T[DBYTE]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSA_C[DBYTE]
DFI_signal	**RTL Bump Name**	**LPDDR4 CH2 (DFI1)**

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Table 4-11 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 10 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

DFI Signal	RTL Bump Name	LPDDR4CHx (DFIx)
dfi1_address_P{0-3}[0]	BP_A[28]	CAB0
dfi1_address_P{0-3}[1]	BP_A[29]	CAB1
dfi1_address_P{0-3}[2]	BP_A[30]	CAB2
dfi1_address_P{0-3}[3]	BP_A[31]	CAB3
dfi1_address_P{0-3}[4]	BP_A[32]	CAB4
dfi1_address_P{0-3}[5]	BP_A[33]	CAB5
dfi1_cke_P{0-3}[0]	BP_A[20]	CKEB0
dfi1_cke_P{0-3}[1]	BP_A[21]	CKEB1
dfi1_cs_P{0-3}[0]	BP_A[23]	CSB0
dfi1_cs_P{0-3}[1]	BP_A[22]	CSB1
dfi1_dram_clk_disable[0]	BP_A[24]	CLKB_T
dfi1_dram_clk_disable[0]	BP_A[25]	CLKB_C
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQB{(8*(DBYTE-4)+7} - DQB{(8*(DBYTE-4))}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIB{(DBYTE-4)}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSB_T[(DBYTE-4)]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSB_C[(DBYTE-4)]

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4.1.7 DWC_DDRPHY_NUM_ANIBS = 12 Defined Configuration(s)

4.1.7.1 DFI Pin List

Table 4-12 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 12

Pin Name	Direction	Description	Clock
dfi0_act_n_P{0..3}	input	DFI activate signal	DfiCtlClk[1]
dfi0_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi0_alert_n_P{0..3}	output	DFI CRC or parity error indicator	DfiCtlClk[1]
dfi0_bank_P{0..3}[2:0]	input	DFI bank bs	DfiCtlClk[1]
dfi0_bg_P{0..3}[1:0]	input	DFI bank group	DfiCtlClk[1]
dfi0_cas_n_P{0..3}	input	DFI column address strobe	DfiCtlClk[1]
dfi0_cid_P{0..3}[2:0]	input	DFI chip ID	DfiCtlClk[1]
dfi0_cke_P{0..3}[3:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[3:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable[3:0]	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi0_odt_P{0..3}[3:0]	input	DFI on-die termination control bus	DfiCtlClk[1]

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Table 4-12 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 12 (Continued)

Pin Name	Direction	Description	Clock
dfi0_parity_in_P{0..3}	input	DFI Parity value	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi0_ras_n_P{0..3}	input	DFI row address strobe	DfiCtlClk[1]
dfi0_we_n_P{0..3}	input	DFI write enable signal	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3} [(4*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3} [(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3} [(4*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]
dfi_wrdata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI write data and data mask enable	DfiCtlClk[1]
dfi_wrdata_mask_P{0..3} [(2*NUM_DBYTES)-1:0]	input	DFI write data byte mask	DfiCtlClk[1]

1. when DFICTLCLK:MEMCLK = 1:2, DfiCtlClk = DfiClk

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4.1.7.2 DDR4 ALT DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12

Table 4-13 DDR4 ALT DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12

DFI Signal	RTL Bump Name	DDR4 ALT CH1 (DFI0)
dfi0_act_n_P{0-3}[0]	BP_A[6]	ACT_N
dfi0_address_P{0-3}[0]	BP_A[31]	A0
dfi0_address_P{0-3}[1]	BP_A[25]	A1
dfi0_address_P{0-3}[2]	BP_A[24]	A2
dfi0_address_P{0-3}[3]	BP_A[15]	A3
dfi0_address_P{0-3}[4]	BP_A[14]	A4
dfi0_address_P{0-3}[5]	BP_A[13]	A5
dfi0_address_P{0-3}[6]	BP_A[12]	A6
dfi0_address_P{0-3}[7]	BP_A[10]	A7
dfi0_address_P{0-3}[8]	BP_A[11]	A8
dfi0_address_P{0-3}[9]	BP_A[7]	A9
dfi0_address_P{0-3}[10]	BP_A[30]	A10
dfi0_address_P{0-3}[11]	BP_A[9]	A11
dfi0_address_P{0-3}[12]	BP_A[8]	A12
dfi0_address_P{0-3}[13]	BP_A[28]	A13
dfi0_alert_n_P{0-3}[0]	BP_ALERT_L	ALERT_N
dfi0_bank_P{0-3}[0]	BP_A[29]	BA0
dfi0_bank_P{0-3}[1]	BP_A[26]	BA1
dfi0_bg_P{0-3}[0]	BP_A[4]	BG0
dfi0_bg_P{0-3}[1]	BP_A[5]	BG1
dfi0_cas_n_P{0-3}[0]	BP_A[33]	CAS_N
dfi0_cid_P{0-3}[0]	BP_A[37]	C0
dfi0_cid_P{0-3}[1]	BP_A[41]	C1
dfi0_cid_P{0-3}[2]	BP_A[38]	C2
dfi0_cke_P{0-3}[0]	BP_A[0]	CKE0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKE1

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Table 4-13 DDR4 ALT DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12 (Continued)

DFI Signal	RTL Bump Name	DDR4 ALT CH1 (DFI0)
dfi0_cs_P{0-3}[0]	BP_A[36]	CS_N0
dfi0_cs_P{0-3}[1]	BP_A[40]	CS_N1
dfi0_dram_clk_disable[0]	BP_A[16]	CLK0_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLK0_C
dfi0_dram_clk_disable[1]	BP_A[20]	CLK1_T
dfi0_dram_clk_disable[1]	BP_A[21]	CLK1_C
dfi0_odt_P{0-3}[0]	BP_A[39]	ODT0
dfi0_odt_P{0-3}[1]	BP_A[45]	ODT1
dfi0_parity_in_P{0-3}[0]	BP_A[27]	PAR
dfi0_ras_n_P{0-3}[0]	BP_A[35]	RAS_N
dfi0_we_n_P{0-3}[0]	BP_A[34]	WE_N
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQ{(8*DBYTE)+7} - DQ{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBI{DBYTE}
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+10,(DBYTE*12)+9]	DQS_C[DBYTE],DQS_T[DBYTE]

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4.1.7.3 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12

Table 4-14 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_act_n_P{0-3}[0]	BP_A[6]	ACT_N
dfi0_address_P{0-3}[0]	BP_A[31]	A0
dfi0_address_P{0-3}[1]	BP_A[25]	A1
dfi0_address_P{0-3}[2]	BP_A[24]	A2
dfi0_address_P{0-3}[3]	BP_A[15]	A3
dfi0_address_P{0-3}[4]	BP_A[14]	A4
dfi0_address_P{0-3}[5]	BP_A[13]	A5
dfi0_address_P{0-3}[6]	BP_A[12]	A6
dfi0_address_P{0-3}[7]	BP_A[10]	A7
dfi0_address_P{0-3}[8]	BP_A[11]	A8
dfi0_address_P{0-3}[9]	BP_A[7]	A9
dfi0_address_P{0-3}[10]	BP_A[30]	A10
dfi0_address_P{0-3}[11]	BP_A[9]	A11
dfi0_address_P{0-3}[12]	BP_A[8]	A12
dfi0_address_P{0-3}[13]	BP_A[28]	A13
dfi0_address_P{0-3}[17]	BP_A[39]	A17
dfi0_alert_n_P{0-3}[0]	BP_ALERT_L	ALERT_N
dfi0_bank_P{0-3}[0]	BP_A[29]	BA0
dfi0_bank_P{0-3}[1]	BP_A[26]	BA1
dfi0_bg_P{0-3}[0]	BP_A[4]	BG0
dfi0_bg_P{0-3}[1]	BP_A[5]	BG1
dfi0_cas_n_P{0-3}[0]	BP_A[33]	CAS_N
dfi0_cid_P{0-3}[0]	BP_A[36]	C0
dfi0_cid_P{0-3}[1]	BP_A[37]	C1
dfi0_cid_P{0-3}[2]	BP_A[38]	C2
dfi0_cke_P{0-3}[0]	BP_A[0]	CKE0

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Table 4-14 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_cke_P{0-3}[1]	BP_A[1]	CKE1
dfi0_cke_P{0-3}[2]	BP_A[2]	CKE2
dfi0_cke_P{0-3}[3]	BP_A[3]	CKE3
dfi0_cs_P{0-3}[0]	BP_A[40]	CS_N0
dfi0_cs_P{0-3}[1]	BP_A[41]	CS_N1
dfi0_cs_P{0-3}[2]	BP_A[42]	CS_N2
dfi0_cs_P{0-3}[3]	BP_A[43]	CS_N3
dfi0_dram_clk_disable[0]	BP_A[16]	CLK0_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLK0_C
dfi0_dram_clk_disable[1]	BP_A[20]	CLK1_T
dfi0_dram_clk_disable[1]	BP_A[21]	CLK1_C
dfi0_dram_clk_disable[2]	BP_A[18]	CLK2_T
dfi0_dram_clk_disable[2]	BP_A[19]	CLK2_C
dfi0_dram_clk_disable[3]	BP_A[22]	CLK3_T
dfi0_dram_clk_disable[3]	BP_A[23]	CLK3_C
dfi0_odt_P{0-3}[0]	BP_A[44]	ODT0
dfi0_odt_P{0-3}[1]	BP_A[45]	ODT1
dfi0_odt_P{0-3}[2]	BP_A[46]	ODT2
dfi0_odt_P{0-3}[3]	BP_A[47]	ODT3
dfi0_parity_in_P{0-3}[0]	BP_A[27]	PAR
dfi0_ras_n_P{0-3}[0]	BP_A[35]	RAS_N
dfi0_we_n_P{0-3}[0]	BP_A[34]	WE_N
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQ{(8*DBYTE)+7} - DQ{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBI{DBYTE}
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+10,(DBYTE*12)+9]	DQS_C[DBYTE],DQS_T[DBYTE]

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4.1.7.4 LPDDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12

Table 4-15 DFI Pin Mapping When DWC_DDRPHY_NUM_ANIBS = 12 for LPDDR4 Mode

DFI Signal	RTL Bump Name	LPDDR4CH1(DFI0)
dfi0_address_P{0-3}[0]	BP_A[13]	CAA0
dfi0_address_P{0-3}[1]	BP_A[7]	CAA1
dfi0_address_P{0-3}[2]	BP_A[12]	CAA2
dfi0_address_P{0-3}[3]	BP_A[11]	CAA3
dfi0_address_P{0-3}[4]	BP_A[10]	CAA4
dfi0_address_P{0-3}[5]	BP_A[4]	CAA5
dfi0_cke_P{0-3}[0]	BP_A[0]	CKEA0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKEA1
dfi0_cs_P{0-3}[0]	BP_A[36]	CSA0
dfi0_cs_P{0-3}[1]	BP_A[37]	CSA1
dfi0_dram_clk_disable[0]	BP_A[16]	CLKA_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLKA_C
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQA{(8*DBYTE)+7} - DQA{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIA{DBYTE}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSA_T[DBYTE]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSA_C[DBYTE]

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4.1.8 DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1 Defined Configuration(s)

4.1.8.1 DFI Pin List

Table 4-16 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1

Pin Name	Direction	Description	Clock
dfi0_act_n_P{0..3}	input	DFI activate signal	DfiCtlClk[1]
dfi0_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi0_alert_n_P{0..3}	output	DFI CRC or parity error indicator	DfiCtlClk[1]
dfi0_bank_P{0..3}[2:0]	input	DFI bank bs	DfiCtlClk[1]
dfi0_bg_P{0..3}[1:0]	input	DFI bank group	DfiCtlClk[1]
dfi0_cas_n_P{0..3}	input	DFI column address strobe	DfiCtlClk[1]
dfi0_cid_P{0..3}[2:0]	input	DFI chip ID	DfiCtlClk[1]
dfi0_cke_P{0..3}[3:0]	input	DFI clock enable	DfiCtlClk[1]
dfi0_cs_P{0..3}[3:0]	input	DFI chip select	DfiCtlClk[1]
dfi0_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi0_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi0_dram_clk_disable[3:0]	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi0_error	output	DFI error	DfiCtlClk[1]
dfi0_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi0_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi0_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi0_geardown_en	input	DFI geardown enable	DfiCtlClk[1]
dfi0_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi0_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi0_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi0_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]
dfi0_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi0_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]

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Table 4-16 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

Pin Name	Direction	Description	Clock
dfi0_odt_P{0..3}[3:0]	input	DFI on-die termination control bus	DfiCtlClk[1]
dfi0_parity_in_P{0..3}	input	DFI Parity value	DfiCtlClk[1]
dfi0_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi0_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi0_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi0_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi0_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi0_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi0_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi0_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi0_ras_n_P{0..3}	input	DFI row address strobe	DfiCtlClk[1]
dfi0_we_n_P{0..3}	input	DFI write enable signal	DfiCtlClk[1]
dfi1_address_P{0..3}[19:0]	input	DFI address bus	DfiCtlClk[1]
dfi1_cke_P{0..3}[1:0]	input	DFI clock enable	DfiCtlClk[1]
dfi1_cs_P{0..3}[1:0]	input	DFI column address strobe	DfiCtlClk[1]
dfi1_ctrlupd_ack	output	DFI memory controller initiated update acknowledge	DfiCtlClk[1]
dfi1_ctrlupd_req	input	DFI memory controller initiated update request	DfiCtlClk[1]
dfi1_dram_clk_disable	input	DFI DRAM clock disable	DfiCtlClk[1]
dfi1_error	output	DFI error	DfiCtlClk[1]
dfi1_error_info[3:0]	output	DFI error Info	DfiCtlClk[1]
dfi1_freq[4:0]	input	DFI frequency	DfiCtlClk[1]
dfi1_freq_ratio[1:0]	input	DFI frequency ratio indicator	DfiCtlClk[1]
dfi1_init_complete	output	DFI PHY initialization complete	DfiCtlClk[1]
dfi1_init_start	input	DFI setup stabilization or frequency change	DfiCtlClk[1]
dfi1_lp_ack	output	DFI low power port acknowledge	DfiCtlClk[1]
dfi1_lp_ctrl_req	input	DFI low power port control request	DfiCtlClk[1]

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Table 4-16 DFI Pin List: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

Pin Name	Direction	Description	Clock
dfi1_lp_data_req	input	DFI low power port data reqeust	DfiCtlClk[1]
dfi1_lp_wakeup[3:0]	input	DFI wakeup from low power	DfiCtlClk[1]
dfi1_odt_P{0..3}	input	DFI on-die termination control bus	DfiCtlClk[1]
dfi1_phymstr_ack	input	DFI PHY Master Acknowledge	DfiCtlClk[1]
dfi1_phymstr_cs_state[1:0]	output	DFI PHY Master CS State	DfiCtlClk[1]
dfi1_phymstr_req	output	DFI PHY Master Request	DfiCtlClk[1]
dfi1_phymstr_state_sel	output	DFI PHY Master State Select	DfiCtlClk[1]
dfi1_phymstr_type[1:0]	output	DFI PHY Master Type	DfiCtlClk[1]
dfi1_phyupd_ack	input	DFI PHY initiated update acknowledge	DfiCtlClk[1]
dfi1_phyupd_req	output	DFI PHY initiated update request	DfiCtlClk[1]
dfi1_phyupd_type[1:0]	output	DFI PHY initiated update select	DfiCtlClk[1]
dfi_rddata_W{0..3}[(16*NUM_DBYTES)-1:0]	output	DFI read data bus	DfiCtlClk[1]
dfi_rddata_cs_n_P{0..3}[(4*NUM_DBYTES)-1:0]	input	DFI read data chip select	DfiCtlClk[1]
dfi_rddata_dbi_W{0..3}[(2*NUM_DBYTES)-1:0]	output	DFI read data DBI	DfiCtlClk[1]
dfi_rddata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI read data enable	DfiCtlClk[1]
dfi_rddata_valid_W{0..3}[NUM_DBYTES-1:0]	output	DFI read data valid indicator	DfiCtlClk[1]
dfi_reset_n	input	DFI reset bus	DfiCtlClk[1]
dfi_wrdata_P{0..3}[(16*NUM_DBYTES)-1:0]	input	DFI write data	DfiCtlClk[1]
dfi_wrdata_cs_n_P{0..3}[(4*NUM_DBYTES)-1:0]	input	DFI write data chip select	DfiCtlClk[1]
dfi_wrdata_en_P{0..3}[NUM_DBYTES-1:0]	input	DFI write data and data mask enable	DfiCtlClk[1]
dfi_wrdata_mask_P{0..3}[(2*NUM_DBYTES)-1:0]	input	DFI write data byte mask	DfiCtlClk[1]

1. when DFICTLCLK:MEMCLK = 1:2, DfiCtlClk = DfiClk

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4.1.8.2 DDR4-ALT DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1

Table 4-17 DDR4-ALT DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1

DFI Signal	RTL Bump Name	DDR4-ALT CH1 (DFI0)
dfi0_act_n_P{0-3}[0]	BP_A[6]	ACT_N
dfi0_address_P{0-3}[0]	BP_A[31]	A0
dfi0_address_P{0-3}[1]	BP_A[25]	A1
dfi0_address_P{0-3}[2]	BP_A[24]	A2
dfi0_address_P{0-3}[3]	BP_A[15]	A3
dfi0_address_P{0-3}[4]	BP_A[14]	A4
dfi0_address_P{0-3}[5]	BP_A[13]	A5
dfi0_address_P{0-3}[6]	BP_A[12]	A6
dfi0_address_P{0-3}[7]	BP_A[10]	A7
dfi0_address_P{0-3}[8]	BP_A[11]	A8
dfi0_address_P{0-3}[9]	BP_A[7]	A9
dfi0_address_P{0-3}[10]	BP_A[30]	A10
dfi0_address_P{0-3}[11]	BP_A[9]	A11
dfi0_address_P{0-3}[12]	BP_A[8]	A12
dfi0_address_P{0-3}[13]	BP_A[28]	A13
dfi0_alert_n_P{0-3}[0]	BP_ALERT_L	ALERT_N
dfi0_bank_P{0-3}[0]	BP_A[29]	BA0
dfi0_bank_P{0-3}[1]	BP_A[26]	BA1
dfi0_bg_P{0-3}[0]	BP_A[4]	BG0
dfi0_bg_P{0-3}[1]	BP_A[5]	BG1
dfi0_cas_n_P{0-3}[0]	BP_A[33]	CAS_N
dfi0_cid_P{0-3}[0]	BP_A[37]	C0
dfi0_cid_P{0-3}[1]	BP_A[41]	C1
dfi0_cid_P{0-3}[2]	BP_A[38]	C2
dfi0_cke_P{0-3}[0]	BP_A[0]	CKE0

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Table 4-17 DDR4-ALT DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

DFI Signal	RTL Bump Name	DDR4-ALT CH1 (DFI0)
dfi0_cke_P{0-3}[1]	BP_A[1]	CKE1
dfi0_cs_P{0-3}[0]	BP_A[36]	CS_N0
dfi0_cs_P{0-3}[1]	BP_A[40]	CS_N1
dfi0_dram_clk_disable[0]	BP_A[16]	CLK0_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLK0_C
dfi0_dram_clk_disable[1]	BP_A[20]	CLK1_T
dfi0_dram_clk_disable[1]	BP_A[21]	CLK1_C
dfi0_odt_P{0-3}[0]	BP_A[39]	ODT0
dfi0_odt_P{0-3}[1]	BP_A[45]	ODT1
dfi0_parity_in_P{0-3}[0]	BP_A[27]	PAR
dfi0_ras_n_P{0-3}[0]	BP_A[35]	RAS_N
dfi0_we_n_P{0-3}[0]	BP_A[34]	WE_N
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQ{(8*DBYTE)+7} - DQ{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBI{DBYTE}
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+10,(DBYTE*12)+9]	DQS_C[DBYTE],DQS_T[DBYTE]
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+11,(DBYTE*12)+8]	DQS_C[DBYTE+9],DQS_T[DBYTE+9]

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4.1.8.3 DDR4 DFI-to-SDRAM Pin Map: DWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1

Table 4-18 DFI Pin Mapping When DWC_DDRPHY_NUM_ANIBS = 12 DWC_DDRPHY_DFI1_EXISTS = 1 for DDR4 Mode

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_act_n_P{0-3}[0]	BP_A[6]	ACT_N
dfi0_address_P{0-3}[0]	BP_A[31]	A0
dfi0_address_P{0-3}[1]	BP_A[25]	A1
dfi0_address_P{0-3}[2]	BP_A[24]	A2
dfi0_address_P{0-3}[3]	BP_A[15]	A3
dfi0_address_P{0-3}[4]	BP_A[14]	A4
dfi0_address_P{0-3}[5]	BP_A[13]	A5
dfi0_address_P{0-3}[6]	BP_A[12]	A6
dfi0_address_P{0-3}[7]	BP_A[10]	A7
dfi0_address_P{0-3}[8]	BP_A[11]	A8
dfi0_address_P{0-3}[9]	BP_A[7]	A9
dfi0_address_P{0-3}[10]	BP_A[30]	A10
dfi0_address_P{0-3}[11]	BP_A[9]	A11
dfi0_address_P{0-3}[12]	BP_A[8]	A12
dfi0_address_P{0-3}[13]	BP_A[28]	A13
dfi0_address_P{0-3}[17]	BP_A[39]	A17
dfi0_alert_n_P{0-3}[0]	BP_ALERT_L	ALERT_N
dfi0_bank_P{0-3}[0]	BP_A[29]	BA0
dfi0_bank_P{0-3}[1]	BP_A[26]	BA1
dfi0_bg_P{0-3}[0]	BP_A[4]	BG0
dfi0_bg_P{0-3}[1]	BP_A[5]	BG1
dfi0_cas_n_P{0-3}[0]	BP_A[33]	CAS_N
dfi0_cid_P{0-3}[0]	BP_A[36]	C0
dfi0_cid_P{0-3}[1]	BP_A[37]	C1
dfi0_cid_P{0-3}[2]	BP_A[38]	C2

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Table 4-18 DFI Pin Mapping When DWC_DDRPHY_NUM_ANIBS = 12 DWC_DDRPHY_DFI1_EXISTS = 1 for DDR4 Mode (Continued)

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
dfi0_cke_P{0-3}[0]	BP_A[0]	CKE0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKE1
dfi0_cke_P{0-3}[2]	BP_A[2]	CKE2
dfi0_cke_P{0-3}[3]	BP_A[3]	CKE3
dfi0_cs_P{0-3}[0]	BP_A[40]	CS_N0
dfi0_cs_P{0-3}[1]	BP_A[41]	CS_N1
dfi0_cs_P{0-3}[2]	BP_A[42]	CS_N2
dfi0_cs_P{0-3}[3]	BP_A[43]	CS_N3
dfi0_dram_clk_disable[0]	BP_A[16]	CLK0_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLK0_C
dfi0_dram_clk_disable[1]	BP_A[20]	CLK1_T
dfi0_dram_clk_disable[1]	BP_A[21]	CLK1_C
dfi0_dram_clk_disable[2]	BP_A[18]	CLK2_T
dfi0_dram_clk_disable[2]	BP_A[19]	CLK2_C
dfi0_dram_clk_disable[3]	BP_A[22]	CLK3_T
dfi0_dram_clk_disable[3]	BP_A[23]	CLK3_C
dfi0_odt_P{0-3}[0]	BP_A[44]	ODT0
dfi0_odt_P{0-3}[1]	BP_A[45]	ODT1
dfi0_odt_P{0-3}[2]	BP_A[46]	ODT2
dfi0_odt_P{0-3}[3]	BP_A[47]	ODT3
dfi0_parity_in_P{0-3}[0]	BP_A[27]	PAR
dfi0_ras_n_P{0-3}[0]	BP_A[35]	RAS_N
dfi0_we_n_P{0-3}[0]	BP_A[34]	WE_N
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQ{(8*DBYTE)+7} - DQ{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBI{DBYTE}

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Table 4-18 DFI Pin Mapping When DWC_DDRPHY_NUM_ANIBS = 12 DWC_DDRPHY_DFI1_EXISTS = 1 for DDR4 Mode (Continued)

DFI Signal	RTL Bump Name	DDR4 CH1 (DFI0)
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+10, (DBYTE*12)+9]	DQS_C[DBYTE],DQS_T[DBYTE]
NULL - Strobe Mapping for Data Byte DBYTE	BP_D[(DBYTE*12)+11, (DBYTE*12)+8]	DQS_C[DBYTE+9],DQS_T[DBYTE+9]

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4.1.8.4 LPDDR4 DFI-to-SDRAM Pin Map: DDWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1

Note

- DBYTES assigned to CH1 (DFI0) are DBYTES{floor(NUM_DBYTES/2) -1 … 0 }
- DBYTES assigned to CH2 (DFI1) are DBYTES{ (NUM_DBYTES-x) … (floor(NUM_DBYTES/2)) }
  - Where x = 1 for an even NUM_DBYTES, and x=2 for odd NUM_DBYTES
- For odd NUM_DBYTES, the most-significant DBYTE is unassigned

Table 4-19 LPDDR4 DFI-to-SDRAM Pin Map: DDWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1

DFI Signal	RTL Bump Name	LPDDR4CHx (DFIx)
DFI_signal	**RTL Bump Name**	**LPDDR4 CH1 (DFI0)**
dfi0_address_P{0-3}[0]	BP_A[13]	CAA0
dfi0_address_P{0-3}[1]	BP_A[7]	CAA1
dfi0_address_P{0-3}[2]	BP_A[12]	CAA2
dfi0_address_P{0-3}[3]	BP_A[11]	CAA3
dfi0_address_P{0-3}[4]	BP_A[10]	CAA4
dfi0_address_P{0-3}[5]	BP_A[4]	CAA5
dfi0_cke_P{0-3}[0]	BP_A[0]	CKEA0
dfi0_cke_P{0-3}[1]	BP_A[1]	CKEA1
dfi0_cs_P{0-3}[0]	BP_A[36]	CSA0
dfi0_cs_P{0-3}[1]	BP_A[37]	CSA1
dfi0_dram_clk_disable[0]	BP_A[16]	CLKA_T
dfi0_dram_clk_disable[0]	BP_A[17]	CLKA_C
dfi_reset_n	BP_MEMRESET_L	RESET_N
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQA{(8*DBYTE)+7} - DQA{(8*DBYTE)}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIA{DBYTE}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSA_T[DBYTE]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSA_C[DBYTE]
DFI_Signal	**RTL Bump Name**	**LPDDR4 CH2 (DFI1)**

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Table 4-19 LPDDR4 DFI-to-SDRAM Pin Map: DDWC_DDRPHY_NUM_ANIBS = 12 and DWC_DDRPHY_DFI1_EXISTS = 1 (Continued)

DFI Signal	RTL Bump Name	LPDDR4CHx (DFIx)
dfi1_address_P{0-3}[0]	BP_A[28]	CAB0
dfi1_address_P{0-3}[1]	BP_A[33]	CAB1
dfi1_address_P{0-3}[2]	BP_A[34]	CAB2
dfi1_address_P{0-3}[3]	BP_A[35]	CAB3
dfi1_address_P{0-3}[4]	BP_A[29]	CAB4
dfi1_address_P{0-3}[5]	BP_A[24]	CAB5
dfi1_cke_P{0-3}[0]	BP_A[46]	CKEB0
dfi1_cke_P{0-3}[1]	BP_A[47]	CKEB1
dfi1_cs_P{0-3}[0]	BP_A[41]	CSB0
dfi1_cs_P{0-3}[1]	BP_A[40]	CSB1
dfi1_dram_clk_disable[0]	BP_A[20]	CLKB_T
dfi1_dram_clk_disable[0]	BP_A[21]	CLKB_C
dfi_wrdata_P{0-3}/dfi_rddata_W{0-3}[(8*DBYTE)+7+(8*NUM_DBYTES):(8*DBYTE)+(8*NUM_DBYTES),(8*DBYTE)+7:(8*DBYTE)]	BP_D[(DBYTE*12)+7:(DBYTE*12)]	DQB{(8*(DBYTE-4)+7} - DQB{(8*(DBYTE-4))}
dfi_wrdata_mask_P{0-3}/dfi_rddata_dbi_W{0-3}[DBYTE+NUM_DBYTES,DBYTE]	BP_D[(DBYTE*12)+8]	DM/DBIB{(DBYTE-4)}
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+9]	DQSB_T[(DBYTE-4)]
NULL - Strobe Mapping for Data Bytes	BP_D[(DBYTE*12)+10]	DQSB_C[(DBYTE-4)]

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4.2 DFI Interface Implementation Details

Different segments of the DFI Control Interface are used depending on the target DRAM protocol. The following list indicates the parts used per protocol (and the maximum bus width allowed by the PHY in the mode):

- DDR4: dfi_address (18), dfi_bank (2), dfi_bg (2), dfi_cid (3), dfi_odt (2)** , dfi_cke (2)**, dfi_cs (2)
  - The 12ACX configuration enables up to 4 ODT/CKE/CS pins in DDR4 mode
- LPDDR4: dfi_address (6), dfi_bank (0), dfi_bg (0), dfi_cid (0), dfi_odt (0) , dfi_cke (2) , dfi_cs (2)

Note For any given PHY configuration, unused pins should be set to the inactive state (as described in the DFI protocol).

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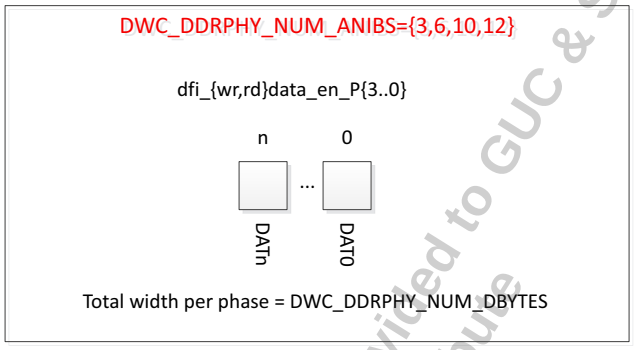
4.3 Phase Bits and Chip Selects

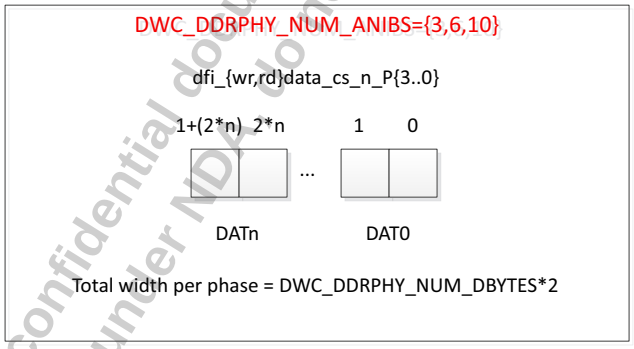
There are four phase bits for each DBYTE read and write enable, with the DFI read and write enable registers organized as shown in Figure 4-1.

Figure 4-1 wr_data_en and rd_data_en Registers: DWC_DDRPHY_NUM_ANIBS = {3,6,10,12}



There are two chip select bits for each DBYTE Phase when DWC_DDRPHY_NUM_ANIBS = {3,6,10}, the wr_data_cs_n and rd_data_cs_n bits are organized as shown in Figure 4-3.

Figure 4-2 wr_data_cs_n and rd_data_cs_n Registers: DWC_DDRPHY_NUM_ANIBS = {3,6,10}



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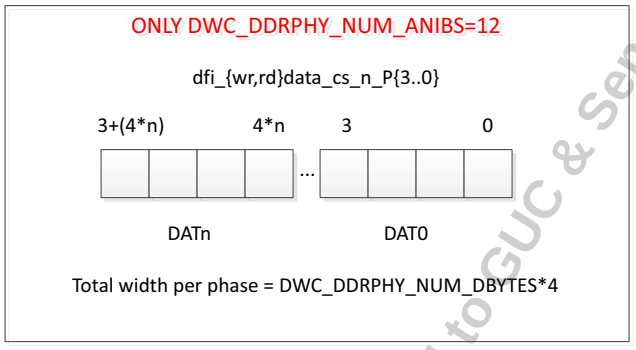
There are four chip select bits for each DBYTE Phase when DWC_DDRPHY_NUM_ANIBS = 12, the wr_data_cs_n and rd_data_cs_n bits are organized as shown in Figure 4-3.

Figure 4-3 wr_data_cs_n and rd_data_cs_n Registers: DWC_DDRPHY_NUM_ANIBS=12



4.4 Command Phase Timing

Since there are two commands per DFI clock cycle, the nomenclature [CMD1:CMD0] denotes the first (even) command and the second (odd) command; for instance, CMD0 is driven out on the first CK cycle and CMD1 is driven on the second CK cycle.

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5
Parameter Description

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This chapter describes the following:

- "PUB Parameters" on page 112

5.1 PUB Parameters

The following tables show the programmable parameters for the PUB that enable functionality.

For clarity, the parameter names for parameterized signals are shown abbreviated in the table and are fully described, including the full parameter name, in the notes section at the end of the table.

5.1.1 DFI Control Timing Parameters

Table 5-1 DFI Control Timing Parameters

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
t_{ctrl_delay}	MEMCLKS	(ARdPtrinitVal[3:0]/2) + (MISC*2)[1]+4	(ARdPtrinitVal[3:0]/2) + (MISC*2)[1] + 3[2]	(ARdPtrinitVal[3:0]/2) + (MISC*2)[1] + 1[2]	Specifies the number of MEMCLKs after a change in the Phase 0 DFI control signals (as sampled by DfiCtlClk in the PHY) that the change is reflected on the PHY-DRAM interface

1. MISC = Setting of DWD_DDRPHY_PIPE_DFI_MISC
2. For changes to _P{1-3} DFI control signals, add 1-3 additional MEMCLK correspondingly.

5.1.2 DFI Programmable Write Parameters and Write Timing Parameters

5.1.2.1 DFI Write Parameters

Table 5-2 DFI Write Data Programmable Parameters

Parameter	Description
phy_{dbi_mode}	Determines which device generates DBI and inverts the data. ‘b0 = DBI generation and data inversion performed in the MC. ‘b1 – Not supported

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5.1.2.2 DFI Write Timing Parameters

Table 5-3 DFI Write Data Timing Parameters

Parameter	Units	Value	Description
$t_{phy\_wrcsgap}$	MEMCLKs	4	This parameter specifies the minimum number of additional MEMCLKs that are required between commands when changing the target chip select that is driven on the dfi_wrdata_cs_n signal.
$t_{phy\_wrcslat}$	MEMCLKs	WL[1]-5 + 2*(MISC[2] – WR[3])	This parameter specifies the number of MEMCLKs from the time that a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs_n signal is asserted.
t_{phy_wrdata}	MEMCLKs	2	This parameter specifies the number of MEMCLKs from the time that the dfi_wrdata_en signal is asserted and when the associated write data is driven on the dfi_wrdata signal. The parameter adjusts the relative time between enable and data transfer with no effect on performance.
t_{phy_wrlat}	MEMCLKs	WL[1]-5 + 2*(MISC[2] – WR[3])	This parameter specifies the number of MEMCLKs from the time that a write command is sent on the DFI control interface and when the dfi_wrdata_en signal is asserted.
tphy_wrdata_delay	MEMCLKs	t_{ctrl_delay} + (6 + BL/2) + Trained_TxDqsDly	This parameter specifies the time from dfi_wrdata_en is asserted to when the write data transfer completes on the DRAM bus.

1.WL = DRAM_WL + AL + PL + (RCD_nladd)* + (tDQSSnom**). Note: **tDQSSnom = 1tck for LPDDR4,-
DRAM_WL: DRAM CAS write latency
- AL: DRAM Additive latency (where applicable)
- PL: DRAM Parity latency (where applicable)
- RCD_nladd: Register Command Latency Adder - F0RC0F (where applicable)

2. MISC: Setting of DWC_DDRPHY_PIPE_DFI_MISC
3. WR: Setting of DWC_DDRPHY_PIPE_DFI_WR

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5.1.3 DFI Read Parameters and Read Timing Parameters

5.1.3.1 DFI Read Parameters

Table 5-4 DFI Read Data Programmable Parameters

Parameter	Description
phy_{dbi_mode}	Determines which device generates DBI and inverts the data. ‘b0 = DBI generation and data inversion performed in the MC. ‘b1 – Not supported

5.1.3.2 DFI Read Timing Parameters

Table 5-5 DFI Read Data Timing Parameters

Parameter	Units	Value	Description
$t_{phy\_rdcsgap}$	MEMCLKs	2	Specifies the minimum number of additional MEMCLKs required between commands when changing the target chip select driven on the dfi_rddata_cs_n signal. This parameter needs to be supported in the MC transaction-to-transaction timing.
$t_{phy\_rdcslat}$	MEMCLKs	RL[1]-5 + 2*(MISC[2] – RD[3])	Specifies the number of MEMCLKs between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs_n signal is asserted.
t_{phy_rdlat}	MEMCLKs	Trained Value + (4*RD)	Specifies the maximum number of MEMCLKs allowed from the assertion of the dfi_rddata_en signal to the assertion of each of the corresponding bits of the dfi_rddata_valid signal.
t_{rddata_en}	MEMCLKs	RL[1]-5 + 2*(MISC[2] – RD[3])	Specifies the number of MEMCLKs from the assertion of a read command on the DFI to the assertion of the dfi_rddata_en signal.

1. RL = DRAM_RL + AL + PL + (RCD_nladd)"
   - DRAM_RL: DRAM CAS read latency
   - AL: DRAM Additive latency (where applicable)
   - PL: DRAM Parity latency (where applicable)
   - RCD_nladd: Register Command Latency Adder - F0RC0F (where applicable)
   - N: PHY Trained Max Read Latency
2. MISC: Setting of DWC_DDRPHY_PIPE_DFI_MISC
3. RD: Setting of DWC_DDRPHY_PIPE_DFI_RD

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5.1.4 DFI Update Timing Parameters

Table 5-6 DFI Update Timing Parameters

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
t_{phyupd_type0}	DfiCtlClk	(4*MISC[1]) + 48+2	(2*MISC[1]) + 24	MISC[1] + 12 + 1.5	Specifies the maximum number of DfiCtlClk cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x0. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.
t_{phyupd_type1}	DfiCtlClk	(4*MISC[1]) + 96+2	(2*MISC[1]) + 48	MISC[1] + 24 + 1.5	Specifies the maximum number of DfiCtlClk cycles that the dfi_phyupd_req signal may remain asserted after the assertion of the dfi_phyupd_ack signal for dfi_phyupd_type = 0x1. The dfi_phyupd_req signal may de-assert at any cycle after the assertion of the dfi_phyupd_ack signal.

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Table 5-6 DFI Update Timing Parameters

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
t_{phyupd_resp} (max)	DfiCtlClk	1020 - (4*MISC[1])	510 - (2*MISC[1])	255 – MISC[1]	Specifies the maximum number of DfiCtlClk cycles after the assertion of the dfi_phyupd_req signal to the assertion of the dfi_phyupd_ack signal.
$t_{ctrlupd\_min}$	DfiCtlClk	48	24	12	Specifies the minimum time for dfi_ctrlupd_req assertion
$t_{ctrlupd\_max}$	DfiCtlClk	98	48	25.5	Specifies the maximum time for dfi_ctrlupd_req assertion

1. MISC is the setting of DWC_DDRPHY_PIPE_DFI_MISC

Note A minimum of 24 dficlk (48 memclk) cycles are required between the de-asserting (1->0) edge of dfi_ctrlupd_req and the next asserting (0->1) edge of dfi_ctrlupd_req. For t_{phyupd_resp}, if the controller requires a larger response time, see register DFIPHYUPD for additional configuration options.

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5.1.5 DFI Geardown Mode Timing Parameter

Table 5-7 DFI Geardown Mode Timing Parameter

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
$t_{geardown\_delay}$	DfiCtlClk	16	8	4	The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands.

5.1.6 DFI Low Power Control Timing Parameters

Note Large values of MISC (see Table 5-8) can cause Tlp_resp to exceed the notional maximum from the DFI Specification. Ensure the memory controller is compatible with Tlp_resp values greater than 7 in these cases.

Table 5-8 DFI Low Power Control Timing Parameters

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
t_{lp_resp}	DfiCtlClk	(4*MISC[1]) + 4	(2*MISC[1]) + 1	MISC[1] + 1	Specifies the maximum number of DfiCtlClk cycles after the assertion of the dfi_lp_ctrl_req or dfi_lp_data_req signal to the assertion of the dfi_lp_ack signal
t_{lp_wakeup}	DfiCtlClk	(4*MISC[1]) + 5	(2*MISC[1]) + 2	MISC[1] + 2.5	Specifies the maximum number of DfiCtlClk cycles that the dfi_lp_ack signal may remain asserted after the de-assertion of the dfi_lp_ctrl_req or dfi_lp_data_req signal. The dfi_lp_ack signal may de-assert at any cycle after the de-assertion of the dfi_lp_ctrl_req or dfi_lp_data_req signal. Exceeding the maximum is not considered an error condition.

1. MISC is the setting of DWC_DDRPHY_PIPE_DFI_MISC

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5.1.7 DFI Error Timing Parameters

Table 5-9 DFI Error Timing Parameters

Parameter	Units	Value	Description
t_{error_resp}	DfiCtlClk	N/A	Specifies the maximum number of DfiCtlClk cycles that may occur from the DFI bus transaction(s) which are known to be affected by the error condition and the assertion of the dfi_error signal.

5.1.8 DFI PHY MASTER Timing Parameters

Table 5-10 DFI PHY MASTER Timing Parameters

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
$t_{phymstr\_resp}$ (max)	DfiCtlClk	8188 - (4*MISC[1])	4090 - (2*MISC[1])	2047 - MISC[1]	For the recommended setting of csrPhyMstrMaxReqToAck (0x5), specifies the maximum number of DfiCtlClk cycles after the dfiphymstr_req signal asserts to the assertion of the dfi_phymstr_ack signal.
$t_{phymstr\_type0}$ (max)	DfiCtlClk	2562	1280	642	Specifies the maximum number of DfiCtlClk cycles that the dfi_phymstr_req signal may remain asserted after the assertion of the dfi_phymstr_ack signal for dfi_phymstr_type = 0x0. The dfi_phymstr_req signal may de-assert at any cycle after the assertion of the dfi_phymstr_ack signal.
$t_{phymstr\_type\{1-3\}}$	-	-	-	-	Not supported

1. MISC is the setting of DWC_DDRPHY_PIPE_DFI_MISC

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5.1.9 DFI Frequency Change Parameters

Table 5-11 DFI Frequency Change Parameters

Parameter	Units	1:1 Mode	1:2 Mode	1:4 Mode	Description
t_{init_start} (max)	DfiCtlClk	514	256	130	Specifies maximum time from assertion of dfi_init_start to deassertion of dfi_init_complete for a frequency change operation.
$t_{init\_complete}$ (max)	DfiCtlClk	3µs + 2560	3µs + 1280	3µs + 640	Specifies maximum time from de-assertion dfi_init_start to assertion of dfi_init_complete for a frequency change operation.

5.1.10 DFI DRAM Clock Disable Parameters

Table 5-12 DFI DRAM Clock Disable Parameters

Parameter	Units	Value			Description
		1:1 Mode	1:2 Mode	1:4 Mode	
$t_{dram\_clk\_disable}$	MEMCLKs	$t_{ctrl\_delay-(1+ODD}$[1])	t_{ctrl_delay}-2	t_{ctrl_delay} - 2	Specifies the time from assertion of dfi_dram_clk_disable until clock is low at DRAM. This specification does not include board and internal DRAM delays.
$T_{dram\_clk\_enable}$	MEMCLKs	$t_{ctrl\_delay-(1+ODD}$[1])	t_{ctrl_delay}-2	t_{ctrl_delay}- 2	Specifies the time from deassertion of dfi_dram_clk_disable until first rising edge of clock at DRAMs. This specification does not include board and internal DRAM delays.

1. ODD = 1 if the signal enters the PHY on an odd phase of DFICLK (DFICLK=0).

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5.1.11 DFI Miscellaneous Parameters

Table 5-13 DFI Miscellaneous Parameters

Parameter	Units	Value	Description
$t_{alert\_latency}$	DfiClk	10ns + BYP[1] + DDR3[2]	Specifies the maximum time from BP_ALERT_N asserted to dfi_alert_n asserted. Fractional values should be rounded up

1. BYP=6 DFICLKs when csrMALERTSyncBypass=0. BYP=0 when csrMALERTSyncBypass=1
2. DDR3 = 2 DFICLKs if csrTestMajorMode=000. Otherwise DDR3=0

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6

Programming Model: Clocks, Resets, Initialization, and Power Management

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This chapter describes the following:

- "Clocks" on page 122
- "Resets" on page 129
- "PHY Initialization" on page 132
- "Power Management" on page 136
- "PHY Initialization Engine Description" on page 155

6.1 Clocks

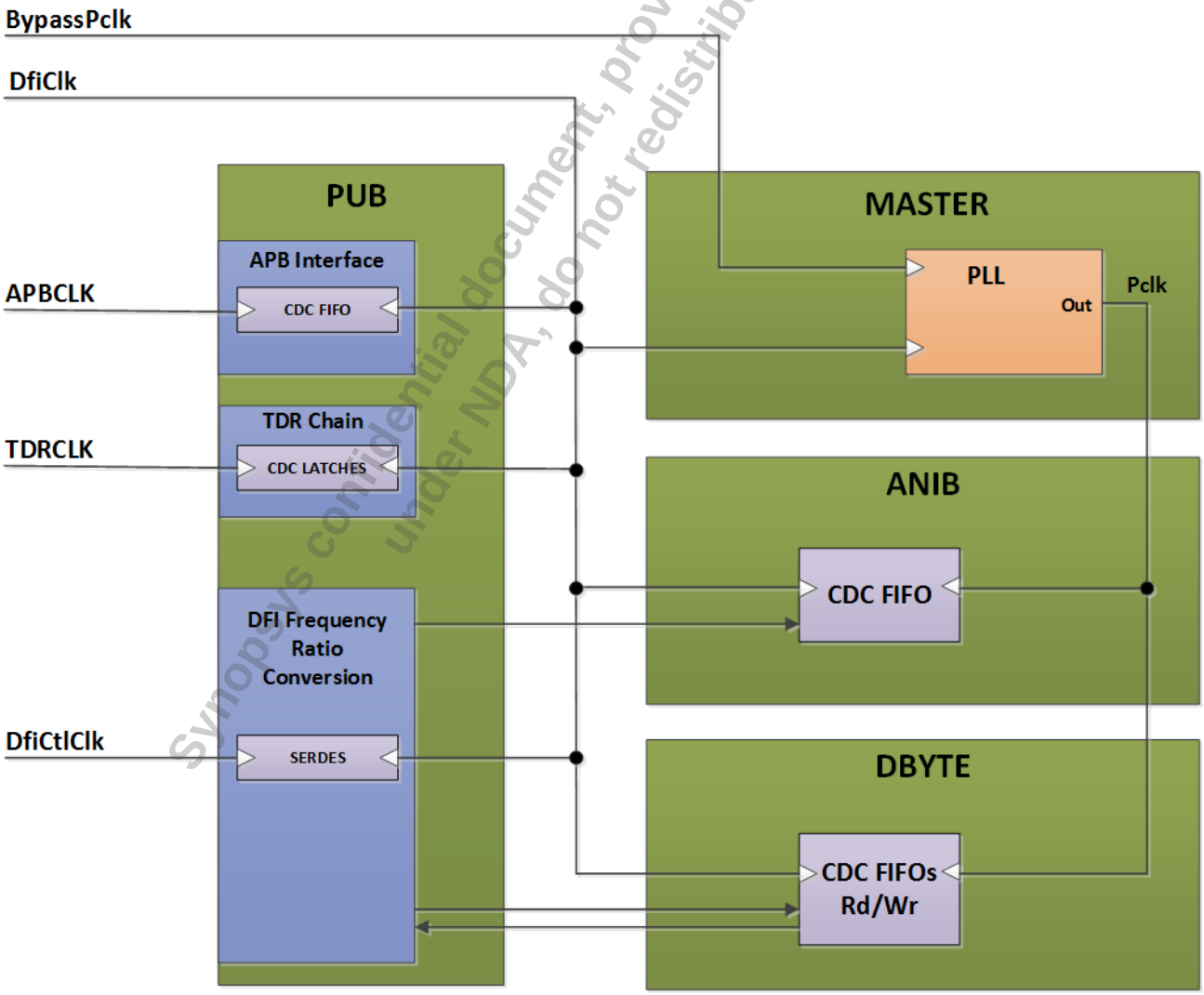
6.1.1 PHY Clocks

The PHY operational clocks include:

- APB Clock (APBCLK)
- DFI Clock (DfiClk)
- DFI Controller Clock (DfiCtlClk)
- Phy High speed Clock (Pclk)
- Phy High speed Bypass Clock (BypassPclk)

Below is a high level diagram of the PHY clock distribution.

Figure 6-1 PHY Clock Distribution Block Diagram



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6.1.1.1 DfiClk

The DfiClk is generated externally and is used by the PHY as a primary mission mode clock input for the PUB logic. The DfiClk is supplied to the PHY must be set to half of the desired memory (MEMCLK) frequency, which is equivalent to one quarter the data rate. The DfiClk is expected as a single-ended, full-CMOS level input on VDD. DFICLK is used as a reference clock input to the PLL in the MASTER PHY.

- The minimum operational DfiCLK frequency = 12.5MHz (this corresponds to DDR50)
- The maximum operational DfiCLK frequency = DATA_RATE/4 (refer to the *DWC PHY Databook* for the maximum supported DATA_RATE)

6.1.1.2 DfiCtlClk

The DfiCtlClk is generated externally and is used by the PUB to support 1:1, 1:2 and 1:4 MC to PHY (MEMCLK) frequency ratios at the DFI interface. The required DfiCtlClk frequency will depend on the desired DFI Frequency Ratio, as set in the csrDfiFreqRatio register. The following table shows the frequency relationships of the operating clocks.

The PUB hardware performing the frequency ratio conversion requires that DfiCtlClk and DfiClk are synchronous (the phase relationship between the clocks must be invariant, and the edges must coincide).

Table 6-1 illustrates the variable ratio between DfiCtlClk and DfiClk. This is implemented as a synchronous data packing/unpacking interface at the DFI interface to the PHY. Each of the three options for DFI_FREQ_RATIO operates differently, as discussed below.

Table 6-1 Frequency Relationships of the Operating Clocks

DFI_FREQ_RATIO	csrDfiFreqRatio	DfiCtlClk	DfiClk	Pclk	BypassPclk
1:1	00	DATA_RATE/2	DATA_RATE/4	DATA_RATE	DATA_RATE
1:2	01	DATA_RATE/4	DATA_RATE/4	DATA_RATE	DATA_RATE
1:4	1x	DATA_RATE/8	DATA_RATE/4	DATA_RATE	DATA_RATE

Note csrDfiFreqRatio should be changed only when the DFI bus is idle. The DFI bus should be idle for at least four DfiClk cycles before, and after, a write to the csrDfiFreqRatio register.

6.1.1.2.1 DFI_FREQ_RATIO = 1:4

In this mode, the DfiCtlClk is set to 1/2 the DfiClk frequency. Thus, to provide data at the PHY rate, twice as many data elements much be provided every DfiCtlClk cycle as in the 1:2 case. The dfi_*_P0, dfi_*_P1, dfi_*_P2, and dfi_*_P3 signals are all used to provide the input information for four consecutive MEMCLK cycles. Figure 6-2 shows how the four DFI input phase signals are mapped internally to two phases.

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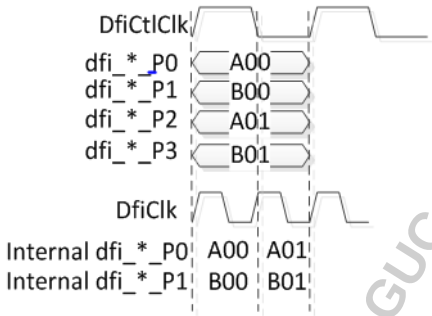
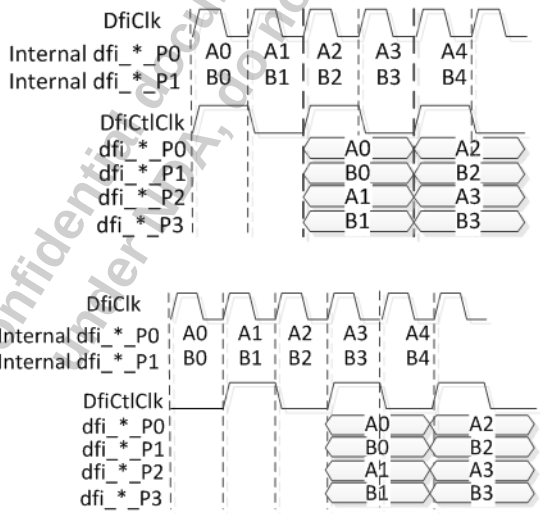
Figure 6-2 DFI Interface to PHY Internal Logic, 1:4 Ratio, phased signals



Note that the above discussion applies to phased signals, that is, DFI signals that end in _P0 or _W0. For non-phased inputs in 1:4 mode, the interface is a wire, see 1:2 mode for details.

In the output direction, the output information from two consecutive MEMCLK cycles is provided externally using all four dfi_*_P0/W0 - dfi_*_P3/W3 output signals. Figure 2 below illustrates the two possible timings.

Figure 6-3 PHY Internal Logic to DFI Interface, 1:4 Ratio, phased signals



Non-phased DFI output signals are delayed one DfiCtlClk cycle, as shown in Figure 6-4.

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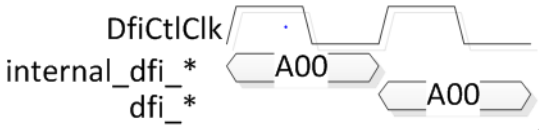
Figure 6-4 PHY Internal Logic to DFI Interface, 1:4 Ratio, non-phased signals



6.1.1.2.2 DFI_FREQ_RATIO = 1:2

For the 1:2 ratio, DfiCtlClk = DfiClk, and the interface is a wire. The dfi_*_P<n> and dfi_*_P1 signals are used to provide the input information for two consecutive MEMCLK cycles, and the output from two consecutive MEMCLK cycles is provided on dfi_*_P0/W0, and dfi_*_P1/W1 output signals, as shown in Figure 6-5 and Figure 6-6.

Figure 6-5 DFI Interface to PHY Internal Logic, 1:2 Ratio

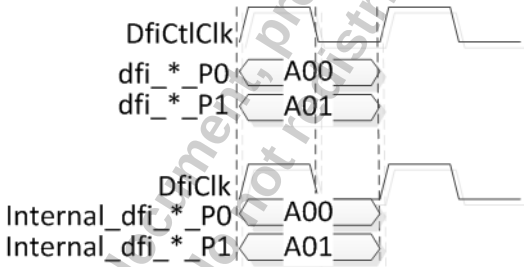
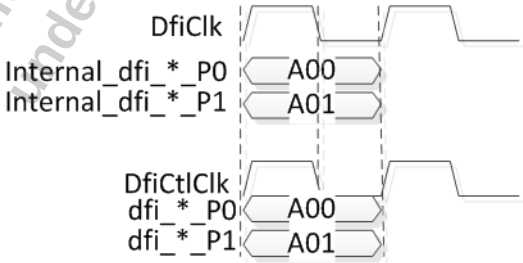


Figure 6-6 PHY Internal Logic to DFI Interface, 1:2 Ratio



Non-phased signals are handled in the same fashion.

6.1.1.2.3 DFI_FREQ_RATIO = 1:1

In this mode, the DfiCtlClk is set to twice the DfiClk frequency. Thus, to provide data at the PHY rate, only one input phase (dfi_*_P0) is used to provide the input for two consecutive MEMCLK cycles. Figure 6-7 below shows how the DFI input signal is mapped internally to two phases.

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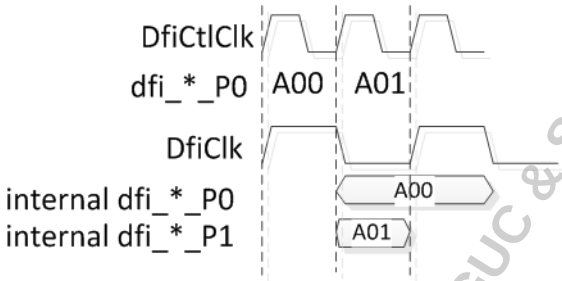
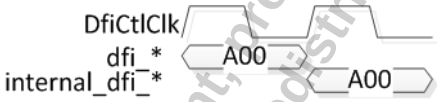
Figure 6-7 DFI Interface to PHY Internal Logic, 1:1 Ratio, phased signals



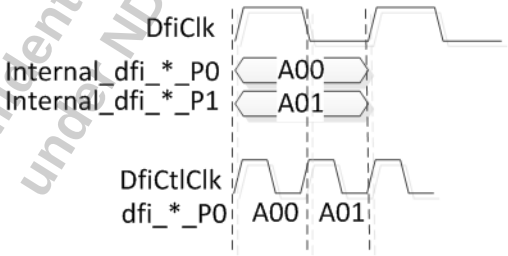
Non-phased DFI input signals, except dfi_reset, are delayed one DfiCtlClk cycle, as shown in Figure 6-8.

Figure 6-8 PHY Internal Logic to DFI Interface, 1:1 Ratio, non-phased signals



In the output direction, the output information from two consecutive MEMCLK cycles is provided on a single output phase. Figure 6-9 illustrates the timing.

Figure 6-9 PHY Internal Logic to DFI Interface, 1:1 Ratio, phased signals



For non-phased outputs in 1:1 mode, the interface is a wire, see 1:2 mode for details.

6.1.1.3 PClk

The PHY high speed clock (PClk) is generated internally by the MASTER PHY PLL. The PHY PLL multiplies the reference input (DfiClk) by 4 to generate the full-rate data-rate clock used by the high speed logic.

The Pclk is used only inside the PHY Hard Macros (MASTER, ACX, DBYTE). As well, all clock domain crossings between Pclk and the DfiClk are performed solely within the PHY Hard Macros.

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6.1.1.4 BypassPclk

The BypassPclk clock is generated externally and is used when PHY is in PLL-bypass mode. The BypassPclk is required when the PHY is operating at datarates below 667 MT/s. When enabled, BypassPclk shall toggle at four times the frequency of DfiClk which is equivalent to the data rate. The BypassPclk is expected as a single-ended, full-CMOS level input on VDD. The BypassPclk is used as the bit-rate clock inside the PHY.

- BypassPclk requirements:
  - Min = 4 * DFI_CLK (min) = 4 * 12.5 MHz = 50 MHz
  - Max = 1067 MHz

When the PLL-bypass feature is not needed, BypassPclk can be tied low or gated.

6.1.1.5 APBCLK

The APB Clock is generated externally and is synchronous to the APB configuration bus. All signals on the APB interface are synchronous to the APBCLK. Internally to the PUB, APB transactions are synchronized into the DfiClk domain to allow APBCLK to operate at a different frequency than DfiClk.

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6.1.2 DFx Clocks

- Test Data Register Clock (TDRCLK)
- ATPG Scan Clocks (atpg*clk)

6.1.2.1 TDRCLK

The Test Data Register clock (TDRCLK) is an externally generated DFT clock for the PHY TDR chain. In test modes, the TDR chains can be used to read and write PHY registers..

Note The frequency(DfiClk) >= frequency(TDRCLK) in order to access registers with TDR interface

6.1.2.2 atpg*clk

The ATPG clock is for test modes only. Independent atpg_clk ports are provided for each internally generated functional clock domain in the PHY.

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6.2 Resets

The PHY supports cold and warm resets. The PHY receives the following control signals for various reset states:

- PwrOkIn
- Reset

The PHY also supports the reset of the APB interface though the following:

- PRESETn_APB

The following reset rules must be followed:

- Reset must have a minimum pulse width of 64 DfiClks
- Reset is synchronous to DfiClk
- PRESETn_APB is synchronous to APBCLK
- PRESETn_APB must have a minimum pulse width of 16 APBCLKs
- The asserting edge(1->0) transition of PRESETn_APB must occur at least 16 APBCLKs before the deasserting edge of Reset
- The deasserting edge of PRESETn_APB may occur after the deasserting edge of Reset
- PHY TDR Interface must be reset 1us prior to "Reset" deassertion.
- WRSTN is synchronous to TDRCLK. As per JTAG specs, WRSTN may be asynchronously asserted, but must be synchronously deasserted
- APB transactions are allowed only after the PHY and the APB interface have exited reset - Reset and PRESETn_APB have both been deasserted
- PwrOkIn is asynchronous
- During Cold Reset, the reset signal must be asserted at least 8 DfiClks prior to the assertion of PwrOkIn
- During Cold Reset, the reset signal must remain asserted for at least 64 DfiClks after the assertion of PwrOkIn
- After the deassertion of PwrOkIn, the DfiClk must cycle for at least 16 DfiClks

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6.2.1 WarmReset

Warm reset occurs when the Reset signal becomes asserted while the PwrOkIn signal is already asserted. On a warm reset, the PHY output is not deterministic.

Note

- WarmReset, started by asserting the Reset input pin while the PwrOKIn pin is asserted, resets all the digital logic in the PHY (including the registers)
- ColdReset is the same as WarmReset with the exception that all the I/O bumps are also immediately forced to their inactive state

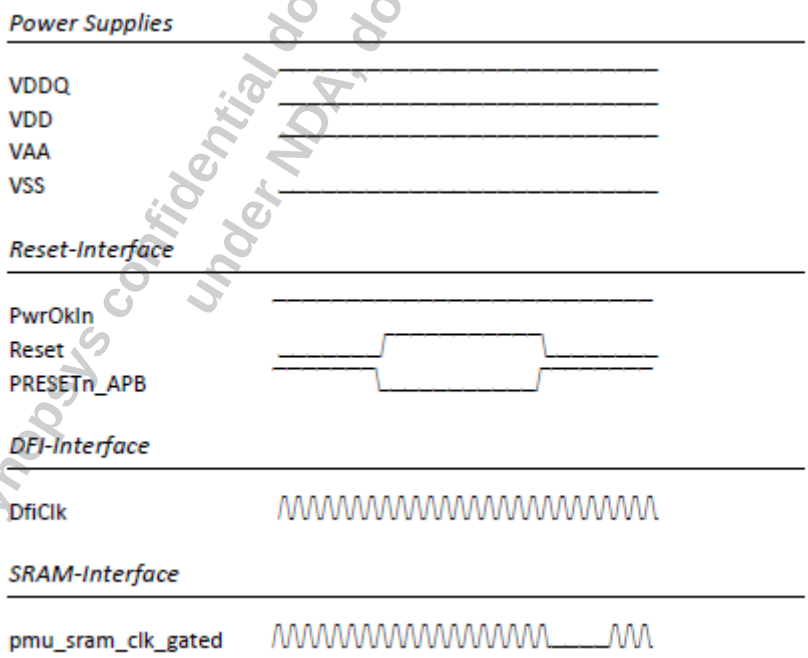
On reset assertion, the PHY stops, asserts internal inits and stops its internal clocks. If the PHY was sequenced to LP3 and PwrOkIn==0, which enables Retention, the PHY will ensure that the CKE and MEMRESET signals are protected from the warm reset signal going x (unknown) or asserting.

Otherwise when the PHY and DRAM are in warm reset, the bus states are not guaranteed. While Reset is asserted, the APB and DFI interfaces are off line.

Warm reset also resets the uCtrl and the SRAM content is not guaranteed. After Reset de-asserts, the PHY must be fully reinitialized before it can be placed in mission mode. After the de-assertion of Reset, the PHY must receive at least 64 DFICLK pulses prior to any APB transaction or the assertion of dfi_init_start.

The following diagram shows Warm Reset operation.

Figure 6-10 WarmReset Operation



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6.2.2 ColdReset

A cold reset occurs when, at power-up, the PwrOkIn signal is low and Reset signal is high.

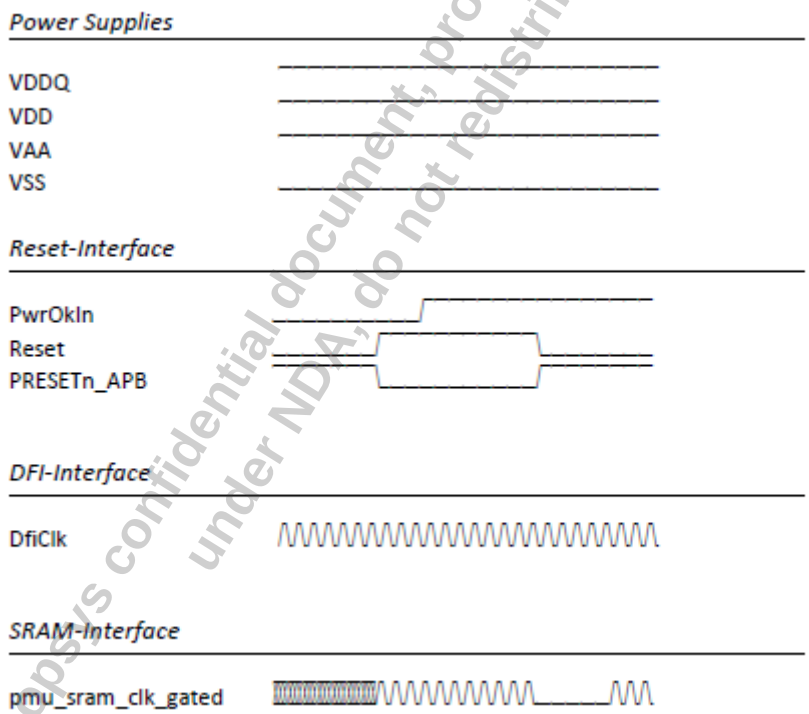
Note ColdReset resets all the digital logic in the PHY, including the registers, and immediately forces all the I/O bumps to their inactive state.

Once the PwrOkIn is asserted (and Reset is still asserted), DfiClk synchronously switches to any legal input frequency.

After power-up, subsequent cold resets can be signaled to the PHY by de-asserting PwrOkIn and asserting Reset, with or without removing power.

The following diagram shows ColdReset operation.

Figure 6-11 ColdReset Operation



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6.3 PHY Initialization

As part of the release directory structure, there is C code that shows exactly what steps need to be executed during PHy initialization. The code is in the phyinit directory in the following location: Product Deliverables in <PHY Install Directory>/synopsys/<technology>_<process>/Latest/phyinit/Latest.

By default, the provided code prints all the register access (complete with register address and data) for all the accesses necessary as part of the initialization process. The user can modify the code to actually call a routine to do the accesses instead.

Note The README document in the phyinit directory details how to compile and use the code provided.

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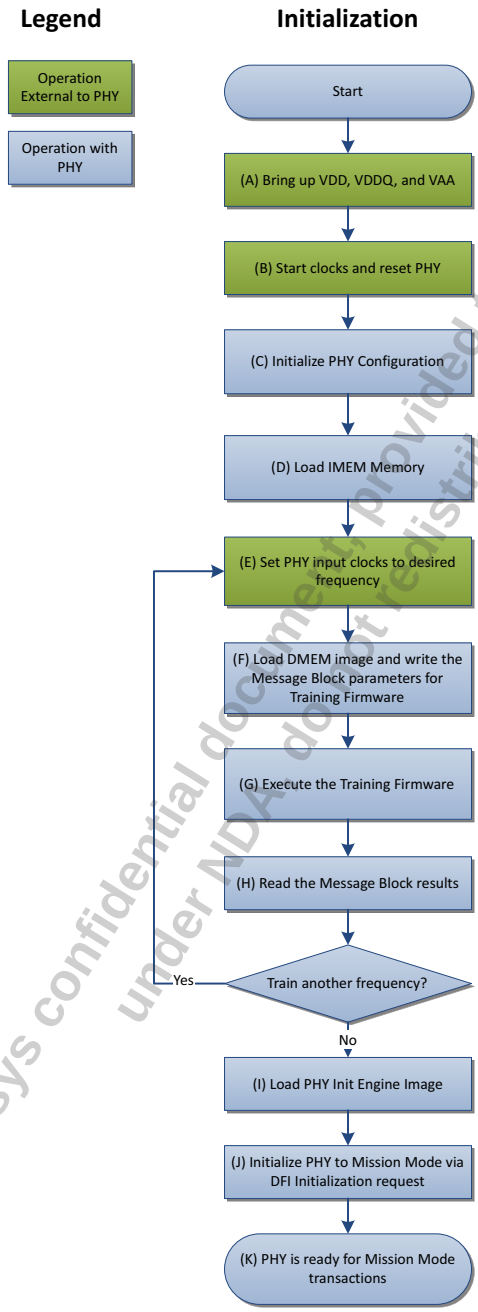
6.3.1 PHY Initialization Sequence

The initialization process is shown in Figure 6-12 on page 133

Figure 6-12 Initialization Sequence



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The sequence is described in detail in the following sections.

6.3.1.1 (A) Bring up VDD, VDDQ, VDDQLP, and VAA

The first step for initializing the PHY is to apply power. The power supplies can come up and stabilize in any order. While the power supplies are coming up, all outputs will be unknown and the values of the inputs are don't cares. Once the power supplies are stable, there are rules on how the power supplies behave. See "Power Management" on page 136 for more information on the power supplies.

For more information, refer to the dwc_ddrphy_phyinit_A_bringupPower() program in the provided code in the phyinit directory.

6.3.1.2 (B) Start Clocks and Reset the PHY

The second step is to start the PHY clocks and apply the synchronous reset.

For more information, refer to the dwc_ddrphy_phyinit_B_startClockResetPhy() program in the provided code in the phyinit directory.

6.3.1.3 (C) Initialize PHY Configuration

The PHY supports multiple memory standards and configurations. There are configuration registers in the PHY that must be set to configure it for the correct memory type and configuration. The routine for this step details the list of configuration registers to set and how to calculate the correct values based on the system.

For more information, refer to the dwc_ddrphy_phyinit_C_initPhyConfig() program in the provided code in the phyinit directory.

6.3.1.4 (D) Load the IMEM Memory

Before the PHY training firmware can be run, the firmware program image must be loaded into the instruction memory SRAM.

For more information, refer to the dwc_ddrphy_phyinit_D_loadIMEM() program in the provided code in the phyinit directory.

6.3.1.5 (E) Set the PHY input clocks to the desired frequency

Set the PHY input clocks to the desired operating frequency. Before proceeding to the next step, the clock should be stable at the new frequency. For more information on clocking requirements, see "Clocks" on page 122.

For more information, refer to the dwc_ddrphy_phyinit_E_setDfiClk() program in the provided code in the phyinit directory.

6.3.1.6 (F) Write the Message Block parameters for the training firmware

In order for the firmware to run, it must be given some information about the system, the memory configuration, and the memory training steps that it is to run. There are several locations in the data memory that must be written for the training firmware to have these parameters.

For more information, refer to the dwc_ddrphy_phyinit_F_loadDMEM() program in the provided example code for more details.

6.3.1.7 (G) Execute the Training Firmware

The training firmware can now be run. There is a protocol for starting the firmware, and interacting with it to determine the training status.

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For more information, refer to the dwc_ddrphy_phyinit_G_execFW() program in the provided code in the phyinit directory.

6.3.2 (H) Read the Message Block results

Once the training firmware has completed, it returns the results of the training in the data memory in the message block structure. The message block can be read to obtain these results.

For more information, refer to the dwc_ddrphy_phyinit_H_readMsgBlock() program in the provided code in the phyinit directory.

6.3.2.1 (I) Load PHY Init Engine Image

Load the PHY Initialization Engine registers with the provided initialization sequence.

For more information, refer to thedwc_ddrphy_phyinit_I_loadPIEImage() program in the provided code in the phyinit directory.

6.3.2.2 (J) Initialize the PHY to Mission Mode through DFI Initialization

Initialize the PHY to mission mode by performing a DFI initialization sequence per the DFI spec.ification

6.3.2.3 (K) PHY is ready for Mission Mode transactions

The PHY is now in mission mode. The outputs are controlled by the DFI bus inputs and must remain valid as long as the PHY is in an operational state. If training was run, the memory is left initialized and in the Self-Refresh state.

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6.4 Power Management

The PHY power states can be grouped into two categories: Active (Mission Mode) and Standby.

6.4.1 Active / Mission Mode PHY Power States (PS0, PS1, PS2 and PS3)

The PHY support 4 Active power states (PS0, PS1, PS2, and PS3). The power states have the following restrictions:

- The frequency of a higher numbered active power state must not exceed the frequency of a lower numbered power state. For example, the frequency of PS3 must not exceed the frequency of PS2, PS1 or PS0.)
- Each power state supports a maximum transfer rate specific to the supported PHY and voltage limitations.
- Active power states are entered by a DFI Initialization or Frequency Change sequence, using the dfi_init_start and dfi_freq[4:0] interface

Note All DRAM(s) connected to the PHY must be in the following state before attempting a DFI Frequency change:

- In DDR4 :: DRAM must be in SelfRefresh
- In DDR4+RCD :: DRAM must be in SelfRefresh, and RCD may optionally be in powerdown.
- In LPDDR4 :: DRAM must be in SelfRefresh+Powerdown.
- The memory controller must ensure the DRAM FSP-OP state must match the destination frequency prior DFI Frequency change

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6.4.2 PHY Low Power and Standby States

The PHY provides a mix of low power states with varying exit latencies so that memory controller / SoC can dynamically take advantage of memory system idle windows.

Note PHY Exit Latency time is measured from the transition of dfi_init_start.

Table 6-2 PHY Low Power State Modes

Low Power State	PHY Exit Latency	PHY State	DRAM Commands available
DFI_LPDATA_ACK	T_{lp_wakeup}	DATA BYTES stopped Receivers are in stand-by	All commands (available other than data-bearing transactions).
DFI_LPCTRL_ACK	T_{lp_wakeup}	DATA BYTES stopped Receivers are in stand-by Chip selects inactive AC signals tristated/inactive except in LPDDR4 Mode[1] MEMCLK toggling	DES or Maintain Power-down or Maintain Self-Refresh
DFI_LPCTRL_ACK +DRAMCLKSTOP	T_{lp_wakeup}	DATA BYTES stopped Receivers are in stand-by Chip selects inactive AC signals tristated/inactive except in LPDDR4 Mode[1] MEMCLK stopped	Maintain Power-down or Maintain Self-Refresh (protocol specific).
LP2 +DFICLKSTOP	3us (3uS + 1280 DfiClks w/retain	DATA BYTES stopped Receivers powered-down Chip selects inactive AC signals tristated/inactive except in LPDDR4 Mode[1] MEMCLK stopped DFICLK stopped ZQ/LCDL Calibration off PLL in Standby	Maintain Self-Refresh

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Table 6-2 PHY Low Power State Modes

Low Power State	PHY Exit Latency	PHY State	DRAM Commands available
LP3 +DFICLKSTOP	33uS (33uS + 1280 Dficlks w/retrain)	DATA BYTES stopped Receivers powered-down Chip selects inactive AC signals tristated/inactive except in LPDDR4 Mode [1] MEMCLK stopped DFICLK stopped ZQ/LCDL Calibration off PLL in PowerDown	Maintain Self-Refresh
PHY IO Retention	Re-Initialization	CKE* driven to zero, MEMRESET held at previous state. All other Pins are tristated. VDD is off	Maintain Self-Refresh

1. In LPDDR4 mode, AC lines are VDDQ terminated, so AC signals are not tristated in low power modes

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6.4.2.1 DFI Low Power Interface (DFI LP)

The DFI Low Power Interface can be used to perform clock gating when there is a sufficient period of time between traffic through the PHY.

Entering and exiting the DFI LP state is performed according to the DFI LP protocol and may be performed while the dfi interface is active (for example, dfi_init_complete asserted *and* no ongoing frequency change handshake).

Prior to performing frequency or power state changes (including LP2/LP3), the dfi_lp_{data,ctrl}_req must be deasserted, since this interface must be inactive prior to frequency changes through dfi_init_start. This clean exit from DFI LP prior to frequency or power state changes ensures safe and well defined transitions and behaviors between power-states, while also preventing possible violations of the dfi_lp handshakes.

Note The LP2/LP3 power states provides superior power savings to that of the DFI LP alone.

In two-channel operation, the DFI Low Power Interfaces operate independently of one another.

If the PHY acknowledges a “dfi_lp_data_req” request, the PHY will perform the following power savings actions:

- Stop the clocks to the data bytes.
- Place all DQ/DQS receivers in standby/powerdown

Note dfi_lp_data_req may be entered anytime there are no in-progress dram read/write transactions

If the PHY acknowledges a "dfi_lp_ctrl_req" request, the PHY will perform the following power savings actions:

- Stop the clocks to the data bytes.
- Place all DQ/DQS receivers in standby/powerdown
- Stop the clocks to the address/command transmitters

Note The MEMCLK outputs to the dram will still be running (unless the memory controller explicitly asserts the dfi_dram_clk_disable pins – for additional power-savings)

6.4.2.1.1 Power Savings

For maximum power-savings during the DFI LP state, the PHY assumes that all pages are closed when the controller issues a dfi_lp_ctrl_req. Although the PHY can accept any legal input on the DFI control interface after the deassertion edge of dfi_lp_ack, the dfi_wrdata* interface cannot accept transactions for an additional four MEMCLKs.

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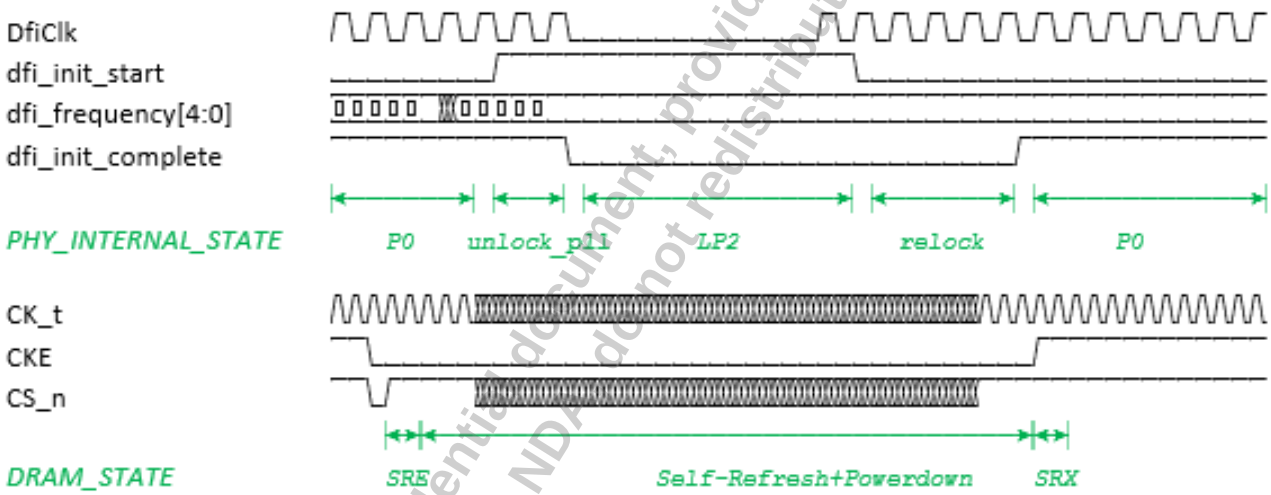
6.4.2.2 PHY Fast Standby (LP2): Leveraging the Frequency Change Protocol to Save Power

PHY Fast Standby (LP2) allows an SOC to save the maximum power while the DRAM is in Self-Refresh and also maintain a reasonable exit latency.

Figure 6-13 on page 140 shows a transaction where the source and destination state are equal. The following list shows the requirements of a PHY Fast Standby (LP2) transaction:

- By entering LP2, the controller may clock gate the entire PHY
- In DDR4 modes, restarting the DFI interface requires <3uS
- In LPDDR4 modes, restarting the DFI interface requires < (3uS + 2560 MEMCLKs)
  - LPDDR4 have larger exit latencies due to automatic link retraining to compensate DRAM drift

Figure 6-13 PHY Fast Standby (LP2) Transaction



Note During PHY LP2, the PHY impedance calibration state machine is paused. If the residency in LP2 is long enough that the system temperature has varied by greater than 20C, it is recommended for the controller to wait an additional 10uS after asserting edge of dfi_init_complete - before issuing the Self-Refresh Exit commands to the DRAMs. If the temperature change while in LP2 has not exceeded the threshold, the extra wait is not required.

Note When DfiClk stops (LP2 or LP3 mode), then DfiCtlClk can also be clock gated or stopped.

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6.4.3 Standby Power State (LP3/IO Retention)

The LP3/IO Retention power state is a non-operational low power state. The standby power state has the following properties:

- This is the lowest possible power state for the PHY.
- In this power state, the DRAM may either be in self-refresh, or in Reset.
- The core VDD and VAA power supplies can be powered down in this state. If the core VDD power supply is shut off, power consumption is predominantly determined by the device leakage on VDDQ and the number of active CKE lanes.
- The state of CKE and MEMRESET pins will be pReserved at their last values when the core VDD is shut off. VDDQ must remain valid for the value of the pins to be pReserved.
- The Standby power state is entered via a Frequency Change sequence, using the dfi_init_start and dfi_freq[4:0] interface.

Note

- When entering or exiting LP3/IO Retention, the DFI interface must be held in a valid state until PwrOkIn is set to 0. While in LP3/IO Retention, the DRAM signals required for proper IO Retention will maintain the appropriate state (including CKE and MEMRESET pins).
- The Memory Controller may ignore the dfi_phyupd_req signals during LP3.
- When DfiClk stops (LP2 or LP3 mode), then DfiCtlClk can also be clock gated or stopped.

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6.4.3.1 LP3/IO Retention Save Registers

To correctly exit retention, the values of PHY CSR's, including those trained by firmware or manually programmed, must be saved prior to entering mission mode. All writable PHY registers can be saved, or, if the configuration is known, PhyInit can be used to generate an optimized list.

Note The number of registers that must be saved prior to LP3/IO Retention entry and restored post LP3/IO Retention Exit varies based upon the DDR standard and the training steps run. PhyInit can be used to generate an initialization sequence that automatically includes saving retention registers based on PHY configuration and protocol. Refer to the *DDRn PhyInit Application Note* for more information.

The sequence generated by PhyInit during for I/O Retention Save performs the following steps:

1. Write the MicroContMuxSel CSR to 0x0 to allow access to the internal CSRs
2. Write the UcclkHclkEnables CSR to 0x3 to enable all the clocks so the reads can complete
3. Read and save all the registers appropriate for the given protocol and training
   a. The register address/data pairs must be saved in some part of the system (such as external non-volatile storage)
4. Write the UcclkHclkEnables CSR to disable the appropriate clocks after all reads done.
   a. For DDR4 , write the UcclkHclkEnables to 0x0
   b. For LPDDR4 , write the UcclkHclkEnables to 0x2
5. Write the MicroContMuxSel CSR to 0x1 to isolate the internal CSRs during mission mode

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6.4.3.2 LP3 / IO Retention Enter

Transitioning to the LP3/IO Retention power state has a few more steps than the active power state transitions.

Note Prior to the LP3/IO Retention Enter procedure, the values of the PHY configuration and trained registers must be saved as part of the PHY initialization process. Refer to "LP3/IO Retention Save Registers" on page 142 for more information.

The following is the full process to enter LP3/IO Retention:

1. Use the DFI interface to put the DRAM into Self-Refresh or Reset.
2. Transition the PHY to the LP3 / IO Retention state by using a DFI Frequency Change operation.
3. Set the PwrOkIn signal to 0. This will enable the data retention feature on the CKE and MEMRESET pins. These pins will hold the current values.
   a. Remaining PHY input signals must be valid, inactive states fro at least 10ns after the PwrOkIN deasserting edge
   b. The PHY input clocks are not required to toggle after the de-asserting edge of PwerOkIN.

Caution In a non-test configurations, the atpg_mode input to the PHY must be defined and driven to zero anytime the VDD supply is active.

4. Turn off the core VDD, VDDQLP and VAA supplies. These supplies can be turned off in any order. The VDDQ power supply must remain active during LP3/IO Retention.

Note This step is optional. Power supplies do not have to be powered down (turned off) at the end of LP3/IO Retention Enter. However, leaving the power supplies active does not provide the best possible power savings.

5. All PHY input values are now don't cares, and can go to X in simulation.

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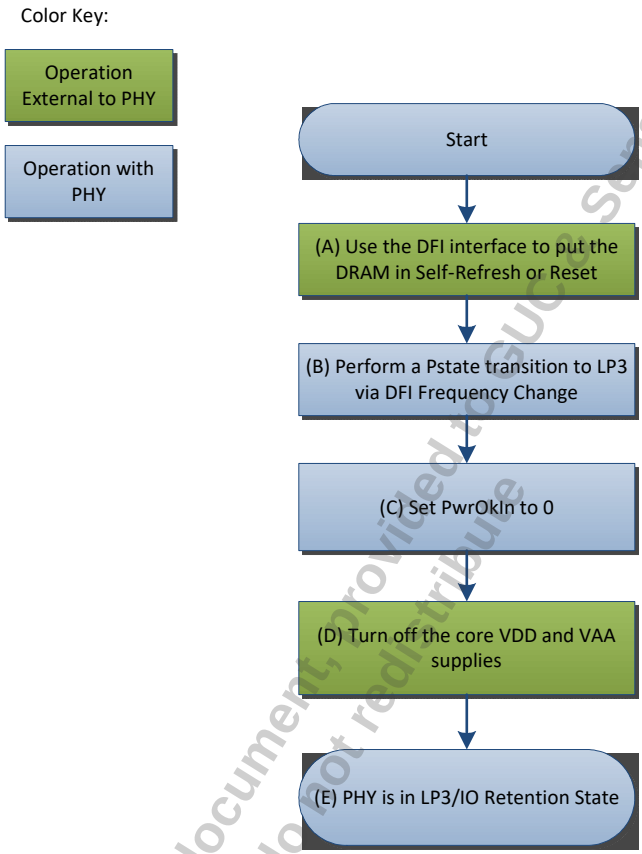
Figure 6-14 LP3 / IO Retention Enter



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6.4.3.3 LP3 / IO Retention Exit

The process to exit LP3/IO Retention is similar to the initialization sequence. PhyInit can be used to automatically generate a detailed retention exit sequence for a given configuration and DRAM protocol. Refer to the *DDRn PhyInit Application Note* for more information.

The following section describes the sequence at a high level.

Note Prior to the LP3/IO Retention Enter procedure, the values of the PHY configuration and trained registers must be saved as part of the PHY initialization process. Refer to "LP3/IO Retention Save Registers" on page 142 for more information.

The exit LP3/IO Retention steps are described in the following process (see the procedure in Figure 6-16 on page 131):

- Step A: The VDDQ power supply will already be active; restore the core VDD and VAA power supplies. This is the same requirement as in "(A) Bring up VDD, VDDQ, VDDQLP, and VAA" on page 134
- Step B: Start clocks and reset the PHY. This is the same requirement as in "(B) Start Clocks and Reset the PHY" on page 134
- Step C: Restore all PHY registers
  - Set up the PHY to write registers:
    - Write the MicroContMuxSel CSR to 0x0 to allow access to the internal CSRs
    - Write the UcclkHclkEnables CSR to 0x3 to enable all the clocks so the reads can complete
  - Issue register writes to restore values. These are all the PHY address/data pairs stored in the external non-volatile storage saved during initialization between Steps I and J.
  - Set up the PHY for mission mode:
    - Write the UcclkHclkEnables CSR to disable the appropriate clocks after all reads done:
      - For DDR4, write the UcclkHclkEnables to 0x0
      - For LPDDR4 , write the UcclkHclkEnables to 0x2
    - Write the MicroContMuxSel CSR to 0x1 to isolate the internal CSRs during mission mode
- Step D: D.Initialize the PHY to mission mode through a DFI initialization request. This is the same requirement as in "(J) Initialize the PHY to Mission Mode through DFI Initialization" on page 135
- The PHY is ready for mission-mode transactions

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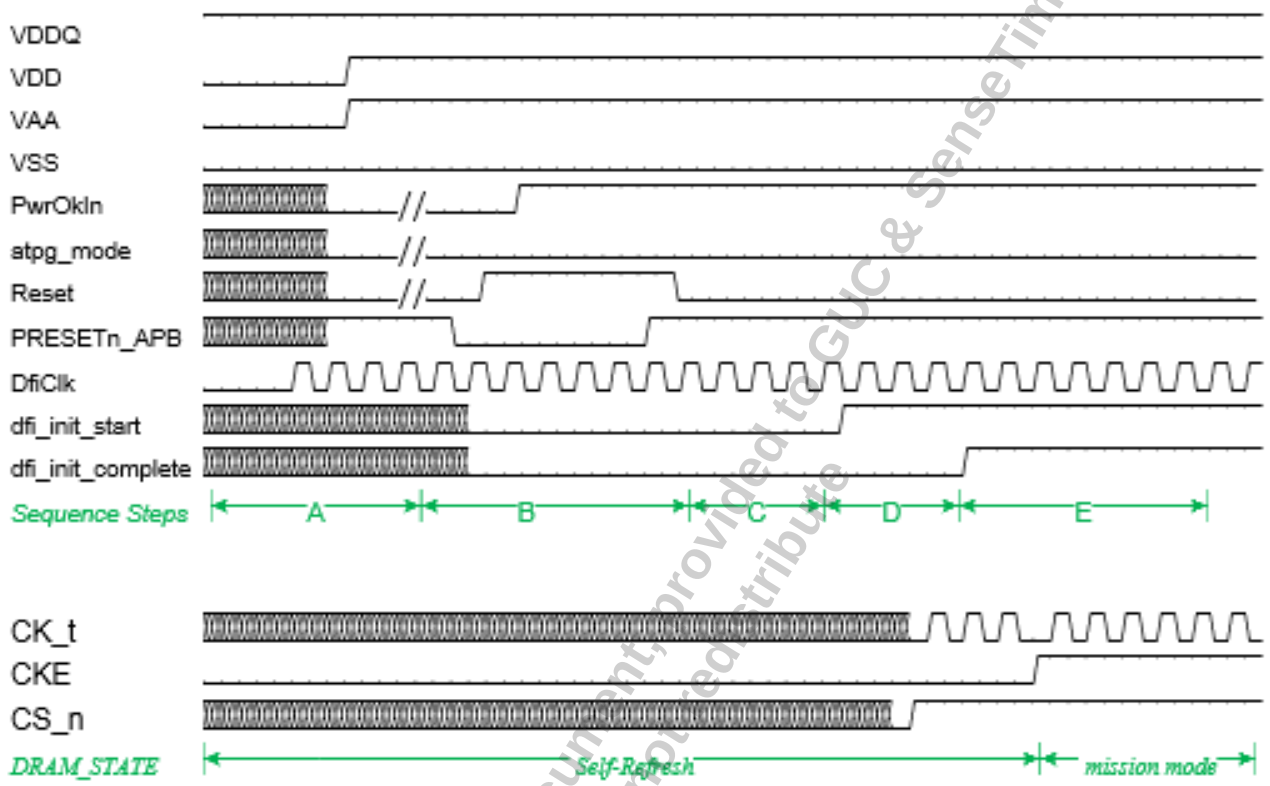
Figure 6-15 IO Retention Exit timing Diagram



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The following requirements must also be addressed when exiting LP3/IO Retention mode:

- For retention exit, all rules regarding resetting the PHY and enabling the clocks apply a standard reset sequence
- Since the CKE* and MEMRESET pin state must be protected, special care must be taken to ensure that the following signals:
  - atpg_mode = 1'b0
  - PwrOkIn = 1'b0
- The {BypassModeEn*, WRSTN} signals may be defined at VDD power-on, but must be driven to ZERO at least 10ns prior to the asserting edge of PwrOkIn

Caution

For proper retention operation, PwrOkIn must be held at 0 while VDD is above the threshold level during VDD ramp up or down.

The recommended process is to drive PwrOkIn directly from an always-on VDD power domain.

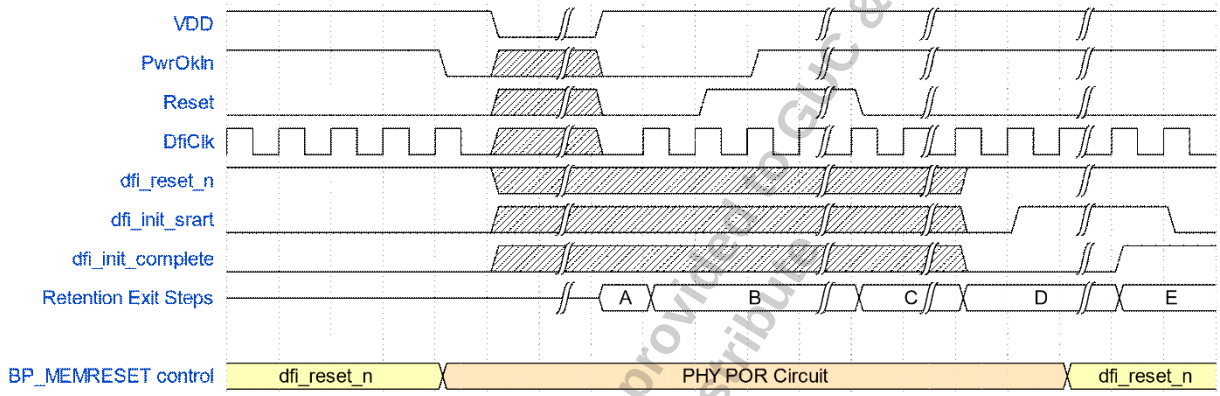
Alternately, PwrOkIn may be driven through core VDD combo logic from a different always-on domain. In this design, SPICE simulation should be performed using the models provided with the IP to ensure there is no gap in holding retention while VDD is ramped down and ramped up.

6.4.4 Protection of MEMRESET During Retention Enter/Exit

During mission mode MEMRESET signal is controlled by MC through dfi_reset_n on VDD domain. Since the state of this signal may become unknown during retention, special care must be taken to ensure MEMRESET is not asserted.

The following figure shows the state of MEMRESET during retention enter and exit.

Figure 6-16 DDR3/4 MEMRESET control during retention enter/exit



The PHY POR circuit deasserts BP_MEMRESET when in control. The memory controller must ensure dfi_reset_n is not asserted during yellow periods in diagram above. Alternatively MemResetL register can be used to override dfi_reset_n. In DDR4 the training firmware messageBlock D4Misc variable must be used to set MEMRESET protection.

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6.4.5 PHY Initialization Engine

The PHY Initialization Engine sequences the PHY between the various supported power states. This HW state machine ensures that power-gating, pll-lock, dll-lock, and other PHY initialization events occur correctly. The PHY Initialization Engine is controlled by the dfi_init_start and dfi_freq[4:0] signals.

The interface follows the DFI spec for Initialization and Frequency Change protocols. See the official DFI for more information on the protocol.

6.4.5.1 DFI Initialization

The DFI initialization protocol is used for the first transition of dfi_init_start. The protocol is as follow:

1. dfi_init_start must start at 0.
2. Set the value of dfi_freq[4:0] and dfi_freq_ratio to the appropriate value for the desired target power state. It is legal to use any active power state as the destination power state. The destination power state must have been trained using the correct frequency.
3. Set dfi_init_start to 1.
4. Wait for dfi_init_complete to be asserted.
5. Before the first frequency change operation, dfi_init_start must be set to 0. The timing of this operation is not critical, but must happen at least 16 cycles before the first frequency change.

The values on dfi_freq[4:0] and dfi_freq_ratio must be held stable between the assertion of dfi_init_start and the assertion of dfi_init_complete.

In two-channel operation, the PHY waits for dfi0_init start and dfi1_init_start to both assert to initiate any transaction. dfi0_freq and dfi1_freq must be the same value during initialization or frequency change transactions.

Note The PHY asserts and deasserts dfi0_init_complete and dfi1_init_complete simultaneously.

6.4.5.2 DFI Frequency Change

The DFI frequency change protocol is used for all transitions after the first 0 to 1 transitions.

1. Set the value of dfi_freq[4:0] and dfi_freq_ratio to the appropriate value for the desired target power state.
2. Set dfi_init_start to 1.
3. Wait for dfi_init_complete to be set to 0 (de-asserted).
4. Change the DfiClk frequency to the new desired frequency.
5. Once the clock is stable at the new frequency, set dfi_init_start to 0.
6. Wait for dfi_init_complete to be asserted.

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The values on dfi_freq[4:0] and dfi_freq_ratio must be held stable between the assertion of dfi_init_start and the assertion of dfi_init_complete.

Caution

The DFI specification is currently unclear about the conditions for dynamically changing the DFI Frequency through the dfi_freq_ratio pins. For good design, the DWC LPDDR4x multiPHY PUB currently uses an internal configuration register (replicated per PHY P-state) to enable DFI Frequency change.

It is recommended that the dfi_freq_ratio pins be driven as specified in the DFI 3.1/4.0 specification to ensure future compliance and interoperability with the DFI specification (and future versions of the DWC LPDDR4x multiPHY PUB).

Note

When entering PState with speeds <DDR666 on the first dfi_init, then the PHYInLP3 register must be set to 0x0 in dwc_ddrphy_phyini_userCustom_customPostTrain()

Note

The PHY ZQ calibration update state-machine only operates when the DFICLK is active. When the background ZQ calibration is enabled, the state machine is restarted on every p-state change. If the residency in a given p-state is less than the cycle-time of the calibration state-machine (<13uS at datarates requiring ZQCAL), the state-machine may not update the calibration code. This is generally harmless as the PHY will continue to use the previous working ZQ calibration result.

Note

All DRAM(s) connected to the PHY must be in the following state before attempting a DFI Frequency change:

- In DDR4 :: DRAM must be in SelfRefresh
- In DDR4+RCD :: DRAM must be in SelfRefresh, and RCD may optionally be in powerdown.
- In LPDDR4 :: DRAM must be in SelfRefresh+Powerdown.
- The memory controller must ensure the DRAM FSP-OP state must match the destination frequency prior DFI Frequency change
- If entering PState with speeds <DDR666 on the first dfi_init, then the PHYInLP3 register must be set to 0x0 in dwc_ddrphy_phyini_userCustom_customPostTrain()

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6.4.5.2.1 Encoding for dfi_init_freq[] bus

The PHY supports low-latency dynamic frequency changes through the in-band DFI frequency change protocol.

The PHY maintains up to 4 independent register contexts (named P0,…,P3) for up to 4 memory system operating frequencies. These 4 contexts are configured (by system software) and trained (by PHY firmware) at initial boot. Once trained, and configured, the PHY has full Hardware acceleration of all sequences {e.g. PLL relock, ZQ cal, LCDL cal, register context switch} needed to switch operating states.

This operating state switching is performed with following the DFI3.1/DFI4.0 Frequency change protocol using the signals {dfi_init_start,dfi_freq[4:0],dfi_freq_ratio,dfi_init_complete}.

The following table shows the allowable values for dfi_freq[] for both the Initialization or Frequency Change operations.

Note For operation above 667Mbps, dfi_freq[4:0] encodings 0x10/0x11/0x12/0x13 cannot be used since retraining is mandatory above this operational frequency.

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Table 6-3 dfi_freq[4:0] encoding

Encoding	Target State	PHY Operation	Notes
New: 0x00	Go to PHY State P0	DDR4 Relock PLL LPDDR4 Relock PLL and Retrain Link	1,2,3,8,9
0x01	Go to PHY State P1		
0x02	Go to PHY State P2		
0x03	Go to PHY State P3		
0x07:0x04	Reserved	-	-
0x08	Remain at PHY State P0 +retrain_only	DDR4 ■ Retraining is not required LPDDR4 ■ Retraining occurs only for daterates equal to or above 667	4,5,6
0x09	Remain at PHY State P1 +retrain_only		
0x0A	Remain at PHY State P2 +retrain_only		
0x0B	Remain at PHY State P3 +retrain_only		
0x0F:0x0C	Reserved	-	-

Table 6-3 dfi_freq[4:0] encoding (Continued)

Encoding	Target State	PHY Operation	Notes
0x10	Go to PHY State P0 +skip_retrain	Relock PLL	2,6,7
0x11	Go to PHY State P1 +skip_retrain		
0x12	Go to PHY State P2 +skip_retrain		
0x13	Go to PHY State P3 +skip_retrain		
0x1E:0x14	Reserved	-	-
0x1F	Go to PHY State LP3 (PHY Deep Sleep / Retention Enable)	-	8,9

Notes:

1. These encodings may be chosen at any time without restrictions
2. DFICLK may be gated and/or change frequency when { dfi_init_start=1,dfi_init_complete=0}
3. In LPDDR4 modes only, link retraining will occur for all populated ranks. No link retraining occurs in DDR4, as well as LPDDR4 at data rates equal to or great than 667.
4. When choosing these encodings, the target PHY State must be the same as the current PHY State
5. This step causes the PHY to retrain the link with the minimum possible latency, by skipping the PHY PLL stop and relock sequence. Since the PLL stop/relock is skipped; DFICLK must not be gated and/or change frequency when { dfi_init_start=1, dfi_init_complete=0}
6. Since link retraining is not required in DDR4 modes -- these encodings are not applicable in these modes.
7. These encodings may be issued when the controller has determined that link retraining is not required.
8. LP3 Exit should be always followed by dfi_freq 0, 1, 2, 3. Other frequency transitions are deemed invalid and will result in undefined behavior.
9. If the current PHY state is LP3, an additional **30uS** may be required to enter the target state.

The following table and formula provides bounds on $t_{init\_complete}$ based on dfi_freq encoding. The total latency is given by the following equation:

- $t_{init\_complete} = t_{fixed\_latency} + nDfiClks * DfiClkPeriod$

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Table 6-4 dfi_freq encoding and tinit_complete latency

Encoding	Data Rate	Number of DfiClks (nDfiClks)		Fixed Latency	Notes
		LPDDR4	DDR4	$t_{fixed\_latency}$ (us)	
0x1-0x3	All Data Rates	1280	-	3	2,4,5
	50 <= Data Rate < 667		270	2	3,5
	667 <= Data Rate < 800		0	3	3
0x8-0xa (skip_relock)	50 <= Data Rate < 667	-	-	-	1
	667 <= Data Rate < 800	1400	-	0.5	4,5
	800 <= Data Rate < 1600	1300	-	0.5	4,5
	1600 <= Data Rate < 2400	1200	-	0.5	4,5
	2400 <= Data Rate < 3200	1100	-	0.5	4,5
	3200 <= Data Rate < 4000	1000	-	0.5	4,5
	4000 <= Data Rate	900	-	0.5	4,5
0x10-0x13 (skip_retrain)	50 <= Data Rate < 800	270	270	2	4,5
	800 <= Data Rate < 1066	340	340	2	4,5
	1066 <= Data Rate	375	375	2	4,5

Notes:

1. Re-training is unconditionally skipped at low data rates.
2. Only applies to LPDDR4
3. Only applies to DDR4
4. Extra 1- DfiClks of latency must be added if LPDDR4 x8 devices are used because they have a higher read latency compared to x16 devices
5. The value of 4*DWC_DDRPHY_PIPR_DFI_MSC DfiClks must be added to the total latency as a direct result of adding pipe stages during RTL synthesis.

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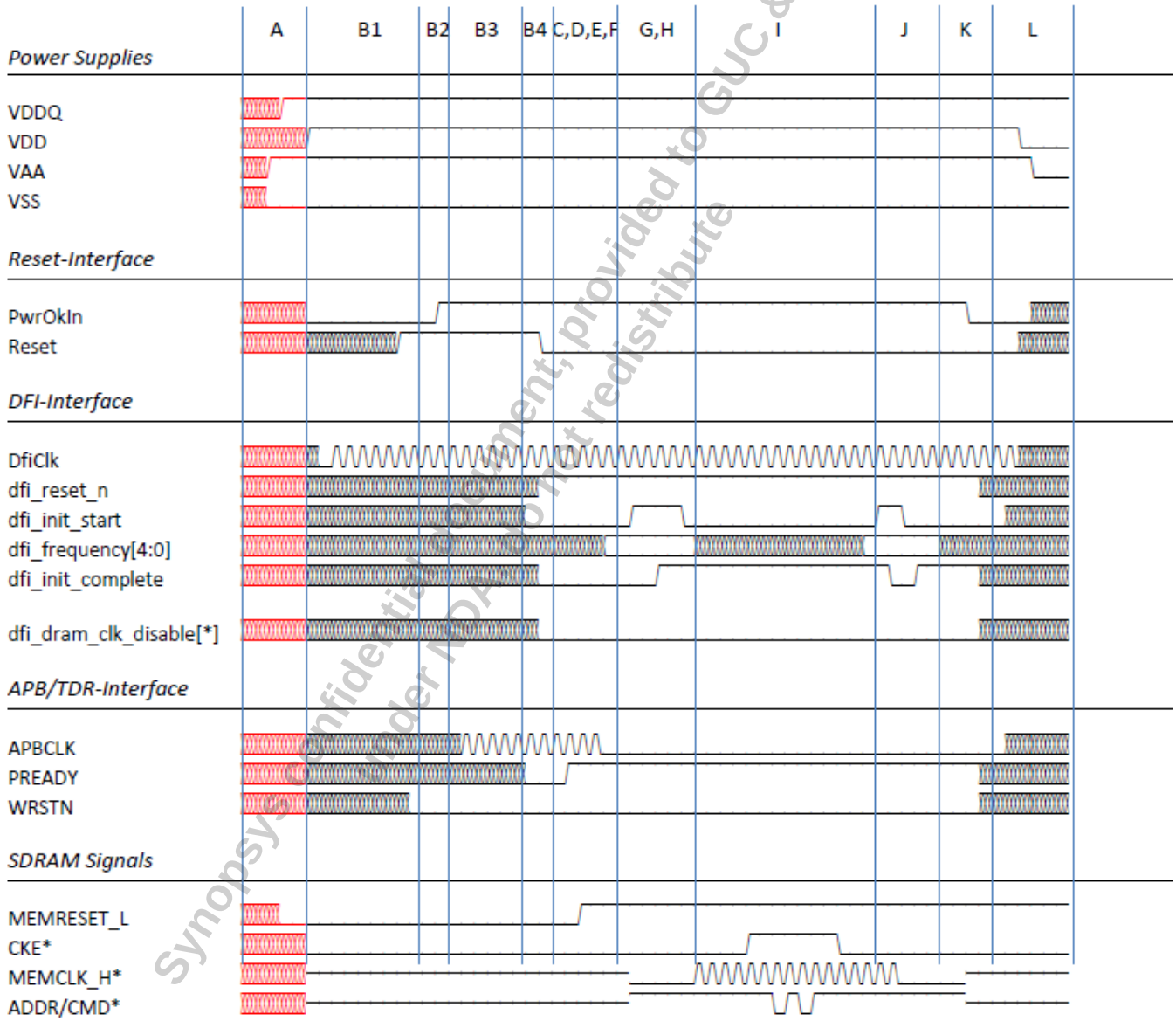
6.4.5.3 Example Waveforms for PHY Initialization Engine operation

The following waveforms illustrate the process for cold boot, initialization and a frequency change to the LP3/IO Retention power state. These waveforms do not include the execution of the training firmware, which would happen as part of step (F).

Figure 6-17 PHY Reset / Retention Sequence



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Key for waveform steps:

- A: Initial Power Supply Ramp
  - Supplies may stabilize in any order

- B1: PHY ColdReset Period
  - DfiClk, Reset, WRSTN may be X
- B2: PHY ColdReset Exit
  - DfiClk, Reset, WRSTN must be valid
- B3: PHY Reset Period
  - APBCLK, DfiClk must run for >64 cycles
- B4: PHY Reset Exit

a. APB/DFI inputs @ valid reset-state

- C, D, E, F: Pre DFI-Init
  - PHY FW/CSRs must be loaded
  - PHY Training may be invoked
    - PHY Training will set MEMRESET_L = 1
- G,H: DFI-initialization @ Requested Frequency
  - PHY will assert dfi_init_complete when ready
- I: Mission Mode operation
  - DFI interface sets SDRAM pin values.
- J: DFI frequency change [to LP3]
  - PHY will protect CKE* , MEMRESET in anticipation of PwrOkIn falling edge
- K: PwrOkIn falls
  - PHY IOs in retention
- L: Non-IO Supply Power Down
  - VAA, VDD may be powered down in any order.
  - All inputs may go X
  - PwrOkIn must not go X ahead of VDD →0
  - VDD,VAA must not go X [in Verilog simulation]
  - VDDQ must stay active

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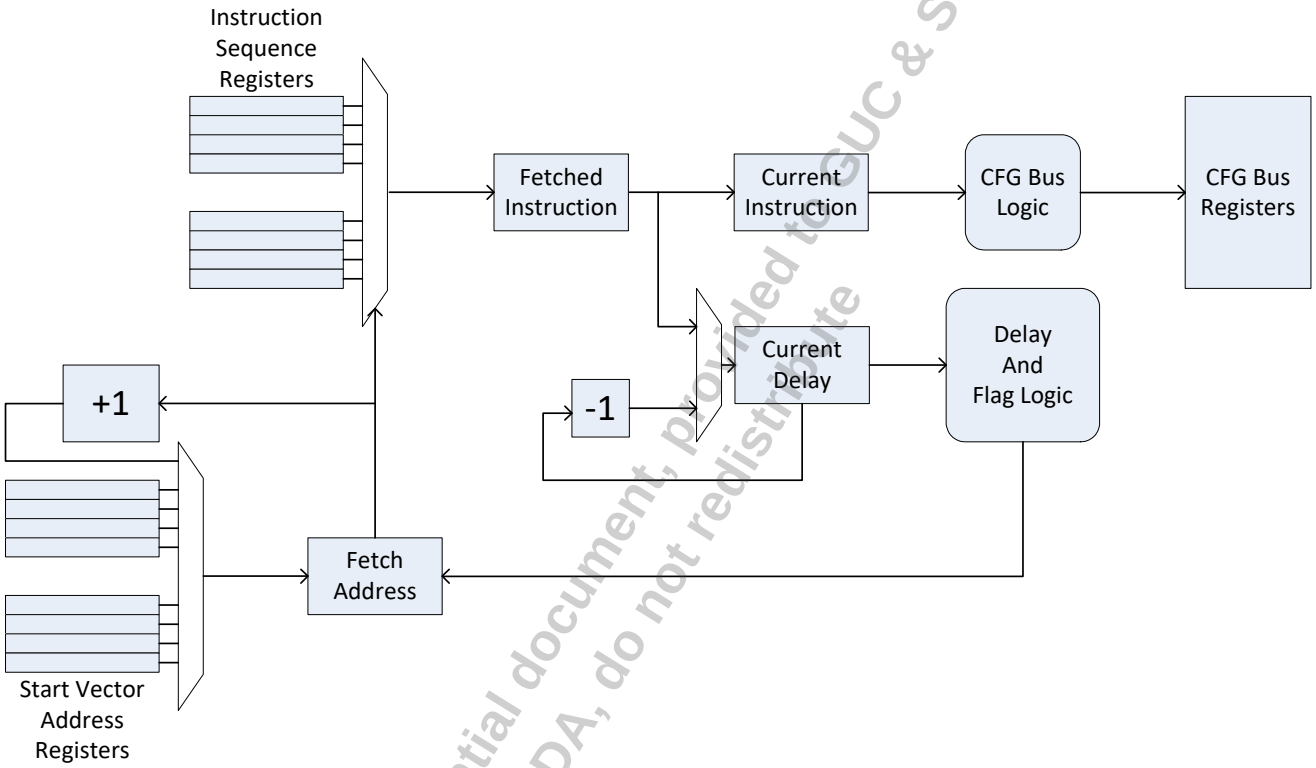
6.5 PHY Initialization Engine Description

The state transitions are handled through the PHY initialization Engine, which is a programmable micro-sequencer. The micro-sequencer is triggered on active edges of dfi_init_start as per the DFI initialization and frequency change protocols.

Figure 6-18 PHY Initialization Engine Block Diagram



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The micro-sequencer operates as a simple fetch/execute machine. It has no branching or looping capabilities. It is capable of executing up to 1 micro-instruction per cycle, but instructions can be programmed to take longer than a cycle by using the delay field of each instruction.

It is programmed through the APB bus with the Initialization and Frequency Change sequences after cold reset and before the DFI initialization sequence is executed. The micro-instruction sequence is provided as part of the initialization that must be performed via the APB bus following a Cold Reset or LP3/IO Retention Exit. The sequence is loaded as part of step (C) in the initialization process described in "PHY Initialization" on page 132.

Until the sequence memory is loaded, the dfi_init_start/dfi_init_freq[] operation is not allowed and attempting to perform an Initialization or Frequency Change sequence will not complete successfully.

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7 Architecture

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This chapter describes the following:

- "Configuration Port" on page 158
- "APB Interface" on page 158
- "Training Sequence" on page 162
- "2T Timing and Control Gear Down Support" on page 162
- "Impedance Calibrator" on page 165
- "Low Power Design" on page 168
- "Interrupt Implementation" on page 169
- "ARCv2 Microcontroller" on page 170
- "SRAM Interface" on page 172
- "Shared AC" on page 175

7.1 Configuration Port

The configuration port provides access to PUB registers. The configuration port includes an APB interface and a TDR serial interface.

7.2 APB Interface

An APB interface can be selected to be the main access protocol for PUB configuration registers.The PUB APB interface is compatible to APB4. Refer to the AMBA APB Protocol Specification v2.0 for details about the APB protocol. The configuration port provides access to PUB registers

The APB address (paddr[g-1:0]) points to a 16-bit data word. Therefore if the rest of the chip is using byte-based APB addresses, then the PUB APB address paddr_arb[g-1:0] must be connected to paddr[g:1] at the chip level. Otherwise if word addresses are used throughout the chip, then PUB paddr_arb[g-1:0] must be connected to chip paddr_arb[g-1:0].

The APB interface supports read register and write register accesses with wait states. If the APB Master adheres to the APB wait state protocol, there are no read register and write register issues.

7.2.1 APB Interface Access Rules

The APB interface must be accessed under the following rules:

1. The APB interface should not be active during mission modes. Any writes during mission mode may result in unexpected behavior
2. The APB interface can only read/write mailboxes during training (while the uCtrl owns the CSR bus))
3. PSTRB functionality is not supported

Note Refer to PSTRB_APB[1:0] in "Signal Descriptions" on page 45 for more information on the following signals:

- During WRITE, PSTRB_APB[1:0] = 2'b11

  During READ, PSTRB_APB[1:0] = 2'b00

4. The APB interface should be inactive, though not necessarily in reset, while the DfiClk is changing frequency.

7.2.1.1 PPROT_PIN Configuration and Purpose

A hardware configurable port for comparison against the value on PPROT during activity

PPROT_PIN[2:0] is a static value provided by the SOC

1. Typically tied off to a particular value, sometimes fuse programmed, or in some highly secure environments this is randomized by a different security engine.
2. The PHY only responds to APB requests where PPROT_APB matches the value of PPROT_PIN
   - This functionality prevents unauthorized accesses to the registers

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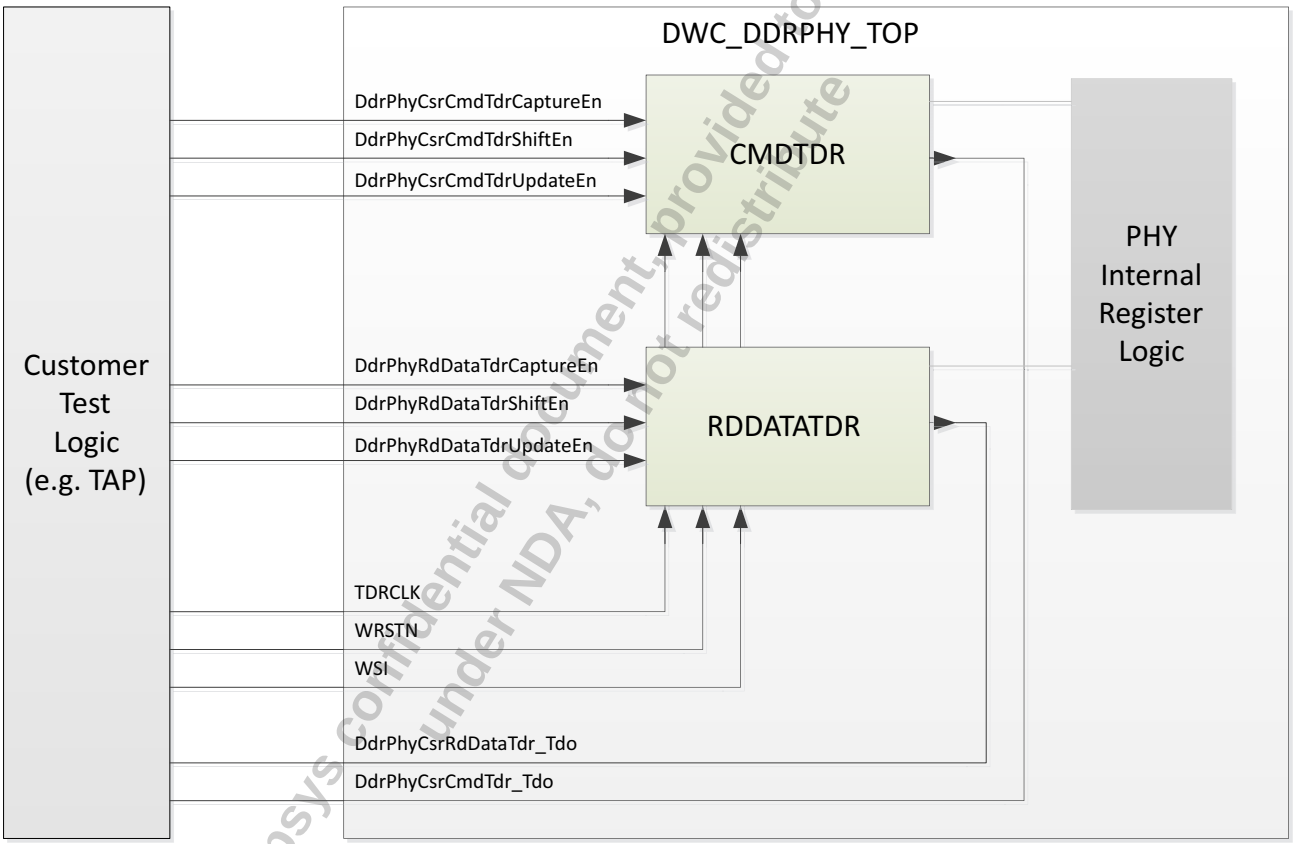
7.2.2 TDR Serial Interface

All of the PHY CSR address space can be accessed through a pair of TDR registers in the PHY. TDR means Test Data Register and it's design is based on the 1149.1 DR-Scan Sequence standard. For example, with a customer supplied TAP controller (optional), a JTAG port can serially access all of the PHY CSRs. This interface may be useful to access or trigger PHY test and/or debug modes without requiring full functional vectors. This method of accessing PHY CSRs can coexist with APB and microcontroller methods. The CSR access logic does not contain arbitration, so the TDR registers should be used only when APB and Microcontroller accesses are suspended. This condition happens naturally in most situations.

The following Figure shows an example implementing for JTAG access of CSRs from the SOC level.

Figure 7-1 Example of CSR Access Through TDR



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7.2.2.1 CsrCmdTdr and CsrRdDataTdr Register Bit Definitions

Table 7-1 CsrCmdTdr and CsrRdDataTdr Register Bit Definitions

TDR Register Bit Names	Bit Definitions
CsrCmdTdr	
TDR_CsrCmdChain[44:29]	CSR Write Data, 16-bits
TDR_CsrCmdChain[28]	WR_RD=1 Write CSR WR_RD=0 Read CSR
TDR_CsrCmdChain[27:0]	CSR Address
CsrRdDataTdr	
TDR_RdDat[15:0]	CSR Read Data, 16-bits

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7.2.2.2 TDR Procedure for CSR Write

The PHY TDR access procedure matches the access pattern for any user defined TDR.

To Perform a CSR Write, a single transaction to TDR DdrPhyCsrCmdTdr is sufficient.

- Capture Phase [assert DdrPhyCsrCmdTdrCaptureEn for 1 clock cycle]
  - Assert DdrPhyCsrCmdTdrCaptureEn for 1 clock cycle
  - This TDR does not have defined capture data .
- Shift Phase [Assert DdrPhyCsrCmdTdrShiftEn for 45 clock cycles]
  - Serially apply 28-bits of CSR address, followed by the WR_RD bit set to 1, followed by the 16-bits of CSR write data to the WSI input.
- Update Phase [Assert DdrPhyCsrCmdTdrUpdateEn for 1 clock cycle]
  - Applies the write command to the CSR path.

7.2.2.3 TDR Procedure for CSR Read

The PHY TDR access procedure matches the access pattern for any user defined TDR.

To Perform a CSR Read, two transactions are required. The first transaction is to TDR DdrPhyCsrCmdTdr to perform the internal command. The second transaction is to TDR DdrPhyCsrRdDataTdr to capture the data.

- First TDR Transaction to DdrPhyCsrCmdTdr
- Capture Phase [assert DdrPhyCsrCmdTdrCaptureEn for 1 clock cycle]
  - Assert DdrPhyCsrCmdTdrCaptureEn for 1 clock cycle
  - This TDR does not have defined capture data .
- Shift Phase [Assert DdrPhyCsrCmdTdrShiftEn for 45 clock cycles]
  - Serially apply 28-bits of CSR address, followed by the WR_RD bit set to 0, followed by the 16-bits of zero to the WSI input.
- Update Phase [Assert DdrPhyCsrCmdTdrUpdateEn for 1 clock cycle]
  - Applies the read command to the CSR path.
- Wait at least 10 TDRCLK cycles
- Second TDR Transaction to DdrPhyCsrRdDataTdr
- Capture Phase [assert DdrPhyCsrRdDataTdrCaptureEn for 1 clock cycle]
  - Assert DdrPhyCsrCmdTdrCaptureEn for 1 clock cycle
  - The TDR will Capture the internal CSR Read data.
- Shift Phase [Assert DdrPhyCsrRdDataTdrShiftEn for 16 clock cycles]
  - Observe DdrPhyCsrRdDataTdr_Tdo to see results of the Captured data. Incoming WSI may be any don't care value (zeros recommended).
- Update Phase [Assert DdrPhyCsrRdDataTdrUpdateEn for 1 clock cycle]

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- Has no effect for this TDR.

Note This step is not strictly necessary in the design, however it was included because the IEEE 1149.1 Specification for TDR accesses indicate that the update is required.

7.3 Training Sequence

The training firmware is loaded and controlled by accessing CSRs and memory. Please see the *DesignWare Cores LPDDR4x multiPHY Training Application Note* for more information.

7.4 2T Timing and Control Gear Down Support

The PHY supports both 2T timing and DDR4 Control Gear Down mode. 2T timing is meant to relax the timing for the purpose of increasing setup and hold times for the address and command signals between the PHY and DRAM at high frequencies, usually in heavily loaded systems with a large fanout on the address/command bus that compromises the signal integrity of the received eye at the DRAMs.

2T timing simply uses two clock cycles for every command and stretches the address/command signal set-up time to span 1.5 clock periods. 2T timing is strictly a function of the memory controller command timing and does not require any special configuration of the DRAMs and is supported for DDR3 or DDR4. DDR4 Control Gear Down mode is intended to further improve 2T timing by allowing the DDR4 SDRAM control bus (CS, CKE, and ODT signals) to operate in a similar 2T mode (referred to as "2N" which is the JEDEC term for "2T" timing on the control bus), along with the address and command signals when they operate in 2T mode.

DDR4 Control Gear Down mode does require the DDR4 SDRAM to be specifically configured to operate in that mode as outlined in the DDR4 JEDEC standard.

Note New versions of the JEDEC RCD02 Specification have added support for RCD02 Geardown Mode. However these RCD02 features were added after PHY Design Freeze, and thus Geardown mode is not supported in DDR4 RDIMM or DDR4 LRDIMM configurations.

The following information is clarification supplemental to the JEDEC and DFI specifications. For more information, please see those specifications.

The PHY can be statically configured (in each PHY operating state) to have CA TIMING in either 1T or 2T mode.

- In 1T mode :: CK, CS, CA all have the same nominal timing [e.g. ATxDly*[6:0] = 0x00]
- In 2T mode :: CK, CS, have the same nominatl timing [e.g. ATxDly{CK,CS}[6:0] = 0x00] ; CA is delayed by 1UI [e.g. ATxDly{CA}[6:0] = 0x00]

For Geardown, MEMCLK must already be running at the appropriate frequency (i.e. >=1200MHz). Since this is already a challenging SI environment for the CA bus – the phy supports entering Geardown (while already in 2T timing mode). This ensures that the only transition on the CA bus for the MRS and SyncPulse will be the CS_n signal

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After the controller issues the syncpulse – the dfi_geardown signal can assert. The phy takes advantage of the requirement that the controller is sending DES to glitchlessly switch the timing of CS.

The PHY does not require all commands to start @ p0 in 2T/2N modes. However, it is recommended to keep this constraint to take advantage of the PHY dynamic tristating feature on Address/Command. Un-aligned commands separate out the command/chip-select information across 2 DFICLK cycles, so it is difficult to correctly tristate the bus without adding latency.

If the controller would like to keep the flexibility to issue 2T commands spanning different DFICLK cycles, we have a feature to keep the tristate ability – assuming one controller hint. This feature relies on the controller sending a specially encoded "IDLE" command over the DFI bus. When the PHY sees the IDLE command, it will tristate the bus. Please see register "TristateModeCA" for more details on this.

When both 2T and Geardown are enabled, the interface will have the following behavior:

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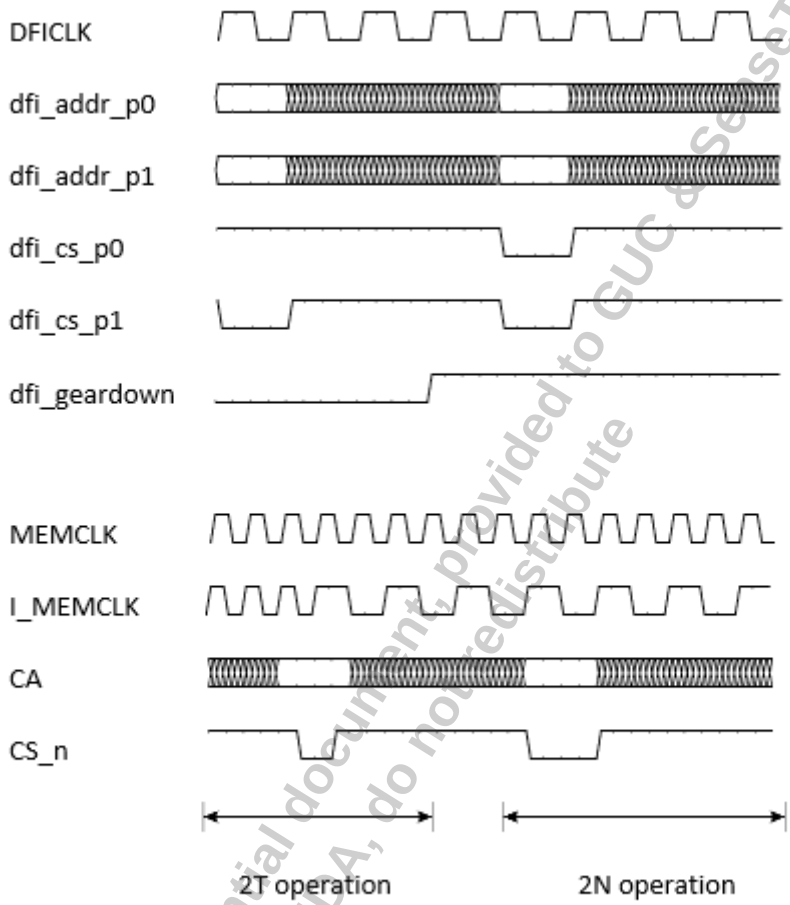
Figure 7-2 2T TIMING ' GEARDOWN [note, both CA, CS_n delayed by 1UI in geardown] {ATxDly.CK[6:0] = 0x00 , ATxDly.CA[6:0] = 0x40, ATxDly.CS[6:0] = 0x00 }



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Note The timing of the CS is modified according to the setting of the DFIGEARDOWNCTL CSR (see "Register Description" on page 103 for more information).

7.5 Impedance Calibrator

The PHY incorporates an impedance compensation engine to match a target value of resistances despite variation in Process, Voltage and Temperature. The analog circuits used for this purpose are grouped inside the dwc_ddrphymaster_top while the synthesizable portions of the controller sit inside the PUB.

The goal of the compensation engine is as follows:

- To find the thermometer pull-down driver code that gives the target DC resistance.
- To find the thermometer pull-up driver code that gives the target DC resistance.
- Transmit these codes to the mission mode drivers with no glitching of normal driver operation while compensation engine is enabled.

7.5.1 Operation

There are three specific calibration stages:

- **Comparator Offset Calibration (Cmpr5):** In which the internal differential offset in the calibration comparator is adjusted to be zero. This does not use the external reference resistor.
- **P Calibration (PExt):** In which the calibrator, with reference to the external pull down resistor, determines the pullup thermometer code for the drivers.
- N Calibration (Next): In which the calibrator, with reference to the external pull down resistor, determines the pullup thermometer code for the NMOS pull up drivers
- **N Calibration (NInt):** In which, with reference to the result of P calibration (and not the external resistor directly), the calibrator determines the pulldown thermometer code for the drivers.

The calibrator is highly programmable through multiple CSRs. It contains the following broad features:

- The result for each target may have an offset added or subtracted.
- The result for each target may be over-ridden.
- The period with which the calibrator runs is variable.
- The reference voltage into the compensation unit are selectable per calibration stage.

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7.5.2 Impedance Calibration Engine Setup

The PHY requires the ZN reference (used for impedance calibration and compensation) to be at the target impedance prior to starting the PHY Impedance Calibration engine. The ZN reference impedance must be stable from this point forward until a reset (or power-cycle) event.

Before a calibration cycles can be started, a few related csr's should be programmed according to the system implementation. These include:

- CalDrvStr0: The calibrator uses a programmable external grounded high tolerance resistor as the reference. This csr should be programmed in accordance with the resistor value. Please refer to the PUB register table specification for settings. This resistor may not be shared between two instances of a phy.
- CalUclkInfo: The internal counters in the engine use this value for their various wait times. The engine runs on DfiClk thus this csr should be programmed with the number of DfiClk cycles in 1us. If programmed incorrectly, calibration results may be inaccurate.
- CalOnce: This is used to determine the behavior of impedance calibration when it is kicked off. If set to 1, the engine will only perform 1 calibration cycle when CalRun is asserted. Otherwise it will continuously perform a calibration cycles with intervals determined by CalInterval.
- CalInterval: This value determines the intervals to perform continuous impedance calibration kickoff.

Note Synopsys recommends keeping all other calibration related CSR's at their default values.

7.5.3 Starting Impedance Calibration

A calibration cycle is started by writing 1 to CalRun csr.

The wait time for impedance calibration is dependent on DfiClk Freq, CalSlowCmpana, CalNumVotes and CalUClkTickPer1uS. At worst case with CalSlowCmpana=1, CalNumVotes=7, CalUClkTickPer1uS set for 166Mhz DfiClk the expected wait time is 36us. It is recommended to check the digital simulations for a more accurate calibration time representing a specific use case.

Note Before starting a calibration cycle, all related csr's must be setup as required. Once Impedance Calibration is complete, the PHY propagates the results to the thermometer codes automatically.

Impedance calibration must be performed as part of PHY initialization as described in "PHY Initialization" on page 132.. The memory controller is expected to simply wait the expected calibration time until calibration is done before assertion of dfi_init_start. No further interaction is required from the memory controller. The Result of the calibration can be queried in Cal<Stage>.

Note The impedance calibrator asserts CalBusy until internal FSM's have run though all the stages of calibration. It is not required to poll CalBusy.

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7.5.4 Disabling or Overriding Impedance Calibration Results

Each stage of the calibration can be disabled individually via Cal<stage>Dis. If set, the engine will simply skip the stage next time it starts. If a stage is disabled, the value of Cal<Stage>Ovr will be propagated to the drivers instead of the engine results.

7.5.5 Offsetting Calibration Results

The engine can also add a systematic offset to the result of each stage before being used by other stages via the Cal<Stage>Offset.

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7.6 Low Power Design

The PHY may reduce its power through selective settings of CSRs such as <Drive Strength>, <DBYTE Enable>, <ANIB lane enable>, etc., based on system configuration requirements.

In addition selected analog circuits within the PHY design provide additional lower-power settings that may be useful in certain configurations.

7.6.1 Dynamic Per-MEMCLK Address Tristate

In DDR4 mode, the PHY can dynamically and transparently tristate the address/command bus on a per-MEMCLK basis to save power anytime the outgoing command is a deselect. This saves significant termination power at the system level, as the Address/Command bus is terminated to VDDQ/2 in DDR4 systems.

In DDR4 (1T address/command timing), this feature works transparently, the PHY will tristate A*/BA*/BG*/RAS_n/CAS_n/WE_n anytime all ranks are deselected.

In DDR4 (2T address/command timing), this feature will require extra support from the controller, please see the register TristateModeCA and "2T Timing and Control Gear Down Support" on page 162 for more information.

In LPDDR4, the feature should be disabled, as it is unnecessary per protocol -- CA[5:0] is VSSQ terminated, and tristating does not save power (see register TristateModeCA).

Note If DDR4 CAL mode is enabled, the Dynamic Per-MEMCLK Address Tristate muct be disabled (see register TristateModeCA::DisDynAdrTri

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7.7 Interrupt Implementation

The PHY has a dedicated active low output signal – dwc_ddrphy_int_n. This output has five registers which are used to determine the state of the signal – csrPhyInterruptEnable, csrPhyInterruptMask, csrPhyInterruptClear, csrPhyInterruptFWControl and csrPhyInterruptStatus.

There are several interrupts which are defined for the PHY, see csrPhyInterruptStatus for details. Some interrupts are controlled by the PHY Hardware in response to hardware error events, others are controlled by the PHY Firmware, and a few can be controlled by the user.

The Firmware posts interrupts to csrPhyInterruptFWControl as appropriate. Once written the values will remain unchanged until the Firmware re-writes the register.

csrPhyInterruptEnable is used to either allow or dis-allow an interrupt's status to appear in csrPhyInterruptStatus. In order for the interrupt to be registered in this read-only register the corresponding bit in csrPhyInterruptEnable register must already be set to 1 at the time the interrupt is detected.

It is possible to see an interrupt in csrPhyInterruptFWControl but not in csrPhyInterruptStatus if the corresponding bit in csrPhyInterruptEnable is 0.

Once an interrupt is registered in csrPhyInterruptStatus it will be used to assert the dwc_ddrphy_int_n output signal if the corresponding bit in csrPhyInterruptMask is 0. If the corresponding bit in csrPhyInterruptMask register is 0 and the dwc_ddrphy_int_n output signal is negated when an interrupt is indicated in csrPhyInterruptStatus, then the dwc_ddrphy_int_n output signal will be asserted. If the dwc_ddrphy_int_n output signal is already asserted no change will be made.

Interrupts are reset or cleared using csrPhyInterruptClear. Writing a 1 to a bit of this register clears the corresponding interrupt in csrPhyInterruptStatus. csrPhyInterruptClear is implemented as write-1-to-clear and so is always read as 0.

When an interrupt is cleared from csrPhyInterruptStatus and no other unmasked interrupts remain asserted, the dwc_ddrphy_int_n output signal will negate. If other interrupts remain asserted and are also unmasked then no change will be observed on the dwc_ddrphy_int_n output signal.

Clearing an interrupt from csrPhyInterruptStatus does not affect the value in the csrPhyInterruptFWControl. It is possible to clear an interrupt from csrPhyInterruptStatus and still see the corresponding bit set in csrPhyInterruptFWControl. An edge detector is used to detect changes in csrPhyInterruptFWControl so once the interrupt is cleared it will not be re-asserted in csrPhyInterruptStatus until csrPhyInterruptFWControl is cleared to 0 and subsequently re-written to a 1.

In the event that an interrupt posts in the same clock cycle that is it cleared, the posting operation will take precedence.

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7.8 ARCv2 Microcontroller

The microcontroller is an ARCv2 EM4 configuration custom generated with a simple set of features to make it very small, yet highly effective for training the pin timing to the off-chip DIMM arrays. The microcontroller core uses a 32-bit Harvard architecture to execute the training application, written in C. The training application controls the pin timing to the DIMMs by writing and reading PHY CSR registers to change pin delays or to launch processes using separate ACSM and DCSM training engines that can iteratively search for the timing edges of the data eye while the C application monitors their results. The training application calculates the final eye centers and applies the optimized values to the PHY CSRs when training completes.

The ARCv2 microcontroller is embedded into the DDR PHY design by using bridges to convert the AHB-Lite IO paths to the protocol used internally on the Cfg Bus. A bridge known as the "CSR Bridge" allows code running on the microcontroller to see the PHY CSRs as directly mapped into its memory address space. PHY CSRs, being an array of registers, looks similar to an array of memory locations, albeit distributed throughout the PHY design. In reverse, an APB interface can also control the Cfg bus and can see the ICCM and DCCM microcontroller memories as mapped into PHY CSR address space through the use of the "BIOS Bridge." Mapping the microcontroller memories into PHY CSR space provides a means of loading the application program into the instruction and data memories that the microcontroller will execute from. Ultimately, both the ARC microcontroller and the APB interface can see all of the PHY CSR registers and all of the ICCM and DCCM microcontroller memory space as a contiguous address space.

Figure 7-3 shows the block diagram of this embedded ARCv2 EM4 microcontroller. The red arrow shows the command path for ARCv2 CSR accesses while the blue arrow shows the command path for an SOC host on APB loading a program into ICCM and DCCM memory. The purple arrow shows the APB can issue commands for CSR access as well.

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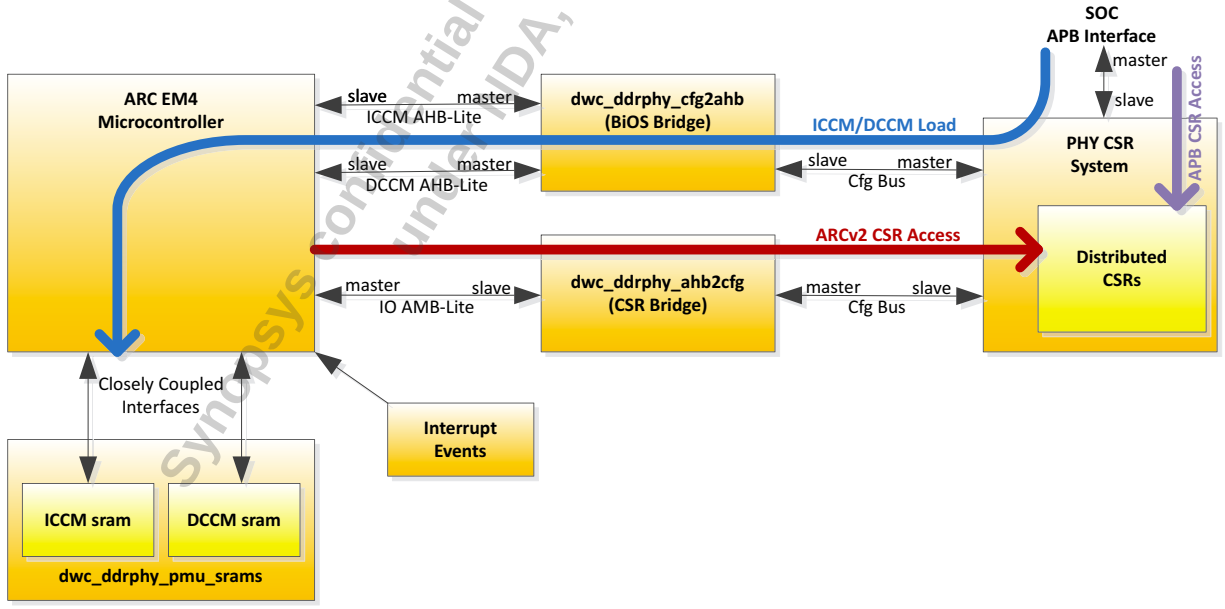
Figure 7-3 Embedded ARCv2 EM4



7.8.1 ARCv2 EM4 Features

The microcontroller is generated with the following basic features:

- ICCM instruction closely-coupled memory populated to 32k bytes
- DCCM data closely-coupled memory populated to 16k bytes
- An IO port with AHB-Lite interface mapping PHY CSRs into microcontroller memory space
- A pair of AHB-Lite interfaces for ICCM and DCCM initialization of the training C application
- Little Endian memory orientation

7.8.2 Mapping of ICCM and DCCM in CSR Address Spaces

Table 7-2 Mapping of ICCM and DCCM in CSR Address Spaces

Memory Type	PHY CSR Address (16-bit word)
ICCM	0x50000 (32kB)
DCCM	0x54000 (16kB)

7.8.3 ICCM and DCCM program loading

The blue arrow in Figure 7-3 on page 170 shows the path an SOC host uses to load a program into ARCv2 ICCM and DCCM closely-coupled memories. Writes and reads of ICCM and DCCM on this path are supported only when ARCv2 is stalled. Stall can be applied by writing the StallToMicro bit in the MicroReset register to one at any time, and released into the run state by writing it back to zero.

If a new program is loaded, ARCv2 can also be reset through the ResetToMicro bit in the MicroReset register to force program execution to start from the beginning.

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7.9 SRAM Interface

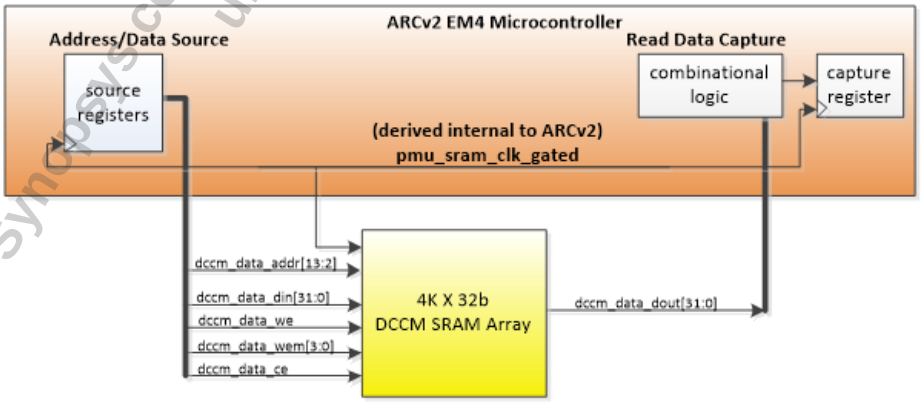
The ARCv2 microcontroller uses two closely coupled SRAM arrays called DCCM and ICCM for storage of program data and instructions. The microcontroller accesses the DCCM and ICCM simultaneously over separate interfaces. To support the training application, the array sizes must be 8K x 32b (32K bytes) for the ICCM array, and 4K x 32b (16 KB) for the DCCM array.

The intended primary use of SRAM is to support the initial training operation during boot. The SRAM is not used during normal DRAM transactional operation and not critical to PHY operation once trained. In the unlikely event of SRAM corruption, link training indicates a fail which results in increased training time, an outcome inconsequential for proper operation of the interface. For this reason, in order to ensure timing closure, and to minimize area required for SRAM, the ARC Microcontroller SRAM is recommended to not include ECC. For systems where it is believed that an extremely heightened level of SRAM fidelity is required, the recommended procedure during Firmware operation is to: write Firmware into SRAM, read Firmware from SRAM and compare to ensure correct as programmed, execute Firmware, read Firmware from SRAM to compare again to ensure correct as programmed, then proceed with operation. For almost all systems, this is not expected to be required.

For the purposes of timing closure, the ARC Microcontroller SRAMs should be hardened together with the PUB, or abutted directly up against the hardened PUB. For best results, hardening the SRAMs in with the PUB is recommended. This allows for best placement and timing closure. When reviewing initial SRAM choices, a Clock-to-Q of less than one-third of the minimum required DfiClk cycle is a recommended starting point. As the physical design development progresses, and a better understanding of overall device performance and timing is obtained, additional trade-offs may be made in the SRAM selection to best suit the users overall system, while still meeting overall SRAM to PUB timing requirements.

The two memory arrays must byte-writeable, fully synchronous designs. Each can be implemented as a single memory instance, or built from multiple memory instances. The memories must retain their output values when chip select is not asserted. You must add latches if your memories change their outputs to the X or Z state when chip select is not asserted. Note that after address is applied, the PHY expects valid data in the next clock cycle.

Figure 7-4 Example Implementation of 16kB DCCM



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The ARCv2 EM4 microcontroller design is provided with a behavioral model of the ICCM and DCCM closely-coupled memories. Simulation on the behavioral model can be started immediately before the actual ICCM and DCCM arrays are constructed. Using the behavioral model establishes working tests in simulation to build confidence for simulations with the memory-based array design.

Table 7-3 ICCM and DCCM Interface Signals

Port Name	Direction	Description	Clock
ICCM Array			
iccm_data_addr[14:2]	output	Instruction memory address	DfiClk
iccm_data_ce	output	Instruction memory chip enable	DfiClk
iccm_data_din[31:0]	output	Instruction memory write data to SRAM	DfiClk
iccm_data_dout[31:0]	input	Instruction memory read data from SRAM	DfiClk
iccm_data_we	output	Instruction memory write enable	DfiClk
iccm_data_wem[3:0]	output	Instruction memory write enable mask	DfiClk
DCCM Array			
dccm_data_addr[14:2]	output	Data memory address	DfiClk
dccm_data_ce	output	Data memory chip nable	DfiClk
dccm_data_din[31:0]	output	Data memory write data to SRAM	DfiClk
dccm_data_dout[31:0]	input	Data Memory Read Data from SRAM	DfiClk
dccm_data_we	output	Data memory write enable	DfiClk
dccm_data_wem[3:0]	output	Data memory write enable mask	DfiClk
Clocking			
pmu_sram_clk_gated	output	Clock from microcontroller to SRAM (gates off when processor is in Halt mode)	DfiClk

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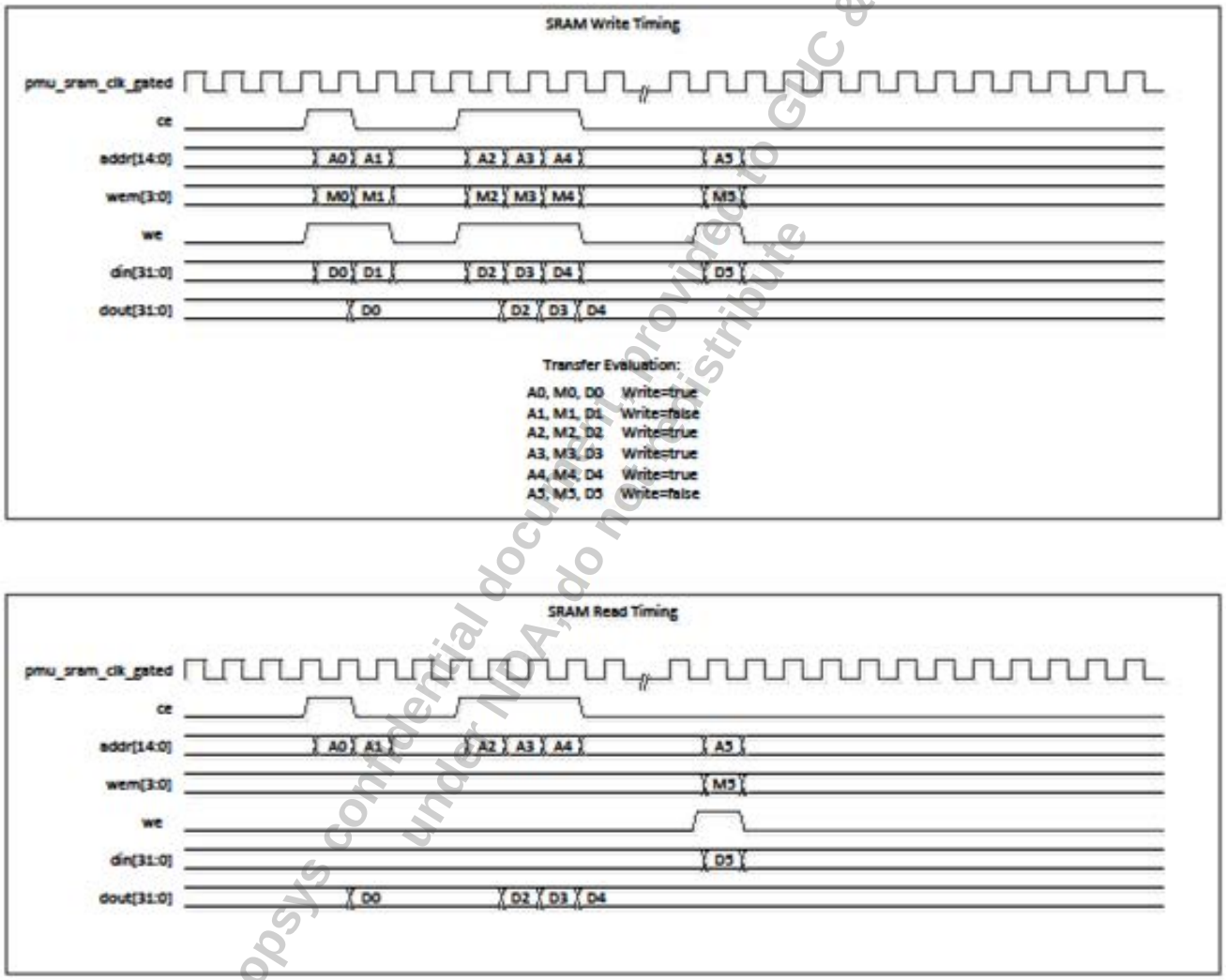
The write and read timing for these two interfaces is the same and is shown in Figure 7-5 on page 174. In the write timing diagram, writes can only happen when ce and we are high. The dout read data bus updates for A0, and A2 through A4, following the clock's rising edge.

In the read timing diagram, the write enable, we, does not assert for addresses A0 through A4. For every cycle where ce asserts, we get read data at the read path mux output in the following clock cycle. With no write enable present, these are true read cycles where the processor expects data to be available on the next clock cycle.

The following figure shows the SRAM write and read timing diagrams.

Note In Figure 7-5 on page 174, all signals should be viewed in relation to the rising clock edge.

Figure 7-5 SRAM Write and Read Timing Diagrams



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7.10 Shared AC

A Shared AC configuration (shared Address Command) refers to the specific external connections between the PHY and SDRAM memories that enables subsets of the DBYTEs to operate independently allowing for largely independent dual channel connections and operations on the DFI.

7.10.1 Memory Connections

To enable Shared AC, the memory channel is routed as follows:

- All ranks share the same address/command/bank/bank group/par signals
- Each rank[i] (defined by an independent MEMCLK,CS_N[i],CKE[i], ODT[i] signal connect) connects to a subset of the PHY DBYTEs

When configured for Shared AC operation the memory typically operates in 1T mode rather than 2T mode. Special care must be taken to ensure proper command and address routing to enable high speed 1T operation.

7.10.2 DFI Connections

The PUB and PHY are compliant to the DFI specification (see "Compatible Standards" on page 29). In compliance with the DFI standard, each DBYTE has fully independent dfi_wrdata and dfi_rddata interfaces, and can support accesses to partially populated ranks.

The most common configuration for a Shared AC system is using a 1:2 DFI frequency ratio. This allows the use of the phasing signals for the command and address information on the DFI interface and allows for the DRAMs to be able to receive commands on every other memory clock.

The common configuration uses two separate DFI compliant memory controllers.

One controller drives:

- dfi_cs[0], dfi_cke[0] and dfi_odt[0] (asserting CS only on phase 0)
- The phase 0 address and control signals
- Half of the DBYTEs read data and write data interfaces

The second controller drives:

- dfi_cs[1], dfi_cke[1] and dfi_odt[1] (asserting CS only on phase 1)
- The phase 1 address and control signals
- The remaining half of the DBYTEs read data and write data interfaces.

The common configuration typically assigns each channel ½ of data interface such that the channels are the same size. However, it is possible to have the channels assigned differing data widths as each DBYTE is fully self-contained and can be used by either channel – but this is not the common model for a Shared AC system.

The PHY only has a single DFI low power interface. If the user wishes to take advantage of the DFI low power interface there will need to be some coordination outside the PHY to ensure that when a DFI low power request is initiated both channels are in the proper state to take action. The same is true for the DFI controller update and DFI PHY update interfaces – there is only one of each, so care must be taken if using two controllers to coordinate properly.

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7.10.3 Restrictions

The Shared AC configuration is only an option when supporting DDR4 devices – it is not an option for supporting LPDDR4 devices.

The two channels must occupy either chip select 0 and chip select 1 or the two channels must occupy chip select 2 and chip select 3 (if you have four chip selects available). It is also acceptable for one channel to occupy a chip select from [0,1] and one from [2,3] and the other channel to occupy the remaining two chip selects. Table 7-4 shows legal channel assignments.

Table 7-4 Legal Options

Chip Select 0	Chip Select 1	Chip Select 2	Chip Select 3
Channel 0	Channel 1	NC	NC
Channel 0	Channel 1	Channel 0	Channel 1

Table 7-5 shows the illegal channel assignments.

Table 7-5 Illegal Options (not exhaustive)

Chip Select 0	Chip Select 1	Chip Select 2	Chip Select 3
Channel 0	NC	-	-
Channel 1	NC	-	-
NC	Channel 0	-	-
NC	Channel 1	-	-
Channel 0	Channel 0	-	-
Channel 1	Channel 1	-	-

No matter how many DBYTEs are assigned to occupy each channel, it is required that across two adjacent channels all DBYTEs must be populated.

User must set the PartialRank bit in the MsgMisc register of the message block header to 0x1 to indicate that the PHY is being used in the Shared-AC configuration.

7.10.4 Training

The restrictions for a Shared AC configuration exist due to the way the PHY trains the memory interface. Even though there are functionally two channels in the Shared AC configuration, the PHY trains the interface as though it were still operating in a single channel configuration. The PHY combines chip selects 0 and 1, treating them as a single logical chip select for training. If chip selects 2 and 3 are present, the same will apply to them.

7.10.5 Example

Figure 7-6 shows an example using a 32-bit PHY in Shared AC configuration with two 16-bit channels. Rank0 is connected to the shared address and command interface (act_n, address, bank, bg, cas, ras, we_n, par), Rank[0] specific signals (cs_n[0], cke[0], odt[0]) and the lower two logically numbered DBYTEs

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(DBYTE[1:0]). Rank1 is connected to the shared address and command interface (act_n, address, bank, bg, cas, ras, we_n, par), Rank]1] specific signals (cs_n[1], cke[1], odt[1]) and the higher two logically numbered DBYTEs (DBYTE[3:2]).

Using this configuration, independent read/write transactions can be performed to RANK0 and RANK1 simultaneously, assuming correct scheduling of the transactions by a DFI compliant memory controller (or two DFI compliant memory controllers time-multiplexing the DFI control bus)."

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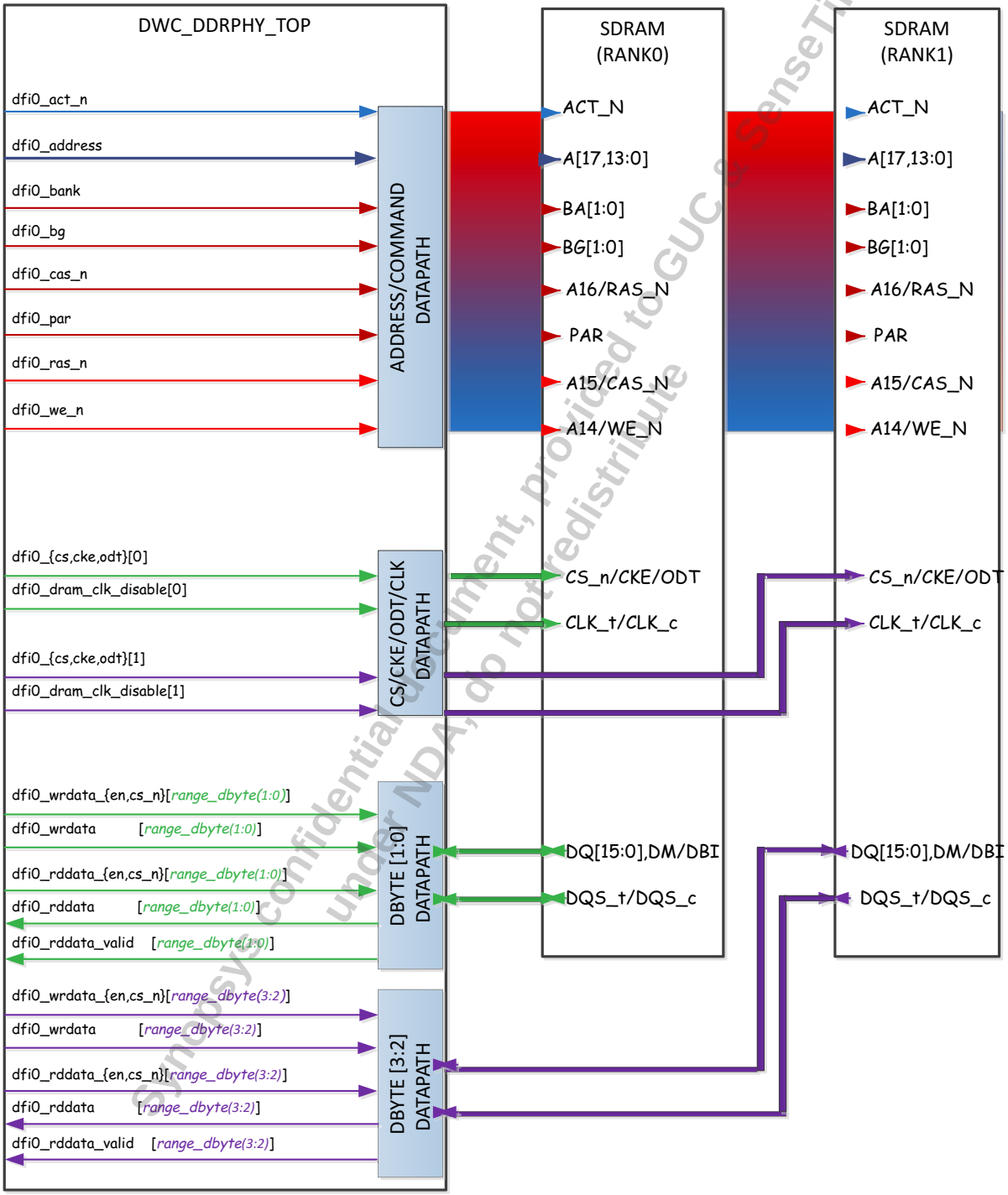
Figure 7-6 Shared AC Example of a 32-bit PHY Connected to Two Ranks in a Dual 16-bit Channel Configuration



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8
System Integration

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This section provides information for integrating the DDR PHY with either the Synopsys DesignWare Cores Protocol or Memory Controllers or a non-Synopsys memory controller. Depending on the user design and implementation methodology, the top-level PHY Verilog module (DDRPHY_top) can be instantiated in the chip logic. This top-level PHY Verilog includes the instantiation of all PHY hard and soft IP blocks and therefore greatly simplifies the connectivity of the DDR PHY IP to the user logic.

If the user design methodology and implementation does not allow for the instantiation of the top-level PHY Verilog module, then the two PHY components can be instantiated separately. The PHY soft IP is the PUB, while all PHY hard macros are grouped together under the DDRPHY hierarchy.

This chapter describes the integration when using either method.

This chapter describes the following:

- "DDR PHY Top Level (DDRPHY_TOP)" on page 180
- "Clocking and Timing" on page 184

8.1 DDR PHY Top Level (DDRPHY_TOP)

8.1.1 Verilog Parameter Configuration

The following `define values are provided as part of the RTL release to customers in the dwc_ddrphy_{config}_VDEFINES.v file. The {config} is determined by the example testbench and customers desired configuration. For example, for a dual-DFI-channel, 24 Address/Command bits (6 nibbles), 32 DQ lanes (4 data bytes), the defines name is dwc_ddrphy_ac6d4ch2_VDEFINES.v.

Caution Do not set any `defines unless they are explicitly documented in this databook.

The contents of the defines are modifiable, with some restrictions, by the customer, with recommended values provided as a unit in several example VDEFINES.v files. The list of defines, and description, follows:

- `define DWC_DDRPHY_NUM_ANIBS_{n}
  - Example for 24-bit (6 nibble) address/command: `define DWC_DDRPHY_NUM_ANIBS_6

Note Customers must define one and only one of: DWC_DDRPHY_NUM_ANIBS_3, DWC_DDRPHY_NUM_ANIBS_6, DWC_DDRPHY_NUM_ANIBS_10, DWC_DDRPHY_NUM_ANIBS12

The DWC_DDRPHY_NUM_ANIBS_{n} defines cause the RTL to compile to a PHY with exactly {n} ACX4 instances. In most cases, customers choose the number of ACX4 based on their DRAM technology support needs. Always consult with Synopsys for questions on configurations.

- `define DWC_DDRPHY_NUM_DBYTES_{m}
  - Example for 32-bit (4 data byte): `define DWC_DDRPHY_NUM_DBYTES_4

Note Customers must define one and only one of DWC_DDRPHY_NUM_DBYTES_{2..10} for their PHY implementation.

- `define DWC_DDRPHY_DFI1_EXISTS

Note Customers wishing to have a second DFI channel must define this. Customers with only single channel needs should not define this. Customers who wish single-channel support from dual-channel RTL can configure their PHY through software, and optionally through tying off ports, in a single-channel configuration.

The above defines are intended to work as a group. Please consult with Synopsys on the support for any desired configuration.

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8.1.1.1 Customer Defines

Other defines available to customer and provided in example testbench:

- `define DWC_DDRPHY_NUM_TOP_SCAN_CHAINS {s}

  DWC_DDRPHY_NUM_TOP_SCAN_CHAINS is provided as the sum of the number of scan chains within the embedded hard IP blocks (ACX4, DBYTE, MASTER) for a given PHY configuration. This is based on values of `DWC_DDRPHY_NUM_ANIBS_{n} and `DWC_DDRPHY_NUM_DBYTES_{m}, as described above. The scan ports are provided as a bundle to the PHY top-level Verilog wrapper, and they can be considered a suggestion dependent on customer balancing and assignment of scan chains in the customer's implementation.

- `define DWC_DDRPHY_CUST_PHYREV 5'b00000

  DWC_DDRPHY_CUST_PHYREV is provided as a convenience for customers, allowing control of the CUSTPHYREV CSR read-only value. Customers may override this for their application of the PHY. The define only affects the content of the CUSTPHYREV CSR when it is read; it has no other effect on PHY RTL or Firmware.

- `define DWC_DDRPHY_CUST_PUBREV 5'b00000

  DWC_DDRPHY_CUST_PUBREV is provided as a convenience for customers, allowing control of the CUSTPUBREV CSR read-only value. Customers may override this for their application of the PHY. The define only affects the content of the CUSTPHYREV CSR when it is read; it has no other effect on PHY RTL or Firmware.

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8.1.1.2 Additional/Optional Customer Defines

8.1.1.2.1 DWC_DDRPHY_VDDQLP_SUPPORT

When DWC_DDRPHY_PG_PINS is defined, the user must define DWC_DDRPHY_VDDLP_SUPPORT as well. This will define VDDQLP ports.

8.1.1.2.2 DWC_DDRPHY_PG_PINS Define

The DWC_DDRPHY_PG_PINS define dds the VDD, VSS, VDDQ, VDDQLP, and VAA ports to top-level and the wiring down through into the hard macros:

In simulation, this define may be provided by customers to drive the logical 0/1 VDD, VSS, VDDQ, VDDQLP,and VAA values via ports on their PHY instance. It may optionally be used for physical purposes (for example, synthesis) in a flow that requires power and ground pins to be visible as top-level ports. In general, follow the Integration Guide directions for physical flow configuration.

If the above DWC_DDRPHY_PG_PINS is *not* defined, the default behavior of the RTL is that a customer uses a upf file/flow to drive hard-macro power/ground pins during simulation.

8.1.1.2.3 DWC_DDRPHY_NO_PG_PINS_MACROS Define

If, instead, the customer wishes to not use upf for simulation, then the DWC_DDRPHY_NO_PG_PINS_MACROS define provides static logic 0/1 values to the various power/ground nets inside the hard macro Verilog as appropriate.

In simulation this provides static tie-off to logical 0/1 values, and no top-level power ports or wiring is added through the top into the hard macros.

Because of certain voltage-sensing circuit modeling inherent in parts of the hard macros, these tie-offs will not reflect any true voltage rail values. So, for example, in an ultra-low power state without data transfer, VDD and VAA may in a system be lowered to non-operational values. However in this simulation mode, the hard macro VDD and VAA wires will remain at logic 1.

Caution If DWC_DDRPHY_NO_PG_PINS_MACROS is defined, at no time in the simulation can PwrOkIn be driven to an unknown state.

8.1.1.2.4 DWC_DDRPHY_PIPE_DFI_* Defines

Pipeline staging flops can be placed at the front end of the DFI interface, between the memory controller and the PHY. To do so, set the following defines to a value of 1, 2, or 3, according to the number of pipeline stages desired. If no pipeline stages are needed, leave these values undefined.

- DWC_DDRPHY_PIPE_DFI_WR -- The number of pipeline stages desired on all dfi_wrdata* signals.
- DWC_DDRPHY_PIPE_DFI_RD -- The number of pipeline stages desired on all dfi_rddata* signals.
- DWC_DDRPHY_PIPE_DFI_MISC -- The number of pipeline stages desired on all other DFI interface signals.

Note DWC_DDRPHY_PIPE_DFI_MISC must have a value that is equal to or greater than both DWC_DDRPHY_PIPE_DFI_WR and DWC_DDRPHY_PIPE_DFI_RD.

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8.1.1.2.5 DWC_DDRPHY_LBIST_EN - Enables Logic BIST

This define enables logic BIST.

8.1.1.2.6 DWC_DDRPHY_FIXED_DFICTLCLK_RATIO

When this is defined, the PHY can more easily interface to a memory controller where the only DfiCtlClk:MEMCLK clock ratio is 1:2. (DfiCtlClk == DfiClk). The logic that supports a 1:4 ratio is removed, and writing csrDfiFreqRatio has no effect.

When this is defined, the following files are unused:

- dwc_ddrphy_pub_serdes.v dwc_ddrphy_serdes_ctl2pub.v
- dwc_ddrphy_serdes_pub2ctl.v dwc_ddrphy_serdes_c2pcell.v
- dwc_ddrphy_serdes_p2ccell.v dwc_ddrphy_serdes_sb.v

There are also Spyglass waivers (see bottom of file) that can be omitted when this is NOT defined.

8.1.1.2.7 DWC_DDRPHY_REMOTE_IMP_CAL

This define enables remote impedance calibration. When defined, the PHY includes logic to support remote impedance calibration. Using this option, two PHYs can share calibration codes where one PHY, acting as a master, pushes its calibration codes to another PHY acting as a slave.

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8.1.2 Cautionary Notes on Simulations

The PHY is a highly configurable product with many internally configurable parameters. The following guidance must be followed to ensure proper operation in simulation:

- The "pvtscale" parameters must never be adjusted or changed

8.2 Clocking and Timing

8.2.1 Normal PLL Mode (PLL Locked)

In the PLL lock mode (also referred to as mission mode) the internal PHY clock Pclk is four times the frequency of the DfiClk. Refer to the PHY databook for optimal PLL settings and detailed timing waveforms for the different PHY modes.

8.2.2 PLL Bypass Mode

PLL Bypass Mode must be enabled in mission mode for data rates below 667 MT/s. In mission mode, for data rates between 667 MT/s and 1066 MT/s it is possible to enable PLL Bypass mode. Data rates above 1066 MT/s do not support PLL Bypass Mode.

A clock must be supplied on the BypassPclk input when operating in PLL Bypass Mode (see "BypassPclk" on page 127).

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8.3 Delay Cell Parametric Characterization and Test

8.3.1 Overview

There are two types of delay cells in the DBYTE and ACX macros:

- LCDL ("local calibrated delay line") which are used to achieve fractional UI timing of the DRAM interface signals
- BDL ("bit delay line") which are used for deskewing read DQ/DBI signals.

The PUB provides support for testing these delay cells so that they can be known to be working correctly for training timing and for locking to the PLL-generated pclk and tracking pclk.

8.3.2 LCDL

Each DBYTE macro has sixteen LCDL, ten for write DQS and DQ/DM/DBI, and six for timing the gate for read DQS and for delaying the DQS edges to generate read-strobes.

Each ACX macro has two LCDL: one LCDL (instance TXDLL) for timing its four output signal lanes and a second LCDL (instance MDLL) which may be used for tracking circuit timing variations due to temperature and voltage changes.

Each LCDL has its own dedicated logic for locking to pclk and tracking pclk.

The delay provided by an LCDL consists of two parts:

1. A non-configurable delay that we call "zerodelay" (also known as “insertion delay”)
2. A configurable delay that we call "Phase[8:0]" on the LCDL wrappers and "dly_sel" on the LCDL/BDL cell, and that is a multiplier on the “stepsize” time.

The total delay is given by: LCDL_delay = (dly_sel[8:0] * stepsize) + zerodelay;

Supporting the LCDL are CSRs whose “fine delay” (fractional UI) are denominated in units of 1/32 UI. These are the fine-delay fields of CSRs ATxDly, TxDqDly, TxDqsDly, RxEnDly, RxClkDly. These delays, specified in units of 1/32 UI, are converted into the native control Phase[8:0] by multiplying by the number of phase units per 1UI in effect at the time of the memory operation. This factor is per LCDL instance and varies with voltage and temperature.

8.3.3 BDL

Each DBYTE macro has nine BDL used for deskewing the nine read DQ[7:0], DBI signals relative to the strobe generated from the read DQS.

The total delay is given by: BDL_delay = (dly_sel[5:0] * stepsize) + zerodelay

Unlike the LCDL, the BDL are uncalibrated. The configurable delay is csrRxPBDly which is in native Phase/dly_sel units (ie not 1/32 UI units).

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8.3.4 Delay-Test Hardware in the PUB

In the PUB, there is one copy of delay-test hardware for all of the ACX macros and one copy per DBYTE.

Each copy of the delay-test hardware consists of the following components:

- 16b up-counter clocked by the ring-oscillator
- Inverter (to make it oscillate)
- Mux for the delay-cell outputs (which allows having just one ring-oscillator counter)
- Drives for the inputs to the delay-cells

The PUB delay test hardware has an additional element that controls the runtime of the delay tests:

- 16b down-counter clocked by DfiClk (which controls how long the ring counter is enabled).

While this counter is non-zero, the ring-oscillators are allowed to run. The initial value is set from a control csr DlyTestCntDfiClkIV[15:0].

There is a synchronizer in the ring-oscillator domain used to stop the oscillator - which adds some variability in the count (see Figure 8-1 and Figure 8-2).

The interface between any delay-cell (in DBYTE macros or in the ACX macros) and the PUB consists of a delay-cell output, a delay-cell input and a delay-test enable per delay-cell.

The delay in the ring consists of the delay cell and the mux+demux+routing delays.

Figure 8-1 AC Delay Cell Test Hardware

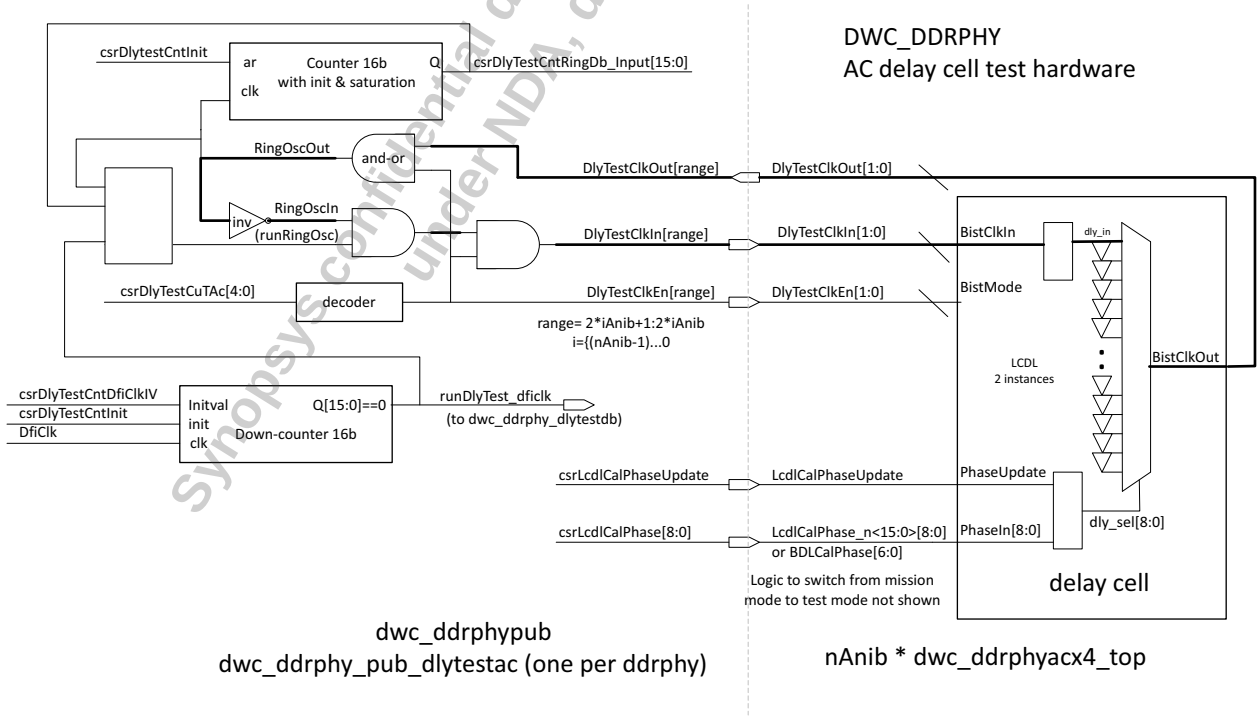

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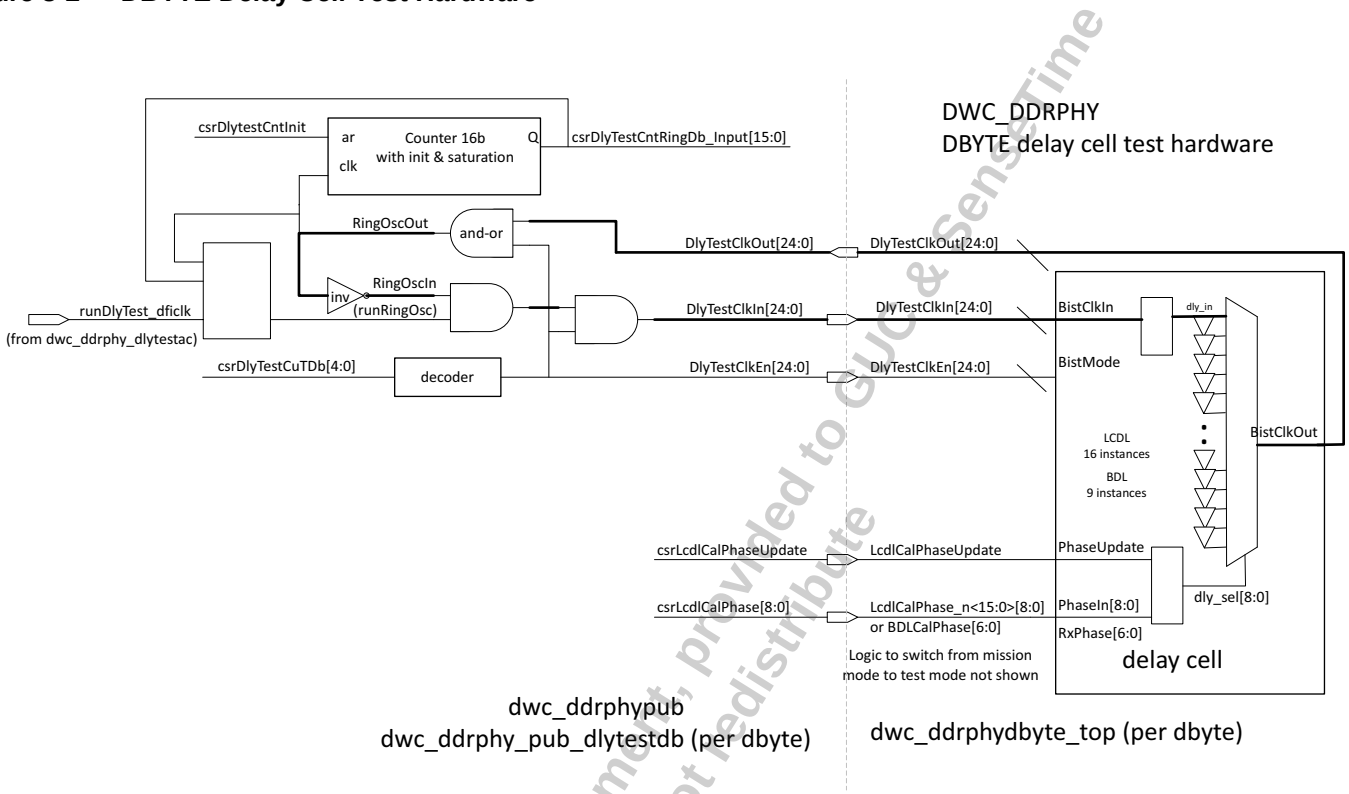
Figure 8-2 DBYTE Delay Cell Test Hardware



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8.3.5 Delay Test CSRs

Table 8-1 Delay Test Registers

Register	Description
DlyTestEn	Enables the connections for the ring-oscillator in the delay macros
DlyTestCntInit	Initializes CntRingOscDb/Ac (to zero) and the CntDfiClk to CntDfiClkIV
LcdlCalPhase[8:0]	Becomes dly_sel[8:0] with pulse on LcdlCalPhaseUpdate
LcdlCalPhaseUpdate	Strobe to load LcdlCalPhase into dly_sel
DlyTestCuTDb[4:0]	"cell under test" selection among 25 delay elements in the dbytes
DlyTestCuTAc[4:0]	"cell under test" selection among 24 delay elements in the addr/cmd nibbles
DlyTestCntDfiClkIV[15:0]	DfiClk counter initial value
DlyTestCntDfiClk[15:0]	Counts down when nonzero, no rollover
DlyTestCntRingOscDb<$db> [15:0]	One counter per data byte
DlyTestCntRingOscAc[15:0]	One counter for all the addr/cmd

8.3.6 Procedure for Linearity Test

1. Measure the oscillator count value at the initial and terminal values that are specified by the user.
2. Use these values to calculate the predicted value of the delay at each phase.
3. Use these predicted delay values to calculate a predicted value of the oscillator counter at each phase.
4. Measure the oscillator counter at each user specified phase (start to end with the user specified stride).
5. Compare the measured oscillator count to the predicted using the following formulas:

   Low Limit = ((Predicted oscillator count) – ((LCDL pass %) * (Predicted oscillator count))

   High Limit = ((Predicted oscillator count) + ((LCDL pass %) * (Predicted oscillator count))

   Low Limit < (Measured oscillator count) < High Limit

   If testing all 512 values of Phase is too costly, then an engineering compromise for production unit test would be to stride the Phase by 17 (or some other number not a power of two). This causes each of the bits of the control Phase[8:0] to be 0 or 1 at some time to test for stuck-at faults.

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9
Design for Test

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Apart from the loopback test modes, there are various other PUB test modes that are used to facilitate the testing of various features of the PHY. These test modes include ATPG scan mode, delay line oscillator mode, and PLL test mode. The guidance provided in this chapter for silicon testing and characterization of Digital Delay Lines (DDLs) and Phase Locked Loops (PLLs) can be applied to either product characterization and/or production testing.

This chapter describes the following:

- "ATPG Test Mode" on page 190
- "Loopback BIST Mode" on page 191
- "Delay Element Testing" on page 194
- "Analog/Digital Test Observability" on page 198
- "Burn-in Recommendations" on page 205
- "Bypass Mode" on page 205
- "I/O Cell DC Parametric Characterization" on page 210
- "VDDQ or VDDLP Quiescent Current Measurement" on page 225
- "Input Pin Leakage Measurement" on page 226

9.1 ATPG Test Mode

To enter ATPG Test Mode, set the atpg_mode input pin to 1.

All possible registers in the PHY blocks are put on scan chains. Each scan chain is based on an internal functional clock group with no mixing of clock edges. Different functional clocks, which have the same edge and have their clock trees functionally balanced, are treated as one clock group. All scan chains have lockup latches at their outputs.

There is a separate scan enable (atpg_se[*]) for each clock domain, even when that domain is local to sub-logic in the tile. Scan pins are intentionally left open in the RTL. The atpg_si and atpg_so (scan in/out) are treated as ports at the top-level for all the hard IP instances.

Chip scan insertion is not done in RTL. It is done in implementation. The scan-insertion tools for the hard-IP will create the scan chains for those hard IP in the gate-level netlist, but not in the RTL. For the PUB, the customer should add the scan insertion and stitching.

Each scan chain has a maximum length of 100 registers. Scan chains belonging to the same group or clocked by the same edge of the clock may be concatenated externally, to build up longer, balanced chains, if required. Since all scan chains use a positive clock edge, it is possible to concatenate all the chains together.

Two additional features are generally implemented internally to increase test pattern coverage without additional effort or actions:

- Reset inputs of infrequently used asynchronous flops are forced off during scan test (using atpg_mode).
- Clock gaters are forced on during test clock strobing (using atpg_se).

Note In ATPG Mode (atpg_mode input pin == 1), all IO drivers are forced to maximum drive strength.

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9.2 Loopback BIST Mode

The PHY contains features to support loopback testing functionality. Once placed in loopback mode, stimulus patterns may be either generated by the core, or by utilizing a Firmware image to activate the hardware training state machines. The recommended procedure for loopback is as follows:

- Follow the PHY Initialization procedure to bring up VDD, VDDA, VDDQ, and VDDQLP ("PHY Initialization" on page 132)
- Follow the PHY initialization procedure to Start Clocks and Reset the PHY ("PHY Initialization" on page 132)
- Load the microcontroller memory with the Loopback BIST firmware
- Lock the DfiClk to the desired Loopback Frequency
- Execute the Loopback BIST Firmware:
  - Initialize the Firmware Message Block with the required test parameters. The content to be written is test dependent, so the documentation provided with each firmware BIST image should be consulted.
  - Enable microcontroller access to the internal CSRs by setting the MicroContMuxSel CSR to 1. This allows the microcontroller unrestricted access to the configuration CSRs. For more information on this CSR see "Register Description" on page 103.
  - Begin execution of the firmware by setting the MicroReset CSR to 4'b0000.
  - Poll mailbox until the microcontroller signals loopback completed
  - Enable external access to the internal CSRs by setting the MicroContMuxSel CSR to 0. This allows the external APB interface unrestricted access to the configuration CSRs. For more information on this CSR, see "Register Description" on page 103.
  - Read the Firmware Message Block to obtain the results from the Loopback BIST

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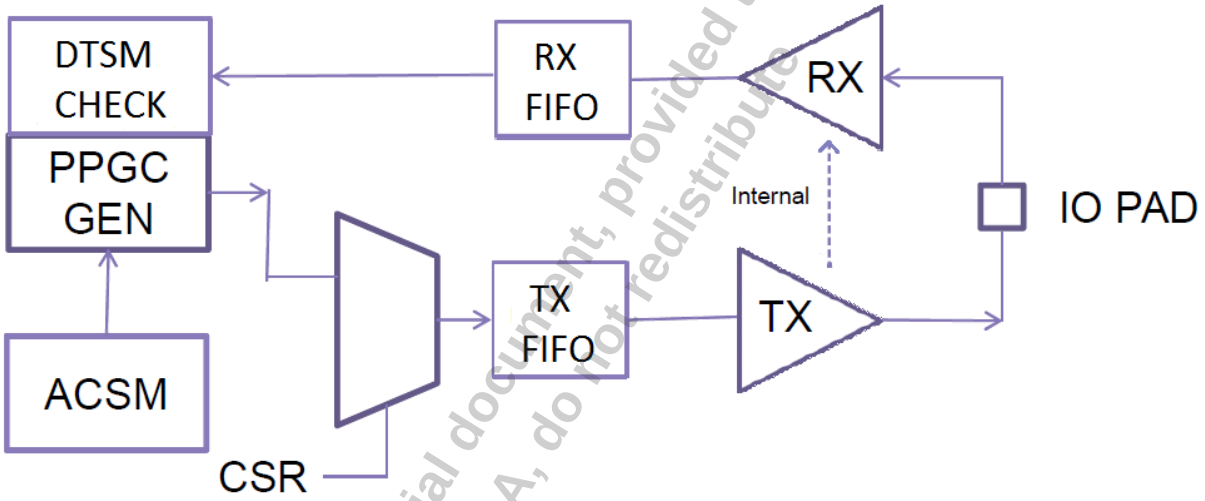
Data signals are optionally looped back internally or at the at the I/O pad. If I/O pad loopback is selected, it is important that these points are correctly externally terminated. Data byte DQ/DM and DQS lanes are loop backed to their respective receivers. Address/command lanes contain dedicated built-in loopback logic. A PRB7 generator and self-synchronizing checkers are implemented for this purpose, along with dedicated test receivers.

A typical Data PHY loopback configuration sequence utilizing the hardware training state machines is shown in the following figure.

Note The following example is for information only. The loopback BIST firmware executes the sequence once loaded and activated.

Figure 9-1 AC Loopback



The portion of the Firmware dedicated to Loopback BIST performs the following functions

- The PPGC is configured to supply a test pattern. In the case of data loopback, a pre-configured PRBS23 or PRBS16 can be selected as the stimulus.
- The test mode configuration registers are configured for data loopback.
- The Tx and Rx delay are set s accordingly
- DTSM configured to check for errors
- ACSM configured to perform a sequence of multiple writes.
- ACSM loopback mode enabled.
- Initiate ACSM run sequence.
- On completion, check the accumulated error counter for each lane.

A typical Address/Command PHY loopback configuration sequence is a follows.

Note The following example is for information only. The Loopback BIST Firmware executes the sequence once loaded and activated.

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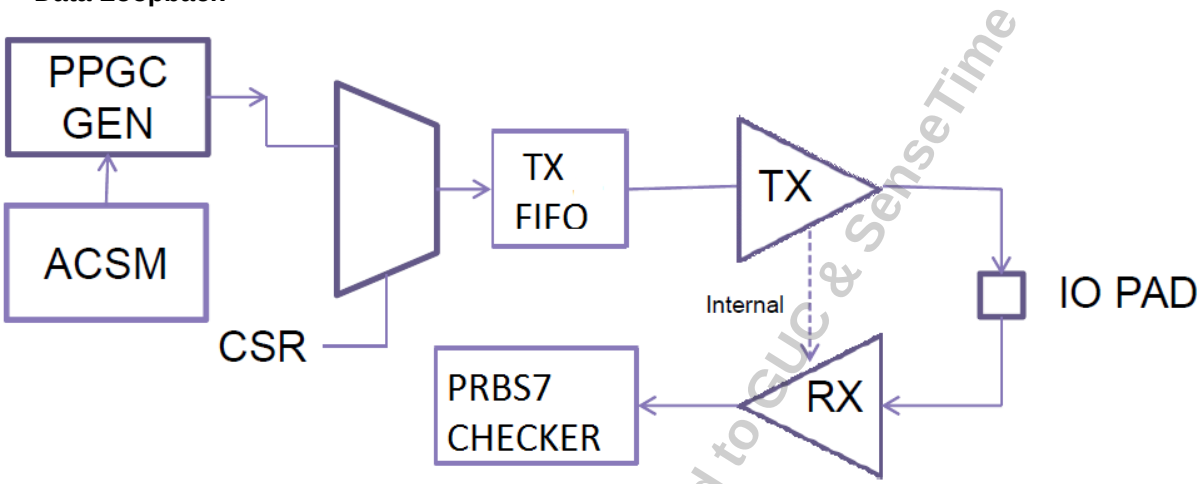
Figure 9-2 Data Loopback



- ACSM configured to perform multiple writes to advance PPGC.
- ACSM Enabled for either half rate or full rate AC PRBS mode.
- Initiate ACSM run sequence.
- On completion, check the error counter for each lane.

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9.3 Delay Element Testing

There is a facility for testing the delay macros for linearity of delay time with changes in delay configuration.

There are two types of delay elements in the design:

1. LCDL used for address/command lane delay, write DQ/DQS delay, RxEn delay, and RxClkDly. (Read LCDL as “local calibrated delay line”. LCDLs are also sometimes called DLLs or DDLs.)
2. BDL used for read DQ delay. (Read BDL as “bit delay line”. BDLs are uncalibrated.) Each DQ/DBI lane has a BDL. The maximum delay BDLs can provide is one-eighth the maximum delay of the LCDLs.

An important property of this test logic is that “pclk”, the SDR UI-period clock generated by the PLL, is not used (that is, the PLL does not need to be locked). The only clock required is the input DfiClk which is used as the PHY's csr clock. Conceivably, a brief LCDL linearity test could be run during PLL locking.

The delay provided by an LCDL consists of two parts:

1. A non-configurable (that is, unavoidable) delay that we call "insertion_delay" or "zerodelay" and
2. A configurable delay that we call "Phase[8:0]" on the LCDL wrappers and "dly_sel" on the LCDL/BDL macro.

The total delay is given by:

- LCDL_delay = (dly_sel[8:0] * stepsize) + zerodelay
- BDL_delay = (dly_sel[5:0] * stepsize) + zerodelay

  where the LCLD/BDL time constants zerodelay and stepsize are technology dependent, and vary with instance, process, temperature, and voltage.

Note The units of dly_sel as being "bufs" (or buffers) are used even though it is not exactly how the LCDL is designed.Units of stepsize are ps/buf when doing measurement unit conversion between dly_sel and register{TxDq,TxDqs,RxEn,RxClk}Dly which are denominated in integer/fractional UI.

Single-delay macros are tested with the following counters:

1. One down-counter clocked by DfiClk to provide an absolute time scale (readable as Register DlyTestCntDfiClk), and
2. A second up-counter clocked by a ring oscillator (RO) comprised of one delay element (cell under test) and an inverter.

The RO counter is readable from register DlyTestCntRingOsc{Db<$db>/Ac}[15:0]. The period of the SDR RO clock is 2*LCDL_delay.

The test might fail because of a design problem of the LCDL, or an individual instance might fail because of a "stuck-at", short, or open-circuit fault of dly_sel or other control signals.

The objective of the linearity test is to show that the delay of the delay cells, and hence the period of the ring-oscillator (Tro) is linear with the dly_sel (RegisterLcdlCalPhase[8:0]):

- Tro = a * dly_sel + b;

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The runtime for testing a single step is:

- runtime = Register DlyTestCntDfiClkIV * Tdficlk = Register DlyTestCntRingOsc * Tro;

or, solving for Tro

- Tro = Register DlyTestCntDfiClkIV * Tdficlk / Register DlyTestCntRingOsc;

By commutivity

- a * dly_sel + b = Register DlyTestCntDfiClkIV * Tdficlk / Register DlyTestCntRingOsc;

Now solve for a and b. An alternative is to calculate the difference step-by-step shown below.

One iteration of the test (ie "the inner loop") consists of the following:

- The dly_sel value is configured with dly_sel_i, by writing Register LcdlCalPhase[8:0]=i and pulsing Register LcdlCalPhaseUpdate.
- The RO up-counter is zeroed and the DfiClk down-counter is loaded with initial value Register DlyTestCntDfiClkIV[15:0] by pulsing Register DlyTestCntInit.
- On the deassertion of Register DlyTestCntInit, the DfiClk down counter starts to count down.
- When Register DlyTestCntDfiClk[15:0] reaches zero the value of the RO counter DlyTestCntRingOsc{Db<$db>/Ac}[15:0]
- is read, and the first of two samples, DlyTestCntRingOsc_i[15:0], is acquired.
- Now repeat the above with dly_sel_j = dly_sel_i + 1 (or Register LcdlCalPhase[8:0]=i+1) to get a second sample,
- DlyTestCntRingOsc_j[15:0];

The difference in the RO counter terminal values is the unnormalized stepsize for that pair of dly_sel values.

The stepsize_i in ps units between dly_sel=i and dly_sel=j=i+1 may be calculated as:

- PeriodRO_i(ps) = (Register DlyTestCntDfiClkIV[15:0] * period(ps,DfiClk))/(Register DlyTestCntRingOsc_i[15:0])
- PeriodRO_j(ps) = (Register DlyTestCntDfiClkIV[15:0] * period(ps,DfiClk))/(Register DlyTestCntRingOsc_j[15:0])
- stepsize_ji = PeriodRO_j - PeriodRO_i

A complete test (for a single delay macro) would march through all 511 values of dly_sel_j[8:0] = [1...511].Each resulting stepsize_j must lay within a tolerance band, for the linearity test to pass.The accuracy of the measurement depends on the length of time that an iteration is allowed to run;larger values Register DlyTestCntDfiClkIV[15:0] will result in better accuracy and affects the tolerance band.

One idea for a "good enough" quick test is to sample only the ten values of dly_sel={0,1,2,4,8,16,...256}.Note that this test mechanism can be used to "calibrate" the BDL (or the LCDL for that matter), where "calibrate" means to find the dly_sel that causes a one-quarter UI delay for the BDL or a one UI delay for the LCDL, using the fact that the period of DfiClk is four UI. But there is a quicker way to do this calibration; see the related topic of LcdlCal.

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Since this test uses hardware that is not used by mission-mode operation, a RO counter is shared for the testing of a group of delay macros. Each data byte "mac" modules (dwc_ddrphydbyte_top.v) has 25 delay macros but is allocated only one RO counter. So a build with nine data bytes has nine RO counters.

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All of the delay macros in all of the address/command anib "mac" module (dwc_ddrphyacx4_top.v) share one RO counter; in a 12 anib build there are 24 delay macros. In 9-byte, 48-addr/cmd lanes build, there are 10 RO counters, and 10 delay macros can be tested in parallel. A complete test of such a build would require 25*511 iterations. The time to complete is proportional to Register DlyTestCntDfiClkIV[15:0].

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9.4 Analog/Digital Test Observability

9.4.1 Digital Observability

The PHY has the capability to send many of the internal important digital signals to output pins to aid with test and debug of the PHY. The number of digital test outputs varies based on the configuration of the PHY. The following table describes each configuration:

Table 9-1 Digital Observability Configurations

Define Used	Number of ANIB Instances	Primary Digital Observation Pin	Secondary Digital Observation Pin
DWC_DDRPHY_NUM_ANIBS_3	3	BP_ALERT_N	(Not Available)
DWC_DDRPHY_NUM_ANIBS_6	6	BP_ALERT_N	(Not Available)
DWC_DDRPHY_NUM_ANIBS_10	10	BP_A[19]	BP_ALERT_N
DWC_DDRPHY_NUM_ANIBS_12	12	BP_A[32]	BP_ALERT_N

The test output selection is built as multiple test selection muxes with all of the mux outputs OR'd together before being sent out to the pins. Each mux has a constant 1'b0 input tied to the 0 input of the mux. The MtestMuxSel CSR controls the selection value to each mux. Setting all the CSR's to 0 will cause all the muxes to select the 1'b0 to the test output, which would cause the test output to be set to a constant 0. Setting one of the mux selection CSRs to a non-zero value will allow that signal value to be sent to the test output. If all other CSR mux selector values are set to 0, then all the other muxes will send 0 which will not interfere with the value of the signal of interest. Therefore, the basic process is:

- Write all the MtestMuxSel CSRs to 0 to force them all to send the constant 0
- Write the one MtestMuxSel CSR that contains the signal to output to the value to select that signal.

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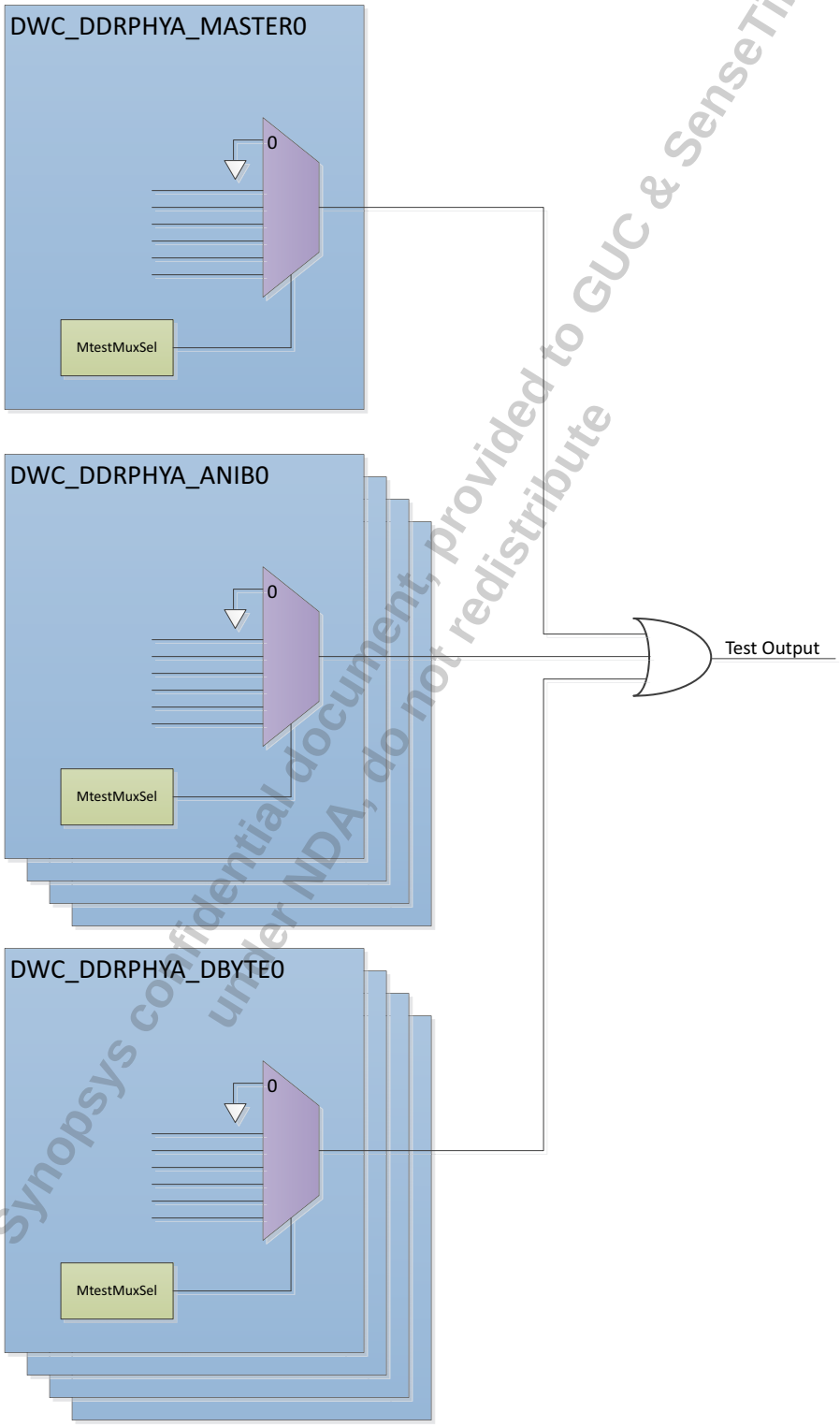
Figure 9-3 Overall Test Selection Structure



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9.4.1.1 Primary Digital Observation Pin

The value output on the Primary Digital Observation pin is controlled by the setting of the MtestMuxSel CSR. There is a copy of this CSR in each ANIB, DBYTE, and MASTER instance inside the PHY. To use the Primary Digital Observation Pins, use the following procedure:

- Setup: Power on and reset the PHY. The digital observation pins can be enabled at any point after the reset.
  - If using the digital observation pin before running training firmware, write the DWC_DDRPHYA_MASTER0_PorControl CSR to 0x1 after completing the reset.
- Step 1: Enable the primary digital output by writing DWC_DDRPHYA_MASTER0_TestBumpCntrl CSR:
  - For DWC_DDRPHY_NUM_ANIBS_3 / DWC_DDRPHY_NUM_ANIBS_6:
    Write DWC_DDRPHYA_MASTER0_TestBumpCntrl to 0x0203
    (ForceMtestOnAlert = 0x1, TestBumpDataSel = 0x00,
    TestBumpToggle = 0x0, TestBumpEn = 0x3).
  - For DWC_DDRPHY_NUM_ANIBS_10 / DWC_DDRPHY_NUM_ANIBS_12:
    Write DWC_DDRPHYA_MASTER0_TestBumpCntrl to 0x0007
    (ForceMtestOnAlert = 0x0, TestBumpDataSel = 0x00,
    TestBumpToggle = 0x1, TestBumpEn = 0x3).
- Step 2: Set all the selection muxes to select constant zero by writing 0x00 to all instances of:
  - DWC_DDRPHYA_ANIB<N>_ MtestMuxSel,
    DWC_DDRPHYA_DBYTE<N>_ MtestMuxSel,
    DWC_DDRPHYA_MASTER0_ MtestMuxSel
- Step 3: Write the MtestMuxSel CSR in a single instance to output the desired signal from a single instance of any one ANIB, DBYTE or MASTER. Selection values are detailed in following tables.

Only a single instance of a MtestMuxSel CSR can be non-zero at a time. To select a different value, repeat steps 2 and 3. The value to write to the MtestMuxSel CSR in Step 3 is based on the instance type that is being written. The following table describe the various signals that are available for output on the Primary Digital Observation Pin.

Note Any value not enumerated in the tables below is reserved and should not be programmed

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Table 9-2 Primary Digital Observation Pin Signals Available in MASTER instance

DWC_DDRPHYA_MASTER0_MtestMuxSel[5:0] Value	Description
0x00	Tied to 1'b0 (disabled)
0x01	Reset
0x02	PllDigTst[1]
0x03	dfi_reset_n
0x04	PllLockStatus
0x08	PllDigTst[0]
0x1F	PORMemReset
0x21	Mtest_CalBusy
0x22	Mtest_CalMeasDone
0x24	mTestSeqRunning
0x3F	Mtest_sarDone

Table 9-3 Primary Digital Observation Pin Signals Available in ANIB instances

DWC_DDRPHYA_ANIB<N>_MtestMuxSel[5:0] Value	Description
0x00	Tied to 1'b0 (disabled)
0x14	MDllPhase[0]
0x15	MDllPhase[1]
0x16	MDllPhase[2]
0x17	MDllPhase[3]
0x18	MDllPhase[4]
0x19	MDllPhase[5]
0x1A	MDllPhase[6]
0x1B	MDllPhase[7]
0x1C	MDllPhase[8]
0x26	WarmReset

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Table 9-3 Primary Digital Observation Pin Signals Available in ANIB instances

0x27	ColdReset
0x29	dfi_error
0x2A	dfi_init_complete
0x2B	internal_dfi_ptrinit

Table 9-4 Primary Digital Observation Pin Signals Available in DBYTE instances

DWC_DDRPHYA_DBYTE<N>_MtestMuxSel[5:0] Value	Description
0x00	Tied to 1'b0 (disabled)
0x04	LcdlCalMode
0x08	RxPadStandby_u0
0x09	RxPadStandby_u1
0x0A	TxDatFifoRdPtrInit
0x0D	RxDatRdPtrInit
0x0F	TxCmdFifoWrPtrInit
0x21	HwtMemSrc_IN
0x22	WarmReset_IN
0x29	PipeInit
0x2A	PtrInit
0x2B	PhyReset

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9.4.1.2 Secondary Digital Observation Pin

The secondary digital observation pin is not available in all configurations. For the DWC_DDRPHY_NUM_ANIBS_10 and DWC_DDRPHY_NUM_ANIBS_12 configurations, the pin can be used to output either a copy of the primary digital observation pin or PLL debug signals.

9.4.1.2.1 Using the Secondary Digital Observation Pin to observe PLL signals

To output the PLL debug signals on the secondary digital observation pin and continue to output the primary digital output, use the following procedure:

- Setup: Power on and reset the PHY. The digital observation pins can be enabled at any point after the reset.
  - If using the digital observation pin before running training firmware, write the DWC_DDRPHYA_MASTER0_PorControl CSR to 0x1 after completing the reset.

- Step 1: Enable the test output.
  - Write the DWC_DDRPHYA_MASTER0_TestBumpCntrl CSR to 0x0007 (ForceMtestOnAlert = 0x0, TestBumpDataSel = 0x00, TestBumpToggle = 0x1, TestBumpEn = 0x3).
- Step 3: The secondary digital observation output will now output the PllDigTstOut[1] value. Use the PllDigTstSel field in the DWC_DDRPHYA_MASTER0_PllTst CSR to select the value. See the DWC_DDRPHYA_MASTER0_PllTst CSR description for possible values to use.

9.4.1.2.2 Using the Secondary Digital Observation Pin to mirror the Primary Digital Observation Pin

To output a copy of the primary digital observation pin, during step 1 of the primary digital observation pin write the ForceMtestOnAlert field to 0x1 instead of 0x0. The full procedure is:

- Setup: Power on and reset the PHY. The digital observation pins can be enabled at any point after the reset.
  - If using the digital observation pin before running training firmware, write the DWC_DDRPHYA_MASTER0_PorControl CSR to 0x1 after completing the reset.
- Step 1: Enable the primary and secondary digital observation outputs.
  - Write the DWC_DDRPHYA_MASTER0_TestBumpCntrl CSR to 0x0207 (ForceMtestOnAlert = 0x1, TestBumpDataSel = 0x00, TestBumpToggle = 0x1, TestBumpEn = 0x3).
- Step 2: Initialize the selection by writing 0x00 to all instances of:
  - DWC_DDRPHYA_ANIB<N>_ MtestMuxSel, DWC_DDRPHYA_DBYTE<N>_ MtestMuxSel, DWC_DDRPHYA_MASTER0_ MtestMuxSel
- Step 3: Write the MtestMuxSel CSR in a single instance to output the desired signal from a single instance of any one ANIB, DBYTE or MASTER. Selection values are detailed in following tables.

Only a single instance of a MtestMuxSel CSR can be non-zero at a time. To select a different value, repeat steps 2 and 3. The value to write to the MtestMuxSel CSR in Step 1 is detailed in "Primary Digital Observation Pin" on page 200.

9.4.1.3 SoC Digital Observation Pin

After configuring the Primary Digital Observation Pin (as described in "Primary Digital Observation Pin" on page 200), a copy of this pin can be output onto the controller-side pin called dwc_ddrphy_dto by writing csrMTESTdtoEn to 0x1.

If use of the SoC Digital Observation Pin is desired, along with observation of the higher speed internal digital debug signals, one may decide that layout considerations are required to output the best quality digital observation signal. The final implementation of the repeaters and connecting signals is dependent on overall observation goals. If the intent is to simply observe static status signals on the SoC Digital Observation Pin, one may consider the option of not having the tools put much work into routing the related signals or choice of repeaters. However, if the user intent is to observe a high speed signal, the final implementation must take that into consideration through the use of appropriate clock repeater choices and signal shield/spacing requirements. The exact implementation details can fall in line with the overall SoC implementation. Please confer with the digital implementation methodology lead for your organization.

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9.4.2 Analog Observability

An analog test point for debug is provided on the BP_VREF bump and internal analog receiver signals can be monitored on the bump. In order to monitor the analog receiver signal, set the TestAnalogOutCntrl register field to monitor the desired signal (see "Register Description" on page 203).

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9.5 Burn-in Recommendations

During burn-in testing, the recommended action is to run a combination of "Loopback BIST Mode" on page 191 and "ATPG Test Mode" on page 190. This will ensure maximum toggling of internal nodes.

The recommendation is to alternate equally between the two modes throughout the burn-in testing process:

- For 50% of the duration, activate Loopback BIST Mode
  - Loopback BIST Mode is enabled through loading and running of the Loopback BIST Firmware Image
- For 50% of the duration, activate ATPG Test Mode
  - Operate in Scan Shift Mode
  - Activate all Scan Chains simultaneously

9.6 Bypass Mode

The Bypass interface is provided to enable fully independent control of the PHY I/Os from customer implemented logic external to the PHY.

When the BypassModeEn{AC,DAT,MASTER} pin is asserted, the associated PHY I/Os controlling BP_{A[*],D[*],…}are placed into asynchronous Bypass Mode, and are directly controlled by the top level inputs Bypass{XXX} (see Figure 9-4 on page 209). When used in Bypass Mode, the PHY I/O terminations are disabled.

Some possible use cases for the Bypass Mode of the PHY I/Os are: Boundary Scan, DC IO Parametric Testing, SoC level ATPG IO, DDR4 Memory Connectivity Testing. Please note that these use cases will require external customer-implemented logic/equipment.

The table below shows the Bypass/Flyover mapping from the Bypass Signal to the Bumps. Boundary scan is added by the customer by connecting the various Bypass signals {ModeEn, OutEn, OutData, InData} {AC, DAT, MASTER} in the customer wrapper code to create the desired boundary-scan order and behavior. The PHY architecture/RTL is fully flexible with respect to this ordering.

Table 9-5 Bypass/Flyover Mapping from the Bypass Signal to the Bumps

Bypass Signal	Bypass Signal Bits	Bump
Bypass{InData,OutData,OutEn}MASTER	1	BP_ALERT_N
Bypass{InData,OutData,OutEn}MASTER	0	BP_MEMRESET_L
Bypass{InData,OutData,OutEn}AC	[DWC_DDRPHY_NUM_ANIBS*4-1:0]	BP_A [DWC_DDRPHY_NUM_ANIBS*4-1:0]
Bypass{InData,OutData,OutEn}DBYTE	[DWC_DDRPHY_NUM_DYTES*12-1:0]	BP_D [DWC_DDRPHY_NUM_DYTES*12-1:0]

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9.6.1 Bypass Mode Rules

The following rules apply to the Bypass Mode control signals:

- All Bypass signals must be zero in mission mode
- All Bypass signals must stay zero until after PwrOkIn goes from 1-->0
- All Bypass signals must be zero before PwrOkIn goes from 0-->1

Due to the design of BP_MEMRESET_L, the following rules apply to that I/O:

- BP_MEMRESET_L does not support tristate
  - Generally BumpData = BypassModeEn && BypassOutData
  - This pin does not accept the JTAG HIGHZ command
- BP_MEMRESET_L is output-only
  - Generally BypassInData = BypassModeEn && BypassOutData

BypassMode control of the PHY I/Os is available for use after the full power-on and reset sequence of the PHY is complete (see "PHY Initialization" on page 132, steps A and B).

For applications where BypassMode control is required prior to the completion of the PHY reset sequence, the primary PHY input, atpg_mode, can be used with BypassMode controls. Refer to the following truth table to enable the functionality.

Table 9-6 BypassMode Conrtol with ATPG_Mode

DfiClk	ATPG_MODE	PwrOkin	Reset	PHY I/O Pins
Stopped	0	0	X	Power-on Defaults
Running	0	0	X	Power-on Defaults
Running	0	0	1	Power-on Defaults
Running	0	1	1	Power-on Defaults
Running	1	1	X	Controlled by BypassMode
Running	1	0	1	Controlled by BypassMode
Running	1	1	1	Controlled by BypassMode
Running	1	1	0	Controlled by BypassMode

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The PHY I/O power-on defaults ensure that any connected DRAMs are in a safe state. To ensure this, the BP_MEMRESET_L pin and any possible CKE is driven to zero. All other pins are placed in High Impedance (Hi-Z) state. The following table describes the PHY I/O Power On Defaults.

Table 9-7 PHY I/O Power-on Defaults[1]

PHY_Configuration	BP_MEMRESET_L	BP_ALERT_N	BP_D[*]	BP_A[*]
DWC_DDRPHY_NUM_ ANIBS_3	0	Hi-Z	Hi-Z	BP_A[0,1]=0 other Hi-Z
DWC_DDRPHY_NUM_ ANIBS_6	0	Hi-Z	Hi-Z	BP_A[0,1, 12, 13]=0 other Hi-Z
DWC_DDRPHY_NUM_ ANIBS_10	0	Hi-Z	Hi-Z	BP_A[0,1, 20, 21]=0 other Hi-Z
DWC_DDRPHY_NUM_ ANIBS_12	0	Hi-Z	Hi-Z	BP_A[0,1, 2, 3, 46, 47]=0 other Hi-Z

1. Note: BP_A[0,1], BP_A[0,1, 12, 13], BP_A[0,1, 20, 21] and BP_A[0,1,2, 3, 46, 47] are mapped to CKE DRAM signal pins based on DWC_DDRPHY_NUM_ ANIBS_3, DWC_DDRPHY_NUM_ ANIBS_6, DWC_DDRPHY_NUM_ ANIBS_10 and DWC_DDRPHY_NUM_ ANIBS_12 respectively. Please Refer to "DFI Pin List and Pin Mapping" on page 68

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9.6.2 Bypass Mode Architecture

The functional architecture of the Bypass/Flyover controls is shown in the following figure.

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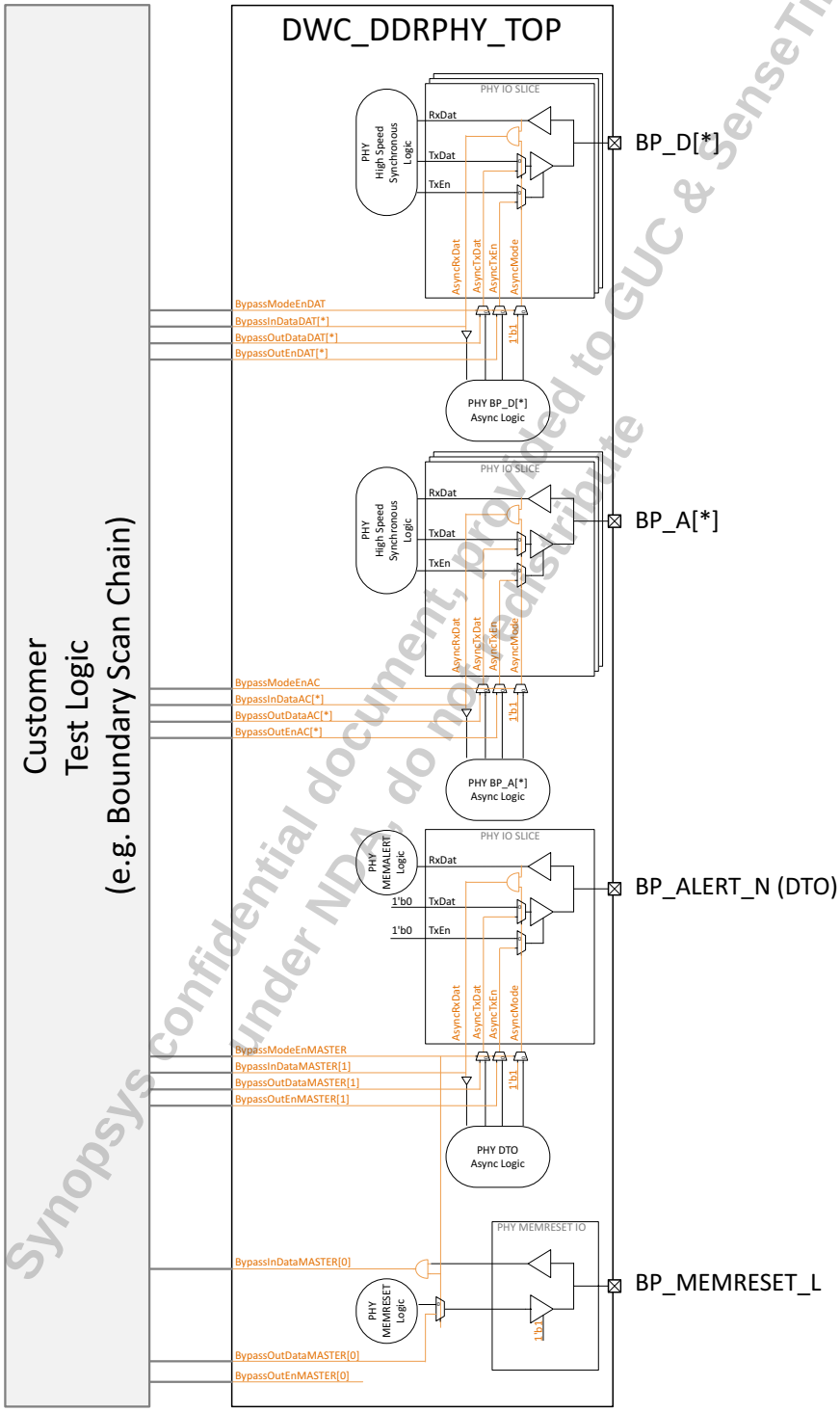
Figure 9-4 Bypass/Flyover Controls



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9.7 I/O Cell DC Parametric Characterization

The PHY I/O library includes the following features related to IO Cell Characterization:

- Programmable input termination (ODT)
- Programmable output impedance
- PVT-compensated ODT and output impedance
- Bypass path to directly control the output driver and monitor received data.
- Driver and receiver power-down control
- PAD and internal loopback modes

The SSTL I/O and PHY Utility Block (PUB) together provide the I/O test functionality. Because control of the testing is via the programmable registers of the PUB, the test methodology may be tailored to suit device requirements. For example, sample testing may be chosen for production testing to reduce test time and more exhaustive testing being reserved for sample/QA testing.

9.7.1 Overview

SSTL I/O testing and characterizing includes the following elements:

- General input and output functional operation
- Output impedance values and control
- Input termination impedance values and control
- Voltage levels (VOH/VOL/VIH/VIL)

Of these tests, general input and output would be both a production test and a characterization test that would be exercised on all signal pins. The remaining tests are characterization tests that also carry high value in production testing. It is recommended that these tests be run in early production testing on all pins if possible. The amount of testing may be eventually reduced with a better understanding of the foundry process yield and the required operating points for the end product.

In order to test the I/O cells, it is required to have monitor and controllability of following at the system level:

- Bypass mode signals
- External (PAD) pin
- Configuration signals

9.7.1.1 Bypass Mode Signals

See "Bypass Mode" on page 205 for general architecture of bypass mode and a detailed list of signals. Control capability is required for the bypass mode input signals and monitor capability for the output signals. It is recommended to control these signals via standard JTAG boundary scan cells.

9.7.1.2 External (PAD) pin

The PAD pin must be controlled and observable via the tester. Additionally, BP_ZN should be connected to ground with R_{ZN} resistor.

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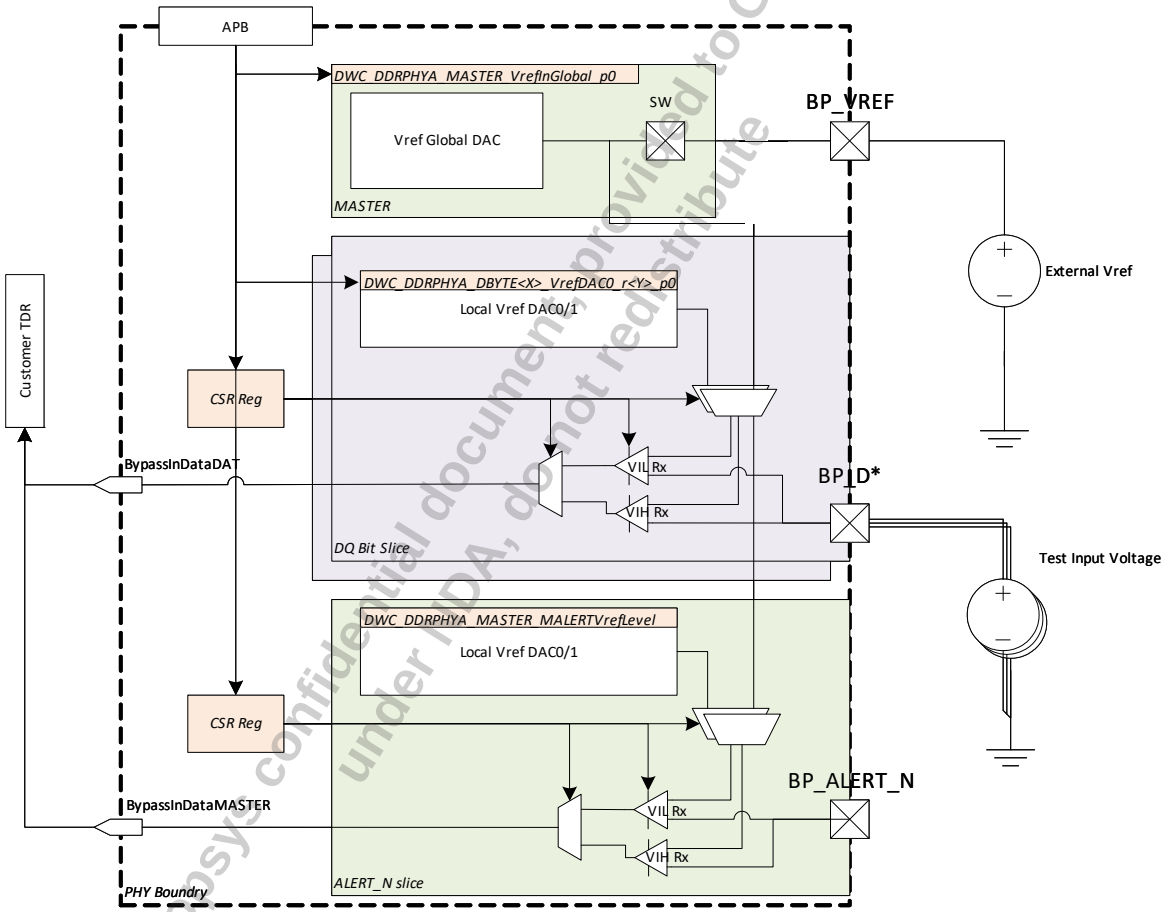
9.7.1.3 Configuration Registers

Access to the APB interface is required to read and write configuration registers. The programing must be in sequence according the test instructions in the following sections.

9.7.2 VIH/VIL Testing

The VIH/VIL test can be done on all of the DQ bit slices and BP_ALERT_N independently and in parallel. Figure 9-5 captures the entire bypass path in the PHY for this test.

Figure 9-5 Bypass Path in the PHY During VIH/VIL Testing



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9.7.3 Selecting VREF Source

There are the following sources for receiver VREF voltage:

- External VREF
- Global VREF generated through DAC in Master
- Local VREF generated through DAC in each bit slice

The output of each receiver is sent out the BypassInData{DAT,MASTER} pin of the PHY and it is expected to be captured through boundary scan or shifted in to a TDR outside the PHY for observability.

To perform VIL/VIH testing the tester is required to sweep the voltages of BP_D and BP_ALERT_N pins for a given static VREF setting. If external VREF is used, the tester must drive this voltage on the BP_VREF pin. For Global VREF generated through DAC in Master and Local VREF generated through DAC in each bit slice, the test is required to program the PHY DAC's through the APB interface to generate the desired VREF level.

When using local VREF, DWC_DDRPHYA_DBYTE*_VrefDAC0_r* must be used to program the local DAC in each receiver.

Note the PHY only has one global VREF DAC and its output is routed to both Slice's of the receiver. Use GlobalVrefInDAC to control the Global VREF when this mode is selected. The following table lists the registers that need to be programmed based on VREF mode.

Table 9-8 Registers Programmed Based on VREF Mode

REGISTER Register Address	Programmed Value			Notes
	External Vref	Global Vref	Local Vref	
DWC_DDRPHYA_MASTER_VrefInGlobal_p0	0x3	See VrefInGlobal register spec for details. Example: LPDDR4 = 0x24 DDR= 0x20	0x0	1,3
DWC_DDRPHYA_MASTER_PorControl_p0	0x1	0x1	0x1	
For DQ pins				
DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl_b0 DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl_b1	DDR4=0x45b1 LPDDR4=0x45a1	DDR4=0x45b1 LPDDR4=0x45a1	DDR4=0x45b0 LPDDR4=0x45a0	
DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl_b0 DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl_b1	DDR4=0x45b1	DDR4=0x45b1	DDR4=0x45b0	4
	DDR4=0x45b5	DDR4=0x45b5	DDR4=0x45b4	5
	DDR4=0x85b5	DDR4=0x85b5	DDR4=0x85b4	6
DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl1	0x0	0x0	0x0	

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Table 9-8 Registers Programmed Based on VREF Mode

DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r0 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r1 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r2 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r3 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r4 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r5 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r6 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r7 DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r8	-	-	See VrefDAC0 Register Spec for programing details.	1
DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r0 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r1 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r2 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r3 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r4 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r5 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r6 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r7 DWC_DDRPHYA_DBYTE_{N}_VrefDAC1_r8	-	-	See VrefDAC1 Register Spec for programing details.	6
For BP_ALERT_N				
DWC_DDRPHYA_MASTER_MemAlertControl	0x80	0x80	0x40	

Note:

1. A minimum of 300ns VREF settling time is required when changing VrefDac0/1 settings.
2. MemAlert does not support DFE.
3. User GlobalVrefInDAC to control the VREF level when Global VREF is used.
4. Setting for DFE disabled.
5. Settings for testing Rx slice 0 when DFE is enabled
6. Settings for testing Rx slice 1 when DFE is enabled.
7. A minimum of 300ns VREF settling time is required when changing VrefDac0/1 settings.
8. MemAlert does not support DFE.
9. User GlobalVrefInDAC to control the VREF level when Global VREF is used.

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9.7.4 VIL/VIH Test Sequence

This step is common to all DC characterization tests described below and must be followed prior to the sequences described in the next section:

1. Bring up VDD, VDDQ, VDDLP and VAA. (see "(A) Bring up VDD, VDDQ, VDDQLP, and VAA" on page 134)

2. Start Clocks and Reset the PHY. (see "(B) Start Clocks and Reset the PHY" on page 134)
3. Set PHY pin atpg_mode=0,
4. Set PHY in Bypass Mode operation for VIL/VIH testing. (see "Bypass Mode" on page 205 for details of bump mapping and bypass mode operation)
   a. BypassModeEnAC=1; set BypassOutEnAC[DWC_DDRPHY_NUM_ANIBS*4-1:0] to all zeros.
   b. BypassModeEnDat=1; Set BypassOutEnDAT[DWC_DDRPHY_NUM_DBYTE*12-1:0] to all zeros.
   c. BypassModeEnMaster=1, BypassOutEnMASTER[1:0] to all zeros.
5. Write PHY REGISTER's per Table 9-7 and type of VREF selected.
   a. DWC_DDRPHYA_MASTER_VrefInGlobal_p0
   b. DWC_DDRPHYA_MASTER_PorControl_p0
   c. For each offset and DBYTE instance write DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl_b{b}. You may use the broadcast address mask to write to all instances at once using address range 0x01F143 to 0x01F043.
   d. For each offset and DBYTE instance write DWC_DDRPHYA_DBYTE_{N}_DqDqsRcvCntrl1. You may use the broadcast address mask to write to all instances at once using address 0x01F04A
   e. For each offset and DBYTE instance write DWC_DDRPHYA_DBYTE_{N}_VrefDAC0_r{r}. You may use the broadcast address mask to write to all instances at once using address range 0x01F040 to 0x01F840
   f. DWC_DDRPHYA_MASTER_MemAlertControl.
6. If using external VREF, set the voltage level on BP_VREF to the desired midpoint of the signal swing: (VIL + VIH) / 2.
7. Set the voltage level on BP_D* and BP_ALERT_N to the desired level for VIH/VIL. See Table 5-3 on page 113 to the desired VIL/VIH voltage levels.
8. Wait at least 300ns.
9. Sample BypassInDataDAT and BypassInDataMaster outputs from the PHY.

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Example 9-1 Example Step 4 (above)

Following is the sequence of register writes for testing BP_D* VIL using local generated VREF for DDR4 DRAM, NUM_DBYTE=4.

```
apb_write(0x0200b2,0x0000) // DWC_DDRPHYA_MASTER_VrefInGlobal_p0
apb_write(0x020090,0x0001) // DWC_DDRPHYA_MASTER_PorControl
// Optional broadcast addressing to DBYTE instances are used in steps
// c-n to reduce the number of register writes. See notes 5.c/d/e.
// If broadcast addressing is not possible in your system, the register
// writes must be repeated for each DBYTE instance.
apb_write(0x01f043,0x45b0) // DWC_DDRPHYA_DBYTE*_DqDqsRcvCntrl_b0
apb_write(0x01f143,0x45b0) // DWC_DDRPHYA_DBYTE*_DqDqsRcvCntrl_b1
apb_write(0x01f04a,0x0000) // DWC_DDRPHYA_DBYTE*_DqDqsRcvCntrl1
apb_write(0x01f040,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r0 Local VREF
apb_write(0x01f140,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r1 Local VREF
apb_write(0x01f240,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r2 Local VREF
apb_write(0x01f340,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r3 Local VREF
apb_write(0x01f440,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r4 Local VREF
apb_write(0x01f540,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r5 Local VREF
apb_write(0x01f640,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r6 Local VREF
apb_write(0x01f740,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r7 Local VREF
apb_write(0x01f840,0x0040) // DWC_DDRPHYA_DBYTE*_VrefDAC0_r8 Local VREF
apb_write(0x02005b,0x0040) // DWC_DDRPHYA_MASTER_MemAlertControl Local VREF
```

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9.7.5 DQS Input Differential Voltage Testing (Vindiff_DQS)

The DQS_t and DQS_c mission receivers directly feed into the clock delay circuits and thus require special programing to enable input differential voltage measurements. The following sequence should be follow to enable observation of DQS receiver the BP_D[10:9] and BP_D[11,8]. Note: the sequence depends on operating mode.

1. Bring up VDD, VDDQ, and VAA ("(A) Bring up VDD, VDDQ, VDDQLP, and VAA" on page 134).
2. Start Clocks and Reset the PHY.(see "(B) Start Clocks and Reset the PHY" on page 134)
3. Write the registers specified in dwc_ddrphy_dqs_vix_setup.txt (see "dwc_ddrphy_dqs_vix_setup.txt" on page 217)
4. Write the following registers:
   a. Program DWC_DDRPHYA_DBYTE*_DqDqsRcvCntrl_b0 per protocol
5. Set PHY pin BypassModeEn=1
6. Set the DQS_t and DQS_c bumps to the desired differential voltage to test.
7. Wait at least 300ns
   - Sample BypassInDataDAT[10+(12*<DBYTE>)]. The pin will toggle per inverse of the sign of VDQS_t - VDQS_C given the large enough delta per JEDEC protocol specification. BypassInDataDAT[9+(12*<DBYTE>)] is not related to DQS mission mode differential receiver and must be ignored.

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9.7.5.1 dwc_ddrphy_dqs_vix_setup.txt

The following shows the content of the setup.txt file (see "DQS Input Differential Voltage Testing (Vindiff_DQS)" on page 216):

```
dwc_ddrphy_apb_wr(32'h20090,16'h0001);
dwc_ddrphy_apb_wr(32'h1ff43,16'h45b0);
dwc_ddrphy_apb_wr(32'h1f04a,16'h0000);
dwc_ddrphy_apb_wr(32'h20077,16'h0004);
dwc_ddrphy_apb_wr(32'h20074,16'h0001);
dwc_ddrphy_apb_wr(32'h20002,16'h0001);
dwc_ddrphy_apb_wr(32'h2006e,16'h0001);
dwc_ddrphy_apb_wr(32'h200f8,16'h0000);
dwc_ddrphy_apb_wr(32'h400f2,16'h0000);
dwc_ddrphy_apb_wr(32'h400f3,16'h0000);
dwc_ddrphy_apb_wr(32'h400f4,16'h0000);
dwc_ddrphy_apb_wr(32'h70015,16'h0688);
dwc_ddrphy_apb_wr(32'h70016,16'h0fac);
dwc_ddrphy_apb_wr(32'h40000,16'h2204);
dwc_ddrphy_apb_wr(32'h40020,16'h0003);
dwc_ddrphy_apb_wr(32'h40001,16'h2204);
dwc_ddrphy_apb_wr(32'h40021,16'h0003);
dwc_ddrphy_apb_wr(32'h40002,16'h2204);
dwc_ddrphy_apb_wr(32'h40022,16'h0003);
dwc_ddrphy_apb_wr(32'h40003,16'h2204);
dwc_ddrphy_apb_wr(32'h40023,16'h0003);
dwc_ddrphy_apb_wr(32'h40004,16'h2204);
dwc_ddrphy_apb_wr(32'h40024,16'h0003);
dwc_ddrphy_apb_wr(32'h40005,16'h2204);
dwc_ddrphy_apb_wr(32'h40025,16'h0003);
dwc_ddrphy_apb_wr(32'h40006,16'h2204);
dwc_ddrphy_apb_wr(32'h40026,16'h0003);
dwc_ddrphy_apb_wr(32'h40007,16'h2204);
dwc_ddrphy_apb_wr(32'h40027,16'h0003);
dwc_ddrphy_apb_wr(32'h40008,16'h2204);
dwc_ddrphy_apb_wr(32'h40028,16'h0003);
dwc_ddrphy_apb_wr(32'h40009,16'h2204);
dwc_ddrphy_apb_wr(32'h40029,16'h0003);
dwc_ddrphy_apb_wr(32'h4000a,16'h2204);
dwc_ddrphy_apb_wr(32'h4002a,16'h0003);
dwc_ddrphy_apb_wr(32'h4000b,16'h2204);
dwc_ddrphy_apb_wr(32'h4002b,16'h0003);
dwc_ddrphy_apb_wr(32'h4000c,16'h2204);
dwc_ddrphy_apb_wr(32'h4002c,16'h0003);
dwc_ddrphy_apb_wr(32'h4000d,16'h2204);
dwc_ddrphy_apb_wr(32'h4002d,16'h0003);
dwc_ddrphy_apb_wr(32'h4000e,16'h2204);
dwc_ddrphy_apb_wr(32'h4002e,16'h0003);
dwc_ddrphy_apb_wr(32'h4000f,16'h2204);
dwc_ddrphy_apb_wr(32'h4002f,16'h0003);
dwc_ddrphy_apb_wr(32'h40010,16'h2204);
dwc_ddrphy_apb_wr(32'h40030,16'h0003);
dwc_ddrphy_apb_wr(32'h40011,16'h2204);
dwc_ddrphy_apb_wr(32'h40031,16'h0003);
dwc_ddrphy_apb_wr(32'h40012,16'h2204);
dwc_ddrphy_apb_wr(32'h40032,16'h0003);
dwc_ddrphy_apb_wr(32'h40013,16'h2204);
dwc_ddrphy_apb_wr(32'h40033,16'h0003);
```

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```
dwc_ddrphy_apb_wr(32'h40014,16'h2204);
dwc_ddrphy_apb_wr(32'h40034,16'h0003);
dwc_ddrphy_apb_wr(32'h40015,16'h2204);
dwc_ddrphy_apb_wr(32'h40035,16'h0003);
dwc_ddrphy_apb_wr(32'h40016,16'h2204);
dwc_ddrphy_apb_wr(32'h40036,16'h0003);
dwc_ddrphy_apb_wr(32'h40017,16'h2204);
dwc_ddrphy_apb_wr(32'h40037,16'h0003);
dwc_ddrphy_apb_wr(32'h40018,16'h2204);
dwc_ddrphy_apb_wr(32'h40038,16'h0003);
dwc_ddrphy_apb_wr(32'h40019,16'h2204);
dwc_ddrphy_apb_wr(32'h40039,16'h0003);
dwc_ddrphy_apb_wr(32'h4001a,16'h2204);
dwc_ddrphy_apb_wr(32'h4003a,16'h0003);
dwc_ddrphy_apb_wr(32'h4001b,16'h2204);
dwc_ddrphy_apb_wr(32'h4003b,16'h0003);
dwc_ddrphy_apb_wr(32'h4001c,16'h2204);
dwc_ddrphy_apb_wr(32'h4003c,16'h0003);
dwc_ddrphy_apb_wr(32'h4001d,16'h2204);
dwc_ddrphy_apb_wr(32'h4003d,16'h0003);
dwc_ddrphy_apb_wr(32'h4001e,16'h2204);
dwc_ddrphy_apb_wr(32'h4003e,16'h0003);
dwc_ddrphy_apb_wr(32'h4001f,16'h2204);
dwc_ddrphy_apb_wr(32'h4003f,16'h0003);
dwc_ddrphy_apb_wr(32'h20079,16'h0080);
dwc_ddrphy_apb_wr(32'h20003,16'h0001);
dwc_ddrphy_apb_wr(32'h20003,16'h0000);
dwc_ddrphy_apb_wr(32'h20079,16'h0001);
dwc_ddrphy_apb_wr(32'h20079,16'h0000);
dwc_ddrphy_apb_wr(32'h400f1,16'h0000);
dwc_ddrphy_apb_wr(32'h20081,16'h0001);
```

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9.7.6 VOH/VOL Testing

In order to test mission mode drive strength, it is required to connect the BP_ZN pin to the ground with the same resistance intended to use in mission mode system.

During the test calibration state machine will run and complete in order to determine the mission mode strength offset so that the desired programmed output impedance is accurately reflected on all PHY drivers.

In order to make accurate VOL and VOH readings, an Rtt resistor must also be connected to every device pin and a termination level Vtt. The recommended Rtt and Vtt should be set based on the system-level termination expected to be used in mission mode operation. For example, LPDDR4 would set Vtt=0V; DDR4 DQ would set Vtt=VDDQ; DDR4 AC would set Vtt=VDDQ/2. An Rtt of 50 ohm is a good, generic value, although the mission mode termination value can also be used

During the test, the PHY transmitter will drive the BP_D* BP_A* to VDDQ/VSS with the impedance Rpu/Rdn programmed in the following:

- BP_D*: DWC_DDRPHYA_DBYTE_{N}_TxImpedanceCtrl1_b_p[3:0]
- BP_A*: DWC_DDRPHYA_ANIB_{N}_ ATxImpedance _p0

The VOH/VOL can be derived using the following equation:

- VOH=(Rtt/(Rtt+Rup))*(VDDQ-Vtt)
- VOL = (Rdn/(Rtt+Rdn))*Vtt

LPDDR4x uses a non-linear output driver. VOH in LPDDR4x should meet the requirements described in the Electrical Specification Chapter of the *LPDDR4x multiPHY Databook*.

Figure 9-6 shows the overall system setup for VOL and VOH testing.

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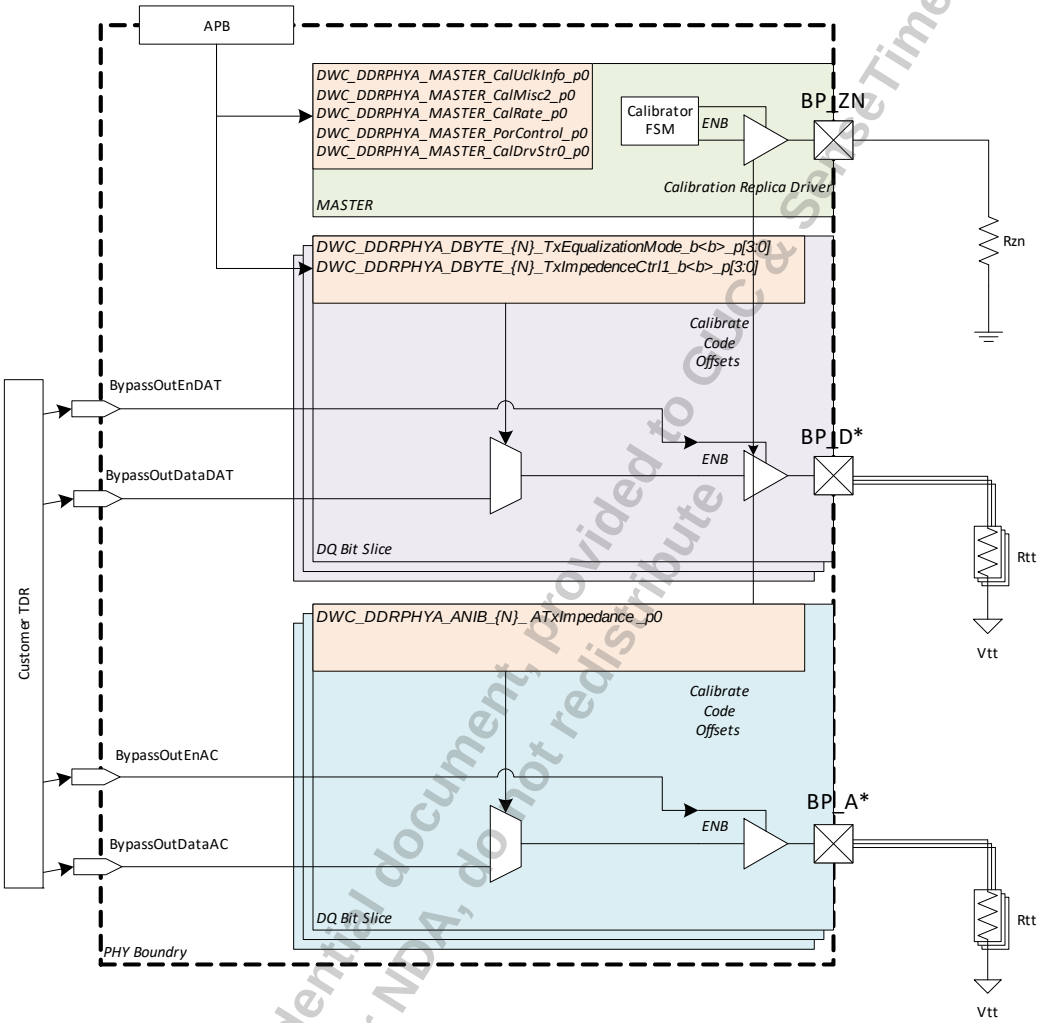
Figure 9-6 VOH/VOL Testing



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9.7.7 VOH/VOL Test Sequence

1. Bring up VDD, VDDQ, VDDQLP and VAA (see "(A) Bring up VDD, VDDQ, VDDQLP, and VAA" on page 134)
2. Start Clocks and Reset the PHY (see "(B) Start Clocks and Reset the PHY" on page 134)
3. Set PHY pin atpg_mode=0.
4. Set PHY in Bypass Mode operation for VOL/VOH testing (see "Bypass Mode" on page 205 for details of bump mapping and bypass mode operation)
   a. BypassModeEnAC=1
      i. Set BypassOutEnAC[DWC_DDRPHY_NUM_ANIBS*4-1:0] to all ones or set individually as desired.
   b. BypassModeEnDat=1
      i. Set BypassOutEnDAT[DWC_DDRPHY_NUM_DBYTE*12-1:0] to all ones or set individually as desired.
   c. BypassModeEnMaster=1, BypassOutEnMASTER[1:0]= 2'h3 or set individually as desired.
5. Program and run impedance calibration. Perform the following REGISTER write via PHY APB interface.
   a. Write DWC_DDRPHYA_MASTER_CalUclkInfo_p[3:0] = x0320.
   b. Write DWC_DDRPHYA_MASTER_CalMisc2 = 0x7.
   c. Write DWC_DDRPHYA_MASTER_CalDrvStr0_p0 with the value corresponding to R_{ZN}.
   d. Kick off calibration by writing DWC_DDRPHYA_MASTER_CalRate = 0x12.
   e. Wait 8 DFI clocks
   f. Write DWC_DDRPHYA_MASTER_CalRate = 0x02
   g. Wait 36ms
   h. Write DWC_DDRPHYA_MASTER_PorControl =0x1 to enable calibration code propagation to the transmitters by setting PllDllLockDone
   i. Wait 16 DFI clocks
   j. For each Pstate, offset and DBYTE instance write DWC_DDRPHYA_DBYTE_{N}_TxEqualizationMode_b<b>_p[3:0] = 0x0. Alternatively, you may use the broadcast address mask to write to all Pstate, offset and instances at once using address 0x71FF48.
   k. For each Pstate, offset and DBYTE instance write DWC_DDRPHYA_DBYTE_{N}_TxImpedanceCtrl1_b<b>_p[3:0] = Desired DQ Impedance code. See Table 3-46 fields DrvStrenFSDqP and DrvStrenFSDqN for mapping of binary values to the desired drive strength in. You may use the broadcast address mask to write to all Pstate, offset and instances at once using address 0x71FF49.
   l. For each ANIB instance write DWC_DDRPHYA_ANIB_{N}_ ATxImpedance _p0 = Desired Address Impedance code. See Table 3-11 fields ADrvStrenP and ADrvStrenN for mapping of binary values to the desired drive strength. You may use the broadcast address mask to write to all instances at once using address 0x70F043.

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6. Set up the tester to drive the BP_D* and BP_A* pins to Vtt via Rtt.
7. Drive the following PHY pins:
   a. BypassOutDataDAT[0] = 1'b1
   b. BypassOutEnDAT[11:0] = 12'hfff
8. Measure voltage at BP_D*, BP_A* and compare with expected result from formula at the tester to determine pass/fail criteria.

Example 9-2 Example Step 4 (above)

Following is an example of register programing to measure VOL/VOH for on BP_D*/BP_A* using Rzn=120Ohm, Rup=60, Rdn=60.

```
a.  apb_write(0xf20008,0x0320) // DWC_DDRPHYA_MASTER_CalUclkInfo_p[3:0] =
    x0320.
b.  apb_write(0x020098,0x2007) // DWC_DDRPHYA_MASTER_CalMisc2 = 0x7.
c.  apb_write(0x020050,0x0000) // DWC_DDRPHYA_MASTER_CalDrvStr0_p0 for
    Rzn=120
d.  apb_write(0x020088,0x0012) // DWC_DDRPHYA_MASTER_CalRate = 0x12.
e.  wait 8 DFI clocks
f.  apb_write(0x020088,0x0002) // DWC_DDRPHYA_MASTER_CalRate = 0x02.
g.  wait 36ms
h.  apb_write(0x020090,0x0001) // DWC_DDRPHYA_MASTER_PorControl =0x1
i.  wait 16 DFI clocks
    // Optional broadcast addressing to DBYTE instances are used in steps
    // j-n to reduce the number of register writes. See notes 5.j/k/l.
    // If broadcast addressing is not possible in your system, the register
    // writes must be repeated for each DBYTE or each DBYTE instance.
j.  apb_write(0x71f048,0x0000) //
    DWC_DDRPHYA_DBYTE_*_TxEqualizationMode_b0_p* = 0x0.
k.  apb_write(0x71f148,0x0000) //
    DWC_DDRPHYA_DBYTE_*_TxEqualizationMode_b1_p* = 0x0.
l.  apb_write(0x71f049,<impedance code>) //
    DWC_DDRPHYA_DBYTE_*_TxImpedanceCtrl1_b0_p* for Rup=Rdn=60 Ohm. ( Refer
    to TxImpedanceCtrl1 register description for the 60 Ohm pull-up and
    pull-down impedance codes )
m.  apb_write(0x71f149, <impedance code>) //
    DWC_DDRPHYA_DBYTE_*_TxImpedanceCtrl1_b1_p* for Rup=Rdn=60 Ohm( Refer to
    TxImpedanceCtrl1 register description for the 60 Ohm pull-up and pull-
    down impedance codes )
n.  apb_write(0x00f043, <impedance code>) // DWC_DDRPHYA_ANIB_*_
    ATxImpedance_p0 for Rup=Rdn=60 ( Refer to ATxImpedance register
    description for the 60 Ohm pull-up and pull-down impedance codes)
o.
```

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p.

Notes: BypassModeRxDqs needs to be asserted.

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9.7.8 Measuring ODT Impedance

Following are instructions to setup the PHY to measure ODT impedance. It is required that BP_ZN calibration resistor to be present at the PHY pins.

1. Bring up VDD, VDDQ, and VAA according to step (A) in PHY Initialization
2. Start Clocks and Reset the PHY according to step (B) in PHY Initialization
3. Set DWC_DDRPHYA_MASTER_ClockingCtrl=0x1to set PclkEnAsyncCtrl
4. Program calibration control registers and kick off calibration state machine
   a. Write DWC_DDRPHYA_MASTER_CalUclkInfo_p[3:0] = 0x320
   b. Write DWC_DDRPHYA_MASTER_CalMisc2 = 0x7
   c. Write DWC_DDRPHYA_MASTER_CalDrvStr0_p0 with the value corresponding to R_{ZN}
   d. Kick off calibration by writing DWC_DDRPHYA_MASTER_CalRate = 0x12
   e. Wait 8 DFI clocks
   f. Write DWC_DDRPHYA_MASTER_CalRate = 0x2
   g. Wait 36 ms
   h. Write DWC_DDRPHYA_MASTER_PorControl =0x1 to enable calibration code propagation to the transmitters by setting PllDllLockDone
   i. Wait 16 DFI clocks
5. Set register `DWC_DDRPHYA_DBYTE_*_TxOdtDrvStren` to the desired value for all DBYTES and PStates
6. Set register DWC_DDRPHYA_MASTER_ProcOdtCtl=0x2
7. Set register DWC_DDRPHYA_MASTER_TxRdPtrInit=0x0
8. Measure termination impedance on any BP_D* pins

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9.8 VDDQ or VDDLP Quiescent Current Measurement

The state of the PHY at the de-asserting edge of the WarmReset sequence is very close to the conditions required to perform VDDQ or VDDQLP quiescent current measurements.

After successfully completing the Power-on and Reset sequence (see "PHY Initialization" on page 132), the following additional registers should be programmed.

Caution No other registers should be programmed other than those specified in order to ensure the correct measurement

- Disable the PHY Master Vref Generator by writing:
  - Address 32'h0200B2 Data 16'h0000 //DWC_DDRPHYA_MASTER0_VrefInGlobal_p0

In this state, the PHY drives the following signals statically to zero. The state of these pins are provided for information only, this state does not affect the measurement.

- BP_MEMRESET_L = 1'b0 //DRAM RESET#
- BP_A pins that can function as CKE:
  - 3ACX::BP_A[1:0]
  - 6ACX::BP_A[13:12,1:0]
  - 10ACX::BP_A[21:20,1:0]
  - 12ACX::BP_A[47:46,3:0]

The procedure for VDDQLP quiescent current measurement is the same procedure described above for VDDQ quiescent current measurement.

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9.9 Input Pin Leakage Measurement

To perform Input Pin Leakage measurements, the following PHY top-level input signals must be set:

- BypassModeEnAC = 1'b1
- BypassOutEnAC[(`DWC_DDRPHY_NUM_ANIBS*4)-1:0] = All zeros
- BypassModeEnDAT = 1'b1
- BypassOutEnDAT[(`DWC_DDRPHY_NUM_DBYTES*12)-1:0] = All zeros
- BypassModeEnMASTER = 1'b1
- BypassOutEnMASTER[1] = 1'b0

All PHY I/O pins will be tristated in this mode and will support the input pin leakage measurements.

The PHY Output-only Pin BP_MEMRESET_L does not support input pin leakage measurements (or the JTAG HIGHZ command).

The PHY Analog pins {BP_VREF, BP_ZN, BP_ZN_SENSE} do not support input pin leakage measurements.

Note This state is typically achieved when the customer has connected the PHY Bypass* signals to a TDR that implements the JTAG HIGHZ command.

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10
Timing

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This chapter describes the PUB's timing, including

- "PHY Latency" on page 228
- "Rank-to-Rank Spacing" on page 232
- "Pre-Amble and Post-Amble Restrictions" on page 235
- "PHY Skew Limits" on page 236
- "PHY Update" on page 238
- "DFI Master Interface" on page 241
- "PHY DFI Sideband Interactions" on page 243
- "DFI Sideband Simultaneous Collisions" on page 247

10.1 PHY Latency

The maximum read latency on the DFI interface (DFIMRL) and the t_{phy_rdlat} DFI parameter has a defined relationship that is outlined in Table 10-1.

Table 10-1 Maximum Read Latency on the DFI Interface[1]

DFIMRL	t_{phy_rdlat} Even Phase	t_{phy_rdlat} Odd Phase
1	14	13
2	16	15
3	18	17
4	20	19
5	22	21
6	24	23
7	26	25
8	28	27
9	30	29
10	32	31
11	34	33
12	36	35
13	38	37
14	40	39
15	42	41

1. The following table assumes no additional DFI pipelining. Refer to "DFI Read Data Timing Parameters" on page 114 to see the effect of DFI pipelining.

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Where:

- DFIMRL: DFI Max Read Latency (units of DFI Clocks)
- t_{phy_rdlat} Even phase: t_{phy_rdlat} value when dfi_rddata_en is launched on the even DFI Phase
- t_{phy_rdlat} Odd phase: t_{phy_rdlat} value when dfi_rddata_en is launched on the odd DFI Phase
- ARdPtrInitVal is in units of 1 Unit Interval (UI)

Note the following constraints:

- ARdPtrInitVal range for Data Rate >= DDR1866 is 1 to 5
- ARdPtrInitVal range for Data Rate < DDR1866 is 0 to 5

- Add 1 to lower bound of ArdPtrInitVal range if PHY is in PLL Bypass Mode
- A DFIMRL value of 1 works with ARdPtrInitVal of 0 only

.

Note The PHY returns dfi_rddata_valid contiguously for each burst. There are no bubbles inserted within a burst.

10.1.1 ARdPtrInitVal Impacts From Construction Skews

The value of ARdPtrInitVal is determined by the implementation of the PHY, in addition to the constraints of the aforementioned DFIMRL values. The value of the ARdPtrInitVal must be increased from the zero delay simulations values based on the following variations:

- DfiClk Skew: Clock skew between all DfiClk input ports of the HardIPs across the PHY
- DfiClk Jitter: Clock jitter from DfiClk generation source to the HardIP DfiClk input ports
- DfiClk PVT variations: Voltage, temperature and process variations on the clock tree branches from the divergence point to the separate HardIP DfiClk input ports
- PClk Skew: Clock skew from the PClk source PLL to the HardIP Pclk input ports. This should be minimized if the PClk routing guidance in the implementation guide is followed
- PClk Jitter: Clock jitter from the PLL generating PClk to the HardIP PClk input ports. This should be minimized if the PClk routing guidance in the implementation guide is followed

Each incremental addition of each of these variations sum together to produce the amount by which the ARdPtrInitVal must be increased to properly space the FIFO pointers. With the unit of ARdPtrInitVal being in 1 Unit Interval (UI), the chosen value should be the ceiling of the sum of variations divide by the Unit Interval for a particular data rate.

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10.1.2 PHY Latency Examples and Equations

The following sections show equations and waveform examples of ideal read transaction timing, read response latency timing equations, and a DDR4 3200 transaction example.

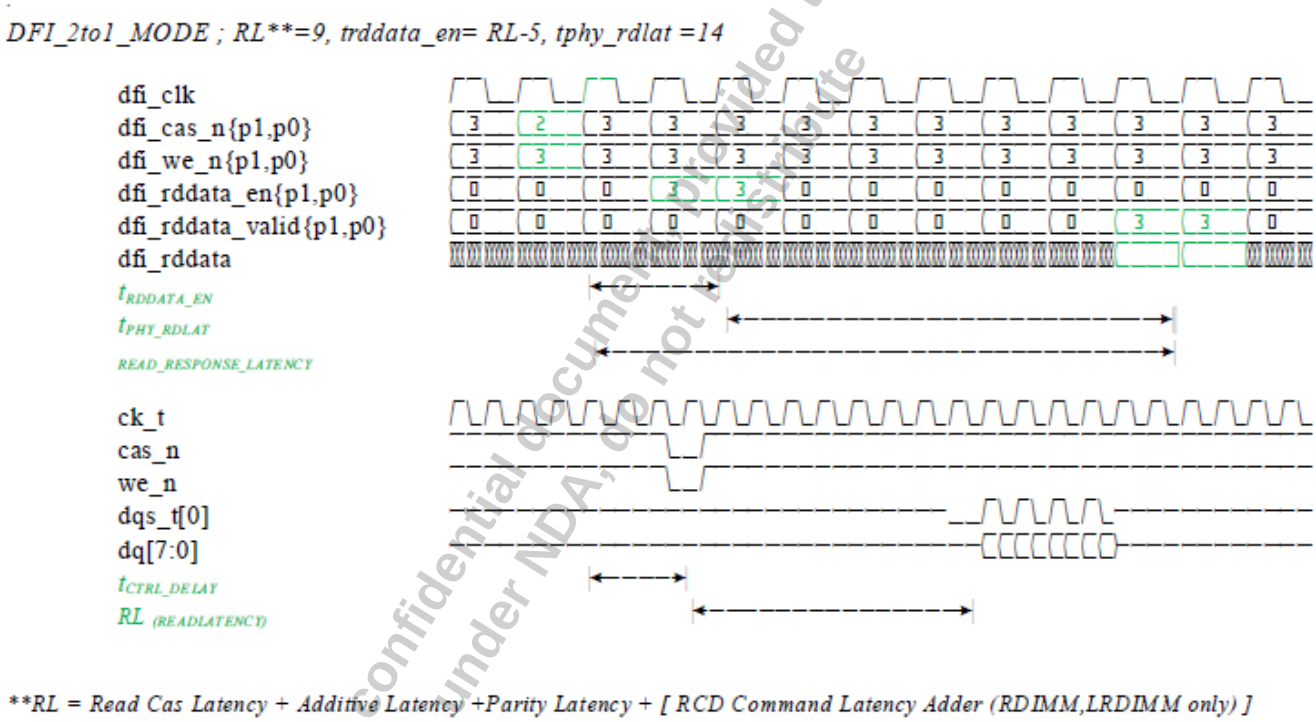
Example 10-1 Ideal Read Transaction Timing Example

Figure 10-1 shows a BL8 read transaction that is even aligned and has the command issued on dfi_phase0.

The PHY latency contribution as described in the DFI Specification

- (phy_rdlat + tphy_rddata_en - RL) = {13} + {RL – 5} - RL = 8 MEMCLKS

Figure 10-1 BL8 Read Transaction: Even Aligned, Command Issued on dfi_phase0



Example 10-2 Read Response Latency Equations

The total read response latency (in SDRAM Clocks) is defined by DFI parameters using the following equations.

- Equation 1 :: Read_Response_Latency = (RL – 5) + T_{phy_rdlat}
  - RL = Read_Cas_Latency + Additive Latency + Parity Latency + RCD_Command_Latency_Adder
- Equation 2: $T_{phy\_rdlat} = 5 + T_{ctrl\_delay} + T_{resp\_delay}$
  - $T_{ctrl\_delay} = 3 + PtrInitVal/2$
    - PtrInitVal = ceiling(($t_{PUB\_DFICLK\_SKEW} + t_{PCLK\_SKEW}$) / t_{CYCLE_PCLK})
    - $t_{PUB\_DFICLK\_SKEW}$: Skew and long-term jitter components of DFICLK tree from SOC PLL

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        - t_{PCLK_SKEW}: Skew and long-term jitter components of PCLK tree from PHY PLL
    - T_{resp_delay} = 3 + 2 * DFIMRL
- Equation 3: DFIMRL = MARGIN + trained_MRL
    - DFIMRL is a trained parameter of the PHY {range is 1…15}
        - Training Firmware includes (user-supplied MARGIN to the smallest passing trained_DFIMRL)
        - MARGIN should include maximum expected drift of $t_{DQSCK\_\{volt,temp\}}$ factors in the worst-case user-application
    - Trained_MRL = ceiling((t_{PHY_IO} + t_{CK_RN} + t_{DQS_RN} + t_{DQSCK}) / t_{CYCLE_DFICLK})
        - tPHY_IO: PHY IO cell analog delays, (estimated at 1.2nS for 14nm process)
        - tCK_RN: MEMCLK flight time, from PHY to furthest rank
        - tDQS_RN: DQS flight time, from furthest rank to PHY
        - tDQSCK: For DDR4 {0.17:0.22}ns

Example 10-3 Example Latency at DDR4-3200

- Equation 3: DFIMRL = MARGIN + ceiling (3.7nS / 1.25nS) = 4 DFICLKs
    - MARGIN: 1 DFICLK
    - t_{PHY_IO}: 1.2nS (estimated at 1.2nS for 14nm process)
    - t_{CK_RN}: 1.4nS (assume ~200mm trace)
    - t_{DQS_RN}: 0.7nS (assume ~100mm trace)
    - t_{DQSCK}: 0.22nS (worst case for DDR4)
- Equation 2: Tphy_rdlat = 5 + Tctrl_delay + Tresp_delay= 20 MEMCLKs
    - PtrInitVal = ceiling((tPUB_DFICLK_SKEW + tPCLK_SKEW) / tCYCLE_PCLK) = 2
        - $t_{PUB\_DFICLK\_SKEW}$: 0.4nS
        - t_{PCLK_SKEW}: 0.2nS
- Equation 1: Read_Response_Latency = (RL – 5) + Tphy_rdlat = 37 MEMCLKs
    - {DDR4-3200AA Unregistered, DBI-off, Parity-off} RL = 22
- Latency Total: 37 MEMCLKs @ DDR3200 = 23.125nS

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10.2 Rank-to-Rank Spacing

- Minimum possible Rank-to-Rank for Write-Write (W-W) transaction are given with the tphy_wrcsgap parameter
- Minimum possible Rank-to-Rank for Read-Read (R-R) transaction are given with the tphy_rdcsgap parameter
  - These values reflect the time required by the PHY to perform internal timing setting updates. The achievable rank-rank spacings in a system will depnd on the channel topology and the termination enable timing of the target DRAMs.
- W-W and R-R values assume the Critical Delay Difference (**CDD** - flight time between ranks) is less than 1 UI
  - For trained systems where the CDD is exceeds 1 UI, the tphy_{wr,rd}csgap parameters increase by "ceiling(CDD/tCK)" for CDD >=0. They do not decrease when CDD < 0
  - The W-W and R-R values assume 1tck preambles and 0.5tck postambles. For more information on DQS post-amble and pre-amble options, refer to "Pre-Amble and Post-Amble Restrictions" on page 235.
  -

Note When the register UseDqsEnReplica=1, the R-R rank spacings will increase by the PHY IO_roundtrip_delay. This value is typically 1nS, for mor information refer to the *DWC LPDDR4x multiPHY Databook*

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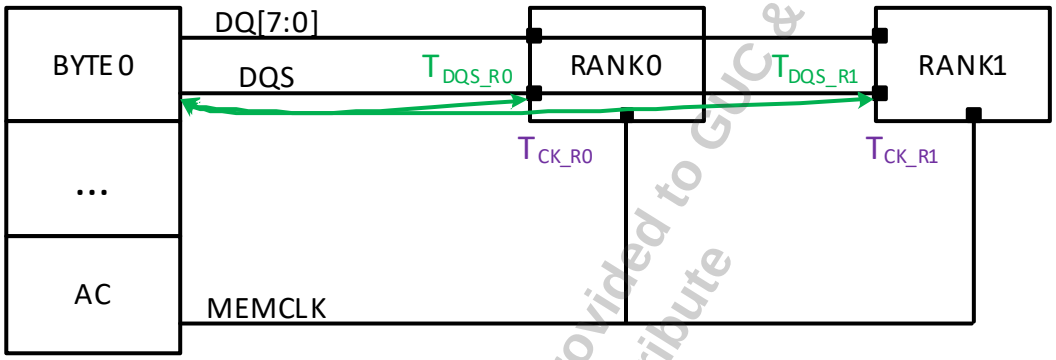
10.2.1 DQ/DQS Bus Turnarounds

The following constraints apply for an unterminated system configuration. Thus, these equations only consider scheduling constraints for the defined toggles/preambles/postambles of DQ/DQS. **Additional DRAM ODT scheduling constraints will need to be considered in terminated systems to ensure correct operation.**

Figure 10-2 Example System, and PHY Trained Parameters



10.2.1.1 Dram Transaction Timing

The Target Rank[i] for a read transaction will begin transmitting the Read DQS preamble @

- $T_{CK\_R[i]}$ + RL - N_{PRE}; // N_{PRE} = {1,2}

The Target Rank[i] for a write transaction will begin receiving the Write DQS preamble @

- $T_{CK\_R[i]}$ + WL - N_{PRE}; // N_{PRE} = {1,2}

10.2.1.2 Phy Trained State

PHY register RxEnDlyD[i] encodes the timing of the PHY readgate, which asserts in the middle of the preamble:

- $T_{CK\_R[i]}$ + $T_{DQS\_R[i]}$ + RL - N_{PRE}/2; // N_{PRE} = {1,2}

PHY register TxDQSDlyD[j] encodes the launch timing of the DQS from the PHY, which must be at :

- $T_{CK\_R[j]}$ – $T_{DQS\_R[j]}$ + WL - N_{PRE} ; // N_{PRE} = {1,2}

10.2.1.2.1 [R2W] Read from Rank[i] ; Write to Rank[j]

Constraint :: Read DQS postamble received by the PHY should complete before the PHY attempts to transmit the Write DQS preamble.

Since the constraint is measured at the PHY DQ, we can use the differences of the trained PHY CSR values for RxEnD[j] and TxDqsDlyD[j].

The absolute value of the PHY FW returned values CDD_RW_R[i]_R[j] can be used to adjust scheduling of reads to writes.

- tCCDmin (R_rank[i], W_rank[j]) = System_R2W + abs(CDD_RW_R[i]_R[j])

System_R2W = scheduling of read/write transactions after correcting for WL, RL, BL, preamble lengths

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10.2.1.2.2 [W2R] Write to Rank[i] ; Read from Rank[j]

Constraint :: Write DQS transmitted by the PHY should be observed to be complete at all Ranks before any Rank attempts to transmit the Read DQS.

- Rank[i] (target rank) will complete receiving the Write DQS postamble at:
  - $T_{CK\_R[i]}$ + WL + BL
- Other, *non-target* ranks will also complete receiving the Write DQS postamble at:
  - $T_{CK\_R[i]}$ + WL + BL + ***max(CDD_WW_R[i]_R[0..3])***
- This means the read transaction at any rank can legally start at:
  - Twrite + WL + BL + **abs(*max(CDD_WW_R[i]_R[0..3])*)**

Note Since CWL is always smaller than CL, tCDD_WR is not used because it may result in a negative number which is not meaningful for most memory controllers. Considering that the DQ bus is free soon after the first WR is completely transmitted, any CAS command can be issued afterwards. The tCDD_WW is considered the best case in this scenario.

- tCCDmin (W_rank[i], R_rank[j]) = System_W2R + abs(max(CDD_WW_R[i]_R[0..3]))
  - System_W2R = scheduling of write/read transactions after correcting for WL, RL, BL, preamble lengths

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10.3 Pre-Amble and Post-Amble Restrictions

The following pre-amble restrictions apply:

- When 2-tCK write preambles are enabled:
  - W-W transaction spacing (different ranks) must increase by 1tCK
  - R-W transaction spacing must increase by 1tCK
- When 2-tCK read preambles are enabled ::
  - R-R transaction spacing (different ranks) must increase by 1-tCK
  - W-R transaction spacing must increase by 1-tCK
- DDR4 Preamble rules
  - 2tCK Wr Preambles are determined by DRAM requirements. For best signal integrity, it is recommended to enable 2tCK Wr Preambles at the minimum frequency supported by the DRAM
  - 2tCK Rd Preambles are required at the minimum frequency supported by the DRAM
- LPDDR4 and LPDDR4x Pre-Amble/Post-Amble rules
  - For best performance, static 2tCK read preambles are recommended. (MR1.OP[3]==0). If toggling 2tCK read preambles are chosen, the system may need to schedule more frequent link retraining events (see section 4.4)
  - For best performance, 0.5 tCK read postambles are recommended (MR1.OP[7]==0). If extended 1.5 tCK read postambles are enabled, R-R transaction spacing (different ranks) and R-W transaction spacing must increase by 1-tCK.
  - 1.5 tCK write postambles may be required by certain DRAM implementations, please refer to DRAM datasheets if this is required. In case 1.5tCK write postambles are enabled, W-W transaction spacing (different ranks) and W-R transaction spacing must increase by 1-tCK.
-
-

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10.4 PHY Skew Limits

The following table shows the skew limits apply to the PHY: The following sections describe the table footnotes.

Table 10-2 PHY Skew Limits

Parameter	DRAM Type	
	DDR4	LPDDR4
Write-Leveling delay	-1 to +5.97 MEMCLKs	-0.5 to +5.47 MEMCLKs
Receive-enable delay[1]	-1 to +14 MEMCLKs	-0.5 to +13.5 MEMCLKs
DQ-to-DQ arrival time mismatch[2]	Up to 200pS within a byte	Up to 200pS within a byte
DQ Flight time to DQS Flight time skew[3]	-100ps to 100ps	-100ps to 100ps
CS, ODT, CKE, Command, Address Flight Time to CK/CK# Flight Time Skew[4]	-30ps to 30ps	-10ps to 10ps between bits of a timing group, -100ps to +100ps between timing groups

1. Refer to "Receive-enable delay" on page 238
2. Refer to "DQ-to-DQ Arrival Time Mismatch" on page 238
3. Refer to "DQ Flight time to DQS Flight time skew" on page 238
4. Refer to "CS, ODT, CKE, Command, Address Flight Time to CK/CK# Flight Time Skew" on page 238

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10.4.1 Receive-enable delay

For Receive-enable, the total supported range is above, however, the total delay difference across all ranks and bytes is 12 MEMCLKs for DDR4 and 11.5 MEMCLKs for LPDDR4 (due to the finite depth of the receive data_fifo - and the requirement for the PHY to send fully aligned receive data to the memory controller.

Example 10-4 Examples:

System 1: trained RxEn (across bytes, ranks) range = {-1 : +11} MEMCLKs

System 2: trained RxEn (across bytes, ranks) range = {+2 : +14} MEMCLKs

For LPDDR4 systems, this skew requirement includes the worst case tDQSCK delay.

10.4.2 DQ-to-DQ arrival time mismatch

- Measured on reads at phy pins. PHY BDL will be trained to compensate for this delay.
- Timing budget shall add up all system terms and account for any difference to the supported range
- Measured on writes at DRAM PIN assuming no skew at phy pin.
- Does not include ISI (clock pattern)

Caution It is strongly recommended to keep all flight times across the DQ's matched within 10ps for signal integrity reasons. It is responsibility of the system designer to mitigate signal integrity issues arising from cross talk alignment due to flight time mismatch

10.4.3 DQ Flight time to DQS Flight time skew

- Includes all system routing delays from PHY pin to DRAM pin
- Includes all DRAM delays, including tDQSQ.
- Timing budget shall add up all system terms and account for any difference to the supported range

10.4.4 CS, ODT, CKE, Command, Address Flight Time to CK/CK# Flight Time Skew

- Includes all system routing delays to the DRAM ball or DIMM connector
- PHY has the ability to add pre-programmed delay on groups of 4 AC bits to patch eventual violations of this spec. It will be responsibility of the user to program the correct values to these of these delays should they be needed

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10.5 PHY Update

As per the DFI spec, the DFI update interface is intended to facilitate various operations that require interruption of transmission on the DFI interface. The update can be initiated by either the Controller (using the dfi_ctrlupd_req signal) or the PHY (using the dfi_phyupd_req signal).

Note In two-channel operation, the PHY Update interfaces operate independently of one another.

10.5.1 Controller initiated updates

The Controller initiated update interface consists of the following two signals:

Table 10-3 Controller initiated update interface signals

Signal Name	Source	Width	Description
dfi_ctrlupd_req	Controller	1	This is a Controller initiated update. Assertion of this signal indicates that the DFI interface will be idle for enough time for the PHY to perform an update. If the PHY acknowledges the request by asserting dfi_ctrlupd_ack, then the controller must continue to hold this signal high until the PHY de-asserts dfi_ctrlupd_ack.
dfi_ctrlupd_ack	PHY	1	This is the acknowledge signal to the Controller initiated update. Once the PHY asserts this, it must be de-asserted before $t_{ctrlupd\_max}$ expires.

The PHY uses the controller initiated updates for two purposes:

- Perform periodic Delay Element Compensation. This function compensates for temperature and voltage drift in the delay elements in the PHY. The Controller can
- Reset the PHY clock crossing FIFO pointers. This can be used by the controller to reset the PHY in the case of a Address/Command parity error from the DRAM on the ALERT_N pin (signaled to the controller on dfi_alert_n[1:0]). In the case of the Addr/Command parity error, the contents of the receive data FIFO are co rrupted and must be discarded by resetting the PHY pointers. The Controller initiated update will accomplish this. In the case where the ALERT was not triggered, this function of the Controller initiated update will still be performed, but has no adverse effect.

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10.5.2 PHY Initiated Updates

The PHY update interface consists of the following signals:

Table 10-4 PHY update interface signals

Signal Name	Source	Width	Description
dfi_phyupd_req	PHY	1	This is a PHY initiated update request. Assertion of this signal indicates that the PHY is requesting that the Controller hold DFI interface idle for enough time for the PHY to perform an update. The Controller must assert the dfi_phyupd_ack signal within t_{phyupd_resp} cycles of the assertion of this signal. When the Controller acknowledges the request by asserting dfi_phyupd_ack, then the Controller must continue to hold dfi_phyupd_ack high until the PHY de-asserts dfi_phyupd_req.
dfi_phyupd_type[1:0]	PHY	2	This is the PHY initiated update select signal. The value of this bus indicates what type of update the PHY is requesting and determines the timing parameters for the update (t_{phyupd_type0}, t_{phyupd_type1}, t_{phyupd_type2}, or t_{phyupd_type3}). This value will remain constant the entire time the dfi_phyupd_req is asserted. The only value that the PHY will use is 2'b00.
dfi_phyupd_ack	Controller	1	This is the acknowledge signal from the Controller in response to the PHY initiated update request.

The PHY only initiates an update for the purposes of performing the same Delay Element Compensation that it does during the Controller initiated updates. Internally, the PHY has a counter to guarantee that the Delay Element Compensation occurs often enough for the temperature and voltage drift will not adversely affect the memory operation. The counter value is defined by the value in the DFIPHYUPDCNT CSR.

If the counter expires, it will issue an update request via the dfi_phyupd_req signal with the dfi_phyupd_type[1:0] field set to 2'b00. (All other values of the type field are unused).

If the Controller acknowledges the request, the PHY will perform the compensation and reset the counter. If the Controller does not acknowledge the request, the PHY will assert the dfi_error signal (with dfi_error_info set to 4'b0000). This indicates that the PHY is beyond its compensation time, and correct memory operation is no longer guaranteed.

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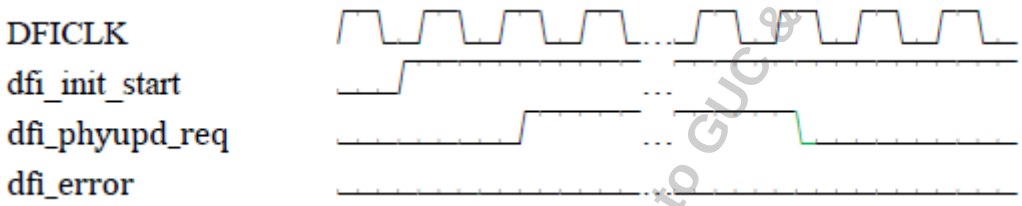
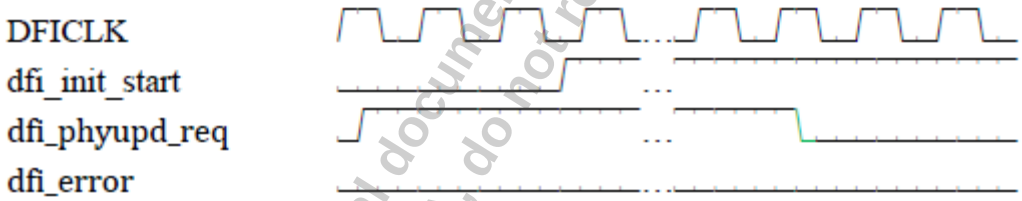
In the event that dfi_init_start is asserted, the state of the PHY update interface can safely be ignored. If the dfi_init_start is asserted prior to the controller observing the dfi_phyupd_req, the PHY will de-assert the dfi_phyupd_req prior to the frequency change or initialization being completed. The de-assertion will occur within 128 cycles of the assertion of dfi_init_start.

Figure 10-3 dfi_init_start prior to dfi_phyupd_req



If the dfi_init_start is asserted after the dfi_phyupd_req is asserted, the PHY may assert the dfi_error signal if the tphyupd_resp time has been violated. The error signal can be safely ignored in this case.

Figure 10-4 dfi_init_start after dfi_phyupd_req



Note In order to ensure continual proper operation of the memory system, it is recommended the dfi_phyupd_ack be deasserted by the memory controller within 8 Dfi clock cycles of the deassertion of dfi_phyupd_req.

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10.5.3 PHY Update Interface Timing Parameters

For PHY timing parameters for the update interface requests, refer to "PUB Parameters" on page 112.

10.5.4 Collisions Between PHY Update and DFI LP

The intention of the dfi_error behavior is to provide a complete solution that prevents lock-up. If the memory controller does not violate tphyupd_resp, then the assertion of the error is not an issue. If there is a collision between DFI LP and PHY update, both behave normally.

If dfi_phyupd_req is asserted when dfi_init_start is asserted for a frequency or power state, then dfi_phyupd_req is deasserted before deasserting dfi_init_complete. dfi_init_start is always taken as a higher priority and the update request stat machine is reset (and the request is dropped).

The purpose for the 128 cycles is to ensure that there is flexibility in the pipelining of the interfaces. The update and frequency change interfaces are not intended to be low latency and high performance interfaces. If the dfi_init_start is asserted, there is a chance that dfi_phyupd_req could be asserted as seen by the memory controller. However, dfi_phyupd_req is deasserted before the PHY acknowledges the init_start. If the memory controller initiates a frequency/power-state change, then the PHY update interface can be ignored.

10.6 DFI Master Interface

As per the DFI specification the DFI PHY Master interface (PMI) is intended to facilitate various operations that require interruption of transmission on the DFI interface. The PHY Master Interface is used in LPDDR4 to initiate the Dram Drift Compensation operations. The PHY Master Interface uses internal timers to determine when the DRAM needs to be retrained. These timers are set up during the initialization process and are activated by frequency change operations on the DFI interface. There is a separate timer for each Pstate that is used when that Pstate is active. When the timer counts down to zero, it will request control of the DRAM by asserting the dfi_phymstr_req signal. Once the request has been acknowledged, it will perform the DDC operation and return the control of the DRAM to the memory controller automatically.

Attention For DDR4, the PHY Master Interface is not active.

Note
- For more information on DRAM Drift Tracking, please see the *DWC DDRPHY Training Application Note*.
- For more information on the operation of the PHY Master Interface and the requirements, refer to the DFI specification.

The DFI PHY Master Interface operation can be seen in the following waveform:

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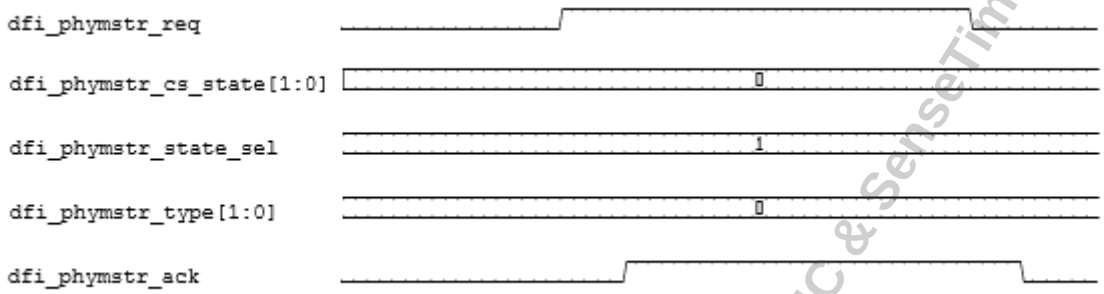
Figure 10-5 DFI PHY Master Interface Operation



When the dfi_phymstr_req signal is asserted, the other PHY master signals will always be set as:

- dfi_phymstr_cs_state[1:0] will always be set to 0
- dfi_phymstr_state_sel will always be set to 1
- dfi_phymstr_type[1:0] will always be set to 0

If the PHY Master Interface is enabled and the dfi_phymstr_ack signal is not asserted within $t_{phymstr\_resp}$ cycles after the dfi_phymstr_req signal is asserted, the dfi_error signal will be asserted (with dfi_error_info set to 4'b0001).

10.6.1 Two-channel Operation

Two-channel operation: Even though there are separate dfi0_phymstr_* and dfi1_phymstr_* signals, a DDC operation affects the entire PHY. Thus, after dfi0_phymstr_req and dfi1_phymstr_req are asserted, both MC channels must assert their dfi*phymstr_ack signals within the required interval to initiate a DDC. If either channel does not assert phymstr_ack within the interval, an error condition occurs.

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10.7 PHY DFI Sideband Interactions

The DFI 3.1 specification + 4.0v2 Addendum defines several sideband interfaces, but leaves some details about the precedence/interaction of these sidebands undefined or implementation specific.

The following section describes the expected behavior of the PHY and Memory Controller.

10.7.1 Supported DFI Sideband Interfaces

The PHY supports the following DFI Sideband interfaces [for full details on each interface, please refer to the appropriate section of the DFI Specification].

- DFI Frequency change Interface
  - This interface is used by the Memory Controller to Start the DFI interface at boot, or to request a frequency change
- Relevant Signals
  - dfi0_init_start, dfi0_init_complete, dfi0_freq[4:0], dfi0_freq_ratio[1:0]
  - dfi1_init_start, dfi1_init_complete, dfi1_freq[4:0], dfi1_freq_ratio[1:0]
- DFI Low Power Interface

  This interface is used by the Memory Controller to notify the PHY of extended traffic idle times that may also be used for entering PHY low power states
  - Relevant Signals
    - dfi0_lp_ctrl_req, dfi0_lp_data_req, dfi0_lp_wakeup[3:0], dfi0_lp_ack
    - dfi1_lp_ctrl_req, dfi1_lp_data_req, dfi1_lp_wakeup[3:0], dfi1_lp_ack
- DFI Controller Update Interface
  - This interface is used by the Memory Controller to notify the PHY of traffic idle times. The PHY uses these intervals to enable VT compensation updates for internal PHY delay lines and to reset the read-data fifo pointers.
  - Relevant Signals
    - dfi0_ctrlupd_req, dfi0_ctrlupd_ack
    - dfi1_ctrlupd_req, dfi1_ctrlupd_ack
- DFI PHY Update Interface
  - This interface is used by the PHY to request traffic idle times to enable VT compensation updates for internal PHY delay lines
  - Relevant Signals
    - dfi0_phyupd_req, dfi0_phyupd_type[1:0], dfi0_phyupd_ack
    - dfi1_phyupd_req, dfi1_phyupd_type[1:0], dfi1_phyupd_ack
- DFI PHY Master Interface
  - This interface is used by the PHY to request complete control of the memory bus to enable sequences to compensate for DRAM drift [e.g. drift in tDQSCK and tDQS2DQ in LPDDDR4]
  - Relevant Signals

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- dfi0_phymstr_req, dfi0_phymstr_type[1:0], df01_phymstr_state_sel, dfi0_phymstr_cs_state[1:0], dfi0_phymstr_ack
- dfi1_phymstr_req, dfi1_phymstr_type[1:0], dfi1_phymstr_state_sel, dfi1_phymstr_cs_state[1:0], dfi1_phymstr_ack

10.7.2 Multi-channel operation

In PHY configurations where the secondary DFI1 interface is enabled [please see `define DWC_DDRPHY_DFI1_EXISTS] the DFI sidebands are also replicated (dfi1_* vs. dfi0_*).

The following interfaces are completely independent between DFI0/DFI1, and have no interaction

- DFI Low Power
- DFI Controller Update
- DFI PHY Update

The following interfaces require acknowledgment by both DFI0/DFI1 channels, and are synchronized by the PHY

- DFI Frequency Change Interface
- DFI PHY Master Interface

10.7.2.1 Synchronization of DFI Init/Frequency Change Interface

Since the PHY has a single PLL shared among both DFI channels, the first DFI Init and subsequent frequency changes must occur for both channels in concert.

- The Memory Controller(s) may transition the dfi{0,1}_init_start signals at different times and in any order.
- The PHY will wait until both dfi{0,1}_init_start signals are at the same state before starting the first init or frequency change.
  - The PHY will remain in the wait state until both dfi{0,1}_init_start signals have transitioned.
- Since the PHY will execute frequency change at the same time for both channels, the dfi{0,1}_init_complete signals will be asserted by the PHY simultaneously.

The following figure shows the PHY behavior during the first DFI initialization.

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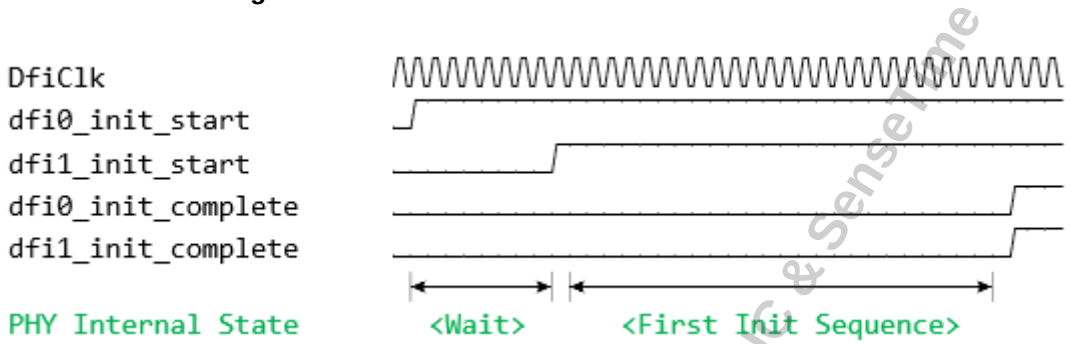
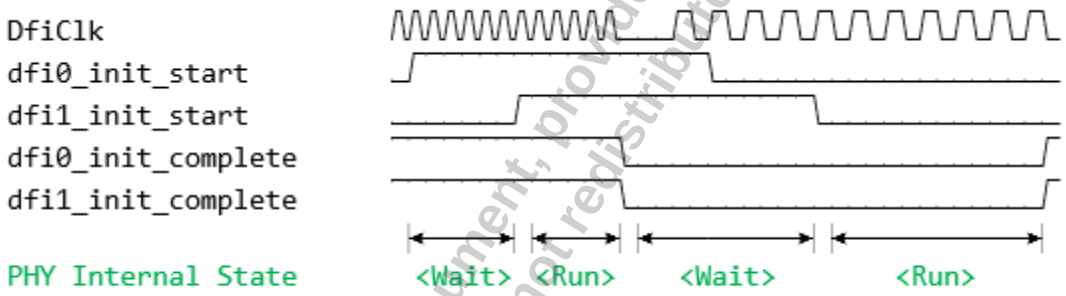
Figure 10-6 PHY Behavior During the First DFI Initialization



The following figure shows the PHY behavior during a DFI frequency change.

Figure 10-7 PHY Behavior During a DFI Frequency Change



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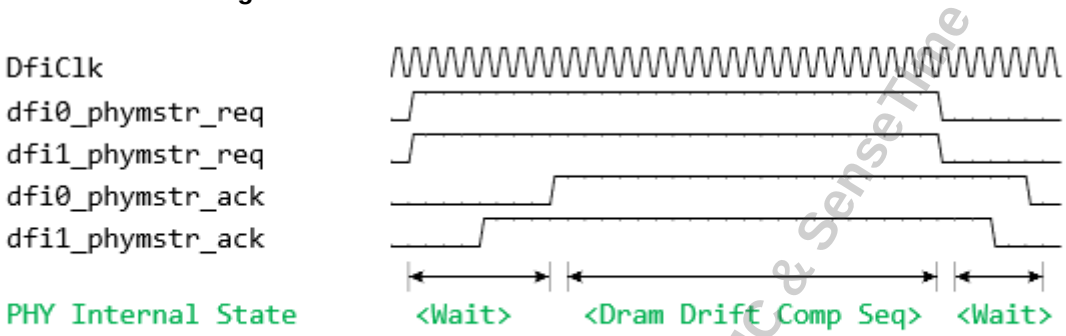
10.7.2.2 Synchronization of DFI PHY Master Interface

- Since the PHY has a single dram-drift-compensation engine for both DFI channels, the DFI PHY Master events for both channels must occur in concert.
- The PHY will assert the dfi{0,1}_phymstr_req signals simultaneously
- The Memory Controller(s) may acknowledge by asserting the dfi{0,1}_phymstr_ack signals in any order.
- The PHY will wait until both dfi{0,1}_phymstr_ack signals are asserted. When both acknowledges are received by the PHY, the internal dram-drift-compensation sequence will start.
- After the dram-drift compensation sequence is complete, the PHY will de-assert both dfi{0,1}_phymstr_req signals in the same cycle.
- The Memory controller(s) may de-assert their respective dfi{0,1}_phymstr_ack signals in any order.

The following figure shows the PHY behavior during a DFI PHY Master Transaction.

Figure 10-8 PHY Behavior during a DFI PHY Master Transaction



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10.8 DFI Sideband Simultaneous Collisions

Since the DFI sideband requesters are a mix of the PHY and MC, there is the possibility that there will be collisions between the interfaces.

The following sidebands are initiated by the Memory Controller, and should not be requested simultaneously. That is, the asserting edge of the requests should not occur in the same DfiClk cycle.

- DFI Init/Frequency Change
- DFI Controller Update
- DFI Low Power

The following sidebands are initiated by the PHY. The PHY logic ensures that the following are not asserted in the same DfiClk cycle.

- DFI Phy Update
- DFI Phy Master

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The following table describes the expected behavior of the PHY and MC in case of simultaneous collisions of the sidebands.

Table 10-5 Expected Behavior of the PHY and MC in Case of Simultaneous Collisions of the Sidebands[1]

Description	DFI Init / Frequency Change	DFI Controller Update	DFI Low Power	DFI Phy Update	DFI Phy Master
DFI Init / Freq Change	- - - - - -	Illegal/Undefined. MC should not to this	Illegal/Undefined. MC should not to this	PHY will start the Freq. Change sequence. PHY deasserts dfi_phyupd_req	PHY will start the Freq. Change sequence. PHY deasserts dfi_phymstr_req
DFI Controller Update	- - - - - -	- - - - - -	PHY asserts dfi_ctrlupd_ack. PHY ignores dfi_lp request.	PHY asserts dfi_ctrlupd_ack. PHY de-asserts dfi_phyupd_req.	PHY asserts dfi_ctrlupd_ack. MC should acknowledge PHY master request after DFI Controller Update is complete
DFI Low Power	- - - - - -	- - - - - -	- - - - - -	These are independent – Both PHY/MC may acknowledge these requests	PHY asserts dfi_lp_ack. MC should acknowledge PHY master request after DFI Low Power transaction is complete
DFI Phy Update	- - - - - -	- - - - - -	- - - - - -	- - - - - -	PHY logic guarantees that this will not occur
DFI Phy Master	- - - - - -	- - - - - -	- - - - - -	- - - - - -	- - - - - -

1. dfi_*_{ack,req} will corresponds to the dfi{0,1}_*{ack,req} as appropriate

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10.8.1 DFI Sideband Sequential Collisions

Some sequential overlap of the sidebands are permitted/undefined by the DFI specification. The following table describes the expected behavior of the PHY and MC in case of simultaneous collisions of the sidebands.

Table 10-6 Expected Behavior of the PHY and MC in Case of Simultaneous Collisions of the Sidebands[1]

1st EVENT	2nd EVENT	DFI Init / Freq Change	DFI Controller Update	DFI Low Power	DFI Phy Update	DFI Phy Master
DFI Init / Freq Change		- - - - - -	Illegal/Undefined. MC should not to this	Illegal/Undefined. MC should not to this	PHY will start the Freq. Change sequence. PHY deasserts dfi_phyupd_req	PHY will start the Freq. Change sequence. PHY deasserts dfi_phymstr_req
DFI Controller Update		Illegal/Undefined. MC should complete Dfi_ctrlupd transaction before requesting Freq. Change	- - - - - -	PHY asserts dfi_ctrlupd_ack. PHY ignores dfi_lp request.	PHY asserts dfi_ctrlupd_ack. PHY de-asserts dfi_phyupd_req.	PHY asserts dfi_ctrlupd_ack. MC should acknowledge PHY master request after dfi_ctrlupd transaction is complete
DFI Low Power		Illegal/Undefined. MC should complete DFI_LP transaction before requesting Freq. Change	PHY asserts dfi_lp_ack. PHY ignores dfi_ctrlupd_req	- - - - - -	These are independent – Both PHY/MC may acknowledge these requests	PHY asserts dfi_lp_ack. MC should acknowledge PHY master request after dfi_lp transaction is complete
DFI Phy Update		If dfi_phyupd_ack=0 PHY will de-assert dfi_phyupd_req, & PHY will start Freq. Change sequence.	If dfi_phyupd_ack=0 PHY will de-assert dfi_phyupd_req. & PHY asserts dfi_ctrlupd_ack	These are independent – Both PHY & MC may acknowledge these requests	- - - - - -	This will not occur unless MC takes longer than 512 DFICLKs to service the outstanding Phy Update Request

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Table 10-6 Expected Behavior of the PHY and MC in Case of Simultaneous Collisions of the Sidebands[1]

1st EVENT	2nd EVENT	DFI Init / Freq Change	DFI Controller Update	DFI Low Power	DFI Phy Update	DFI Phy Master
DFI Phy Master		If dfi_phymstr_ack=0 PHY will de-assert dfi_phymstr_req. & PHY will start Freq. Change sequence. if dfi_phymstr_ack=1 , this combination is Illegal/Undefined	If dfi_phymstr_ack=0 PHY asserts dfi_ctrlupd_ack. MC should acknowledge PHY master request after dfi_ctrlupd transaction is complete if dfi_phymstr_ack=1 , this combination is Illegal/Undefined	If dfi_phymstr_ack=0 PHY asserts dfi_lp_ack. MC should acknowledge PHY master request after dfi_lp transaction is complete if dfi_phymstr_ack=1 , this combination is Illegal/Undefined	PHY logic guarantees that this will not occur	- - - - - -

1. dfi_*_{ack,req} will corresponds to the dfi{0,1}_*{ack,req} as appropriate

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11

Register Description

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This chapter describes the following:

- "Register Map Overview" on page 252
- "Register Address Map" on page 257
  - "DWC_DDRPHYA_ACSM Register Block Address Map" on page 257
  - "DWC_DDRPHYA_ANIB Register Block Address Map" on page 266
  - "DWC_DDRPHYA_APBONLY Register Block Address Map" on page 267
  - "DWC_DDRPHYA_DBYTE Register Block Address Map" on page 268
  - "DWC_DDRPHYA_DRTUB Register Block Address Map" on page 283
  - "DWC_DDRPHYA_INTENG Register Block Address Map" on page 284
  - "DWC_DDRPHYA_MASTER Register Block Address Map" on page 317
  - "DWC_DDRPHYA_PPGC Register Block Address Map" on page 331
- "Register Description" on page 334

11.1 Register Map Overview

The PHY utility block has registers that are used to configure, control or provide status of certain features of the PHY. The user accesses these registers using the configuration port write and read commands. "Register Address Map" on page 257 shows the address mapping of the PUB registers.

The following are PUB register rules:

- All register accesses over the APB in units of 16 bits, though the addressed register itself may be less then 16 bits wide.
- Values should not be written to registers that are marked reserved
- Values should not be written to undocumented addresses

The following sections describe the PUB registers in detail. Unless specified otherwise, control register bits are assumed active-high

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11.1.1 Register Address Overview

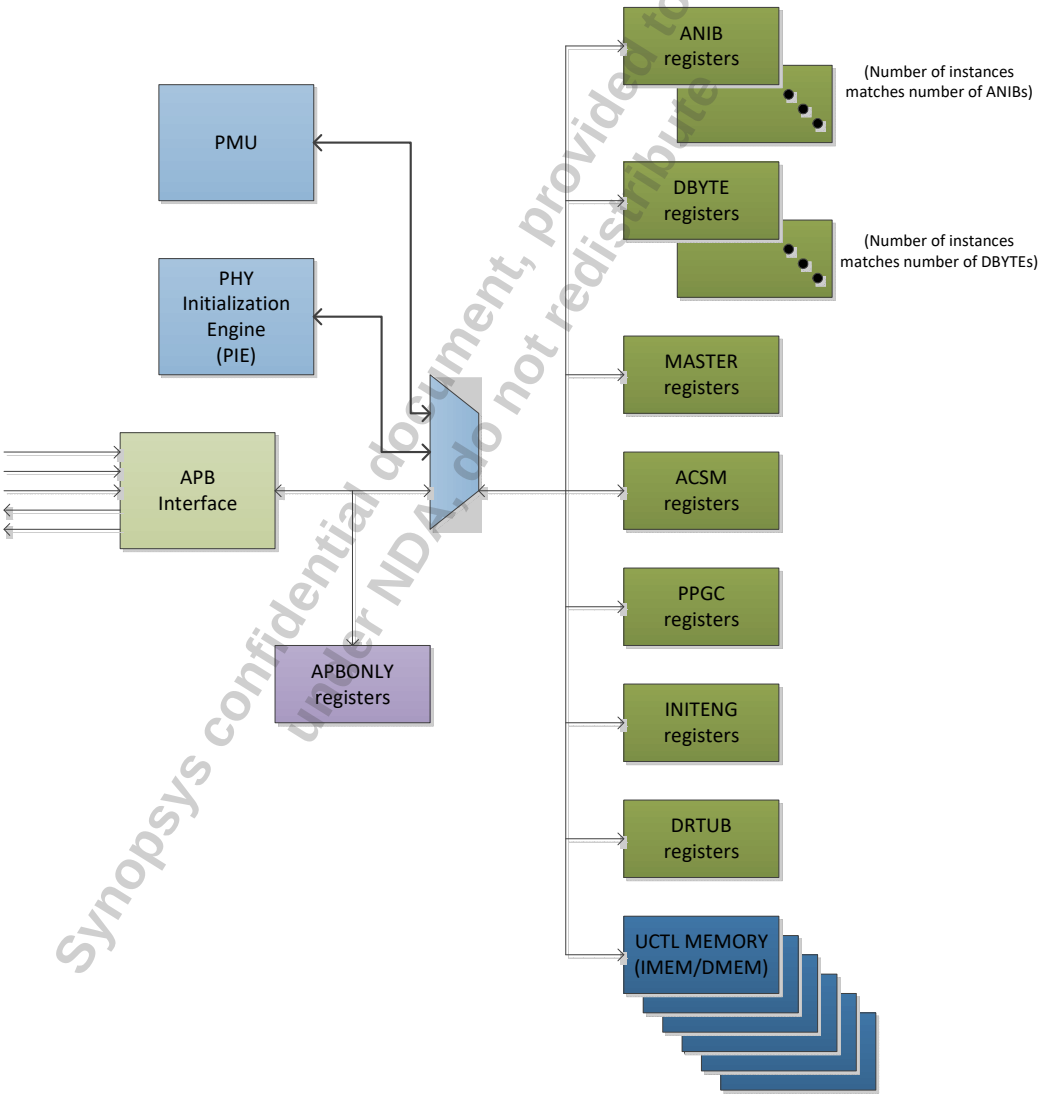
Sets of registers are in specific register-blocks. The register-block is a group of registers which are synthesized as one, share a common Verilog module, and respond to addresses for that kind of register-block. There may be multiple instances of each kind of register-block.

Note

- Register addresses are 23-bits wide
- The architecture supports the optional feature to broadcast same value to many registers during a write operation.

Refer to the "Register Address Map" on page 257 for all register blocks.

Figure 11-1 Block Diagram of Architecture for the CSRs



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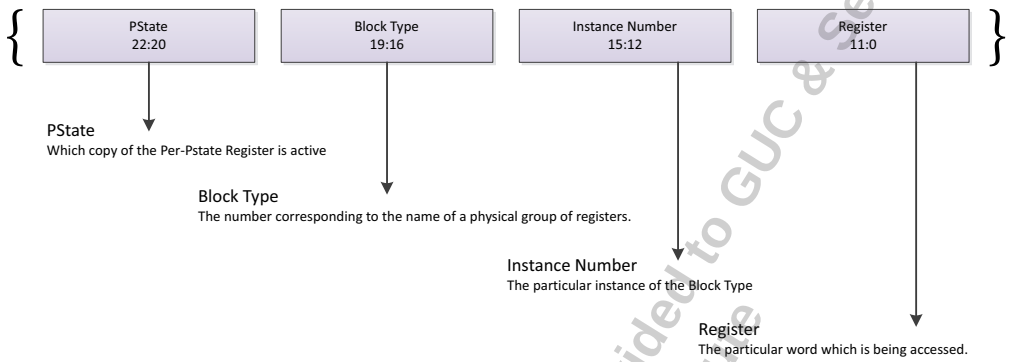
11.1.1.1 Specifying Register Addresses

The 23 bit register address is specified by the concatenation of the following fields: {PState, Block Type, Instance Number, Register}.

Figure 11-2 Register Fields Used in Addressing



The following sections describe the fields in detail.

11.1.1.1.1 PState

PState: Certain registers have four copies, one per PState. Each copy can be accessed individually by setting the PState field appropriately. Registers which are not copied per P-state exist at Pstate0.

- PState = 3'b000 : PState0
- PState = 3'b001 : PState1
- PState = 3'b010 : PState2
- PState = 3'b011 : PState3
- PState = 3'b111 : Broadcast to all PStates.

In an operational PHY, only one set of PState registers is active at a time. The PState is the operating point of the PHY (that is, the particular frequency/power operating point to which is configured).

See register PState in the MASTER register block for information on moving between Pstates.

11.1.1.1.2 Block Type

Block Type: Registers are grouped together in blocks, for reasons of physical proximity and ease of replication where more than one set is needed. For example, there is one register per DBYTE and there are multiple DBYTEs. Bits [19:16] specify the block-type, according to the following table:

- Block Type = 4'h0: ANIB
- Block Type = 4'h1: DBYTE
- Block Type = 4'h2: MASTER
- Block Type = 4'h4: ACSM
- Block Type = 4'h5: UCTL MEMORY
- Block Type = 4'h7: PPGC
- Block Type = 4'h9 : INITENG
- Block Type = 4'hC : PUB

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- Block Type = 4'hD : APBONLY

11.1.1.1.3 Instance Number

Instance Number: This field specifies which instance of a block-type is being addressed. For most block-types there is only one instance and so this field must be set to 4'h0. For the DBYTE and ANIB types there may be more than one instance, the number depending upon the construction of the PUB.

- Instance Number = 4'h0: Instance 0 of specified Block Type.
- Instance Number = 4'h1: Instance 1 of specified Block Type, if it exists.
- Instance Number = 4'hN: Instance N of specified Block Type, if it exists.
- Instance Number = 4'hF: All instances of specified Block Type.

11.1.1.1.4 Register

Register: This 12 bit field specifies the particular register which is being accessed.

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11.1.2 Register Access Types

Each CSR has Type field which describes what operations are permitted on that register. The following list shows the encodings for this field.

- R/W: The majority of registers are R/W. Read and write by software, read only by the hardware.
- R: Read-only by software; read-write by hardware

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11.2 Register Address Map

11.2.1 DWC_DDRPHYA_ACSM Register Block Address Map

Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
0	040000	AcsmSeq0x0	R/W	Reserved for PHY training firmware use.
1	040001	AcsmSeq0x1	R/W	Reserved for PHY training firmware use.
2	040002	AcsmSeq0x2	R/W	Reserved for PHY training firmware use.
3	040003	AcsmSeq0x3	R/W	Reserved for PHY training firmware use.
4	040004	AcsmSeq0x4	R/W	Reserved for PHY training firmware use.
5	040005	AcsmSeq0x5	R/W	Reserved for PHY training firmware use.
6	040006	AcsmSeq0x6	R/W	Reserved for PHY training firmware use.
7	040007	AcsmSeq0x7	R/W	Reserved for PHY training firmware use.
8	040008	AcsmSeq0x8	R/W	Reserved for PHY training firmware use.
9	040009	AcsmSeq0x9	R/W	Reserved for PHY training firmware use.
10	04000A	AcsmSeq0x10	R/W	Reserved for PHY training firmware use.
11	04000B	AcsmSeq0x11	R/W	Reserved for PHY training firmware use.
12	04000C	AcsmSeq0x12	R/W	Reserved for PHY training firmware use.
13	04000D	AcsmSeq0x13	R/W	Reserved for PHY training firmware use.
14	04000E	AcsmSeq0x14	R/W	Reserved for PHY training firmware use.
15	04000F	AcsmSeq0x15	R/W	Reserved for PHY training firmware use.
16	040010	AcsmSeq0x16	R/W	Reserved for PHY training firmware use.
17	040011	AcsmSeq0x17	R/W	Reserved for PHY training firmware use.
18	040012	AcsmSeq0x18	R/W	Reserved for PHY training firmware use.
19	040013	AcsmSeq0x19	R/W	Reserved for PHY training firmware use.
20	040014	AcsmSeq0x20	R/W	Reserved for PHY training firmware use.
21	040015	AcsmSeq0x21	R/W	Reserved for PHY training firmware use.
22	040016	AcsmSeq0x22	R/W	Reserved for PHY training firmware use.
23	040017	AcsmSeq0x23	R/W	Reserved for PHY training firmware use.
24	040018	AcsmSeq0x24	R/W	Reserved for PHY training firmware use.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
25	040019	AcsmSeq0x25	R/W	Reserved for PHY training firmware use.
26	04001A	AcsmSeq0x26	R/W	Reserved for PHY training firmware use.
27	04001B	AcsmSeq0x27	R/W	Reserved for PHY training firmware use.
28	04001C	AcsmSeq0x28	R/W	Reserved for PHY training firmware use.
29	04001D	AcsmSeq0x29	R/W	Reserved for PHY training firmware use.
30	04001E	AcsmSeq0x30	R/W	Reserved for PHY training firmware use.
31	04001F	AcsmSeq0x31	R/W	Reserved for PHY training firmware use.
32	040020	AcsmSeq1x0	R/W	Reserved for PHY training firmware use.
33	040021	AcsmSeq1x1	R/W	Reserved for PHY training firmware use.
34	040022	AcsmSeq1x2	R/W	Reserved for PHY training firmware use.
35	040023	AcsmSeq1x3	R/W	Reserved for PHY training firmware use.
36	040024	AcsmSeq1x4	R/W	Reserved for PHY training firmware use.
37	040025	AcsmSeq1x5	R/W	Reserved for PHY training firmware use.
38	040026	AcsmSeq1x6	R/W	Reserved for PHY training firmware use.
39	040027	AcsmSeq1x7	R/W	Reserved for PHY training firmware use.
40	040028	AcsmSeq1x8	R/W	Reserved for PHY training firmware use.
41	040029	AcsmSeq1x9	R/W	Reserved for PHY training firmware use.
42	04002A	AcsmSeq1x10	R/W	Reserved for PHY training firmware use.
43	04002B	AcsmSeq1x11	R/W	Reserved for PHY training firmware use.
44	04002C	AcsmSeq1x12	R/W	Reserved for PHY training firmware use.
45	04002D	AcsmSeq1x13	R/W	Reserved for PHY training firmware use.
46	04002E	AcsmSeq1x14	R/W	Reserved for PHY training firmware use.
47	04002F	AcsmSeq1x15	R/W	Reserved for PHY training firmware use.
48	040030	AcsmSeq1x16	R/W	Reserved for PHY training firmware use.
49	040031	AcsmSeq1x17	R/W	Reserved for PHY training firmware use.
50	040032	AcsmSeq1x18	R/W	Reserved for PHY training firmware use.
51	040033	AcsmSeq1x19	R/W	Reserved for PHY training firmware use.
52	040034	AcsmSeq1x20	R/W	Reserved for PHY training firmware use.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
53	040035	AcsmSeq1x21	R/W	Reserved for PHY training firmware use.
54	040036	AcsmSeq1x22	R/W	Reserved for PHY training firmware use.
55	040037	AcsmSeq1x23	R/W	Reserved for PHY training firmware use.
56	040038	AcsmSeq1x24	R/W	Reserved for PHY training firmware use.
57	040039	AcsmSeq1x25	R/W	Reserved for PHY training firmware use.
58	04003A	AcsmSeq1x26	R/W	Reserved for PHY training firmware use.
59	04003B	AcsmSeq1x27	R/W	Reserved for PHY training firmware use.
60	04003C	AcsmSeq1x28	R/W	Reserved for PHY training firmware use.
61	04003D	AcsmSeq1x29	R/W	Reserved for PHY training firmware use.
62	04003E	AcsmSeq1x30	R/W	Reserved for PHY training firmware use.
63	04003F	AcsmSeq1x31	R/W	Reserved for PHY training firmware use.
64	040040	AcsmSeq2x0	R/W	Reserved for PHY training firmware use.
65	040041	AcsmSeq2x1	R/W	Reserved for PHY training firmware use.
66	040042	AcsmSeq2x2	R/W	Reserved for PHY training firmware use.
67	040043	AcsmSeq2x3	R/W	Reserved for PHY training firmware use.
68	040044	AcsmSeq2x4	R/W	Reserved for PHY training firmware use.
69	040045	AcsmSeq2x5	R/W	Reserved for PHY training firmware use.
70	040046	AcsmSeq2x6	R/W	Reserved for PHY training firmware use.
71	040047	AcsmSeq2x7	R/W	Reserved for PHY training firmware use.
72	040048	AcsmSeq2x8	R/W	Reserved for PHY training firmware use.
73	040049	AcsmSeq2x9	R/W	Reserved for PHY training firmware use.
74	04004A	AcsmSeq2x10	R/W	Reserved for PHY training firmware use.
75	04004B	AcsmSeq2x11	R/W	Reserved for PHY training firmware use.
76	04004C	AcsmSeq2x12	R/W	Reserved for PHY training firmware use.
77	04004D	AcsmSeq2x13	R/W	Reserved for PHY training firmware use.
78	04004E	AcsmSeq2x14	R/W	Reserved for PHY training firmware use.
79	04004F	AcsmSeq2x15	R/W	Reserved for PHY training firmware use.
80	040050	AcsmSeq2x16	R/W	Reserved for PHY training firmware use.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
81	040051	AcsmSeq2x17	R/W	Reserved for PHY training firmware use.
82	040052	AcsmSeq2x18	R/W	Reserved for PHY training firmware use.
83	040053	AcsmSeq2x19	R/W	Reserved for PHY training firmware use.
84	040054	AcsmSeq2x20	R/W	Reserved for PHY training firmware use.
85	040055	AcsmSeq2x21	R/W	Reserved for PHY training firmware use.
86	040056	AcsmSeq2x22	R/W	Reserved for PHY training firmware use.
87	040057	AcsmSeq2x23	R/W	Reserved for PHY training firmware use.
88	040058	AcsmSeq2x24	R/W	Reserved for PHY training firmware use.
89	040059	AcsmSeq2x25	R/W	Reserved for PHY training firmware use.
90	04005A	AcsmSeq2x26	R/W	Reserved for PHY training firmware use.
91	04005B	AcsmSeq2x27	R/W	Reserved for PHY training firmware use.
92	04005C	AcsmSeq2x28	R/W	Reserved for PHY training firmware use.
93	04005D	AcsmSeq2x29	R/W	Reserved for PHY training firmware use.
94	04005E	AcsmSeq2x30	R/W	Reserved for PHY training firmware use.
95	04005F	AcsmSeq2x31	R/W	Reserved for PHY training firmware use.
96	040060	AcsmSeq3x0	R/W	Reserved for PHY training firmware use.
97	040061	AcsmSeq3x1	R/W	Reserved for PHY training firmware use.
98	040062	AcsmSeq3x2	R/W	Reserved for PHY training firmware use.
99	040063	AcsmSeq3x3	R/W	Reserved for PHY training firmware use.
100	040064	AcsmSeq3x4	R/W	Reserved for PHY training firmware use.
101	040065	AcsmSeq3x5	R/W	Reserved for PHY training firmware use.
102	040066	AcsmSeq3x6	R/W	Reserved for PHY training firmware use.
103	040067	AcsmSeq3x7	R/W	Reserved for PHY training firmware use.
104	040068	AcsmSeq3x8	R/W	Reserved for PHY training firmware use.
105	040069	AcsmSeq3x9	R/W	Reserved for PHY training firmware use.
106	04006A	AcsmSeq3x10	R/W	Reserved for PHY training firmware use.
107	04006B	AcsmSeq3x11	R/W	Reserved for PHY training firmware use.
108	04006C	AcsmSeq3x12	R/W	Reserved for PHY training firmware use.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
109	04006D	AcsmSeq3x13	R/W	Reserved for PHY training firmware use.
110	04006E	AcsmSeq3x14	R/W	Reserved for PHY training firmware use.
111	04006F	AcsmSeq3x15	R/W	Reserved for PHY training firmware use.
112	040070	AcsmSeq3x16	R/W	Reserved for PHY training firmware use.
113	040071	AcsmSeq3x17	R/W	Reserved for PHY training firmware use.
114	040072	AcsmSeq3x18	R/W	Reserved for PHY training firmware use.
115	040073	AcsmSeq3x19	R/W	Reserved for PHY training firmware use.
116	040074	AcsmSeq3x20	R/W	Reserved for PHY training firmware use.
117	040075	AcsmSeq3x21	R/W	Reserved for PHY training firmware use.
118	040076	AcsmSeq3x22	R/W	Reserved for PHY training firmware use.
119	040077	AcsmSeq3x23	R/W	Reserved for PHY training firmware use.
120	040078	AcsmSeq3x24	R/W	Reserved for PHY training firmware use.
121	040079	AcsmSeq3x25	R/W	Reserved for PHY training firmware use.
122	04007A	AcsmSeq3x26	R/W	Reserved for PHY training firmware use.
123	04007B	AcsmSeq3x27	R/W	Reserved for PHY training firmware use.
124	04007C	AcsmSeq3x28	R/W	Reserved for PHY training firmware use.
125	04007D	AcsmSeq3x29	R/W	Reserved for PHY training firmware use.
126	04007E	AcsmSeq3x30	R/W	Reserved for PHY training firmware use.
127	04007F	AcsmSeq3x31	R/W	Reserved for PHY training firmware use.
128-131	040080 140080 240080 340080	AcsmPlayback0x0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
132-135	040081 140081 240081 340081	AcsmPlayback1x0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
136-139	040082 140082 240082 340082	AcsmPlayback0x1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
140-143	040083 140083 240083 340083	AcsmPlayback1x1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
144-147	040084 140084 240084 340084	AcsmPlayback0x2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
148-151	040085 140085 240085 340085	AcsmPlayback1x2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
152-155	040086 140086 240086 340086	AcsmPlayback0x3	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
156-159	040087 140087 240087 340087	AcsmPlayback1x3	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
160-163	040088 140088 240088 340088	AcsmPlayback0x4	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
164-167	040089 140089 240089 340089	AcsmPlayback1x4	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
168-171	04008A 14008A 24008A 34008A	AcsmPlayback0x5	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
172-175	04008B 14008B 24008B 34008B	AcsmPlayback1x5	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
176-179	04008C 14008C 24008C 34008C	AcsmPlayback0x6	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
180-183	04008D 14008D 24008D 34008D	AcsmPlayback1x6	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
184-187	04008E 14008E 24008E 34008E	AcsmPlayback0x7	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
188-191	04008F 14008F 24008F 34008F	AcsmPlayback1x7	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
192	040090	AcsmPStateOvrEn	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for Controling Playback Engine
193	040091	AcsmPStateOvrVal	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for Controling Playback Engine
194	0400C0	AcsmCtrl23	R/W	Reserved for PHY training firmware use.
195	0400C2	AcsmCkeVal	R/W	Reserved for PHY training firmware use.
196	0400C8	LowSpeedClockDivider	R/W	Reserved for PHY training firmware use.
197	0400D0	AcsmCsMapCtrl0	R/W	Reserved for PHY training firmware use.
198	0400D1	AcsmCsMapCtrl1	R/W	Reserved for PHY training firmware use.
199	0400D2	AcsmCsMapCtrl2	R/W	Reserved for PHY training firmware use.
200	0400D3	AcsmCsMapCtrl3	R/W	Reserved for PHY training firmware use.
201	0400D4	AcsmCsMapCtrl4	R/W	Reserved for PHY training firmware use.
202	0400D5	AcsmCsMapCtrl5	R/W	Reserved for PHY training firmware use.
203	0400D6	AcsmCsMapCtrl6	R/W	Reserved for PHY training firmware use.
204	0400D7	AcsmCsMapCtrl7	R/W	Reserved for PHY training firmware use.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
205	0400D8	AcsmCsMapCtrl8	R/W	Reserved for PHY training firmware use.
206	0400D9	AcsmCsMapCtrl9	R/W	Reserved for PHY training firmware use.
207	0400DA	AcsmCsMapCtrl10	R/W	Reserved for PHY training firmware use.
208	0400DB	AcsmCsMapCtrl11	R/W	Reserved for PHY training firmware use.
209	0400DC	AcsmCsMapCtrl12	R/W	Reserved for PHY training firmware use.
210	0400DD	AcsmCsMapCtrl13	R/W	Reserved for PHY training firmware use.
211	0400DE	AcsmCsMapCtrl14	R/W	Reserved for PHY training firmware use.
212	0400DF	AcsmCsMapCtrl15	R/W	Reserved for PHY training firmware use.
213	0400E0	AcsmOdtCtrl0	R/W	Reserved for PHY training firmware use.
214	0400E1	AcsmOdtCtrl1	R/W	Reserved for PHY training firmware use.
215	0400E2	AcsmOdtCtrl2	R/W	Reserved for PHY training firmware use.
216	0400E3	AcsmOdtCtrl3	R/W	Reserved for PHY training firmware use.
217	0400E4	AcsmOdtCtrl4	R/W	Reserved for PHY training firmware use.
218	0400E5	AcsmOdtCtrl5	R/W	Reserved for PHY training firmware use.
219	0400E6	AcsmOdtCtrl6	R/W	Reserved for PHY training firmware use.
220	0400E7	AcsmOdtCtrl7	R/W	Reserved for PHY training firmware use.
221	0400E8	AcsmOdtCtrl8	R/W	Reserved for PHY training firmware use.
222	0400E9	AcsmCtrl16	R/W	Reserved for PHY training firmware use.
223	0400EA	LowSpeedClockStopVal	R/W	Reserved for PHY training firmware use.
224	0400EB	AcsmCtrl18	R	Reserved for PHY training firmware use.
225	0400EC	AcsmCtrl19	R/W	Reserved for PHY training firmware use.
226	0400ED	AcsmCtrl20	R	Reserved for PHY training firmware use.
227	0400EE	AcsmCtrl21	R/W	Reserved for PHY training firmware use.
228	0400EF	AcsmCtrl22	R/W	Reserved for PHY training firmware use.
229	0400F0	AcsmCtrl0	R/W	Reserved for PHY training firmware use.
230	0400F1	AcsmCtrl1	R/W	Reserved for PHY training firmware use.
231	0400F2	AcsmCtrl2	R/W	Reserved for PHY training firmware use.
232	0400F3	AcsmCtrl3	R/W	Reserved for PHY training firmware use.

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Table 11-1 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ACSM (type = 0x4), instance 0

Register Number	Address	Name	Access	Description
233	0400F4	AcsmCtrl4	R/W	Reserved for PHY training firmware use.
234	0400F5	AcsmCtrl5	R/W	Reserved for PHY training firmware use.
235	0400F6	AcsmCtrl6	R/W	Reserved for PHY training firmware use.
236	0400F7	AcsmCtrl7	R/W	Reserved for PHY training firmware use.
237	0400F8	AcsmCtrl8	R/W	Reserved for PHY training firmware use.
238	0400F9	AcsmCtrl9	R/W	Reserved for PHY training firmware use.
239	0400FA	AcsmCtrl10	R/W	Reserved for PHY training firmware use.
240	0400FB	AcsmCtrl11	R/W	Reserved for PHY training firmware use.
241	0400FC	AcsmCtrl12	R/W	Reserved for PHY training firmware use.
242	0400FD	AcsmCtrl13	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
243	0400FE	AcsmCtrl14	R/W	Reserved for PHY training firmware use.
244	0400FF	AcsmCtrl15	R/W	Reserved for PHY training firmware use.

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11.2.2 DWC_DDRPHYA_ANIB Register Block Address Map

Table 11-2 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_ANIB (type = 0x0), instances 0..`DWC_DDRPHYA_ANIBS_{N}-1

Register Number	Address	Name	Access	Description
245	00001A	MtestMuxSel	R/W	"Register Name: MtestMuxSel Register-block: DWC_DDRPHYA_ANIB,DBYTE,MASTER" on page 341
246	000027	AForceDrvCont	R/W	"Register Name: AForceDrvCont Register-block: DWC_DDRPHYA_ANIB" on page 334
247	000028	AForceTriCont	R/W	"Register Name: AForceTriCont Register-block: DWC_DDRPHYA_ANIB" on page 335
248	000043	ATxImpedance	R/W	"Register Name: ATxImpedance Register-block: DWC_DDRPHYA_ANIB" on page 336
249	000053	ATestPrbsErr	R	"Register Name: ATestPrbsErr Register-block: DWC_DDRPHYA_ANIB" on page 337
250	000055	ATxSlewRate	R/W	"Register Name: ATxSlewRate Register-block: DWC_DDRPHYA_ANIB" on page 338
251	000056	ATestPrbsErrCnt	R	"Register Name: ATestPrbsErrCnt Register-block: DWC_DDRPHYA_ANIB" on page 339
252-255	000080 100080 200080 300080	ATxDly	R/W	"Register Name: ATxDly Register-block: DWC_DDRPHYA_ANIB" on page 340

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11.2.3 DWC_DDRPHYA_APBONLY Register Block Address Map

Table 11-3 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_APBONLY (type = 0xd), instance 0

Register Number	Address	Name	Access	Description
256	0D0000	MicroContMuxSel	R/W	"Register Name: MicroContMuxSel Register-block: DWC_DDRPHYA_APBONLY" on page 342
257	0D0004	UctShadowRegs	R	"Register Name: UctShadowRegs Register-block: DWC_DDRPHYA_APBONLY" on page 343
258	0D0030	DctWriteOnly	R/W	"Register Name: DctWriteOnly Register-block: DWC_DDRPHYA_APBONLY" on page 344
259	0D0031	DctWriteProt	R/W	"Register Name: DctWriteProt Register-block: DWC_DDRPHYA_APBONLY" on page 345
260	0D0032	UctWriteOnlyShadow	R	"Register Name: UctWriteOnlyShadow Register-block: DWC_DDRPHYA_APBONLY" on page 346
261	0D0034	UctDatWriteOnlyShadow	R	"Register Name: UctDatWriteOnlyShadow Register-block: DWC_DDRPHYA_APBONLY" on page 347
262	0D0035	NeverGateCsrClock	R/W	Reserved for PHY training firmware use.
263	0D0037	DfiCfgRdDataValidTicks	R/W	"Register Name: DfiCfgRdDataValidTicks Register-block: DWC_DDRPHYA_APBONLY" on page 348
264	0D0099	MicroReset	R/W	"Register Name: MicroReset Register-block: DWC_DDRPHYA_APBONLY" on page 349
265	0D00E7	SequencerOverride	R/W	Reserved for PHY training firmware use.
266	0D00FA	DfiInitCompleteShadow	R	"Register Name: DfiInitCompleteShadow Register-block: DWC_DDRPHYA_APBONLY" on page 350

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11.2.4 DWC_DDRPHYA_DBYTE Register Block Address Map

Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
267	010000	DbyteMiscMode	R/W	"Register Name: DbyteMiscMode Register-block: DWC_DDRPHYA_DBYTE" on page 351
268	010001	TsmByte0	R/W	Reserved for PHY training firmware use.
269	010002	TrainingParam	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
270-273	010003 110003 210003 310003	UseDqsEnReplica	R/W	Reserved for PHY training firmware use.
274	010010	RxTrainPatternEnable	R/W	Reserved for PHY training firmware use.
275	010011	TsmByte1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
276	010012	TsmByte2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
277	010013	TsmByte3	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() for protocols that support DRAM drift compensation.
278	010014	TsmByte4	R/W	Reserved for PHY training firmware use.
279	010017	TestModeConfig	R/W	Reserved for PHY test firmware use.
280	010018	TsmByte5	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
281	01001A	MtestMuxSel	R/W	"Register Name: MtestMuxSel Register-block: DWC_DDRPHYA_ANIB,DBYTE,MASTER" on page 341
282	01001F	DtsmTrainModeCtrl	R/W	Reserved for PHY training firmware use.
283-286	010020 110020 210020 310020	DFIMRL	R/W	"Register Name: DFIMRL Register-block: DWC_DDRPHYA_DBYTE" on page 380

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
287	010024	AsyncDbyteMode	R/W	Reserved for PHY training firmware use.
288	010026	AsyncDbyteTxEn	R/W	Reserved for PHY training firmware use.
289	010028	AsyncDbyteTxData	R/W	Reserved for PHY training firmware use.
290	01002A	AsyncDbyteRxData	R	Reserved for PHY training firmware use.
291-299	010030 010130 010230 010330 010430 010530 010630 010730 010830	VrefDAC1	R/W	“Register Name: VrefDAC1 Register-block: DWC_DDRPHYA_DBYTE” on page 370
300-308	010032 010132 010232 010332 010432 010532 010632 010732 010832	TrainingCntr	R/W	Reserved for PHY training firmware use.
309-317	010040 010140 010240 010340 010440 010540 010640 010740 010840	VrefDAC0	R/W	“Register Name: VrefDAC0 Register-block: DWC_DDRPHYA_DBYTE” on page 371

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
318-325	010041 010141 110041 110141 210041 210141 310041 310141	TxImpedanceCtrl0	R/W	"Register Name: TxImpedanceCtrl0 Register-block: DWC_DDRPHYA_DBYTE" on page 383
326-333	010043 010143 110043 110143 210043 210143 310043 310143	DqDqsRcvCntrl	R/W	"Register Name: DqDqsRcvCntrl Register-block: DWC_DDRPHYA_DBYTE" on page 384
334-337	010048 110048 210048 310048	TxEqualizationMode	R/W	"Register Name: TxEqualizationMode Register-block: DWC_DDRPHYA_DBYTE" on page 381
338-345	010049 010149 110049 110149 210049 210149 310049 310149	TxImpedanceCtrl1	R/W	"Register Name: TxImpedanceCtrl1 Register-block: DWC_DDRPHYA_DBYTE" on page 386
346	01004A	DqDqsRcvCntrl1	R/W	"Register Name: DqDqsRcvCntrl1 Register-block: DWC_DDRPHYA_DBYTE" on page 352
347-354	01004B 01014B 11004B 11014B 21004B 21014B 31004B 31014B	TxImpedanceCtrl2	R/W	"Register Name: TxImpedanceCtrl2 Register-block: DWC_DDRPHYA_DBYTE" on page 388

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
355-358	01004C 11004C 21004C 31004C	DqDqsRcvCntrl2	R/W	"Register Name: DqDqsRcvCntrl2 Register-block: DWC_DDRPHYA_DBYTE" on page 382
359-366	01004D 01014D 11004D 11014D 21004D 21014D 31004D 31014D	TxOdtDrvStren	R/W	"Register Name: TxOdtDrvStren Register-block: DWC_DDRPHYA_DBYTE" on page 389
367	010056	RxFifoCheckStatus	R	"Register Name: RxFifoCheckStatus Register-block: DWC_DDRPHYA_DBYTE" on page 353
368	010057	RxFifoCheckErrValues	R	"Register Name: RxFifoCheckErrValues Register-block: DWC_DDRPHYA_DBYTE" on page 354
369	010058	RxFifoInfo	R	"Register Name: RxFifoInfo Register-block: DWC_DDRPHYA_DBYTE" on page 355
370	010059	RxFifoVisibility	R/W	"Register Name: RxFifoVisibility Register-block: DWC_DDRPHYA_DBYTE" on page 357
371	01005A	RxFifoContentsDQ3210	R	"Register Name: RxFifoContentsDQ3210 Register-block: DWC_DDRPHYA_DBYTE" on page 358
372	01005B	RxFifoContentsDQ7654	R	"Register Name: RxFifoContentsDQ7654 Register-block: DWC_DDRPHYA_DBYTE" on page 359
373	01005C	RxFifoContentsDBI	R	"Register Name: RxFifoContentsDBI Register-block: DWC_DDRPHYA_DBYTE" on page 360
374-381	01005F 01015F 11005F 11015F 21005F 21015F 31005F 31015F	TxSlewRate	R/W	"Register Name: TxSlewRate Register-block: DWC_DDRPHYA_DBYTE" on page 391

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
382-390	010062 010162 010262 010362 010462 010562 010662 010762 010862	TrainingIncDecDtsmEn	R/W	Reserved for PHY training firmware use.
391-399	010068 010168 010268 010368 010468 010568 010668 010768 010868	RxPBDlyTg0	R/W	"Register Name: RxPBDlyTg0 Register-block: DWC_DDRPHYA_DBYTE" on page 373
400-408	010069 010169 010269 010369 010469 010569 010669 010769 010869	RxPBDlyTg1	R/W	"Register Name: RxPBDlyTg1 Register-block: DWC_DDRPHYA_DBYTE" on page 375
409-417	01006A 01016A 01026A 01036A 01046A 01056A 01066A 01076A 01086A	RxPBDlyTg2	R/W	"Register Name: RxPBDlyTg2 Register-block: DWC_DDRPHYA_DBYTE" on page 377

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
418-426	01006B 01016B 01026B 01036B 01046B 01056B 01066B 01076B 01086B	RxPBDlyTg3	R/W	“Register Name: RxPBDlyTg3 Register-block: DWC_DDRPHYA_DBYTE” on page 379
427-434	010080 010180 110080 110180 210080 210180 310080 310180	RxEnDlyTg0	R/W	“Register Name: RxEnDlyTg0 Register-block: DWC_DDRPHYA_DBYTE” on page 396
435-442	010081 010181 110081 110181 210081 210181 310081 310181	RxEnDlyTg1	R/W	“Register Name: RxEnDlyTg1 Register-block: DWC_DDRPHYA_DBYTE” on page 397
443-450	010082 010182 110082 110182 210082 210182 310082 310182	RxEnDlyTg2	R/W	“Register Name: RxEnDlyTg2 Register-block: DWC_DDRPHYA_DBYTE” on page 398

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
451-458	010083 010183 110083 110183 210083 210183 310083 310183	RxEnDlyTg3	R/W	"Register Name: RxEnDlyTg3 Register-block: DWC_DDRPHYA_DBYTE" on page 399
459-466	01008C 01018C 11008C 11018C 21008C 21018C 31008C 31018C	RxClkDlyTg0	R/W	"Register Name: RxClkDlyTg0 Register-block: DWC_DDRPHYA_DBYTE" on page 400
467-474	01008D 01018D 11008D 11018D 21008D 21018D 31008D 31018D	RxClkDlyTg1	R/W	"Register Name: RxClkDlyTg1 Register-block: DWC_DDRPHYA_DBYTE" on page 401
475-482	01008E 01018E 11008E 11018E 21008E 21018E 31008E 31018E	RxClkDlyTg2	R/W	"Register Name: RxClkDlyTg2 Register-block: DWC_DDRPHYA_DBYTE" on page 402

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
483-490	01008F 01018F 11008F 11018F 21008F 21018F 31008F 31018F	RxClkDlyTg3	R/W	“Register Name: RxClkDlyTg3 Register-block: DWC_DDRPHYA_DBYTE” on page 403
491-498	010090 010190 110090 110190 210090 210190 310090 310190	RxClkcDlyTg0	R/W	“Register Name: RxClkcDlyTg0 Register-block: DWC_DDRPHYA_DBYTE” on page 404
499-506	010091 010191 110091 110191 210091 210191 310091 310191	RxClkcDlyTg1	R/W	“Register Name: RxClkcDlyTg1 Register-block: DWC_DDRPHYA_DBYTE” on page 405
507-514	010092 010192 110092 110192 210092 210192 310092 310192	RxClkcDlyTg2	R/W	“Register Name: RxClkcDlyTg2 Register-block: DWC_DDRPHYA_DBYTE” on page 406

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
515-522	010093 010193 110093 110193 210093 210193 310093 310193	RxClkcDlyTg3	R/W	"Register Name: RxClkcDlyTg3 Register-block: DWC_DDRPHYA_DBYTE" on page 407
523	0100A0	Dq0LnSel	R/W	"Register Name: Dq0LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 361
524	0100A1	Dq1LnSel	R/W	"Register Name: Dq1LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 362
525	0100A2	Dq2LnSel	R/W	"Register Name: Dq2LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 363
526	0100A3	Dq3LnSel	R/W	"Register Name: Dq3LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 364
527	0100A4	Dq4LnSel	R/W	"Register Name: Dq4LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 365
528	0100A5	Dq5LnSel	R/W	"Register Name: Dq5LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 366
529	0100A6	Dq6LnSel	R/W	"Register Name: Dq6LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 367
530	0100A7	Dq7LnSel	R/W	"Register Name: Dq7LnSel Register-block: DWC_DDRPHYA_DBYTE" on page 368
531	0100AA	PptCtlStatic	R/W	Programmed by PHY training firmware.
532	0100AB	PptCtlDyn	R/W	This register is dynamically written by PHY Initialization Engine during frequency changes and should not be written by the user.
533	0100AC	PptInfo	R	Reserved for PHY training firmware use.
534	0100AD	PptRxEnEvnt	R/W	This register is dynamically written by PHY Initialization Engine during frequency changes and should not be written by the user.
535-538	0100AE 1100AE 2100AE 3100AE	PptDqsCntInvTrnTg0	R/W	Programmed by PHY training firmware to support LPDDR3/LPDDR4 DRAM drift compensation.

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
539-542	0100AF 1100AF 2100AF 3100AF	PptDqsCntInvTrnTg1	R/W	Programmed by PHY training firmware to support LPDDR3/LPDDR4 DRAM drift compensation.
543	0100B1	DtsmBlankingCtrl	R/W	Reserved for PHY training firmware use.
544-552	0100B2 0101B2 0102B2 0103B2 0104B2 0105B2 0106B2 0107B2 0108B2	Tsm0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
553-561	0100B3 0101B3 0102B3 0103B3 0104B3 0105B3 0106B3 0107B3 0108B3	Tsm1	R	Reserved for PHY training firmware use.
562-570	0100B4 0101B4 0102B4 0103B4 0104B4 0105B4 0106B4 0107B4 0108B4	Tsm2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
571	0100B5	Tsm3	R/W	Reserved for PHY training firmware use.
572	0100B6	TxChkDataSelects	R/W	Reserved for PHY training firmware use.
573	0100B7	DtsmUpThldXingInd	R	Reserved for PHY training firmware use.
574	0100B8	DtsmLoThldXingInd	R	Reserved for PHY training firmware use.
575	0100B9	DbyteAllDtsmCtrl0	R/W	Reserved for PHY training firmware use.

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
576	0100BA	DbyteAllDtsmCtrl1	R/W	Reserved for PHY training firmware use.
577	0100BB	DbyteAllDtsmCtrl2	R/W	Reserved for PHY training firmware use.
578-613	0100C0 0101C0 0102C0 0103C0 0104C0 0105C0 0106C0 0107C0 0108C0 1100C0 1101C0 1102C0 1103C0 1104C0 1105C0 1106C0 1107C0 1108C0 2100C0 2101C0 2102C0 2103C0 2104C0 2105C0 2106C0 2107C0 2108C0 3100C0 3101C0 3102C0 3103C0 3104C0 3105C0 3106C0 3107C0 3108C0	TxDqDlyTg0	R/W	“Register Name: TxDqDlyTg0 Register-block: DWC_DDRPHYA_DBYTE” on page 392

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
614-649	0100C1 0101C1 0102C1 0103C1 0104C1 0105C1 0106C1 0107C1 0108C1 1100C1 1101C1 1102C1 1103C1 1104C1 1105C1 1106C1 1107C1 1108C1 2100C1 2101C1 2102C1 2103C1 2104C1 2105C1 2106C1 2107C1 2108C1 3100C1 3101C1 3102C1 3103C1 3104C1 3105C1 3106C1 3107C1 3108C1	TxDqDlyTg1	R/W	“Register Name: TxDqDlyTg1 Register-block: DWC_DDRPHYA_DBYTE” on page 393

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
650-685	0100C2 0101C2 0102C2 0103C2 0104C2 0105C2 0106C2 0107C2 0108C2 1100C2 1101C2 1102C2 1103C2 1104C2 1105C2 1106C2 1107C2 1108C2 2100C2 2101C2 2102C2 2103C2 2104C2 2105C2 2106C2 2107C2 2108C2 3100C2 3101C2 3102C2 3103C2 3104C2 3105C2 3106C2 3107C2 3108C2	TxDqDlyTg2	R/W	“Register Name: TxDqDlyTg2 Register-block: DWC_DDRPHYA_DBYTE” on page 394

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
686-721	0100C3 0101C3 0102C3 0103C3 0104C3 0105C3 0106C3 0107C3 0108C3 1100C3 1101C3 1102C3 1103C3 1104C3 1105C3 1106C3 1107C3 1108C3 2100C3 2101C3 2102C3 2103C3 2104C3 2105C3 2106C3 2107C3 2108C3 3100C3 3101C3 3102C3 3103C3 3104C3 3105C3 3106C3 3107C3 3108C3	TxDqDlyTg3	R/W	“Register Name: TxDqDlyTg3 Register-block: DWC_DDRPHYA_DBYTE” on page 395

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Table 11-4 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DBYTE (type = 0x1), instances 0..`DWC_DDRPHYA_DBYTES_{N}-1

Register Number	Address	Name	Access	Description
722-729	0100D0 0101D0 1100D0 1101D0 2100D0 2101D0 3100D0 3101D0	TxDqsDlyTg0	R/W	"Register Name: TxDqsDlyTg0 Register-block: DWC_DDRPHYA_DBYTE" on page 408
730-737	0100D1 0101D1 1100D1 1101D1 2100D1 2101D1 3100D1 3101D1	TxDqsDlyTg1	R/W	"Register Name: TxDqsDlyTg1 Register-block: DWC_DDRPHYA_DBYTE" on page 409
738-745	0100D2 0101D2 1100D2 1101D2 2100D2 2101D2 3100D2 3101D2	TxDqsDlyTg2	R/W	"Register Name: TxDqsDlyTg2 Register-block: DWC_DDRPHYA_DBYTE" on page 410
746-753	0100D3 0101D3 1100D3 1101D3 2100D3 2101D3 3100D3 3101D3	TxDqsDlyTg3	R/W	"Register Name: TxDqsDlyTg3 Register-block: DWC_DDRPHYA_DBYTE" on page 411
754	0100E4	DxLcdlStatus	R	"Register Name: DxLcdlStatus Register-block: DWC_DDRPHYA_DBYTE" on page 369

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11.2.5 DWC_DDRPHYA_DRTUB Register Block Address Map

Table 11-5 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_DRTUB (type = 0xc), instance 0

Register Number	Address	Name	Access	Description
755	0C0004	DctShadowRegs	R	Reserved for PHY training firmware use.
756	0C0030	DctWriteOnlyShadow	R	Reserved for PHY training firmware use.
757	0C0032	UctWriteOnly	R/W	Reserved for PHY training firmware use.
758	0C0033	UctWriteProt	R/W	Reserved for PHY training firmware use.
759	0C0034	UctDatWriteOnly	R/W	Reserved for PHY training firmware use.
760	0C0035	UctDatWriteProt	R/W	Reserved for PHY training firmware use.
761	0C0036	UctlErr	R/W	Reserved for PHY training firmware use.
762	0C0080	UcclkHclkEnables	R/W	“Register Name: UcclkHclkEnables Register-block: DWC_DDRPHYA_DRTUB” on page 412
763	0C0081	CurPstate0b	R/W	“Register Name: CurPstate0b Register-block: DWC_DDRPHYA_DRTUB” on page 413
764	0C0095	ClrWakeupSticky	R/W	Reserved for PHY training firmware use.
765	0C0096	WakeupMask	R/W	Reserved for PHY training firmware use.
766	0C00ED	CUSTPUBREV	R	“Register Name: CUSTPUBREV Register-block: DWC_DDRPHYA_DRTUB” on page 414
767	0C00EE	PUBREV	R	“Register Name: PUBREV Register-block: DWC_DDRPHYA_DRTUB” on page 415

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11.2.6 DWC_DDRPHYA_INTENG Register Block Address Map

Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
768	090000	PreSequenceReg0b0s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
769	090100	SequenceReg0b71s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
770	090001	PreSequenceReg0b0s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
771-774	090201 190201 290201 390201	Seq0BGPR1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
775	090101	SequenceReg0b72s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
776	090002	PreSequenceReg0b0s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
777-780	090202 190202 290202 390202	Seq0BGPR2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
781	090102	SequenceReg0b72s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
782	090003	PreSequenceReg0b1s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
783-786	090203 190203 290203 390203	Seq0BGPR3	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
787	090103	SequenceReg0b72s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
788	090004	PreSequenceReg0b1s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
789-792	090204 190204 290204 390204	Seq0BGPR4	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
793	090104	SequenceReg0b73s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
794	090005	PreSequenceReg0b1s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
795-798	090205 190205 290205 390205	Seq0BGPR5	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
799	090105	SequenceReg0b73s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
800	090006	PostSequenceReg0b0s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
801-804	090206 190206 290206 390206	Seq0BGPR6	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
805	090106	SequenceReg0b73s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
806	090007	PostSequenceReg0b0s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
807-810	090207 190207 290207 390207	Seq0BGPR7	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
811	090107	SequenceReg0b74s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
812	090008	PostSequenceReg0b0s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
813-816	090208 190208 290208 390208	Seq0BGPR8	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
817	090108	SequenceReg0b74s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
818	090009	PostSequenceReg0b1s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
819	090109	SequenceReg0b74s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
820	09000A	PostSequenceReg0b1s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
821	09010A	SequenceReg0b75s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
822	09000B	PostSequenceReg0b1s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
823	09010B	SequenceReg0b75s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
824	09000C	Seq0BDisableFlag0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
825	09010C	SequenceReg0b75s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
826	09000D	Seq0BDisableFlag1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
827	09010D	SequenceReg0b76s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
828	09000E	Seq0BDisableFlag2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
829	09010E	SequenceReg0b76s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
830	09000F	Seq0BDisableFlag3	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
831	09010F	SequenceReg0b76s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
832	090010	Seq0BDisableFlag4	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
833	090110	SequenceReg0b77s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
834	090011	Seq0BDisableFlag5	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
835	090111	SequenceReg0b77s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
836	090012	Seq0BDisableFlag6	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
837	090112	SequenceReg0b77s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
838	090013	Seq0BDisableFlag7	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
839	090113	SequenceReg0b78s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
840	090114	SequenceReg0b78s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
841	090115	SequenceReg0b78s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
842	090116	SequenceReg0b79s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
843	090017	StartVector0b0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
844	090117	SequenceReg0b79s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
845	090018	StartVector0b1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
846	090118	SequenceReg0b79s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
847	090019	StartVector0b2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
848	090119	SequenceReg0b80s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
849	09001A	StartVector0b3	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
850	09011A	SequenceReg0b80s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
851	09001B	StartVector0b4	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
852	09011B	SequenceReg0b80s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
853	09001C	StartVector0b5	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
854	09011C	SequenceReg0b81s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
855	09001D	StartVector0b6	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
856	09011D	SequenceReg0b81s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
857	09001E	StartVector0b7	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
858	09011E	SequenceReg0b81s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
859	09001F	StartVector0b8	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
860	09011F	SequenceReg0b82s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
861	090020	StartVector0b9	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
862	090120	SequenceReg0b82s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
863	090021	StartVector0b10	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
864	090121	SequenceReg0b82s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
865	090022	StartVector0b11	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
866	090122	SequenceReg0b83s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
867	090023	StartVector0b12	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
868	090123	SequenceReg0b83s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
869	090024	StartVector0b13	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
870	090124	SequenceReg0b83s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
871	090025	StartVector0b14	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
872	090125	SequenceReg0b84s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
873	090026	StartVector0b15	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
874	090126	SequenceReg0b84s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
875	090027	Seq0bWaitCondSel	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
876	090127	SequenceReg0b84s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
877	090028	PhyInLP3	R/W	"Register Name: PhyInLP3 Register-block: DWC_DDRPHYA_INITENG" on page 416

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
878	090128	SequenceReg0b85s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
879	090029	SequenceReg0b0s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
880	090129	SequenceReg0b85s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
881	09002A	SequenceReg0b0s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
882	09012A	SequenceReg0b85s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
883	09002B	SequenceReg0b0s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
884	09012B	SequenceReg0b86s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
885	09002C	SequenceReg0b1s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
886	09012C	SequenceReg0b86s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
887	09002D	SequenceReg0b1s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
888	09012D	SequenceReg0b86s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
889	09002E	SequenceReg0b1s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
890	09012E	SequenceReg0b87s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
891	09002F	SequenceReg0b2s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
892	09012F	SequenceReg0b87s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
893	090030	SequenceReg0b2s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
894	090130	SequenceReg0b87s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
895	090031	SequenceReg0b2s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
896	090131	SequenceReg0b88s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
897	090032	SequenceReg0b3s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
898	090132	SequenceReg0b88s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
899	090033	SequenceReg0b3s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
900	090133	SequenceReg0b88s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
901	090034	SequenceReg0b3s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
902	090134	SequenceReg0b89s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
903	090035	SequenceReg0b4s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
904	090135	SequenceReg0b89s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
905	090036	SequenceReg0b4s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
906	090136	SequenceReg0b89s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
907	090037	SequenceReg0b4s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
908	090137	SequenceReg0b90s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
909	090038	SequenceReg0b5s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
910	090138	SequenceReg0b90s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
911	090039	SequenceReg0b5s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
912	090139	SequenceReg0b90s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
913	09003A	SequenceReg0b5s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
914	09013A	SequenceReg0b91s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
915	09003B	SequenceReg0b6s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
916	09013B	SequenceReg0b91s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
917	09003C	SequenceReg0b6s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
918	09013C	SequenceReg0b91s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
919	09003D	SequenceReg0b6s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
920	09013D	SequenceReg0b92s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
921	09003E	SequenceReg0b7s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
922	09013E	SequenceReg0b92s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
923	09003F	SequenceReg0b7s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
924	09013F	SequenceReg0b92s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
925	090040	SequenceReg0b7s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
926	090140	SequenceReg0b93s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
927	090041	SequenceReg0b8s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
928	090141	SequenceReg0b93s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
929	090042	SequenceReg0b8s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
930	090142	SequenceReg0b93s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
931	090043	SequenceReg0b8s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
932	090143	SequenceReg0b94s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
933	090044	SequenceReg0b9s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
934	090144	SequenceReg0b94s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
935	090045	SequenceReg0b9s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
936	090145	SequenceReg0b94s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
937	090046	SequenceReg0b9s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
938	090146	SequenceReg0b95s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
939	090047	SequenceReg0b10s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
940	090147	SequenceReg0b95s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
941	090048	SequenceReg0b10s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
942	090148	SequenceReg0b95s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
943	090049	SequenceReg0b10s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
944	090149	SequenceReg0b96s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
945	09004A	SequenceReg0b11s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
946	09014A	SequenceReg0b96s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
947	09004B	SequenceReg0b11s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
948	09014B	SequenceReg0b96s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
949	09004C	SequenceReg0b11s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
950	09014C	SequenceReg0b97s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
951	09004D	SequenceReg0b12s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
952	09014D	SequenceReg0b97s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
953	09004E	SequenceReg0b12s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
954	09014E	SequenceReg0b97s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
955	09004F	SequenceReg0b12s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
956	09014F	SequenceReg0b98s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
957	090050	SequenceReg0b13s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
958	090150	SequenceReg0b98s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
959	090051	SequenceReg0b13s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
960	090151	SequenceReg0b98s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
961	090052	SequenceReg0b13s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
962	090152	SequenceReg0b99s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
963	090053	SequenceReg0b14s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
964	090153	SequenceReg0b99s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
965	090054	SequenceReg0b14s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
966	090154	SequenceReg0b99s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
967	090055	SequenceReg0b14s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
968	090155	SequenceReg0b100s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
969	090056	SequenceReg0b15s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
970	090156	SequenceReg0b100s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
971	090057	SequenceReg0b15s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
972	090157	SequenceReg0b100s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
973	090058	SequenceReg0b15s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
974	090158	SequenceReg0b101s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
975	090059	SequenceReg0b16s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
976	090159	SequenceReg0b101s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
977	09005A	SequenceReg0b16s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
978	09015A	SequenceReg0b101s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
979	09005B	SequenceReg0b16s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
980	09015B	SequenceReg0b102s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
981	09005C	SequenceReg0b17s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
982	09015C	SequenceReg0b102s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
983	09005D	SequenceReg0b17s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
984	09015D	SequenceReg0b102s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
985	09005E	SequenceReg0b17s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
986	09015E	SequenceReg0b103s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
987	09005F	SequenceReg0b18s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
988	09015F	SequenceReg0b103s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
989	090060	SequenceReg0b18s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
990	090160	SequenceReg0b103s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
991	090061	SequenceReg0b18s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
992	090161	SequenceReg0b104s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
993	090062	SequenceReg0b19s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
994	090162	SequenceReg0b104s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
995	090063	SequenceReg0b19s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
996	090163	SequenceReg0b104s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
997	090064	SequenceReg0b19s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
998	090164	SequenceReg0b105s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
999	090065	SequenceReg0b20s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1000	090165	SequenceReg0b105s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1001	090066	SequenceReg0b20s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1002	090166	SequenceReg0b105s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1003	090067	SequenceReg0b20s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1004	090167	SequenceReg0b106s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1005	090068	SequenceReg0b21s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1006	090168	SequenceReg0b106s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1007	090069	SequenceReg0b21s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1008	090169	SequenceReg0b106s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1009	09006A	SequenceReg0b21s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1010	09016A	SequenceReg0b107s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1011	09006B	SequenceReg0b22s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1012	09016B	SequenceReg0b107s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1013	09006C	SequenceReg0b22s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1014	09016C	SequenceReg0b107s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1015	09006D	SequenceReg0b22s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1016	09016D	SequenceReg0b108s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1017	09006E	SequenceReg0b23s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1018	09016E	SequenceReg0b108s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1019	09006F	SequenceReg0b23s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1020	09016F	SequenceReg0b108s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1021	090070	SequenceReg0b23s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1022	090170	SequenceReg0b109s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1023	090071	SequenceReg0b24s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1024	090171	SequenceReg0b109s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1025	090072	SequenceReg0b24s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1026	090172	SequenceReg0b109s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1027	090073	SequenceReg0b24s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1028	090173	SequenceReg0b110s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1029	090074	SequenceReg0b25s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1030	090174	SequenceReg0b110s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1031	090075	SequenceReg0b25s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1032	090175	SequenceReg0b110s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1033	090076	SequenceReg0b25s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1034	090176	SequenceReg0b111s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1035	090077	SequenceReg0b26s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1036	090177	SequenceReg0b111s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1037	090078	SequenceReg0b26s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1038	090178	SequenceReg0b111s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1039	090079	SequenceReg0b26s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1040	090179	SequenceReg0b112s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1041	09007A	SequenceReg0b27s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1042	09017A	SequenceReg0b112s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1043	09007B	SequenceReg0b27s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1044	09017B	SequenceReg0b112s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1045	09007C	SequenceReg0b27s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1046	09017C	SequenceReg0b113s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1047	09007D	SequenceReg0b28s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1048	09017D	SequenceReg0b113s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1049	09007E	SequenceReg0b28s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1050	09017E	SequenceReg0b113s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1051	09007F	SequenceReg0b28s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1052	09017F	SequenceReg0b114s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1053	090080	SequenceReg0b29s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1054	090180	SequenceReg0b114s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1055	090081	SequenceReg0b29s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1056	090181	SequenceReg0b114s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1057	090082	SequenceReg0b29s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1058	090182	SequenceReg0b115s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1059	090083	SequenceReg0b30s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1060	090183	SequenceReg0b115s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1061	090084	SequenceReg0b30s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1062	090184	SequenceReg0b115s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1063	090085	SequenceReg0b30s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1064	090185	SequenceReg0b116s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1065	090086	SequenceReg0b31s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1066	090186	SequenceReg0b116s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1067	090087	SequenceReg0b31s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1068	090187	SequenceReg0b116s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1069	090088	SequenceReg0b31s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1070	090188	SequenceReg0b117s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1071	090089	SequenceReg0b32s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1072	090189	SequenceReg0b117s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1073	09008A	SequenceReg0b32s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1074	09018A	SequenceReg0b117s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1075	09008B	SequenceReg0b32s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1076	09018B	SequenceReg0b118s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1077	09008C	SequenceReg0b33s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1078	09018C	SequenceReg0b118s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1079	09008D	SequenceReg0b33s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1080	09018D	SequenceReg0b118s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1081	09008E	SequenceReg0b33s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1082	09018E	SequenceReg0b119s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1083	09008F	SequenceReg0b34s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1084	09018F	SequenceReg0b119s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1085	090090	SequenceReg0b34s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1086	090190	SequenceReg0b119s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1087	090091	SequenceReg0b34s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1088	090191	SequenceReg0b120s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1089	090092	SequenceReg0b35s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1090	090192	SequenceReg0b120s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1091	090093	SequenceReg0b35s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1092	090193	SequenceReg0b120s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1093	090094	SequenceReg0b35s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1094	090194	SequenceReg0b121s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1095	090095	SequenceReg0b36s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1096	090195	SequenceReg0b121s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1097	090096	SequenceReg0b36s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1098	090196	SequenceReg0b121s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1099	090097	SequenceReg0b36s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1100	090098	SequenceReg0b37s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1101	090099	SequenceReg0b37s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1102	09009A	SequenceReg0b37s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1103	09009B	SequenceReg0b38s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1104	09009C	SequenceReg0b38s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1105	09009D	SequenceReg0b38s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1106	09009E	SequenceReg0b39s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1107	09009F	SequenceReg0b39s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1108	0900A0	SequenceReg0b39s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1109	0900A1	SequenceReg0b40s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1110	0900A2	SequenceReg0b40s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1111	0900A3	SequenceReg0b40s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1112	0900A4	SequenceReg0b41s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1113	0900A5	SequenceReg0b41s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1114	0900A6	SequenceReg0b41s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1115	0900A7	SequenceReg0b42s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1116	0900A8	SequenceReg0b42s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1117	0900A9	SequenceReg0b42s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1118	0900AA	SequenceReg0b43s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1119	0900AB	SequenceReg0b43s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1120	0900AC	SequenceReg0b43s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1121	0900AD	SequenceReg0b44s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1122	0900AE	SequenceReg0b44s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1123	0900AF	SequenceReg0b44s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1124	0900B0	SequenceReg0b45s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1125	0900B1	SequenceReg0b45s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1126	0900B2	SequenceReg0b45s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1127	0900B3	SequenceReg0b46s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1128	0900B4	SequenceReg0b46s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1129	0900B5	SequenceReg0b46s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1130	0900B6	SequenceReg0b47s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1131	0900B7	SequenceReg0b47s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1132	0900B8	SequenceReg0b47s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1133	0900B9	SequenceReg0b48s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1134	0900BA	SequenceReg0b48s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1135	0900BB	SequenceReg0b48s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1136	0900BC	SequenceReg0b49s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1137	0900BD	SequenceReg0b49s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1138	0900BE	SequenceReg0b49s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1139	0900BF	SequenceReg0b50s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1140	0900C0	SequenceReg0b50s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1141	0900C1	SequenceReg0b50s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1142	0900C2	SequenceReg0b51s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1143	0900C3	SequenceReg0b51s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1144	0900C4	SequenceReg0b51s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1145	0900C5	SequenceReg0b52s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1146	0900C6	SequenceReg0b52s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1147	0900C7	SequenceReg0b52s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1148	0900C8	SequenceReg0b53s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1149	0900C9	SequenceReg0b53s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1150	0900CA	SequenceReg0b53s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1151	0900CB	SequenceReg0b54s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1152	0900CC	SequenceReg0b54s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1153	0900CD	SequenceReg0b54s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1154	0900CE	SequenceReg0b55s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1155	0900CF	SequenceReg0b55s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1156	0900D0	SequenceReg0b55s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1157	0900D1	SequenceReg0b56s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1158	0900D2	SequenceReg0b56s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1159	0900D3	SequenceReg0b56s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1160	0900D4	SequenceReg0b57s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1161	0900D5	SequenceReg0b57s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1162	0900D6	SequenceReg0b57s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1163	0900D7	SequenceReg0b58s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1164	0900D8	SequenceReg0b58s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1165	0900D9	SequenceReg0b58s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1166	0900DA	SequenceReg0b59s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1167	0900DB	SequenceReg0b59s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1168	0900DC	SequenceReg0b59s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1169	0900DD	SequenceReg0b60s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1170	0900DE	SequenceReg0b60s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1171	0900DF	SequenceReg0b60s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1172	0900E0	SequenceReg0b61s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1173	0900E1	SequenceReg0b61s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1174	0900E2	SequenceReg0b61s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1175	0900E3	SequenceReg0b62s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1176	0900E4	SequenceReg0b62s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1177	0900E5	SequenceReg0b62s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1178	0900E6	SequenceReg0b63s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1179	0900E7	SequenceReg0b63s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1180	0900E8	SequenceReg0b63s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1181	0900E9	SequenceReg0b64s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1182	0900EA	SequenceReg0b64s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1183	0900EB	SequenceReg0b64s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1184	0900EC	SequenceReg0b65s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1185	0900ED	SequenceReg0b65s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1186	0900EE	SequenceReg0b65s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1187	0900EF	SequenceReg0b66s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1188	0900F0	SequenceReg0b66s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1189	0900F1	SequenceReg0b66s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1190	0900F2	SequenceReg0b67s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1191	0900F3	SequenceReg0b67s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1192	0900F4	SequenceReg0b67s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1193	0900F5	SequenceReg0b68s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1194	0900F6	SequenceReg0b68s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1195	0900F7	SequenceReg0b68s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1196	0900F8	SequenceReg0b69s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1197	0900F9	SequenceReg0b69s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1198	0900FA	SequenceReg0b69s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1199	0900FB	SequenceReg0b70s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1200	0900FC	SequenceReg0b70s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1201	0900FD	SequenceReg0b70s2	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1202	0900FE	SequenceReg0b71s0	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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Table 11-6 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_INITENG (type = 0x9), instance 0

Register Number	Address	Name	Access	Description
1203	0902FF	Seq0BFixedAddrBits	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.
1204	0900FF	SequenceReg0b71s1	R/W	Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes.

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11.2.7 DWC_DDRPHYA_MASTER Register Block Address Map

Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1205	020000	RxFifoInit	R/W	"Register Name: RxFifoInit Register-block: DWC_DDRPHYA_MASTER" on page 417
1206	020100	MapCAA0toDfi	R/W	"Register Name: MapCAA0toDfi Register-block: DWC_DDRPHYA_MASTER" on page 522
1207	020001	ForceClkDisable	R/W	"Register Name: ForceClkDisable Register-block: DWC_DDRPHYA_MASTER" on page 418
1208	020101	MapCAA1toDfi	R/W	"Register Name: MapCAA1toDfi Register-block: DWC_DDRPHYA_MASTER" on page 523
1209	020002	ClockingCtrl	R/W	This register is dynamically written by PHY Initialization Engine during frequency changes and should not be written by the user.
1210	020102	MapCAA2toDfi	R/W	"Register Name: MapCAA2toDfi Register-block: DWC_DDRPHYA_MASTER" on page 524
1211	020003	ForceInternalUpdate	R/W	"Register Name: ForceInternalUpdate Register-block: DWC_DDRPHYA_MASTER" on page 419
1212	020103	MapCAA3toDfi	R/W	"Register Name: MapCAA3toDfi Register-block: DWC_DDRPHYA_MASTER" on page 525
1213	020004	PhyConfig	R	"Register Name: PhyConfig Register-block: DWC_DDRPHYA_MASTER" on page 420
1214	020104	MapCAA4toDfi	R/W	"Register Name: MapCAA4toDfi Register-block: DWC_DDRPHYA_MASTER" on page 526
1215	020005	PGCR	R/W	"Register Name: PGCR Register-block: DWC_DDRPHYA_MASTER" on page 421
1216	020105	MapCAA5toDfi	R/W	"Register Name: MapCAA5toDfi Register-block: DWC_DDRPHYA_MASTER" on page 527
1217	020106	MapCAA6toDfi	R/W	"Register Name: MapCAA6toDfi Register-block: DWC_DDRPHYA_MASTER" on page 528
1218	020007	TestBumpCntrl1	R/W	"Register Name: TestBumpCntrl1 Register-block: DWC_DDRPHYA_MASTER" on page 422
1219	020107	MapCAA7toDfi	R/W	"Register Name: MapCAA7toDfi Register-block: DWC_DDRPHYA_MASTER" on page 529

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1220-1223	020008 120008 220008 320008	CalUclkInfo	R/W	"Register Name: CalUclkInfo Register-block: DWC_DDRPHYA_MASTER" on page 583
1224	020108	MapCAA8toDfi	R/W	"Register Name: MapCAA8toDfi Register-block: DWC_DDRPHYA_MASTER" on page 530
1225	020109	MapCAA9toDfi	R/W	"Register Name: MapCAA9toDfi Register-block: DWC_DDRPHYA_MASTER" on page 531
1226	02000A	TestBumpCntrl	R/W	"Register Name: TestBumpCntrl Register-block: DWC_DDRPHYA_MASTER" on page 424
1227-1230	02000B 12000B 22000B 32000B	Seq0BDLY0	R/W	"Register Name: Seq0BDLY0 Register-block: DWC_DDRPHYA_MASTER" on page 585
1231-1234	02000C 12000C 22000C 32000C	Seq0BDLY1	R/W	"Register Name: Seq0BDLY1 Register-block: DWC_DDRPHYA_MASTER" on page 587
1235-1238	02000D 12000D 22000D 32000D	Seq0BDLY2	R/W	"Register Name: Seq0BDLY2 Register-block: DWC_DDRPHYA_MASTER" on page 589
1239-1242	02000E 12000E 22000E 32000E	Seq0BDLY3	R/W	"Register Name: Seq0BDLY3 Register-block: DWC_DDRPHYA_MASTER" on page 591
1243	02000F	PhyAlertStatus	R	"Register Name: PhyAlertStatus Register-block: DWC_DDRPHYA_MASTER" on page 425
1244-1247	020010 120010 220010 320010	PPTTrainSetup	R/W	"Register Name: PPTTrainSetup Register-block: DWC_DDRPHYA_MASTER" on page 592
1248	020110	MapCAB0toDfi	R/W	"Register Name: MapCAB0toDfi Register-block: DWC_DDRPHYA_MASTER" on page 532

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1249-1252	020011 120011 220011 320011	PPTTrainSetup2	R/W	Programmed by PHY training firmware to support LPDDR4/4X DRAM drift compensation.
1253	020111	MapCAB1toDfi	R/W	"Register Name: MapCAB1toDfi Register-block: DWC_DDRPHYA_MASTER" on page 533
1254	020012	ATestMode	R/W	"Register Name: ATestMode Register-block: DWC_DDRPHYA_MASTER" on page 426
1255	020112	MapCAB2toDfi	R/W	"Register Name: MapCAB2toDfi Register-block: DWC_DDRPHYA_MASTER" on page 534
1256	020113	MapCAB3toDfi	R/W	"Register Name: MapCAB3toDfi Register-block: DWC_DDRPHYA_MASTER" on page 535
1257	020014	TxCalBinP	R	"Register Name: TxCalBinP Register-block: DWC_DDRPHYA_MASTER" on page 427
1258	020114	MapCAB4toDfi	R/W	"Register Name: MapCAB4toDfi Register-block: DWC_DDRPHYA_MASTER" on page 536
1259	020015	TxCalBinN	R	"Register Name: TxCalBinN Register-block: DWC_DDRPHYA_MASTER" on page 428
1260	020115	MapCAB5toDfi	R/W	"Register Name: MapCAB5toDfi Register-block: DWC_DDRPHYA_MASTER" on page 537
1261	020016	TxCalPOvr	R/W	"Register Name: TxCalPOvr Register-block: DWC_DDRPHYA_MASTER" on page 429
1262	020116	MapCAB6toDfi	R/W	"Register Name: MapCAB6toDfi Register-block: DWC_DDRPHYA_MASTER" on page 538
1263	020017	TxCalNOvr	R/W	"Register Name: TxCalNOvr Register-block: DWC_DDRPHYA_MASTER" on page 430
1264	020117	MapCAB7toDfi	R/W	"Register Name: MapCAB7toDfi Register-block: DWC_DDRPHYA_MASTER" on page 539
1265	020018	DfiMode	R/W	"Register Name: DfiMode Register-block: DWC_DDRPHYA_MASTER" on page 431
1266	020118	MapCAB8toDfi	R/W	"Register Name: MapCAB8toDfi Register-block: DWC_DDRPHYA_MASTER" on page 540
1267-1270	020019 120019 220019 320019	TristateModeCA	R/W	"Register Name: TristateModeCA Register-block: DWC_DDRPHYA_MASTER" on page 594

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1271	020119	MapCAB9toDfi	R/W	"Register Name: MapCAB9toDfi Register-block: DWC_DDRPHYA_MASTER" on page 541
1272	02001A	MtestMuxSel	R/W	"Register Name: MtestMuxSel Register-block: DWC_DDRPHYA_ANIB,DBYTE,MASTER" on page 341
1273	02001B	MtestPgmInfo	R/W	"Register Name: MtestPgmInfo Register-block: DWC_DDRPHYA_MASTER" on page 432
1274	02011B	PhyInterruptEnable	R/W	"Register Name: PhyInterruptEnable Register-block: DWC_DDRPHYA_MASTER" on page 542
1275	02001C	DynPwrDnUp	R/W	"Register Name: DynPwrDnUp Register-block: DWC_DDRPHYA_MASTER" on page 433
1276	02011C	PhyInterruptFWControl	R/W	"Register Name: PhyInterruptFWControl Register-block: DWC_DDRPHYA_MASTER" on page 544
1277	02001D	PMIEnable	R/W	This register is dynamically written by PHY Initialization Engine during frequency changes and should not be written by the user.
1278	02011D	PhyInterruptMask	R/W	"Register Name: PhyInterruptMask Register-block: DWC_DDRPHYA_MASTER" on page 545
1279	02001E	PhyTID	R/W	"Register Name: PhyTID Register-block: DWC_DDRPHYA_MASTER" on page 434
1280	02011E	PhyInterruptClear	R/W	"Register Name: PhyInterruptClear Register-block: DWC_DDRPHYA_MASTER" on page 547
1281	02011F	PhyInterruptStatus	R	"Register Name: PhyInterruptStatus Register-block: DWC_DDRPHYA_MASTER" on page 549
1282-1285	020020 120020 220020 320020	HwtMRL	R/W	"Register Name: HwtMRL Register-block: DWC_DDRPHYA_MASTER" on page 596
1286	020120	HwtSwizzleHwtAddress0	R/W	"Register Name: HwtSwizzleHwtAddress0 Register-block: DWC_DDRPHYA_MASTER" on page 553
1287	020021	DFIPHYUPD	R/W	"Register Name: DFIPHYUPD Register-block: DWC_DDRPHYA_MASTER" on page 435
1288	020121	HwtSwizzleHwtAddress1	R/W	"Register Name: HwtSwizzleHwtAddress1 Register-block: DWC_DDRPHYA_MASTER" on page 555
1289	020022	PdaMrsWriteMode	R/W	"Register Name: PdaMrsWriteMode Register-block: DWC_DDRPHYA_MASTER" on page 437

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1290	020122	HwtSwizzleHwtAddress2	R/W	"Register Name: HwtSwizzleHwtAddress2 Register-block: DWC_DDRPHYA_MASTER" on page 556
1291	020023	DFIGEARDOWNCTL	R/W	"Register Name: DFIGEARDOWNCTL Register-block: DWC_DDRPHYA_MASTER" on page 438
1292	020123	HwtSwizzleHwtAddress3	R/W	"Register Name: HwtSwizzleHwtAddress3 Register-block: DWC_DDRPHYA_MASTER" on page 557
1293-1296	020024 120024 220024 320024	DqsPreambleControl	R/W	"Register Name: DqsPreambleControl Register-block: DWC_DDRPHYA_MASTER" on page 597
1297	020124	HwtSwizzleHwtAddress4	R/W	"Register Name: HwtSwizzleHwtAddress4 Register-block: DWC_DDRPHYA_MASTER" on page 558
1298	020025	MasterX4Config	R/W	"Register Name: MasterX4Config Register-block: DWC_DDRPHYA_MASTER" on page 439
1299	020125	HwtSwizzleHwtAddress5	R/W	"Register Name: HwtSwizzleHwtAddress5 Register-block: DWC_DDRPHYA_MASTER" on page 559
1300	020026	WrLevBits	R/W	"Register Name: WrLevBits Register-block: DWC_DDRPHYA_MASTER" on page 440
1301	020126	HwtSwizzleHwtAddress6	R/W	"Register Name: HwtSwizzleHwtAddress6 Register-block: DWC_DDRPHYA_MASTER" on page 560
1302	020027	EnableCsMulticast	R/W	"Register Name: EnableCsMulticast Register-block: DWC_DDRPHYA_MASTER" on page 441
1303	020127	HwtSwizzleHwtAddress7	R/W	"Register Name: HwtSwizzleHwtAddress7 Register-block: DWC_DDRPHYA_MASTER" on page 561
1304	020028	HwtLpCsMultiCast	R/W	"Register Name: HwtLpCsMultiCast Register-block: DWC_DDRPHYA_MASTER" on page 442
1305	020128	HwtSwizzleHwtAddress8	R/W	"Register Name: HwtSwizzleHwtAddress8 Register-block: DWC_DDRPHYA_MASTER" on page 562
1306	020129	HwtSwizzleHwtAddress9	R/W	"Register Name: HwtSwizzleHwtAddress9 Register-block: DWC_DDRPHYA_MASTER" on page 563
1307	02012A	HwtSwizzleHwtAddress10	R/W	"Register Name: HwtSwizzleHwtAddress10 Register-block: DWC_DDRPHYA_MASTER" on page 564
1308	02012B	HwtSwizzleHwtAddress11	R/W	"Register Name: HwtSwizzleHwtAddress11 Register-block: DWC_DDRPHYA_MASTER" on page 565

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1309	02002C	Acx4AnibDis	R/W	"Register Name: Acx4AnibDis Register-block: DWC_DDRPHYA_MASTER" on page 443
1310	02012C	HwtSwizzleHwtAddress12	R/W	"Register Name: HwtSwizzleHwtAddress12 Register-block: DWC_DDRPHYA_MASTER" on page 566
1311-1314	02002D 12002D 22002D 32002D	DMIPinPresent	R/W	"Register Name: DMIPinPresent Register-block: DWC_DDRPHYA_MASTER" on page 599
1315	02012D	HwtSwizzleHwtAddress13	R/W	"Register Name: HwtSwizzleHwtAddress13 Register-block: DWC_DDRPHYA_MASTER" on page 567
1316-1319	02002E 12002E 22002E 32002E	ARdPtrInitVal	R/W	"Register Name: ARdPtrInitVal Register-block: DWC_DDRPHYA_MASTER" on page 600
1320	02012E	HwtSwizzleHwtAddress14	R/W	"Register Name: HwtSwizzleHwtAddress14 Register-block: DWC_DDRPHYA_MASTER" on page 568
1321	02012F	HwtSwizzleHwtAddress15	R/W	"Register Name: HwtSwizzleHwtAddress15 Register-block: DWC_DDRPHYA_MASTER" on page 569
1322	020030	Db0LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1323	020130	HwtSwizzleHwtAddress17	R/W	"Register Name: HwtSwizzleHwtAddress17 Register-block: DWC_DDRPHYA_MASTER" on page 570
1324	020031	Db1LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1325	020131	HwtSwizzleHwtActN	R/W	"Register Name: HwtSwizzleHwtActN Register-block: DWC_DDRPHYA_MASTER" on page 571
1326	020032	Db2LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1327	020132	HwtSwizzleHwtBank0	R/W	"Register Name: HwtSwizzleHwtBank0 Register-block: DWC_DDRPHYA_MASTER" on page 572
1328	020033	Db3LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1329	020133	HwtSwizzleHwtBank1	R/W	"Register Name: HwtSwizzleHwtBank1 Register-block: DWC_DDRPHYA_MASTER" on page 573
1330	020034	Db4LcdlCalPhDetOut	R	Reserved for PHY training firmware use.

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1331	020134	HwtSwizzleHwtBank2	R/W	"Register Name: HwtSwizzleHwtBank2 Register-block: DWC_DDRPHYA_MASTER" on page 574
1332	020035	Db5LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1333	020135	HwtSwizzleHwtBg0	R/W	"Register Name: HwtSwizzleHwtBg0 Register-block: DWC_DDRPHYA_MASTER" on page 575
1334	020036	Db6LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1335	020136	HwtSwizzleHwtBg1	R/W	"Register Name: HwtSwizzleHwtBg1 Register-block: DWC_DDRPHYA_MASTER" on page 576
1336	020037	Db7LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1337	020137	HwtSwizzleHwtCasN	R/W	"Register Name: HwtSwizzleHwtCasN Register-block: DWC_DDRPHYA_MASTER" on page 577
1338	020038	Db8LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1339	020138	HwtSwizzleHwtRasN	R/W	"Register Name: HwtSwizzleHwtRasN Register-block: DWC_DDRPHYA_MASTER" on page 578
1340	020039	Db9LcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1341	020139	HwtSwizzleHwtWeN	R/W	"Register Name: HwtSwizzleHwtWeN Register-block: DWC_DDRPHYA_MASTER" on page 579
1342	02003A	DbyteDllModeCntrl	R/W	"Register Name: DbyteDllModeCntrl Register-block: DWC_DDRPHYA_MASTER" on page 444
1343	02013A	HwtSwizzleHwtParityIn	R/W	"Register Name: HwtSwizzleHwtParityIn Register-block: DWC_DDRPHYA_MASTER" on page 580
1344	02003B	DbyteRxEnTrain	R/W	Reserved for PHY training firmware use.
1345	02013C	DfiHandshakeDelays0	R/W	"Register Name: DfiHandshakeDelays0 Register-block: DWC_DDRPHYA_MASTER" on page 581
1346	02013D	DfiHandshakeDelays1	R/W	"Register Name: DfiHandshakeDelays1 Register-block: DWC_DDRPHYA_MASTER" on page 582
1347	02003F	AnLcdlCalPhDetOut	R	Reserved for PHY training firmware use.
1348	020045	CalOffsets	R/W	"Register Name: CalOffsets Register-block: DWC_DDRPHYA_MASTER" on page 445
1349	020047	SarInitVals	R/W	"Register Name: SarInitVals Register-block: DWC_DDRPHYA_MASTER" on page 446
1350	020049	CalPExtOvr	R/W	"Register Name: CalPExtOvr Register-block: DWC_DDRPHYA_MASTER" on page 447

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1351	02004A	CalCmpr5Ovr	R/W	"Register Name: CalCmpr5Ovr Register-block: DWC_DDRPHYA_MASTER" on page 448
1352	02004B	CalNIntOvr	R/W	"Register Name: CalNIntOvr Register-block: DWC_DDRPHYA_MASTER" on page 449
1353	020050	CalDrvStr0	R/W	"Register Name: CalDrvStr0 Register-block: DWC_DDRPHYA_MASTER" on page 450
1354	020055	ProcOdtCtl	R/W	Reserved for PHY training firmware use.
1355-1358	020056 120056 220056 320056	ProcOdtTimeCtl	R/W	"Register Name: ProcOdtTimeCtl Register-block: DWC_DDRPHYA_MASTER" on page 602
1359	02005B	MemAlertControl	R/W	"Register Name: MemAlertControl Register-block: DWC_DDRPHYA_MASTER" on page 451
1360	02005C	MemAlertControl2	R/W	"Register Name: MemAlertControl2 Register-block: DWC_DDRPHYA_MASTER" on page 453
1361	020060	MemResetL	R/W	"Register Name: MemResetL Register-block: DWC_DDRPHYA_MASTER" on page 454
1362	02006E	PUBMODE	R/W	"Register Name: PUBMODE Register-block: DWC_DDRPHYA_MASTER" on page 455
1363	02006F	MiscPhyStatus	R	"Register Name: MiscPhyStatus Register-block: DWC_DDRPHYA_MASTER" on page 456
1364	020070	CoreLoopbackSel	R/W	"Register Name: CoreLoopbackSel Register-block: DWC_DDRPHYA_MASTER" on page 457
1365	020071	DllTrainParam	R/W	"Register Name: DllTrainParam Register-block: DWC_DDRPHYA_MASTER" on page 458
1366	020072	HwtLpCsEnA	R/W	Programmed by PHY training firmware to support LPDDR4/LPDDR4X DRAM drift compensation.
1367	020073	HwtLpCsEnB	R/W	Programmed by PHY training firmware to support LPDDR3/LPDDR4 DRAM drift compensation.
1368	020074	HwtLpCsEnBypass	R/W	"Register Name: HwtLpCsEnBypass Register-block: DWC_DDRPHYA_MASTER" on page 459
1369	020075	DfiCAMode	R/W	"Register Name: DfiCAMode Register-block: DWC_DDRPHYA_MASTER" on page 460
1370	020076	HwtCACtl	R/W	Reserved for PHY training firmware use.

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1371	020077	HwtCAMode	R/W	Programmed by PHY training firmware to support LPDDR4/4X DRAM drift compensation.
1372	020078	DllControl	R/W	"Register Name: DllControl Register-block: DWC_DDRPHYA_MASTER" on page 461
1373	020079	PulseDllUpdatePhase	R/W	"Register Name: PulseDllUpdatePhase Register-block: DWC_DDRPHYA_MASTER" on page 462
1374	02007A	HwtControlOvr0	R/W	Reserved for PHY training firmware use.
1375	02007B	HwtControlOvr1	R/W	Reserved for PHY training firmware use.
1376-1379	02007C 12007C 22007C 32007C	DllGainCtl	R/W	"Register Name: DllGainCtl Register-block: DWC_DDRPHYA_MASTER" on page 603
1380-1383	02007D 12007D 22007D 32007D	DllLockParam	R/W	Reserved for PHY training firmware use.
1384	02007E	HwtControlVal0	R/W	Reserved for PHY training firmware use.
1385	02007F	HwtControlVal1	R/W	Reserved for PHY training firmware use.
1386	020081	AcsmGlblStart	R/W	Reserved for PHY training firmware use.
1387	020082	AcsmGlblSglStpCtrl	R/W	Reserved for PHY training firmware use.
1388	020084	LcdlCalPhase	R/W	Reserved for PHY test firmware use.
1389	020085	LcdlCalCtrl	R/W	Reserved for PHY test firmware use.
1390	020088	CalRate	R/W	"Register Name: CalRate Register-block: DWC_DDRPHYA_MASTER" on page 464
1391	020089	CalZap	R/W	"Register Name: CalZap Register-block: DWC_DDRPHYA_MASTER" on page 466
1392	02008B	PState	R/W	"Register Name: PState Register-block: DWC_DDRPHYA_MASTER" on page 468
1393	02008C	CalPreDriverOverride	R/W	Reserved for PHY training firmware use.
1394	02008D	PllOutGateControl	R/W	"Register Name: PllOutGateControl Register-block: DWC_DDRPHYA_MASTER" on page 469

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1395	02008F	UcMemResetControl	R/W	This register is dynamically written by PHY Initialization Engine during frequency changes and should not be written by the user.
1396	020090	PorControl	R/W	"Register Name: PorControl Register-block: DWC_DDRPHYA_MASTER" on page 470
1397	020097	CalBusy	R	"Register Name: CalBusy Register-block: DWC_DDRPHYA_MASTER" on page 471
1398	020098	CalMisc2	R/W	"Register Name: CalMisc2 Register-block: DWC_DDRPHYA_MASTER" on page 472
1399	02009A	CalMisc	R/W	"Register Name: CalMisc Register-block: DWC_DDRPHYA_MASTER" on page 474
1400	02009B	CalVRefs	R/W	"Register Name: CalVRefs Register-block: DWC_DDRPHYA_MASTER" on page 476
1401	02009C	CalCmpr5	R	"Register Name: CalCmpr5 Register-block: DWC_DDRPHYA_MASTER" on page 477
1402	02009D	CalNInt	R	"Register Name: CalNInt Register-block: DWC_DDRPHYA_MASTER" on page 478
1403	02009E	CalPExt	R	"Register Name: CalPExt Register-block: DWC_DDRPHYA_MASTER" on page 479
1404	0200A8	CalCmpInvert	R/W	"Register Name: CalCmpInvert Register-block: DWC_DDRPHYA_MASTER" on page 480
1405	0200AE	CalCmpanaCntrl	R/W	"Register Name: CalCmpanaCntrl Register-block: DWC_DDRPHYA_MASTER" on page 481
1406-1409	0200B0 1200B0 2200B0 3200B0	DfiRdDataCsDestMap	R/W	"Register Name: DfiRdDataCsDestMap Register-block: DWC_DDRPHYA_MASTER" on page 604
1410-1413	0200B2 1200B2 2200B2 3200B2	VrefInGlobal	R/W	"Register Name: VrefInGlobal Register-block: DWC_DDRPHYA_MASTER" on page 605
1414-1417	0200B4 1200B4 2200B4 3200B4	DfiWrDataCsDestMap	R/W	"Register Name: DfiWrDataCsDestMap Register-block: DWC_DDRPHYA_MASTER" on page 607

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1418	0200B5	MasUpdGoodCtr	R	"Register Name: MasUpdGoodCtr Register-block: DWC_DDRPHYA_MASTER" on page 482
1419	0200B6	PhyUpd0GoodCtr	R	"Register Name: PhyUpd0GoodCtr Register-block: DWC_DDRPHYA_MASTER" on page 483
1420	0200B7	PhyUpd1GoodCtr	R	"Register Name: PhyUpd1GoodCtr Register-block: DWC_DDRPHYA_MASTER" on page 484
1421	0200B8	CtlUpd0GoodCtr	R	"Register Name: CtlUpd0GoodCtr Register-block: DWC_DDRPHYA_MASTER" on page 485
1422	0200B9	CtlUpd1GoodCtr	R	"Register Name: CtlUpd1GoodCtr Register-block: DWC_DDRPHYA_MASTER" on page 486
1423	0200BA	MasUpdFailCtr	R	"Register Name: MasUpdFailCtr Register-block: DWC_DDRPHYA_MASTER" on page 487
1424	0200BB	PhyUpd0FailCtr	R	"Register Name: PhyUpd0FailCtr Register-block: DWC_DDRPHYA_MASTER" on page 488
1425	0200BC	PhyUpd1FailCtr	R	"Register Name: PhyUpd1FailCtr Register-block: DWC_DDRPHYA_MASTER" on page 489
1426	0200BD	PhyPerfCtrEnable	R/W	"Register Name: PhyPerfCtrEnable Register-block: DWC_DDRPHYA_MASTER" on page 490
1427	0200C3	PllPwrDn	R/W	"Register Name: PllPwrDn Register-block: DWC_DDRPHYA_MASTER" on page 491
1428	0200C4	PllReset	R/W	"Register Name: PllReset Register-block: DWC_DDRPHYA_MASTER" on page 492
1429-1432	0200C5 1200C5 2200C5 3200C5	PllCtrl2	R/W	"Register Name: PllCtrl2 Register-block: DWC_DDRPHYA_MASTER" on page 608
1433	0200C6	PllCtrl0	R/W	"Register Name: PllCtrl0 Register-block: DWC_DDRPHYA_MASTER" on page 493
1434-1437	0200C7 1200C7 2200C7 3200C7	PllCtrl1	R/W	"Register Name: PllCtrl1 Register-block: DWC_DDRPHYA_MASTER" on page 609
1438	0200C8	PllTst	R/W	"Register Name: PllTst Register-block: DWC_DDRPHYA_MASTER" on page 495
1439	0200C9	PllLockStatus	R	"Register Name: PllLockStatus Register-block: DWC_DDRPHYA_MASTER" on page 499

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1440-1443	0200CA 1200CA 2200CA 3200CA	PllTestMode	R/W	"Register Name: PllTestMode Register-block: DWC_DDRPHYA_MASTER" on page 610
1444	0200CB	PllCtrl3	R/W	"Register Name: PllCtrl3 Register-block: DWC_DDRPHYA_MASTER" on page 500
1445-1448	0200CC 1200CC 2200CC 3200CC	PllCtrl4	R/W	"Register Name: PllCtrl4 Register-block: DWC_DDRPHYA_MASTER" on page 611
1449	0200CD	PllEndofCal	R	"Register Name: PllEndofCal Register-block: DWC_DDRPHYA_MASTER" on page 501
1450	0200CE	PllStandbyEff	R	"Register Name: PllStandbyEff Register-block: DWC_DDRPHYA_MASTER" on page 502
1451	0200CF	PllDacValOut	R	"Register Name: PllDacValOut Register-block: DWC_DDRPHYA_MASTER" on page 503
1452	0200D0	DlyTestSeq	R/W	Reserved for PHY test firmware use.
1453	0200D1	DlyTestRingSelDb	R/W	Reserved for PHY test firmware use.
1454	0200D2	DlyTestRingSelAc	R/W	Reserved for PHY test firmware use.
1455	0200D3	DlyTestCntDfiClkIV	R/W	Reserved for PHY training firmware use.
1456	0200D4	DlyTestCntDfiClk	R	Reserved for PHY training firmware use.
1457	0200D5	DlyTestCntRingOscDb0	R	Reserved for PHY training firmware use.
1458	0200D6	DlyTestCntRingOscDb1	R	Reserved for PHY training firmware use.
1459	0200D7	DlyTestCntRingOscDb2	R	Reserved for PHY training firmware use.
1460	0200D8	DlyTestCntRingOscDb3	R	Reserved for PHY training firmware use.
1461	0200D9	DlyTestCntRingOscDb4	R	Reserved for PHY training firmware use.
1462	0200DA	DlyTestCntRingOscDb5	R	Reserved for PHY training firmware use.
1463	0200DB	DlyTestCntRingOscDb6	R	Reserved for PHY training firmware use.
1464	0200DC	DlyTestCntRingOscDb7	R	Reserved for PHY training firmware use.
1465	0200DD	DlyTestCntRingOscDb8	R	Reserved for PHY training firmware use.
1466	0200DE	DlyTestCntRingOscDb9	R	Reserved for PHY training firmware use.

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1467	0200DF	DlyTestCntRingOscAc	R	Reserved for PHY training firmware use.
1468	0200E0	MstLcdlDbgCntl	R/W	Reserved for PHY training firmware use.
1469	0200E1	MstLcdl0DbgRes	R	Reserved for PHY training firmware use.
1470	0200E2	MstLcdl1DbgRes	R	Reserved for PHY training firmware use.
1471	0200E3	LcdlDbgCntl	R/W	"Register Name: LcdlDbgCntl Register-block: DWC_DDRPHYA_MASTER" on page 504
1472	0200E4	AcLcdlStatus	R	"Register Name: AcLcdlStatus Register-block: DWC_DDRPHYA_MASTER" on page 506
1473	0200ED	CUSTPHYREV	R	"Register Name: CUSTPHYREV Register-block: DWC_DDRPHYA_MASTER" on page 507
1474	0200EE	PHYREV	R	"Register Name: PHYREV Register-block: DWC_DDRPHYA_MASTER" on page 508
1475	0200EF	LP3ExitSeq0BStartVector	R/W	"Register Name: LP3ExitSeq0BStartVector Register-block: DWC_DDRPHYA_MASTER" on page 509
1476	0200F0	DfiFreqXlat0	R/W	"Register Name: DfiFreqXlat0 Register-block: DWC_DDRPHYA_MASTER" on page 510
1477	0200F1	DfiFreqXlat1	R/W	"Register Name: DfiFreqXlat1 Register-block: DWC_DDRPHYA_MASTER" on page 511
1478	0200F2	DfiFreqXlat2	R/W	"Register Name: DfiFreqXlat2 Register-block: DWC_DDRPHYA_MASTER" on page 512
1479	0200F3	DfiFreqXlat3	R/W	"Register Name: DfiFreqXlat3 Register-block: DWC_DDRPHYA_MASTER" on page 513
1480	0200F4	DfiFreqXlat4	R/W	"Register Name: DfiFreqXlat4 Register-block: DWC_DDRPHYA_MASTER" on page 514
1481	0200F5	DfiFreqXlat5	R/W	"Register Name: DfiFreqXlat5 Register-block: DWC_DDRPHYA_MASTER" on page 515
1482	0200F6	DfiFreqXlat6	R/W	"Register Name: DfiFreqXlat6 Register-block: DWC_DDRPHYA_MASTER" on page 516
1483	0200F7	DfiFreqXlat7	R/W	"Register Name: DfiFreqXlat7 Register-block: DWC_DDRPHYA_MASTER" on page 517
1484	0200F8	TxRdPtrInit	R/W	"Register Name: TxRdPtrInit Register-block: DWC_DDRPHYA_MASTER" on page 518
1485	0200F9	DfiInitComplete	R/W	"Register Name: DfiInitComplete Register-block: DWC_DDRPHYA_MASTER" on page 519

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Table 11-7 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_MASTER (type = 0x2), instance 0

Register Number	Address	Name	Access	Description
1486-1489	0200FA 1200FA 2200FA 3200FA	DfiFreqRatio	R/W	"Register Name: DfiFreqRatio Register-block: DWC_DDRPHYA_MASTER" on page 612
1490	0200FB	RxFifoChecks	R/W	"Register Name: RxFifoChecks Register-block: DWC_DDRPHYA_MASTER" on page 520
1491	0200FF	MTestDtoCtrl	R/W	"Register Name: MTestDtoCtrl Register-block: DWC_DDRPHYA_MASTER" on page 521

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11.2.8 DWC_DDRPHYA_PPGC Register Block Address Map

Table 11-8 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_PPGC (type = 0x7), instance 0

Register Number	Address	Name	Access	Description
1492	070011	PPGCCtrl1	R/W	Reserved for PHY training firmware use.
1493	070015	PpgcLane2CrcInMap0	R/W	Reserved for PHY training firmware use.
1494	070016	PpgcLane2CrcInMap1	R/W	Reserved for PHY training firmware use.
1495-1503	070024 070124 070224 070324 070424 070524 070624 070724 070824	PrbsTapDly0	R/W	Reserved for PHY training firmware use.
1504-1512	070025 070125 070225 070325 070425 070525 070625 070725 070825	PrbsTapDly1	R/W	Reserved for PHY training firmware use.
1513-1521	070026 070126 070226 070326 070426 070526 070626 070726 070826	PrbsTapDly2	R/W	Reserved for PHY training firmware use.

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Table 11-8 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_PPGC (type = 0x7), instance 0

Register Number	Address	Name	Access	Description
1522-1530	070027 070127 070227 070327 070427 070527 070627 070727 070827	PrbsTapDly3	R/W	Reserved for PHY training firmware use.
1531	070030	GenPrbsByte0	R/W	Reserved for PHY training firmware use.
1532	070031	GenPrbsByte1	R/W	Reserved for PHY training firmware use.
1533	070032	GenPrbsByte2	R/W	Reserved for PHY training firmware use.
1534	070033	GenPrbsByte3	R/W	Reserved for PHY training firmware use.
1535	070034	GenPrbsByte4	R/W	Reserved for PHY training firmware use.
1536	070035	GenPrbsByte5	R/W	Reserved for PHY training firmware use.
1537	070036	GenPrbsByte6	R/W	Reserved for PHY training firmware use.
1538	070037	GenPrbsByte7	R/W	Reserved for PHY training firmware use.
1539	070038	GenPrbsByte8	R/W	Reserved for PHY training firmware use.
1540	070039	GenPrbsByte9	R/W	Reserved for PHY training firmware use.
1541	07003A	GenPrbsByte10	R/W	Reserved for PHY training firmware use.
1542	07003B	GenPrbsByte11	R/W	Reserved for PHY training firmware use.
1543	07003C	GenPrbsByte12	R/W	Reserved for PHY training firmware use.
1544	07003D	GenPrbsByte13	R/W	Reserved for PHY training firmware use.
1545	07003E	GenPrbsByte14	R/W	Reserved for PHY training firmware use.
1546	07003F	GenPrbsByte15	R/W	Reserved for PHY training firmware use.
1547	070060	PrbsGenCtl	R/W	Reserved for PHY training firmware use.
1548	070061	PrbsGenStateLo	R/W	Reserved for PHY training firmware use.
1549	070062	PrbsGenStateHi	R/W	Reserved for PHY training firmware use.
1550	070063	PrbsChkStateLo	R/W	Reserved for PHY training firmware use.
1551	070064	PrbsChkStateHi	R/W	Reserved for PHY training firmware use.

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Table 11-8 DDRPHY Registers Address Mapping of register-block DWC_DDRPHYA_PPGC (type = 0x7), instance 0

Register Number	Address	Name	Access	Description
1552	070065	PrbsGenCtl1	R/W	Reserved for PHY training firmware use.
1553	070066	PrbsGenCtl2	R/W	Reserved for PHY training firmware use.

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11.3 Register Description

11.3.1 AForceDrvCont

- Description: Force Address/Command Driven (Lanes A3-A0)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 027
- Replicated per PState: No
- Exists: Always

Table 11-9 Register Name: AForceDrvCont Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[3:0]	AForceDrvCont	Force continuous drive, per-lane, of the ACX4 instance controlled by this register Setting this register will cause the PHY to drive the target lane when dfi_init_complete==1 Bit [0] = controls lane 0 of the target ACX4 block Bit [1] = controls lane 1 of the target ACX4 block Bit [2] = controls lane 2 of the target ACX4 block Bit [3] = controls lane 3 of the target ACX4 block	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.2 AForceTriCont

- Description: Force Address/Command Tristate (Lanes A3-A0)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 028
- Replicated per PState: No
- Exists: Always

Table 11-10 Register Name: AForceTriCont Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[3:0]	AForceTriCont	Force tristate control, per-lane, of the ACX4 instance controlled by this register Setting this register will cause the PHY to tristate the target lane when dfi_init_complete==1 Bit [0] = controls lane 0 of the target ACX4 block Bit [1] = controls lane 1 of the target ACX4 block Bit [2] = controls lane 2 of the target ACX4 block Bit [3] = controls lane 3 of the target ACX4 block	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.3 ATxImpedance

- Description: Tx impedance of Address driver cells.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 043
- Replicated per PState: No
- Exists: Always

Table 11-11 Register Name: ATxImpedance Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[4:0]	ADrvStrenP	5 bit bus used to select the target pull up output impedance. Please Refer to Technology specific PHY DATABOOK for supported options Connects to the DrvStren pins of the driver. 110_xx = 120R pull-up connected to VDDQLP (LPDDR4X) 100_xx = 60R pull-up connected to VDDQLP (LPDDR4X) 000_xx = 40R pull-up connected to VDDQLP (LPDDR4X) 111_00 = 120R pull-up connected to VDDQ (DDR4, LPDDR4) 111_01 = 60R pull-up connected to VDDQ (DDR4, LPDDR4) 111_11 = 40R pull-up connected to VDDQ (DDR4, LPDDR4)	R/W	0x1f
[9:5]	ADrvStrenN	5 bit bus used to select the target pull down output impedance. Please Refer to Technology specific PHY DATABOOK for supported option Connects to the DrvStren pins of the driver. xxx_00 = 120R pull-down (DDR4, LP4/4X) xxx_01 = 60R pull-down (DDR4, LP4/4X) xxx_11 = 40R pull-down (DDR4, LP4/4X)	R/W	0x1f
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.4 ATestPrbsErr

- Description: Address Loopback PRBS Error status for an entire ACX4 block
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 053
- Replicated per PState: No
- Exists: Always

Table 11-12 Register Name: ATestPrbsErr Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[3:0]	ATestPrbsErr	Overall error indicator for each prbs bump checker. Bit[0] = Lane0 Error Status {1 = errors found, 0 = no errors} Bit[1] = Lane1 Error Status Bit[2] = Lane2 Error Status Bit[3] = Lane3 Error Status	R	-
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.5 ATxSlewRate

- Description: controls slew rates of address/command/memclk drivers.
  Tx predriver cal trims driver timing to account for clock duty cycle variation.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 055
- Replicated per PState: No
- Exists: Always

Table 11-13 Register Name: ATxSlewRate Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[3:0]	ATxPreP	4 bit binary trim for the driver pull up slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[7:4]	ATxPreN	4 bit binary trim for the driver pull down slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[10:8]	ATxPreDrvMode	Controls predrivers to adjust timing of turn-on and turn-off of pull-up and pull-down segments. Recommended settings if the ANIB drives CK pins: DDR4 = 3'b000 LPDDR4 = 3'b001 Recommended settings if the ANIB does not drive CK pins: DDR4 = 3'b011 LPDDR4 = 3'b001	R/W	0x7
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.6 ATestPrbsErrCnt

- Description: Address Loopback Test Result register
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 056
- Replicated per PState: No
- Exists: Always

Table 11-14 Register Name: ATestPrbsErrCnt Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[15:0]	ATestPrbsErrCnt	Overall error indicator for each prbs bump checker. Bit [3:0] = Lane0 Error Count Bit [7:4] = Lane1 Error Count Bit [11:8] = Lane2 Error Count Bit [15:12] = Lane3 Error Count	R	-

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11.3.7 ATxDly

- Description: Address/Command Delay, per pstate.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB
- Register Offset: 080
- Replicated per PState: Yes
- Exists: Always

Table 11-15 Register Name: ATxDly Register-block: DWC_DDRPHYA_ANIB

Bits	Name	Description	Access	Default
[6:0]	ATxDly	Trained for LPDDR4/4X to generate timed address and command signals to the DRAMs, per ACX4. For DDR4, it is recommended that address and command ACX4 have it ATxDly=0x00 The four signals generated by an ACX4 will have common timing. ATxDly[6] is the coarse delay, ie one unit of delay is 1 UI. ATxDly[5] is reserved. ATxDly[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. The target ACX4 used for memory clock generation, must have its ATxDly configured to 0x00.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.8 MtestMuxSel

- Description: Digital Observation Pin control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_ANIB,DBYTE,MASTER
- Register Offset: 01A
- Replicated per PState: No
- Exists: Always

Table 11-16 Register Name: MtestMuxSel Register-block: DWC_DDRPHYA_ANIB,DBYTE,MASTER

Bits	Name	Description	Access	Default
[5:0]	MtestMuxSel	Controls for the 64-1 mux for asynchronous data to the Digital Observation Pin. Encoding 6'h0 --> Drive 0 from this chiplet (allows flat 'OR' of pass-through information) Encoding 6'h01:1f --> Select local data from AC/DBYTE/MASTER macro Encoding 6'h20 --> Reserved (Drive 0 from macro into mux; Drive 0 from PUB synth logic path into mux) Encoding 6'h21:3f --> Select local data from PUB AC/DBYTE/MASTER synthesized logic Note: See PUB documentation for how, or if, the Digital Observation Pin is mapped to a physical bump in this configuration.	R/W	0x00
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.9 MicroContMuxSel

- Description: PMU Config Mux Select
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 000
- Replicated per PState: No
- Exists: Always

Table 11-17 Register Name: MicroContMuxSel Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[0:0]	MicroContMuxSel	This register controls access to the PHY configuration registers. 1 = MicroController/PHY Init Engine has control of csr bus. 0 = MicroController/PHY Init Engine csr requests are ignored.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.10 UctShadowRegs

- Description: This is used for the mailbox protocol between the firmware and the system. See section 3.4.1 of the training firmware AppNote for details on the protocol.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 004
- Replicated per PState: No
- Exists: Always

Table 11-18 Register Name: UctShadowRegs Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[0:0]	UctWriteProtShadow	When set to 0, the PMU has a message for the user	R	-
[1:1]	UctDatWriteProtShadow	Reserved for future use.	R	-
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.11 DctWriteOnly

- Description: Reserved for future use.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 030
- Replicated per PState: No
- Exists: Always

Table 11-19 Register Name: DctWriteOnly Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[15:0]	DctWriteOnly	Reserved for future use.	R/W	0x0000

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11.3.12 DctWriteProt

- Description: DCT downstream mailbox protocol CSR.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 031
- Replicated per PState: No
- Exists: Always

Table 11-20 Register Name: DctWriteProt Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[0:0]	DctWriteProt	By setting this register to 0, the user acknowledges the receipt of the message.	R/W	0x1
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.13 UctWriteOnlyShadow

- Description: Read-only view of the csr UctDatWriteOnly
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 032
- Replicated per PState: No
- Exists: Always

Table 11-21 Register Name: UctWriteOnlyShadow Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[15:0]	UctWriteOnlyShadow	Used to pass the message ID for major messages. Also used to pass the lower 16 bits for streaming messages.	R	-

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11.3.14 UctDatWriteOnlyShadow

- Description: Read-only view of the csr UctDatWriteOnly
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 034
- Replicated per PState: No
- Exists: Always

Table 11-22 Register Name: UctDatWriteOnlyShadow Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[15:0]	UctDatWriteOnlyShadow	Used to pass the upper 16 bits for streaming messages. Not used in passing major messages.	R	-

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11.3.15 DfiCfgRdDataValidTicks

- Description: Number of DfiClk ticks required for valid csr Rd Data.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 037
- Replicated per PState: No
- Exists: Always

Table 11-23 Register Name: DfiCfgRdDataValidTicks Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[5:0]	DfiCfgRdDataValidTicks	Roundtrip delay of a register read access. This value must not be changed from its reset value.	R/W	0x06
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.16 MicroReset

- Description: Controls reset and clock shutdown on the local microcontroller.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 099
- Replicated per PState: No
- Exists: Always

Table 11-24 Register Name: MicroReset Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[0:0]	StallToMicro	Set this bit to stall the microcontroller by hardware. Clear this bit to allow the microcontroller to continue executing from its current program counter location. Typically, this bit is used at power up to hold the program counter at the boot vector while BIOS loads the microcontroller program code. While stalled, the microcontroller clocks are gated off for power reduction.	R/W	0x1
[1:1]	TestWakeup	Reserved. Must always be set to 0.	R/W	0x0
[2:2]	RSVDMicro	RSVD	R/W	0x0
[3:3]	ResetToMicro	Set this bit to apply synchronous reset to the microcontroller. Clear this bit to release reset to the microcontroller. This reset initializes the program counter to begin execution from the boot vector. This reset also clears the interrupt sticky bits.	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.17 DfiInitCompleteShadow

- Description: dfi_init_complete - Controller Read-only Shadow
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_APBONLY
- Register Offset: 0FA
- Replicated per PState: No
- Exists: Always

Table 11-25 Register Name: DfiInitCompleteShadow Register-block: DWC_DDRPHYA_APBONLY

Bits	Name	Description	Access	Default
[0:0]	DfiInitCompleteShadow	This csr presents a read-only view (a shadow) of the Register DfiInitComplete which is used by the sequencer to control the state of dfi_init_complete. The value in this Register is not affected by the BlockSeq0BAck field of the SequencerOverride register. While the Register MicroContMuxSel is set, access to this Shadow register will not steal config bus bandwidth from the micro controller. That is polling won't have a performance penalty.	R	-
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.18 DbyteMiscMode

- Description: Controls the enable/disable state of the DBYTE module.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 000
- Replicated per PState: No
- Exists: Always

Table 11-26 Register Name: DbyteMiscMode Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[1:0]	Unimplemented	Returns zero on reads	R	0x0
[2:2]	DByteDisable	Controls whether this DBYTE module is disabled. If this DBYTE module is not enabled, it receives no clocks and remains in reset. 0 - Enable this DBYTE module 1 - Disable this DBYTE module This field should only be changed PHY initialization step C.	R/W	0x0
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.19 DqDqsRcvCntrl1

- Description: Misc control of rxdq cell and rxdqs cell
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 04A
- Replicated per PState: No
- Exists: Always

Table 11-27 Register Name: DqDqsRcvCntrl1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[8:0]	PowerDownRcvr	Active high signal which powers down the receiver. [7:0 -> dq[7:0], 8 -> dbi] After this pin is deasserted the receiver cannot be used for a minimum of 100 ns.	R/W	0x000
[9:9]	PowerDownRcvrDqs	Active high signal which powers down the receiver. After this pin is deasserted the receiver cannot be used for a minimum of 100 ns. This control powers down both the upper and lower DQS receivers. If Register X4TG[3:0]=0000, then the upper DQS receiver is powered down.	R/W	0x0
[10:10]	RxPadStandbyEn	Enables the rxdq/rxdqs StandBy power savings, per pad-group.	R/W	0x1
[11:11]	EnLPReqPDR	Reserved for future use	R/W	0x0
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.20 RxFifoCheckStatus

- Description: When a PhyRxFifoCheck interrupt is posted. These bits indicate which pair of fifo pointers didn't match as expected. The non-zero pointer values can be read from the RxFifoCheckStatusValues register. Setting the PhyRxFifoCheckClr in the PhyInterruptClear register clears these bits.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 056
- Replicated per PState: No
- Exists: Always

Table 11-28 Register Name: RxFifoCheckStatus Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[0:0]	RxFifoLocErr	If set, the read pointer (DFI side) on the read FIFO associated with data bits [3:0] didn't match the write pointer (DQS side) on the read FIFO associated with data bits [3:0];	R	-
[1:1]	RxFifoLocUErr	If set, the read pointer (DFI side) on the read FIFO associated with data bits [7:4] didn't match the write pointer (DQS side) on the read FIFO associated with data bits [7:4];	R	-
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.21 RxFifoCheckErrValues

- Description: Contains the value of the fifo pointer for the first mismatch captured in the RxFifoCheckStatus register. Setting the PhyRxFifoCheckClr in the PhyInterruptClear register clears these bits.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 057
- Replicated per PState: No
- Exists: Always

Table 11-29 Register Name: RxFifoCheckErrValues Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[3:0]	RxFifoRdLocErrValue	The first error value captured for the read pointer (DFI side) on the read FIFO associated with data bits [3:0];	R	-
[7:4]	RxFifoWrLocErrValue	The first error value captured for the write pointer (DQS side) on the read FIFO associated with data bits [3:0];	R	-
[11:8]	RxFifoRdLocUErrValue	The first error value captured for the read pointer (DFI side) on the read FIFO associated with data bits [7:4];	R	-
[15:12]	RxFifoWrLocUErrValue	The first error value captured for the write pointer (DQS side) on the read FIFO associated with data bits [7:4];	R	-

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11.3.22 RxFifoInfo

- Description: Provides visibility of the read and write pointers of the RxFifos for debug purposes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 058
- Replicated per PState: No
- Exists: Always

Table 11-30 Register Name: RxFifoInfo Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[3:0]	RxFifoRdLoc	The Mission mode read pointer of the lower-nibble Rx fifo.	R	-
[7:4]	RxFifoWrLoc	The Mission mode write pointer of the lower-nibble Rx fifo.	R	-
[11:8]	RxFifoRdLocU	The Mission mode read pointer of the upper-nibble Rx fifo.	R	-
[15:12]	RxFifoWrLocU	The Mission mode write pointer of the upper-nibble Rx fifo.	R	-

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11.3.23 RxFifoVisibility

- Description: Allows the contents of the data rx fifo to be read
  via CSRs RxFifoContentsDBI,RxFifoContentsDQ7654,RxFifoContentsDQ3210.
  The fifo must be quiescent, ie no actual operations in progress,
  while reading the fifo That is, the read from the RxFifo must be
  after the max-read-latency (DFIMRL) time.
  Procedure to read the contents of the entire RxFifo:

```
 wait for any outstanding reads to complete (min 2*DFIMRL MemClks)
 read and store RxFifoWrLoc[3:0] and RxFifoWrLocU[3:0] (they should be equal).
 perform four BL8 memory reads
 wait at least 2*DFIMRL MemClks.
 for (iNib=0, iNib<8, iNib++) {
   myRdPtr[2:0] = (stored RxFifoWrLoc[3:0]>>1) + iNib  (may wrap 7 to 0)
   write addr=RxFifoVisibility, data={csrRxFifoRdEn=0,csrFifoRdPtrOvr=1,csrRxFifoRdPtr=myRdPtr}
   write addr=RxFifoVisibility, data={csrRxFifoRdEn=1,csrFifoRdPtrOvr=1,csrRxFifoRdPtr=myRdPtr}
   write addr=RxFifoVisibility, data={csrRxFifoRdEn=0,csrFifoRdPtrOvr=1,csrRxFifoRdPtr=myRdPtr}
   wait for 8  DfiClk.
   read addr=RxFifoContentsDBI
   read addr=RxFifoContentsDQ7654
   read addr=RxFifoContentsDQ3210
   unpack/align resulting data as described in descriptions of RxFifoContents registers, and
     map according to the configuration of the csr Dq<7..0>LnSel[2:0].
 }
 evaluate/compare with data that travels through normal read path (dfi_read_data_dbi,dfi_read_data).
 write {csrRxFifoRdEn=0,csrFifoRdPtrOvr=0,csrRxFifoRdPtr = 0}
 PHY is now available for normal mission-mode operation.
end of Procedure
```

- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 059
- Replicated per PState: No
- Exists: Always

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Table 11-31 Register Name: RxFifoVisibility Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	RxFifoRdPtr	If CSR RxFifoRdPtrOVr is set, then this CSR selects the rxfifo entry is visible in CSR This 3b field addresses 4b units of the 8x4b (32entry) fifo; that is, rdfifo_nibble_address[2:0]=csrRxFifoRdPtr[2:0] For example, Register RxFifoRdPtr[2:0]=2 will enable reading bit-entries 11..8. The exact location of read data will depend on the prior history of reads and PHY initialization.	R/W	0x0
[3:3]	RxFifoRdPtrOvr	0 : Normal operation - mission mode read pointer is enabled 1 : Override - Control of the rx fifo read pointer is ceded to CSR RxFifoRdPtr.	R/W	0x0
[4:4]	RxFifoRdEn	Pulse {set 0-->1-->0} this bit to capture the Fifo Contents.	R/W	0x0
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.24 RxFifoContentsDQ3210

- Description: RX FIFO contents, lane[3:0]
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 05A
- Replicated per PState: No
- Exists: Always

Table 11-32 Register Name: RxFifoContentsDQ3210 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[15:0]	RxFifoContentsDQ3210	A window into the contents of the RxFifo, as controlled by CSR RxFifoVisibility This register reads 4b at a time from lane0..3 from the four fifo entries addressed by rdfifo_nibble_address[2:0]=RxFifoRdPtr[2:0] Register [15:12] = {lane3_ui3,lane3_ui2,lane3_ui1,lane3_ui0} where ui0 is the first occurring bit [11: 8] = {lane2_ui3,lane2_ui2,lane2_ui1,lane2_ui0} [7: 4] = {lane1_ui3,lane1_ui2,lane1_ui1,lane1_ui0} [3: 0] = {lane0_ui3,lane0_ui2,lane0_ui1,lane0_ui0} Note that the DBYTE lane of a given index is not the same as a memory DQ of the same index unless the csr Dq<7..0>LnSel[2:0] have their default/reset value.	R	-

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11.3.25 RxFifoContentsDQ7654

- Description: RX FIFO contents, lane[7:4]
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 05B
- Replicated per PState: No
- Exists: Always

Table 11-33 Register Name: RxFifoContentsDQ7654 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[15:0]	RxFifoContentsDQ7654	A window into the contents of the RxFifo, as controlled by CSR RxFifoVisibility This register reads 4b at a time from lane4..7 from the four fifo entries addressed by rdfifo_nibble_address[2:0]=RxFifoRdPtr[2:0] Register [15:12] = {lane7_ui3,lane7_ui2,lane7_ui1,lane7_ui0} [11: 8] = {lane6_ui3,lane6_ui2,lane6_ui1,lane6_ui0} [7: 4] = {lane5_ui3,lane5_ui2,lane5_ui1,lane5_ui0} [3: 0] = {lane4_ui3,lane4_ui2,lane4_ui1,lane4_ui0} Note that the DBYTE lane of a given index is not the same as a memory DQ of the same index unless the csr Dq<7..0>LnSel[2:0] have their default/reset value.	R	-

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11.3.26 RxFifoContentsDBI

- Description: RX FIFO contents, dbi
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 05C
- Replicated per PState: No
- Exists: Always

Table 11-34 Register Name: RxFifoContentsDBI Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[3:0]	RxFifoContentsDBI	A window into the contents of the RxFifo, as controlled by CSR RxFifoVisibility This register reads 4b at a time from DBI from the four fifo entries addressed by rdfifo_nibble_address[2:0]=RxFifoRdPtr[2:0] Register [3: 0] = {dbi_ui3,dbi_ui2,dbi_ui1,dbi_ui0} Note that the DBYTE DBI lane is the same as the memory DBI; it is not subject to mapping using csr Dq<7..0>LnSel[2:0] as the DQ are.	R	-
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.27 Dq0LnSel

- Description: Maps Phy DQ lane to memory DQ0
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A0
- Replicated per PState: No
- Exists: Always

Table 11-35 Register Name: Dq0LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq0LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq0 (on this dbyte), then Register Dq0LnSel for this dbyte should be 3.	R/W	0x0
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.28 Dq1LnSel

- Description: Maps Phy DQ lane to memory DQ1
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A1
- Replicated per PState: No
- Exists: Always

Table 11-36 Register Name: Dq1LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq1LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq1 (on this dbyte), then Register Dq1LnSel for this dbyte should be 3.	R/W	0x1
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.29 Dq2LnSel

- Description: Maps Phy DQ lane to memory DQ2
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A2
- Replicated per PState: No
- Exists: Always

Table 11-37 Register Name: Dq2LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq2LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq2 (on this dbyte), then Register Dq2LnSel for this dbyte should be 3.	R/W	0x2
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.30 Dq3LnSel

- Description: Maps Phy DQ lane to memory DQ3
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A3
- Replicated per PState: No
- Exists: Always

Table 11-38 Register Name: Dq3LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq3LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq3 (on this dbyte), then Register Dq3LnSel for this dbyte should be 3.	R/W	0x3
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.31 Dq4LnSel

- Description: Maps Phy DQ lane to memory DQ4
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A4
- Replicated per PState: No
- Exists: Always

Table 11-39 Register Name: Dq4LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq4LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq4 (on this dbyte), then Register Dq4LnSel for this dbyte should be 3.	R/W	0x4
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.32 Dq5LnSel

- Description: Maps Phy DQ lane to memory DQ5
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A5
- Replicated per PState: No
- Exists: Always

Table 11-40 Register Name: Dq5LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq5LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq5 (on this dbyte), then Register Dq5LnSel for this dbyte should be 3.	R/W	0x5
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.33 Dq6LnSel

- Description: Maps Phy DQ lane to memory DQ6
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A6
- Replicated per PState: No
- Exists: Always

Table 11-41 Register Name: Dq6LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq6LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq6 (on this dbyte), then Register Dq6LnSel for this dbyte should be 3.	R/W	0x6
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.34 Dq7LnSel

- Description: Maps Phy DQ lane to memory DQ7
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0A7
- Replicated per PState: No
- Exists: Always

Table 11-42 Register Name: Dq7LnSel Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[2:0]	Dq7LnSel	Supports mapping of PHY dq to dram dq within a byte (swizzle). Intended to undo the swizzle of board-level phy-to-dram connections. such that MRR operations of binary counters may be return correct values. Note that this register is per-dbyte such that the swizzle may be different per dbyte. Each register in a byte's set of DqLnSel must have a unique value within the set. For example, if, on this dbyte, PHY lane 3 is connected to memory dq7 (on this dbyte), then Register Dq7LnSel for this dbyte should be 3.	R/W	0x7
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.35 DxLcdlStatus

- Description: Status of dbyte macro LCDL selected by Register LcdlStatusSel
  Note that is register is per dbyte.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0E4
- Replicated per PState: No
- Exists: Always

Table 11-43 Register Name: DxLcdlStatus Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[9:0]	DxLcdlFineSnapVal	Value of the LCDL 1UI estimate code, latched by pulse on csr LcdlFineSnap while csr LcdlTstEnable=1. Index 9 is reserved for growth.	R	-
[10:10]	DxLcdlPhdSnapVal	Value of the LCDL phase-detector output, latched by pulse on csr LcdlFineSnap. while csr LcdlTstEnable=1.	R	-
[11:11]	DxLcdlStickyLock	latched value of whether the LCDL ever achieved lock after the assertion of LcdlTstEnable.	R	-
[12:12]	DxLcdlStickyUnlock	latched value of whether the LCDL ever lost lock after the assertion of LcdlTstEnable.	R	-
[13:13]	DxLcdlLiveLock	present value of whether the LCDL is locked, valid when LcdlTstEnable=1.	R	-
[15:14]	Unimplemented	Returns zero on reads	R	0x0

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11.3.36 VrefDAC1

- Description: VrefDAC1 control for DQ Receiver (used only when DFE is enabled in DDR4)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 030 130 230 330 430 530 630 730 830
- Replicated per PState: No
- Exists: Always

Table 11-44 Register Name: VrefDAC1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:0]	VrefDAC1	VrefDAC1 controls the alternate VREF setting for DFE (used only when DFE is enabled in DDR4) DAC control for rxdq cell internal VREF, trained by Firmware The VREF generators have different ranges, depending on the Mission Mode settings for {DqDqsRcvCntrl::MajorMode,DqDqsRcvCntrl::ExtVrefRange} {011,0} :: VREF = VDDQ*(0.510 + VrefDAC1[6:0]*0.00345) {011,1} :: VREF = VDDQ*(0.453 + VrefDAC1[6:0]*0.00385) {non-enumerated encodings are reserved} Register Block Offset Address 0x030 is the VrefDAC1 for lane0. Register Block Offset Address 0x130 is the VrefDAC1 for lane1. Register Block Offset Address 0x230 is the VrefDAC1 for lane2. Register Block Offset Address 0x330 is the VrefDAC1 for lane3. Register Block Offset Address 0x430 is the VrefDAC1 for lane4. Register Block Offset Address 0x530 is the VrefDAC1 for lane5. Register Block Offset Address 0x630 is the VrefDAC1 for lane6. Register Block Offset Address 0x730 is the VrefDAC1 for lane7. Register Block Offset Address 0x830 is the VrefDAC1 for lane{DBI}.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.37 VrefDAC0

- Description: VrefDAC0 control for DQ Receiver
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 040 140 240 340 440 540 640 740 840
- Replicated per PState: No
- Exists: Always

Table 11-45 Register Name: VrefDAC0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:0]	VrefDAC0	PHY RX VREF DAC control for rxdq cell internal VREF, (used only when 2D training is enabled in LPDDR4,DDR4) DAC control for rxdq cell internal VREF, trained by Firmware The VREF generators have different ranges, depending on the Mission Mode settings for {DqDqsRcvCntrl::MajorMode,DqDqsRcvCntrl::ExtVrefRange} {000,0} :: VREF = VDDQ*(0.287 + VrefDAC0[6:0]*0.00330) {000,1} :: VREF = VDDQ*(0.250 + VrefDAC0[6:0]*0.00385) {011,0} :: VREF = VDDQ*(0.510 + VrefDAC0[6:0]*0.00345) {011,1} :: VREF = VDDQ*(0.453 + VrefDAC0[6:0]*0.00385) {010,0} :: VREF = VDDQ*(0.047 + VrefDAC0[6:0]*0.00367) {non-enumerated encodings are reserved} Register Block Offset Address 0x040 is the VrefDAC0 for lane0. Register Block Offset Address 0x140 is the VrefDAC0 for lane1. Register Block Offset Address 0x240 is the VrefDAC0 for lane2. Register Block Offset Address 0x340 is the VrefDAC0 for lane3. Register Block Offset Address 0x440 is the VrefDAC0 for lane4. Register Block Offset Address 0x540 is the VrefDAC0 for lane5. Register Block Offset Address 0x640 is the VrefDAC0 for lane6. Register Block Offset Address 0x740 is the VrefDAC0 for lane7. Register Block Offset Address 0x840 is the VrefDAC0 for lane{DBI}.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.38 RxPBDlyTg0

- Description: Read DQ per-bit BDL delay (Timing Group 0).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 068 168 268 368 468 568 668 768 868
- Replicated per PState: No
- Exists: Always

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Table 11-46 Register Name: RxPBDlyTg0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:0]	RxPBDlyTg0	Read DQ per-bit BDL delay (Timing Group 0). Trained to deskew the read DQ data that will be sampled by the incoming per-nibble read DQS, to improve the composite eye. The unit of change is a LSB in the control of the delay circuit, and is not denoninated in units of UI. Register Block Offset Address 0x068 controls the lane0 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x168 controls the lane1 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x268 controls the lane2 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x368 controls the lane3 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x468 controls the lane4 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x568 controls the lane5 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x668 controls the lane6 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x768 controls the lane7 read deskew timing. (For Timing Group 0) Register Block Offset Address 0x868 controls the lane{DBI} read deskew timing. (For Timing Group 0) Note that this register is not per-pstate. The same deskew (for channel-routing differences) is used for all pstates. . Note: Timing Group 0 = RANK0.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.39 RxPBDlyTg1

- Description: Read DQ per-bit BDL delay (Timing Group 1).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 069 169 269 369 469 569 669 769 869
- Replicated per PState: No
- Exists: Always

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Table 11-47 Register Name: RxPBDlyTg1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:0]	RxPBDlyTg1	Read DQ per-bit BDL delay (Timing Group 1). Trained to deskew the read DQ data that will be sampled by the incoming per-nibble read DQS, to improve the composite eye. The unit of change is a LSB in the control of the delay circuit, and is not denoninated in units of UI. Register Block Offset Address 0x069 controls the lane0 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x169 controls the lane1 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x269 controls the lane2 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x369 controls the lane3 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x469 controls the lane4 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x569 controls the lane5 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x669 controls the lane6 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x769 controls the lane7 read deskew timing. (For Timing Group 1) Register Block Offset Address 0x869 controls the lane{DBI} read deskew timing. (For Timing Group 1) Note that this register is not per-pstate. The same deskew (for channel-routing differences) is used for all pstates. . Note: Timing Group 1 = RANK1.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.40 RxPBDlyTg2

- Description: Read DQ per-bit BDL delay (Timing Group 2).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 06A 16A 26A 36A 46A 56A 66A 76A 86A
- Replicated per PState: No
- Exists: Always

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Table 11-48 Register Name: RxPBDlyTg2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:0]	RxPBDlyTg2	Read DQ per-bit BDL delay (Timing Group 2). Trained to deskew the read DQ data that will be sampled by the incoming per-nibble read DQS, to improve the composite eye. The unit of change is a LSB in the control of the delay circuit, and is not denoninated in units of UI. Register Block Offset Address 0x06a controls the lane0 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x16a controls the lane1 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x26a controls the lane2 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x36a controls the lane3 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x46a controls the lane4 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x56a controls the lane5 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x66a controls the lane6 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x76a controls the lane7 read deskew timing. (For Timing Group 2) Register Block Offset Address 0x86a controls the lane{DBI} read deskew timing. (For Timing Group 2) Note that this register is not per-pstate. The same deskew (for channel-routing differences) is used for all pstates. . Note: Timing Group 2 = RANK2.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.41 RxPBDlyTg3

- Description: Read DQ per-bit BDL delay (Timing Group 3).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 06B 16B 26B 36B 46B 56B 66B 76B 86B
- Replicated per PState: No
- Exists: Always

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Table 11-49 Register Name: RxPBDlyTg3 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:0]	RxPBDlyTg3	Read DQ per-bit BDL delay (Timing Group 3). Trained to deskew the read DQ data that will be sampled by the incoming per-nibble read DQS, to improve the composite eye. The unit of change is a LSB in the control of the delay circuit, and is not denoninated in units of UI. Register Block Offset Address 0x06b controls the lane0 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x16b controls the lane1 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x26b controls the lane2 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x36b controls the lane3 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x46b controls the lane4 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x56b controls the lane5 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x66b controls the lane6 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x76b controls the lane7 read deskew timing. (For Timing Group 3) Register Block Offset Address 0x86b controls the lane{DBI} read deskew timing. (For Timing Group 3) Note that this register is not per-pstate. The same deskew (for channel-routing differences) is used for all pstates. . Note: Timing Group 3 = RANK3.	R/W	0x00
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.42 DFIMRL

- Description: DFI MaxReadLatency
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 020
- Replicated per PState: Yes
- Exists: Always

Table 11-50 Register Name: DFIMRL Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[4:0]	DFIMRL	This Max Read Latency CSR is to be trained to ensure the rx-data fifo is not read until after all dbytes have their read data valid. This is the value, in units of two mem clocks, between dfi_rddata_en and dfi_rddata_valid A unit change in the LSB is a change in MRL of two mem clocks.	R/W	0x06
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.43 TxEqualizationMode

- Description: Tx DQ driver equalization is a technique for improving the write-data eye at the DRAMs. The driver can drive with full strength (configured with DrvStrenFSHiDqP and DrvStrenFSLoDqN0 or with weak strength (configured with DrvStrenEQHiDqP and DrvStrenEQLoDqN) depending on the dq value sequence.
  TxEqMode = 00 Off; drive with full strength only
  TxEqMode = 01 Mode0 drive with full strength.or weak strength depending on present logical value and the previous logical value.
  TxEqMode = 10 Mode1 drive with full strength.or weak strength depending on present logical value and the next logical value.
  Mode1 is a lower power mode.
  TxEqMode = 11 reserved
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 048
- Replicated per PState: Yes
- Exists: Always

Table 11-51 Register Name: TxEqualizationMode Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[1:0]	TxEqMode		R/W	0x0
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.44 DqDqsRcvCntrl2

- Description: Control for an agressive power-saving feature to powerdown dq and dqs receiver cells dynamically.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 04C
- Replicated per PState: Yes
- Exists: Always

Table 11-52 Register Name: DqDqsRcvCntrl2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[0:0]	EnRxAgressivePDR	reserved	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.45 TxImpedanceCtrl0

- Description: Reserved
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 041 141
- Replicated per PState: Yes
- Exists: Always

Table 11-53 Register Name: TxImpedanceCtrl0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	DrvStrenDqP	Reserved	R/W	0x3f
[11:6]	DrvStrenDqN	Reserved	R/W	0x3f
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.46 DqDqsRcvCntrl

- Description: Connected to the rxdqs and rxdq Mode selects and trim controls, per nibble.
  Register Block Offset Address 0x043 controls the lower DQ nibble
  Register Block Offset Address 0x143 controls the upper DQ nibble
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 043 143
- Replicated per PState: Yes
- Exists: Always

Table 11-54 Register Name: DqDqsRcvCntrl Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[0:0]	SelAnalogVref	Setting this signal high will force the local per-bit VREF generator to pass the global VREFA to the samplers.	R/W	0x0
[1:1]	ExtVrefRange	Extends the range available in the local per-bit VREF generator.	R/W	0x0
[3:2]	DfeCtrl	DFE may be used with MajorModeDbyte=011 only 00 - DFE off 01 - DFE on 10 - Train DFE0 Amplifier 11 - Train DFE1 Amplifier These settings are determined by PHY Training FW and should not be overridden.	R/W	0x0

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Table 11-54 Register Name: DqDqsRcvCntrl Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[6:4]	MajorModeDbyte	Selects the major mode of operation for the receiver. These settings are determined by PHY Configuration based on DRAM protocol 000 - Input signal is terminated/referenced to VDDQ/2 (or unterminated) 001 - reserved 010 - Input signal is terminated/referenced to VSSQ 011 - Input signal is terminated/referenced to VDDQ 100 - reserved 101 - reserved 110 - reserved 111 - reserved	R/W	0x3
[11:7]	GainCurrAdj	Adjust gain current of RX amplifier stage. It is recommended to use default values for this CSR.	R/W	0x0b
[15:12]	Reserved	Reserved[12] unavailable - should not be set Reserved[13] unavailable - should not be set Reserved[14] Set to 1 to enable VIL/VIH testing of the DFE0 Amp Reserved[15] Set to 1 to enable VIL/VIH testing of the DFE1 Amp NOTE: Reserved[15:14] should not be asserted simultaneously	R/W	0x0

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11.3.47 TxImpedanceCtrl1

- Description: Tx impedance of DQ driver cells when equalization is disabled.
  Register Block Offset Address 0x049 controls the lower DQ nibble
  Register Block Offset Address 0x149 controls the upper DQ nibble
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 049 149
- Replicated per PState: Yes
- Exists: Always

Table 11-55 Register Name: TxImpedanceCtrl1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	DrvStrenFSDqP	Please Refer to Technology specific PHY DATABOOK for supported options. 6 bit bus used to select the target pull up output impedance. Connects to the DrvStren pins of the driver. xxx_110 = 120R pull-up connected to VDDQLP (LPDDR4X) xxx_100 = 60R pull-up connected to VDDQLP (LPDDR4X) xxx_000 = 40R pull-up connected to VDDQLP (LPDDR4X) 000_111 = HiZ 001_111 = 120R pull-up connected to VDDQ (DDR4, LPDDR4) 011_111 = 60R pull-up connected to VDDQ (DDR4, LPDDR4) 111_111 = 40R pull-up connected to VDDQ (DDR4, LPDDR4) NOTE: if any pull-up connected to VDDQLP is enabled, all pull-ups connect to VDDQ will be disabled.	R/W	0x3f
[11:6]	DrvStrenFSDqN	Please Refer to Technology specific PHY DATABOOK for supported options. 6 bit bus used to select the target pull down output impedance. Connects to the DrvStren pins of the driver. 000_xxx = HiZ 001_xxx = 120R pull-down (DDR4, LP4/4X) 011_xxx = 60R pull-down (DDR4, LP4/4X) 111_xxx = 40R pull-down (DDR4, LP4/4X)	R/W	0x3f

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Table 11-55 Register Name: TxImpedanceCtrl1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.48 TxImpedanceCtrl2

- Description: Reserved
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 04B 14B
- Replicated per PState: Yes
- Exists: Always

Table 11-56 Register Name: TxImpedanceCtrl2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	DrvStrenEQHiDqP	Reserved	R/W	0x00
[11:6]	DrvStrenEQLoDqN	Reserved	R/W	0x00
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.49 TxOdtDrvStren

- Description: Selects desired impedance value for Host ODT
  Must be set by user before PHY initialization
  Setting for each protocol:
  DDR4:
  ODT pull-up connected to VDDQ - non-zero value
  ODT pull-up connected to VDDQLP - high-impedance
  ODT pull-down - high-impedance
  LPDDR4/4X:
  ODT pull-up connected to VDDQ - high-impedance
  ODT pull-up connected to VDDQLP - high-impedance
  ODT pull-down - non-zero value
  Register Block Offset Address 0x04d controls the lower DQ nibble
  Register Block Offset Address 0x14d controls the upper DQ nibble
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 04D 14D
- Replicated per PState: Yes
- Exists: Always

Table 11-57 Register Name: TxOdtDrvStren Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	ODTStrenP	Selects the ODT pull-up impedance. Please Refer to Technology specific PHY DATABOOK for supported options xxx_001 = 120R pull-up connected to VDDQLP xxx_011 = 60R pull-up connected to VDDQLP xxx_111 = 40R pull-up connected to VDDQLP 000_000 = HiZ 001_000 = 120R pull-up connected to VDDQ (DDR4) 011_000 = 60R pull-up connected to VDDQ (DDR4) 111_000 = 40R pull-up connected to VDDQ (DDR4) NOTE: if any pull-up connected to VDDQLP is enabled, ODTStrenP value is ignored and all pull-ups connect to VDDQ will be disabled.	R/W	0x00

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Table 11-57 Register Name: TxOdtDrvStren Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[11:6]	ODTStrenN	Selects the ODT pull-down impedance.. Please Refer to Technology specific PHY DATABOOK for supported options 000_000 = HiZ 001_000 = 120R pull-down (LP4/4X) 011_000 = 60R pull-down (LP4/4X) 111_000 = 40R pull-down (LP4/4X)	R/W	0x00
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.50 TxSlewRate

- Description: Controls slew rates of the DQ/DQS drivers per nibble.
  Tx predriver cal trims driver timing to account for clock duty cycle variation.
  Register Block Offset Address 0x05f is the TxSlewRate for the lower nibble.
  Register Block Offset Address 0x15f is the TxSlewRate for the upper nibble.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 05F 15F
- Replicated per PState: Yes
- Exists: Always

Table 11-58 Register Name: TxSlewRate Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[3:0]	TxPreP	4 bit binary trim for the driver pull up slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[7:4]	TxPreN	4 bit binary trim for the driver pull down slew rate. 4'b0000 has a slower slew rate than 4'b1111	R/W	0xf
[10:8]	TxPreDrvMode	Controls predrivers to adjust timing of turn-on and turn-off of pull-up and pull-down segments. Recommended settings: DDR4 = 3'b010 LPDDR4 = 3'b001 LPDDR4X = 3'b101	R/W	0x7
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.51 TxDqDlyTg0

- Description: Write DQ Delay (Timing Group 0).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0C0 1C0 2C0 3C0 4C0 5C0 6C0 7C0 8C0
- Replicated per PState: Yes
- Exists: Always

Table 11-59 Register Name: TxDqDlyTg0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[8:0]	TxDqDlyTg0	Write DQ Delay (Timing Group 0). Trained to center the delay between the write DQ to the write DQS. Tx DQ Delay (9 bits, includes 3b coarse and 6b fine delays); (For Timing Group 0) TxDqDlyTg0[8:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqDlyTg0[4:0] is the fine (fractional UI) delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqDlyTg0[5] is reserved. Register Block Offset Address 0x0C0 controls the lane0 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x1C0 controls the lane1 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x2C0 controls the lane2 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x3C0 controls the lane3 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x4C0 controls the lane4 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x5C0 controls the lane5 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x6C0 controls the lane6 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x7C0 controls the lane7 write DQ timing. (For Timing Group 0) Register Block Offset Address 0x8C0 controls the lane{DMDBI} write DQ timing. (For Timing Group 0) These Registers are replicated per pstate. . Note: Timing Group 0 = RANK0.	R/W	0x010
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.52 TxDqDlyTg1

- Description: Write DQ Delay (Timing Group 1).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0C1 1C1 2C1 3C1 4C1 5C1 6C1 7C1 8C1
- Replicated per PState: Yes
- Exists: Always

Table 11-60 Register Name: TxDqDlyTg1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[8:0]	TxDqDlyTg1	Write DQ Delay (Timing Group 1). Trained to center the delay between the write DQ to the write DQS. Tx DQ Delay (9 bits, includes 3b coarse and 6b fine delays); (For Timing Group 1) TxDqDlyTg1[8:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqDlyTg1[4:0] is the fine (fractional UI) delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqDlyTg1[5] is reserved. Register Block Offset Address 0x0C1 controls the lane0 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x1C1 controls the lane1 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x2C1 controls the lane2 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x3C1 controls the lane3 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x4C1 controls the lane4 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x5C1 controls the lane5 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x6C1 controls the lane6 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x7C1 controls the lane7 write DQ timing. (For Timing Group 1) Register Block Offset Address 0x8C1 controls the lane{DMDBI} write DQ timing. (For Timing Group 1) These Registers are replicated per pstate. . Note: Timing Group 1 = RANK1.	R/W	0x010
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.53 TxDqDlyTg2

- Description: Write DQ Delay (Timing Group 2).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0C2 1C2 2C2 3C2 4C2 5C2 6C2 7C2 8C2
- Replicated per PState: Yes
- Exists: Always

Table 11-61 Register Name: TxDqDlyTg2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[8:0]	TxDqDlyTg2	Write DQ Delay (Timing Group 2). Trained to center the delay between the write DQ to the write DQS. Tx DQ Delay (9 bits, includes 3b coarse and 6b fine delays); (For Timing Group 2) TxDqDlyTg2[8:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqDlyTg2[4:0] is the fine (fractional UI) delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqDlyTg2[5] is reserved. Register Block Offset Address 0x0C2 controls the lane0 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x1C2 controls the lane1 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x2C2 controls the lane2 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x3C2 controls the lane3 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x4C2 controls the lane4 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x5C2 controls the lane5 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x6C2 controls the lane6 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x7C2 controls the lane7 write DQ timing. (For Timing Group 2) Register Block Offset Address 0x8C2 controls the lane{DMDBI} write DQ timing. (For Timing Group 2) These Registers are replicated per pstate. . Note: Timing Group 2 = RANK2.	R/W	0x010
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.54 TxDqDlyTg3

- Description: Write DQ Delay (Timing Group 3).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0C3 1C3 2C3 3C3 4C3 5C3 6C3 7C3 8C3
- Replicated per PState: Yes
- Exists: Always

Table 11-62 Register Name: TxDqDlyTg3 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[8:0]	TxDqDlyTg3	Write DQ Delay (Timing Group 3). Trained to center the delay between the write DQ to the write DQS. Tx DQ Delay (9 bits, includes 3b coarse and 6b fine delays); (For Timing Group 3) TxDqDlyTg3[8:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqDlyTg3[4:0] is the fine (fractional UI) delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqDlyTg3[5] is reserved. Register Block Offset Address 0x0C3 controls the lane0 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x1C3 controls the lane1 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x2C3 controls the lane2 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x3C3 controls the lane3 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x4C3 controls the lane4 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x5C3 controls the lane5 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x6C3 controls the lane6 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x7C3 controls the lane7 write DQ timing. (For Timing Group 3) Register Block Offset Address 0x8C3 controls the lane{DMDBI} write DQ timing. (For Timing Group 3) These Registers are replicated per pstate. . Note: Timing Group 3 = RANK3.	R/W	0x010
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.55 RxEnDlyTg0

- Description: Trained Receive Enable Delay (For Timing Group 0)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 080 180
- Replicated per PState: Yes
- Exists: Always

Table 11-63 Register Name: RxEnDlyTg0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[10:0]	RxEnDlyTg0	Trained Receive Enable Delay (For Timing Group 0) Trained to set the delay from the memory-read command to the signal enabling the read DQS to generate read-data strobes. The trained read DQS enable asserts during the read DQS preamble and deasserts at the end of the read burst. RxEnDlyTg0[10:6] is the coarse delay, ie one unit of delay is 1 UI. RxEnDlyTg0[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxEnDlyTg0[5] is reserved. Register Block Offset Address 0x080 controls the lower DQ nibble DqsEn. (For Timing Group 0) Register Block Offset Address 0x180 controls the upper DQ nibble DqsEn. (For Timing Group 0) These Registers are replicated per pstate. . Note: Timing Group 0 = RANK0.	R/W	0x100
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.56 RxEnDlyTg1

- Description: Trained Receive Enable Delay (For Timing Group 1)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 081 181
- Replicated per PState: Yes
- Exists: Always

Table 11-64 Register Name: RxEnDlyTg1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[10:0]	RxEnDlyTg1	Trained Receive Enable Delay (For Timing Group 1) Trained to set the delay from the memory-read command to the signal enabling the read DQS to generate read-data strobes. The trained read DQS enable asserts during the read DQS preamble and deasserts at the end of the read burst. RxEnDlyTg1[10:6] is the coarse delay, ie one unit of delay is 1 UI. RxEnDlyTg1[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxEnDlyTg1[5] is reserved. Register Block Offset Address 0x081 controls the lower DQ nibble DqsEn. (For Timing Group 1) Register Block Offset Address 0x181 controls the upper DQ nibble DqsEn. (For Timing Group 1) These Registers are replicated per pstate. . Note: Timing Group 1 = RANK1.	R/W	0x100
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.57 RxEnDlyTg2

- Description: Trained Receive Enable Delay (For Timing Group 2)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 082 182
- Replicated per PState: Yes
- Exists: Always

Table 11-65 Register Name: RxEnDlyTg2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[10:0]	RxEnDlyTg2	Trained Receive Enable Delay (For Timing Group 2) Trained to set the delay from the memory-read command to the signal enabling the read DQS to generate read-data strobes. The trained read DQS enable asserts during the read DQS preamble and deasserts at the end of the read burst. RxEnDlyTg2[10:6] is the coarse delay, ie one unit of delay is 1 UI. RxEnDlyTg2[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxEnDlyTg2[5] is reserved. Register Block Offset Address 0x082 controls the lower DQ nibble DqsEn. (For Timing Group 2) Register Block Offset Address 0x182 controls the upper DQ nibble DqsEn. (For Timing Group 2) These Registers are replicated per pstate. . Note: Timing Group 2 = RANK2.	R/W	0x100
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.58 RxEnDlyTg3

- Description: Trained Receive Enable Delay (For Timing Group 3)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 083 183
- Replicated per PState: Yes
- Exists: Always

Table 11-66 Register Name: RxEnDlyTg3 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[10:0]	RxEnDlyTg3	Trained Receive Enable Delay (For Timing Group 3) Trained to set the delay from the memory-read command to the signal enabling the read DQS to generate read-data strobes. The trained read DQS enable asserts during the read DQS preamble and deasserts at the end of the read burst. RxEnDlyTg3[10:6] is the coarse delay, ie one unit of delay is 1 UI. RxEnDlyTg3[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxEnDlyTg3[5] is reserved. Register Block Offset Address 0x083 controls the lower DQ nibble DqsEn. (For Timing Group 3) Register Block Offset Address 0x183 controls the upper DQ nibble DqsEn. (For Timing Group 3) These Registers are replicated per pstate. . Note: Timing Group 3 = RANK3.	R/W	0x100
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.59 RxClkDlyTg0

- Description: Trained Read DQS to RxClk Delay (Timing Group DEST=0).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 08C 18C
- Replicated per PState: Yes
- Exists: Always

Table 11-67 Register Name: RxClkDlyTg0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkDlyTg0	Trained Read DQS to RxClk Delay (Timing Group DEST=0). Trained to generate read DQ receive clock from the received read DQS. RxClk Delay (6 bits, fine delay only); (For Timing Group 0) RxClkDlyTg0[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkDlyTg0[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x08c controls the lower DQ nibble RxClk timing. (For Timing Group 0) Register Block Offset Address 0x18c controls the upper DQ nibble RxClk timing. (For Timing Group 0) These Registers are replicated per pstate. . Note: Timing Group 0 = RANK0.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.60 RxClkDlyTg1

- Description: Trained Read DQS to RxClk Delay (Timing Group DEST=1).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 08D 18D
- Replicated per PState: Yes
- Exists: Always

Table 11-68 Register Name: RxClkDlyTg1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkDlyTg1	Trained Read DQS to RxClk Delay (Timing Group DEST=1). Trained to generate read DQ receive clock from the received read DQS. RxClk Delay (6 bits, fine delay only); (For Timing Group 1) RxClkDlyTg1[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkDlyTg1[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x08d controls the lower DQ nibble RxClk timing. (For Timing Group 1) Register Block Offset Address 0x18d controls the upper DQ nibble RxClk timing. (For Timing Group 1) These Registers are replicated per pstate. . Note: Timing Group 1 = RANK1.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.61 RxClkDlyTg2

- Description: Trained Read DQS to RxClk Delay (Timing Group DEST=2).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 08E 18E
- Replicated per PState: Yes
- Exists: Always

Table 11-69 Register Name: RxClkDlyTg2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkDlyTg2	Trained Read DQS to RxClk Delay (Timing Group DEST=2). Trained to generate read DQ receive clock from the received read DQS. RxClk Delay (6 bits, fine delay only); (For Timing Group 2) RxClkDlyTg2[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkDlyTg2[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x08e controls the lower DQ nibble RxClk timing. (For Timing Group 2) Register Block Offset Address 0x18e controls the upper DQ nibble RxClk timing. (For Timing Group 2) These Registers are replicated per pstate. . Note: Timing Group 2 = RANK2.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.62 RxClkDlyTg3

- Description: Trained Read DQS to RxClk Delay (Timing Group DEST=3).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 08F 18F
- Replicated per PState: Yes
- Exists: Always

Table 11-70 Register Name: RxClkDlyTg3 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkDlyTg3	Trained Read DQS to RxClk Delay (Timing Group DEST=3). Trained to generate read DQ receive clock from the received read DQS. RxClk Delay (6 bits, fine delay only); (For Timing Group 3) RxClkDlyTg3[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkDlyTg3[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x08f controls the lower DQ nibble RxClk timing. (For Timing Group 3) Register Block Offset Address 0x18f controls the upper DQ nibble RxClk timing. (For Timing Group 3) These Registers are replicated per pstate. . Note: Timing Group 3 = RANK3.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.63 RxClkcDlyTg0

- Description: Trained Read DQS_c to RxClkc Delay (Timing Group DEST=0).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 090 190
- Replicated per PState: Yes
- Exists: Always

Table 11-71 Register Name: RxClkcDlyTg0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkcDlyTg0	Trained Read DQS_c to RxClkc Delay (Timing Group DEST=0). Trained to generate read DQ receive clock from the received read DQS_c. RxClkc Delay (6 bits, fine delay only); (For Timing Group 0) RxClkcDlyTg0[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkcDlyTg0[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x090 controls the lower DQ nibble RxClkc timing. (For Timing Group 0) Register Block Offset Address 0x190 controls the upper DQ nibble RxClkc timing. (For Timing Group 0) These Registers are replicated per pstate. . Note: Timing Group 0 = RANK0.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.64 RxClkcDlyTg1

- Description: Trained Read DQS_c to RxClkc Delay (Timing Group DEST=1).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 091 191
- Replicated per PState: Yes
- Exists: Always

Table 11-72 Register Name: RxClkcDlyTg1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkcDlyTg1	Trained Read DQS_c to RxClkc Delay (Timing Group DEST=1). Trained to generate read DQ receive clock from the received read DQS_c. RxClkc Delay (6 bits, fine delay only); (For Timing Group 1) RxClkcDlyTg1[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkcDlyTg1[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x091 controls the lower DQ nibble RxClkc timing. (For Timing Group 1) Register Block Offset Address 0x191 controls the upper DQ nibble RxClkc timing. (For Timing Group 1) These Registers are replicated per pstate. . Note: Timing Group 1 = RANK1.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.65 RxClkcDlyTg2

- Description: Trained Read DQS_c to RxClkc Delay (Timing Group DEST=2).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 092 192
- Replicated per PState: Yes
- Exists: Always

Table 11-73 Register Name: RxClkcDlyTg2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkcDlyTg2	Trained Read DQS_c to RxClkc Delay (Timing Group DEST=2). Trained to generate read DQ receive clock from the received read DQS_c. RxClkc Delay (6 bits, fine delay only); (For Timing Group 2) RxClkcDlyTg2[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkcDlyTg2[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x092 controls the lower DQ nibble RxClkc timing. (For Timing Group 2) Register Block Offset Address 0x192 controls the upper DQ nibble RxClkc timing. (For Timing Group 2) These Registers are replicated per pstate. . Note: Timing Group 2 = RANK2.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.66 RxClkcDlyTg3

- Description: Trained Read DQS_c to RxClkc Delay (Timing Group DEST=3).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 093 193
- Replicated per PState: Yes
- Exists: Always

Table 11-74 Register Name: RxClkcDlyTg3 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[5:0]	RxClkcDlyTg3	Trained Read DQS_c to RxClkc Delay (Timing Group DEST=3). Trained to generate read DQ receive clock from the received read DQS_c. RxClkc Delay (6 bits, fine delay only); (For Timing Group 3) RxClkcDlyTg3[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. RxClkcDlyTg3[5] is reserved. There is no coarse delay field, ie the max configurable delay is 31/32 UI. Register Block Offset Address 0x093 controls the lower DQ nibble RxClkc timing. (For Timing Group 3) Register Block Offset Address 0x193 controls the upper DQ nibble RxClkc timing. (For Timing Group 3) These Registers are replicated per pstate. . Note: Timing Group 3 = RANK3.	R/W	0x10
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.67 TxDqsDlyTg0

- Description: Write DQS Delay (Timing Group DEST=0).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0D0 1D0
- Replicated per PState: Yes
- Exists: Always

Table 11-75 Register Name: TxDqsDlyTg0 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[9:0]	TxDqsDlyTg0	Write DQS Delay (Timing Group DEST=0). Trained to set the delay from the memory-write command to the signal driving the write DQS Tx DQS Delay (10 bits, includes coarse and fine delays); (For Timing Group 0) TxDqsDlyTg0[9:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqsDlyTg0[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqsDlyTg0[5] is reserved. Register is per nibble, per timing-group, per pstate. Register Block Offset Address 0x0D0 controls the lower DQ nibble write DQS timing. (For Timing Group 0) Register Block Offset Address 0x1D0 controls the upper DQ nibble write DQS timing. (For Timing Group 0) . Note: Timing Group 0 = RANK0.	R/W	0x100
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.68 TxDqsDlyTg1

- Description: Write DQS Delay (Timing Group DEST=1).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0D1 1D1
- Replicated per PState: Yes
- Exists: Always

Table 11-76 Register Name: TxDqsDlyTg1 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[9:0]	TxDqsDlyTg1	Write DQS Delay (Timing Group DEST=1). Trained to set the delay from the memory-write command to the signal driving the write DQS Tx DQS Delay (10 bits, includes coarse and fine delays); (For Timing Group 1) TxDqsDlyTg1[9:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqsDlyTg1[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqsDlyTg1[5] is reserved. Register is per nibble, per timing-group, per pstate. Register Block Offset Address 0x0D1 controls the lower DQ nibble write DQS timing. (For Timing Group 1) Register Block Offset Address 0x1D1 controls the upper DQ nibble write DQS timing. (For Timing Group 1) . Note: Timing Group 1 = RANK1.	R/W	0x100
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.69 TxDqsDlyTg2

- Description: Write DQS Delay (Timing Group DEST=2).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0D2 1D2
- Replicated per PState: Yes
- Exists: Always

Table 11-77 Register Name: TxDqsDlyTg2 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[9:0]	TxDqsDlyTg2	Write DQS Delay (Timing Group DEST=2). Trained to set the delay from the memory-write command to the signal driving the write DQS Tx DQS Delay (10 bits, includes coarse and fine delays); (For Timing Group 2) TxDqsDlyTg2[9:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqsDlyTg2[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqsDlyTg2[5] is reserved. Register is per nibble, per timing-group, per pstate. Register Block Offset Address 0x0D2 controls the lower DQ nibble write DQS timing. (For Timing Group 2) Register Block Offset Address 0x1D2 controls the upper DQ nibble write DQS timing. (For Timing Group 2) . Note: Timing Group 2 = RANK2.	R/W	0x100
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.70 TxDqsDlyTg3

- Description: Write DQS Delay (Timing Group DEST=3).
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DBYTE
- Register Offset: 0D3 1D3
- Replicated per PState: Yes
- Exists: Always

Table 11-78 Register Name: TxDqsDlyTg3 Register-block: DWC_DDRPHYA_DBYTE

Bits	Name	Description	Access	Default
[9:0]	TxDqsDlyTg3	Write DQS Delay (Timing Group DEST=3). Trained to set the delay from the memory-write command to the signal driving the write DQS Tx DQS Delay (10 bits, includes coarse and fine delays); (For Timing Group 3) TxDqsDlyTg3[9:6] is the coarse delay, ie one unit of delay is 1 UI. TxDqsDlyTg3[4:0] is the fine delay, ie one unit of delay is one-thirtysecond of a UI = UI/32. TxDqsDlyTg3[5] is reserved. Register is per nibble, per timing-group, per pstate. Register Block Offset Address 0x0D3 controls the lower DQ nibble write DQS timing. (For Timing Group 3) Register Block Offset Address 0x1D3 controls the upper DQ nibble write DQS timing. (For Timing Group 3) . Note: Timing Group 3 = RANK3.	R/W	0x100
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.71 UcclkHclkEnables

- Description: UcClk/Hclk Enables. [UcClk and Hclk run at either DFICLK or are gated]
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DRTUB
- Register Offset: 080
- Replicated per PState: No
- Exists: Always

Table 11-79 Register Name: UcclkHclkEnables Register-block: DWC_DDRPHYA_DRTUB

Bits	Name	Description	Access	Default
[0:0]	UcclkEn	When training has completed (and assuming no further need for the microcontroller), the enable should be set to 0 to reduce power.	R/W	0x1
[1:1]	HclkEn	When training has completed (and assuming no further need for the training hardware), the enable should be set to 0 to reduce power.	R/W	0x1
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.72 CurPstate0b

- Description: PIE current Pstate value
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DRTUB
- Register Offset: 081
- Replicated per PState: No
- Exists: Always

Table 11-80 Register Name: CurPstate0b Register-block: DWC_DDRPHYA_DRTUB

Bits	Name	Description	Access	Default
[3:0]	CurPstate0b	PIE current Pstate value This register is used to select values for writing by the Pstate sequencer and is written in the beginning of the Pstate switch. It can also be used to reference which Pstate the sequencer thinks it's in.	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.73 CUSTPUBREV

- Description: Customer settable by the customer
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DRTUB
- Register Offset: 0ED
- Replicated per PState: No
- Exists: Always

Table 11-81 Register Name: CUSTPUBREV Register-block: DWC_DDRPHYA_DRTUB

Bits	Name	Description	Access	Default
[5:0]	CUSTPUBREV	The customer settable PUB version number. The value is derived from the `define DWC_DDRPHY_CUST_PUBREV	R	-
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.74 PUBREV

- Description: The hardware version of this PUB, excluding the PHY
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_DRTUB
- Register Offset: 0EE
- Replicated per PState: No
- Exists: Always

Table 11-82 Register Name: PUBREV Register-block: DWC_DDRPHYA_DRTUB

Bits	Name	Description	Access	Default
[3:0]	PUBMNR	Indicates minor update of the PUB.	R	0x0
[7:4]	PUBMDR	Indicates moderate revision of the PUB.	R	0x0
[15:8]	PUBMJR	Indicates major revision of the PUB.	R	0x22

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11.3.75 PhyInLP3

- Description: Indicator for PIE Lower Power 3 (LP3) Status
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_INITENG
- Register Offset: 028
- Replicated per PState: No
- Exists: Always

Table 11-83 Register Name: PhyInLP3 Register-block: DWC_DDRPHYA_INITENG

Bits	Name	Description	Access	Default
[0:0]	PhyInLP3	Read Only. Set to 1 by the PIE once completed LP3 Entry sequence; Cleared during LP3 Exit sequence. System software can read this csr for the status of PIE engine.	R/W	0x1
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.76 RxFifoInit

- Description: This Register enables overrides of the PHY RXDATAFIFO pointers.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 000
- Replicated per PState: No
- Exists: Always

Table 11-84 Register Name: RxFifoInit Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	RxFifoInitPtr	Setting this bit will reset the PHY RXDATAFIFO read and write pointers. This bit must be Cleared to return to normal operation. This is not required in normal operation, but can be used instead of a dfi_ctrlupdate (for controllers that don't support ctrlupdate)	R/W	0x0
[1:1]	InhibitRxFifoRd	This field is reserved for training FW use. Setting this inhibits reads of the PHYRXDATAFIFO.	R/W	0x0
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.77 ForceClkDisable

- Description: Clock gating control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 001
- Replicated per PState: No
- Exists: Always

Table 11-85 Register Name: ForceClkDisable Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	ForceClkDisable	This CSR forces the gating of MEMCLKs driven from the PHY ForceClkDisable[0] - controls CLK_{H/L}0 ForceClkDisable[1] - controls CLK_{H/L}1 (if present) ForceClkDisable[2] - controls CLK_{H/L}2 (if present) ForceClkDisable[3] - controls CLK_{H/L}3 (if present)	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.78 ForceInternalUpdate

- Description: This Register used by Training Firmware to force an internal PHY Update Event.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 003
- Replicated per PState: No
- Exists: Always

Table 11-86 Register Name: ForceInternalUpdate Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	ForceInternalUpdate	This Register is used by Training Firmware to force an internal PHY Update Event. Optionally can be used by System Software to issue a PHY update Event. The register may be written to 1'b1 only when all of the following are true: [+] The DFI interface is offline. [+] The Training Hardware is sending only DES and all transactions have retired. Additionally, this Register must stay asserted for at least 32 DFICLKs before clearing. Prematurely clearing this register may result in an incomplete update.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.79 PhyConfig

- Description: Displays PHY Configuration
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 004
- Replicated per PState: No
- Exists: Always

Table 11-87 Register Name: PhyConfig Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PhyConfigAnibs	Returns the following value ... depending on the chosen define "0x3" if DWC_DDRPHY_NUM_ANIBS_3 "0x6" if DWC_DDRPHY_NUM_ANIBS_6 "0xA" if DWC_DDRPHY_NUM_ANIBS_10 "0xC" if DWC_DDRPHY_NUM_ANIBS_12	R	-
[7:4]	PhyConfigDbytes	Returns the following value ... depending on the chosen define "0x1" if DWC_DDRPHY_NUM_DBYTES_1 "0x2" if DWC_DDRPHY_NUM_DBYTES_2 "0x3" if DWC_DDRPHY_NUM_DBYTES_3 "0x4" if DWC_DDRPHY_NUM_DBYTES_4 "0x5" if DWC_DDRPHY_NUM_DBYTES_5 "0x6" if DWC_DDRPHY_NUM_DBYTES_6 "0x7" if DWC_DDRPHY_NUM_DBYTES_7 "0x8" if DWC_DDRPHY_NUM_DBYTES_8 "0x9" if DWC_DDRPHY_NUM_DBYTES_9 "0xA" if DWC_DDRPHY_NUM_DBYTES_10	R	-
[9:8]	PhyConfigDfi	Returns the following value ... depending on the define "0x1" if DWC_DDRPHY_DFI1_EXISTS is not defined "0x2" if DWC_DDRPHY_DFI1_EXISTS is defined	R	-
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.80 PGCR

- Description: PHY General Configuration Register(PGCR)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 005
- Replicated per PState: No
- Exists: Always

Table 11-88 Register Name: PGCR Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	RxClkRiseFallMode	This register field controls independent training for RxClk_c and RxClk_t. 0: Independent training for RxClk_c and RxClk_t is disabled. 1: Independent training for RxClk_c and RxClk_t is enabled. Default Value is 0.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.81 TestBumpCntrl1

- Description: Control for Test Bumps
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 007
- Replicated per PState: No
- Exists: Always

Table 11-89 Register Name: TestBumpCntrl1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[2:0]	TestMajorMode	Selects the major mode of operation for the receiver. These modes are mutually exclusive. 000 - reserved 001 - reserved 010 - reserved 011 - setting for DDR4 systems to receive Alert_n 100 - reserved for debug 101 - reserved 110 - reserved 111 - reserved for debug	R/W	0x3
[3:3]	TestBiasBypassEn	Do not use, for debug only	R/W	0x0
[7:4]	TestAnalogOutCtrl	Select receiver internal analog signals to monitor at analog test point 0xxx: AnalogTestOut=HiZ 1000: AnalogTestOut=VSS 1001: AnalogTestOut=vref_dfe0 -- observe by sweeping MALERTVrefLevel 1010: AnalogTestOut=vref_dfe1 -- observe by sweeping MALERTVrefLevel 1011: AnalogTestOut=VSS 1100: AnalogTestOut=vstg2 1101: AnalogTestOut=vcasc_cs1 1110: AnalogTestOut=vbias_cs1 Recommended mission mode default = 4'b0000	R/W	0x0

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Table 11-89 Register Name: TestBumpCntrl1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[12:8]	TestGainCurrAdj	Adjust gain and current of analog observe RX amplifier stage at analog test point Recommended mission mode default = 5'b01011	R/W	0x0b
[13:13]	TestSelExternalVref	Do not use, for debug only	R/W	0x0
[14:14]	TestExtVrefRange	Setting this bit will extend the VREF DAC range for debug. MUST BE SET TO ZERO in mission mode when MemAlert is enabled	R/W	0x0
[15:15]	TestPowerGateEn	Do not use, for debug only	R/W	0x0

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11.3.82 TestBumpCntrl

- Description: Control for Test Bumps
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 00A
- Replicated per PState: No
- Exists: Always

Table 11-90 Register Name: TestBumpCntrl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	TestBumpEn	Field TestBumpEn[1:0] controls the output function of: the signal BP_ALERT_N. TestBumpEn Value on {BP_ALERT_N} output ---------- ---------- 2'b00 high-z, 2'b01 Pllout-divided-by-2, works up to full data rate 2'b10 PllDigTst[1], works up to 400MHz 2'b11 PllDigTst[1], works up to 400MHz	R/W	0x0
[2:2]	TestBumpToggle	This field controls the output function of the signal Digital Observation Pin, if available in the configuration of the PHY. When set to 1'b0 -- the output will be tristated When set to 1'b1 -- the output will be selected by MtestMuxSel	R/W	0x0
[8:3]	TestBumpDataSel	RVSD.	R/W	0x00
[9:9]	ForceMtestOnAlert	When set, causes the Digital Observation output pin to be driven onto BP_ALERT_N	R/W	0x0
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.83 PhyAlertStatus

- Description: This Read Only CSR represents the status of the ALERT_N pin to the PHY
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 00F
- Replicated per PState: No
- Exists: Always

Table 11-91 Register Name: PhyAlertStatus Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PhyAlert	Current state of ALERT_N.	R	-
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.84 ATestMode

- Description: Controls for Address Command Loopback. This CSR is written by ATE firmware.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 012
- Replicated per PState: No
- Exists: Always

Table 11-92 Register Name: ATestMode Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	ATestPrbsEn	Enables loopback PRBS7 testing of all the DDR output pins in this chiplet. The asserting edge resets all the individual TestPrbsErrCnt & consequently TestPrbsErr; there is no other reset for the TestPrbsErrCnt.	R/W	0x0
[1:1]	ATestClkEn	Obsolete. Unused.	R/W	0x0
[4:2]	ATestModeSel	Master Mode select for ATest (Loopback) 000 - Mission mode, all ATest disabled, loopback receivers powered down 001 - External Loopback mode [Single data rate pattern - dfi_cas sent to all lanes] 010 - Internal Loopback mode [Single data rate pattern] 011 - Internal Loopback mode [Double data rate pattern] 100 - External Loopback mode [Single data rate pattern - corresponding DFI signal sent to each lane]	R/W	0x0
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.85 TxCalBinP

- Description: TX P Impedance Calibration observation
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 014
- Replicated per PState: No
- Exists: Always

Table 11-93 Register Name: TxCalBinP Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	TxCalBinP	This csr holds the binary result of the 31 bit thermometer pullup code.	R	-
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.86 TxCalBinN

- Description: TX N Impedance Calibration observation
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 015
- Replicated per PState: No
- Exists: Always

Table 11-94 Register Name: TxCalBinN Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	TxCalBinN	This csr holds the binary result of the 31 bit thermometer pulldown code.	R	-
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.87 TxCalPOvr

- Description: Override values for Register TxCalBinP.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 016
- Replicated per PState: No
- Exists: Always

Table 11-95 Register Name: TxCalPOvr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	TxCalBinPOvrVal	The binary value which can overide the Register TxCalBinP calibrator results if Register TxCalBinPOvrEn is set.	R/W	0x00
[5:5]	TxCalBinPOvrEn	1 = use the override value present in Register TxCalBinPOvrVal 0 = don't.	R/W	0x0
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.88 TxCalNOvr

- Description: Override values for Register TxCalBinN.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 017
- Replicated per PState: No
- Exists: Always

Table 11-96 Register Name: TxCalNOvr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	TxCalBinNOvrVal	The binary value which can overide the Register TxCalBinN calibrator results if Register TxCalBinPOvrEn is set.	R/W	0x00
[5:5]	TxCalBinNOvrEn	1 = use the override value present in Register TxCalBinNOvrVal 0 = don't.	R/W	0x0
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.89 DfiMode

- Description: Each bit enables the Phy Update, Phy Master Update, and low power logic for the respective interfaces
  There are 3 valid configurations:
  'b101: DFI0 is enabled and controls the entire PHY
  'b001: DFI0 controls 1/2 the PHY, external logic ties off inputs to DFI1
  'b011: DFI0 and DFI1 are active and are separately controlled.
  This field interacts with the DWC_DDRPHY_DFI1_EXISTS define as follows:
  DfiMode=001, DWC_DDRPHY_DFI1_EXISTS defined: ANIBs/DBYTEs assigned to DFI1 are idle
  DfiMode=011, DWC_DDRPHY_DFI1_EXISTS defined: DFI0 controls 1/2 PHY (CH. A), DFI1 controls 1/2 PHY (CH. B)
  DfiMode=101, DWC_DDRPHY_DFI1_EXISTS defined: ANIBs/DBYTEs assigned to DFI1 are controlled by DFI0. Only DFI0 sideband signals are active.
  DfiMode=001, DWC_DDRPHY_DFI1_EXISTS undefined: DFI0 controls entire PHY
  DfiMode=011, DWC_DDRPHY_DFI1_EXISTS undefined: illegal
  DfiMode=101, DWC_DDRPHY_DFI1_EXISTS undefined: not applicable
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 018
- Replicated per PState: No
- Exists: Always

Table 11-97 Register Name: DfiMode Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	Dfi0Enable	Enables operation for the PHY logic associated with DFI0	R/W	0x1
[1:1]	Dfi1Enable	Enables operation for the PHY logic associated with DFI1	R/W	0x0
[2:2]	Dfi1Override	DFI0 is used to control the PHY logic associated with both DFI0 and DFI1	R/W	0x1
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.90 MtestPgmInfo

- Description: Digital Observation Pin program info for debug
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 01B
- Replicated per PState: No
- Exists: Always

Table 11-98 Register Name: MtestPgmInfo Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	MtestPgmInfo	The value of this csr may be driven onto the Digital Observation Pin. It has no other hardware effect.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.91 DynPwrDnUp

- Description: NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 01C
- Replicated per PState: No
- Exists: Always

Table 11-99 Register Name: DynPwrDnUp Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DynPowerDown	1 - analog circuitry (voltage dacs, bias gen) is turned off. 0 - normal operation.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.92 PhyTID

- Description: PHY Technology ID Register
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 01E
- Replicated per PState: No
- Exists: Always

Table 11-100 Register Name: PhyTID Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	PhyTID	This register is a placeholder to store technology-specific information	R/W	0x0000

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11.3.93 DFIPHYUPD

- Description: This Register is used to determine the DFI Update request interval and the maximum update response time.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 021
- Replicated per PState: No
- Exists: Always

Table 11-101 Register Name: DFIPHYUPD Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DFIPHYUPDCNT	This controls the interval between the end of a phyupdate transaction and a subsequent request. 4'b0000 - Disable timer-based Phy Update when DFIPHYUPDMODE==1'b0 4'b0001 - 16K MEMCLKs minus nMEMCLKs_phyupd_resp 4'b0011 - 32K MEMCLKs minus nMEMCLKs_phyupd_resp 4'b0111 - 64K MEMCLKs minus nMEMCLKs_phyupd_resp 4'b1111 - 128K MEMCLKs minus nMEMCLKs_phyupd_resp Any code not enumerated above is RSVD and should not be set.	R/W	0x7
[6:4]	DFIPHYUPDRESP	Enforces the t_phyupd_resp time, the maximum time that is allowed to controller to respond to the request for a PHY update. A dfi_error will be signaled if there is no acknowledgement of the update request within nMEMCLKs_phyupd_resp. 3'b000 nMEMCLKs_phyupd_resp= 1024 MEMCLKs, default value 3'b001 nMEMCLKs_phyupd_resp= 2048 MEMCLKs 3'b010 nMEMCLKs_phyupd_resp= 4096 MEMCLKs 3'b011 nMEMCLKs_phyupd_resp= 8192 MEMCLKs, [not allowed in LPDDR4, LPDDR4X modes] Note 1: The above are nominal values. The actual values are reduced by (2 + (DWC_DDRPHY_PIPE_DFI_MISC * MEMCLK/DfiCtlClk)) * 2 Note 2: Any code not enumerated above is RSVD and should not be set. Note 3: This signal interacts with dfi_phymstr_req. See Section 10.5.5 of the PUB Databook	R/W	0x0

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Table 11-101 Register Name: DFIPHYUPD Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[7:7]	DFIPHYUPDMODE	1'b0 [Recommended/Default] deterministic timer-based Phy Update Requests; enables multi-channel/multi-phy lockstep operation. 1'b1 Non-deterministic threshold-based Phy Update Requests; multi-channel/multi-phy operation not permitted, all reqs must be ack'd.	R/W	0x0
[11:8]	DFIPHYUPDTHRESHOLD	4'h0 Disable Threshold-based Phy Update Requests when DFIPHYUPDMODE==1'b1 Nonzero codes are the threshold value for the change in the master LCDL 1UI phase code since the last Phy Update Request that will trigger a new Phy Update Request; If (current_1UI_phase - last_1UI_phase) > DFIPHYUPDTHRESHOLD, then a Phy Update will be requested. In units of native-control phase units, Minimum value is 1. With DFIPHYUPDTHRESHOLD=1, a master LCDL dithering between two values will not cause a Phy Update Request.	R/W	0xf
[15:12]	DFIPHYUPDINTTHRESHOLD	This subfield is similar to DFIPHYUPDTHRESHOLD except that rather than affecting the Phy Update request, it affects only the threshold used to generate the VT Drift Alarm Interrupt. Further, the actual threshold is twice what is specified in the field.	R/W	0xf

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11.3.94 PdaMrsWriteMode

- Description: Controls the write DQ generation for Per-Dram-Addressing of MRS
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 022
- Replicated per PState: No
- Exists: Always

Table 11-102 Register Name: PdaMrsWriteMode Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PdaMrsWriteMode	Controls the write DQ generation per the timing requirements on the DQ signals used for Per-Dram-Addressing mode of MRS commands. When asserted, the DQ are driven for an additional UI before the logical burst and for an additonal UI after the logical burst. The early UI has the value of first logical UI, and the late UI has the value of the last logical UI. The timing of the logical burst is unchanged; no modification to csr TxDqDly is required or performed. Strongly recommended to be cleared after completing the MRS that clears MR3 A4 and for mission-mode writes, else required bubbles will be larger and the power consumed will be greater. See JEDEC MR3 A4, Per DRAM Addresssability.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.95 DFIGEARDOWNCTL

- Description: Controls whether dfi_geardown_en will cause CS and CKE timing to change.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 023
- Replicated per PState: No
- Exists: Always

Table 11-103 Register Name: DFIGEARDOWNCTL Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	DFIGEARDOWNCTL	DFIGEARDOWNCTL[0] controls whether dfi_geardown_en will cause chip-select (CS) timing to change. 0 - CS timing will not be dynamically modified wtih dfi_geardown_en 1 - CS will be delayed by an additional 1UI dynamically when dfi_geardown_en==1 Note, this CSR must be set to zero if the PHY is not in DDR4 Mode DFIGEARDOWNCTL[1] controls whether dfi_geardown_en will cause clock-enable (CKE) timing to change. 0 - CKE timing will not be dynamically modified with dfi_geardown_en 1 - CKE will be delayed by an additional 1UI dynamically when dfi_geardown_en==1 Note, this CSR must be set to zero if the PHY is not in DDR4 Mode	R/W	0x0
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.96 MasterX4Config

- Description: DBYTE module controls to select X4 Dram device mode
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 025
- Replicated per PState: No
- Exists: Always

Table 11-104 Register Name: MasterX4Config Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	X4TG	Set to 1 if this Timing Group/Rank is x4 (as opposed to x8) memory. XXX[1|0] : TxReqDest/RxReqDest 0 X4/X8. XX[1|0]X : TxReqDest/RxReqDest 1 X4/X8. X[1|0]XX : TxReqDest/RxReqDest 2 X4/X8. [1|0]XXX : TxReqDest/RxReqDest 3 X4/X8. This CSR must be written before dfi_init_start is asserted.	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.97 WrLevBits

- Description: Write level feedback DQ observability selection
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 026
- Replicated per PState: No
- Exists: Always

Table 11-105 Register Name: WrLevBits Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	WrLevForDQSL	Indicates which DQ bit is used for Write Levelization. 0000 - use DQ0 ... 0111 - use DQ7 1000 - use |DQ[3:0] 1001 - use |DQ[7:4] 1010 - use |DQ[7:0]	R/W	0x8
[7:4]	WrLevForDQSU	Indicates which DQ bit is used for Write Levelization. 0000 - use DQ0 ... 0111 - use DQ7 1000 - use |DQ[3:0] 1001 - use |DQ[7:4] 1010 - use |DQ[7:0]	R/W	0x9
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.98 EnableCsMulticast

- Description: In DDR4 Mode , this controls whether CS_N[3:2] should be multicast on CID[1:0]
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 027
- Replicated per PState: No
- Exists: Always

Table 11-106 Register Name: EnableCsMulticast Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	EnableCsMulticast	In DDR4 Mode , this controls whether CS_N[3:2] should be multicast on CID[1:0] 0 - Do not override pins corresponding to cid[1:0] (dfi_cid[1:0] will connect to the pads) 1 - Overrirde pins corresponding to cid[1:0] with dfi_cs[3:2]. (cs[3:2] will be multicast on cs[3:2] and cid[1:0])	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.99 HwtLpCsMultiCast

- Description: Drives cs_n[0] onto cs_n[1] during training
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 028
- Replicated per PState: No
- Exists: Always

Table 11-107 Register Name: HwtLpCsMultiCast Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	HwtLpCsMultiCast	When set, drives cs_n[0] onto cs_n[1] during training	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.100 Acx4AnibDis

- Description: Disable for unused ACX Nibbles
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 02C
- Replicated per PState: No
- Exists: Always

Table 11-108 Register Name: Acx4AnibDis Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[11:0]	Acx4AnibDis	When a bit is set, the corresponding ACX nibble is disabled (specifically, the I/O OE is disabled, as is the Dfi-side FIFO clock	R/W	0x000
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.101 DbyteDllModeCntrl

- Description: DLL Mode control Register in DBYTE modules
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 03A
- Replicated per PState: No
- Exists: Always

Table 11-109 Register Name: DbyteDllModeCntrl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	Unimplemented	Returns zero on reads	R	0x0
[1:1]	DllRxPreambleMode	Must be set to 1 if read DQS preamble contains a toggle, for example DDR4 or LPDDR4 read toggling preamble mode	R/W	0x0
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.102 CalOffsets

- Description: A safety register that can be used to correct systematic offsets from each calibration stage. It is not recommended to change these values from the default zero value.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 045
- Replicated per PState: No
- Exists: Always

Table 11-110 Register Name: CalOffsets Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[5:0]	CalCmpr5Offset	This value adjusts the offset-compensated DAC code for the cmpana circuit at VRef == 0.5 * VDDQ.	R/W	0x00
[9:6]	CalDrvPdThOffset	This value adjusts the driver pulldown calibration code	R/W	0x0
[13:10]	CalDrvPuThOffset	This value adjusts the driver pullup calibration code	R/W	0x0
[15:14]	Unimplemented	Returns zero on reads	R	0x0

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11.3.103 SarInitVals

- Description: This register specifies the initial value for the compensation engine. It is not recommended to change the default value.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 047
- Replicated per PState: No
- Exists: Always

Table 11-111 Register Name: SarInitVals Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[2:0]	SarInitOFFSET05	Specify the SAR starting value for OFFSET05 calibration. This is an 8 bit wide target.	R/W	0x7
[5:3]	SarInitNINT	Specify the SAR starting value for NINT calibration. This is a 5 bit wide target.	R/W	0x4
[8:6]	SarInitPEXT	Specify the SAR starting value for PEXT calibration. This is a 5 bit wide target.	R/W	0x4
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.104 CalPExtOvr

- Description: Impedance Calibration PExt Override control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 049
- Replicated per PState: No
- Exists: Always

Table 11-112 Register Name: CalPExtOvr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	CalPExtOvr	If the CSR CalPExtDis is set then the value provided here by software will be used instead of the automatically generated value which is visible via CSR CalPExt This CSR may only be written when the calibrator is not running.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.105 CalCmpr5Ovr

- Description: Impedance Calibration Cmpr 50 control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 04A
- Replicated per PState: No
- Exists: Always

Table 11-113 Register Name: CalCmpr5Ovr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[7:0]	CalCmpr5Ovr	If the CSR CalCmpr5Dis is set then the value provided here by software will be used instead of the automatically generated value which is visible via CSR CalCmpr5 This CSR may only be written when the calibrator is not running.	R/W	0x00
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.106 CalNIntOvr

- Description: Impedance Calibration NInt Override control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 04B
- Replicated per PState: No
- Exists: Always

Table 11-114 Register Name: CalNIntOvr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	CalNIntOvr	If the CSR CalNIntDis is set then the value provided here by software will be used instead of the automatically generated value which is visible via CSR CalNInt. This CSR may only be written when the calibrator is not running.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.107 CalDrvStr0

- Description: For a given calibration target these CSRs specify the drive strength(s) to be used. There is no encoding. Note The strength selected should match the external resistor value used for calibration. Make CalDrvStrPd50 value equal to CalDrvStrPu50 value.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 050
- Replicated per PState: No
- Exists: Always

Table 11-115 Register Name: CalDrvStr0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	CalDrvStrPd50	5..15 - Reserved for future. 4 - 120R pull-down and 120R NMOS pull-up at VOH=VDDQ/3 3 - 120R pull-down and 120R NMOS pull-up at VOH=VDDQ/2.5 2 - 40R pull-down and 40R PMOS pull-up 1 - 120R pull-down and 120R PMOS pull-up 0 - 120R pull-down and 120R NMOS pull-up (Default)	R/W	0x0
[7:4]	CalDrvStrPu50	5..15 - Reserved for future. 4 - 120R pull-down and 120R NMOS pull-up at VOH=VDDQ/3 3 - 120R pull-down and 120R NMOS pull-up at VOH=VDDQ/2.5 2 - 40R pull-down and 40R PMOS pull-up 1 - 120R pull-down and 120R PMOS pull-up 0 - 120R pull-down and 120R NMOS pull-up (Default)	R/W	0x0
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.108 MemAlertControl

- Description: Controls for the receiver for MemAlert (D4 Parity or WCRC Error)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 05B
- Replicated per PState: No
- Exists: Always

Table 11-116 Register Name: MemAlertControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[6:0]	MALERTVrefLevel	Sets the vref level of internal VREF DAC. Assuming the following Mission mode settings: {TestExtVrefRange,TestMajorMode} = {0011 or 0000) The VREF level chosen by the receiver follows the equation:: VREF = VDDQ*(0.51 + MALERTVrefLevel[6:0]*0.00345) The min/max values possible are: VREF_min = VDDQ*(0.51) ; VREF_max = VDDQ*(0.948)	R/W	0x00
[7:7]	MALERTVrefExtEn	When set for test/debug, selects external Vref source, This should not be set in mission mode.	R/W	0x0

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Table 11-116 Register Name: MemAlertControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[11:8]	MALERTPuStren	Controls the Pull-up termination on MALERT ========== bit[8] - controls a 240 Ohm Pull-up leg bit[9] - controls a 240 Ohm Pull-up leg bit[10] - controls a 120 Ohm Pull-up leg bit[11] - controls a 120 Ohm Pull-up leg ========== 0000 - No PullUp Strength 0001 - 240 Ohm PullUp Strength 0010 - 240 Ohm PullUp Strength 0011 - 120 Ohm PullUp Strength 0100 - 120 Ohm PullUp Strength 0101 - 80 Ohm PullUp Strength 0110 - 80 Ohm PullUp Strength 0111 - 60 Ohm PullUp Strength 1000 - 120 Ohm PullUp Strength 1001 - 80 Ohm PullUp Strength 1010 - 80 Ohm PullUp Strength 1011 - 60 Ohm PullUp Strength 1100 - 60 Ohm PullUp Strength 1101 - 48 Ohm PullUp Strength 1110 - 48 Ohm PullUp Strength 1111 - 40 Ohm PullUp Strength	R/W	0x0
[12:12]	MALERTPuEn	When set, enables the Pull-up termination on MALERT	R/W	0x0
[13:13]	MALERTRxEn	1 - Enables receiver and received data is forwared to dfi_alert_n. 0 - Disable the receiver and send MALERTDisableVal to dfi_alert_n	R/W	0x0
[14:14]	MALERTDisableVal	When MALERTRxEn is not set, this CSR state is used to drive dfi_alert_n.	R/W	0x1
[15:15]	MALERTForceError	When MALERTForceError is set, this CSR state is used to force parity error to memory.	R/W	0x0

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11.3.109 MemAlertControl2

- Description: Controls for the MemAlert output (dfi_alert_n)
  The DFI interface defines that the signal dfi_alert_n as a synchronous output on DFICLK.
  For some memory systems, this signal is synchronized again elsewhere in the SOC, so the synchronizer in the PHY is useless (and simply adds to the latency of observing an ALERT transition.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 05C
- Replicated per PState: No
- Exists: Always

Table 11-117 Register Name: MemAlertControl2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	MALERTSyncBypass	MALERTSyncBypass==[0], the phy will drive dfi_alert_n with a synchronized value of the ALERT_N receiver. MALERTSyncBypass==[1], the phy will drive dfi_alert_n with the asynchronous value of the ALERT_N receiver.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.110 MemResetL

- Description: Control the MemResetL output of the PHY. Intended to be used to protect/force the BP_MemReset_L output.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 060
- Replicated per PState: No
- Exists: Always

Table 11-118 Register Name: MemResetL Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	MemResetLValue	Control the MemResetL output of the PHY. The state of this field is transfered to the PHY BP_MemReset_L output when ProtectMemReset is set.	R/W	0x0
[1:1]	ProtectMemReset	Control the MemResetL output of the PHY. The state of the MemResetL field is transfered to the PHY BP_MemReset_L output when ProtectMemReset is set.	R/W	0x0
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.111 PUBMODE

- Description: Selects between HWT and DCT as the source of memory transactions.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 06E
- Replicated per PState: No
- Exists: Always

Table 11-119 Register Name: PUBMODE Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	HwtMemSrc	When this is set to a 1, the mux that switches between DCT and HWT for the source of memory transactions is switched to HWT. Setting this bit relinquishes control to the HWT. Clearing this bit relinquishes control to the DCT. The transition can only be made when the FIFOs are all in PtrInit (i.e. all PtrInit signals are high).	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.112 MiscPhyStatus

- Description: This Read Only CSR represent misc status of the PHY
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 06F
- Replicated per PState: No
- Exists: Always

Table 11-120 Register Name: MiscPhyStatus Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DctSane	Returns the status of the custom circuit which protects the MemResetL output of the PHY on initial power-on or reset. This circuit resets to 0 meaning that hardware has control of the MemResetL output. If set to 1, memory RESET is being controlled by Registers MemResetLVaue and ProtectMemReset or dfi_reset_n.	R	-
[1:1]	PORMemReset	Returns the active-high value used by the custom circuit which drives the memory RESET signal. To comply with JEDEC specifications for memory reset, this signal powers on 1'b1. This signal is reset during the PHY Initialization sequence.	R	-
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.113 CoreLoopbackSel

- Description: Controls whether the loopback path bypasses the final PAD node.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 070
- Replicated per PState: No
- Exists: Always

Table 11-121 Register Name: CoreLoopbackSel Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	CoreLoopbackSel	This register is controlled by the PHY test firmware This register enables Core-Side loopback operation of the PHY. When set, the PHY PAD node will be bypassed, and pre-pad node will be selected for sampling by the PHY RX. Setting this register enables full-speed loopback operation of the PHY regardless of the loading of the pad. This register must be set to 1'b0 for mission mode operation (or pad-side loopback).	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.114 DllTrainParam

- Description: DLL Training Parameters
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 071
- Replicated per PState: No
- Exists: Always

Table 11-122 Register Name: DllTrainParam Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	ExtendPhdTime	Used by the PHY firmware locking the LCDL delay cells. The number of extra DfiClk periods (= 4*UI) for the DLL phase-detector outputs to become not-metastable	R/W	0x2
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.115 HwtLpCsEnBypass

- Description: CSn Disable Bypass for LPDDR3/4
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 074
- Replicated per PState: No
- Exists: Always

Table 11-123 Register Name: HwtLpCsEnBypass Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	HwtLpCsEnBypass	When set, these bits disable LpCsEn function for LPDDR3/4	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.116 DfiCAMode

- Description: This CSR controls the PHY signal-to-bump-mapping mode. The default state is all bits 0. Setting bits fields to 1 changes the arch mode and are required to be 1-hot. While all fields of this csr are present in all products, some will not always be relevant as a particular dram type may not be supported. Irrelevant bits must be set to 0, always. Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() according to PHY configuration and DRAM type.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 075
- Replicated per PState: No
- Exists: Always

Table 11-124 Register Name: DfiCAMode Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DfiLp3CAMode	Controls the output data-rate of the AC module Command/Address pins Field must be set to 0.	R/W	0x0
[1:1]	DfiD4CAMode	Enable DDR4 Mode 0: D4 mode disabled 1: D4 mode enabled	R/W	0x0
[2:2]	DfiLp4CAMode	Enable LP4 Mode 0: LP4 mode disabled 1: LP4 mode enabled	R/W	0x0
[3:3]	DfiD4AltCAMode	Enable DDR4-Alt Mode (only available in certain configurations) 0: D4-Altmode disabled 1: D4-Altmode enabled	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.117 DllControl

- Description: NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 078
- Replicated per PState: No
- Exists: Always

Table 11-125 Register Name: DllControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DllResetRelock	Used to reset the DDL/LCDL lock state machine. Deasserting starts locking sequence. This must be done anytime the DLLs are to be relocked (e.g. frequency change).	R/W	0x1
[1:1]	DllResetSlave	Reserved.	R/W	0x1
[2:2]	DllResetRSVD	RSVD for future use	R/W	0x0
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.118 PulseDllUpdatePhase

- Description: This register is used only for test and for training; it is not used in PIE frequency change or power-state change.
  The CfgWE for this register causes a UpdatePhase, aka ClkPhase, for the DLL associated with the subfield enables.
  Writing a 1 to one of the PulseXDllUpdatePhase will cause a pulse, ie it will assert ClkPhase=1 then clear ClkPhase=0.
  There is no need to write a 0 after writing a 1 to one of the PulseXDllUpdatePhase.
  A written 1 will read back a 1, but that does not mean that ClkPhase to the corresponding DLL is being held high.
  Writing this CSR must be in a traffic bubble.
  Writing all-0s to this register is a nop for the DLLs; it will clear any readback values if they were set.
  This function requires Register AlwaysEnCfgClk=1.
  Example to update the active Phases of the DBYTE module DLLs (nop for AC module DLLs):

```
io_write16(c0 | tMASTER | csr_CalAndPllConfig_ADDR, csr_AlwaysEnCfgClk_MASK);

io_write16(cbrd | tANIB | csr_PulseDllUpdatePhase_ADDR, csr_PulseDbyteDllUpdatePhase_MASK);

io_write16(cbrd | tANIB | csr_PulseDllUpdatePhase_ADDR, 0x0);
```

- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 079
- Replicated per PState: No
- Exists: Always

Table 11-126 Register Name: PulseDllUpdatePhase Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PulseDbyteDllUpdate Phase	Causes a LongBubble to the DBYTE modules, which causes a update of the DBYTE module DLLs (tx,rxen,rxclk). The value of Register UpdatePhaseDest must be setup prior to this pulse.	R/W	0x0
[1:1]	PulseACkDllUpdateP hase	Causes an AC module CK (memck) DLL phase update. This should be written with 1 only when the memory CKE=0 or memory RST=0, or when there is no memory, as in tester mode.	R/W	0x0
[2:2]	PulseACaDllUpdateP hase	Causes an AC module CA (command/address/cke/odt) DLL phase update.	R/W	0x0

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Table 11-126 Register Name: PulseDllUpdatePhase Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[5:3]	UpdatePhaseDestReserved	reserved, not used	R/W	0x0
[6:6]	TrainUpdatePhaseOnLongBubble	Causes LongBubble to update the dbyte & anib LDCL Phase. May be used for training, but not to be used for mission mode.	R/W	0x0
[7:7]	AlwaysUpdateLcdlPhase	Causes each new operation to reload the LcdlPhase; will increase bubbles.	R/W	0x0
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.119 CalRate

- Description: This CSR controls the impedance calibration engine in the PHY.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 088
- Replicated per PState: No
- Exists: Always

Table 11-127 Register Name: CalRate Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	CalInterval	This CSR specifies the interval between successive calibrations, in mS. csrValue : Interval (mS) 0 : 0 (continuous) 1 : 0.010 2 : 0.10 3 : 1 4 : 2 5 : 3 6 : 4 7 : 8 8 : 10 9 : 20 10-15 : Reserved. This field should only be changed while the calibrator is idle. ie before csr CalRun is set. The calibration intervals are valid only at DFICLK frequency >=24MHz. If the DFICLK frequency is less than 24MHz, the interval may be up to 2.4x larger than the value programmed in the register.	R/W	0x9

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Table 11-127 Register Name: CalRate Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:4]	CalRun	1: A calibration sequence will be triggered by the 0->1 transition of this bit, as determined by CSR CalOnce. 0: Calibrator will not run. If already active then it will complete the current sequence before quiescing. The default value of this field is 0 because the calibrator needs to know the correct operating mode before it starts up. This csr won't do anything while CalZap is asserted.	R/W	0x0
[5:5]	CalOnce	The setting of this CSR changes the behaviour of CSR CalRun. 1: The 0->1 transition of CSR CalRun causes a single iteration of the calibration sequence to occur. Once the calibration is complete, the calibration engine will remain IDLE until another CalRun Trigger. 0: Calibration will proceed at the rate determined by Register CalInterval. This field should only be changed while the calibrator is idle. ie before csr CalRun is set.	R/W	0x0
[6:6]	DisableBackgroundZQUpdates	Reserved for debug only. When this bit is set, ZQ compensation code updates will occur only during a DFI sideband {PHYUPDATE,CTRLUPDATE,PHYMSTR} handshake. This debug feature must be disabled if DFI1 is active.	R/W	0x0
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.120 CalZap

- Description: Impedance Calibration Zap/Reset
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 089
- Replicated per PState: No
- Exists: Always

Table 11-128 Register Name: CalZap Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	CalZap	NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten. Setting this csr resets the calibrator to its idle state. Must be cleared in order for the calibration engine to run again.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.121 PState

- Description: PSTATE Selection
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 08B
- Replicated per PState: No
- Exists: Always

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Table 11-129 Register Name: PState Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PState	NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten. The current PState inferred by the PIE from handshake requests on DFI status interface. 0000 - PState P0 0001 - PState P1 0010 - PState P2 0011 - PState P3 0100 - Reserved 0101 - Reserved 0110 - Reserved 0111 - Reserved 1000 - Reserved 1001 - Reserved 1010 - Reserved 1011 - Reserved 1100 - LP2 1101 - Reserved 1110 - Reserved 1111 - LP3 The lower two bits of this CSR are used to select the PHY's current Pstate for all Pstateable registers. Note: It is a don't care what value is selected in either LP2 or LP3 because no transactions will be taking place when in those states.	R/W	0xc
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.122 PllOutGateControl

- Description: NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 08D
- Replicated per PState: No
- Exists: Always

Table 11-130 Register Name: PllOutGateControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PclkGateEn	Reserved.	R/W	0x0
[1:1]	Reserved2x1	Reserved for future.	R/W	0x0
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.123 PorControl

- Description: Power On Reset Control. Register is written PIE during PHY operation.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 090
- Replicated per PState: No
- Exists: Always

Table 11-131 Register Name: PorControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllDllLockDone	Set by the PIE to 1 during execution, Cleared on PHY Reset or on power cycle. When Set, releases control of PHY I/O's from power on defaults. Note: This is a legacy register name and no longer represents when PHY internal PLL or DLL is locked.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.124 CalBusy

- Description: Impedance Calibration Busy Status
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 097
- Replicated per PState: No
- Exists: Always

Table 11-132 Register Name: CalBusy Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	CalBusy	Read 1 if the calibrator is actively calibrating. Any changes to calibrator-related CSRs may only be made if the calibrator is disabled (via CSR CalRun) and this CSR reads 0.	R	-
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.125 CalMisc2

- Description: Second set of miscellaneous impedance calbrator controls.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 098
- Replicated per PState: No
- Exists: Always

Table 11-133 Register Name: CalMisc2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[2:0]	CalNumVotes	This CSR controls the number of consecutive comparator output bits over which majority voting is done. The result of the voting is fed into the SAR. The voting is initiated after the time configured via csrs CalSlowCmpana has elapsed. CSR Value : number of Votes 0 : 1 1 : 9 2 : 17 3 : 33 4 : 65 (defaults) 5 : 129 6 : 193 7 : 255	R/W	0x4
[10:3]	Reserved10x3	Reserved for future use.	R/W	0x00
[11:11]	Reserved11	Reserved for future use. Formerly used to Skip ODT calibration if required.	R/W	0x0
[12:12]	CalCmptrResTrim	Reserved for future use.	R/W	0x0

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Table 11-133 Register Name: CalMisc2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[13:13]	CalCancelRoundErrDis	The PEXT calibration result and NINT calibration results naturally include a rounding error which manifests as a change of impedance at the pad. Where both of these errors are in the same direction the PEXT calibration result will be adjusted by 1 to offset NINT error. Setting thie csr to 1 prevents this adjustment.	R/W	0x0
[14:14]	CalSlowCmpana	When set, this CSR increases the time allowed for the cmpana cell to settle, by 50%. It changes from 3 to 6 refClk ticks.	R/W	0x0
[15:15]	Reserved15		R/W	0x0

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11.3.126 CalMisc

- Description:
  Table of impedance calibration CSR relatedness:

```
-----------------------------------------------------------------------------------
                 :  working  : R_W viewing : over-ride  : offset CSR      :
target    aka    :   state   :    CSR      :   CSR      : offset CSR      : dest CSR
-----------------------------------------------------------------------------------
OFFSET05 CalCmpr5 : resCalCmpr5 : CalCmpr5    : CalCmpr5Ovr : CalCmpr5Offset   : --
NINT    CalDrvPd5 : resCalNInt  : CalNInt     : CalNIntOvr  : {CalDrvPdOffset,  : --
                 :            :            :             : CalDrvPdThOffset} :
PEXT    CalDrvPu5 : resCalPExt  : CalPExt     : CalPExtOvr  : {CalDrvPuOffset,  : --
                 :            :            :             : CalDrvPuThOffset} :
-----------------------------------------------------------------------------------
```

  Miscellaneous calibration control knobs. These values may only be changed when the calibrator is not running.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 09A
- Replicated per PState: No
- Exists: Always

Table 11-134 Register Name: CalMisc Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	CalCmpr5Dis	Setting this CSR prevents the calibration engine from using the result from the CalCmpr5 stage of calibration. Software must supply a replacement value via CSR CalCmpr5Ovr.	R/W	0x0
[1:1]	CalNIntDis	Setting this CSR prevents the calibration engine from overwriting the CSRs TxCalBinN and TxCalThN with an automatically generated value, in which case a value must be supplied by software.	R/W	0x0
[2:2]	CalPExtDis	Setting this CSR prevents the calibration engine from overwriting the CSRs TxCalBinP and TxCalThP with an automatically generated value, in which case a value must be supplied by software.	R/W	0x0

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Table 11-134 Register Name: CalMisc Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:3]	Unimplemented	Returns zero on reads	R	0x0

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11.3.127 CalVRefs

- Description: VREF code for Comparator offset compensation.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 09B
- Replicated per PState: No
- Exists: Always

Table 11-135 Register Name: CalVRefs Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	CalVRefs	This CSR drives the Cmpdig_CalRef pin of the cmpana cell at various stages of calibration. Following are the encoding values 2'b00 - 40% Vref 2'b01 - 41.34% Vref 2'b10 - 50% Vref (Default) 2'b11 - 60% Vref	R/W	0x2
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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11.3.128 CalCmpr5

- Description: Impedance Calibration Cmpr control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 09C
- Replicated per PState: No
- Exists: Always

Table 11-136 Register Name: CalCmpr5 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[7:0]	CalCmpr5	Returns the offset-compensated DAC code for the cmpana circuit at VRef == 0.5 * VDDQ.	R	-
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.129 CalNInt

- Description: Observation of callibration engine pulldown calibration code.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 09D
- Replicated per PState: No
- Exists: Always

Table 11-137 Register Name: CalNInt Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	CalNIntThB	The value here is the number of thermometer bits which are set.	R	-
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.130 CalPExt

- Description: Observation of callibration engine pullup calibration code.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 09E
- Replicated per PState: No
- Exists: Always

Table 11-138 Register Name: CalPExt Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	CalPExtThB	The value here is the number of thermometer bits which are set.	R	-
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.131 CalCmpInvert

- Description: A safety bit for each calibration target, which controls the inversion (or not) of the comparator output before it is sampled. A 1 in the CSR causes the comparator output to be inverted.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0A8
- Replicated per PState: No
- Exists: Always

Table 11-139 Register Name: CalCmpInvert Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	CmpInvertCalDac50		R/W	0x1
[1:1]	CmpInvertCalDrvPd50		R/W	0x1
[2:2]	CmpInvertCalDrvPu50		R/W	0x0
[3:3]	CmpInvertCalOdtPd		R/W	0x0
[4:4]	CmpInvertCalOdtPu		R/W	0x0
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.132 CalCmpanaCntrl

- Description: This register control the cmpana custom circuit analog control. It is not recommended to change their values from the reset values.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0AE
- Replicated per PState: No
- Exists: Always

Table 11-140 Register Name: CalCmpanaCntrl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[7:0]	CmprGainCurrAdj		R/W	0x12
[8:8]	CmprGainResAdj		R/W	0x1
[9:9]	CmprBiasBypassEn		R/W	0x0
[15:10]	Unimplemented	Returns zero on reads	R	0x0

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11.3.133 MasUpdGoodCtr

- Description: Counts successful PHY Master Interface Updates (PPTs)
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B5
- Replicated per PState: No
- Exists: Always

Table 11-141 Register Name: MasUpdGoodCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	MasUpdGoodCtr	This register increments whenever the Memory Controller acknowledges a PHY Master Interface request (i.e., a request for the PHY to take over the DFI for Periodic Phase Training (PPT)). (As per section 11 of the Preliminary DFI 4.0 Specification Rev. 2) In a 2-channel system, both MC channels must ack. The counter saturates at max value 65535.	R	-

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11.3.134 PhyUpd0GoodCtr

- Description: Counts successful PHY-initiated DFI0 Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B6
- Replicated per PState: No
- Exists: Always

Table 11-142 Register Name: PhyUpd0GoodCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	PhyUpd0GoodCtr	This register increments whenever the Memory Controller acknowledges a PHY-initiated DFI0 interface update request. The counter saturates at max value 65535.	R	-

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11.3.135 PhyUpd1GoodCtr

- Description: Counts successful PHY-initiated DFI1 Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B7
- Replicated per PState: No
- Exists: Always

Table 11-143 Register Name: PhyUpd1GoodCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	PhyUpd1GoodCtr	This register increments whenever the Memory Controller acknowledges a PHY-initiated DFI1 interface update request. The counter saturates at max value 65535.	R	-

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11.3.136 CtlUpd0GoodCtr

- Description: Counts successful Memory Controller DFI0 Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B8
- Replicated per PState: No
- Exists: Always

Table 11-144 Register Name: CtlUpd0GoodCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	CtlUpd0GoodCtr	This register increments whenever the PHY acknowledges a Memory Controller-initiated DFI0 interface update request. The counter saturates at max value 65535.	R	-

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11.3.137 CtlUpd1GoodCtr

- Description: Counts successful Memory Controller DFI1 Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B9
- Replicated per PState: No
- Exists: Always

Table 11-145 Register Name: CtlUpd1GoodCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	CtlUpd1GoodCtr	This register increments whenever the PHY acknowledges a Memory Controller-initiated DFI1 interface update request. The counter saturates at max value 65535.	R	-

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11.3.138 MasUpdFailCtr

- Description: Counts unsuccessful PHY Master Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0BA
- Replicated per PState: No
- Exists: Always

Table 11-146 Register Name: MasUpdFailCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	MasUpdFailCtr	This register increments whenever the PHY asserts a PHY Master Interface request, but the Memory Controller doesn't acknowledge the request within the allowed interval. (As per section 11 of the Preliminary DFI 4.0 Specification Rev. 2) The counter saturates at max value 65535. In a 2-channel system, a failure occurs if either MC channels fails to ack.	R	-

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11.3.139 PhyUpd0FailCtr

- Description: Counts unsuccessful PHY-initiated DFI0 Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0BB
- Replicated per PState: No
- Exists: Always

Table 11-147 Register Name: PhyUpd0FailCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	PhyUpd0FailCtr	This register increments whenever the PHY asserts a DFI0 Interface update request, but the Memory Controller doesn't acknowledge the request within the allowed interval. (As per section 11 of the Preliminary DFI 4.0 Specification Rev. 2) The counter saturates at max value 65535.	R	-

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11.3.140 PhyUpd1FailCtr

- Description: Counts unsuccessful PHY-initiated DFI1 Interface Updates
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0BC
- Replicated per PState: No
- Exists: Always

Table 11-148 Register Name: PhyUpd1FailCtr Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	PhyUpd1FailCtr	This register increments whenever the PHY asserts a DFI1 Interface update request, but the Memory Controller doesn't acknowledge the request within the allowed interval. (As per section 11 of the Preliminary DFI 4.0 Specification Rev. 2) The counter saturates at max value 65535.	R	-

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11.3.141 PhyPerfCtrEnable

- Description: Each bit corresponds to one performance counter. Set the bit to enable the counter. Clearing the bit stops and clears the counter.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0BD
- Replicated per PState: No
- Exists: Always

Table 11-149 Register Name: PhyPerfCtrEnable Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	MasUpdGoodCtl	Enables MasUpdGoodCtr	R/W	0x0
[1:1]	PhyUpd0GoodCtl	Enables PhyUpd0GoodCtr	R/W	0x0
[2:2]	PhyUpd1GoodCtl	Enables PhyUpd1GoodCtr	R/W	0x0
[3:3]	CtlUpd0GoodCtl	Enables CtlUpd0GoodCtr	R/W	0x0
[4:4]	CtlUpd1GoodCtl	Enables CtlUpd1GoodCtr	R/W	0x0
[5:5]	MasUpdFailCtl	Enables MasUpdFailCtr	R/W	0x0
[6:6]	PhyUpd0FailCtl	Enables PhyUpd0FailCtr	R/W	0x0
[7:7]	PhyUpd1FailCtl	Enables PhyUpd1FailCtr	R/W	0x0
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.142 PllPwrDn

- Description: PLL Power Down
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C3
- Replicated per PState: No
- Exists: Always

Table 11-150 Register Name: PllPwrDn Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllPwrDn	NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten. Places the PLL in Power Down when asserted.	R/W	0x1
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.143 PllReset

- Description: PLL Reset
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C4
- Replicated per PState: No
- Exists: Always

Table 11-151 Register Name: PllReset Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllReset	Reserved	R/W	0x1
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.144 PllCtrl0

- Description: NOTE : This CSR is written by PHY Initialization Engine (PIE) and the data in here will be overwritten.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C6
- Replicated per PState: No
- Exists: Always

Table 11-152 Register Name: PllCtrl0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllStandby	Connects directly to standby pin of PLL. Puts PLL into standbymode.	R/W	0x0
[1:1]	PllBypSel	Reserved.	R/W	0x0
[2:2]	PllX2Mode	conects to x2_mode pins of PLL. pllout_x4x2 output frequency selection. 0: PLOUT_X4X2 output = 4*pllin_x1 frequency 1: PLOUT_X4X2 output = 2*pllin_x1 frequency	R/W	0x0
[3:3]	PllOutBypEn	Controls the antiglitch mux on the pllout_x1x2x4 path 1: pllout_x1x2x4 = byp_pllin_x1 0: pllout_x1x2x4 = VCO (SCD) (selected by x2_mode)	R/W	0x1
[4:4]	PllPreset	Put PLL in preset mode.	R/W	0x0
[5:5]	PllBypassMode	PLL Bypass clock mux control. If set, BypassPclk input will be used as byp_pll1x_in clock for PLL. Default 0.	R/W	0x0
[6:6]	PllSelDfiFreqRatio	reserved.	R/W	0x0
[7:7]	PllSyncBusFlush	Used to flush the syncbus logic of the PLL during PHY initialization or LP3 Exit sequence. Should Only be toggled when synbus is not used and Register PllOutBypEn is asserted.	R/W	0x0
[8:8]	PllSyncBusByp	When asserted bypasses the Pll SyncPulse and uses a synchronizer of the same latency.	R/W	0x0

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Table 11-152 Register Name: PllCtrl0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[10:9]	PllReserved10x9	for future use.	R/W	0x0
[11:11]	PllGearShift	Puts PLL in fast re-locking mode 0: default, normal mode 1: fast relock gear	R/W	0x0
[12:12]	PllLockCntSel	Lock detect counter selection. 0: Normal lock detector behavior phase lock 1: Test mode (Shorten lock cycle count 16->8)	R/W	0x0
[14:13]	PllLockPhSel	Lock detect phase selection. 0: Test mode reduced lock window 1: Default operation phase lock 2: Test mode (mismatch check) 3: Test mode (+80ps window)	R/W	0x1
[15:15]	PllSpareCtrl0	Spare bits for PLL control.	R/W	0x0

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11.3.145 PllTst

- Description: Control Register for PLL Test
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C8
- Replicated per PState: No
- Exists: Always

Table 11-153 Register Name: PllTst Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllAnaTstEn	Connects directly to pll_ana_test_en of PLL. Analog test port enable 0 = analog test port disabled (hi-Z) 1 = analog test port enabled	R/W	0x0

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Table 11-153 Register Name: PllTst Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:1]	PllAnaTstSel	Connects directly to pll_ana_test_sel<3:0> of PLL. Control bits are decoded to enable various analog test signals to be brought out via analog test pin (pll_analog_test). Table below provides decode detail. |PllAnaTstSel | Pll Analog | Description | [4:1] | Pin Function | |========== | 0000 | Hi-Z | This code should be set when the PLL | | | is in normal use or when the digital | | | test port is being used for accurate | | | timing measurements | 0001 | core | Override vmarg_ext with analog pin | 0010 | core | Override regulator input with analog pin | 0011 | core | Observe gd voltage on analog test pin | 0100 | core | Observe vp voltage on analog test pin | 0101 | core | Observe vph voltage on analog test pin | 0110 | core | Observe vreg_cp voltage on analog test pin | 0111 | core | Observe v2i current (~10uA) on analog test pin | 1000 | core | Observe vreg_v2i voltage on analog test pin | 1001 | core | Observe vbp voltage from current source on | | | analog pin | 1010 | core | Observe vbn voltage from current source on | | | analog tpin | 1011 | core | NC | 1100 | core | NC | 1101 | VSS | 0v probe ir drop test | 1110 | VP | Core supply probe SCD IR drop test | 1111 | VPH | Core Supply probe Refdiv IR drop test	R/W	0x0

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Table 11-153 Register Name: PllTst Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[8:5]	PllDigTstSel	Connects directly to pll_dig_test_sel<2:0> of PLL. Digital test mux select. Control bits are decoded to enable various digital test signals to be brought out via digital test pin, see decoder table for detail. PllDigTstOut[1] is observable on BP_ALERT and Digital Observation Pin via MtestMuxSel logic. (if enabled in this configuration) PllDigTstOut[0] is observable on Digital Observation Pin via MtestMuxSel logic only. During mission mode PllDigTstSel should be set to 3'h0. Byp = PllBypassMode CSR value Sel = PllDigTstSel CSR value |---------- | | | PllDigTstOut | |Byp| Sel | [1] [0] | Description |========== ========== | 0 | 000 | 0 | 0 | This code should be set during normal use | | | | | to minimize clock jitter | 0 | 001 | fbk_clk_ldet | pllin_x1 | Buffered version of fbk_clk at PFD input | 0 | 010 | ref_clk_ldet | pllin_x1 | Buffered version of ref_clk at PFD input | 0 | 011 | pllin_x1 | pllin_x1 | For calibrating delay skew between two | | | | | test outputs - input reference clock | 0 | 100 | clk_fbk | pllin_x1 | Buffered version of pllout_x1 | 0 | 101 | pllout_amux_x1x2x4 | pllin_x1 | Syncbus clock output (Fout<Fmax_dto only) | 0 | 110 | en_count | pll_lock | Lock detector state test | 0 | 111 | standby_eff | eoc | Calibration state test | 1 | 000 | 0 | 0 | This code should be set during normal use | | | | | to minimize clock jitter | 1 | 001 | fbk_clk_ldet | pllin_x1 | Buffered version of fbk_clk at PFD input | | | | | if PLL in mission/byp 1 modes | 1 | 010 | ref_clk_ldet | pllin_x1 | Buffered version of ref_clk at PFD input | | | | | if PLL in mission/byp 1 modes | 1 | 011 | pllin_x1 | pllin_x1 | For calibrating delay skew between two | | | | | test outputs - input reference clock | 1 | 100 | clk_fbk | pllin_x1 | Buffered version of pllout_x1 if PLL in | | | | | mission/byp 1 modes | 1 | 101 | pllout_amux_x1x2x4 | pllin_x1 | Syncbus clock output (Fout<Fmax_dto only)	R/W	0x0

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Table 11-153 Register Name: PllTst Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.146 PllLockStatus

- Description: PLL's pll_lock pin output
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C9
- Replicated per PState: No
- Exists: Always

Table 11-154 Register Name: PllLockStatus Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllLockStatus	Directly connected to the pll_Lock output. When asserted Pll macro has asserted the Lock status. To avoid metastability issues, this register should perform a majority-vote after reading this register several times.	R	-
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.147 PllCtrl3

- Description: It is recommended to use default values for this CSR. Otherwise, it can be programmed by bios or other means.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0CB
- Replicated per PState: No
- Exists: Always

Table 11-155 Register Name: PllCtrl3 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PllSpare	Spare bits for future PLL control modes	R/W	0x0
[8:4]	PllMaxRange	connects directly to maxrange of PLL. Setting for Saturation control of PLL.	R/W	0x1f
[13:9]	PllDacValIn	connects directly to dacval_in<4:0> of PLL. Calibration DAC input current setting, can be forced at rising edge of preset if force_cal =1	R/W	0x00
[14:14]	PllForceCal	connects directly to force_cal of PLL. Forces Calibration code dacval_in<4:0> to be used at preset mode if force_cal=1 if force_cal=0 previous stored value will be used	R/W	0x0
[15:15]	PllEnCal	Calibration will run at standby rising edge if en_cal=1 if en_cal=0 calibration will not run	R/W	0x0

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11.3.148 PllEndofCal

- Description: PLL's eoc (end of calibration) output
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0CD
- Replicated per PState: No
- Exists: Always

Table 11-156 Register Name: PllEndofCal Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllEndofCal	Directly connected to the pll's eoc output.	R	-
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.149 PllStandbyEff

- Description: PLL's standby_eff (effective standby) output
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0CE
- Replicated per PState: No
- Exists: Always

Table 11-157 Register Name: PllStandbyEff Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PllStandbyEff	Returns state off PLL standby. PLL will be in standby in PHY LP2 states.	R	-
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.150 PllDacValOut

- Description: PLL's Dacval_out output
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0CF
- Replicated per PState: No
- Exists: Always

Table 11-158 Register Name: PllDacValOut Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	PllDacValOut	Directly connected to the pll's dacval_out output. Used for observation of PLL DAC code.	R	-
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.151 LcdlDbgCntl

- Description: Controls for use in observing and testing the LCDLs.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0E3
- Replicated per PState: No
- Exists: Always

Table 11-159 Register Name: LcdlDbgCntl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[8:0]	LcdlFineOvrVal	Value forced as the initial value while LcdlTstEnable=1 and LcdlFineOvr. After the deassertion of LcdlFineOvr, the locking state-machine will attempt locking.	R/W	0x000
[9:9]	LcdlFineOvr	Forces the value of the present LCDL 1UI estimate code to be LcdlFineOvrVal for all LCDLs.	R/W	0x0
[10:10]	LcdlFineSnap	Latch enable for reading the present LCDL 1UI estimate code in LcdlFineSnapVal and the present phase-detector value in LcdlPhdSnapVal	R/W	0x0
[11:11]	LcdlTstEnable	Enables the debug/test operations and status Ovr,Snap,StickyLock,StickyUnlock, and LiveLock.	R/W	0x0

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Table 11-159 Register Name: LcdlDbgCntl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:12]	LcdlStatusSel	Selects the LCDL status, from among the status for the 16 LCDLs in the DBYTE, for reading via Register DxLcdlStatus and an LCDL from among the LCDLs in the ANIB for reading via Register AcLcdlStatus LcdlStatusSel source for DxLcdlStatus source for AcLcdlStatus 15 lcdl_rxclk1t reserved 14 lcdl_rxclk0t reserved 13 lcdl_rxclk1c reserved 12 lcdl_rxclk0c reserved 11 lcdl_rxen1 anib11-tx 10 lcdl_rxen0 anib10-tx 9 lcdl_txln9 (dqs-lower) anib9-tx 8 lcdl_txln8 (dm/dqs-upper) anib8-tx 7 lcdl_txln7 (dq7) anib7-tx 6 lcdl_txln6 (dq6) anib6-tx 5 lcdl_txln5 (dq5) anib5-tx 4 lcdl_txln4 (dq4) anib4-tx 3 lcdl_txln3 (dq3) anib3-tx 2 lcdl_txln2 (dq2) anib2-tx 1 lcdl_txln1 (dq1) anib1-tx 0 lcdl_txln0 (dq0) anib0-tx	R/W	0x0

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11.3.152 AcLcdlStatus

- Description: Status of anib macro LCDL selected by Register LcdlStatusSel
  Note that there is just one copy of this register, with the information from the implemented ANIBs multiplexed per csr LcdlStatus Sel
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0E4
- Replicated per PState: No
- Exists: Always

Table 11-160 Register Name: AcLcdlStatus Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[9:0]	AcLcdlFineSnapVal	Value of the LCDL 1UI estimate code, latched by pulse on csrLcdlFineSnap while csr LcdlTstEnable=1. Index 9 is reserved for growth.	R	-
[10:10]	AcLcdlPhdSnapVal	Value of the LCDL phase-detector output, latched by pulse on LcdlFineSnap while csr LcdlTstEnable=1.	R	-
[11:11]	AcLcdlStickyLock	latched value of whether the LCDL ever achieved lock after the assertion of LcdlTstEnable.	R	-
[12:12]	AcLcdlStickyUnlock	latched value of whether the LCDL ever lost lock after the assertion of LcdlTstEnable.	R	-
[13:13]	AcLcdlLiveLock	present value of whether the LCDL is locked, valid when LcdlTstEnable=1.	R	-
[15:14]	Unimplemented	Returns zero on reads	R	0x0

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11.3.153 CUSTPHYREV

- Description: Customer settable by the customer
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0ED
- Replicated per PState: No
- Exists: Always

Table 11-161 Register Name: CUSTPHYREV Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[5:0]	CUSTPHYREV	The customer settable PHY version number. The value is derived from the `define DWC_DDRPHY_CUST_PHYREV	R	-
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.154 PHYREV

- Description: The hardware version of this PHY, excluding the PUB
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0EE
- Replicated per PState: No
- Exists: Always

Table 11-162 Register Name: PHYREV Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PHYMNR	Indicates minor update of the PHY.	R	0x0
[7:4]	PHYMDR	Indicates moderate revision of the PHY.	R	0x0
[15:8]	PHYMJR	Indicates major revision of the PHY.	R	0x01

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11.3.155 LP3ExitSeq0BStartVector

- Description: Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes. Set the start vector to be used in LP3-exit or Init PIE sequence.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0EF
- Replicated per PState: No
- Exists: Always

Table 11-163 Register Name: LP3ExitSeq0BStartVector Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	LP3ExitSeq0BStartVecPllEnabled	PIE Start Vector value to be used for LP3-exit or Init and target P-state has PLL enabled	R/W	0xe
[7:4]	LP3ExitSeq0BStartVecPllBypassed	PIE Start Vector value to be used for LP3-exit or Init and target P-state has PLL bypassed	R/W	0xd
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.156 DfiFreqXlat0

- Description: DFI Frequency Translation Register 0
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F0
- Replicated per PState: No
- Exists: Always

Table 11-164 Register Name: DfiFreqXlat0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal0	The sequencer start vector used when dfi_freq value is 0.	R/W	0x0
[7:4]	DfiFreqXlatVal1	The sequencer start vector used when dfi_freq value is 1.	R/W	0x0
[11:8]	DfiFreqXlatVal2	The sequencer start vector used when dfi_freq value is 2.	R/W	0x0
[15:12]	DfiFreqXlatVal3	The sequencer start vector used when dfi_freq value is 3.	R/W	0x0

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11.3.157 DfiFreqXlat1

- Description: DFI Frequency Translation Register 1
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F1
- Replicated per PState: No
- Exists: Always

Table 11-165 Register Name: DfiFreqXlat1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal4	The sequencer start vector used when dfi_freq value is 4.	R/W	0x0
[7:4]	DfiFreqXlatVal5	The sequencer start vector used when dfi_freq value is 5.	R/W	0x0
[11:8]	DfiFreqXlatVal6	The sequencer start vector used when dfi_freq value is 6.	R/W	0x0
[15:12]	DfiFreqXlatVal7	The sequencer start vector used when dfi_freq value is 7.	R/W	0x0

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11.3.158 DfiFreqXlat2

- Description: DFI Frequency Translation Register 2
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F2
- Replicated per PState: No
- Exists: Always

Table 11-166 Register Name: DfiFreqXlat2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal8	The sequencer start vector used when dfi_freq value is 8.	R/W	0x0
[7:4]	DfiFreqXlatVal9	The sequencer start vector used when dfi_freq value is 9.	R/W	0x0
[11:8]	DfiFreqXlatVal10	The sequencer start vector used when dfi_freq value is 10.	R/W	0x0
[15:12]	DfiFreqXlatVal11	The sequencer start vector used when dfi_freq value is 11.	R/W	0x0

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11.3.159 DfiFreqXlat3

- Description: DFI Frequency Translation Register 3
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F3
- Replicated per PState: No
- Exists: Always

Table 11-167 Register Name: DfiFreqXlat3 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal12	The sequencer start vector used when dfi_freq value is 12.	R/W	0x0
[7:4]	DfiFreqXlatVal13	The sequencer start vector used when dfi_freq value is 13.	R/W	0x0
[11:8]	DfiFreqXlatVal14	The sequencer start vector used when dfi_freq value is 14.	R/W	0x0
[15:12]	DfiFreqXlatVal15	The sequencer start vector used when dfi_freq value is 15.	R/W	0x0

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11.3.160 DfiFreqXlat4

- Description: DFI Frequency Translation Register 4
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F4
- Replicated per PState: No
- Exists: Always

Table 11-168 Register Name: DfiFreqXlat4 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal16	The sequencer start vector used when dfi_freq value is 16.	R/W	0x0
[7:4]	DfiFreqXlatVal17	The sequencer start vector used when dfi_freq value is 17.	R/W	0x0
[11:8]	DfiFreqXlatVal18	The sequencer start vector used when dfi_freq value is 18.	R/W	0x0
[15:12]	DfiFreqXlatVal19	The sequencer start vector used when dfi_freq value is 19.	R/W	0x0

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11.3.161 DfiFreqXlat5

- Description: DFI Frequency Translation Register 5
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F5
- Replicated per PState: No
- Exists: Always

Table 11-169 Register Name: DfiFreqXlat5 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal20	The sequencer start vector used when dfi_freq value is 20.	R/W	0x0
[7:4]	DfiFreqXlatVal21	The sequencer start vector used when dfi_freq value is 21.	R/W	0x0
[11:8]	DfiFreqXlatVal22	The sequencer start vector used when dfi_freq value is 22.	R/W	0x0
[15:12]	DfiFreqXlatVal23	The sequencer start vector used when dfi_freq value is 23.	R/W	0x0

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11.3.162 DfiFreqXlat6

- Description: DFI Frequency Translation Register 6
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F6
- Replicated per PState: No
- Exists: Always

Table 11-170 Register Name: DfiFreqXlat6 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal24	The sequencer start vector used when dfi_freq value is 24.	R/W	0x0
[7:4]	DfiFreqXlatVal25	The sequencer start vector used when dfi_freq value is 25.	R/W	0x0
[11:8]	DfiFreqXlatVal26	The sequencer start vector used when dfi_freq value is 26.	R/W	0x0
[15:12]	DfiFreqXlatVal27	The sequencer start vector used when dfi_freq value is 27.	R/W	0x0

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11.3.163 DfiFreqXlat7

- Description: DFI Frequency Translation Register 7
  Programmed by dwc_ddrphy_phyinit_C_initPhyConfig() to support frequency changes.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F7
- Replicated per PState: No
- Exists: Always

Table 11-171 Register Name: DfiFreqXlat7 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DfiFreqXlatVal28	The sequencer start vector used when dfi_freq value is 28.	R/W	0x0
[7:4]	DfiFreqXlatVal29	The sequencer start vector used when dfi_freq value is 29.	R/W	0x0
[11:8]	DfiFreqXlatVal30	The sequencer start vector used when dfi_freq value is 30.	R/W	0x0
[15:12]	DfiFreqXlatVal31	The sequencer start vector used when dfi_freq value is 31.	R/W	0x0

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11.3.164 TxRdPtrInit

- Description: TxRdPtrInit control register
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F8
- Replicated per PState: No
- Exists: Always

Table 11-172 Register Name: TxRdPtrInit Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	TxRdPtrInit	This register directly controls TxRdPtrInit, and is meant to be written by the PState sequencer as part of the power state switching sequence. It should be written to a 1 once the transition to LP2 is complete and 32 cycles before the de-asserting of init_complete. Likewise it should be written to 0 once the transition to an active PState is complete and 32 cycles before the assertion of init_complete. It should reset to a 1 on both warm and cold reset.	R/W	0x1
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.165 DfiInitComplete

- Description: DFI Init Complete control
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0F9
- Replicated per PState: No
- Exists: Always

Table 11-173 Register Name: DfiInitComplete Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DfiInitComplete	This register directly controls DfiInitComplete, and is meant to be written by the PState sequencer as part of the power state switching sequence. It should be written to a 1 once the transition to LP2 is complete. Likewise it should be written to 0 once the transition to an active and PState is complete. It should reset to a 0 on both warm and cold reset.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.166 RxFifoChecks

- Description: Enable more frequent consistency checks of the RX FIFOs
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0FB
- Replicated per PState: No
- Exists: Always

Table 11-174 Register Name: RxFifoChecks Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DoFrequentRxFifoChecks	When 0, read data FIFO pointer consistency checks are performed only during sideband transactions (i.e., phyupd, ctrlupd, lp_data, phymstr) or when dfi_init_start is asserted. This option relies upon intentional quiescing of the DFI interface in order for the check to be performed. When 1, read data FIFO consistency checks are performed as when this bit is 0, and also at the beginning of each break in read data traffic from the DRAM. This options provides the lowest latency in reporting of a discrepancy in the read data FIFO pointer values.	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.167 MTestDtoCtrl

- Description: If set, allows the MTestCombo observability signal to be routed out core-side through the dwc_ddrphy_dto pin
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0FF
- Replicated per PState: No
- Exists: Always

Table 11-175 Register Name: MTestDtoCtrl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	MTESTdtoEn	MTESTdtoEn==[0], dwc_ddrphy_dto will be squelched (0) MTESTdtoEn==[1], dwc_ddrphy_dto will reflect the observability signal multiplexed on MTestCombo	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.168 MapCAA0toDfi

- Description: Maps PHY CAA lane 0 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 100
- Replicated per PState: No
- Exists: Always

Table 11-176 Register Name: MapCAA0toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA0toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 0. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA0 is mapped from dfi0_address[2], then Register MapCAA0toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.169 MapCAA1toDfi

- Description: Maps PHY CAA lane 1 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 101
- Replicated per PState: No
- Exists: Always

Table 11-177 Register Name: MapCAA1toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA1toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 1. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA1 is mapped from dfi0_address[2], then Register MapCAA1toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x1
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.170 MapCAA2toDfi

- Description: Maps PHY CAA lane 2 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 102
- Replicated per PState: No
- Exists: Always

Table 11-178 Register Name: MapCAA2toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA2toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 2. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA2 is mapped from dfi0_address[2], then Register MapCAA2toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x2
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.171 MapCAA3toDfi

- Description: Maps PHY CAA lane 3 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 103
- Replicated per PState: No
- Exists: Always

Table 11-179 Register Name: MapCAA3toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA3toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 3. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA3 is mapped from dfi0_address[2], then Register MapCAA3toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x3
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.172 MapCAA4toDfi

- Description: Maps PHY CAA lane 4 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 104
- Replicated per PState: No
- Exists: Always

Table 11-180 Register Name: MapCAA4toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA4toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 4. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA4 is mapped from dfi0_address[2], then Register MapCAA4toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x4
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.173 MapCAA5toDfi

- Description: Maps PHY CAA lane 5 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 105
- Replicated per PState: No
- Exists: Always

Table 11-181 Register Name: MapCAA5toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA5toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 5. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA5 is mapped from dfi0_address[2], then Register MapCAA5toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x5
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.174 MapCAA6toDfi

- Description: Maps PHY CAA lane 6 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 106
- Replicated per PState: No
- Exists: Always

Table 11-182 Register Name: MapCAA6toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA6toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 6. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA6 is mapped from dfi0_address[2], then Register MapCAA6toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x6
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.175 MapCAA7toDfi

- Description: Maps PHY CAA lane 7 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 107
- Replicated per PState: No
- Exists: Always

Table 11-183 Register Name: MapCAA7toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA7toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 7. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA7 is mapped from dfi0_address[2], then Register MapCAA7toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x7
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.176 MapCAA8toDfi

- Description: Maps PHY CAA lane 8 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 108
- Replicated per PState: No
- Exists: Always

Table 11-184 Register Name: MapCAA8toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA8toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 8. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA8 is mapped from dfi0_address[2], then Register MapCAA8toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x8
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.177 MapCAA9toDfi

- Description: Maps PHY CAA lane 9 from dfi0_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 109
- Replicated per PState: No
- Exists: Always

Table 11-185 Register Name: MapCAA9toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAA9toDfi	For LPDDR4 applications, these CSRs map a dfi0_address to CAA 9. Unused for DDR4 applications. Each register in the set of MapCAAtoDfi must have a unique value within the set. For example, if PHY CAA9 is mapped from dfi0_address[2], then Register MapCAA9toDfi should be 2. LPDDR4 ACX3,ACX6,ACX10,ACX12 registers MapCAA{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAA{6..9}toDfi are reserved	R/W	0x9
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.178 MapCAB0toDfi

- Description: Maps PHY CAB lane 0 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 110
- Replicated per PState: No
- Exists: Always

Table 11-186 Register Name: MapCAB0toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB0toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 0. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB0 is mapped from dfi1_address[2], then Register MapCAB0toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.179 MapCAB1toDfi

- Description: Maps PHY CAB lane 1 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 111
- Replicated per PState: No
- Exists: Always

Table 11-187 Register Name: MapCAB1toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB1toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 1. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB1 is mapped from dfi1_address[2], then Register MapCAB1toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x1
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.180 MapCAB2toDfi

- Description: Maps PHY CAB lane 2 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 112
- Replicated per PState: No
- Exists: Always

Table 11-188 Register Name: MapCAB2toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB2toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 2. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB2 is mapped from dfi1_address[2], then Register MapCAB2toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x2
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.181 MapCAB3toDfi

- Description: Maps PHY CAB lane 3 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 113
- Replicated per PState: No
- Exists: Always

Table 11-189 Register Name: MapCAB3toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB3toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 3. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB3 is mapped from dfi1_address[2], then Register MapCAB3toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x3
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.182 MapCAB4toDfi

- Description: Maps PHY CAB lane 4 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 114
- Replicated per PState: No
- Exists: Always

Table 11-190 Register Name: MapCAB4toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB4toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 4. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB4 is mapped from dfi1_address[2], then Register MapCAB4toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x4
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.183 MapCAB5toDfi

- Description: Maps PHY CAB lane 5 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 115
- Replicated per PState: No
- Exists: Always

Table 11-191 Register Name: MapCAB5toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB5toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 5. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB5 is mapped from dfi1_address[2], then Register MapCAB5toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x5
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.184 MapCAB6toDfi

- Description: Maps PHY CAB lane 6 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 116
- Replicated per PState: No
- Exists: Always

Table 11-192 Register Name: MapCAB6toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB6toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 6. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB6 is mapped from dfi1_address[2], then Register MapCAB6toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x6
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.185 MapCAB7toDfi

- Description: Maps PHY CAB lane 7 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 117
- Replicated per PState: No
- Exists: Always

Table 11-193 Register Name: MapCAB7toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB7toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 7. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB7 is mapped from dfi1_address[2], then Register MapCAB7toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x7
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.186 MapCAB8toDfi

- Description: Maps PHY CAB lane 8 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 118
- Replicated per PState: No
- Exists: Always

Table 11-194 Register Name: MapCAB8toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB8toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 8. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB8 is mapped from dfi1_address[2], then Register MapCAB8toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x8
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.187 MapCAB9toDfi

- Description: Maps PHY CAB lane 9 from dfi1_address of the index of the register contents
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 119
- Replicated per PState: No
- Exists: Always

Table 11-195 Register Name: MapCAB9toDfi Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	MapCAB9toDfi	For LPDDR4 applications, these CSRs map a dfi1_address to CAB 9. Unused for DDR4 applications. Unused for the 3-ANIB configuration. Each register in the set of MapCABtoDfi must have a unique value within the set. For example, if PHY CAB9 is mapped from dfi1_address[2], then Register MapCAB9toDfi should be 2. LPDDR4 ACX3 registers MapCAB{0..9}toDfi are reserved, second channel not supportd LPDDR4 ACX6,ACX10,ACX12 registers MapCAB{0..5}toDfi are used, values 0-5 are valid, values 6-15 are reserved registers MapCAB{6..9}toDfi are reserved	R/W	0x9
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.188 PhyInterruptEnable

- Description: Enables various interrupts to appear in the PhyInterruptStatus CSR. Only interrupts which are enabled by writing a 1 to the appropriate location in this CSR will be observable in the PhyInterruptStatus CSR. If a 0 is written in a particular location the corresponding interrupt will not be visible in the PhyInterruptStatus CSR. See the description of PhyInterruptStatus for more information on specific interrupts.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 11B
- Replicated per PState: No
- Exists: Always

Table 11-196 Register Name: PhyInterruptEnable Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PhyTrngCmpltEn	Enable for the PHY Training Complete interrupt. 0 : Interrupt not enabled 1 : Interrupt enabled	R/W	0x0
[1:1]	PhyInitCmpltEn	Enable for the PHY Initialization Complete interrupt. 0 : Interrupt not enabled 1 : Interrupt enabled	R/W	0x0
[2:2]	PhyTrngFailEn	Enable for the PHY Training Failure interrupt. 0 : Interrupt not enabled 1 : Interrupt enabled	R/W	0x0
[7:3]	PhyFWReservedEn	Reserved	R/W	0x00
[9:8]	PhyVTDriftAlarmEn	Enable for the PHY VT Drift Alarm interrupts. 0 : Interrupt not enabled 1 : Interrupt enabled	R/W	0x0
[10:10]	PhyRxFifoCheckEn	Enable for the RxFifo Pointers Check Interrupt 0 : Interrupt not enabled 1 : Interrupt enabled	R/W	0x0

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Table 11-196 Register Name: PhyInterruptEnable Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:11]	PhyHWReservedEn	Reserved	R/W	0x00

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11.3.189 PhyInterruptFWControl

- Description: A 0 to 1 transition for any of the interrupts will set the corresponding bit location in the PhyInterruptStatus CSR if the corresponding bit location in the PhyInterruptEnable CSR is set to 1. See the description of PhyInterruptStatus for more information on specific interrupts.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 11C
- Replicated per PState: No
- Exists: Always

Table 11-197 Register Name: PhyInterruptFWControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PhyTrngCmpltFW	PHY Training Complete Firmware interrupt. Written only by PHY Firmware. 0 : Interrupt not asserted 1 : Interrupt asserted	R/W	0x0
[1:1]	PhyInitCmpltFW	PHY Initialization Complete Firmware interrupt. The PhyInitCmpIt interrupt is not written by PHY firmware. It can be written by the user once dfi_init_complete is asserted. 0 : Interrupt not asserted 1 : Interrupt asserted	R/W	0x0
[2:2]	PhyTrngFailFW	PHY Training Failure Firmware interrupt. Written only by PHY Firmware. 0 : Interrupt not asserted 1 : Interrupt asserted	R/W	0x0
[7:3]	PhyFWReservedFW	Implemented, reserved for future use. 0 : Interrupt not asserted 1 : Interrupt asserted Reserved	R/W	0x00
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.190 PhyInterruptMask

- Description: This register is used to mask various interrupts to prevent them from affecting the output pin dwc_ddrphy_int_n. Only interrupts which are not masked by clearing to 0 the corresponding location in this CSR will be able to affect the dwc_ddrphy_int_n output when asserted in the PhyInterruptStatus CSR. If a 1 is written in a particular location that interrupt will still be visible in the PhyInterruptStatus CSR but that interrupt will not affect the output pin dwc_ddrphy_int_n.
  See the description of PhyInterruptStatus for more information on specific interrupts.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 11D
- Replicated per PState: No
- Exists: Always

Table 11-198 Register Name: PhyInterruptMask Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PhyTrngCmpltMsk	Mask for the PHY Training Complete interrupt. 0 : Interrupt not masked 1 : Interrupt masked	R/W	0x0
[1:1]	PhyInitCmpltMsk	Mask for the PHY Initialization Complete interrupt. 0 : Interrupt not masked 1 : Interrupt masked	R/W	0x0
[2:2]	PhyTrngFailMsk	Mask for the PHY Training Failure interrupt. 0 : Interrupt not masked 1 : Interrupt masked	R/W	0x0
[7:3]	PhyFWReservedMsk	Reserved	R/W	0x00
[9:8]	PhyVTDriftAlarmMsk	Mask for the PHY VT Drift Alarm interrupts. 0 : Interrupt not masked 1 : Interrupt masked	R/W	0x0
[10:10]	PhyRxFifoCheckMsk	Mask for the RxFifo Pointers Check Interrupt 0 : Interrupt not masked 1 : Interrupt masked	R/W	0x0

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Table 11-198 Register Name: PhyInterruptMask Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:11]	PhyHWReservedMsk	Reserved	R/W	0x00

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11.3.191 PhyInterruptClear

- Description: This register clears various interrupts and will negate the output pin dwc_ddrphy_int_n if the cleared interrupt was the cause of the assertion of the output pin dwc_ddrphy_int_n. A 0 to 1 transition on a bit will clear the corresponding interrupt, and cause the hardware to immediately clear the bit.
  See the description of PhyInterruptStatus for more information on specific interrupts.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 11E
- Replicated per PState: No
- Exists: Always

Table 11-199 Register Name: PhyInterruptClear Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PhyTrngCmpltClr	Clear for the PHY Training Complete interrupt. 0 : Interrupt not affected 1 : Interrupt cleared	R/W	0x0
[1:1]	PhyInitCmpltClr	Clear for the PHY Initialization Complete interrupt. 0 : Interrupt not affected 1 : Interrupt cleared	R/W	0x0
[2:2]	PhyTrngFailClr	Clear for the PHY Training Failure interrupt. 0 : Interrupt not affected 1 : Interrupt cleared	R/W	0x0
[7:3]	PhyFWReservedClr	Reserved	R/W	0x00
[9:8]	PhyVTDriftAlarmClr	Clear for the PHY VT Drift Alarm interrupt. 0 : Interrupt not affected 1 : Interrupt cleared	R/W	0x0
[10:10]	PhyRxFifoCheckClr	Clear for the RxFifo Pointers Check Interrupt 0 : Interrupt not affected 1 : Interrupt cleared	R/W	0x0

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Table 11-199 Register Name: PhyInterruptClear Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:11]	PhyHWReservedClr	Reserved	R/W	0x00

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11.3.192 PhyInterruptStatus

- Description: This register displays the current status of various PHY interrupts. This is a read only CSR. The PHY is the only entity which can write to it. In order for a bit to become set in the PhyInterruptStatus CSR the corresponding bit must be set in the PhyInterruptEnable CSR. If an interrupt is set in the PhyInterruptStatus CSR and the corresponding bit in the PhyInterruptMask CSR is cleared the dwc_ddrphy_int_n output signal will be asserted. Once the dwc_ddrphy_int_n output signal is asserted it can only be negated when all unmasked interrupts in the PhyInterruptStatus CSR have been cleared by writing the corresponding bit in the PhyInterruptClear CSR to 1.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 11F
- Replicated per PState: No
- Exists: Always

Table 11-200 Register Name: PhyInterruptStatus Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	PhyTrngCmplt	PHY Training Complete interrupt. Assertion of this interrupt indicates that the PHY has successfully trained the memory interface at all indicated frequencies and is ready for the PHY Initialization Engine to be loaded. 0 : Interrupt not enabled and asserted 1 : Interrupt enabled and asserted	R	-
[1:1]	PhyInitCmplt	PHY Initialization Complete interrupt. Written by the user. Assertion of this interrupt is meant to indicate that the PHY Initialization Engine has been fully loaded and dfi_init_complete has been asserted. 0 : Interrupt not enabled and asserted 1 : Interrupt enabled and asserted	R	-
[2:2]	PhyTrngFail	PHY Training Failure interrupt. Assertion of this interrupt indicates there was an issue during training which did not allow the PHY to successfully complete training. 0 : Interrupt not enabled and asserted 1 : Interrupt enabled and asserted	R	-
[7:3]	PhyFWReserved	Reserved	R	-

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Table 11-200 Register Name: PhyInterruptStatus Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[9:8]	VTDriftAlarm	PHY VT Drift Alarm interrupt. Assertion of this interrupt indicates the number of tap points in the master DLL has shifted by an amount greater than 2 * DfiPhyUpdIntThreshold. There is one bit for each master DLL and they are fully independent of one another. Please see the DfiPhyUpdIntThreshold CSR for additional information. 0 : Interrupt not enabled and asserted 1 : Interrupt enabled and asserted	R	-
[10:10]	PhyRxFifoCheck	A mechanism in the PHY checks the Read Fifo pointers for consistency at times they are idle. If a check fails, this interrupt is asserted, and detailed status is found in the RxFifoCheckStatus register. 0 : Interrupt not enabled and asserted 1 : Interrupt enabled and asserted	R	-
[15:11]	PhyHWReserved	Reserved	R	-

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11.3.193 HwtSwizzleHwtAddress0

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 120
- Replicated per PState: No
- Exists: Always

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Table 11-201 Register Name: HwtSwizzleHwtAddress0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress0	This set of registers is used in DDR4 mode where a user has re-mapped the DFI inputs to the PHY. This register does not affect the mapping of those signals, or remap the tristate properties of the bumps. However, when the user remaps the DFI signals, the HWT inputs must be mapped in a similar fashion using this register. Each remappable hwt bit has a register associated with it. When the register value is zero, the bit is not re-mapped. When the register value is non-zero, the signal associated with the number in the table below is mapped to the signal associated with the register. So, for example, if the value for the register associated with hwt_act_n (HwtSwizzleHwtActN) is set to 27, then hwt_parity_in will be mapped to hwt_act_n. These registers should always be 0 for LPDDR4. Some registers are used only for DDR4. These are noted in the descriptions. ----- Index: Signal 0: No-remapping 1: hwt_address[0] 2: hwt_address[1] 3: hwt_address[2] 4: hwt_address[3] 5: hwt_address[4] 6: hwt_address[5] 7: hwt_address[6] 8: hwt_address[7] 9: hwt_address[8] 10: hwt_address[9] 11: hwt_address[10] 12: hwt_address[11] 13: hwt_address[12] 14: hwt_address[13] 15: hwt_address[14] (DDR3 Only) 16: hwt_address[15] (DDR3 Only) 17: hwt_address[17] (DDR4 Only) 18: hwt_act_n (DDR4 Only) 19: hwt_bank[0]	R/W	0x00

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Table 11-201 Register Name: HwtSwizzleHwtAddress0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.194 HwtSwizzleHwtAddress1

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 121
- Replicated per PState: No
- Exists: Always

Table 11-202 Register Name: HwtSwizzleHwtAddress1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress1	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.195 HwtSwizzleHwtAddress2

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 122
- Replicated per PState: No
- Exists: Always

Table 11-203 Register Name: HwtSwizzleHwtAddress2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress2	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.196 HwtSwizzleHwtAddress3

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 123
- Replicated per PState: No
- Exists: Always

Table 11-204 Register Name: HwtSwizzleHwtAddress3 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress3	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.197 HwtSwizzleHwtAddress4

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 124
- Replicated per PState: No
- Exists: Always

Table 11-205 Register Name: HwtSwizzleHwtAddress4 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress4	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.198 HwtSwizzleHwtAddress5

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 125
- Replicated per PState: No
- Exists: Always

Table 11-206 Register Name: HwtSwizzleHwtAddress5 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress5	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.199 HwtSwizzleHwtAddress6

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 126
- Replicated per PState: No
- Exists: Always

Table 11-207 Register Name: HwtSwizzleHwtAddress6 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress6	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.200 HwtSwizzleHwtAddress7

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 127
- Replicated per PState: No
- Exists: Always

Table 11-208 Register Name: HwtSwizzleHwtAddress7 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress7	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.201 HwtSwizzleHwtAddress8

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 128
- Replicated per PState: No
- Exists: Always

Table 11-209 Register Name: HwtSwizzleHwtAddress8 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress8	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.202 HwtSwizzleHwtAddress9

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 129
- Replicated per PState: No
- Exists: Always

Table 11-210 Register Name: HwtSwizzleHwtAddress9 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress9	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.203 HwtSwizzleHwtAddress10

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 12A
- Replicated per PState: No
- Exists: Always

Table 11-211 Register Name: HwtSwizzleHwtAddress10 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress10	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.204 HwtSwizzleHwtAddress11

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 12B
- Replicated per PState: No
- Exists: Always

Table 11-212 Register Name: HwtSwizzleHwtAddress11 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress11	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.205 HwtSwizzleHwtAddress12

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 12C
- Replicated per PState: No
- Exists: Always

Table 11-213 Register Name: HwtSwizzleHwtAddress12 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress12	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.206 HwtSwizzleHwtAddress13

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 12D
- Replicated per PState: No
- Exists: Always

Table 11-214 Register Name: HwtSwizzleHwtAddress13 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress13	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.207 HwtSwizzleHwtAddress14

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 12E
- Replicated per PState: No
- Exists: Always

Table 11-215 Register Name: HwtSwizzleHwtAddress14 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress14	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR3.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.208 HwtSwizzleHwtAddress15

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 12F
- Replicated per PState: No
- Exists: Always

Table 11-216 Register Name: HwtSwizzleHwtAddress15 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress15	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR3.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.209 HwtSwizzleHwtAddress17

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 130
- Replicated per PState: No
- Exists: Always

Table 11-217 Register Name: HwtSwizzleHwtAddress17 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtAddress17	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR4.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.210 HwtSwizzleHwtActN

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 131
- Replicated per PState: No
- Exists: Always

Table 11-218 Register Name: HwtSwizzleHwtActN Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtActN	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR4.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.211 HwtSwizzleHwtBank0

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 132
- Replicated per PState: No
- Exists: Always

Table 11-219 Register Name: HwtSwizzleHwtBank0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtBank0	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.212 HwtSwizzleHwtBank1

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 133
- Replicated per PState: No
- Exists: Always

Table 11-220 Register Name: HwtSwizzleHwtBank1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtBank1	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.213 HwtSwizzleHwtBank2

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 134
- Replicated per PState: No
- Exists: Always

Table 11-221 Register Name: HwtSwizzleHwtBank2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtBank2	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR3.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.214 HwtSwizzleHwtBg0

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 135
- Replicated per PState: No
- Exists: Always

Table 11-222 Register Name: HwtSwizzleHwtBg0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtBg0	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR4.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.215 HwtSwizzleHwtBg1

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 136
- Replicated per PState: No
- Exists: Always

Table 11-223 Register Name: HwtSwizzleHwtBg1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtBg1	See Description of HwtSwizzleHwtAddress0 for details. Used only for DDR4.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.216 HwtSwizzleHwtCasN

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 137
- Replicated per PState: No
- Exists: Always

Table 11-224 Register Name: HwtSwizzleHwtCasN Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtCasN	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.217 HwtSwizzleHwtRasN

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 138
- Replicated per PState: No
- Exists: Always

Table 11-225 Register Name: HwtSwizzleHwtRasN Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtRasN	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.218 HwtSwizzleHwtWeN

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 139
- Replicated per PState: No
- Exists: Always

Table 11-226 Register Name: HwtSwizzleHwtWeN Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtWeN	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.219 HwtSwizzleHwtParityIn

- Description: Signal swizzle selection for HWT swizzle
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 13A
- Replicated per PState: No
- Exists: Always

Table 11-227 Register Name: HwtSwizzleHwtParityIn Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtSwizzleHwtParity In	See Description of HwtSwizzleHwtAddress0 for details.	R/W	0x00
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.220 DfiHandshakeDelays0

- Description: Add assertion/deassertion delays on handshake signals
  Logic assumes that dfi signal assertions exceed the programmed delays
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 13C
- Replicated per PState: No
- Exists: Always

Table 11-228 Register Name: DfiHandshakeDelays0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PhyUpdAckDelay0	Adds 0-15 DfiClks of delay after dfi0_phyupd_ack asserts, before the PHY takes any action (such as starting DDL calibration).	R/W	0x0
[7:4]	PhyUpdReqDelay0	Adds 0-15 DfiClks of delay after the PHY completes all PHY update activities, before de-asserting dfi0_phyupd_req.	R/W	0x0
[11:8]	CtrlUpdAckDelay0	Adds 0-15 DfiClks of delay after dfi0_ctrlupd_req asserts, before the PHY takes any action.	R/W	0x0
[15:12]	CtrlUpdReqDelay0	Adds 0-15 DfiClks of delay after the PHY completes all PHY update activities, before de-asserting dfi0_ctrlupd_ack.	R/W	0x0

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11.3.221 DfiHandshakeDelays1

- Description: Add assertion/deassertion delays on handshake signals
  Logic assumes that dfi signal assertions exceed the programmed delays
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 13D
- Replicated per PState: No
- Exists: Always

Table 11-229 Register Name: DfiHandshakeDelays1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PhyUpdAckDelay1	Adds 0-15 DfiClks of delay after dfi1_phyupd_ack asserts, before the PHY takes any action (such as starting DDL calibration).	R/W	0x0
[7:4]	PhyUpdReqDelay1	Adds 0-15 DfiClks of delay after the PHY completes all PHY update activities, before de-asserting dfi1_phyupd_req.	R/W	0x0
[11:8]	CtrlUpdAckDelay1	Adds 0-15 DfiClks of delay after dfi1_ctrlupd_req asserts, before the PHY takes any action.	R/W	0x0
[15:12]	CtrlUpdReqDelay1	Adds 0-15 DfiClks of delay after the PHY completes all PHY update activities, before de-asserting dfi1_ctrlupd_ack.	R/W	0x0

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11.3.222 CalUclkInfo

- Description: Informs the impedance calibration engine about frequency of DfiClk
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 008
- Replicated per PState: Yes
- Exists: Always

Table 11-230 Register Name: CalUclkInfo Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[10:0]	CalUClkTicksPer1uS	Must be programmed to the number of DfiClks in 1us (rounded up), with minimum value of 24. if (DfiClk < 24MHz) CalUclkInfo = 24 else CalUclkInfo = (number of DfiClks in 1us)	R/W	0x320
[15:11]	Unimplemented	Returns zero on reads	R	0x0

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11.3.223 Seq0BDLY0

- Description: PHY Initialization Engine (PIE) Delay Register 0
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 00B
- Replicated per PState: Yes
- Exists: Always

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Table 11-231 Register Name: Seq0BDLY0 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	Seq0BDLY0	PHY Initialization Engine (PIE) Delay Register 0 This register is available for selection by the NOP and WAIT instructions in the PIE for the delay value. Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes. Programming Seq0BDLY[3,2,1,0] Registers: ---------- These registers are used to control various delays during PLL, DLL initialization. These registers should be programmed with the corresponding number of MEMCLK cycles representing a fixed amount of delay irrespective of DfiClk Frequency. When calculating the number of cycles to be programmed for each PState, it should be noted that the sequencer multiplies programmed values by a factor of 8 and values are round down to the closest integer. Register Required Delay Programmed Value --------- ---------- ---------- Seq0BDLY0 0.5us (0.5us / MEMCLK period) / 8) Seq0BDLY1 1.0us (1.0us / MEMCLK period) / 8) Seq0BDLY2 10.0us (10.0us / MEMCLK period) / 8) 64/4 if (MEMCLK Freq <= 400MHz) Seq0BDLY3 - 132/4 if (400MHz Freq < MEMCLK Freq <= 533MHz) 176/4 if (MEMCLK Freq > 533MHz)	R/W	0x0000

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11.3.224 Seq0BDLY1

- Description: PHY Initialization Engine (PIE) Delay Register 1
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 00C
- Replicated per PState: Yes
- Exists: Always

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Table 11-232 Register Name: Seq0BDLY1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	Seq0BDLY1	PHY Initialization Engine (PIE) Delay Register 1 This register is available for selection by the NOP and WAIT instructions in the PIE for the delay value. Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes. Programming Seq0BDLY[3,2,1,0] Registers: ---------- These registers are used to control various delays during PLL, DLL initialization. These registers should be programmed with the corresponding number of MEMCLK cycles representing a fixed amount of delay irrespective of DfiClk Frequency. When calculating the number of cycles to be programmed for each PState, it should be noted that the sequencer multiplies programmed values by a factor of 8 and values are round down to the closest integer. Register Required Delay Programmed Value --- --- --- Seq0BDLY0 0.5us (0.5us / MEMCLK period) / 8) Seq0BDLY1 1.0us (1.0us / MEMCLK period) / 8) Seq0BDLY2 10.0us (10.0us / MEMCLK period) / 8) 64/4 if (MEMCLK Freq <= 400MHz) Seq0BDLY3 - 132/4 if (400MHz Freq < MEMCLK Freq <= 533MHz) 176/4 if (MEMCLK Freq > 533MHz)	R/W	0x0000

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11.3.225 Seq0BDLY2

- Description: PHY Initialization Engine (PIE) Delay Register 2
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 00D
- Replicated per PState: Yes
- Exists: Always

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Table 11-233 Register Name: Seq0BDLY2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	Seq0BDLY2	PHY Initialization Engine (PIE) Delay Register 2 This register is available for selection by the NOP and WAIT instructions in the PIE for the delay value. Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes. Programming Seq0BDLY[3,2,1,0] Registers: ---------- These registers are used to control various delays during PLL, DLL initialization. These registers should be programmed with the corresponding number of MEMCLK cycles representing a fixed amount of delay irrespective of DfiClk Frequency. When calculating the number of cycles to be programmed for each PState, it should be noted that the sequencer multiplies programmed values by a factor of 8 and values are round down to the closest integer. Register Required Delay Programmed Value --- --- --- Seq0BDLY0 0.5us (0.5us / MEMCLK period) / 8) Seq0BDLY1 1.0us (1.0us / MEMCLK period) / 8) Seq0BDLY2 10.0us (10.0us / MEMCLK period) / 8) 64/4 if (MEMCLK Freq <= 400MHz) Seq0BDLY3 - 132/4 if (400MHz Freq < MEMCLK Freq <= 533MHz) 176/4 if (MEMCLK Freq > 533MHz)	R/W	0x0000

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11.3.226 Seq0BDLY3

- Description: PHY Initialization Engine (PIE) Delay Register 3
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 00E
- Replicated per PState: Yes
- Exists: Always

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Table 11-234 Register Name: Seq0BDLY3 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	Seq0BDLY3	PHY Initialization Engine (PIE) Delay Register 3 This register is available for selection by the NOP and WAIT instructions in the PIE for the delay value. Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support frequency changes. Programming Seq0BDLY[3,2,1,0] Registers: ---------- These registers are used to control various delays during PLL, DLL initialization. These registers should be programmed with the corresponding number of MEMCLK cycles representing a fixed amount of delay irrespective of DfiClk Frequency. When calculating the number of cycles to be programmed for each PState, it should be noted that the sequencer multiplies programmed values by a factor of 8 and values are round down to the closest integer. Register Required Delay Programmed Value --- --- --- Seq0BDLY0 0.5us (0.5us / MEMCLK period) / 8) Seq0BDLY1 1.0us (1.0us / MEMCLK period) / 8) Seq0BDLY2 10.0us (10.0us / MEMCLK period) / 8) 64/4 if (MEMCLK Freq <= 400MHz) Seq0BDLY3 - 132/4 if (400MHz Freq < MEMCLK Freq <= 533MHz) 176/4 if (MEMCLK Freq > 533MHz)	R/W	0x0000

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11.3.227 PPTTrainSetup

- Description: For LPDDR4/4X some tracking is required periodically using the DFI PHY MASTER interface.
  This register control the interval.
  Setting the register to 0 completely disables the PHY Master Interface
  Programmed by dwc_ddrphy_phyinit_I_loadPIEImage() to support LPDDR4/4X DRAM drift compensation.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 010
- Replicated per PState: Yes
- Exists: Always

Table 11-235 Register Name: PPTTrainSetup Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	PhyMstrTrainInterval	Bits 3:0 of this register specifies the time between the end of one training and the start of the next. (As per section 11 of the Preliminary DFI 4.0 Specification, V2, it is the max expected time from dfi_init_complete asserted to tdfi_phymstr_ack asserted). 4'b0000 Disable PHY Master Interface 4'b0001 PHY MASTER Request Interval = 524288 MEMCLKs 4'b0010 PHY MASTER Request Interval = 1048576 MEMCLKs 4'b0011 PHY MASTER Request Interval = 2097152 MEMCLKs 4'b0100 PHY MASTER Request Interval = 4194304 MEMCLKs 4'b0101 PHY MASTER Request Interval = 8388608 MEMCLKs 4'b0110 PHY MASTER Request Interval = 16777216 MEMCLKs 4'b0111 PHY MASTER Request Interval = 33554432 MEMCLKs 4'b1000 PHY MASTER Request Interval = 67108864 MEMCLKs 4'b1001 PHY MASTER Request Interval = 134217728 MEMCLKs 4'b1010 PHY MASTER Request Interval = 268435456 MEMCLKs 4'b1011 - 4'b1111 PHY MASTER Request Interval = undefined	R/W	0x0

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Table 11-235 Register Name: PPTTrainSetup Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[6:4]	PhyMstrMaxReqToAck	Bits 6:4 of this register specify the max time from tdfi_phymstr_req asserted to tdfi_phymstr_ack asserted. If the request is not acknowledged by this time, dfi_error will be asserted. 3'b000 Disable PHY Master Interface 3'b001 set tPHYMSTR_resp. = 512 MEMCLKs 3'b010 set tPHYMSTR_resp. = 1024 MEMCLKs 3'b011 set tPHYMSTR_resp. = 2048 MEMCLKs 3'b100 set tPHYMSTR_resp. = 4096 MEMCLKs 3'b101 set tPHYMSTR_resp. = 8192 MEMCLKs 3'b110 set tPHYMSTR_resp. = 32768 MEMCLKs 3'b111 set tPHYMSTR_resp. = undefined Note 1: The above are nominal values. The actual values are reduced by (2 + (DWC_DDRPHY_PIPE_DFI_MISC * MEMCLK/DfiCtlClk)) * 2 Note 2: This signal interacts with dfi_phyupd_req. See Section 10.5.5 of the PUB Databook	R/W	0x0
[15:7]	Unimplemented	Returns zero on reads	R	0x0

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11.3.228 TristateModeCA

- Description: This register is used to control the PHY Dynamic Address/Command Tristate Feature, and the stopped MEMCLK state.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 019
- Replicated per PState: Yes
- Exists: Always

Table 11-236 Register Name: TristateModeCA Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	DisDynAdrTri	When DisDynAdrTri=1, Dynamic Tristating is disabled. Dynamic Tristating is on by default. . Dynamic Tristating should be disabled (DisDynAdrTri=1) for these modes: 1. DDR4/2T/2N if the controller cannot follow the 2T PHY tristate protocol. 2. LPDDR4 . When DisDynAdrTri=0 (default), In DDR4 mode, The following SDRAM pins can be dynamically tristated: A,BA,BG,ACT_n . In 1T mode, the PHY will tristate the relevant pins when all ranks are DESelected . In 2T mode (or geardown), the PHY will tristate the relevant pins when: DDR4 -- All ranks DESelected (all CS_L==1) AND {RAS_n,CAS_n,WE_n,BA0,ACT_n} = {1,1,1,0,1} When in this mode, the controller should avoid sending the above patterns with any rank selected. [e.g. NOPs sent by the controller should have BA0 set to a non-zero value]	R/W	0x0
[1:1]	DDR2TMode	Must be set to 1 for Dynamic Tristate to work when CA bus is 2T or Geardown mode. This CSR bit has no effect when DisDynAdrTri==1	R/W	0x0

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Table 11-236 Register Name: TristateModeCA Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:2]	CkDisVal	The PHY provides 4 memory clocks, n=0..3. When the toggling of memory clock CK_t[n] is disabled with dfi_clk_disable[n]=1, the memory clock CK_t[n] is driven with Register CkDisVal[1]. When the toggling of memory clock CK_c[n] is disabled with dfi_clk_disable[n]=1, the memory clock CK_c[n] is driven with ~(Register CkDisVal[0]) (ie inverted). Note that the non-toggling differential memory clock {CK_t[n],CK_c[n]} may be driven with any combination, LL,LH,HL,HH; the default {CK_t[n],CK_c[n]}=LH.	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.229 HwtMRL

- Description: HWT MaxReadLatency.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 020
- Replicated per PState: Yes
- Exists: Always

Table 11-237 Register Name: HwtMRL Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	HwtMRL	This Max Read Latency CSR is to be trained to ensure the rx-data fifo is not read until after all dbytes have their read data valid. The CSR is in units of two mem clocks; that is, a unit change in the LSB is a change in MRL of two mem clocks. This MASTER copy of MRL is used by the PHY training hardware only.	R/W	0x06
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.230 DqsPreambleControl

- Description: For improved robustness in operating with DRAM timing drift, this register provides controls for the width of the write DQS preamble and postamble, and controls for the anticipated width of DQS preamble for reads.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 024
- Replicated per PState: Yes
- Exists: Always

Table 11-238 Register Name: DqsPreambleControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	TwoTckRxDqsPre	Widens the RxDqsEn window to allow larger drift in the incoming read DQS to take advantage of the larger/wider preamble generated by the DRAMSs when the D4 DRAMS are configured with DDR4 MR4 A11 Read Preamble=1 for causing a 2nCK read preamble. For LPDDR4, all read operations are 2nCK such that this control must be set to 1. Note the nominal trained-to-center point will be earlier relative to the first strobing edge of DQS than when not in this mode.	R/W	0x0
[1:1]	TwoTckTxDqsPre	0: Standard 1tck TxDqs Preamble 1: Enable Optional D4 2tck TxDqs Preamble The DDR4 MR4 A12 is Write Preamble, 1=2nCK, 0=1nCK.	R/W	0x0
[4:2]	PositionDfeInit	For DDR4 phy only when receive DFE is enabled. PositionDfeInit[2]=1 causes DfeInit to be asserted late PositionDfeInit[1]=1 causes DfeInit to be asserted at the nominal time PositionDfeInit[0]=1 causes DfeInit to be asserted early PositionDfeInit=3'b010 is the nominal, recommended value for leading edge used by receiver.	R/W	0x2
[5:5]	LP4TglTwoTckTxDqs Pre	Used in LPDDR4 mode to modify the early preamble when Register TwoTckTxDqsPre=1 0: level first-memclk preamble 1: toggling first-memclk preamble	R/W	0x0

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Table 11-238 Register Name: DqsPreambleControl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[6:6]	LP4PostambleExt	In LPDDR4 mode must be set to extend the write postamble. 0: half-memclk postamble, as in D4 1: one-and-one-half-memclk postamble; see LPDDR4 Spec MR3, OP[1] WR PST, vendor-specific function.	R/W	0x0
[7:7]	LP4SttcPreBridgeRxEn	Used in LPDDR4 static-preamble mode to bridge the RxEn between two reads to the same timing group when the bubble is 1 memclk. LPDDR4 static-preamble mode is set in the DRAMs with MR1, OP[3]=0.	R/W	0x0
[8:8]	WDQSEXTENSION	When set, DQS_T and DQS_C will be driven differentially to 0 and 1, respectively, before and after a write burst, except during a memory read transaction. See DesignWare Cores LPDDR4 MultiPHY: WDQS Extension Application Note. Use of WDQSEXTENSION requires POdtTailWidth=3 and POdtStartDelay=00	R/W	0x0
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.231 DMIPinPresent

- Description: This Register is used to instruct the PHY whether to enable the Read-DBI function on Lane8 of each DBYTE. Only the LPDDR4 and DDR4 Protocols support the Read-DBI feature.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 02D
- Replicated per PState: Yes
- Exists: Always

Table 11-239 Register Name: DMIPinPresent Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[0:0]	RdDbiEnabled	This bit must be set to 1'b1 if Read-DBI is enabled in a connected DDR4 or LPDDR4 device. If set, the following DRAM MR should also be set [DDR4.MR5.A12=1 or LPDDR4.MR3.OP[7]=1]	R/W	0x0
[15:1]	Unimplemented	Returns zero on reads	R	0x0

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11.3.232 ARdPtrInitVal

- Description: Address/Command FIFO ReadPointer Initial Value
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 02E
- Replicated per PState: Yes
- Exists: Always

Table 11-240 Register Name: ARdPtrInitVal Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	ARdPtrInitVal	This is the initial Pointer Offset for the free-running FIFOs in the DBYTE and ACX4 hardips. The units of this register are in UI. The pointer separation should be chosen to compensate for all sources of skew and drift of the PHY DFICLK and PCLK networks. Please see PUB databook section 8.1.1 This CSR must be programmed in Step C of the PHY Initialization sequence	R/W	0x0
[15:4]	Unimplemented	Returns zero on reads	R	0x0

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11.3.233 ProcOdtTimeCtl

- Description: Controls timing of ProcOdt for DQ and DQS termination during reads.
  The enabling and disabling of ProcOdt can be shifted with a granularity of 1UI.

  If WDQSEXTENSION is enabled, this register should be set to 0x03.

  Otherwise, use the recommended settings based on MEMCLK frequency and TwoTckRxDqsPre.
  This will ensure that ProcOdt is enabled before the DQS preamble begins
  and is not disabled until after the DQS postamble ends.

  Recommended configuration if Register TwoTckRxDqsPre==1
  0000MHz < memclk-freq <= 0933 Register POdtStartDelay= 2 Register POdtTailWidth=2
  0933MHz < memclk-freq <= 1200 Register POdtStartDelay= 0 Register POdtTailWidth=2
  1200MHz < memclk-freq <= ------ Register POdtStartDelay= 0 Register POdtTailWidth=3
  ...
  Recommended configuration if TwoTckRxDqsPre==0
  0000MHz < memclk-freq <= 933 Register POdtStartDelay= 2 Register POdtTailWidth=2
  0933MHz < memclk-freq <= 1200 Register POdtStartDelay= 1 Register POdtTailWidth=2
  1200MHz < memclk-freq <= ------ Register POdtStartDelay= 1 Register POdtTailWidth=3
  ...
  See related CSR TxOdtDrvStren.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 056
- Replicated per PState: Yes
- Exists: Always

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Table 11-241 Register Name: ProcOdtTimeCtl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	POdtTailWidth	controls the length of the tail of ProcOdt, units of UI 3 tail 3UI more than for POdtTailWidth + POdtTailWidthExt = 0, maximum 2 tail 2UI more than for POdtTailWidth + POdtTailWidthExt = 0, default 1 tail 1UI more than for POdtTailWidth + POdtTailWidthExt = 0 0 minimum length tail The time from closing the window to receive DQS to ProcODT deassertion is (3 + POdtTailWidth + POdtTailWidthExt - csrTwoTckRxDqsPre) UI	R/W	0x2
[3:2]	POdtStartDelay	controls the start of ProcOdt, units of UI 3 delay start 2 UI, maximum delay of start of ProcOdt 2 delay start 1 UI, 1 delay start 0 UI, default 0 early by 1 UI, The time from ProcODT assertion to opening the window to receive DQS is than (10 - POdtStartDelay) UI. It may be up to 4 pclk smaller if small coarse delays are used (used only at the lowest clock frequencies)	R/W	0x1
[5:4]	POdtTailWidthExt	controls the length of the tail of ProcOdt, units of UI 3 tail 3UI more than for POdtTailWidth + POdtTailWidthExt = 0, 2 tail 2UI more than for POdtTailWidth + POdtTailWidthExt = 0, 1 tail 1UI more than for POdtTailWidth + POdtTailWidthExt = 0 0 minimum length tail extension - default The time from closing the window to receive DQS to ProcODT deassertion is (3 + POdtTailWidth + POdtTailWidthExt - csrTwoTckRxDqsPre) UI	R/W	0x0
[15:6]	Unimplemented	Returns zero on reads	R	0x0

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11.3.234 DllGainCtl

- Description: Controls for the DllGain sequencing for locking and maintaining lock of the LCDL delay cells.
  The DllGain sequencer will start locking with the DllGainIV.
  As the end of locking approaches, the DllGain will be incremented in stages
  until, at the end of locking, the DllGain is the terminal values DllGainTV.
  2^(5-DllGain) is fractional change in the DAC code MstPhase1UI[8:0] of Dll per pclk.
  Firmware uses values for DllGainIV, DllGainTV, and LcdlSeed0 that are optimized
  for minimum locking time; these controls are not to be configured by the user.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 07C
- Replicated per PState: Yes
- Exists: Always

Table 11-242 Register Name: DllGainCtl Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[3:0]	DllGainIV	Initial value of DllGain.	R/W	0x1
[7:4]	DllGainTV	Terminal value of DllGain, ie the value in effect when locking is done and the value used for maintaining lock, ie tracking pclk variation. DllGainTV must be greater than or equal to DllGainIV. The maximum value is 10. The minimum value is 6.	R/W	0xa
[11:8]	DllSeedSel	Reserved, must be configured to be 0.	R/W	0x0
[15:12]	Unimplemented	Returns zero on reads	R	0x0

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11.3.235 DfiRdDataCsDestMap

- Description: This CSR must be default values in LPDDR4 modes.
  Maps dfi_rddata_cs_n (read chip-select asserted low) to destination dimm timing group.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B0
- Replicated per PState: Yes
- Exists: Always

Table 11-243 Register Name: DfiRdDataCsDestMap Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	DfiRdDestm0	Maps dfi_rddata_cs_n_p0[0] to dest DfiRdDestm0 timing For example, if 0 dfi_rddata_cs_n_p0[0] will use Register Rx{En,Clk}DlyTg0 timing.	R/W	0x0
[3:2]	DfiRdDestm1	Maps dfi_rddata_cs_n_p0[1] to dest DfiRdDestm1 timing For example, if 1 dfi_rddata_cs_n[_p01] will use Register Rx{En,Clk}DlyTg1 timing.	R/W	0x1
[5:4]	DfiRdDestm2	Maps dfi_rddata_cs_n_p0[2] to dest DfiRdDestm2 timing For example, if 2 dfi_rddata_cs_n_p0[2] will use Register Rx{En,Clk}DlyTg2 timing.	R/W	0x2
[7:6]	DfiRdDestm3	Maps dfi_rddata_cs_n_p0[3] to dest DfiRdDestm3 timing For example, if 3 dfi_rddata_cs_n_p0[3] will use Register Rx{En,Clk}DlyTg3 timing.	R/W	0x3
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.236 VrefInGlobal

- Description: This Register controls the PHY global VREF generator, and the PHY analog pad BP_VREF
  The mission mode function of the PHY VREF generator is to generate VrefDQ for the PHY RX function.
  This register is written and configured by the PHY training firmware for mission mode function.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B2
- Replicated per PState: Yes
- Exists: Always

Table 11-244 Register Name: VrefInGlobal Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[2:0]	GlobalVrefInSel	GlobalVrefInSel[1:0] controls the mode of the PHY VREF DAC and the BP_VREF pin ========== 2'b00 - PHY Vref DAC Range0 -- BP_VREF = Hi-Z 2'b01 - Reserved Encoding 2'b10 - PHY Vref DAC Range0 -- BP_VREF connected to PLL Analog Bus 2'b11 - PHY Vref DAC Range0 -- BP_VREF connected to PHY Vref DAC ========== GlobalVrefInSel[2] shall be set according to Dram Protocol: Protocol GlobalVrefInSel[2] ---------- DDR4 1'b0 LPDDR4 1'b1 LPDDR4X 1'b1	R/W	0x0

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Table 11-244 Register Name: VrefInGlobal Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[9:3]	GlobalVrefInDAC	DAC code for internal Vref generation The DAC has two ranges; the range is set by GlobalVrefInSel[2] ========== RANGE0 : DDR4 [GlobalVrefInSel[2] = 0] DAC Output Voltage = GlobalVrefInDAC == 6'h00 ? Hi-Z : 0.345*VDDQ + (0.005*GlobalVrefInDAC)*VDDQ ========== RANGE1 : LPDDR4 [GlobalVrefInSel[2] = 1] DAC Output Voltage = GlobalVrefInDAC == 6'h00 ? Hi-Z : (0.005*(GlobalVrefInDAC-1))*VDDQ	R/W	0x40
[13:10]	GlobalVrefInTrim	RSVD	R/W	0x0
[14:14]	GlobalVrefInMode	RSVD	R/W	0x0
[15:15]	Unimplemented	Returns zero on reads	R	0x0

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11.3.237 DfiWrDataCsDestMap

- Description: This CSR must be default values in LPDDR4 modes
  Maps dfi_wrdata_cs_n (write chip-select asserted low) to destination dimm timing group.
  The full dfi interface has 72 values of dfi_wrdata_cs_n, with 8 per byte.
  Byte db (0..8) uses values dfi_wrdata_cs_n[(db*8 + 7):(db*8 + 0)].
  and this register, which is per byte, to determine the timing-control registers
  to use for the asserted chip-select. For simplicity, the subfield description
  does not include the byte offset for dfi_wrdata_cs_n.
  Note that the example values below are the default/reset values.
  If this register is written to all zeroes, then all writes will use Register Tx{Dq,Dqs}Dlyd0 timing.
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0B4
- Replicated per PState: Yes
- Exists: Always

Table 11-245 Register Name: DfiWrDataCsDestMap Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	DfiWrDestm0	Maps dfi_wrdata_cs_n_p0[0] to dest DfiWrDestm0 timing For example, if 0 dfi_wrdata_cs_n_p0[0] will use Register Tx{Dq,Dqs}DlyTg0 timing.	R/W	0x0
[3:2]	DfiWrDestm1	Maps dfi_wrdata_cs_n_p0[1] to dest DfiWrDestm1 timing For example, if 1 dfi_wrdata_cs_n_p0[0] will use Register Tx{Dq,Dqs}DlyTg1 timing.	R/W	0x1
[5:4]	DfiWrDestm2	Maps dfi_wrdata_cs_n_p0[2] to dest DfiWrDestm2 timing For example, if 2 dfi_wrdata_cs_n_p0[0] will use Register Tx{Dq,Dqs}DlyTg2 timing.	R/W	0x2
[7:6]	DfiWrDestm3	Maps dfi_wrdata_cs_n_p0[3] to dest DfiWrDestm3 timing (use Register Tx{Dq,Dqs}DlyTg3) For example, if 3 dfi_wrdata_cs_n_p0[0] will use Register Tx{Dq,Dqs}DlyTg3 timing.	R/W	0x3
[15:8]	Unimplemented	Returns zero on reads	R	0x0

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11.3.238 PllCtrl2

- Description: This csr is to be programmed by bios or other means to set PLL charge-pump settings in various PStates.

```
Dficlk   Dficlk   | PllFreqSel  PllCpPropCtrl  PllCpIntCtrl  PllCpPropGsCtrl  PllCpIntGsCtrl
min (MHz) max (MHz) | [4:0]      [3:0]         [4:0]         [3:0]           [4:0]
==================================================================================================
937.5    1067     | 11000'b    0001'b       00000'b      1011'b        11111'b
625      937.5    | 11001'b    0001'b       00000'b      1011'b        11111'b
468.75   625      | 01010'b    0001'b       00000'b      1011'b        11111'b
312.5    468.75   | 01011'b    0001'b       00000'b      1011'b        11111'b
234.4    312.5    | 00110'b    0001'b       00000'b      1011'b        11111'b
166      234.4    | 00111'b    0001'b       00000'b      1011'b        11111'b
```

- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C5
- Replicated per PState: Yes
- Exists: Always

Table 11-246 Register Name: PllCtrl2 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	PllFreqSel	Adjusts the loop parameters to compensate for different VCO bias points, and input/output clock division ratios. Program based on reference clock freqency (DfiClk) with this table.	R/W	0x19
[15:5]	Unimplemented	Returns zero on reads	R	0x0

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11.3.239 PllCtrl1

- Description: This csr is to be programmed by bios or other means to define PLL frequency in various PStates. See this table for programming based on reference clock frequency (DfiClk).

```
Dficlk   Dficlk   | PllFreqSel  PllCpPropCtrl  PllCpIntCtrl  PllCpPropGsCtrl PllCpIntGsCtrl
min (MHz) max (MHz) | [4:0]      [3:0]         [4:0]        [3:0]          [4:0]
==================================================================================================
937.5    1067     | 11000'b    0001'b       00000'b      1011'b       11111'b
625      937.5    | 11001'b    0001'b       00000'b      1011'b       11111'b
468.75   625      | 01010'b    0001'b       00000'b      1011'b       11111'b
312.5    468.75   | 01011'b    0001'b       00000'b      1011'b       11111'b
234.4    312.5    | 00110'b    0001'b       00000'b      1011'b       11111'b
166      234.4    | 00111'b    0001'b       00000'b      1011'b       11111'b
```

- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0C7
- Replicated per PState: Yes
- Exists: Always

Table 11-247 Register Name: PllCtrl1 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	PllCpIntCtrl	connects directly to cp_int_cntrl<4:0> in PLL. Charge pump integrating current control.	R/W	0x00
[8:5]	PllCpPropCtrl	connects directly to cp_prop_cntrl<3:0> of PLL. Charge pump proportional current control.	R/W	0x1
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.240 PllTestMode

- Description: Additional controls for PLL CP/VCO modes of operation
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0CA
- Replicated per PState: Yes
- Exists: Always

Table 11-248 Register Name: PllTestMode Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[15:0]	PllTestMode	It is required to use default values for this CSR unless directed otherwise by Synopsys. Directly connected to testmode[15:0] pin of PLL	R/W	0x0124

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11.3.241 PllCtrl4

- Description: This csr is to be programmed by bios or other means to set PLL charge-pump settings in various PStates. See this table for programming based on reference clock frequency (DfiClk).

Dficlk min (MHz)	Dficlk max (MHz)	PllFreqSel [4:0]	PllCpPropCtrl [3:0]	PllCpIntCtrl [4:0]	PllCpPropGsCtrl [3:0]	PllCpIntGsCtrl [4:0]
937.5	1067	11000'b	0001'b	00000'b	1011'b	11111'b
625	937.5	11001'b	0001'b	00000'b	1011'b	11111'b
468.75	625	01010'b	0001'b	00000'b	1011'b	11111'b
312.5	468.75	01011'b	0001'b	00000'b	1011'b	11111'b
234.4	312.5	00110'b	0001'b	00000'b	1011'b	11111'b
166	234.4	00111'b	0001'b	00000'b	1011'b	11111'b

- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0CC
- Replicated per PState: Yes
- Exists: Always

Table 11-249 Register Name: PllCtrl4 Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[4:0]	PllCpIntGsCtrl	connects directly to cp_int_gs_cntrl<4:0> in PLL. Charge pump integrating current control for fast relock and gearshift.	R/W	0x1f
[8:5]	PllCpPropGsCtrl	connects directly to cp_prop_gs_cntrl<3:0> of PLL. Charge pump proportional current control for fast relock and gearshift.	R/W	0xb
[15:9]	Unimplemented	Returns zero on reads	R	0x0

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11.3.242 DfiFreqRatio

- Description: DFI Frequency Ratio
- Size: 16 bits
- Register Block type: DWC_DDRPHYA_MASTER
- Register Offset: 0FA
- Replicated per PState: Yes
- Exists: Always

Table 11-250 Register Name: DfiFreqRatio Register-block: DWC_DDRPHYA_MASTER

Bits	Name	Description	Access	Default
[1:0]	DfiFreqRatio	Specifies the ratio DfiCtlClk:MemClk. 00 = 1:1 mode 01 = 1:2 mode 1x = 1:4 mode When DWC_DDRPHY_FIXED_DFICTLCLK_RATIO is defined. This register is ignored.	R/W	0x1
[15:2]	Unimplemented	Returns zero on reads	R	0x0

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