HDMI TX PHY S40
Specification

Revision 1.0

2018/1/30

Revision History

Version	Date	Description
1.0	2018/01/30	Initial release version

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Glossary

The glossary is intended to cover the acronyms used in the document.

Term	Definition
R	Read only/non-Write
R/W	Read/Write
RC	Read-Clear/non-Write
RS	Read-Set/non-Write
RC/W	Read-Clear/Write
RS/W	Read-Set/Write
R/WAC	Read/Write-Automatic-Clear， Clear the bit automatically when the operation of complete. Writing 0 has no effect.
R/WC	Read/Write-Clear
R/WS	Read/Write-Set
RC/WS	Read-Clear/Write-Set
RS/WC	Read-Set/Write-Clear
R/W1C	Read/Write 1 to Clear, Write 0 has non-effect
R/W1S	Read/Write 1 to Set, Write 0 has non-effect
R/W1T	Read/Write 1 to Flip, Write 0 has non-effect
R/W0C	Read/Write 0 to Clear, Write 1 has non-effect
R/W0S	Read/Write 0 to Set, Write 1 has non-effect
R/W0T	Read/Write 0 to Flip, Write 1 has non-effect
RC/W1S	Read-Clear/Write 1 to Set, Write 0 has non-effect
RS/W1C	Read-Set/Write 1 to Clear, Write 0 has non-effect
RC/W0S	Read-Clear/Write 0 to Set, Write 1 has non-effect
RS/W0C	Read-Set/Write 0 to Clear, Write 1 has non-effect
W	Write only/non-Read
WC	Write-Clear/non-Read
WS	Write-Set/non-Read
W1	After reset, Write at the first time, non-Write after the first time/Read
WO1	After reset, Write at the first time, non-Write after the first time/non-Read

1. Product Overview

1.1. Feature

- Support for 4k x 2k and 3D video format
- Support for power collapsing
- Driver with features for extra-long cables
  - Pre-emphasis enable
  - Slope boosting
- Programmable source terminations
- HPD input analog comparator
- Rx sensing
- 27-297 MHz input reference clock
- 50% duty-cycle output clock

1.2. Operating mode

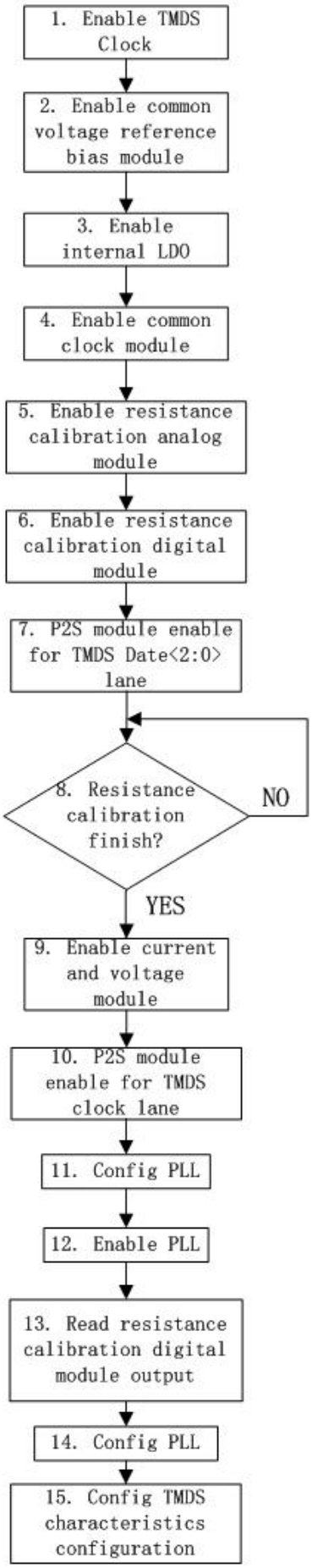
1.2.1. Power-Down Mode

The PHY enters this mode when the ANA_CFG1 register and PLL_CFG1 Register are set to 0x0.

1.2.2. Power Sequence

To operate the HDMI PHY, the following steps have to be followed:

- Write 1'b1 in the ANA_CFG1.TMDSCLK_EN <16> bit field register.
- Write 1'b1 in the ANA_CFG1.ENVBS <1> bit field register.
- Write 1'b1 in the ANA_CFG1.LDOEN <2> bit field register.
- Write 1'b1 in the ANA_CFG1.CKEN <3> bit field register.
- Write 1'b1 in the ANA_CFG1.ENRCAL <19> bit field register.
- Write 1'b1 in the ANA_CFG1.ENCALOG bit field register.
- Write 0x7 in the ANA_CFG1.ENP2S <7:4> bit field register.
- Read the ANA_STS.RCALEND2D <7> bit field register. Until this bit changes to 1'b1, the next step can be followed.
- Write 0xf in the ANA_CFG1.BIASEN <11:8> bit field register.
- Write 0xf in the ANA_CFG1.ENP2S <7:4> bit field register.
- According to the PLL Recommended Configuration(Table 1.1), config the PLL module.
- Write 0x1 in the PLL_CFG1.PLLEN <25> bit field register.
- Read the ANA_STS.RESDO2D <5:0> bit field register. According to the Source Termination Resistors Configuration (Table 1.3), this value is used to calibrate the source termination resistors.
- The PLL mode depends on the B_in. Write 0x1 in the PLL_CFG1.REG_OD1 <31> bit and PLL_CFG1.REG_OD0 <30> bit field register. And write ANA_STS.B_OUT <16:11> bit in the PLL_CFG1.B_IN <5:0> bit field register.
- According to the TMDS Characteristics Recommended Configuration(Table 1.2), config TMDS Characteristics Configuration.



1.2.3. PLL Recommended Configuration

Register Name	Address	Different TMDS Character Rate			
		297MHz	148.5MHz	74.25MHz	27MHz
PLL_CFG1	0x1002C	0x35dc5fc0	0x3ddc5040	0x3ddc5040	0x3ddc5040
PLL_CFG2	0x10030	0x800863C0	0x80084381	0x80084343	0x8008430a
PLL_CFG3	0x10034	0x1	0x1	0x1	0x1

1.2.4. TMDS Characteristics Recommended Configuration

Register Name	Address	Different TMDS Character Rate			
		297MHz	148.5MHz	74.25MHz	27MHz
ANA_CFG1	0x10020	0x01FFFF7F	0x01FFFF7F	0x11FFFF7F	0x11FFFF7F
ANA_CFG2	0x10024	0x8063b000	0x8063a800	0x80623000 | tmp_rcal_200	0x80623000 | tmp_rcal_200
ANA_CFG3	0x10028	0x0F8246B5	0x0F81C485	0x0F814385	0x0F80C285

1.2.5. Source termination resistors Configuration

Symbol	Source termination resistors	Value
tmp_rcal_100	100ohm	RESDO2D >> 1
tmp_rcal_200	200ohm	RESDO2D >> 2

1.3. HDMI TX PHY Register List

Module Name	Base Address
HDMI TX PHY	0x06000000

Register Name	Offset	Description
ANA_CFG1	0x10020	
ANA_CFG2	0x10024	
ANA_CFG3	0x10028	
PLL_CFG1	0x1002c	
PLL_CFG2	0x10030	
PLL_CFG3	0x10034	
ANA_STS	0x10038	
CEC	0x1003c	

1.4. HDMI TX PHY Register Description

1.4.1. CEC Register(Default Value: 0x0000_0000)

Offset: 0x1003c			Register Name: CEC
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	CEC CONTROL SEL 0:cec controller 1:reg control
6	/	/	/

5	~~/~~	~~0x0~~	~~CEC PAD SELO2~~
4	~~/~~	~~0x0~~	~~CEC PAD SELO1~~
3	~~/~~	~~0x1~~	~~CEC PAD INPUT ENABLE~~
2	~~/~~	~~0x1~~	~~CEC PAD OUTPUT ENABLE~~
1	R	0x0	CEC INPUT DATA
0	R/W	0x0	CEC OUTPUT DATA

1.4.2. Controller Version Register(Default Value: 0x0100_0000)

Offset: 0x10ff8			Register Name: CEC
Bit	Read/Write	Default/Hex	Description
31:0	R	32'h01000000	Version of Controller

1.4.3. PHY Version Register(Default Value: 0x0101_0000)

Offset: 0x10ffc			Register Name: CEC
Bit	Read/Write	Default/Hex	Description
31:0	R	32'h01010000	Version of PHY

1.4.4. Debug Control Register(Default Value: 0x0000_0000)

Offset: 0x10000			Register Name: Debug Control
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	reset_reg
30	R/W	0x0	reset_reg_sel
29	R/W	0x0	ppdq_reg
28	R/W	0x0	ppdq_reg_sel
27	R/W	0x0	txpwron_reg
26	R/W	0x0	txpwron_reg_sel
25	R/W	0x0	px_rxsense_reg
24	R/W	0x0	px_rxsense_reg_sel
23:1	/	/	/
0	R/W	0x0	px_lock_reg

1.4.5. Rext Control Register(Default Value: 0x0000_0000)

Offset: 0x10004			Register Name:
Bit	Read/Write	Default/Hex	Description: Rext Control
31	R/W	0x0	enrext
30	R/W	0x0	reg_rext
29:28	R/W	0x0	reg_sint
27:25	/	0x0	
24:20	R/W	0x0	reg_snk
19:18	/	0x0	
17	R/W	0x0	Ib_sel
16	R/W	0x0	cec_cken
15:0	R/W	0x0	hdcptimer set