A40i User Manual

Revision 1.1

Jun. 15, 2018

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Revision History

Revision	Date	Description
1.0	May.22,2018	Initial release version
1.1	Jun.15,2018	**Chapter 3 System** 1. Add notes about clock tree in Section 3.3.2.1. 2. Add guide about spread spectrum function in Section 3.3.2.7. 3. Add operations and functional descriptions, programming guidelines for Timer module in Section 3.7. 4. Add operations and functional descriptions, programming guidelines for High Speed Timer module in Section 3.8. 5. Add operations and functional descriptions, programming guidelines for RTC module in Section 3.11. 6. Add programming guidelines for KEYADC module in Section 3.13. 7. Add programming guidelines for Thermal Sensor module in Section 3.15. 8. Add block diagram, operations and functional descriptions for RTC module in Section 3.18. **Chapter 4 Memory** 1. Add programming guidelines about NDFC in Section 4.2.4. 2. Add programming guidelines about SMHC in Section 4.3.4. **Chapter 7 Display** 1. Add BT656 using guides in Section 7.2.4. **Chapter 8 Interfaces** 1. Add SPI data transfer/receive process in CPU and DMA mode in Section 8.2.4.2. 2. Add programming guidelines about I2S/PCM in Section 8.8.4.

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Chapter 1. About This Documentation

1.1. Purpose

This documentation provides an overall description of the Allwinner's A40i application processor, which describes the overview, features, logical structures, functions and register listings of each module. For details about the interface timings and related parameters ,the pins, pin usages, performance parameters, and package dimension ,please refer to the ***Allwinner A40i Datasheet***.

1.2. Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Programmers in writing code or modifying the Allwinner provided code

1.3. Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

1.4. Notes

1.4.1. Register Attributes

The register attributes that may be found in this document are defined as follows.

Symbol	Description
R	Read Only
R/W	Read/Write

R/WAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete. Writing 0 has no effect
R/WC	Read/Write-Clear
R/W0C	Read/Write 0 to Clear, Writing 1 has no effect
R/W1C	Read/Write 1 to Clear, Writing 0 has no effect
R/W1S	Read/Write 1 to Set, Writing 0 has no effect
W	Write Only

1.4.2. Reset Value Conventions

In the register definition tables:

If other column value in a bit or multiple bits row is "/" ，that this bit or these multiple bits are unused.

If the default value of a bit or multiple bits is "UDF", that the default value is undefined.

1.4.3. Numerical System

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency,data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

The expressions of addresses and data are described as follows.

Symbol	Example	Description
0x	0x0200,0x79	Address or data in hexadecimal
0b	0b010,0b00 000 111	Data or sequence in binary(register description is excluded.)
X	00X,XX1	In data expression,X indicates 0 or 1.For example, 00X indicates 000 or 001, XX1 indicates 001,011,101 or 111.

1.5. Acronyms and Abbreviations

The table below contains acronyms and abbreviations used in this documentation.

AES	Advanced Encryption Standard
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AHB	AMBA High-speed Bus
APB	Advanced Peripheral Bus

ARM	Advanced RISC Machine
AVS	Audio Video Standard
CIR	Consumer Infrared
CP15	Coprocessor 15
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSI	Camera Serial Interface
CVBS	Composite Video Broadcast Signal
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRC	Dynamic Range Compression
DSI	MIPI Display Serial Interface
DVFS	Dynamic Voltage and Frequency Scaling
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FIFO	First In First Out
GIC	Generic Interrupt Controller
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
KEYADC	Analog to Digital Converter for Key
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MAC	Media Access Control
MII	Media Independent Interface
MIPI	Mobile Industry Processor Interface
MIPI DSI	MIPI Display Serial Interface
MMC	Multimedia Card
MPEG	Motion Pictures Expert Group
MPEG1	The First MPEG Compression Scheme Specification
MPEG4	The Most Current MPEG Compression Scheme Specification
MSB	Most Significant Bit

N/A	Not Application
NMI	Non Maskable Interrupt
NTSC	National Television Standards Committee
OHCI	Open Host Controller Interface
OWA	One Wire Audio
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller
PID	Packet Identifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RGB	Read Green Blue
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RTC	Real Time Clock
RSB™	Reduced Serial Bus
SATA	Serial Advanced Technology Attachment
SDIO	Secure Digital Input Output
SDRAM	Sychronous Dynamic Random Access Memory
SOC	System On Chip
SPI	Serial Peripheral Interface
S/PDIF	Sony/Philips Digital Interface Format
SRAM	Static Random Access Memory
TDM	Time Division Multiplexing
TWI	Two Wire Interface
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB OTG	Universal Serial Bus On The Go
UTMI	USB2.0 Transceiver Macrocell Interface
VGA	Video Graphics Array

Chapter 2. Overview

This part describes the overview for A40i processor.

2.1. Processor Overview

The A40i processor represents Allwinner's latest achievement in intelligent industrial control processors. The processor is ideal for applications that require 3D graphics, advanced video processing, rich user interfaces, lower power consumption and higher system integration.

The A40i processor has some very exciting features:

- **CPU:** A40i is based on quad-core Cortex™-A7 CPU architecture, the most power efficient CPU core ARM's ever developed.
- **GPU:** A40i adopts the extensively implemented and technically mature Mali400 MP2 to provide mobile users with superior experience in web browsing, video playback and games.
- **Video Engine:** Supports mainstream high-definition video decoding including H.264, H.263, MPEG1/2/4, xvid, Sorenson Spark, VP6, VP8, AVS/AVS+, WMV7, WMV8 by 1080p@60fps. In the aspect of video encoding, the A40i supports 1080p@45fps H.264 encoding ability.
- **Camera:** Supports dual CMOS sensor parallel interfaces and 4-channel TVIN , which can easily finish multi-channel video recording.
- **Display:** Content can be displayed on 4-lane MIPI DSI displays,or RGB panel, or LVDS panel.TV-out on HDMI V1.4 is also supported.
- **Audio:** Integrated audio codec with 24bit/192kHz DAC playback, and supports I2S/PCM interface for connecting to an external audio codec.I2S/PCM interface includes eight channels of TDM with sampling precision up to 32bit/192kHz.
- **Memory:** Supports external memory interfaces to NAND Flash,SD/eMMC,Nor Flash and SDRAM port. SDRAM port can be configured to support LPDDR2, LPDDR3, DDR2, DDR3, DDR3L.
- **Peripherals:** To reduce total system cost, A40i has a broad range of hardware peripherals to meet the flexible peripheral configuration requirements such as UART, RTP, SPI, CIR, USB2.0 OTG, TWI etc.

2.2. Features

2.2.1. CPU Architecture

- Quad-core ARM Cortex™-A7 Processor
- ARMv7 ISA standard ARM instruction set
- Thumb-2 Technology
- Jazeller RCT
- NEON Advanced SIMD
- VFPv4 floating point
- Large Physical Address Extensions(LPAE)
- 32KB L1 Instruction cache and 32KB L1 Data cache for per CPU
- 512KB L2 cache shared

2.2.2. GPU Architecture

- Mali400 MP2
- Supports OpenGL ES 2.0 ,OpenGL ES 1.1, Open VG 1.1 standard

2.2.3. Memory

2.2.3.1. Boot ROM

- On-chip 36KB ROM boot loader
- Supports fast boot from NAND Flash, eMMC, SD/TF card and SPI Nor Flash
- Supports system code download through USB OTG
- Boot select pin(FEL) is used to select system boot method: boot from USB when FEL is low level,or else enter into fast boot process

2.2.3.2. SDRAM

- Compatible with JEDEC standard DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Up to 2GB address space
- 32-bit data bus width
- DDR3/DDR3L interface with the maximum frequency of 576MHz
- LPDDR3 interface with the maximum frequency of 480MHz
- LPDDR2 interface with the maximum frequency of 432MHz

2.2.3.3. NAND Flash

- Compliant with ONFI 2.3 and Toggle 1.0
- Up to 64-bit ECC per 512 bytes or 1024 bytes
- Supports 1K/2K/4K/8K/16KB page size
- Up to 8-bit data bus width
- Supports 8 chip selects, and 2 ready_busy signals
- Supports SLC/MLC NAND and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

2.2.3.4. SMHC

- Up to four SMHC controllers
- Compatible with eMMC standard specification V5.0, SD physical layer specification V3.0 ,SDIO card specification V2.0
- 1/4/8-bit bus width
- Embedded special DMA to do data transfer
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.2.4. System Peripherals

2.2.4.1. Timer

- 6 Timers
- Two 33-bit AVS counters to synchronize video and audio in the player
- One watchdog to generate reset signal or interrupt
- External 24MHz or 32768Hz crystal oscillator input

2.2.4.2. High Speed Timer

- 4 High Speed Timers
- Clock source is fixed to AHBCLK, and the pre-scale ranges from 1 to 16
- 56-bit counter that can be separated to 24-bit high register and 32-bit low register

2.2.4.3. GIC

- Supports 16 SGIs(Software Generated Interrupt), 16 PPIs(Private Peripheral Interrupt) and 101 SPIs(Shared Peripheral Interrupts)
- Supports ARM architecture security extensions
- Supports ARM architecture virtualization extensions

2.2.4.4. DMA

- 16 channels
- Interrupt generated for each DMA channel
- Transfers data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Programs the DMA burst size
- Flexible data source and destination address generation
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

2.2.4.5. CCU

- 13 PLLs,one external 24MHz oscillator, one 32768Hz oscillator ,an on-chip RC oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.2.4.6. RTC

- Timer, Calendar, Alarm
- Supports full clock features: second/minute/hour/day/month/year(with leap year)

2.2.4.7. PWM

- 8 PWM channels outputs(4 PWM pairs)
- Supports capture input
- Supports three kinds of output waveforms: continuous waveform, pulse waveform and complementarity pair
- Programmable deadzone generator and controllable dead-time
- 0% to 100% adjustable duty cycle
- Up to 24/100MHz output frequency
- Minimum resolution is 1/65536
- Supports interrupt for PWM output and capture input

2.2.4.8. Thermal Sensor

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Supports 2 sensors: sensor0 for CPU,sensor1 for GPU

2.2.4.9. Crypto Engine

- Supports symmetrical algorithm: AES, DES, 3DES
- Supports hash algorithm: MD5,SHA1,SHA224,SHA256,SHA384,SHA512,HMAC
- Supports asymmetrical algorithm: RSA512,RSA1024,RSA2048
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- AES mode: ECB,CBC,CTR,CTS,OFB,CFB
- DES/3DES mode: ECB,CBC,CTR

2.2.4.10. Security ID

- One on-chip efuse
- Size up to 2Kbit for security chip ID
- Supports on-line LDO programming

2.2.5. Video Engine

2.2.5.1. Video Decoder

- Supports video decoding up to 1080p@60fps
- Supports multi-formats:
  - MPEG1 MP/HL: 1080p@60fps
  - MPEG2 MP/HL: 1080p@60fps
  - MPEG4 SP/ASP L5: 1080p@60fps
  - H.263 BP: 1080p@60fps
  - H.264 BP/MP/HP Level4.2: 1080p@60fps
  - xvid: 1080p@60fps

- Sorenson Spark: 1080p@60fps
- VP6 6.0/6.1/6.2: 1080P@60fps
- VP8: 1080p@60fps
- AVS/AVS+ JiZhun: 1080p@60fps
- WMV7/WMV8: 1080p@60fps
- WMV9/VC-1 SP/MP/AP: 1080p@60fps
- JPEG: 16384 x 16384@45MPPS

2.2.5.2. Video Encoder

- H.264 HP encoding up to 1080p@45fps
- JPEG baseline: picture size up to 4096x4096
- Supports H.264 encoding input formats:NV12/NV21/YUV420SP,YUV422SP/NV16,NU12/NV21/YVU420SP, YVU422SP/NV61, 32 x 32 tile-based,128 x 32 tile-based,ARGB8888,RGBA8888,ABGR8888,BGRA8888, YU12/YUV420P,YV12/YVU420P,YU16/YUV422P,YV16/YVU422P,raw YUYV422,raw UYVY422,raw YVYU422,raw VYUY422
- Supports JPEG encoding input formats:YUV420/YUV422/YUV444
- Alpha blending
- Thumb generation
- 4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

2.2.6. Display Subsystem

2.2.6.1. DE2.0

- Supports output size up to 2048 x 2048
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports motion-adaptive de-interlace for 480i, 576i and 1080i inputs
- Supports input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports SmartColor2.0 for excellent display experience

2.2.6.2. Video Output

- Supports HDMI 1.4 transmitter with HDCP 1.2, up to 1080p@60fps
- Supports 4 lanes MIPI DSI up to 1080p@60fps
- Supports LVDS interface up to 1920 x 1080@60fps
- Supports RGB interface up to 1920 x 1080@60fps
- Supports TV output, including 4-ch CVBS, 1-ch YPbPr and 1-ch VGA

2.2.7. Image Subsystem

- Supports TV decoder: 4-ch analog CVBS or 1-ch YPbPr(480i/576i/480p/576p) signal input
- Dual CMOS sensor parallel interfaces :CSI0 and CSI1
  - Supports 8-bit YUV422 CMOS sensor interface and 8bit BT656 interface for each CSI

- Supports CCIR656 protocol for each CSI
- Supports 16-bit BT1120 interface for CSI0
- Supports 24-bit RGB/YUV444 input for CSI1
- Supports multi-channel ITU-R BT.656 time-multiplexed format for CSI0
- CSI0 supports still capture resolution up to 5M,and video capture resolution up to 1080p@30fps
- CSI1 supports still capture resolution up to 5M,and video capture resolution up to 720p@30fps

2.2.8. Analog Subsystem

2.2.8.1. Analog Codec

- Two audio digital-to-analog(DAC) channels
  - Up to 100±3dB SNR during DAC playback
  - Supports DAC sample rate from 8kHz to 192kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Two audio analog-to-digital(ADC) channels
  - Up to 93±3dB SNR during ADC capture
  - Supports ADC sample rate from 8kHz to 48kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Four audio inputs:
  - Two mono microphone inputs
  - One stereo Line-in input
  - One stereo FM-in input
- Two audio outputs:
  - One differential PHONEOUT output
  - One stereo headphone output
- Supports analog/digital volume control
- Supports dynamic range controller adjusting the DAC playback and ADC capture

2.2.8.2. I2S/PCM

- Up to two I2S/PCM interfaces
- Compliant with standard Philips Inter-IC sound(I2S) bus specification
- Compliant with left-justified, right-justified, PCM mode, and TDM(Time Division Multiplexing) format
- Full-duplex synchronous work mode
- Master and slave mode configured
- Adjustable audio sample resolution from 8-bit to 32-bit
- Sample rate from 8kHz to 192kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- Supports programmable PCM frame width:1 BCLK width(short frame) and 2 BCLKs width(long frame)

2.2.8.3. OWA

- IEC-60958 transmitter and receiver functionality
- Compatible with S/PDIF protocol
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 32x24 bits TX FIFO for audio data transfer
- Programmable FIFO thresholds

2.2.8.4. AC97

- Compliant with AC97 2.3 component specification
- Full-duplex synchronous serial interface
- Up to 48kHz sampling rate
- Channels support mono or stereo samples of 16(standard),18(optional) and 20(optional) bit wide
- Supports DRA mode

2.2.9. External Peripherals

2.2.9.1. USB

- USB 2.0 OTG, with integrated one USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Support High-Speed(HS,480Mbit/s),Full-Speed(FS,12Mbit/s),and Low-Speed(LS,1.5Mbit/s) in host mode
  - Supports High-Speed (HS, 480Mbit/s), Full-Speed (FS, 12Mbit/s) in Device mode
  - Up to 8 user-configurable endpoints for Bulk , Isochronous, Control and Interrupt(Endpoint1, Endpoint2, Endpoint3, Endpoint4)
- Two USB Hosts, with integrated two USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface(EHCI)Specification, Version 1.0, and the Open Host Controller Interface(OHCI) Specification, Version 1.0a.

2.2.9.2. EMAC

- Compliant with IEEE 802.3 standard
- Supports 10/100Mbps data transfer rate
- Supports MII PHY interface
- Supports full and half duplex operations

2.2.9.3. GMAC

- Compliant with the IEEE 802.3-2002 standard
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
- Supports 10/100/1000Mbps data transfer rates
- Supports MII/RGMII PHY interface
- Supports a variety of flexible address filtering modes
- Supports full and half duplex operations

2.2.9.4. Transport Stream Controller

- Up to 2 Transport Stream Controllers
- One external Synchronous Parallel Interface(SPI) and one external Synchronous Serial Interface(SSI)
- SPI and SSI timing parameters are configurable
- Multiple transport stream packet(188,192,204) format support
- Supports 32-channel PID filter
- Supports hardware PCR packet detecting

2.2.9.5. TWI

- Up to 5 TWIs(Two Wire Interface)
- Supports Standard mode(up to 100kbit/s) and Fast mode(up to 400kbit/s)

- Master/Slave configurable
- Allows 10-bit addressing transactions

2.2.9.6. Smart Card Reader

- Supports ISO/IEC 7816-3 and EMV2000(4.0) specifications
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports configurable timing functions:
  - Smart Card activation time
  - Smart Card reset time
  - Guard time
  - Timeout timers

2.2.9.7. SPI

- Up to 4 independent SPI controllers,each SPI controller with two CS signals
- Full-duplex synchronous serial interface
- Master/Slave configurable
- 1-,or 2-wire mode
- Polarity and phase are configurable
- SPI clock is configurable

2.2.9.8. UART

- Up to 8 UART controllers
  - UART0 with 2 wires for debug tools
  - UART1 with 8 wires
  - UART2/3 each with 4 wires
  - Others with 2 wires
- Compatible with industry-standard 16550 UARTs
- Supports for word length from 5 to 8 bits,an optional parity bit,and 1,1.5 or 2 stop bits
- Programmable parity(even,odd and no parity)

2.2.9.9. PS2

- Two PS2 controllers
- Compliant with IBM PS2 and AT-compatible keyboard and mouse interface
- Dual-role controller: PS2 host or PS2 device
- Odd parity generation and checking

2.2.9.10. CIR

- Two CIR controllers
- Flexible receiver for consumer IR remote control

- Programmable FIFO thresholds

2.2.9.11. SATA

- One SATA Host controller
- Supports SATA 1.5Gb/s and SATA 3.0Gb/s
- Compliant with SATA spec 2.6 and AHCI Revision 1.3 specifications
- Supports external SATA(eSATA)
- Supports power management features including automatic Partial to Slumber transition

2.2.9.12. Keypad

- One keypad matrix interface up to 8 rows and 8 columns
- Interrupt for key press or key release
- Internal debouncing filter to prevent switching noises

2.2.9.13. KEYADC

- Up to two ADC channels for key application
- 6-bit resolution
- Voltage input range between 0V to 2V
- Supports hold key,already hold key and continuous key
- Supports single,normal and continuous mode

2.2.9.14. RTP

- 4-wire I/F
- 12-bit SAR type A/D converter
- Dual touch detection
- Sampling frequency up to 2MHz
- Supports X,Y change function

2.2.10. Package

- FBGA 468 balls,0.65mm ball pitch, 16x16 mm

2.3. Block Diagram

The follow figure shows the block diagram of the A40i processor.

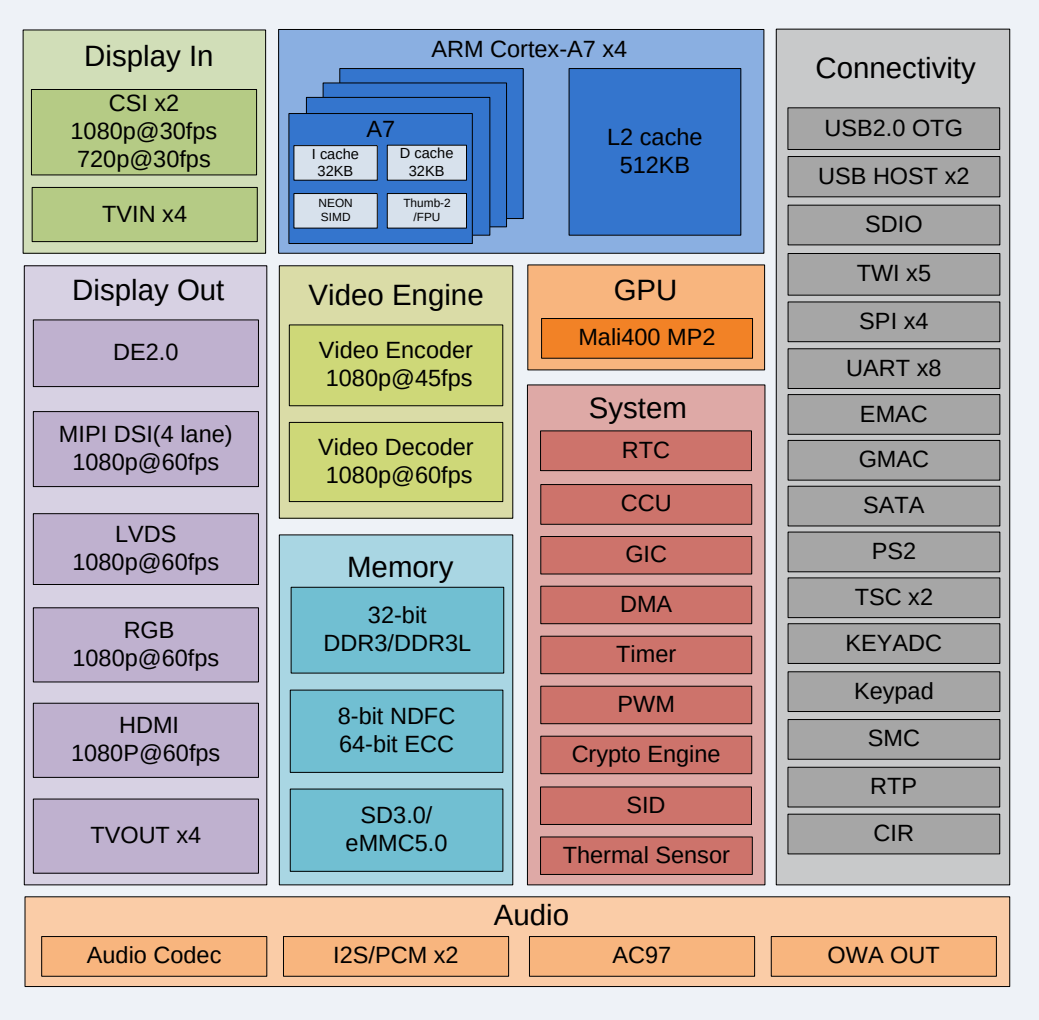


Figure 2-1. A40i Block Diagram

The A40i typical application diagram is shown in Figure 2-2.

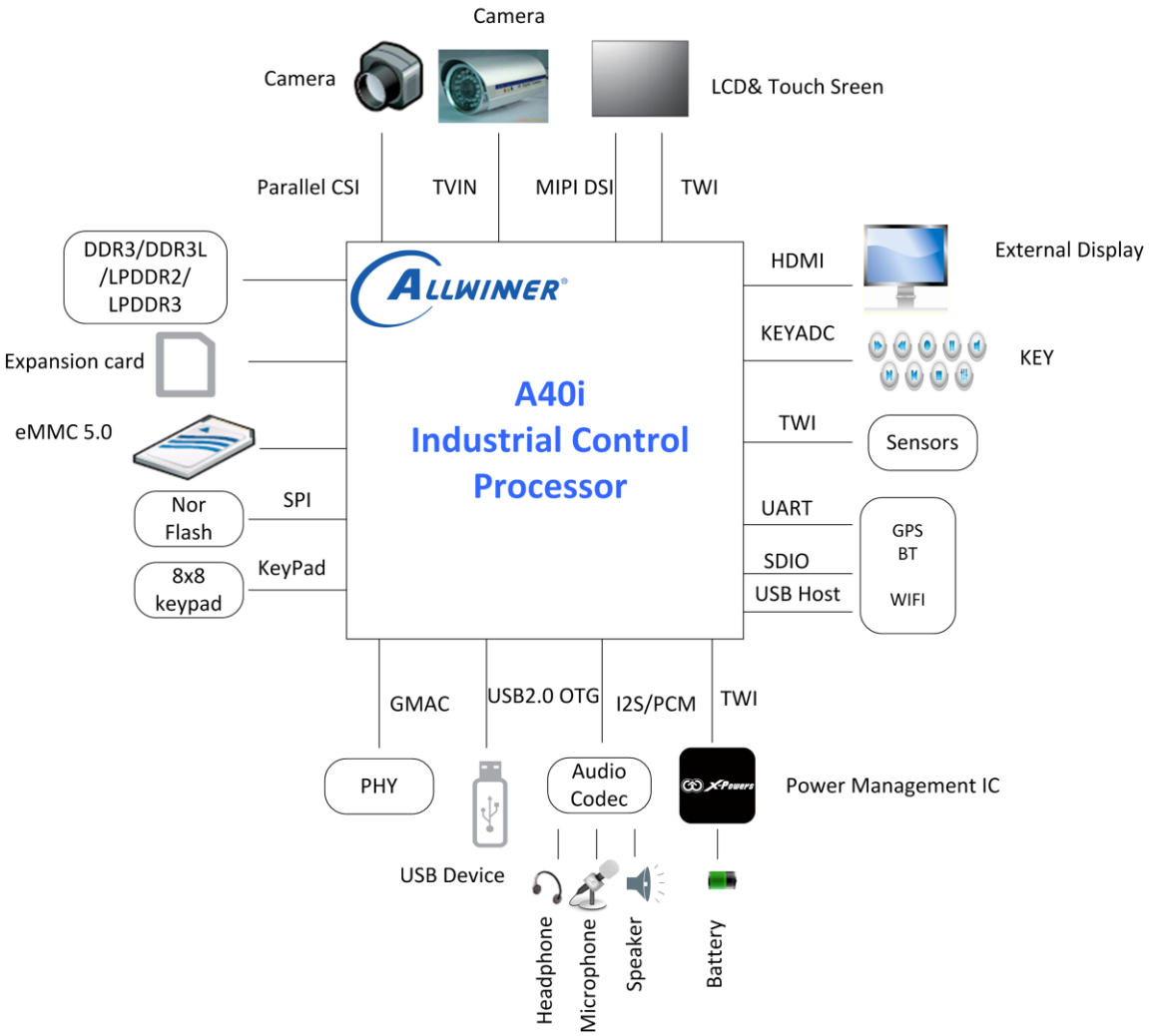


Figure 2-2. A40i Typical Application Diagram

Chapter 3. System

This part details the A40i system construction from following aspects.

- Memory Mapping
- CPU Configuration
- CCU
- System Boot
- System Control
- PWM
- Timer
- High Speed Timer
- GIC
- DMA
- RTC
- Audio Codec
- KEYADC
- RTP
- Thermal Sensor
- Crypto Engine
- Security ID
- Port Controller

3.1. Memory Mapping

Module	Address	Size(Bytes)
SRAM A1	0x0000 0000---0x0000 3FFF	16K
SRAM A2	0x0000 4000---0x0000 7FFF	16K
SRAM A3	0x0000 8000---0x0000 B3FF	13K
SRAM A4	0x0000 B400---0x0000 BFFF	3K
DE2.0	0x0100 0000---0x013F FFFF	4M
De-interlaced	0x0140 0000---0x0141 FFFF	128K
SRAM Controller	0x01C0 0000---0x01C0 0FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
NDFC	0x01C0 3000---0x01C0 3FFF	4K
Transport Stream Controller	0x01C0 4000---0x01C0 4FFF	4K
SPI 0	0x01C0 5000---0x01C0 5FFF	4K
SPI 1	0x01C0 6000---0x01C0 6FFF	4K
CSI 0	0x01C0 9000---0x01C0 9FFF	4K
KEYSRAM	0x01C0 A000---0x01C0 AFFF	4K
EMAC	0x01C0 B000---0x01C0 BFFF	4K
SD/MMC 0	0x01C0 F000---0x01C0 FFFF	4K
SD/MMC 1	0x01C1 0000---0x01C1 0FFF	4K
SD/MMC 2	0x01C1 1000---0x01C1 1FFF	4K
SD/MMC 3	0x01C1 2000---0x01C1 2FFF	4K
USB 0_OTG	0x01C1 3000---0x01C1 3FFF	4K
USB 0_HOST	0x01C1 4000---0x01C1 4FFF	4K
Crypto Enigne	0x01C1 5000---0x01C1 5FFF	4K
SPI 2	0x01C1 7000---0x01C1 7FFF	4K
SATA	0x01C1 8000---0x01C1 8FFF	4K
USB1_HOST	0x01C1 9000---0x01C1 9FFF	4K
SID	0x01C1 B000---0x01C1 BFFF	4K
USB 2_HOST	0x01C1 C000---0x01C1 CFFF	4K
CSI 1	0x01C1 D000---0x01C1 DFFF	4K
SPI 3	0x01C1 F000---0x01C1 FFFF	4K
CCU	0x01C2 0000---0x01C2 03FF	1K
RTC	0x01C2 0400---0x01C2 07FF	1K
Port Controller	0x01C2 0800---0x01C2 0BFF	1K
Timer	0x01C2 0C00---0x01C2 0FFF	1K
OWA	0x01C2 1000---0x01C2 13FF	1K
AC97	0x01C2 1400---0x01C2 17FF	1K
CIR 0	0x01C2 1800---0x01C2 1BFF	1K
CIR 1	0x01C2 1C00---0x01C2 1FFF	1K
I2S/PCM 0	0x01C2 2000---0x01C2 23FF	1K
I2S/PCM 1	0x01C2 2400---0x01C2 27FF	1K
I2S/PCM 2	0x01C2 2800---0x01C2 2BFF	1K
Audio Codec	0x01C2 2C00---0x01C2 2FFF	1K

Module	Address	Size(Bytes)
Keypad	0x01C2 3000---0x01C2 33FF	1K
PWM	0x01C2 3400---0x01C2 37FF	1K
KEYADC	0x01C2 4400---0x01C2 47FF	1K
THS	0x01C2 4C00---0x01C2 4FFF	1K
RTP	0x01C2 5000---0x01C2 53FF	1K
PMU	0x01C2 5400---0x01C2 57FF	1K
CPU Configuration	0x01C2 5C00---0x01C2 5FFF	1K
UART 0	0x01C2 8000---0x01C2 83FF	1K
UART 1	0x01C2 8400---0x01C2 87FF	1K
UART 2	0x01C2 8800---0x01C2 8BFF	1K
UART 3	0x01C2 8C00---0x01C2 8FFF	1K
UART 4	0x01C2 9000---0x01C2 93FF	1K
UART 5	0x01C2 9400---0x01C2 97FF	1K
UART 6	0x01C2 9800---0x01C2 9BFF	1K
UART 7	0x01C2 9C00---0x01C2 9FFF	1K
PS2 0	0x01C2 A000---0x01C2 A3FF	1K
PS2 1	0x01C2 A400---0x01C2 A7FF	1K
TWI 0	0x01C2 AC00---0x01C2 AFFF	1K
TWI 1	0x01C2 B000---0x01C2 B3FF	1K
TWI 2	0x01C2 B400---0x01C2 B7FF	1K
TWI 3	0x01C2 B800---0x01C2 BBFF	1K
Reserved	0x01C2 BC00---0x01C2 BFFF	1K
TWI 4	0x01C2 C000---0x01C2 C3FF	1K
Smart Card Reader	0x01C2 C400---0x01C2 C7FF	1K
TVD_TOP	0x01C3 0000---0x01C3 0FFF	4K
TVD0	0x01C3 1000---0x01C3 1FFF	4K
TVD1	0x01C3 2000---0x01C3 2FFF	4K
TVD2	0x01C3 3000---0x01C3 3FFF	4K
TVD3	0x01C3 4000---0x01C3 4FFF	4K
GPU	0x01C4 0000---0x01C4 FFFF	64K
GMAC	0x01C5 0000---0x01C5 FFFF	64K
High Speed Timer	0x01C6 0000---0x01C6 0FFF	4K
DRAM Common	0x01C6 2000---0x01C6 2FFF	4K
DRAM Controller	0x01C6 3000---0x01C6 3FFF	4K
TCON_TOP	0x01C7 0000---0x01C7 0FFF	4K
TCON_LCD0	0x01C7 1000---0x01C7 1FFF	4K
TCON_LCD1	0x01C7 2000---0x01C7 2FFF	4K
TCON_TV0	0x01C7 3000---0x01C7 3FFF	4K
TCON_TV1	0x01C7 4000---0x01C7 4FFF	4K
GIC	0x01C8 0000---0x01C8 7FFF	32K
TVE_TOP	0x01C9 0000---0x01C9 3FFF	16K
TVE0	0x01C9 4000---0x01C9 7FFF	16K
TVE1	0x01C9 8000---0x01C9 BFFF	16K
MIPI_DSI	0x01CA 0000---0x01CA 0FFF	4K

Module	Address	Size(Bytes)
MIPI_DPHY	0x01CA 1000---0x01CA 1FFF	4K
VE	0x01D0 0000---0x01DF FFFF	1024K
MP	0x01E8 0000---0x01E9 FFFF	128K
HDMI	0x01EE 0000---0x01EF FFFF	128K
CoreSight Debug Module	0x3F50 0000---0x3F50 FFFF	64K
CPUBIST	0x3F50 1000---0x3F50 1FFF	4K
DCU	0x3FFF 0000---0x3FFF FFFF	64K
DRAM	0x4000 0000---0xBFFF FFFF	2G
BROM	0xFFFF 0000---0xFFFF 8FFF	36K

3.2. CPU Configuration

3.2.1. Overview

The CPU configuration module features:

- Software reset control
- CPU configuration
- CPU IDLE configuration
- Power control
- 64-bit common counter

3.2.2. Register List

Module Name	Base Address
CPU Configuration	0x01C25C00

Register Name	Offset	Description
CPU0_RST_CTRL	0x0040	CPU0 Reset Control
CPU0_CTRL_REG	0x0044	CPU0 Control Register
CPU0_STATUS_REG	0x0048	CPU0 Status Register
CPU1_RST_CTRL	0x0080	CPU1 Reset Control
CPU1_CTRL_REG	0x0084	CPU1 Control Register
CPU1_STATUS_REG	0x0088	CPU1 Status Register
CPU2_RST_CTRL	0x0040	CPU2 Reset Control
CPU2_CTRL_REG	0x0044	CPU2 Control Register
CPU2_STATUS_REG	0x0048	CPU2 Status Register
CPU3_RST_CTRL	0x0080	CPU3 Reset Control
CPU3_CTRL_REG	0x0084	CPU3 Control Register
CPU3_STATUS_REG	0x0088	CPU3 Status Register
CPUX_PWROFF_GATING_REG	0x0110	CPUX Power Off Gating(Power clamp) Register
CPU0_PWR_SWITCH_REG	0x0120	CPU0 Power Switch Control Register
CPU1_PWR_SWITCH_REG	0x0124	CPU1 Power Switch Control Register
CPUIDLE_EN	0x0140	CPUIDLE Enable Control Register
CLOSE_FLAG	0x0144	Close Core Flag Register
IRQ_FIQ_STATUS_CTRL	0x0148	IRQ_FIQ Output Status and Control Register
PWR_SW_DELAY	0x0150	Power Switch Operation Delay Register
CONFIG_DELAY	0x0154	Configuration Delay Register
PWR_DOWN_CFG	0x0158	Power Down Configuration Register
PWR_UP_CFG0	0x0160	Power Up Configuration Register0
PWR_UP_CFG1	0x0164	Power Up Configuration Register1
PWR_UP_CFG2	0x0168	Power Up Configuration Register2
PWR_UP_CFG3	0x016C	Power Up Configuration Register3

Register Name	Offset	Description
PWR_UP_CFG4	0x0170	Power Up Configuration Register4
PWR_UP_CFG5	0x0174	Power Up Configuration Register5
GENER_CTRL_REG	0x0184	General Control Register
EVENT_IN_REG	0x0190	Event Input Register
CNT64_CTRL_REG	0x0280	64-bit Counter Control Register
CNT64_LOW_REG	0x0284	64-bit Counter Low Register
CNT64_HIGH_REG	0x0288	64-bit Counter High Register

3.2.3. Register Description

3.2.3.1. CPU0 Reset Control(Default Value: 0x0000_0003)

Offset: 0x0040			Register Name: CPU0_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x1	CPU0_CORE_RESET. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: Assert 1: De-assert
0	R/W	0x1	CPU0_RESET. CPU0 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: Assert 1: De-assert

3.2.3.2. CPU0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CPU0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU0_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: Enable 1: Disable

3.2.3.3. CPU0 Status Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: CPU0_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

Offset: 0x0048			Register Name: CPU0_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode 0: Processor is not in WFI standby mode 1: Processor is in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode 0: Processor is not in WFE standby mode 1: Processor is in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.2.3.4. CPU1 Reset Control(Default Value: 0x0000_0001)

Offset: 0x0080			Register Name: CPU1_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CPU1_CORE_RESET. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: Assert 1: De-assert
0	R/W	0x1	CPU1_RESET. CPU1 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: Assert 1: De-assert

3.2.3.5. CPU1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: CPU1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU1_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: Enable 1: Disable

3.2.3.6. CPU1 Status Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: CPU1_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode 0: Processor is not in WFI standby mode. 1: Processor is in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode 0: Processor is not in WFE standby mode 1: Processor is in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.2.3.7. CPU2 Reset Control(Default Value: 0x0000_0001)

Offset: 0x00C0			Register Name: CPU2_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CPU2_CORE_RESET. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: Assert 1: De-assert
0	R/W	0x1	CPU2_RESET. CPU2 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: Assert 1: De-assert

3.2.3.8. CPU2 Control Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: CPU2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: Enable 1: Disable

3.2.3.9. CPU2 Status Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: CPU2_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode 0: Processor is not in WFI standby mode. 1: Processor is in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode 0: Processor is not in WFE standby mode 1: Processor is in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.2.3.10. CPU3 Reset Control(Default Value: 0x0000_0001)

Offset: 0x0100			Register Name: CPU3_RST_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	CPU3_CORE_RESET. These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic. 0: Assert 1: De-assert
0	R/W	0x1	CPU3_RESET. CPU3 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: Assert 1: De-assert

3.2.3.11. CPU3 Control Register(Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: CPU3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CPU_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: Enable 1: Disable

3.2.3.12. CPU3 Status Register(Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: CPU3_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode 0: Processor is not in WFI standby mode. 1: Processor is in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode 0: Processor is not in WFE standby mode 1: Processor is in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

3.2.3.13. CPUX Power Off Gating Register(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: CPUX_PWROFF_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	PWROFF_GATING[3:0] Gating the corresponding modules when the corresponding CPU power off. 0: Invalid 1: Valid The corresponding bit should be set to 1 before the corresponding CPU power-off while it should be set to 0 after CPU power-on.

3.2.3.14. CPU0 Power Switch Control Register(Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: CPU0_PWR_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CPU_PWR_SWITCH[7:0] 0x00: Power On 0xFF: Power Off

3.2.3.15. CPU1 Power Switch Control Register(Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: CPU1_PWR_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CPU_PWR_SWITCH[7:0]

Offset: 0x0124			Register Name: CPU1_PWR_SWITCH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0x00: Power On 0xFF: Power Off

3.2.3.16. CPUIDLE Enable Control Register(Default Value: 0x0000_0000)

Offset: 0x140			Register Name: CPUIDLE_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	KEYFILED Only the register can be written with 0x16AAXXXX at first(X means any value),then write 0xAA16000x,the “x”(x stand for 0 or 1) can be written into the bit0.
15:1	/	/	/
0	R/W	0x0	CPUIDLE_EN 0: Disable 1: Enable

3.2.3.17. Close Core Flag Register(Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: CLOSE_FLAG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x0	CLOSE_CORE[3:0] 0: Normal 1: Start to close core Only the corresponding core could set the corresponding bit filed.The bit will be cleared after the corresponding core power-off.

3.2.3.18. IRQ_FIQ Status and Control Register(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: IRQ_FIQ_STATUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	FIQ_MASK[3:0] FIQ output mask to this module 0: Normal 1: Mask
23:20	/	/	/
19:16	R/W	0x0	IRQ_MASK[3:0] IRQ output mask to this module 0: Normal 1: Mask
15:12	/	/	/
11:8	R	0x0	FIQ_OUT[3:0]

Offset: 0x0148			Register Name: IRQ_FIQ_STATUS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			FIQ wakeup output 0: Normal 1: FIQ Happen
7:4	/	/	/
3:0	R	0x0	IRQ_OUT[3:0] IRQ wakeup output 0: Normal 1: IRQ Happen

3.2.3.19. Power Switch Delay Register(Default Value: 0x0000_000A)

Offset: 0x0150			Register Name: PWR_SW_DELAY
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xA	DELAY_TMR Delay time(1~255us) when setting power switch value.

3.2.3.20. Configuration Delay Register(Default Value: 0x0000_0001)

Offset: 0x0154			Register Name: CONFIG_DELAY
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x1	DELAY_TMR Delay time(1~255us) between different steps.

3.2.3.21. Power Down Configuration Register(Default Value: 0x0000_00FF)

Offset: 0x0158			Register Name: PWR_DOWN_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xFF	Set this value to power switch register when CPUx power down.

3.2.3.22. Power Up Configuration Register0(Default Value: 0x0000_00FE)

Offset: 0x0160			Register Name: PWR_UP_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0xFE	Set this value to power switch register when CPUx power up.

3.2.3.23. Power Up Configuration Register1(Default Value: 0x0000_00FC)

Offset: 0x0164			Register Name: PWR_UP_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0164			Register Name: PWR_UP_CFG1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xFC	Set this value to power switch register when CPUx power up.

3.2.3.24. Power Up Configuration Register2(Default Value: 0x0000_00F8)

Offset: 0x0168			Register Name: PWR_UP_CFG2
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xF8	Set this value to power switch register when CPUx power up.

3.2.3.25. Power Up Configuration Register3(Default Value: 0x0000_00F0)

Offset: 0x016C			Register Name: PWR_UP_CFG3
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xF0	Set this value to power switch register when CPUx power up.

3.2.3.26. Power Up Configuration Register4(Default Value: 0x0000_00C0)

Offset: 0x0170			Register Name: PWR_UP_CFG4
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xC0	Set this value to power switch register when CPUx power up.

3.2.3.27. Power Up Configuration Register5(Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: PWR_UP_CFG5
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x00	Set this value to power switch register when CPUx power up.

3.2.3.28. General Control Register(Default Value: 0x1000_0020)

Offset: 0x0184			Register Name: GENER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x1	AXI2MBUS_RST AXI2MBUS logic circuit reset 0: Assert 1: De-assert
27:9	/	/	/
8	R/W	0x0	CFGSDISABLE. Disable write access to some secure GIC registers.
7:6	/	/	/

Offset: 0x0184			Register Name: GENER_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R/W	0x1	L2_RST. L2 Reset.(SCU global reset) 0: Apply reset to shared L2 memory system controller. 1: Do not apply reset to shared L2 memory system controller.
4	R/W	0x0	L2_RST_DISABLE. Disable automatic L2 cache invalidate at reset 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3:0	R/W	0x0	L1_RST_DISABLE. L1 Reset Disable[3:0]. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

3.2.3.29. Event Input Register(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: EVENT_IN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EVENT_IN. Event input that can wake-up CPUx from WFE standby mode.

3.2.3.30. 64-bit Counter Control Register(Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: CNT64_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: /
1	R/W	0x0	CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: No effect 1: Latch the 64-bit counter to the Low/High registers and it will change to zero after the registers are latched.
0	R/W	0x0	CNT64_CLR_EN. 64-bit Counter Clear Enable. 0: No effect 1: Clear the 64-bit Counter Low/High registers and it will change to zero after the registers are cleared. It is not recommended to clear this counter arbitrarily.

NOTE

This 64-bit counter will start to count as soon as the system power on finished.

3.2.3.31. 64-bit Counter Low Register(Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: CNT64_LOW_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CNT64_LO. 64-bit Counter [31:0].

3.2.3.32. 64-bit Counter High Register(Default Value: 0x0000_0000)

Offset: 0x0288			Register Name: CNT64_HIGH_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CNT64_HI. 64-bit Counter [63:32].

3.3. CCU

3.3.1. Overview

The CCU provides the registers to program the PLLs and the controls most of the clock generation, division, distribution, synchronization and gating. CCU input signals include the external clock for the reference frequency (24MHz). The outputs from CCU are mostly clocks to the other blocks in the system.

Features:

- 13 PLLs, a 24MHz oscillator, a 32768Hz low-power oscillator,and an on-chip RC oscillator
- Bus source and division
- Clock output control
- Bus clock gating and software reset

The PLLs detailed specification is as follows:

Table 3-1. PLLs Detailed Specification

PLL	Frequency Range	Actual Work Frequency	Spread Spectrum	Linear FM	Rate Control	Pk-Pk	Lock Time
PLL_CPU	60MHz~2.1GHz	60MHz~1.2GHz	Yes	No	No	<200ps	<1.5ms
PLL_AUDIO	24.576MHz, 22.5792MHz	24.576MHz, 22.5792MHz, 196.608MHz, 180.637MHz	Yes(fractional frequency division)	No	No	<200ps	<500us
PLL_GPU	192MHz~600MHz	384MHz	Yes	No	No	<200ps	<500us
PLL_PERIPH0(2X)	504MHz~1.4GHz	1.2GHz	No	No	No	<200ps	<500us
PLL_PERIPH1(2X)	504MHz~1.4GHz	1.2GHz	Yes	No	No	<200ps	<500us
PLL_MIPI	182MHz~1.508GHz	200MHz~1.5GHz	Yes	No	No	<200ps	<500us
PLL_DDR0	192MHz~800MHz	240MHz~800MHz	Yes	Yes	Yes	<200ps	<2ms
	800MHz~1.3GHz	800MHz~1.3GHz				<140ps	
	1.3GHz~1.8GHz	1.3GHz~1.6GHz				<100ps	
PLL_DDR1	192MHz~800MHz	240MHz~800MHz	Yes	Yes	Yes	<200ps	<2ms
	800MHz~1.3GHz	800MHz~1.3GHz				<140ps	
	1.3GHz~1.8GHz	1.3GHz~1.6GHz				<100ps	
PLL_VIDEO0	192MHz~600MHz	192MHz~600MHz	Yes	No	No	<200ps	<500us
PLL_VIDEO1	192MHz~600MHz	297MHz	Yes	No	No	<200ps	<500us
PLL_VE	192MHz~600MHz	297MHz,321MHz	Yes	No	No	<200ps	<500us
PLL_DE	192MHz~600MHz	192MHz~600MHz	Yes	No	No	<200ps	<500us
PLL_SATA	8MHz~300MHz	100MHz	No	No	No	<140ps	2ms

3.3.2. Operations and Functional Descriptions

3.3.2.1. Block Diagram

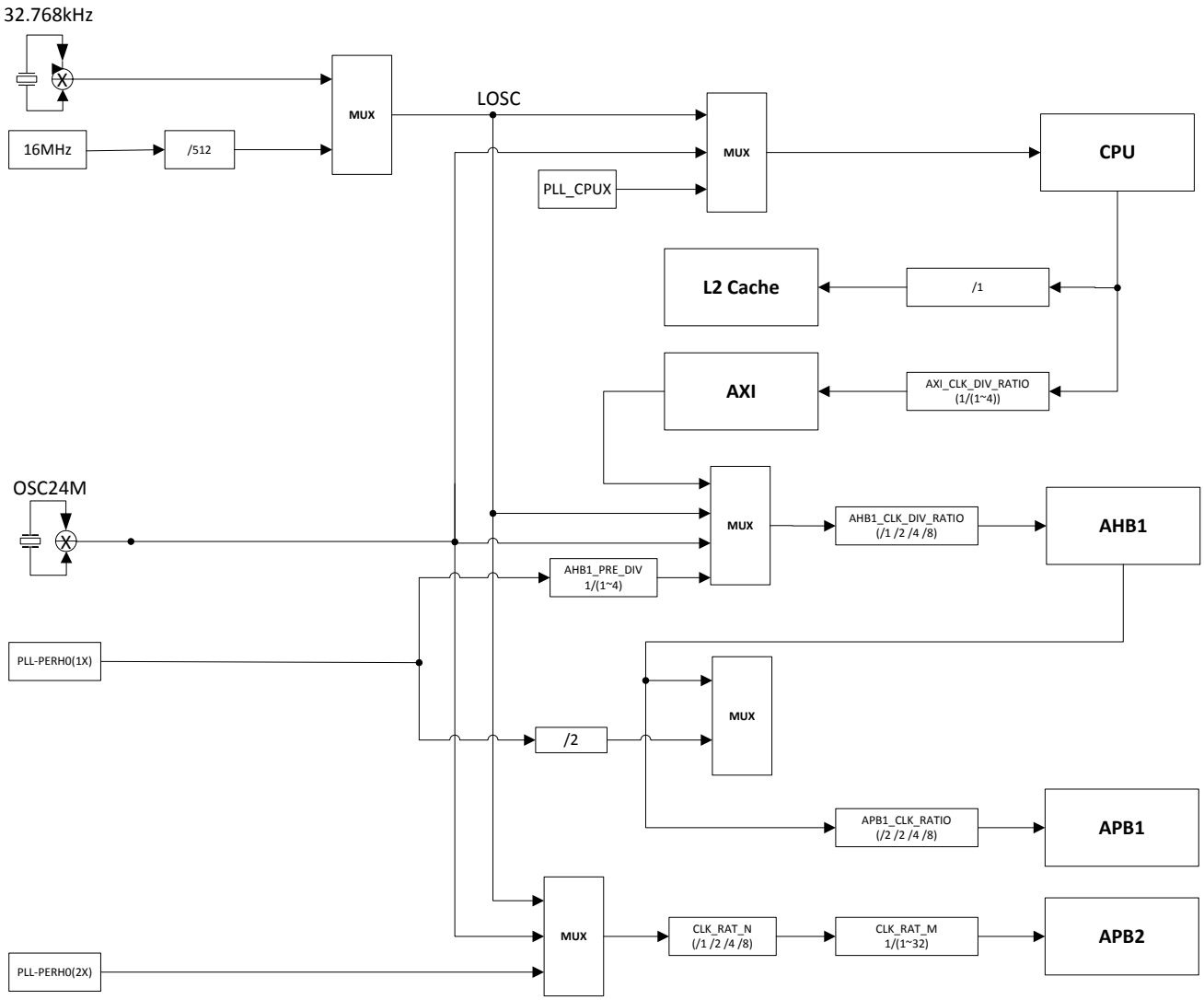


Figure 3-1. A40i Bus Block Diagram

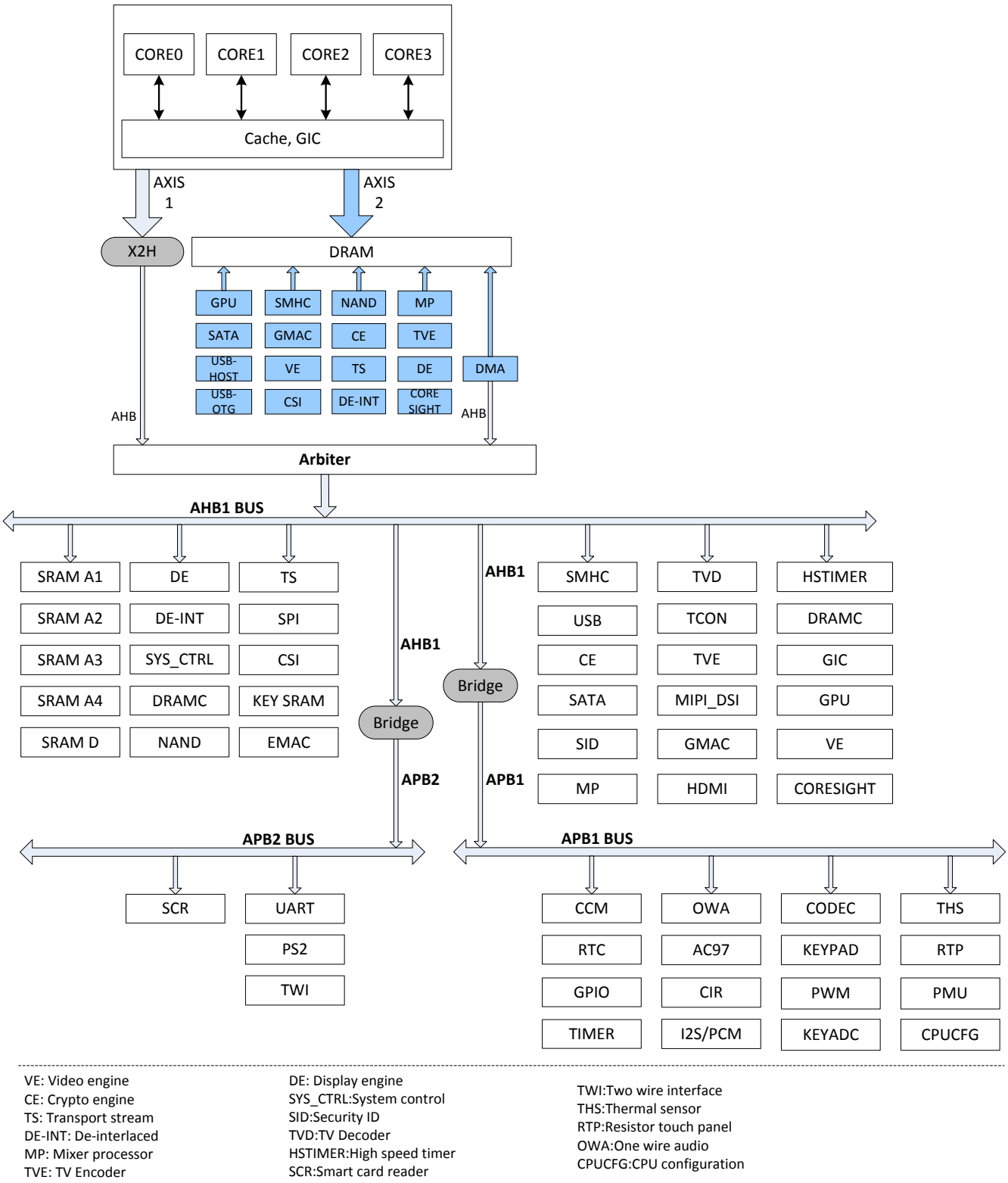


Figure 3-2. A40i Clock Tree Diagram

The above clock tree is used to introduce bus interface of every module. These modules can divide into two types: bus master, slave. For example, CPU core and DMA is as bus master that can access corresponding register of every slave through bus. Every slave hangs in corresponding bus, the access path can be informed by the above diagram. Also Arbiter is bus arbiter that judge whether CPU core or DMA accesses AHB1 bus .

For example, CPU core accesses RTC module, the process is as follows:
(1).CPU instruction firstly passes AXIS1 bus, goes to AHB bus through X2H bridge, then accesses AHB1 bus through

Arbiter;
(2).AHB1 goes to APB1 bus through bus bridge;
(3).Finally RTC is operated based on relevant bus protocol .
The access time from CPU to RTC , is relevant with the CPU clock , AXIS1 bus clock, Arbiter rate, AHB1 bus clock, and APB1 bus clock. Any lower bus clock will lead to the access time very long.

The above blue area module indicates the interaction between module and DRAM, CPU core can access DRAM through AXIS2 bus, other modules(for example:GPU,SMHC,USB-HOST) also can interact directly with DRAM without using CPU.

The clocks of these modules(such as TWI and UART) to be hung on APB2 are from their respective bus clock , however the clocks of most other modules are from related CLK register , such as DE_CLK_REG. Each module clock requirement can refer to their module.

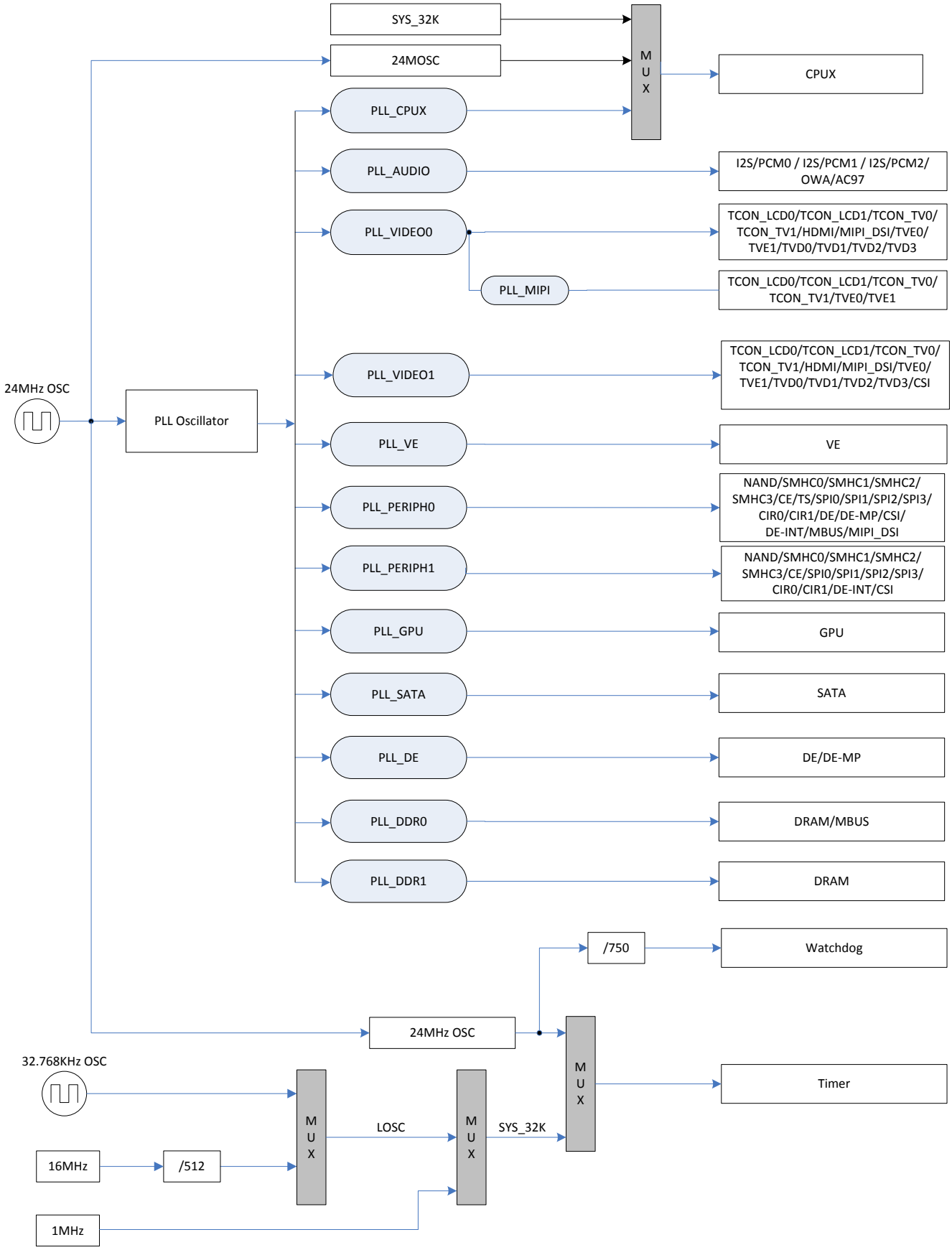


Figure 3-3. Module Clock Diagram

3.3.2.2. Typical Applications

PLL Applications: use the available clock sources to generate clock roots to various parts of the chip. In practical application, other PLLs don't support dynamic frequency scaling except for **PLL_CPUX** and **PLL_DDR1**.

Table 3-2. PLLs Typical Applications

PLLs	Typical Applications	Dynamic Frequency Scaling(DFS)
PLL_CPUX	CPU	Support
PLL_AUDIO	I2S/PCM0,I2S/PCM1,OWA,AC97	Not Support
PLL_VIDEO0(1X)	TCON,HDMI,MIPI_DSI,TVE,TVD	Not Support
PLL_VIDEO0(2X)	TCON ,TVE,TVD	Not Support
PLL_VIDEO1(1X)	TCON ,HDMI,MIPI_DSI,TVE,TVD,CSI	Not Support
PLL_VE	VE	Not Support
PLL_DDR0	MBUS,DRAM	Not Support
PLL_DDR1	DRAM	Support
PLL_PERIPH0(2X)	APB2/MBUS,DRAM,SMHC0,SMHC1,SMHC2,SMHC3,DE-MP,DE	Not Support
PLL_PERIPH0(1X)	AHB1,APB1,NAND,TS,SPI0,SPI1,SPI2,SPI3,CSI,MIPI_DSI, DEINTERLACE,CIR0,CIR1	Not Support
PLL_GPU	GPU	Not Support
PLL_MIPI	TCON,TVE	Not Support
PLL_SATA	SATA	Not Support
PLL_DE	DE	Not Support

3.3.2.3. PLL

(1) After the **PLL_DDR0** frequency changed, the **30**-bit of **PLL_DDR0 Control Register** should be written 1 to make it valid.

(2) After the **PLL_DDR1** frequency changed, the **30**-bit of **PLL_DDR1 Control Register** should be written 1 to make it valid.

(3) The user guide of **PLL Lock New Mode:**

(a). PLL_CPU from close to open:

Write 0 to the bit0 of **PLL_LOCK_CTRL_REG**.
Configure the parameters **(N,K,M,P)** of **PLL_CPU_CTRL_REG**.
Write 1 to the **Enable** bit of CPU PLL**PLL_CPU_CTRL_REG**.
Write 1 to the bit0 of **PLL_LOCK_CTRL_REG**.
Read the bit28 of **PLL_CPU_CTRL_REG**, when it is 1, then CPU PLL is locked.
Delay 20us.

(b). PLL_CPU frequency conversion:

Write 0 to the bit0 of **PLL_LOCK_CTRL_REG**.
Configure the parameters **(N,K,M,P)** of **PLL_CPU_CTRL_REG**.
Write 1 to the bit0 of **PLL_LOCK_CTRL_REG**.
Read the bit28 of **PLL_CPU_CTRL_REG**, when it is 1, then CPU PLL is locked.
Delay 20us.

(c). PLL_CPU from open to close:

Write 0 to the **Enable** bit of CPU PLL**PLL_CPU_CTRL_REG**
Write 0 to the bit0 of **PLL_LOCK_CTRL_REG**.

3.3.2.4. Bus

(1) When setting the **Bus Clock** , you should set the division factor first, and after the division factor available ,switch the clock source. The switching of clock source will be available after at least three clock cycles.
(2) The **Bus Clock** should not be dynamically changed in most applications.

3.3.2.5. Clock Switch

Make sure that the clock source output is valid before the clock source switch, and then set a proper divide ratio; after the division factor becomes valid, switch the clock source.

3.3.2.6. Reset and Gating

Make sure that the reset signal is released before the release of module clock gating.

3.3.2.7. Spread Spectrum Function

The configuration of spread spectrum follows the following steps.

Step1: Configure PLL_CTRL Register

- According to PLL frequency and PLL frequency formula f = [(N+1)/(M0+1)/(M1+1)+X] * 24MHz, suppose the value of divisor M0 and divisor M1, calculate factor N and decimal value X, and write M0、M1、N and PLL frequency to the PLL_CTRL register.
- Configure the SDM_Enable bit of the PLL_CTRL register to 1 to enable spread spectrum function.

NOTE

Having different PLL calculate formula for different PLL, please refer to each PLL_CTRL register.

Step 2: Configure PLL_PAT Register

- According to decimal value X and spread spectrum frequency(the bit[18:17] of the PLL_PAT register), calculate WAVE_BOT (= 2^{17} * X1) and WAVE_STEP (= 2^{17} * (X2-X1) / (24MHz/PREQ) * 2).
- Configure spread spectrum mode(SPR_FREQ_MODE) to 2 or 3.
- Configure the spread spectrum clock source select bit(SDM_CLK_SEL) to 0 by default. But if the PLL_INPUT_DIV_M1 bit of the PLL_CTRL register is 1, the bit should set to 1.
- Write WAVE_BOT、WAVE_STEP、PREQ、SPR_FREQ_MODE and SDM_CLK_SEL to the PLL_PAT register, and configure SIG_DELT_PAT_EN to 1.

Step 3: Delay 20us

3.3.3. Register List

Module Name	Base Address
CCU	0x01C20000

Register Name	Offset	Description
PLL_CPUX_CTRL_REG	0x0000	PLL_CPUX Control Register
PLL_AUDIO_CTRL_REG	0x0008	PLL_AUDIO Control Register
PLL_VIDEO0_CTRL_REG	0x0010	PLL_VIDEO0 Control Register

Register Name	Offset	Description
PLL_VE_CTRL_REG	0x0018	PLL_VE Control Register
PLL_DDR0_CTRL_REG	0x0020	PLL_DDR0 Control Register
PLL_PERIPH0_CTRL_REG	0x0028	PLL_PERIPH0 Control Register
PLL_PERIPH1_CTRL_REG	0x002C	PLL_PERIPH1 Control Register
PLL_VIDEO1_CTRL_REG	0x0030	PLL_VIDEO1 Control Register
PLL_SATA_CTRL_REG	0x0034	PLL_SATA Control Register
PLL_GPU_CTRL_REG	0x0038	PLL_GPU Control Register
PLL_MIPI_CTRL_REG	0x0040	PLL_MIPI Control Register
PLL_DE_CTRL_REG	0x0048	PLL_DE Control Register
PLL_DDR1_CTRL_REG	0x004C	PLL_DDR1 Control Register
CPU_AXI_CFG_REG	0x0050	CPUX/AXI Configuration Register
AHB1_APB1_CFG_REG	0x0054	AHB1/APB1 Configuration Register
APB2 _CFG_REG	0x0058	APB2 Configuration Register
BUS_CLK_GATING_REG0	0x0060	Bus Clock Gating Register 0
BUS_CLK_GATING_REG1	0x0064	Bus Clock Gating Register 1
BUS_CLK_GATING_REG2	0x0068	Bus Clock Gating Register 2
BUS_CLK_GATING_REG3	0x006C	Bus Clock Gating Register 3
BUS_CLK_GATING_REG4	0x0070	Bus Clock Gating Register 4
THS_CLK_REG	0x0074	THS Clock Register
NAND_CLK_REG	0x0080	NAND Clock Register
SDMMC0_CLK_REG	0x0088	SDMMC0 Clock Register
SDMMC1_CLK_REG	0x008C	SDMMC1 Clock Register
SDMMC2_CLK_REG	0x0090	SDMMC2 Clock Register
SDMMC3_CLK_REG	0x0094	SDMMC3 Clock Register
TS_CLK_REG	0x0098	TS Clock Register
CE_CLK_REG	0x009C	CE Clock Register
SPI0_CLK_REG	0x00A0	SPI0 Clock Register
SPI1_CLK_REG	0x00A4	SPI1 Clock Register
SPI2_CLK_REG	0x00A8	SPI2 Clock Register
SPI3_CLK_REG	0x00AC	SPI3 Clock Register
DAUDIO0_CLK_REG	0x00B0	DAUDIO0 Clock Register
DAUDIO1_CLK_REG	0x00B4	DAUDIO1 Clock Register
DAUDIO2_CLK_REG	0x00B8	DAUDIO2 Clock Register
AC97_CLK_REG	0x00BC	AC97 Clock Register
OWA_CLK_REG	0x00C0	OWA Clock Register
KEYPAD_CLK_REG	0x00C4	KEYPAD Clock Register
SATA_CLK_REG	0x00C8	SATA Clock Register
USBPHY_CFG_REG	0x00CC	USBPHY Configuration Register
CIR0_CLK_REG	0x00D0	CIR0 Clock Register
CIR1_CLK_REG	0x00D4	CIR1 Clock Register
PLL_DDR_AUX_REG	0x00F0	PLL_DDR Auxiliary Register
DRAM_CFG_REG	0x00F4	DRAM Configuration Register
PLL_DDR1_CFG_REG	0x00F8	PLL_DDR1 Configuration Register
MBUS_RST_REG	0x00FC	MBUS Reset Register
DRAM_CLK_GATING_REG	0x0100	DRAM Clock Gating Register
DE_CLK_REG	0x0104	DE Clock Register
DE_MP_CLK_REG	0x0108	DE_MP Clock Register
TCON_LCD0_CLK_REG	0x0110	TCON LCD0 Clock Register

Register Name	Offset	Description
TCON_LCD1_CLK_REG	0x0114	TCON LCD1 Clock Register
TCON_TV0_CLK_REG	0x0118	TCON TV0 Clock Register
TCON_TV1_CLK_REG	0x011C	TCON TV1 Clock Register
DEINTERLACE _CLK_REG	0x0124	DEINTERLACE Clock Register
CSI_MISC_CLK_REG	0x0130	CSI_MISC Clock Register
CSI_CLK_REG	0x0134	CSI Clock Register
VE_CLK_REG	0x013C	VE Clock Register
AC_DIG_CLK_REG	0x0140	AC Digital Clock Register
AVS_CLK_REG	0x0144	AVS Clock Register
HDMI_CLK_REG	0x0150	HDMI Clock Register
HDMI_SLOW_CLK_REG	0x0154	HDMI Slow Clock Register
MBUS_CLK_REG	0x015C	MBUS Clock Register
GMAC_CLK_REG	0x0164	GMAC Clock Register
MIPI_DSI_CLK_REG	0x0168	MIPI_DSI Clock Register
TVE0_CLK_REG	0x0180	TVE0 Clock Register
TVE1_CLK_REG	0x0184	TVE1 Clock Register
TVD0_CLK_REG	0x0188	TVD0 Clock Register
TVD1_CLK_REG	0x018C	TVD1 Clock Register
TVD2_CLK_REG	0x0190	TVD2 Clock Register
TVD3_CLK_REG	0x0194	TVD3 Clock Register
GPU_CLK_REG	0x01A0	GPU Clock Register
CLK_OUTA_REG	0x01F0	Clock Output A Register
CLK_OUTB_REG	0x01F4	Clock Output B Register
PLL_SATA_BIAS_REG	0x0218	PLL_SATA Bias Register
PLL_PERIPH1_BIAS_REG	0x021C	PLL_PERIPH1 Bias Register
PLL_CPUX_BIAS_REG	0x0220	PLL_CPUX Bias Register
PLL_AUDIO_BIAS_REG	0x0224	PLL_AUDIO Bias Register
PLL_VIDEO0_BIAS_REG	0x0228	PLL_VIDEO0 Bias Register
PLL_VE_BIAS_REG	0x022C	PLL_VE Bias Register
PLL_DDR0_BIAS_REG	0x0230	PLL_DDR0 Bias Register
PLL_PERIPH0_BIAS_REG	0x0234	PLL_PERIPH0 Bias Register
PLL_VIDEO1_BIAS_REG	0x0238	PLL_VIDEO1 Bias Register
PLL_GPU_BIAS_REG	0x023C	PLL_GPU Bias Register
PLL_DE_BIAS_REG	0x0248	PLL_DE Bias Register
PLL_DDR1_BIAS_REG	0x024C	PLL_DDR1 Bias Register
PLL_CPUX_TUN_REG	0x0250	PLL_CPUX Tuning Register
PLL_DDR0_TUN_REG	0x0260	PLL_DDR0 Tuning Register
PLL_PERIPH1_PAT_CTRL_REG	0x027C	PLL_PERIPH1 Pattern Control Register
PLL_CPUX_PAT_CTRL_REG	0x0280	PLL_CPUX Pattern Control Register
PLL_AUDIO_PAT_CTRL_REG	0x0284	PLL_AUDIO Pattern Control Register
PLL_VIDEO0_PAT_CTRL_REG	0x0288	PLL_VIDEO0 Pattern Control Register
PLL_VE_PAT_CTRL_REG	0x028C	PLL_VE Pattern Control Register
PLL_DDR0_PAT_CTRL_REG	0x0290	PLL_DDR0 Pattern Control Register
PLL_VIDEO1_PAT_CTRL_REG	0x0298	PLL_VIDEO1 Pattern Control Register
PLL_GPU_PAT_CTRL_REG	0x029C	PLL_GPU Pattern Control Register
PLL_DE_PAT_CTRL_REG	0x02A8	PLL_DE Pattern Control Register
PLL_DDR1_PAT_CTRL_REG0	0x02AC	PLL_DDR1 Pattern Control Register0
PLL_DDR1_PAT_CTRL_REG1	0x02B0	PLL_DDR1 Pattern Control Register1

Register Name	Offset	Description
BUS_SOFT_RST_REG0	0x02C0	Bus Software Reset Register 0
BUS_SOFT_RST_REG1	0x02C4	Bus Software Reset Register 1
BUS_SOFT_RST_REG2	0x02C8	Bus Software Reset Register 2
BUS_SOFT_RST_REG3	0x02D0	Bus Software Reset Register 3
BUS_SOFT_RST_REG4	0x02D8	Bus Software Reset Register 4
PS_CTRL_REG	0x0300	PS Control Register
PS_CNT_REG	0x0304	PS Counter Register
SYS_32K_CLK_REG	0x0310	System 32K Clock Control Register
INTOSC_CLK_AUTO_CALI_REG	0x0314	System Internal 32K Clock Auto Calibration Register
PLL_LOCK_CTRL_REG	0x0320	PLL Lock Control Register

3.3.4. Register Description

3.3.4.1. PLL_CPUX Control Register (Default Value: 0x0000_1000)

Offset: 0x0000			Register Name: PLL_CPUX_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL _CPUX = ((24MHz/K)*N)/(M*P). The PLL output is for the CPUX Clock. 10≤N*K≤88. 24MHz*N*K must be in the range of 240MHz~2.1GHz. The default value of PLL _CPUX is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	CPUX_SDM_EN. 0: Disable 1: Enable.
23:18	/	/	/
17:16	R/W	0x0	PLL_OUT_EXT_DIV_P PLL Output External Divider P 00: /1 01: /2 10: /4 11: /.
15:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32.

Offset: 0x0000			Register Name: PLL_CPUX_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K. (K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M. (M=Factor + 1) The range is from 1 to 4.

3.3.4.2. PLL_AUDIO Control Register (Default Value: 0x000_35514)

Offset: 0x0008			Register Name: PLL_AUDIO_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL is for Audio. The PLL_AUDIO= (24MHz*N)/(M*P). The PLL_AUDIO(8X) = (24MHz*N*2)/M 3≤N/M≤21. (24MHz*N)/P must be in the range of 72MHz~504MHz . PLL_AUDIO default is 24.571MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable. In this case, the only low 4 bits of **PLL_FACTOR_N** are valid (N: The range is from 1 to 16).
23:20	/	/	/
19:16	R/W	0x3	PLL_POSTDIV_P. Post-div factor (P= Factor+1) The range is from 1 to 16.
14:8	R/W	0x55	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 …… Factor=127, N=128.
7:5	/	/	/
4:0	R/W	0x14	PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 32.

3.3.4.3. PLL_VIDEO0 Control Register (Default Value: 0x0300_6207)

Offset: 0x0010			Register Name: PLL_VIDEO0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. In the integer mode, PLL_VIDEO0(1X) = (24MHz*N)/M. PLL_VIDEO0(2X) =((24MHz*N)/M)*2. In the fractional mode, the PLL Output is select by bit 25. 8≤N/M≤25 (24MHz*N)/M must be in the range of 192MHz~600MHz. PLL_VIDEO0(1X) default is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PREDIV_M** factor must be set to 0); No meaning when **PLL_MODE_SEL** =1. 0: PLL Output=270MHz 1: PLL Output =297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode. **NOTE** **When in Fractional mode, the Pre Divider M should be set to 0.**
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=127,N=128.
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 16.

3.3.4.4. PLL_VE Control Register (Default Value: 0x0300_6207)

Offset: 0x0018			Register Name: PLL_VE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. In the integer mode, The PLL_VE = (24MHz*N)/M. In the fractional mode, the PLL Output is select by **FRAC_CLK_OUT**. 8≤N/M≤25 (24MHz*N)/M must be in the range of 192MHz~600MHz. The default value of PLL_VE is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PREDIV_M** factor must be set to 0); No meaning when **PLL_MODE_SEL** =1. 0: PLL Output = 270MHz 1: PLL Output = 297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode. **NOTE** **When in Fractional mode, the Pre Divider M should be set to 0.**
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32 … Factor=127,N=128.
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 16.

3.3.4.5. PLL_DDR0 Control Register (Default Value: 0x0000_1000)

Offset: 0x0020			Register Name: PLL_DDR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL_DDR0 = (24MHz*N*K)/M. 10≤N*K≤77 (24MHz*N*K) must be in the range of 240MHz~1.8GHz. The default value of PLL_DDR0 is 408MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:25	/	/	/
24	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable.
23:21	/	/	/
20	R/W	0x0	PLL_DDR0_CFG_UPDATE. PLL_DDR0 Configuration Update. When PLL_DDR0 has been changed, this bit should be set to 1 to validate the PLL, otherwise the change would be invalid. And this bit would be cleared automatically after the PLL change is valid. 0: No effect 1: Validating the PLL_DDR0.
19:13	/	/	/
12:8	R/W	0x10	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32.
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4.

3.3.4.6. PLL_PERIPH0 Control Register (Default Value: 0x0004_1811)

Offset: 0x0028			Register Name: PLL_PERIPH0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE.

Offset: 0x0028			Register Name: PLL_PERIPH0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Disable 1: Enable. For SATA module, the output is: The PLL_PERIPH0 = 24MHz*N*K/(M*6). For other modules, the output is: The PLL_PERIPH0(1X) = 24MHz*N*K/2. The PLL_PERIPH0(2X) = 24MHz*N*K. 21≤N*K≤58 The PLL_PERIPH0(2X) should be fixed to 1.2GHz, it is not recommended to vary this value arbitrarily. 24MHz*N*K clock must be in the range of 504MHz~1.4GHz. The default value of PLL_PERIPH0(2X) is 1.2GHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x0	PLL_BYPASS_EN. PLL Output Bypass Enable. 0: Disable 1: Enable. If the bypass is enabled, the PLL output is 24MHz.
24	R/W	0x0	PLL_CLK_OUT_EN. PLL clock output enable.(Just for the SATA Phy) 0: Disable 1: Enable.
23:19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable. When 25MHz crystal used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32.
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/

Offset: 0x0028			Register Name: PLL_PERIPH0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x1	PLL_FACTOR_M. The range is from 1 to 4.

3.3.4.7. PLL_PERIPH1 Control Register (Default Value: 0x0004_1811)

Offset: 0x002C			Register Name: PLL_PERIPH1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL_PERIPH1(1X) = 24MHz*N*K/2. The PLL_PERIPH1(2X) = 24MHz*N*K. 21≤N*K≤58 PLL_PERIPH1(2X) should be fixed to 1.2GHz, it is not recommended to vary this value arbitrarily. 24MHz*N*K must be in the range of 504MHz~1.4GHz. The default value of PLL_PERIPH1(2X) is 1.2GHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x0	PLL_BYPASS_EN. PLL Output Bypass Enable. 0: Disable 1: Enable. If the bypass is enabled, the PLL output is 24MHz.
24	R/W	0x0	PLL_CLK_OUT_EN. PLL clock output enable.(Just for the SATA Phy) 0: Disable 1: Enable.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN 0: Disable 1: Enable.
19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz Output Enable. 0: Disable 1: Enable. When 25MHz crystal used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M Output Clock Post Divider (When 25MHz crystal used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N.

Offset: 0x002C			Register Name: PLL_PERIPH1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32.
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL_FACTOR_M. The range is from 1 to 4.

3.3.4.8. PLL_VIDEO1 Control Register (Default Value: 0x0300_6207)

Offset: 0x0030			Register Name: PLL_VIDEO1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. In the integer mode, PLL_VIDEO1(1X) = (24MHz*N)/M. PLL_VIDEO1(2X) =((24MHz*N)/M)*2. In the fractional mode, the PLL Output is selected by **FRAC_CLK_OUT**. 8≤N/M≤25 (24MHz*N)/M must be in the range of 192MHz~600MHz. The default value of PLL_VIDEO1(1X) is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PREDIV_M** factor must be set to 0); No meaning when **PLL_MODE_SEL** =1. 0: PLL Output=270MHz 1: PLL Output =297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode. **NOTE** **When in Fractional mode, the Per Divider M should be set to 0.**
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable

Offset: 0x0030			Register Name: PLL_VIDEO1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=127,N=128.
7:4	/	/	/
3:0	R/W	0x7	PLL_PREDIV_M. PLL Pre-div Factor(M = Factor+1). The range is from 1 to 16.

3.3.4.9. PLL_SATA Control Register (Default Value: 0x0000_1811)

Offset: 0x0034			Register Name: PLL_SATA_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL_SATA = 24MHz*N*K/(M*6). The PLL should be in the range of 8 MHz ~ 300 MHz. The default value is 100 MHz.
30	R/W	0x0	PLL_OUTPUT_SEL. 0: PLL output from SATA_PLL 1: PLL output from PLL_PERIPH0
29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:15	/	/	/
14	R/W	0x0	SATA_CLK_EN. SATA Clock Output Enable. 0: Disable 1: Enable.
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=31,N=32.
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/

Offset: 0x0034			Register Name: PLL_SATA_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W	0x1	PLL_FACTOR_M. (M=Factor + 1) The range is from 1 to 4.

3.3.4.10. PLL_GPU Control Register (Default Value: 0x0300_6207)

Offset: 0x0038			Register Name: PLL_GPU_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. In the integer mode, The PLL_GPU = (24MHz*N)/M. In the fractional mode, the PLL Output is selected by **FRAC_CLK_OUT**. 8≤N/M≤25 (24MHz*N)/M must be in the range of 192 MHz ~ 600 MHz. The default value of PLL_GPU is 297 MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PRE_DIV_M** factor must be set to 0); no meaning when **PLL_MODE_SEL** =1. 0: PLL Output=270MHz 1: PLL Output=297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode. 1: Integer Mode. **NOTE** **When in Fractional mode, the Per Divider M should be set to 0.**
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=127,N=128.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL Pre Divider (M = Factor+1). The range is from 1 to 16.

3.3.4.11. PLL_MIPI Control Register (Default Value: 0x0000_0515)

Offset: 0x0040			Register Name: PLL_MIPI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL_MIPI= (PLL_VIDEO0(1X)*N*K)/M when **VFB_SEL** =0 (MIPI mode). When VFB_SEL=1, the PLL Output is depend on these bits: sint_frac,sdiv2, s6p25_7p5 , pll_feedback_div.6 K≥2; M/N≤3; (PLL_VIDEO0)/M≥24MHz; PLL_MIPI must be in the range of 500 MHz ~ 1.4 GHz. The default value of PLL_MIPI is 594 MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27	R/W	0x0	SINT_FRAC. When **VFB_SEL** =1, PLL mode control, otherwise no meaning. 0: Integer Mode 1: Fractional Mode.
26	R/W	0x0	SDIV2. PLL clock output when **VFB_SEL** =1; no meaning when **VFB_SEL** =0 0: PLL Output 1: PLL Output X2.
25	R/W	0x0	S6P25_7P5. PLL Output is selected by this bit when **VFB_SEL** =1 and **SINT_FRAC** =1, otherwise no meaning. 0: PLL Output=PLL Input*6.25 1: PLL Output= PLL Input *7.5.
24	/	/	/
23	R/W	0x0	LDO1_EN. On-chip LDO1 Enable.
22	R/W	0x0	LDO2_EN. On-chip LDO2 Enable.
21	R/W	0x0	PLL_SRC. PLL Source Select. 0: VIDEO0 PLL 1: /.
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable.
19:18	/	/	/
17	R/W	0x0	PLL_FEEDBACK_DIV. PLL feed-back divider control. PLL clock output when **VFB_SEL** =1; no

Offset: 0x0040			Register Name: PLL_MIPI_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			meaning when **VFB_SEL** =0 0: Divided by 5 1: Divided by 7.
16	R/W	0x0	VFB_SEL. 0: MIPI Mode(N, K, M valid) 1: HDMI Mode(sint_frac,sdiv2,s6p25_7p5 , pll_feedback_div valid)
15:12	/	/	/
11:8	R/W	0x5	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 …… Factor=15,N=16;
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 2 to 4.
3:0	R/W	0x5	PLL_PRE_DIV_M. PLL Pre Divider (M = Factor+1). The range is from 1 to 16.

3.3.4.12. PLL_DE Control Register (Default Value: 0x0300_6207)

Offset: 0x0048			Register Name: PLL_DE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE 0: Disable 1: Enable. In the integer mode, The PLL_DE = (24MHz*N)/M. In the fractional mode, the PLL Output is selected by **FRAC_CLK_OUT**. 8≤N/M≤25 (24MHz*N)/M must be in the range of 192MHz~600MHz. The default value of PLL_DE is 297MHz.
30:29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT. PLL clock output when **PLL_MODE_SEL** =0(**PLL_PRE_DIV_M** factor must be set to 0); no meaning when **PLL_MODE_SEL** =1. 0: PLL Output=270MHz 1: PLL Output =297MHz.
24	R/W	0x1	PLL_MODE_SEL. 0: Fractional Mode 1: Integer Mode.

Offset: 0x0048			Register Name: PLL_DE_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			NOTE **When in Fractional mode, the Pre Divider M should be set to 0.**
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1 Factor=1, N=2 Factor=2, N=3 …… Factor=0x7F,N=128.
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL Per Divider (M = Factor+1). The range is from 1 to 16.

3.3.4.13. PLL_DDR1 Control Register (Default Value: 0x0000_1800)

Offset: 0x004C			Register Name: PLL_DDR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_ENABLE. 0: Disable 1: Enable. The PLL_DDR1 = 24MHz*N/M. 16≤N≤75. 24MHz*N/M must be in the range of 192 MHz ~ 1.6 GHz. Its default value is 600 MHz.
30	R/W	0x0	SDRPLL_UPD. SDRPLL Configuration Update. **NOTE** **When PLL_DDR1 has changed, this bit should be set to 1 to validate the PLL, otherwise the change is invalid. It will be automatically cleared after the PLL is valid.** 0: No effect 1: To validate the PLL_DDR1.
29	/	/	/
28	R	0x0	LOCK 0: Unlocked 1: Locked (It indicates that the PLL has been stable.)
27:16	/	/	/
15	R/W	0x0	N_MODE

Offset: 0x004C			Register Name: PLL_DDR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: New mode 1: Original mode If new mode, avoid config N=0 mistake.
14:8	R/W	0x18	PLL_FACTOR_N. N= Factor +1. The range is from 0 to 127
7:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. M= Factor +1. The range is from 0 to 4

3.3.4.14. CPUX/AXI Configuration Register (Default Value: 0x0001_0300)

Offset: 0x0050			Register Name: CPU_AXI_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x1	CPUX_CLK_SRC_SEL. CPUX Clock Source Select. CPUX Clock = Clock Source 00: LOSC 01: OSC24M 1X: PLL_CPUX If the clock source is changed, there need to wait for 8 present running clock cycles at most.
15:2	/	/	/
1:0	R/W	0x0	AXI_CLK_DIV_RATIO. AXI Clock Divide Ratio. AXI Clock source is CPU clock source. 00: /1 01: /2 10: /3 11: /4.

3.3.4.15. AHB1/APB1 Configuration Register (Default Value: 0x0000_1010)

Offset: 0x0054			Register Name: AHB1_APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x1	AHB1_CLK_SRC_SEL. 00: LOSC 01: OSC24M 10: AXI 11: PLL_PERIPH0(1X)/AHB1_PRE_DIV.
11:10	/	/	/
9:8	R/W	0x0	APB1_CLK_RATIO. APB1 Clock Divide Ratio. APB1 clock source is AHB1 clock.

Offset: 0x0054			Register Name: AHB1_APB1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			00: /2 01: /2 10: /4 11: /8.
7:6	R/W	0x0	AHB1_PRE_DIV AHB1 Clock Pre Divide Ratio 00: /1 01: /2 10: /3 11: /4.
5:4	R/W	0x1	AHB1_CLK_DIV_RATIO. AHB1 Clock Divide Ratio. 00: /1 01: /2 10: /4 11: /8.
3:0	/	/	/

3.3.4.16. APB2 Configuration Register (Default Value: 0x0100_0000)

Offset: 0x0058			Register Name: APB2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x1	APB2_CLK_SRC_SEL. APB2 Clock Source Select 00: LOSC 01: OSC24M 1X: PLL_PERIPH0(2X). This clock is used for some special module apbclk(UART, TWI, PS2). Because these modules need special clock rate even if the apb1clk changed.
23:18	/	/	/
17:16	R/W	0x0	CLK_RAT_N Clock Per Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:5	/	/	/
4:0	R/W	0x0	CLK_RAT_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

3.3.4.17. Bus Clock Gating Register 0 (Default Value: 0x0000_0000)

Offset: 0x0060	Register Name: BUS_CLK_GATING_REG0

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	USBOHCI2_GATING. Gating Clock for USB OHCI1 0: Mask 1: Pass
30	R/W	0x0	USBOHCI1_GATING. Gating Clock for USB OHCI1 0: Mask 1: Pass
29	R/W	0x0	USBOHCI0_GATING. Gating Clock for USB OHCI0 0: Mask 1: Pass
28	R/W	0x0	USBEHCI2_GATING. Gating Clock for USB EHCI1 0: Mask 1: Pass
27	R/W	0x0	USBEHCI1_GATING. Gating Clock for USB EHCI1 0: Mask 1: Pass
26	R/W	0x0	USBEHCI0_GATING. Gating Clock for USB EHCI0 0: Mask 1: Pass
25	R/W	0x0	USBOTG_GATING. Gating Clock for USB OTG 0: Mask 1: Pass
24	R/W	0x0	SATA_GATING. Gating Clock for SATA 0: Mask 1: Pass.
23	R/W	0x0	SPI3_GATING. Gating Clock for SPI3 0: Mask 1: Pass.
22	R/W	0x0	SPI2_GATING. Gating Clock for SPI2 0: Mask 1: Pass.
21	R/W	0x0	SPI1_GATING. Gating Clock for SPI1 0: Mask 1: Pass.

Offset: 0x0060			Register Name: BUS_CLK_GATING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
20	R/W	0x0	SPI0_GATING. Gating Clock for SPI0 0: Mask 1: Pass.
19	R/W	0x0	HSTMR_GATING. Gating Clock for High Speed Timer 0: Mask 1: Pass.
18	R/W	0x0	TS_GATING. Gating Clock for TS 0: Mask 1: Pass
17	R/W	0x0	EMAC_GATING. Gating Clock for EMAC 0: Mask 1: Pass
16:15	/	/	/
14	R/W	0x0	DRAM_GATING. Gating Clock for DRAM 0: Mask 1: Pass.
13	R/W	0x0	NAND_GATING. Gating Clock for NAND 0: Mask 1: Pass.
12	/	/	/
11	R/W	0x0	SMHC3_GATING. Gating Clock for SMHC3 0: Mask 1: Pass.
10	R/W	0x0	SMHC2_GATING. Gating Clock for SMHC2 0: Mask 1: Pass.
9	R/W	0x0	SMHC1_GATING. Gating Clock for SMHC1 0: Mask 1: Pass.
8	R/W	0x0	SMHC0_GATING. Gating Clock for SMHC0 0: Mask 1: Pass.
7	/	/	/
6	R/W	0x0	DMA_GATING.

Offset: 0x0060			Register Name: BUS_CLK_GATING_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			Gating Clock for DMA 0: Mask 1: Pass.
5	R/W	0x0	CE_GATING. Gating Clock for CE 0: Mask 1: Pass.
4:2	/	/	/
1	R/W	0x0	MIPIDSI_GATING Gating Clock for MIPI DSI 0: Mask 1: Pass
0	/	/	/

3.3.4.18. Bus Clock Gating Register 1 (Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: BUS_CLK_GATING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TCON_TOP_GATING 0: Mask 1: Pass
29	R/W	0x0	TCON_TV1_GATING 0: Mask 1: Pass
28	R/W	0x0	TCON_TV0_GATING 0: Mask 1: Pass
27	R/W	0x0	TCON_LCD1_GATING 0: Mask 1: Pass
26	R/W	0x0	TCON_LCD0_GATING 0: Mask 1: Pass
25	R/W	0x0	TVD_TOP_GATING 0:Mask 1:Pass
24	R/W	0x0	TVD3_GATING 0: Mask 1: Pass
23	R/W	0x0	TVD2_GATING

Offset: 0x0064			Register Name: BUS_CLK_GATING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Mask 1: Pass
22	R/W	0x0	TVD1_GATING 0: Mask 1: Pass
21	R/W	0x0	TVD0_GATING 0: Mask 1: Pass
20	R/W	0x0	GPU_GATING. Gating Clock for GPU 0: Mask 1: Pass.
19:18	/	/	/
17	R/W	0x0	GMAC_GATING. Gating Clock for GMAC 0: Mask 1: Pass.
16	/	/	/
15	R/W	0x0	TVE_TOP_GATING 0: Mask 1: Pass
14	R/W	0x0	TVE1_GATING 0: Mask 1: Pass
13	R/W	0x0	TVE0_GATING 0: Mask 1: Pass
12	R/W	0x0	DE_GATING. Gating Clock For DE 0: Mask 1: Pass.
11	R/W	0x0	HDMI1_GATING. 0: Mask 1: Pass.
10	R/W	0x0	HDMI0_GATING. 0: Mask 1: Pass.
9	R/W	0x0	CSI1_GATING. Gating Clock for CSI1 0: Mask 1: Pass.
8	R/W	0x0	CSI0_GATING. Gating Clock for CSI0

Offset: 0x0064			Register Name: BUS_CLK_GATING_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Mask 1: Pass.
7:6	/	/	/
5	R/W	0x0	DI_GATING. Gating Clock for DEINTERLACE 0: Mask 1: Pass
4:3	/	/	/
2	R/W	0x0	MP_GATING Gating Clock for MP 0: Mask 1: Pass
1	/	/	/
0	R/W	0x0	VE_GATING. Gating Clock for VE 0: Mask 1: Pass.

3.3.4.19. Bus Clock Gating Register 2 (Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: BUS_CLK_GATING_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	I2S/PCM2_GATING. Gating Clock for I2S/PCM2 0: Mask 1: Pass.
13	R/W	0x0	I2S/PCM1_GATING. Gating Clock for I2S/PCM1 0: Mask 1: Pass.
12	R/W	0x0	I2S/PCM0_GATING. Gating Clock for I2S/PCM0 0: Mask 1: Pass.
11	/	/	/
10	R/W	0x0	KEYPAD_GATING. Gating Clock for KEYPAD 0: Mask 1: Pass.
9	/	/	/
8	R/W	0x0	THS_GATING. Gating Clock for THS

Offset: 0x0068			Register Name: BUS_CLK_GATING_REG2
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Mask 1: Pass
7	R/W	0x0	CIR1_GATING. Gating Clock for CIR1 0: Mask 1: Pass
6	R/W	0x0	CIR0_GATING. Gating Clock for CIR0 0: Mask 1: Pass
5	R/W	0x0	PIO_GATING. Gating Clock for PIO 0: Mask 1: Pass.
4:3	/	/	/
2	R/W	0x0	AC97_GATING. Gating Clock for AC97 0: Mask 1: Pass
1	R/W	0x0	OWA_GATING. Gating Clock for OWA 0: Mask 1: Pass
0	R/W	0x0	AC_DIG_GATING. Gating Clock for AC Digital 0: Mask 1: Pass

3.3.4.20. Bus Clock Gating Register 3 (Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: BUS_CLK_GATING_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/.
23	R/W	0x0	UART7_GATING. Gating Clock for UART7 0: Mask 1: Pass.
22	R/W	0x0	UART6_GATING. Gating Clock for UART6 0: Mask 1: Pass.
21	R/W	0x0	UART5_GATING. Gating Clock for UART5

Offset: 0x006C			Register Name: BUS_CLK_GATING_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Mask 1: Pass.
20	R/W	0x0	UART4_GATING. Gating Clock for UART4 0: Mask 1: Pass.
19	R/W	0x0	UART3_GATING. Gating Clock for UART3 0: Mask 1: Pass.
18	R/W	0x0	UART2_GATING. Gating Clock for UART2 0: Mask 1: Pass.
17	R/W	0x0	UART1_GATING. Gating Clock for UART1 0: Mask 1: Pass.
16	R/W	0x0	UART0_GATING. Gating Clock for UART0 0: Mask 1: Pass.
15	R/W	0x0	TWI4_GATING. Gating Clock for TWI4 0: Mask 1: Pass.
14:8	/	/	/
7	R/W	0x0	PS2_1_GATING. Gating Clock for PS2_1 0: Mask 1: Pass
6	R/W	0x0	PS2_0_GATING. Gating Clock for PS2_0 0: Mask 1: Pass
5	R/W	0x0	SCR_GATING. Gating Clock for SCR 0: Mask 1: Pass
4	R/W	0x0	Reserved
3	R/W	0x0	TWI3_GATING. Gating Clock for TWI3 0: Mask 1: Pass.

Offset: 0x006C			Register Name: BUS_CLK_GATING_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
2	R/W	0x0	TWI2_GATING. Gating Clock for TWI2 0: Mask 1: Pass.
1	R/W	0x0	TWI1_GATING. Gating Clock for TWI1 0: Mask 1: Pass.
0	R/W	0x0	TWI0_GATING. Gating Clock for TWI0 0: Mask 1: Pass.

3.3.4.21. Bus Clock Gating Register 4 (Default Value: 0x0000_0000)

Offset: 0x0070			Register Name: BUS_CLK_GATING_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DBGSYS_GATING. Gating Clock for DBGSYS 0: Mask 1: Pass
6:0	/	/	/

3.3.4.22. THS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: THS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock. 0: Clock is OFF 1: Clock is ON This special clock = **THS_CLK_SRC_SEL** / **THS_CLK_DIV_RATIO**.
30:26	/	/	/
25:24	R/W	0x0	THS_CLK_SRC_SEL. Clock Source Select 00: OSC24M Others: /
23:2	/	/	/
1:0	R/W	0x0	THS_CLK_DIV_RATIO. THS clock divide ratio. 00: /1 01: /2

Offset: 0x0074			Register Name: THS_CLK_REG
Bit	Read/Write	Default/Hex	Description
			10: /4 11: /8

3.3.4.23. NAND Clock Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: NAND_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

3.3.4.24. SMHC0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SDMMC0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X)

Offset: 0x0088			Register Name: SDMMC0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			10: PLL_PERIPH1(2X) 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.25. SMHC1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.26. SMHC2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0090			Register Name: SMHC2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.27. SMHC3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: SMHC3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4

Offset: 0x0094			Register Name: SMHC3_CLK_REG
Bit	Read/Write	Default/Hex	Description
			11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.28. TS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating of SCLK (Max Clock = 200MHz). 0: Clock is OFF 1: Clock is ON SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:28	/	/	/
27:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 0000: OSC24M 0001: PLL_PERIPH0(1X) Others: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.29. CE Clock Register (Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: CE_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 400MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_PERIPH1(2X) 11: /

Offset: 0x009C			Register Name: CE_CLK_REG
Bit	Read/Write	Default/Hex	Description
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.30. SPI0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: SPI0_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON. SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.31. SPI1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: SPI1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz)

Offset: 0x00A4			Register Name: SPI1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Clock is OFF 1: Clock is ON SCLK= **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.32. SPI2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: SPI2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON SCLK= **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8.
15:4	/	/	/

Offset: 0x00A8			Register Name: SPI2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.33. SPI3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: SPI3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON SCLK= **CLK_SRC_SEL** / **CLK_DIV_RATIO_N** / **CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (n) 00: /1 01: /2 10: /4 11: /8
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.34. I2S/PCM0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: I2S/PCM0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO (8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4

Offset: 0x00B0			Register Name: I2S/PCM0_CLK_REG
Bit	Read/Write	Default/Hex	Description
			11: PLL_AUDIO.
15:0	/	/	/.

3.3.4.35. I2S/PCM1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: I2S/PCM1_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO(8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO.
15:0	/	/	/.

3.3.4.36. I2S/PCM2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: I2S/PCM2_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON.
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO (8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO.
15:0	/	/	/.

3.3.4.37. AC97 Clock Register(Default Value: 0x0003_0000)

Offset: 0x00BC			Register Name: AC97_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF

Offset: 0x00BC			Register Name: AC97_CLK_REG
Bit	Read/Write	Default/Hex	Description
			1: Clock is ON
30:28	/	/	/
17:16	R/W	0x3	CLK_SRC_SEL. 00: PLL_AUDIO(8x) 01: PLL_AUDIO(4X) 10: PLL_AUDIO(2X) 11: PLL_AUDIO(1X)
15:0	/	/	/

3.3.4.38. OWA Clock Register (Default Value: 0x0001_0000)

Offset: 0x00C0			Register Name: OWA_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x1	CLK_SRC_SEL. 00: PLL_AUDIO(8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO.
15:0	/	/	/

3.3.4.39. KEYPAD Clock Register (Default Value: 0x0000_001F)

Offset: 0x00C4			Register Name: KEYPAD_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON This special clock = **CLK_SRC_SEL** / **CLK_RATIO_N** / **CLK_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: / 10: LOSC 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.

Offset: 0x00C4			Register Name: KEYPAD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:5	/	/	/.
4:0	R/W	0x1f	CLK_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

3.3.4.40. SATA Clock Register (Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: SATA_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON
30:25	/	/	/
24	R/W	0x0	CLK_SRC_GATING. Clock Source Select 0: PLL_SATA for SATA(100MHz) 1: External Clock
23:0	/	/	/

3.3.4.41. USBPHY Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: USBPHY_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	OHCI2_12M_SRC_SEL. OHCI2 12M Source Select 00: 12M divided from 48M 01: 12M divided from 24M 10: LOSC 11: /
23:22	R/W	0x0	OHCI1_12M_SRC_SEL. OHCI1 12M Source Select 00: 12M divided from 48M 01: 12M divided from 24M 10: LOSC 11: /
21:20	R/W	0x0	OHCI0_12M_SRC_SEL. OHCI0 12M Source Select 00: 12M divided from 48M 01: 12M divided from 24M 10: LOSC 11: /
19	/	/	/
18	R/W	0x0	SCLK_GATING_OHCI2.

Offset: 0x00CC			Register Name: USBPHY_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Gating Special Clock for OHCI2(48M and 12M) 0: Clock is OFF 1: Clock is ON
17	R/W	0x0	SCLK_GATING_OHCI1. Gating Special Clock for OHCI1(48M and 12M) 0: Clock is OFF 1: Clock is ON
16	R/W	0x0	SCLK_GATING_OHCI0. Gating Special Clock for OHCI0(48M and 12M) 0: Clock is OFF 1: Clock is ON
15:11	/	/	/
10	R/W	0x0	SCLK_GATING_USBPHY2. Gating Special Clock for USB PHY2 0: Clock is OFF 1: Clock is ON
9	R/W	0x0	SCLK_GATING_USBPHY1. Gating Special Clock for USB PHY1 0: Clock is OFF 1: Clock is ON
8	R/W	0x0	SCLK_GATING_USBPHY0. Gating Special Clock for USB PHY0 0: Clock is OFF 1: Clock is ON
7:3	/	/	/
2	R/W	0x0	USBPHY2_RST. USB PHY2 Reset Control 0: Assert 1: De-assert
1	R/W	0x0	USBPHY1_RST. USB PHY1 Reset Control 0: Assert 1: De-assert
0	R/W	0x0	USBPHY0_RST. USB PHY0 Reset Control 0: Assert 1: De-assert

3.3.4.42. CIR0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: CIR0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING.

Offset: 0x00D0			Register Name: CIR0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON The special clock = **CLK_SRC_SEL/CLK_DIV_RATIO_N/CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: LOSC.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.43. CIR1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: CIR1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON The special clock = **CLK_SRC_SEL/CLK_DIV_RATIO_N/CLK_DIV_RATIO_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH0(1X) 10: PLL_PERIPH1(1X) 11: LOSC.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.44. PLL_DDR Auxiliary Register (Default Value: 0x0000_0001)

Offset: 0x00F0			Register Name: PLL_DDR_AUX_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R/W	0x0	PLL_DDR1_CLK_OPTION. 0: 24M_SYS 1: 24M_PLL_DDR1
3:1	/	/	/
0	R/W	0x1	PLL_DDR1_RST. PLL DDR1 reset 0: Assert 1: De-assert

3.3.4.45. DRAM Configuration Register (Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: DRAM_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DRAM_CTR_RST. DRAM Controller Reset for S_CLK Domain. 0: Assert 1: De-assert.
30:22	/	/	/
21:20	R/W	0x0	DDR_SRC_SELECT. 00: PLL_DDR0 01: PLL_DDR1 1X: /.
19:17	/	/	/
16	R/W	0x0	SDRCLK_UPD. SDRCLK Configuration 0 Update. The DRAMCLK Source is from PLL_DDR. 0: Invalid 1: Valid. **NOTE** **Setting this bit will validate Configuration 0. It will be automatically cleared after the Configuration 0 is valid.**
15:2	/	/	/
1:0	R/W	0x0	DRAM_DIV_M. DRAMCLK Divider of Configuration. The clock is divided by (m+1). The divider should be from 1 to 4.

3.3.4.46. PLL_DDR1 Configuration Register (Default Value: 0x0CCC_A000)

Offset: 0x00F8			Register Name: PLL_DDR1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	PLL_DDR1_MODE.

Offset: 0x00F8			Register Name: PLL_DDR1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Normal Mode 1: Continuously Frequency Scale
30:29	/	/	/
28:12	R/W	0xCCCA	PLL_SSC The amplitude of **SSC** must be the integer times of (2^**STEP**). Spread Frequency Amplitude =(**SSC** Amplitude +2^**STEP**)*24/(2^17),the unit is MHz
11:7	/	/	/
6:4	R/W	0x0	PLL_DDR1_PHASE_COMPENSATE. The value of bit[6:4] is based on 24M clock, then the default PLL_DDR phase compensate is (3/24000000) s.
3:0	R/W	0x0	PLL_DDR1_STEP. 0000: 0.00439MHz/us (576/2^17) 0001: 0.00879MHz/us (576/2^16) 0010: 0.01758MHz/us (576/2^15) 0011: 0.03516MHz/us (576/2^14) 0100: 0.07031MHz/us (576/2^13) 0101: 0.14062MHz/us (576/2^12) 0110: 0.28125MHz/us (576/2^11) 0111: 0.56250MHz/us (576/2^10) 1000: 1.12500MHz/us (576/2^9) 1001: 2.25000MHz/us (576/2^8) 1010: 4.50000Mhz/us (576/2^7) 1011: 9.00000Mhz/us (576/2^6) Others: 0.00439MHz/us (576/2^17)

3.3.4.47. MBUS Reset Register (Default Value: 0x8000_0000)

Offset: 0x00FC			Register Name: MBUS_RST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MBUS_RESET. 0: Assert 1: De-assert.
30:0	/	/	/

3.3.4.48. DRAM Clock Gating Register (Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: DRAM_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0X0	DI_DCLK_GATING Gating DRAM for DE-INTERLACE 0: Mask 1: Pass
5	R/W	0x0	MP_DCLK_GATING. Gating DRAM for MP

Offset: 0x0100			Register Name: DRAM_CLK_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Mask 1: Pass
4	R/W	0x0	TVD_DCLK_GATING. Gating DRAM for TVD 0: Mask 1: Pass
3	R/W	0x0	TS_DCLK_GATING. Gating DRAM for TS 0: Mask 1: Pass
2	R/W	0x0	CSI1_DCLK_GATING. Gating DRAM Clock for CSI1 0: Mask 1: Pass.
1	R/W	0x0	CSI0_DCLK_GATING. Gating DRAM Clock for CSI0 0: Mask 1: Pass.
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM Clock for VE 0: Mask 1: Pass.

3.3.4.49. DE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: DE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_PERIPH0(2X) 001: PLL_DE Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.50. DE_MP Clock Register (Default Value: 0x0000_0000)

Offset: 0x0108			Register Name: DE_MP_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = **CLK_SRC_SEL** /**CLK_DIV_RATIO_M**.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_PERIPH0(2X) 001: PLL_DE Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.51. TCON0 LCD Clock Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: TCON0_LCD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON.
30:26	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others: /
23:0	/	/	/

3.3.4.52. TCON1 LCD Clock Register (Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: TCON1_LCD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON.

Offset: 0x0114			Register Name: TCON1_LCD_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
30:26	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others: /
23:0	/	/	/

3.3.4.53. TCON0 TV Clock Register (Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: TCON0_TV_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. TV0 clock = **CLK_SRC_SEL** /**CLK_DIV_RATIO_M**.
30:26	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.54. TCON1 TV Clock Register (Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: TCON1_TV_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. TV1 clock = **CLK_SRC_SEL** /**CLK_DIV_RATIO_M**.
30:26	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select

Offset: 0x011C			Register Name: TCON1_TV_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.55. DEINTERLACE Clock Register (Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: DEINTERLACE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK = **CLK_SRC_SEL** / **CLK_DIV_RATIO_M**
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_PERIPH0(1X) 001: PLL_PERIPH1(1X) Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.56. CSI_MISC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: CSI_MCLK_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	CSI_MCLK1_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON. SCLK =**MCLK1_SRC_SEL** / **CSI_MCLK1_DIV_M**.
14:11	/	/	/
10:8	R/W	0x0	MCLK1_SRC_SEL. Master Clock Source Select 000: OSC24M

Offset: 0x0130			Register Name: CSI_MCLK_CLK_REG
Bit	Read/Write	Default/Hex	Description
			001: PLL_VIDEO1(1X) 010: PLL_PERIPH1(1X) Others: /
7:5	/	/	/
4:0	R/W	0x0	CSI_MCLK1_DIV_M. CSI Master Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

3.3.4.57. CSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: CSI_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	CSI_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = **SCLK_SRC_SEL** /**CSI_SCLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	SCLK_SRC_SEL. Special Clock Source Select 000: PLL_PERIPH0(1X) 001: PLL_PERIPH1(1X) Others: /.
23:20	/	/	/
19:16	R/W	0x0	CSI_SCLK_DIV_M. CSI Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
15	R/W	0x0	CSI_MCLK0_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON. SCLK =**MCLK0_SRC_SEL** / **CSI_MCLK0_DIV_M**.
14:11	/	/	/
10:8	R/W	0x0	MCLK0_SRC_SEL. Master Clock Source Select 000: OSC24M 001: PLL_VIDEO1(1X) 010: PLL_PERIPH1(1X) Others: /
7:5	/	/	/
4:0	R/W	0x0	CSI_MCLK0_DIV_M. CSI Master Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

3.3.4.58. VE Clock Register (Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: VE_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VE_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = PLL_VE /**CLK_DIV_RATIO_N**.
30:19	/	/	/.
18:16	R/W	0x0	CLK_DIV_RATIO_N. Clock Pre Divide Ratio (N) The select clock source is pre-divided by n+1. The divider is from 1 to 8.
15:0	/	/	/

3.3.4.59. Audio Codec Clock Register(Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: AUDIO_CODEC_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_1X_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK = 1X Clock Output.
30:0	/	/	/

3.3.4.60. AVS Clock Register (Default Value: 0x0000_0000)

Offset: 0x0144			Register Name: AVS_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON. SCLK= OSC24M.
30:0	/	/	/

3.3.4.61. HDMI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0150			Register Name: HDMI_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON SCLK= **SCLK_SEL** / **CLK_DIV_RATIO_M**.

Offset: 0x0150			Register Name: HDMI_CLK_REG
Bit	Read/Write	Default/Hex	Description
30:26	/	/	/
25:24	R/W	0x0	SCLK_SEL. Special Clock Source Select 00: PLL_VIDEO0(1X) 01: PLL_VIDEO1(1X) Others: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock Divide Ratio (m) The pre-divided clock is divided by (m+1). The divider M is from 1 to 16.

3.3.4.62. HDMI Slow Clock Register (Default Value: 0x0000_0000)

Offset: 0x0154			Register Name: HDMI_SLOW_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HDMI_DDC_CLK_GATING. 0: Clock is OFF 1: Clock is ON SCLK = OSC24M.
30:0	/	/	/

3.3.4.63. MBUS Clock Register (Default Value: 0x0000_0000)

Offset: 0x015C			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS 0: Clock is OFF 1: Clock is ON. MBUS_CLOCK = **MBUS_SCLK_SRC** / **MBUS_SCLK_RATIO_M**
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select 00: OSC24M 01: PLL_PERIPH0(2X) 10: PLL_DDR0 11: /.
23:18	/	/	/
17:16	R/W	0x0	MBUS_SCLK_RATIO_N Clock Pre-divide Ratio (N) The select clock source is pre-divided by 2^N. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (M) The divided clock is divided by (M+1). The divider is from 1 to 16. The divide ratio must be changed smoothly.

Offset: 0x015C			Register Name: MBUS_CLK_REG
Bit	Read/Write	Default/Hex	Description
			NOTE **If the clock has been changed ,it must wait for at least 16 cycles.**

3.3.4.64. GMAC Clock Register (Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: GMAC_CLK_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	TXC_DIV_CFG Clock pre-divide ratio(n) External transmit clock (125 MHz) is pre-divided by as follows for RGMII. 00: /1,generate 125 MHz 01: /5,generate 25 MHz 10: /50,generate 2.5 MHz 11: Reserved
7:5	R/W	0x0	GRXDC Configure GMAC Receive Clock Delay Chian. 000: 001: … 111:
4	R/W	0x0	GRXIE Enable GMAC Receive Clock Invertor. 0: Disable 1: Enable
3	R/W	0x0	GTXIE Enable GMAC Transmit Clock Invertor. 0: Disable 1: Enable
2	R/W	0x0	GPIT GMAC PHY Interface Type 0: MII 1: RGMII
1:0	R/W	0x0	GTCS GMAC Transmit Clock Source 00: Transmit clock source for MII 01: External transmit clock source(125 MHz) for RGMII 10: Internal transmit clock source for RGMII 11: Reserved

3.3.4.65. MIPI_DSI Clock Register (Default Value: 0x0000_0000)

Offset: 0x0168	Register Name: MIPI_DSI_CLK_REG

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	DSI_DPHY_GATING. Gating DSI DPHY Clock 0: Clock is OFF 1: Clock is ON. This DSI DPHY clock = **Clock Source** / **DPHY_CLK_DIV_M**.
14:10	/	/	/
9:8	R/W	0x0	DSI_DPHY_SRC_SEL. DSI DPHY Clock Source Select. 00: PLL_VIDEO0(1X) 01: PLL_VIDEO1(1X) 10: PLL_PERIPH0(1X) 11: /
7:4	/	/	/
3:0	R/W	0x0	DPHY_CLK_DIV_M. DSI DPHY Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.66. TVE0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: TVE0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TVE0_GATING. Gating TVE0 Clock 0: Clock is OFF 1: Clock is ON. This TVE0 clock = **Clock Source**/**TVE0_CLK_DIV_M**
30:27	/	/	/
26:24	R/W	0x0	TVE0_SRC_SEL. TVE0 Clock Source Select. 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others: /
23:4	/	/	/
3:0	R/W	0x0	TVE0_CLK_DIV_M. TVE0 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.67. TVE1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: TVE1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TVE1_GATING. Gating TVE0 Clock

Offset: 0x0184			Register Name: TVE1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Clock is OFF 1: Clock is ON. This TVE1 clock = **Clock Source** /**TVE1_CLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	TVE1_SRC_SEL. TVE1 Clock Source Select. 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) 100: PLL_MIPI Others: /
23:4	/	/	/
3:0	R/W	0x0	TVE1_CLK_DIV_M. TVE1 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.68. TVD0 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: TVD0_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TVD0_GATING. Gating TVD0 Clock 0: Clock is OFF 1: Clock is ON. This TVD0 clock = **Clock Source**/**TVD0_CLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	TVD0_SRC_SEL. TVD0 Clock Source Select. 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) Others: /
23:4	/	/	/.
3:0	R/W	0x0	TVD0_CLK_DIV_M. TVE0 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.69. TVD1 Clock Register (Default Value: 0x0000_0000)

Offset: 0x018C			Register Name: TVD1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TVD1_GATING. Gating TVD0 Clock

Offset: 0x018C			Register Name: TVD1_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Clock is OFF 1: Clock is ON. This TVD1 clock = **Clock Source**/**TVD1_CLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	TVD1_SRC_SEL. TVD1 Clock Source Select. 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) Others: /
23:4	/	/	/.
3:0	R/W	0x0	TVD1_CLK_DIV_M. TVE1 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.70. TVD2 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: TVD2_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TVD2_GATING. Gating TVD0 Clock 0: Clock is OFF 1: Clock is ON. This TVD2 clock = **Clock Source**/**TVD2_CLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	TVD2_SRC_SEL. TVD2 Clock Source Select. 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) Others: /
23:4	/	/	/.
3:0	R/W	0x0	TVD2_CLK_DIV_M. TVE2 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.71. TVD3 Clock Register (Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: TVD3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TVD3_GATING. Gating TVD0 Clock 0: Clock is OFF 1: Clock is ON.

Offset: 0x0194			Register Name: TVD3_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			This TVD3 clock = **Clock Source** /**TVD3_CLK_DIV_M**.
30:27	/	/	/
26:24	R/W	0x0	TVD3_SRC_SEL. TVD3 Clock Source Select. 000: PLL_VIDEO0(1X) 001: PLL_VIDEO1(1X) 010: PLL_VIDEO0(2X) 011: PLL_VIDEO1(2X) Others: /
23:4	/	/	/.
3:0	R/W	0x0	TVD3_CLK_DIV_M. TVE3 Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

3.3.4.72. GPU Clock Register (Default Value: 0x0000_0000)

Offset: 0x01A0			Register Name: GPU_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SCLK_GATING. 0: Clock is OFF 1: Clock is ON. SCLK= PLL_GPU/**CLK_DIV_RATIO_N**.
30:3	/	/	/.
2:0	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (N) The select clock source is pre-divided by (n+1). The divider is from 1 to 8.

3.3.4.73. Clock OUTA Register (Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: CLK_OUTA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUT_EN Clock Output Enable 0: Disable 1: Clock Output Enable OutputA = **CLK_OUT_SRC_SEL**/**DIVIDER_N**/**DIVIDER_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_OUT_SRC_SEL 00: OSC24MHz/750=32KHz 01: LOSC 10: OSC24MHz 11: /
23:22	/	/	/
21:20	R/W	0x0	DIVIDER_N Clock Output Divide Factor N

Offset: 0x01F0			Register Name: CLK_OUTA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			00: /1 01: /2 10: /4 11: /8
19:13	/	/	/
12:8	R/W	0x0	DIVIDER_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

3.3.4.74. Clock OUTB Register (Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: CLK_OUTB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLK_OUT_EN Clock Output Enable 0: Disable 1: Clock Output Enable OutputB = **CLK_OUT_SRC_SEL**/**DIVIDER_N**/**DIVIDER_M**.
30:26	/	/	/
25:24	R/W	0x0	CLK_OUT_SRC_SEL 00: OSC24MHz/750=32KHz 01: LOSC 10: OSC24MHz 11: /
23:22	/	/	/
21:20	R/W	0x0	DIVIDER_N Clock Output Divide Factor N 00: /1 01: /2 10: /4 11: /8
19:13	/	/	/
12:8	R/W	0x0	DIVIDER_M Clock Output Divide Factor M 00000: /1 00001: /2 00010: /3 …… 11111: /32
7:0	/	/	/

3.3.4.75. PLL_SATA Bias Register (Default Value: 0x1010_0000)

Offset: 0x0218			Register Name: PLL_SATA_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:0	/	/	/

3.3.4.76. PLL_PERIPH1 Bias Register (Default Value: 0x1010_0010)

Offset: 0x021C			Register Name: PLL_PERIPH1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide.
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0].

3.3.4.77. PLL_CPUX Bias Register (Default Value: 0x0810_0200)

Offset: 0x0220			Register Name: PLL_CPUX_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	VCO_RST. VCO reset in.
30:29	/	/	/
28	R/W	0x0	EXG_MODE. Exchange Mode. **NOTE** **CPU PLL source will select PLL_PERIPH instead of PLL_CPU.**
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL. PLL Lock Time Control[2:0].

Offset: 0x0220			Register Name: PLL_CPUX_BIAS_REG
Bit	Read/Write	Default/Hex	Description
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACT_CTRL. PLL Damping Factor Control[3:0].

3.3.4.78. PLL_AUDIO Bias Register (Default Value: 0x1010_0000)

Offset: 0x0224			Register Name: PLL_AUDIO_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:0	/	/	/

3.3.4.79. PLL_VIDEO0 Bias Register (Default Value: 0x1010_0000)

Offset: 0x0228			Register Name: PLL_VIDEO0_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

3.3.4.80. PLL_VE Bias Register (Default Value: 0x1010_0000)

Offset: 0x022C			Register Name: PLL_VE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

3.3.4.81. PLL_DDR0 Bias Register (Default Value: 0x8110_4000)

Offset: 0x0230			Register Name: PLL_DDR0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[3:0].
27:26	/	/	/
25	R/W	0x0	PLL_VCO_GAIN_CTRL_EN. PLL VCO Gain Control Enable. 0: Disable 1: Enable.
24	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide.
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15	/	/	/
14:12	R/W	0x4	PLL_VCO_GAIN_CTRL. PLL VCO Gain Control Bit[2:0].
11:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[3:0].

3.3.4.82. PLL_PERIPH0 Bias Register (Default Value: 0x1010_0010)

Offset: 0x0234			Register Name: PLL_PERIPH0_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL Band Width Control. 0: Narrow 1: Wide.
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[1:0].

3.3.4.83. PLL_VIDEO1 Bias Register (Default Value: 0x1010_0000)

Offset: 0x0238			Register Name: PLL_VIDEO1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/

Offset: 0x0238			Register Name: PLL_VIDEO1_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

3.3.4.84. PLL_GPU Bias Register (Default Value: 0x1010_0000)

Offset: 0x023C			Register Name: PLL_GPU_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

3.3.4.85. PLL_MIPI Bias Register (Default Value: 0xF810_0400)

Offset: 0x0240			Register Name: PLL_MIPI_BIAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	VCO_RST. VCO Reset In.
30:28	R/W	0x7	PLLVDD_LDO_OUT_CTRL. PLLVDD LDO Output Control. **PLL_INPUT_POWER_SEL** =1 **PLL_INPUT_POWER_SEL** =0 000: 1.00V 000: 1.20V 001: 1.02V 001: 1.225V 010: 1.04V 010: 1.25V 011: 1.06V 011: 1.275V 100: 1.08V 100: 1.30V 101: 1.10V 101: 1.325V 110: 1.12V 110: 1.35V 111: 1.14V. 111: 1.375V The **PLL_INPUT_POWER_SEL** bit is in the PLL_MIPI Tuning Register.
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control [3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:11	/	/	/
10:8	R/W	0x4	PLL_LOCK_CTRL. PLL Lock Time Control[2:0].

Offset: 0x0240			Register Name: PLL_MIPI_BIAS_REG
Bit	Read/Write	Default/Hex	Description
7:0	/	/	/
0	R/W	0x0	PLL_DAMP_FACT_CTRL PLL Damping Factor Control

3.3.4.86. PLL_DE Bias Register (Default Value: 0x1010_0000)

Offset: 0x0248			Register Name: PLL_DE_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL Damping Factor Control[2:0].

3.3.4.87. PLL_DDR1 Bias Register (Default Value: 0x1001_0000)

Offset: 0x024C			Register Name: PLL_DDR1_BIAS_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x01	PLL_CUR_BIAS_CTRL. PLL Current Bias Control[4:0].
15:0	/	/	/

3.3.4.88. PLL_CPUX Tuning Register (Default Value: 0x0A10_1000)

Offset: 0x0250			Register Name: PLL_CPUX_TUN_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	PLL_BAND_WID_CTRL. PLL Band Width Control. 0: Narrow 1: Wide.
26	R/W	0x0	VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: Disable 1: Enable.
25:23	R/W	0x4	VCO_GAIN_CTRL. VCO Gain Control Bits[2:0].
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL.

Offset: 0x0250			Register Name: PLL_CPUX_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			PLL Initial Frequency Control[6:0].
15	R/W	0x0	C_OD. C-Reg-Od For Verify.
14:8	R/W	0x10	C_B_IN. C-B-In[6:0] For Verify.
7	R/W	0x0	C_OD1. C-Reg-Od1 For Verify.
6:0	R	0x0	C_B_OUT. C-B-Out[6:0] For Verify.

3.3.4.89. PLL_DDR0 Tuning Register (Default Value: 0x1488_0000)

Offset: 0x0260			Register Name: PLL_DDR0_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	VREG1_OUT_EN. Vreg1 Out Enable. 0: Disable 1: Enable.
27	/	/	/
26:24	R/W	0x4	PLL_LTIME_CTRL. PLL Lock Time Control[2:0].
23	R/W	0x1	VCO_RST. VCO Reset In.
22:16	R/W	0x08	PLL_INIT_FREQ_CTRL. PLL Initial Frequency Control[6:0].
15	R/W	0x0	OD1. Reg-od1 for Verify.
14:8	R/W	0x0	B_IN. B-in[6:0] for Verify.
7	R/W	0x0	OD. Reg-od for Verify.
6:0	R	0x0	B_OUT. B-out[6:0] for Verify.

3.3.4.90. PLL_MIPI Tuning Register (Default Value: 0x8A00_2000)

Offset: 0x0270			Register Name: PLL_MIPI_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	PLL_INPUT_POWER_SEL 0: 2.5V 1: 3.0V
30	/	/	/
29:28	R/W	0x0	VREG_OUT_EN. For Verify
27	R/W	0x1	PLL_BAND_WID_CTRL. PLL Band Width Control.

Offset: 0x0270			Register Name: PLL_MIPI_TUN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Narrow 1: Wide.
26	R/W	0x0	VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: Disable 1: Enable.
25:23	R/W	0x4	VCO_GAIN_CTRL. VCO Gain Control Bits[2:0].
22	/	/	/
21:16	R/W	0x0	CNT_INT. For Verify[5:0].
15	R/W	0x0	C_OD. C-reg-od for Verify
14	/	/	/
13:8	R/W	0x20	C_B_IN. C-B-in[5:0] for Verify
7	R/W	0x0	C_OD1. C-reg-od1 for Verify
6	/	/	/
5:0	R	0x0	C_B_OUT. C-B-out[5:0] for Verify

3.3.4.91. PLL_PERIPH1 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x027C			Register Name: PLL_PERIPH1_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.92. PLL_CPUX Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0280			Register Name: PLL_CPUX_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.93. PLL_AUDIO Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0284			Register Name: PLL_AUDIO_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.94. PLL_VIDEO0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x288			Register Name: PLL_VIDEO0_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.95. PLL_VE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x028C			Register Name: PLL_VE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.96. PLL_DDR0 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0290			Register Name: PLL_DDR0_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.97. PLL_VIDEO1 Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x0298			Register Name: PLL_VIDEO1_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.98. PLL_GPU Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x029C			Register Name: PLL_GPU_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.99. PLL_MIPI Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x02A0			Register Name: PLL_MIPI_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.100. PLL_DE Pattern Control Register (Default Value: 0x0000_0000)

Offset: 0x02A8			Register Name: PLL_DE_PAT_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 1X: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.101. PLL_DDR1 Pattern Control Register 0 (Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: PLL_DDR1_PAT_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-Delta Pattern Enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: / 11: Triangular.
28:20	R/W	0x0	WAVE_STEP. Wave Step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5kHz 01: 32kHz 10: 32.5kHz 11: 33kHz.
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

3.3.4.102. PLL_DDR1 Pattern Control Register 1 (Default Value: 0x0000_0000)

Offset: 0x02B0			Register Name: PLL_DDR1_PAT_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
30:25	/	/	/
24	R/W	0x0	DITHER_EN.
23:21	/	/	/
20	R/W	0x0	FRAC_EN.
19:17	/	/	/
16:0	R/W	0x0	FRAC_IN.

3.3.4.103. Bus Software Reset Register 0 (Default Value: 0x0000_0000)

Offset: 0x02C0			Register Name: BUS_SOFT_RST_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	USBOHCI2_RST. Gating Clock for USB OHCI2 0: Assert 1: De-assert.
30	R/W	0x0	USBOHCI1_RST. Gating Clock for USB OHCI1 0: Assert 1: De-assert.
29	R/W	0x0	USBOHCI0_RST. Gating Clock for USB OHCI0 0: Assert 1: De-assert.
28	R/W	0x0	USBEHCI2_RST. Gating Clock for USB EHCI2 0: Assert 1: De-assert.
27	R/W	0x0	USBEHCI1_RST. Gating Clock for USB EHCI1 0: Assert 1: De-assert.
26	R/W	0x0	USBEHCI0_RST. Gating Clock for USB EHCI0 0: Assert 1: De-assert.
25	R/W	0x0	USBOTG_RST. Gating Clock for USB OTG 0: Assert 1: De-assert.
24	R/W	0x0	SATA_RST. Gating Clock for SATA 0: Assert

Offset: 0x02C0			Register Name: BUS_SOFT_RST_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: De-assert.
23	R/W	0x0	SPI3_RST. Gating Clock for SPI3 0: Assert 1: De-assert.
22	R/W	0x0	SPI2_RST. SPI2 Reset. 0: Assert 1: De-assert.
21	R/W	0x0	SPI1_RST. SPI1 Reset. 0: Assert 1: De-assert.
20	R/W	0x0	SPI0_RST. SPI0 Reset. 0: Assert 1: De-assert.
19	R/W	0x0	HSTMR_RST. High Speed Timer Reset. 0: Assert 1: De-assert.
18	R/W	0x0	TS_RST. TS Reset. 0: Assert 1: De-assert
17	R/W	0x0	EMAC_RST. EMAC Reset. 0: Assert 1: De-assert
16:15	/	/	/
14	R/W	0x0	SDRAM_RST. SDRAM AHB Reset. 0: Assert 1: De-assert.
13	R/W	0x0	NAND_RST. NAND Reset. 0: Assert 1: De-assert.
12	/	/	/
11	R/W	0x0	SMHC3_RST. SMHC3 Reset. 0: Assert 1: De-assert.
10	R/W	0x0	SMHC2_RST.

Offset: 0x02C0			Register Name: BUS_SOFT_RST_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			SMHC2 Reset. 0: Assert 1: De-assert.
9	R/W	0x0	SMHC1_RST. SMHC1 Reset. 0: Assert 1: De-assert.
8	R/W	0x0	SMHC0_RST. SMHC0 Reset. 0: Assert 1: De-assert.
7	/	/	/
6	R/W	0x0	DMA_RST. DMA Reset. 0: Assert 1: De-assert.
5	R/W	0x0	CE_RST. CE Reset. 0: Assert 1: De-assert.
4:2	/	/	/
1	R/W	0x0	MIPI_DSI_RST MIPI DSI Reset 0: Assert 1: De-assert
0	/	/	/

3.3.4.104. Bus Software Reset Register 1 (Default Value: 0x0000_0000)

Offset: 0x02C4			Register Name: BUS_SOFT_RST_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DCU_RST. DCU Reset. 0: Assert 1: De-assert
30	R/W	0x0	TCON_TOP_RST TCON_TOP Reset. 0: Assert 1: De-assert
29	R/W	0x0	TCON_TV1_RST TCON_TV1 Reset. 0: Assert 1: De-assert

Offset: 0x02C4			Register Name: BUS_SOFT_RST_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	TCON_TV0_RST TCON_TV0 Reset. 0: Assert 1: De-assert
27	R/W	0x0	TCON_LCD1_RST TCON_LCD1 Reset. 0: Assert 1: De-assert
26	R/W	0x0	TCON_LCD0_RST TCON_LCD0 Reset. 0: Assert 1: De-assert
25	R/W	0x0	TVD_TOP_RST TVD_TOP Reset. 0: Assert 1: De-assert
24	R/W	0x0	TVD3_RST TVD3 Reset. 0: Assert 1: De-assert
23	R/W	0x0	TVD2_RST TVD2 Reset. 0: Assert 1: De-assert
22	R/W	0x0	TVD1_RST TVD1 Reset. 0: Assert 1: De-assert
21	R/W	0x0	TVD0_RST TVD0 Reset. 0: Assert 1: De-assert
20	R/W	0x0	GPU_RST. GPU Reset. 0: Assert 1: De-assert.
19:18	/	/	/
17	R/W	0x0	GMAC_RST. GMAC Reset. 0: Assert 1: De-assert.
16	/	/	/
15	R/W	0x0	TVE_TOP_RST TVE_TOP Reset.

Offset: 0x02C4			Register Name: BUS_SOFT_RST_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Assert 1: De-assert.
14	R/W	0x0	TVE1_RST TVE1 Reset. 0: Assert 1: De-assert.
13	R/W	0x0	TVE0_RST TVE0 Reset. 0: Assert 1: De-assert.
12	R/W	0x0	DE_RST. DE Reset. 0: Assert 1: De-assert.
11	R/W	0x0	HDMI1_RST. HDMI1 Reset. 0: Assert 1: De-assert
10	R/W	0x0	HDMI0_RST. HDMI0 Reset. 0: Assert 1: De-assert
9	R/W	0x0	CSI1_RST. CSI0 Reset. 0: Assert 1: De-assert.
8	R/W	0x0	CSI0_RST. CSI0 Reset. 0: Assert 1: De-assert.
7:6	/	/	
5	R/W	0x0	DI_RST. DEINTERLACE Reset. 0: Assert 1:De-assert
4:3	/	/	/
2	R/W	0x0	MP_RST MP Reset 0: Assert 1:De-assert
1	/	/	/
0	R/W	0x0	VE_RST. VE Reset.

Offset: 0x02C4			Register Name: BUS_SOFT_RST_REG1
Bit	Read/Write	Default/Hex	Description
			0: Assert 1: De-assert.

3.3.4.105. Bus Software Reset Register 2 (Default Value: 0x0000_0000)

Offset: 0x02C8			Register Name: BUS_SOFT_RST_REG2
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	LVDS_RST. LVDS Reset. 0: Assert 1: De-assert.

3.3.4.106. Bus Software Reset Register 3 (Default Value: 0x0000_0000)

Offset: 0x02D0			Register Name: BUS_SOFT_RST_REG3
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14	R/W	0x0	I2S/PCM2_RST. I2S/PCM2 Reset. 0: Assert 1: De-assert.
13	R/W	0x0	I2S/PCM1_RST. I2S/PCM1 Reset. 0: Assert 1: De-assert.
12	R/W	0x0	I2S/PCM0_RST. I2S/PCM0 Reset. 0: Assert 1: De-assert.
11	/	/	/
10	R/W	0x0	KEY_RST KEY Reset 0:Assert 1:De-assert
9	/	/	/
8	R/W	0x0	THS_RST. THS Reset. 0: Assert 1: De-assert
7	R/W	0x0	CIR1_RST CIR1 Reset 0: Assert

Offset: 0x02D0			Register Name: BUS_SOFT_RST_REG3
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: De-assert
6	R/W	0x0	CIR0_RST CIR0 Reset 0: Assert 1: De-assert
5:3	/	/	/
2	R/W	0x0	AC97_RST AC97 Reset 0: Assert 1: De-assert
1	R/W	0x0	C
0	R/W	0x0	AC_RST. AC Reset. 0: Assert 1: De-assert

3.3.4.107. Bus Software Reset Register 4 (Default Value: 0x0000_0000)

Offset: 0x02D8			Register Name: BUS_SOFT_RST_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	UART7_RST. UART7 Reset. 0: Assert 1: De-assert.
22	R/W	0x0	UART6_RST. UART6 Reset. 0: Assert 1: De-assert.
21	R/W	0x0	UART5_RST. UART5 Reset. 0: Assert 1: De-assert.
20	R/W	0x0	UART4_RST. UART4 Reset. 0: Assert 1: De-assert.
19	R/W	0x0	UART3_RST. UART3 Reset. 0: Assert 1: De-assert.
18	R/W	0x0	UART2_RST. UART2 Reset.

Offset: 0x02D8			Register Name: BUS_SOFT_RST_REG4
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Assert 1: De-assert.
17	R/W	0x0	UART1_RST. UART1 Reset. 0: Assert 1: De-assert.
16	R/W	0x0	UART0_RST. UART0 Reset. 0: Assert 1: De-assert.
15	R/W	0x0	TWI4_RST. TWI4 Reset. 0: Assert 1: De-assert.
14:8	/	/	/
7	R/W	0x0	PS2_1_RST PS2_1 Reset 0: Assert 1: De-assert
6	R/W	0x0	PS2_0_RST PS2_0 Reset 0: Assert 1: De-assert
5	R/W	0x0	SCR_RST. SCR Reset. 0: Assert 1: De-assert
4	R/W	0x0	Reserved
3	R/W	0x0	TWI3_RST. TWI3 Reset. 0: Assert 1: De-assert.
2	R/W	0x0	TWI2_RST. TWI2 Reset. 0: Assert 1: De-assert.
1	R/W	0x0	TWI1_RST. TWI1 Reset. 0: Assert 1: De-assert.
0	R/W	0x0	TWI0_RST. TWI0 Reset. 0: Assert 1: De-assert.

3.3.4.108. PS Control Register (Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: PS_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	DEC_SEL Device Select
7	R/W	0x0	DET_FIN. Detect Finish. 0: Unfinished 1: Finished Setting 1 to this bit will clear it.
6	R/W	0x0	DLY_SEL. Delay Select 0: 1 Cycle 1: 2 Cycles
5:4	R/W	0x0	OSC_SEL OSC Select. 00: IDLE 01: SVT 10: LVT 11: ULVT
3:1	R/W	0x0	TIME_DET. Time Detect. 000: 0.5/4 us 001: 0.5/2 us 010: 0.5/1 us 011: 0.5*2us ..... 111:0.5*2^5us
0	R/W	0x0	MOD_EN. Module Enable. 0: Disable 1: Enable

3.3.4.109. PS Counter Register (Default Value: 0x0000_0000)

Offset: 0x0304			Register Name: PS_CNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	RO	0x0	PS_CNT. PS Counter.

3.3.4.110. System 32K Clock Control Register(Default Value: 0x0000_000F)

Offset: 0x0310			Register Name: SYS_32K_CLK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 8 can be written with the new value.
8	R/W	0x0	SYS_32K_SEL. System 32K Select. 0: System internal 32K. 1: LOSC(from RTC) System internal 32K = 2M / **SYS_INTERNAL_RC_DIV**.
7:5	/	/	/
4:0	R/W	0xF	SYS_INTERNAL_RC_DIV. System internal RC divide. **NOTE** **System internal RC = 2M.** 00000: 1 00001: 2 00010: 3 ..... 11111: 31

3.3.4.111. System Internal 32K Clock Auto Calibration Register(Default Value: 0x0000_0000)

Offset: 0x0314			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	RC Calibration Enable 0: Disable 1: Enable
0	R/W	0x0	RC Calibration Function Enable

3.3.4.112. PLL Lock Control Register (Default Value: 0x0000_0000)

Offset: 0x0320			Register Name: PLL_LOCK_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	DBG_EN Debug Enable 0: Disable 1: Enable
23:20	R/W	0x0	DBG_SEL Debug Select 0000: PLL_CPUX

Offset: 0x0320			Register Name: PLL_LOCK_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0001: PLL_AUDIO 0010: PLL_VIDEO0 0011: PLL_VE 0100: PLL_DDR0 0101: PLL_PERIPH0 0110: PLL_VIDEO1 0111: PLL_GPU 1000: PLL_MIPI 1001: PLL_SATA 1010: PLL_DE 1011: PLL_DDR1 1100: PLL_PERIPH1 Others: /
19	/	/	/
18:17	R/W	0x0	UNLOCK_LEVEL Unlock Level 00: 21~29 Clock Cycles 01: 22~28 Clock Cycles 1X: 20~30 Clock Cycles
16	R/W	0x0	LOCK_LEVEL Lock Level 0: 24~26 Clock Cycles 1: 23~27 Clock Cycles
15:13	/	/	/
12:0	R/W	0x0	LOCK_EN Lock Enable Bit12: PLL_PERIPH1 Bit11: PLL_DDR1 Bit10: PLL_DE Bit9: PLL_SATA Bit8: PLL_MIPI Bit7: PLL_GPU Bit6: PLL_VIDEO1 Bit5: PLL_PERIPH0 Bit4: PLL_DDR0 Bit3: PLL_VE Bit2: PLL_VIDEO0 Bit1: PLL_AUDIO Bit0: PLL_CPUX

3.4. System Boot

3.4.1. Overview

A40i processor supports system boot from NAND Flash, eMMC,SPI NOR Flash (SPI0), SD card (SDC 0/2), and USB.

After power on, the system will try to boot from SDC0, SPI0, eMMC2, SDC2, NAND Flash and USB successively, but if the Boot Select Pin, an external pin that is used to select system boot method, is checked to be in low level state, the system will direclty boot from USB. In normal state, this pin is pulled up by an internal 50kohm resistor.

3.4.2. System Boot Diagram

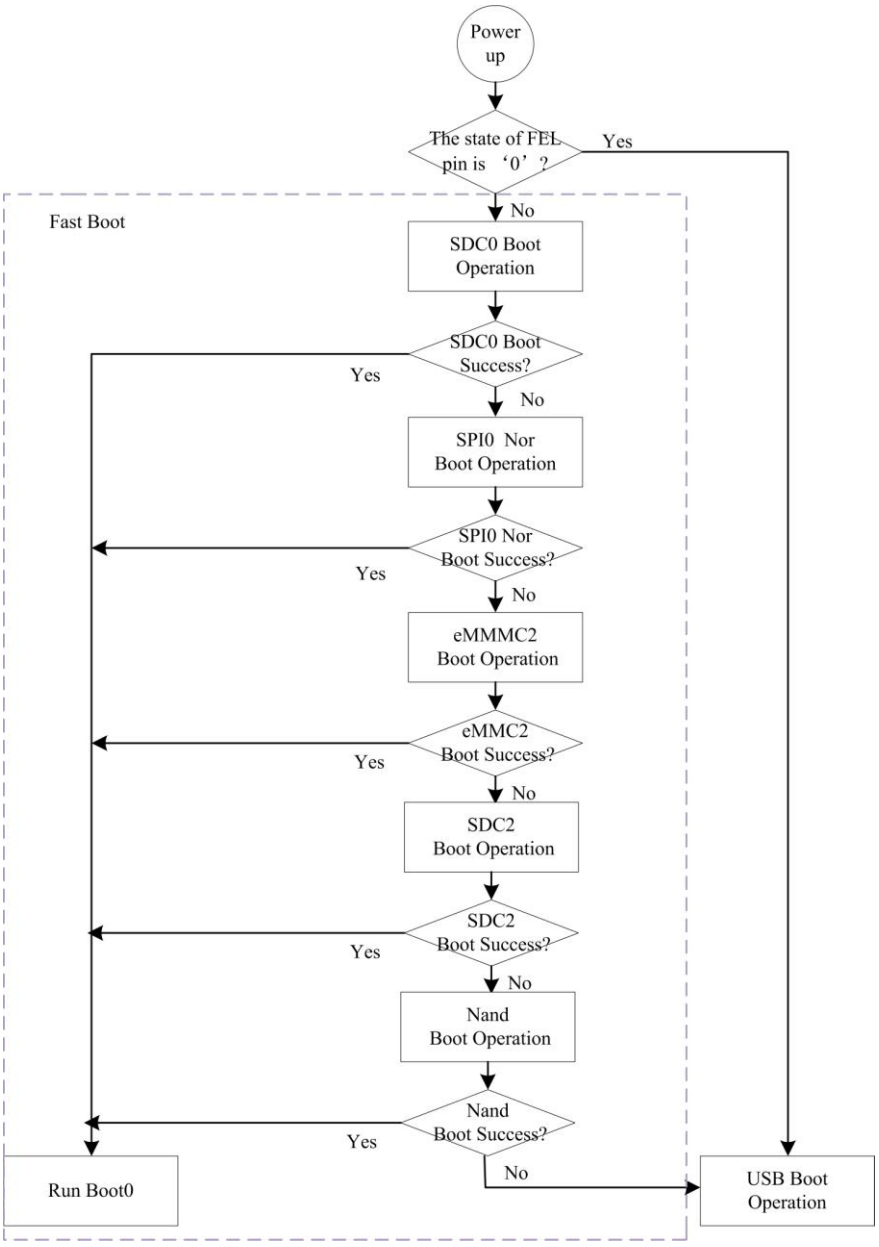


Figure 3-4. System Boot Diagram

3.5. System Control

3.5.1. Overview

The chip embeds a high-speed SRAM. This internal SRAM is split into five areas, and its memory mapping is detailed in the following table.

Area	Address	Size(Bytes)
A1	0x0000 0000--0x0000 3FFF	16K
A2	0x0000 4000--0x0000 7FFF	16K
A3	0x0000 8000--0x0000 B3FF	13K
A4	0x0000 B400--0x0000 BFFF	3K
C1	0x01D0 0000-0x01D7 FFFF	VE
C2	0x01D8 0000-0x01D9 FFFF	ACE
C3	0x01DC 0000-0x01DC FFFF	ISP
NAND		2K
D(USB)	0x0001 0000—0x0001 0FFF	4K
CPU0 I-Cache		32K
CPU0 D-Cache		32K
CPU1 I-Cache		32K
CPU1 D-Cache		32K
CPU2 I-Cache		32K
CPU2 D-Cache		32K
CPU3 I-Cache		32K
CPU3 D-Cache		32K
CPU L2 Cache		512K

3.5.2. Register List

Module Name	Base Address
SYS_CTRL	0x01C00000

Register Name	Offset	Description
SRAM_CTRL_REG0	0x0000	SRAM Control Register 0
SRAM_CTRL_REG1	0x0004	SRAM Control Register 1
GPU_SRAM_TEST_CTRL_REG	0x0008	GPU SRAM Control Register
NMI_IRQ_CTRL_REG	0x0030	NMI Interrupt Control Register
NMI_IRQ_PEND_REG	0x0034	NMI Interrupt Pending Register
NMI_IRQ_ENABLE_REG	0x0038	NMI Interrupt Enable Register
L1_CFG_REG	0x003C	L1 Cache Configuration Register
L2_CFG_REG	0x0044	L2 Cache Configuration Register
BOOT_CPU_HP_FLAG_REG	0x00B8	Boot CPU Hot Plug Flag Register
CPU_SOFT_ENT_REG0	0x00BC	CPU Software Entry Register 0

3.5.3. Register Description

3.5.3.1. SRAM Control Register 0(Default Value: 0x7FFF_FFFF)

Offset: 0x0000			Register Name: SRAM_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:0	R/W	0x7fffffff	SRAM_C1_MAP. SRAM Area C1 50K Byte Configuration by AHB. 0: Map to CPU/DMA 1: Map to VE

3.5.3.2. SRAM Control Register 1(Default Value: 0x0000_1300)

Offset: 0x0004			Register Name: SRAM_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	BIST_DMA_CTRL_SEL. Bist and DMA control select. 0: DMA 1: Bist.
30:13	/	/	/
12	R/W	0x1	SRAM_C3_MAP. SRAM C3 map configuration. 0: Map to CPU/BIST 1: Map to ISP
11:10	/	/	/
9:8	R/W	0x3	SRAM_C2_MAP. SRAM C2 map configuration. 00: Map to CPU/BIST 01: Map to AE 10: Map to CE 11: Map to ACE
7:6	/	/	/
5:4	R/W	0x0	SRAM_A3_A4_MAP. SRAM Area A3/A4 Configuration by AHB. 00: Map to CPU/DMA 01: Map to EMAC 10: / 11: /
3:1	/	/	/
0	R/W	0x0	SRAMD_MAP. SRAM D Area Config. 0: Map to CPU/DMA 1: Map to USB0

3.5.3.3. GPU SRAM Test Control Register (Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GPU_SRAM_TEST_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	GPU_SRAM_TEST_CTRL. GPU sram test control.

3.5.3.4. NMI Interrupt Control Register(Default Value: 0x0000_0000)

Offset:0x0030			Register Name: NMI_IRQ_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	NMI_IRQ_SRC_TYPE. External NMI Interrupt Source Type. External NMI pin will be changed to alarm output if the power of I/O is switched off, and its power source is RTCVDD. 00: Low level sensitive 01: Negative edge trigged 10: High level sensitive 11: Positive edge sensitive

3.5.3.5. NMI Interrupt Pending Register(Default Value: 0x0000_0000)

Offset:0x0034			Register Name: NMI_IRQ_PEND_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	NMI_IRQ_SRC_PEND. NMI Source Pending and Clear Bit 0: NMI interrupt is not pending 1: NMI interrupt is pending

3.5.3.6. NMI Interrupt Enable Register(Default Value: 0x0000_0000)

Offset:0x0038			Register Name: NMI_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	NMI_IRQ_SRC_ENABLE. NMI Source Enable and Disable Bit. 0: NMI interrupt is disable 1: NMI interrupt is enable

3.5.3.7. L1 Cache Configuration Register (Default Value: 0x0022_2222)

Offset:0x003C			Register Name: L1_CACHE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset:0x003C			Register Name: L1_CACHE_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x1	L1TLB_DELAY.
19	/	/	/
18:16	R/W	0x1	L1DY_DELAY.
15	/	/	/
14:12	R/W	0x1	L1DT_DELAY.
11	/	/	/
10:8	R/W	0x1	L1DD_DELAY.
7	/	/	/
6:4	R/W	0x1	L1IT_DELAY.
3	/	/	/
2:0	R/W	0x1	L1ID_DELAY.

3.5.3.8. L2 Cache Configuration Register (Default Value: 0x2222_2220)

Offset:0x0044			Register Name: L2_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x2222	/
15:14	R/W	0x0	/
13:12	R/W	0x2	L2_EMAW[1:0]
11	R/W	0x0	/
10:8	R/W	0x2	L2_EMA[2:0]
7	R/W	0x0	/
6:4	R/W	0x1	L2T_DELAY[2:0]
3:2	R/W	0x0	/
1:0	R/W	0x0	/

3.5.3.9. Boot CPU Hot Plug Flag Register(Default Value: 0x0000_0000)

Offset:0x00B8			Register Name: BOOT_CPU_HP_FLAG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Boot CPU software flag when acting from hot plug.

3.5.3.10. CPU Software Entry Register 0(Default Value: 0x0000_0000)

Offset:0x00BC			Register Name: CPU_SOFT_ENT_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	Boot CPU software entry register when acting from hot plug or Non-boot CPU software entry register.

3.6. PWM

3.6.1. Overview

PWM controller has 8 PWM channels(PWM0,PWM1,PWM2,PWM3,PWM4,PWM5,PWM6,PWM7), and divides to 4 PWM pairs:PWM01 pair,PWM23 pair,PWM45 pair,PWM67 pair.PWM01 pair consists of PWM0 and PWM1, PWM23 pair consists of PWM2 and PWM3, PWM45 pair consists of PWM4 and PWM5, PWM67 pair consists of PWM6 and PWM7.Each PWM pair built-in 1 clock module, 2 timer logic module and 1 programmable dead-time generator.

Each PWM channel supports two functions including PWM output and capture input.The clock sources of PWM channel have OSC24M and APB1.PWM channel can output single-pulse waveform or long-period waveform,the frequency range of the output waveform is from 0Hz to OSC24M/APB1 CLK.PWM also can capture input waveform.PWM channel captures the current value of 16bit adding-counter at the external rising edge, and loads to **Capture Rise Lock Register**, PWM channel captures the current value of 16bit adding-counter at the external falling edge,and loads to **Capture Fall Lock Register**,then the frequency of the external clock can be calculated accurately by the value of **Capture Rise Lock Register** and **Capture Fall Lock Register**.

PWM pair can output complementary waveform pair or dead-time PWM pair. When the two channel at a PWM pair have the same prescale,the same period register and opposite active state, then PWM pair output a complementary wareform pair; when the programmable dead-time generator of PWM pair is enabled,then PWM pair output the waveform pair with dead-time, and the dead-time is controllable.

PWM channel can configure to generate interrupt. PWM is as output function, when 16bit adding-counter is equal to the value of entire cycle, PWM channel can be enabled to generate interrupt. PWM is as input function, when PWM channel captures the external rising edge, PWM channel can be enabled to generate one interrupt; when PWM channel captures the external falling edge, PWM channel can be enabled to generated one interrupt;when PWM channel captures rising edge or falling edge,PWM can trigger interrupt.

3.6.2. Block Diagram

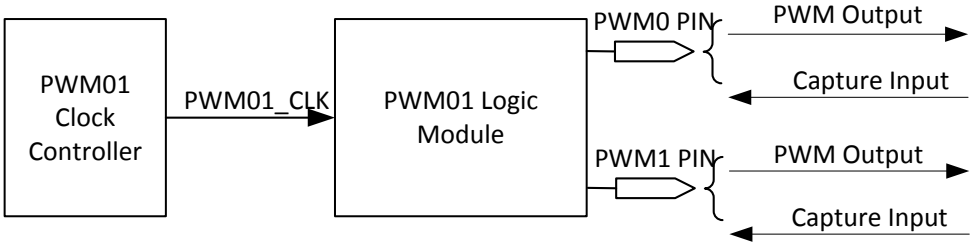


Figure 3-5. PWM01 Block Diagram

The above figure indicates PWM01 block diagram, the block diagram of other PWM pairs is the same as PWM01 pair. Each PWM pair supports PWM output and capture input.When using PWM output function, two channels of each PWM pair are all configured as PWM output;when using capture input function,two channels of each PWM pair are all configured as capture input.

3.6.3. Operations and Functional Descriptions

3.6.3.1. Clock Controller

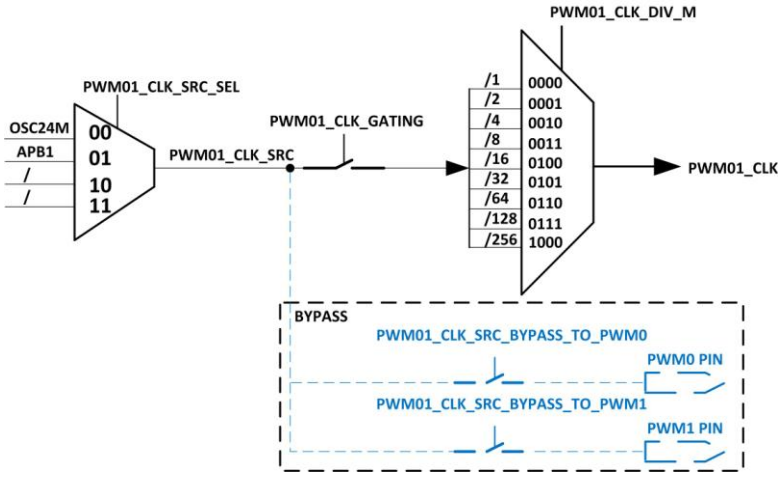


Figure 3-6. PWM01 Clock Controller Diagram

The clock controller of each PWM pair includes clock source select,1~256 scaler and clock source bypass.The clock sources of PWM have OSC24M and APB1 Bus.The clock source bypass function is that clock source directly accesses PWM output,the PWM output waveform is the waveform of clock source. At last the output clock of the clock controller is sent to PWM logic module.

3.6.3.2. PWM Logic Module Clock Controller

The logic module of each PWM pair consists of three parts: two 8bit prescaler, two timer logic and one programmable dead-zone generator. Using PWM01 as an example.Figure 3-7 indicates PWM output logic module diagram.

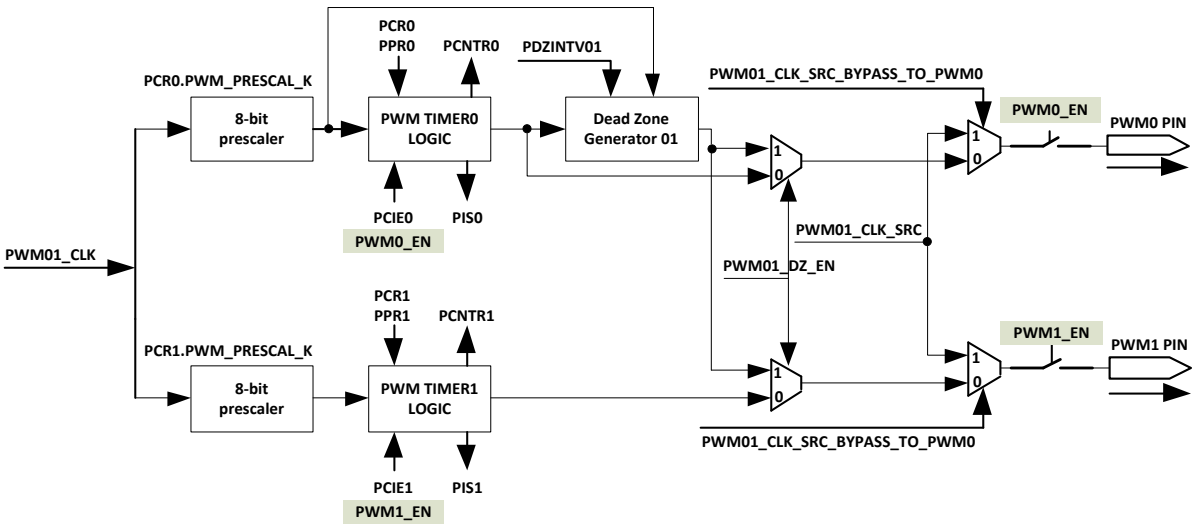


Figure 3-7. PWM Output Logic Module Diagram

In the above figure, PWM Timer Logic consists of one 16bit adding-counter and one 16bit comparator. The adding-counter is used to control period, and the comparator is used to control duty-cycle. The adding-counter and the comparator support cache-loading, PWM output is enabled, the register value of the counter and the comparator can

be changed at any time,the changed value is cached to the cache register,when the value of adding-counter is equal to PPR.PWM_ENTIRE_CYCLE, the value of the cache register is loaded to the counter and the comparator. Cache-loading is good to avoid unstable PWM output waveform with burred feature when updating the counter value and the comparator value.

PWM supports long-period and single-pulse waveform output.
Long-period mode: When the value of adding-counter reaches PPR.PWM_ENTIRE_CYCLE, the value of adding-counter is loaded automatically to 0 and continues to count, then the output waveform is a continuous waveform.
Single-pulse mode: When the value of adding-counter reaches PPR.PWM_ENTIRE_CYCLE, the value of adding-counter is loaded automatically to 0 but stop counting, then the output waveform is a single-pulse waveform.

3.6.3.3. Adding-counter and Comparator

The period, duty-cycle and active state of PWM output waveform are decided by the adding-counter and comparator.The rule of the comparator is as follows.
PCNTR >= (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “active state”
PCNTR < (PWM_ENTIRE_CYCLE - PWM_ACT_CYCLE), output “~ (active state)”
(1) Active state of PWM0 channel is high level (PCR0. PWM_ACT_STA = 1)
When PCNTR0 >= (PPR0. PWM_ENTIRE_CYCLE – PPR0.PWM_ACT_CYCLE), then PWM0 output 1.
When PCNTR0 < (PPR0. PWM_ENTIRE_CYCLE – PPR0.PWM_ACT_CYCLE), then PWM0 output 0.

The formula of PWM output period and duty-cycle is as follows.
T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE
$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE
$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE – PPR0.PWM_ACT_CYCLE)
Duty-cycle = (high level time) / (1 period time)

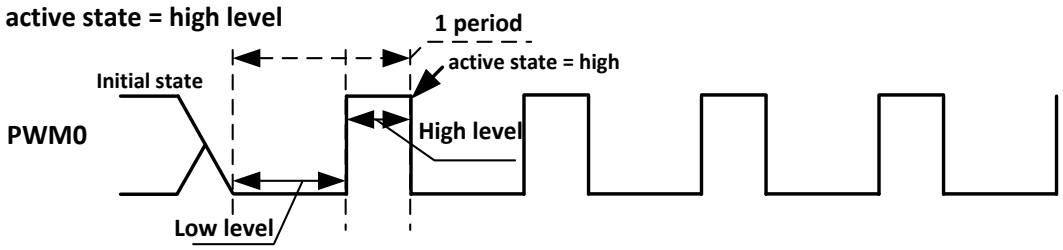


Figure 3-8. PWM0 High Level Active State

(2) Active state of PWM0 channel is low level (PCR0. PWM_ACT_STA = 0)
When PCNTR0 >= (PPR0. PWM_ENTIRE_CYCLE – PPR0.PWM_ACT_CYCLE), then PWM0 output 0.
When PCNTR0 < (PPR0. PWM_ENTIRE_CYCLE – PPR0.PWM_ACT_CYCLE), then PWM0 output 1.

The formula of PWM output period and duty-cycle is as follows.
T_{period} = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0. PWM_ENTIRE_CYCLE
$T_{high\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * (PPR0.PWM_ENTIRE_CYCLE – PPR0.PWM_ACT_CYCLE)
$T_{low\text{-}level}$ = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PPR0.PWM_ACT_CYCLE
Duty-cycle = (high level time) / (1 period time)

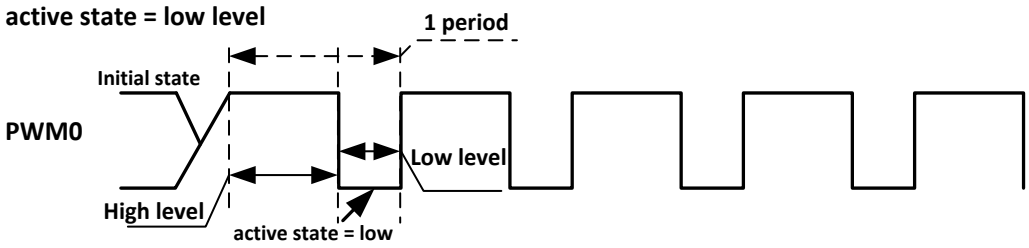


Figure 3-9. PWM0 Low Level Active State

3.6.3.4. Single-pulse Mode and Long-period Mode

PWM output supports single-pulse mode and long-period mode. PWM in single-pulse mode outputs a single-pulse waveform, but PWM in long-period mode outputs continuous waveform.Figure 3-10 shows the PWM output waveform in single-pulse mode and long-period mode.

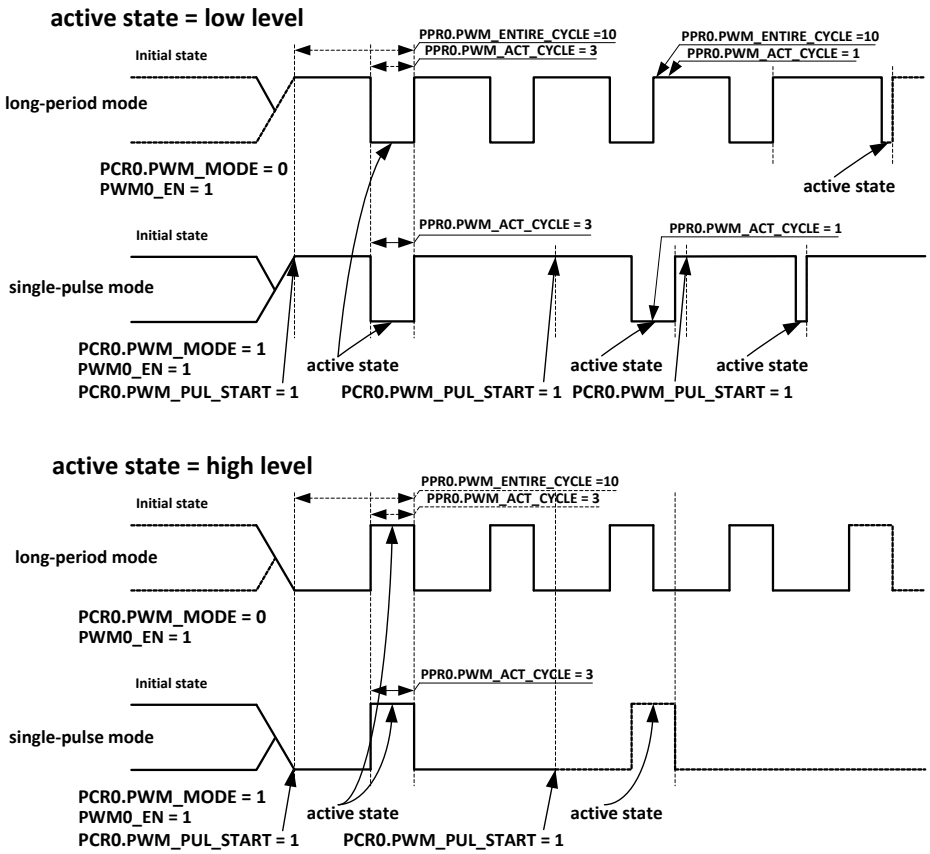


Figure 3-10. PWM0 Output Waveform in Single-pulse Mode and Long-period Mode

When PCR0.PWM_MODE is 0, PWM0 outputs long-period waveform.The calculating formula of T_{period} and $T_{active\text{-}state}$ refers to **3.6.3.3. Adding-counter and Comparator**.

When PCR0.PWM_MODE is 1, PWM0 outputs single-pulse waveform.The calculating formula of single-pulse length is as follows.

Single-pulse length = PWM01_CLK / PWM0_PRESCALE_K * PPR0. PWM_ACT_CYCLE

When PCR0.PWM_ACT_STA is 0, the pulse level is low level, PWM0 channel outputs low pulse.

When PCR0.PWM_ACT_STA is 1, the pulse level is high level, PWM0 channel outputs high pulse.

3.6.3.5. Complementary Pair Output

Every PWM pair supports complementary pair output and PWM pair with dead-time**.** Figure 3-11 shows the complementary pair output of PWM01.

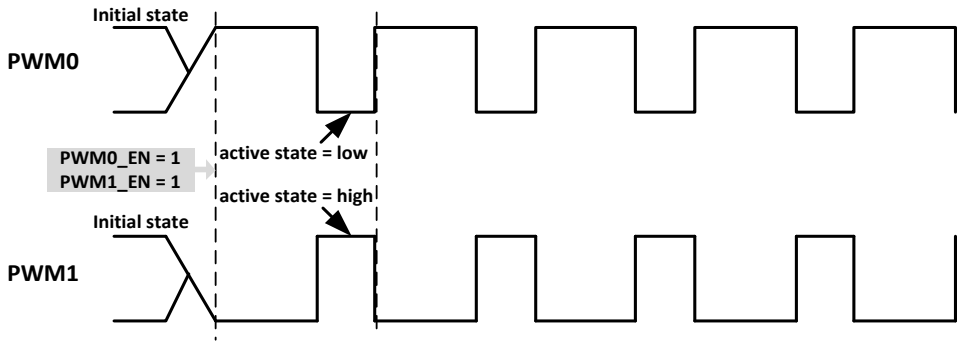


Figure 3-11. PWM01 Complementary Pair Output

The complementary pair output need satisfy the following three conditions:

The same frequency, the same duty-cycle

Opposite active state

Enable two channels of PWM pair at the same time

Every PWM pair has a programmable dead-time generator. When the dead-time function of PWM pair enabled,PWM01 output waveform is desided by PWM timer logic and DeadZone Generator. Figure 3-12 shows the output waveform.

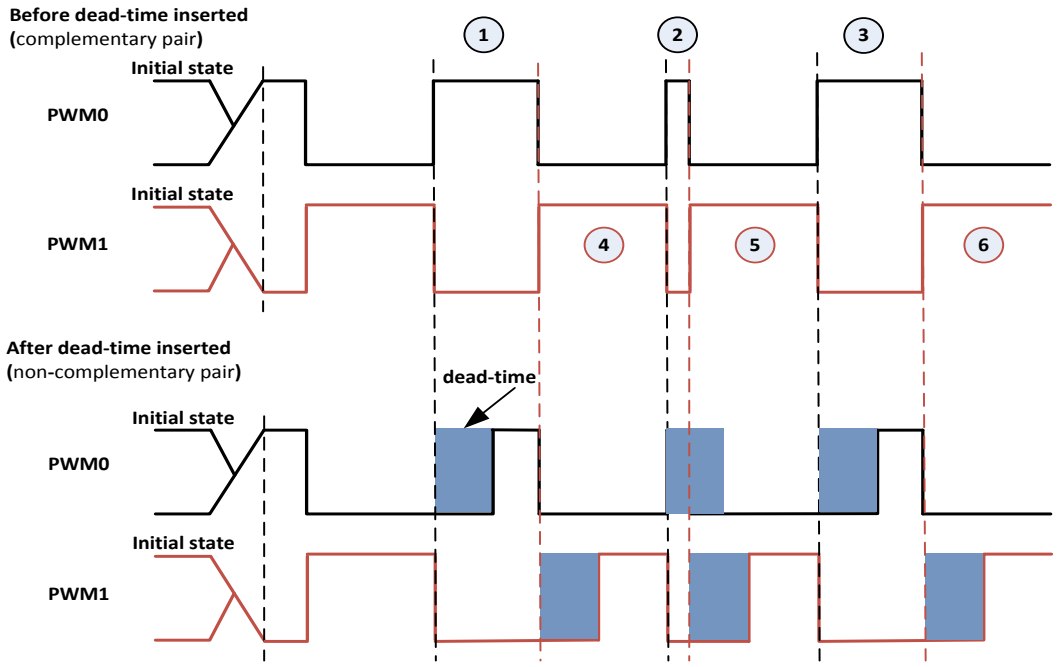


Figure 3-12. Dead-time Output Waveform

Dead Zone Generator 01 inserts dead-time as soon as the rising edge came. If high level time is less than dead-time,then dead-time will cover the high level. The setting of dead-time need consider the period and duty-cycle of output waveform. Dead-time formula is defined as follows:

Dead-time = (PWM01_CLK / PWM0_PRESCALE_K)$^{-1}$ * PDZINTV01

3.6.3.6. Capture Input

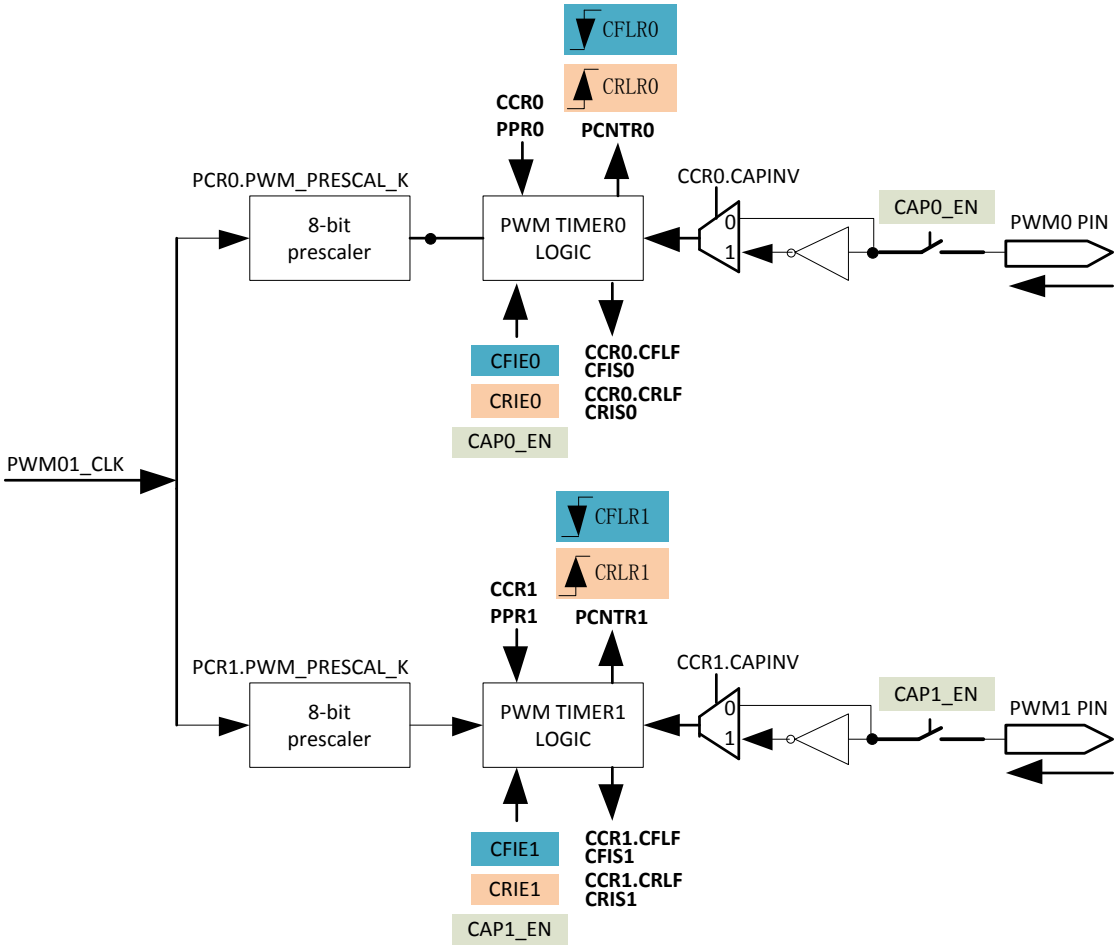


Figure 3-13. PWM01 Capture Logic Module Diagram

Besides the timer logic module of every PWM channel generates PWM output, it can be used to capture the external clock.Using PWM0 channel as an example,PWM0 channel has one **CFLR** and one **CRLR** for capturing adding-counter value in falling edge, in rising edge,respectively.You can calculate the period of external clock by **CFLR** and **CRLR.**

$T_{high\text{-}level} = (PWM01\_CLK / PWM0\_PRESCALE\_K)^{-1} * CRLR0$

$T_{low\text{-}level} = (PWM01\_CLK / PWM0\_PRESCALE\_K)^{-1} * CFLR0$

$T_{period} = T_{high\text{-}level} + T_{low\text{-}level}$

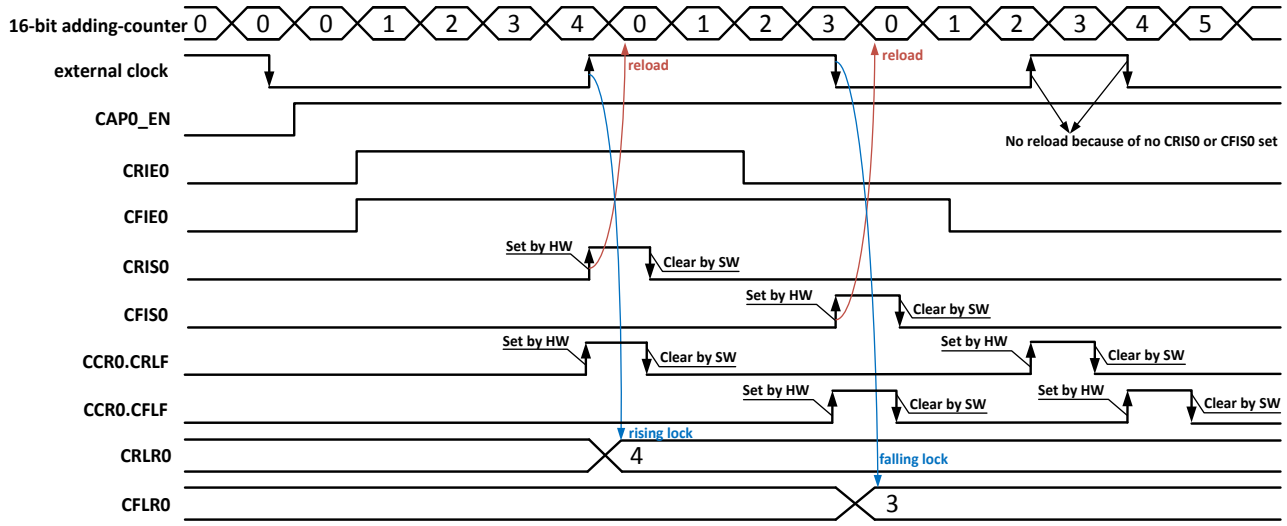


Figure 3-14. PWM0 Channel Capture Timing

When the capture input function of PWM channel is enabled, the adding-counter of PWM0 channel starts to work. when the timer logic module of PWM0 captures one rising edge,the current value of adding-counter is locked to **CRLR** and **CRLF** is set to 1 . If **CRIE0** is 1, then **CRIS0** is set to 1, PWM0 channel sends interrupt request, and the adding-counter is loaded to 0 and continues to count. If **CRIE0** is 0, the adding-counter is not loaded to 0.

When the timer logic module of PWM0 captures one falling edge, the current value of adding-counter is locked to **CFLR** and **CFLF** is set to 1 . If **CFIE0** is 1, then **CFIS0** is set to 1, PWM0 channel sends interrupt request, and the adding-counter is loaded to 0 and continues to count. If **CFIE0** is 0, the adding-counter is not loaded to 0.

3.6.4. Register List

Module Name	Base Address
PWM	0x01C23400

Register Name	Offset	Description
PIER	0x0000	PWM IRQ Enable Register
PISR	0x0004	PWM IRQ Status Register
CIER	0x0010	Capture IRQ Enable Register
CISR	0x0014	Capture IRQ Status Register
PCCR01	0x0020	PWM01 Clock Configuration Register
PCCR23	0x0024	PWM23 Clock Configuration Register
PCCR45	0x0028	PWM45 Clock Configuration Register
PCCR67	0x002C	PWM67 Clock Configuration Register
PDZCR01	0x0030	PWM01 Dead Zone Control Register
PDZCR23	0x0034	PWM23 Dead Zone Control Register
PDZCR45	0x0038	PWM45 Dead Zone Control Register
PDZCR67	0x003C	PWM67 Dead Zone Control Register
PER	0x0040	PWM Enable Register
CER	0x0044	Capture Enable Register
PCR	0x0060+N*0x20(N= 0~7)	PWM Control Register
PPR	0x0064+N*0x20(N= 0~7)	PWM Period Register
PCNTR	0x0068+N*0x20(N= 0~7)	PWM Count Register
CCR	0x006C+N*0x20(N= 0~7)	Capture Control Register

Register Name	Offset	Description
CRLR	0x0070+N*0x20(N= 0~7)	Capture Rise Lock Register
CFLR	0x0074+N*0x20(N= 0~7)	Capture Fall Lock Register

3.6.5. Register Description

3.6.5.1. PWM IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: PWM_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PCIE7. PWM channel 7 Interrupt Enable. 0: PWM channel 7 Interrupt Disable 1: PWM channel 7 Interrupt Enable
6	R/W	0x0	PCIE6. PWM channel 6 Interrupt Enable. 0: PWM channel 6 Interrupt Disable 1: PWM channel 6 Interrupt Enable
5	R/W	0x0	PCIE5. PWM channel 5 Interrupt Enable. 0: PWM channel 5 Interrupt Disable 1: PWM channel 5 Interrupt Enable
4	R/W	0x0	PCIE4. PWM channel 4 Interrupt Enable. 0: PWM channel 4 Interrupt Disable 1: PWM channel 4 Interrupt Enable
3	R/W	0x0	PCIE3. PWM channel 3 Interrupt Enable. 0: PWM channel 3 Interrupt Disable 1: PWM channel 3 Interrupt Enable
2	R/W	0x0	PCIE2. PWM channel 2 Interrupt Enable. 0: PWM channel 2 Interrupt Disable 1: PWM channel 2 Interrupt Enable
1	R/W	0x0	PCIE1. PWM channel 1 Interrupt Enable. 0: PWM channel 1 Interrupt Disable 1: PWM channel 1 Interrupt Enable
0	R/W	0x0	PCIE0. PWM channel 0 Interrupt Enable. 0: PWM channel 0 Interrupt Disable 1: PWM channel 0 Interrupt Enable

3.6.5.2. PWM IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PWM_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	PIS7. PWM channel 7 Interrupt Status. When PWM channel 7 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 7 interrupt is not pending. 1: PWM channel 7 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 7 interrupt status.
6	R/W1C	0x0	PIS6. PWM channel 6 Interrupt Status. When PWM channel 6 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 6 interrupt is not pending. 1: PWM channel 6 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 6 interrupt status.
5	R/W1C	0x0	PIS5. PWM channel 5 Interrupt Status. When PWM channel 5 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 5 interrupt is not pending. 1: PWM channel 5 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 5 interrupt status.
4	R/W1C	0x0	PIS4. PWM channel 4 Interrupt Status. When PWM channel 4 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 4 interrupt is not pending. 1: PWM channel 4 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 4 interrupt status.
3	R/W1C	0x0	PIS3. PWM channel 3 Interrupt Status. When PWM channel 3 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 3 interrupt is not pending. 1: PWM channel 3 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 3 interrupt status.
2	R/W1C	0x0	PIS2. PWM channel 2 Interrupt Status. When PWM channel 2 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 2 interrupt is not pending.

Offset: 0x0004			Register Name: PWM_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: PWM channel 2 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 2 interrupt status.
1	R/W1C	0x0	PIS1. PWM channel 1 Interrupt Status. When PWM channel 1 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 1 interrupt is not pending. 1: PWM channel 1 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 1 interrupt status.
0	R/W1C	0x0	PIS0. PWM channel 0 Interrupt Status. When PWM channel 0 counter reaches Entire Cycle Value, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: PWM channel 0 interrupt is not pending. 1: PWM channel 0 interrupt is pending. Writes 0: No effect. 1: Clear PWM channel 0 interrupt status.

NOTE

The active cycles should be no larger than the period cycles.

3.6.5.3. Capture IRQ Enable Register (Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CAPTURE_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	CFIE7. If this enable bit is set to 1, when capture channel 7 captures falling edge, it generates a capture channel 7 pending. 0: Capture channel 7 fall lock interrupt disable 1: Capture channel 7 fall lock interrupt enable
14	R/W	0x0	CRIE7. If this enable bit is set to 1, when capture channel 7 captures rising edge, it generates a capture channel 7 pending. 0: Capture channel 7 rise lock interrupt disable 1: Capture channel 7 rise lock interrupt enable
13	R/W	0x0	CFIE6. If this enable bit is set to 1, when capture channel 6 captures falling edge, it generates a capture channel 6 pending. 0: Capture channel 6 fall lock interrupt disable 1: Capture channel 6 fall lock interrupt enable
12	R/W	0x0	CRIE6. If this enable bit is set to 1, when capture channel 6 captures rising edge, it generates a capture channel 6 pending.

Offset: 0x0010			Register Name: CAPTURE_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Capture channel 6 rise lock interrupt disable 1: Capture channel 6 rise lock interrupt enable
11	R/W	0x0	CFIE5. If this enable bit is set to 1, when capture channel 5 captures falling edge, it generates a capture channel 5 pending. 0: Capture channel 5 fall lock interrupt disable 1: Capture channel 5 fall lock interrupt enable
10	R/W	0x0	CRIE5. If this enable bit is set to 1, when capture channel 5 captures rising edge, it generates a capture channel 5 pending. 0: Capture channel 5 rise lock interrupt disable 1: Capture channel 5 rise lock interrupt enable
9	R/W	0x0	CFIE4. If this enable bit is set to 1, when capture channel 4 captures falling edge, it generates a capture channel 4 pending. 0: Capture channel 4 fall lock interrupt disable 1: Capture channel 4 fall lock interrupt enable
8	R/W	0x0	CRIE4. If this enable bit is set to 1, when capture channel 4 captures rising edge, it generates a capture channel 4 pending. 0: Capture channel 4 rise lock interrupt disable 1: Capture channel 4 rise lock interrupt enable
7	R/W	0x0	CFIE3. If this enable bit is set to 1, when capture channel 3 captures falling edge, it generates a capture channel 3 pending. 0: Capture channel 3 fall lock interrupt disable 1: Capture channel 3 fall lock interrupt enable
6	R/W	0x0	CRIE3. If this enable bit is set to 1, when capture channel 3 captures rising edge, it generates a capture channel 3 pending. 0: Capture channel 3 rise lock interrupt disable 1: Capture channel 3 rise lock interrupt enable
5	R/W	0x0	CFIE2. If this enable bit is set to 1, when capture channel 2 captures falling edge, it generates a capture channel 2 pending. 0: Capture channel 2 fall lock interrupt disable 1: Capture channel 2 fall lock interrupt enable
4	R/W	0x0	CRIE2. If this enable bit is set to 1, when capture channel 2 captures rising edge, it generates a capture channel 2 pending. 0: Capture channel 2 rise lock interrupt disable 1: Capture channel 2 rise lock interrupt enable
3	R/W	0x0	CFIE1. If this enable bit is set to 1, when capture channel 1 captures falling edge, it generates a capture channel 1 pending.

Offset: 0x0010			Register Name: CAPTURE_IRQ_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Capture channel 1 fall lock interrupt disable 1: Capture channel 1 fall lock interrupt enable
2	R/W	0x0	CRIE1. If this enable bit is set 1, when capture channel 1 captures rising edge, it generates a capture channel 1 pending. 0: Capture channel 1 rise lock Interrupt disable 1: Capture channel 1 rise lock Interrupt enable
1	R/W	0x0	CFIE0. If this enable bit is set to 1, when capture channel 0 captures falling edge, it generates a capture channel 0 pending. 0: Capture channel 0 fall lock interrupt disable 1: Capture channel 0 fall lock interrupt enable
0	R/W	0x0	CRIE0. If this enable bit is set to 1, when capture channel 0 captures rising edge, it generates a capture channel 0 pending. 0: Capture channel 0 rise lock interrupt disable 1: Capture channel 0 rise lock interrupt enable

3.6.5.4. Capture IRQ Status Register (Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CAPTURE_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
15	R/W1C	0x0	CFIS7. Capture channel 7 falling lock interrupt status. When capture channel 7 captures falling edge, if capture channel 7 fall lock interrupt (**CFIE7**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 7 interrupt status.
14	R/W1C	0x0	CRIS7. Capture channel 7 rising lock interrupt status. When capture channel 7 captures rising edge, if capture channel 7 rise lock interrupt (**CRIE7**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 7 interrupt is not pending. 1: Capture channel 7 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 7 interrupt status.
13	R/W1C	0x0	CFIS6. Capture channel 6 falling lock interrupt status. When capture channel 6 captures falling edge, if capture channel 6 fall lock interrupt (**CFIE6**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit.

Offset: 0x0014			Register Name: CAPTURE_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 6 interrupt status.
12	R/W1C	0x0	CRIS6. Capture channel 6 rising lock interrupt status. When capture channel 6 captures rising edge, if capture channel 6 rise lock interrupt (**CRIE6**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 6 interrupt is not pending. 1: Capture channel 6 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 6 interrupt status.
11	R/W1C	0x0	CFIS5. Capture channel 5 falling lock interrupt status. When capture channel 5 captures falling edge, if capture channel 5 fall lock interrupt (**CFIE5**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 5 interrupt status.
10	R/W1C	0x0	CRIS5. Capture channel 5 rising lock interrupt status. When capture channel 5 captures rising edge, if capture channel 5 rise lock interrupt (**CRIE5**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 5 interrupt is not pending. 1: Capture channel 5 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 5 interrupt status.
9	R/W1C	0x0	CFIS4. Capture channel 4 falling lock interrupt status. When capture channel 4 captures falling edge, if capture channel 4 fall lock interrupt (**CFIE4**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 4 interrupt status.
8	R/W1C	0x0	CRIS4. Capture channel 4 rising lock interrupt status. When capture channel 4 captures rising edge, if capture channel 4 rise lock interrupt (**CRIE4**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 4 interrupt is not pending. 1: Capture channel 4 interrupt is pending. Writes 0: no effect. 1: Clear capture channel 4 interrupt status.

Offset: 0x0014			Register Name: CAPTURE_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W1C	0x0	CFIS3. Capture channel 3 falling lock interrupt status. When capture channel 3 captures falling edge, if capture channel 3 fall lock interrupt (**CFIE3**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 3 interrupt status.
6	R/W1C	0x0	CRIS3. Capture channel 3 rising lock interrupt status. When capture channel 3 captures rising edge, if capture channel 3 rise lock interrupt (**CRIE3**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 3 interrupt is not pending. 1: Capture channel 3 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 3 interrupt status.
5	R/W1C	0x0	CFIS2. Capture channel 2 falling lock interrupt status. When capture channel 2 captures falling edge, if capture channel 2 fall lock interrupt (**CFIE2**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 2 interrupt status.
4	R/W1C	0x0	CRIS2. Capture channel 2 rising lock interrupt status. When capture channel 2 captures rising edge, if capture channel 2 rise lock interrupt (**CRIE2**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 2 interrupt is not pending. 1: Capture channel 2 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 2 interrupt status.
3	R/W1C	0x0	CFIS1. Capture channel 1 falling lock interrupt status. When capture channel 1 captures falling edge, if capture channel 1 fall lock interrupt (**CFIE1**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 1 interrupt status.
2	R/W1C	0x0	CRIS1. Capture channel 1 rising lock interrupt status. When capture channel 1 captures rising edge, if capture channel 1 rise lock interrupt (**CRIE1**) is enabled, this bit is set to 1 by hardware.

Offset: 0x0014			Register Name: CAPTURE_IRQ_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Write 1 to clear this bit. Reads 0: Capture channel 1 interrupt is not pending. 1: Capture channel 1 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 1 interrupt status.
1	R/W1C	0x0	CFIS0. Capture channel 0 falling lock interrupt status. When capture channel 0 captures falling edge, if capture channel 0 fall lock interrupt (**CFIE0**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 0 interrupt status.
0	R/W1C	0x0	CRIS0. Capture channel 0 rising lock interrupt status. When capture channel 0 captures rising edge, if capture channel 0 rise lock interrupt (**CRIE0**) is enabled, this bit is set to 1 by hardware. Write 1 to clear this bit. Reads 0: Capture channel 0 interrupt is not pending. 1: Capture channel 0 interrupt is pending. Writes 0: No effect. 1: Clear capture channel 0 interrupt status.

3.6.5.5. PWM01 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PWM01_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x00	PWM01_CLK_SRC. Select PWM01 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM1. Bypass PWM01 clock source to PWM1 output. 0: Not bypass 1: Bypass
5	R/W	0x0	PWM01_CLK_SRC_BYPASS_TO_PWM0. Bypass PWM01 clock source to PWM0 output. 0: Not bypass 1: Bypass
4	R/W	0x0	PWM01_CLK_GATING. Gating clock for PWM01. 0: Mask

Offset: 0x0020			Register Name: PWM01_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Pass
3:0	R/W	0x0	PWM01_CLK_DIV_M. PWM01 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

3.6.5.6. PWM23 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PWM23_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM23_CLK_SRC_SEL. Select PWM23 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM3. Bypass PWM23 clock source to PWM3 output. 0: Not bypass 1: Bypass
5	R/W	0x0	PWM23_CLK_SRC_BYPASS_TO_PWM2. Bypass PWM23 clock source to PWM2 output. 0: Not bypass 1: Bypass
4	R/W	0x0	PWM23_CLK_GATING Gating clock for PWM23. 0: Mask 1: Pass
3:0	R/W	0x0	PWM23_CLK_DIV_M. PWM23 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128

Offset: 0x0024			Register Name: PWM23_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1000: /256 others: /

3.6.5.7. PWM45 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: PWM45_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM45_CLK_SRC_SEL. Select PWM45 clock source. 00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM5. Bypass PWM45 clock source to PWM5 output. 0: Not bypass 1: Bypass
5	R/W	0x0	PWM45_CLK_SRC_BYPASS_TO_PWM4. Bypass PWM45 clock source to PWM4 output. 0: Not bypass 1: Bypass
4	R/W	0x0	PWM45_CLK_GATING. Gating clock for PWM45. 0: Mask 1: Pass
3:0	R/W	0x0	PWM45_CLK_DIV_M. PWM45 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

3.6.5.8. PWM67 Clock Configuration Register (Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: PWM67_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	PWM67_CLK_SRC_SEL. Select PWM67 clock source.

Offset: 0x002C			Register Name: PWM67_CLK_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			00: 24M_PLL 01: APB1 Others: /
6	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM7. Bypass PWM67 clock source to PWM7 output. 0: Not bypass 1: Bypass
5	R/W	0x0	PWM67_CLK_SRC_BYPASS_TO_PWM6. Bypass PWM67 clock source to PWM6 output. 0: Not bypass 1: Bypass
4	R/W	0x0	PWM67_CLK_GATING. Gating clock for PWM67. 0: Mask 1: Pass
3:0	R/W	0x0	PWM67_CLK_DIV_M. PWM67 clock divide M 0000: /1 0001: /2 0010: /4 0011: /8 0100: /16 0101: /32 0110: /64 0111: /128 1000: /256 others: /

3.6.5.9. PWM01 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PWM01_DZ_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PDZINTV01. PWM01 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM01_DZ_EN. PWM01 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

3.6.5.10. PWM23 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0034	Register Name: PWM23_DZ_CTR_REG

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x0	PWM23_DZ_INTV. PWM23 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM23_DZ_EN. PWM23 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

3.6.5.11. PWM45 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: PWM45_DZ_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM45_DZ_INTV. PWM45 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM45_DZ_EN. PWM45 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

3.6.5.12. PWM67 Dead Zone Control Register (Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: PWM67_DZ_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	PWM67_DZ_INTV. PWM67 Dead Zone interval value.
7:1	/	/	/
0	R/W	0x0	PWM67_DZ_EN. PWM67 Dead Zone enable. 0: Dead Zone disable 1: Dead Zone enable.

3.6.5.13. PWM Enable Register (Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PWM_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PWM7_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel7 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
6	R/W	0x0	PWM6_EN.

Offset: 0x0040			Register Name: PWM_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			When enable PWM, the 16-bit up-counter starts working and PWM channel6 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
5	R/W	0x0	PWM5_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel5 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
4	R/W	0x0	PWM4_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel4 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
3	R/W	0x0	PWM3_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel3 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
2	R/W	0x0	PWM2_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel2 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
1	R/W	0x0	PWM1_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel1 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.
0	R/W	0x0	PWM0_EN. When enable PWM, the 16-bit up-counter starts working and PWM channel0 is permitted to output PWM waveform. 0: PWM disable 1: PWM enable.

3.6.5.14. Capture Enable Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: CAPTURE_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	CAP7_EN. When enable capture function, the 16-bit up-counter starts working and capture channel7 is permitted to capture external falling edge or rising edge.

Offset: 0x0044			Register Name: CAPTURE_ENABLE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Capture disable 1: Capture enable.
6	R/W	0x0	CAP6_EN. When enable capture function, the 16-bit up-counter starts working and capture channel6 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
5	R/W	0x0	CAP5_EN. When enable capture function, the 16-bit up-counter starts working and capture channel5 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
4	R/W	0x0	CAP4_EN. When enable capture function, the 16-bit up-counter starts working and capture channel4 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
3	R/W	0x0	CAP3_EN. When enable capture function, the 16-bit up-counter starts working and capture channel3 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
2	R/W	0x0	CAP2_EN. When enable capture function, the 16-bit up-counter starts working and capture channel2 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
1	R/W	0x0	CAP1_EN. When enable capture function, the 16-bit up-counter starts working and capture channel1 is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.
0	R/W	0x0	CAP0_EN. When enable capture function, the 16-bit up-counter starts working and capture channel is permitted to capture external falling edge or rising edge. 0: Capture disable 1: Capture enable.

3.6.5.15. PWM Control Register (Default Value: 0x0000_0000)

Offset: 0x0060+N*0x20(N= 0~7)			Register Name: PWM_CTR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/.
11	R	0x0	PWM_PERIOD_RDY. PWM period register ready. 0: PWM period register is ready to write 1: PWM period register is busy.
10	R/W1S	0x0	PWM_PUL_START. PWM pulse output start. 0: No effect 1: Output 1 pulse. After finishing configurating for outputting pulse, set this bit once and then PWM would output one pulse. After the pulse is finished, the bit will be cleared automatically.
9	R/W	0x0	PWM_MODE. PWM output mode select. 0: Cycle mode 1: Pulse mode.
8	R/W	0x0	PWM_ACT_STA. PWM active state. 0: Low Level 1: High Level.
7:0	R/W	0x0	PWM_PRESCAL_K. PWM pre-scale K, actual pre-scale is (K+1). K = 0, actual pre-scale: 1 K = 1, actual pre-scale: 2 K = 2, actual pre-scale: 3 K = 3, actual pre-scale: 4 …… K = 255, actual pre-scale: 256.

3.6.5.16. PWM Period Register (Default Value: 0x0000_0000)

Offset: 0x0064+N*0x20(N=0~7)			Register Name: PWM_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	PWM_ENTIRE_CYCLE. Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK .
15:0	R/W	0x0	PWM _ACT_CYCLE. Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles

Offset: 0x0064+N*0x20(N=0~7)			Register Name: PWM_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
			…… N = N cycles

3.6.5.17. PWM Counter Register (Default Value: 0x0000_0000)

Offset: 0x0068+N*0x20(N=0~7)			Register Name: PWM_CTR_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	On PWM output or capture input, reading this register could get the current value of the PWM 16bit up-counter.

3.6.5.18. Capture Control Register (Default Value: 0x0000_0000)

Offset: 0x006C+N*0x20(N=0~7)			Register Name: CAPTURE_CTR_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	CRLF. When capture channel captures rising edge, the 16-bit up-counter's current value is latched to **CRLR** and then this bit is set to 1 by hardware. Write 1 to clear this bit.
1	R/W	0x0	CFLF. When capture channel captures falling edge, the 16-bit up-counter's current value is latched to **CFLR** and then this bit is set to 1 by hardware. Write 1 to clear this bit.
0	R/W	0x0	CAPINV. Inversing the signal inputted form capture channel before capture channel's 16bit counter. 0: Not inverse 1: Inverse

3.6.5.19. Capture Rise Lock Register (Default Value: 0x0000_0000)

Offset: 0x0070+N*0x20(N=0~7)			Register Name: CAPTURE_RISE_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CRLR When capture channel captures rising edge, the 16-bit up-counter's current value is latched to this register.

3.6.5.20. Capture Fall Lock Register (Default Value: 0x0000_0000)

Offset: 0x0074+N*0x20(N=0~7)			Register Name: CAPTURE_FALL_REG
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R	0x0	CFLR When capture channel captures falling edge, the 16-bit up-counter's

Offset: 0x0074+N*0x20(N=0~7)			Register Name: CAPTURE_FALL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			current value is latched to this register.

3.7. Timer

3.7.1. Overview

The timer module implements the timing and counting functions.The timer module includes timer0,timer1,timer2, timer3,timer4 and timer5,watchdog and AVS.

The timer0/1/2/3/4/5 are completely consistent.The timer0/1/2/3/4/5 has the following features:

- Configurable count clock: LOSC and OSC24M. LOSC is the internal low-frequency clock or the external low-frequency clock by setting LOSC_SRC_SEL. The external low-frequency has much accuracy.
- Configurable 8 prescale factor
- Programmable 32-bit down timer
- Two working modes: continue mode and single count mode
- Generates an interrupt when the count is decreased to 0

The watchdog is used to transimit a reset signal to reset the entire system after an exception occurs in the system.The watchdog has the following features:

- Single clock source: OSC24M/750
- 12 initial values to configure
- Generation of timeout interrupts
- Generation of reset signal
- Watchdog restart the timing

The AVS is used to the synchronization of audio and video. The AVS module includes AVS0 and AVS1, the AVS0 and AVS1 are completely consistent.The AVS has the following features:

- Single clock source: OSC24M
- Programmable 33-bit up timer
- Initial value can be updated anytime
- 12-bit frequency divider factor
- Pause/Start function

3.7.2. Block Diagram

The block diagram of the Timer is as follows.

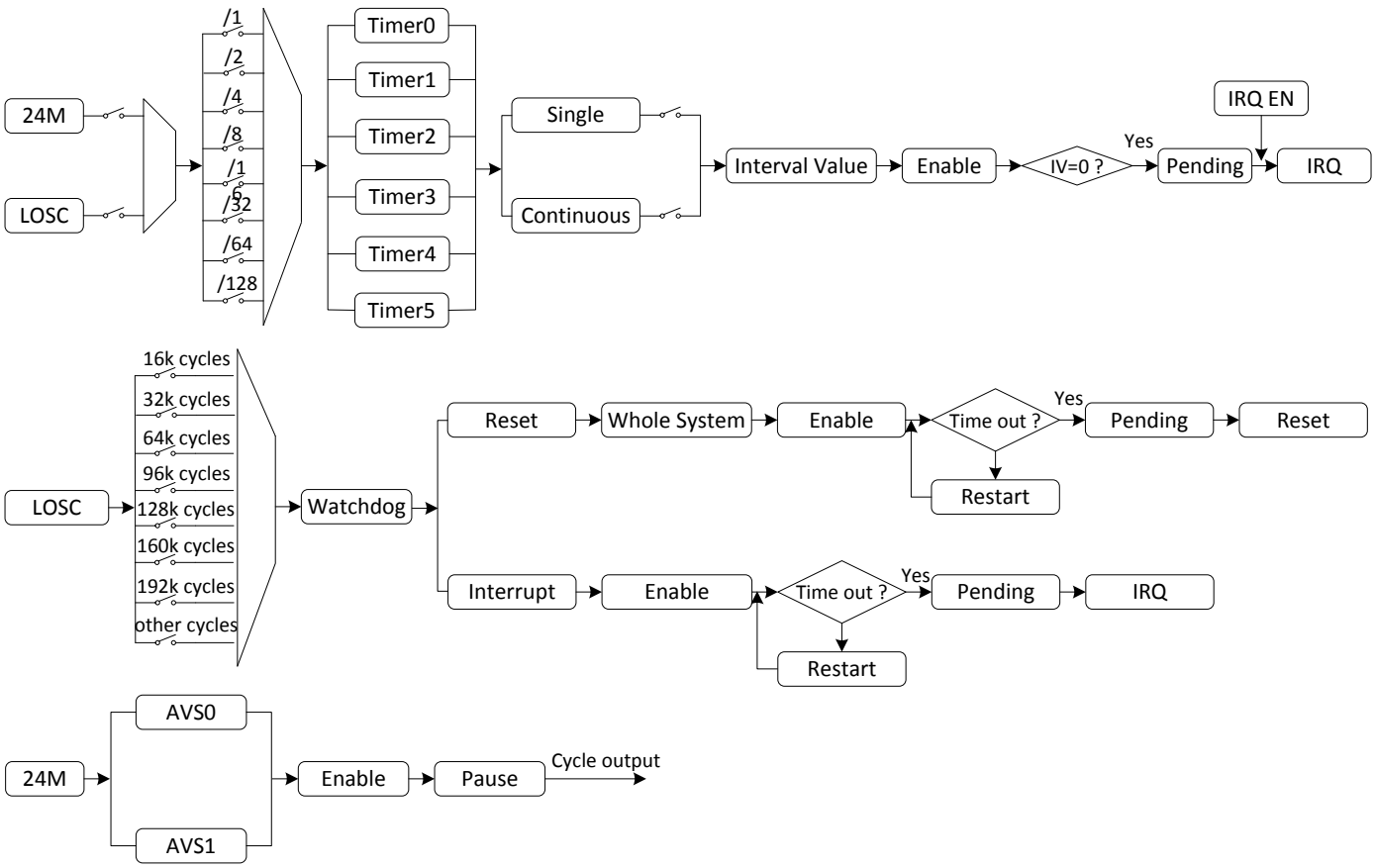


Figure 3-15. Timer Block Diagram

3.7.3. Operations and Functional Descriptions

3.7.3.1. Timer Formula

$$T_{timer0} = \frac{TMR0\_INTV\_VALUE\_REG - TMR0\_CUR\_VALUE\_REG}{TMR0\_CLK\_SRC} \times TMR0\_CLK\_PRES$$

TMR0_INTV_VALUE_REG: timer initial value;
TMR0_CUR_VALUE_REG: timer current counter;
TMR0_CLK_SRC: timer clock source;
TMR0_CLK_PRES: timer clock prescale ratio.

3.7.3.2. Typical Application

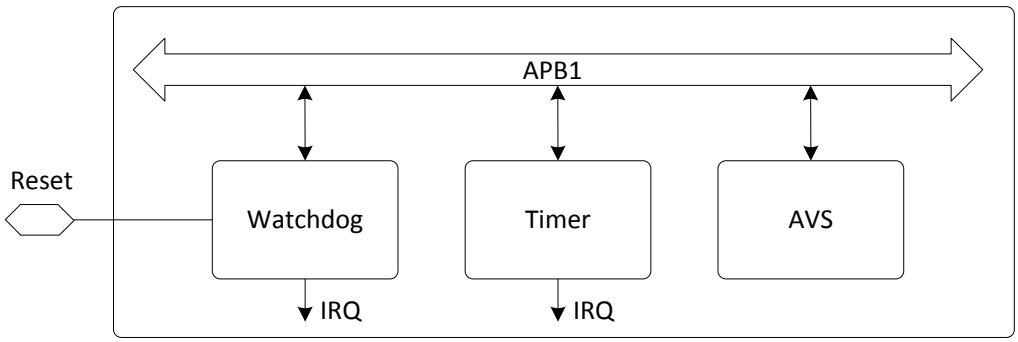


Figure 3-16. Timer Application Diagram

3.7.3.3. Function Implemention

(1).Timer

The timer is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock. Each timer has independent interrupt.

The timer has two operating modes.

- **Continuous mode**

The bit7 of the TMRn_CTRL_REG is set to the continuous mode, when the count value is decreased to 0, the timer module reloads data from TMRn_INTV_VALUE_REG then continues to count.

- **Single mode**

The bit7 of the TMRn_CTRL_REG is set to the single mode, when the count value is decreased to 0, the timer stops counting. The timer starts to count again only when a new initial value is loaded.

Each timer has a prescaler that divides the working clock frequency of each timer by 1,2,4,8,16,32,64,128.

(2).Watchdog

The watchdog is a 32-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.
The watchdog supports reset modes.
The bit1 of WDOG_MODE_REG is set to 0x1, when the counter value reaches 0, the watchdog generates a reset signal to reset the entire system.
The clock source of the watchdog is LOSC.There are 12 configurable initial count values.
The watchdog can restart to count by setting **WDOG0_CTRL_REG**: write 0xA57 to bit[12:1],then write 1 to bit[0].

(3).AVS

The AVS is a 33-bit up counter.The counter value is increased by 1 on each rising edge of the count clock.
The AVS can be operated after its clock gating in CCU module is opened.
The AVS has an OSC24M clock source and a 12-bit division factor N. When the timer increases to N from 0, AVS counter adds 1; when the counter reaches 33-bit upper limit,the AVS will start to count from initial value again.
In counter working process, the division factor and initial counter of the AVS can be changed anytime.And the AVS can stop or start to operate counter anytime.

3.7.4. Programming Guidelines

3.7.4.1. Timer

Take making a 1ms delay for an example, 24M clock source, single mode and 2 pre-scale will be selected in the instance.

```
writel(0x2EE0,TMR_0_INTV);                  //Set interval value
writel(0x94, TMR_0_CTRL);                   //Select Single mode,24MHz clock source,2 pre-scale
writel(readl(TMR_0_CTRL)|(1<<1), TMR_0_CTRL);  //Set Reload bit
while((readl(TMR_0_CTRL)>>1)&1);            //Waiting Reload bit turns to 0
writel(readl(TMR_0_CTRL)|(1<<0), TMR_0_CTRL);  //Enable Timer0
```

If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0.
If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1.
In timer pause state, the interval value register can be modified. If the timer is started again, and the software hopes the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.7.4.2. Watchdog Reset

In the following instance making configurations for Watchdog: configurate Interval Value as 1s and configurate Watchdog Configuration as To whole system. This instance indicates that reset system after 1s.

```
writel(readl(WDOG_MODE) | (1<<1), WDOG_MODE);  //To whole system
writel(readl(WDOG_MODE) | (1<<3), WDOG_MODE);  //Interval Value set 1s
writel(readl(WDOG_MODE) | (1<<0), WDOG_MODE);  //Enable Watchdog
```

3.7.4.3. Watchdog Restart

In the following instance making configurations for Watchdog: configurate Interval Value as 1s and configurate Watchdog Configuration as To whole system. In the following instance, if the time of other codes is larger than 1s, watchdog will reset the whole system. If the sentence of restart watchdog is implemented inside 1s, watchdog will be restarted.

```
writel(readl(WDOG_MODE) | (1<<1), WDOG_MODE);  //To whole system
writel(readl(WDOG_MODE) | (1<<3), WDOG_MODE);  //Interval Value set 1s
writel(readl(WDOG_MODE) | (1<<0), WDOG_MODE);  //Enable Watchdog
----other codes---
writel(readl(WDOG_CTRL) | (0xA57<<1) | (1<<0)， WDOG_CTRL); //Writel 0xA57 at Key Field and Restart Watchdog
```

3.7.5. Register List

Module Name	Base Address
Timer	0x01C20C00

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x0004	Timer Status Register

Register Name	Offset	Description
TMR0_CTRL_REG	0x0010	Timer 0 Control Register
TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value Register
TMR0_CUR_VALUE_REG	0x0018	Timer 0 Current Value Register
TMR1_CTRL_REG	0x0020	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x0028	Timer 1 Current Value Register
TMR2_CTRL_REG	0x0030	Timer 2 Control Register
TMR2_INTV_VALUE_REG	0x0034	Timer 2 Interval Value Register
TMR2_CUR_VALUE_REG	0x0038	Timer 2 Current Value Register
TMR3_CTRL_REG	0x0040	Timer 3 Control Register
TMR3_INTV_VALUE_REG	0x0044	Timer 3 Interval Value Register
TMR4_CTRL_REG	0x0050	Timer 4 Control Register
TMR4_INTV_VALUE_REG	0x0054	Timer 4 Interval Value Register
TMR4_CUR_VALUE_REG	0x0058	Timer 4 Current Value Register
TMR5_CTRL_REG	0x0060	Timer 5 Control Register
TMR5_INTV_VALUE_REG	0x0064	Timer 5 Interval Value Register
TMR5_CUR_VALUE_REG	0x0068	Timer 5 Current Value Register
AVS_CNT_CTL_REG	0x0080	AVS Control Register
AVS_CNT0_REG	0x0084	AVS Counter 0 Register
AVS_CNT1_REG	0x0088	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x008C	AVS Divisor Register
WDOG_CTRL_REG	0x0090	Watchdog Control Register
WDOG_MODE_REG	0x0094	Watchdog Mode Register

3.7.6. Register Description

3.7.6.1. Timer IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	WDOG_IRQ_EN. Watchdog Interrupt Enable. 0: No effect 1: Watchdog Interval Value reached interrupt enable.
7:6	/	/	/
5	R/W	0x0	TMR5_IRQ_EN. Timer 5 Interrupt Enable. 0: No effect 1: Timer 5 Interval Value reached interrupt enable.
4	R/W	0x0	TMR4_IRQ_EN. Timer 4 Interrupt Enable. 0: No effect 1: Timer 4 Interval Value reached interrupt enable.
3	R/W	0x0	TMR3_IRQ_EN. Timer 3 Interrupt Enable.

Offset: 0x0000			Register Name: TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No effect 1: Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	TMR2_IRQ_EN. Timer 2 Interrupt Enable. 0: No effect 1: Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	TMR1_IRQ_EN. Timer 1 Interrupt Enable. 0: No effect 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	TMR0_IRQ_EN. Timer 0 Interrupt Enable. 0: No effect 1: Timer 0 Interval Value reached interrupt enable.

3.7.6.2. Timer IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/.
8	R/W1C	0x0	WDOG_IRQ_PEND. Watchdog IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, Watchdog counter value is reached.
7:6	/	/	/
5	R/ W1C	0x0	TMR5_IRQ_PEND. Timer 5 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 5 counter value is reached.
4	R/W1C	0x0	TMR4_IRQ_PEND. Timer 4 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 4 counter value is reached.
3	R/W1C	0x0	TMR3_IRQ_PEND. Timer 3 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 3 counter value is reached.
2	R/W1C	0x0	TMR2_IRQ_PEND. Timer 2 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 2 counter value is reached.
1	R/W1C	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Setting 1 to the bit will clear it.

Offset: 0x0004			Register Name: TMR_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No effect 1: Pending, timer 1 interval value is reached.
0	R/W1C	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached.

3.7.6.3. Timer 0 Control Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7	R/W	0x0	TMR0_MODE. Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR0_CLK_PRES. Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer 0 Clock Source. 00: Low speed OSC, 01: OSC24M. 10: PLL_PERIPH0_1X/36 11: /.
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect 1: Reload timer 0 Interval value.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the

Offset: 0x0010			Register Name: TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

NOTE

The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

3.7.6.4. Timer 0 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TMR0_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_INTV_VALUE. Timer 0 Interval Value.

NOTE

The value setting should consider the system clock and the timer clock source.

3.7.6.5. Timer 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TMR0_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

NOTE

Timer 0 current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).

3.7.6.6. Timer 1 Control Register(Default Value: 0x0000_0004)

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.
7	R/W	0x0	TMR1_MODE. Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2

Offset: 0x0020			Register Name: TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer 1 Clock Source. 00: Low speed OSC 01: OSC24M. 10: PLL6/6 11: /.
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect 1: Reload timer 1 Interval value.
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

NOTE

The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

3.7.6.7. Timer 1 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: TMR1_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR1_INTV_VALUE. Timer 1 Interval Value.

NOTE

The value setting should take into consideration the system clock and the timer clock source.

3.7.6.8. Timer 1 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0028	Register Name: TMR1_CUR_VALUE_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

NOTE

Timer 1 current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).

3.7.6.9. Timer 2 Control Register(Default Value: 0x0000_0004)

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7	R/W	0x0	TMR2_MODE. Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR2_CLK_PRES. Select the pre-scale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer 2 Clock Source. 00: Low speed OSC 01: OSC24M. 1x: /.
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect 1: Reload timer 2 Interval value.
0	R/W	0x0	TMR2_EN. Timer 2 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to

Offset: 0x0030			Register Name: TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
			down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

NOTE

The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

3.7.6.10. Timer 2 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TMR2_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_INTV_VALUE. Timer 2 Interval Value.

NOTE

The value setting should consider the system clock and the timer clock source.

3.7.6.11. Timer 2 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: TMR2_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR2_CUR_VALUE. Timer 2 Current Value.

NOTE

Timer current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).

3.7.6.12. Timer 3 Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/.
4	R/W	0x0	TMR3_MODE. Timer 3 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
3:2	R/W	0x0	TMR3_CLK_PRES. Select the pre-scale of timer 3 clock source. Timer 3 clock source is the LOSC. 00: /16 01: /32 10: /64 11: /
1	/	/	/

Offset: 0x0040			Register Name: TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
0	R/W	0x0	TMR3_EN. Timer 3 Enable. 0: Disable 1: Enable.

NOTE

The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

3.7.6.13. Timer 3 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: TMR3_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR3_INTV_VALUE. Timer 3 Interval Value.

3.7.6.14. Timer 4 Control Register(Default Value: 0x0000_0004)

Offset: 0x0050			Register Name: TMR4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.
7	R/W	0x0	TMR4_MODE. Timer 4 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR4_CLK_PRES. Select the pre-scale of timer 4 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR4_CLK_SRC. Timer 4 Clock Source. 00: Low speed OSC 01: OSC24M. 10: External CLKIN0 11: /.
1	R/W	0x0	TMR4_RELOAD. Timer 4 Reload. 0: No effect

Offset: 0x0050			Register Name: TMR4_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Reload timer 4 Interval value.
0	R/W	0x0	TMR4_EN. Timer 4 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

NOTE

If the clock source is external CLKIN, the interval value register is not used, the current value register is an up counter that counting from 0.
The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

3.7.6.15. Timer 4 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: TMR4_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR4_INTV_VALUE. Timer 4 Interval Value. **The value setting should take the system clock and the timer clock source into consideration.**

3.7.6.16. Timer 4 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: TMR4_CUR_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TMR4_CUR_VALUE. Timer 4 Current Value.

NOTE

Timer current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).
Before the timer 4 is enabled, the timer 4 current value register needs to be written to zero.

3.7.6.17. Timer 5 Control Register(Default Value: 0x0000_0004)

Offset: 0x0060			Register Name: TMR5_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/.
7	R/W	0x0	TMR5_MODE. Timer 5 mode.

Offset: 0x0060			Register Name: TMR5_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	TMR5_CLK_PRES. Select the pre-scale of timer 5 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR5_CLK_SRC. Timer 5 Clock Source. 00: Low speed OSC 01: OSC24M. 10: External CLKIN1 11: /.
1	R/W	0x0	TMR5_RELOAD. Timer 5 Reload. 0: No effect 1: Reload timer 5 Interval value.
0	R/W	0x0	TMR5_EN. Timer 5 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

NOTE

If the clock source is External CLKIN, the interval value register is not used, the current value register is an up counter that counts from 0.

The time between the timer disabled and enabled should be larger than 2*Tcycles(Tcycles= Timer clock source/pre-scale).

3.7.6.18. Timer 5 Interval Value Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: TMR5_INTV_VALUE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0064			Register Name: TMR5_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR5_INTV_VALUE. Timer 5 Interval Value. **When you set the value, please take into consideration the system clock and the timer clock source.**

3.7.6.19. Timer 5 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: TMR5_CUR_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR5_CUR_VALUE. Timer 5 Current Value.

NOTE

Timer 1 current value is a 32-bit down-counter(from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq(TimerFreq = TimerClkSource/pre-scale).
Before timer 5 is enabled, timer 5 current value register needs to be written to zero.

3.7.6.20. AVS Counter Control Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: AVS_CNT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 1 Enable/Disable. The counter source is OSC24M. 0: Disable 1: Enable

3.7.6.21. AVS Counter 0 Register(Default Value: 0x0000_0000)

Offset: 0x0084	Register Name: AVS_CNT0_REG

Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting **AVS_CNT0_PS** to '1'. When it is paused, the counter won't increase.

3.7.6.22. AVS Counter 1 Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: AVS_CNT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bit counter register can be set by software. The LSB bit of the 33-bit counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting **AVS_CNT1_PS** to '1'. When it is paused, the counter will not increase.

3.7.6.23. AVS Counter Divisor Register(Default: 0x05DB_05DB)

Offset: 0x008C			Register Name: AVS_CNT_DIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter1 AVS CN1 CLK=24MHz/Divisor_N1. Divisor N1 = Bit[27:16] + 1. The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again. **NOTE** **It can be configured by software at any time.**
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter0 AVS CN0 CLK=24MHz/Divisor_N0. Divisor N0 = Bit[11:0] + 1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bit counter engine will maintain another 12-bit counter. The 12-bit counter is used for counting the cycle number of one 24MHz clock. When the 12-bit counter reaches (>= N) the divisor value, the internal 33-bit counter register will increase 1 and the 12-bit counter will reset to zero and restart again.

Offset: 0x008C			Register Name: AVS_CNT_DIV_REG
Bit	Read/Write	Default/Hex	Description
			NOTE It can be configured by software at any time.

3.7.6.24. Watchdog Control Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: WDOG_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:1	R/W	0x0	WDOG_KEY_FIELD Watchdog Key Field. Should be written 0xA57.Writing any other value in this field aborts the writing operation.
0	R/W	0x0	WDOG_RSTART. Watchdog Restart. 0: No effect 1: Restart the Watchdog.

3.7.6.25. Watchdog Mode Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: WDOG_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:3	R/W	0x0	WDOG_INTV_VALUE. Watchdog Interval Value Watchdog clock source is LOSC. If the LOSC is turned off, the watchdog will not work. 0000: 0.5sec 0001: 1sec 0010: 2sec 0011: 3sec 0100: 4sec 0101: 5sec 0110: 6sec 0111: 8sec 1000: 10sec 1001: 12sec 1010: 14sec 1011: 16sec 1100: / 1101: / 1110: / 1111: /
2	/	/	/
1	R/W	0x0	WDOG_RST_EN. Watchdog Reset Enable. 0: No effect on the resets 1: Enables the Watchdog to activate the system reset.

Offset: 0x0094			Register Name: WDOG_MODE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	WDOG_EN. Watchdog Enable. 0: No effect 1: Enable the Watchdog.

3.8. High Speed Timer

3.8.1. Overview

The high speed timer(HSTimer) module implements the timing and counting functions. The clock source of HSTimer0_1_2_3 is fixed to AHBCLK, which is much higher than OSC24M. Compared with other timers, the clock source of HSTimer is synchronized with AHB clock, and when the relevant bit in the Control Register is set to 1, HSTimer goes into the test mode, which is used to system simulation. When the current value in both LO and HI Current Value Register are counting down to zero, the HSTimer will generate interrupt if the interrupt enable bit is set.

The HSTimer has the following features:

- Timing clock is AHB1 that can provides more accurate timing clock
- Configurable 5 prescale factor
- Configurable 56-bit down timer
- Supports 2 working modes: continuous mode and single mode
- Supports test mode
- Generates an interrupt when the count is decreased to 0

3.8.2. Block Diagram

Figure 3-17 shows a block diagram of the HSTimer.

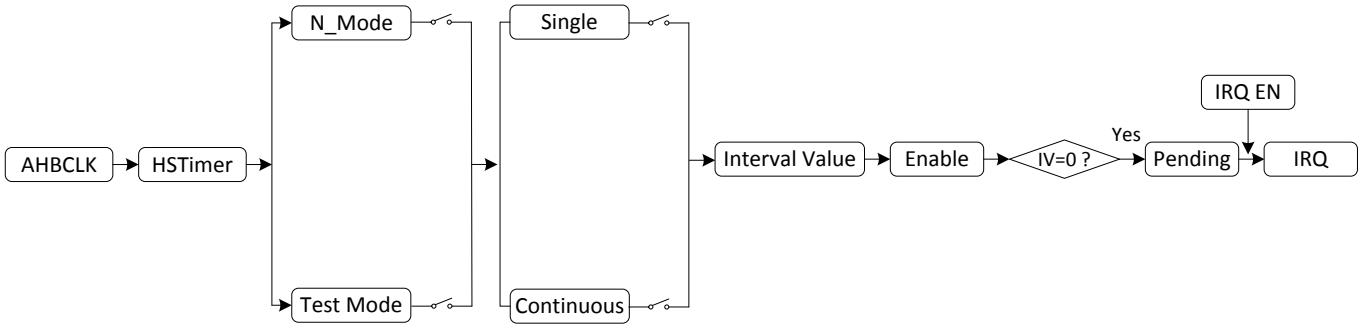


Figure 3-17. HSTimer Block Diagram

3.8.3. Operations and Functional Description

3.8.3.1. HSTimer Formula

$$T_{HSTimer} = \frac{(HS\_TMR\_INTV\_HI\_REG<<32 + HS\_TMR\_INTV\_LO\_REG) - (HS\_TMR\_CURNT\_HI\_REG<<32 + HS\_TMR\_CURNT\_LO\_REG)}{AHB1CLK} \times HS\_TMR\_CLK$$

HS_TMR_INTV_HI_REG: Initial of Counter Higher Bit
HS_TMR_INTV_LO_REG: Initial of Counter Lower Bit
HS_TMR_CURNT_HI_REG: Current Value of Counter Higher Bit
HS_TMR_CURNT_LO_REG: Current Vaule of Counter Lower Bit
AHB1CLK: AHB1 Clock Frequency
HS_TMR_CLK: Time Prescale Ratio of Counter

3.8.3.2. Typical Application

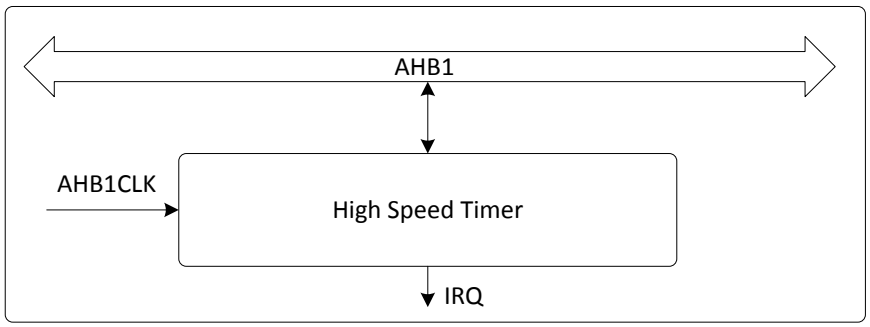


Figure 3-18. HSTimer Application Diagram

The HSTimer is on AHB1, and the HSTimer controls registers by AHB1.
The HSTimer has single clock source: AHB. The HSTimer can generate interrupt.

3.8.3.3. Function Implemention

The HSTimer is a 56-bit down counter, the counter value is decreased by 1 on each rising edge of the count clock.

The HSTimer has two timing modes.

- Continuous mode : The bit7 of **HS_TMR_CTRL_REG** is set to the continuous mode, when the count value is decreased to 0, the HSTimer module reloads data from **HS_TMR_INTV_LO_REG** and **HS_TMR_INTV_HI_REG** , then continues to count.
- Single mode : The bit7 of **HS_TMR_CTRL_REG** is set to the single mode, when the count value is decreased to 0, the HSTimer stops counting. The HSTimer starts to count again only when a new initial value is loaded.

The HSTimer has two operating modes.

- Normal mode: When the bit31 of **HS_TMR_CTRL_REG** is set to the normal mode, the HSTimer is used as 56-bit down counter, which can continuous timing and single timing.
- Test mode: When the bit31 of **HS_TMR_CTRL_REG** is set to the test mode, then **HS_TMR_INTV_LO_REG** must be set to 0x1, the HSTimer is used as 24-bit down counter, and **HS_TMR_INTV_HI_REG** is the initial value of the HSTimer.

Each HSTimer has a prescaler that divides the working clock frequency of each working timer by 1,2,4,8,16.

3.8.3.4. Operating Mode

3.8.3.4.1. Clock Gating and Reset

By default the HSTimer clock gating is mask. When it is necessary to use HSTimer, HSTimer clock gating should be enabled by the bit[19] of **Bus Clock Gating Register 0** and then de-asserted the software reset by the bit[19] of **Bus Software Reset Register 0** in CCU module.If it is no need to use HSTimer, both the gating bit and software reset bit should be set to 0.

3.8.3.4.2. HSTimer Initial

(1) AHB1 clock management: Enable the clock gating of AHB1 and de-assert the soft reset of AHB1 in CCU.
(2) Configure the corresponding parameters of the HSTimer: clock source, prescaler factor, working mode, counting mode. These parameters that are written to **HS_TMR_CTRL_REG** have no sequences.

(3) Write the initial value: Firstly write the low-bit register **HS_TMR_INTV_LO_REG**, then write the high-bit register **HS_TMR_INTV_HI_REG**. Write the bit1 of **HS_TMR_CTRL_REG** to load the initial value. If in timing stop stage of HSTimer, write the bit1 and bit0 of **HS_TMR_CTRL_REG** to reload the initial value.
(4) Enable HSTimer: Write the bit[0] of **HS_TMR_CTRL_REG** to enable HSTimer to count.

3.8.3.4.3. HSTimer Interrupt

(1) Enable interrupt: Write the corresponding interrupt enable bit of **HS_TMR_IRQ_EN_REG**, when the counting time of HSTimer reaches , the corresponding interrupt generates.
(2) After enter the interrupt process, write **HS_TMR_IRQ_STAS_REG** to clear the interrupt pending.
(3) Resume the interrupt and continue to execute the interrupted process.

3.8.3.4.4. HSTimer Reload

Differing from the reload of Timer, when interval value is reloaded into current value register, the reload bit would not turn to 0 automatically until you clear it. If software hopes the current value register to down-count from the new interval value in pause status, the reload bit and the enable bit should be written 1 at the same time.

3.8.4. Programming Guidelines

Take making a 1us delay using HSTimer0 for an instance as follow, AHB1CLK will be configurated as 100MHz and n_mode,single mode and 2 pre-scale will be selected in this instance.

```
writel(0x0, HS_TMR0_INTV_HI);                    //Set interval value Hi 0x0
writel(0x32, HS_TMR0_INTV_LO);                   //Set interval value Lo 0x32
writel(0x90, HS_TMR0_CTRL);                      //Select n_mode,2 pre-scale,single mode
writel(readl(HS_TMR0_CTRL)|(1<<1), HS_TMR0_CTRL);  //Set Reload bit
writel(readl(HS_TMR0_CTRL)|(1<<0), HS_TMR0_CTRL);  //Enable HSTimer0
while(!(readl(HS_TMR_IRQ_STAS)&1));              //Wait for HSTimer0 to generate pending
writel(1,HS_TMR_IRQ_STAS);                       //Clear HSTimer0 pending
```

3.8.5. Register List

Module Name	Base Address
HSTimer	0x01C60000

Register Name	Offset	Description
HS_TMR_IRQ_EN_REG	0x0000	HSTimer IRQ Enable Register
HS_TMR_IRQ_STAS_REG	0x0004	HSTimer Status Register
HS_TMR0_CTRL_REG	0x0010	HSTimer 0 Control Register
HS_TMR0_INTV_LO_REG	0x0014	HSTimer 0 Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x0018	HSTimer 0 Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x001C	HSTimer 0 Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x0020	HSTimer 0 Current Value High Register
HS_TMR1_CTRL_REG	0x0030	HSTimer 1 Control Register
HS_TMR1_INTV_LO_REG	0x0034	HSTimer 1 Interval Value Low Register
HS_TMR1_INTV_HI_REG	0x0038	HSTimer 1 Interval Value High Register

Register Name	Offset	Description
HS_TMR1_CURNT_LO_REG	0x003C	HSTimer 1 Current Value Low Register
HS_TMR1_CURNT_HI_REG	0x0040	HSTimer 1 Current Value High Register
HS_TMR2_CTRL_REG	0x0050	HSTimer 2 Control Register
HS_TMR2_INTV_LO_REG	0x0054	HSTimer 2 Interval Value Low Register
HS_TMR2_INTV_HI_REG	0x0058	HSTimer 2 Interval Value High Register
HS_TMR2_CURNT_LO_REG	0x005C	HSTimer 2 Current Value Low Register
HS_TMR2_CURNT_HI_REG	0x0060	HSTimer 2 Current Value High Register
HS_TMR3_CTRL_REG	0x0070	HSTimer 3 Control Register
HS_TMR3_INTV_LO_REG	0x0074	HSTimer 3 Interval Value Low Register
HS_TMR3_INTV_HI_REG	0x0078	HSTimer 3 Interval Value High Register
HS_TMR3_CURNT_LO_REG	0x007C	HSTimer 3 Current Value Low Register
HS_TMR3_CURNT_HI_REG	0x0080	HSTimer 3 Current Value High Register

3.8.6. Register Description

3.8.6.1. HSTimer IRQ Enable Register(Default Value: 0x0000_0000)

Offset:0x0000			Register Name: HS_TMR_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1S	0x0	HS_TMR3_INT_EN. High Speed Timer 3 Interrupt Enable. 0: No effect 1: High Speed Timer 3 Interval Value reached interrupt enable.
2	R/W1S	0x0	HS_TMR2_INT_EN. High Speed Timer 2 Interrupt Enable. 0: No effect 1: High Speed Timer 2 Interval Value reached interrupt enable.
1	R/W1S	0x0	HS_TMR1_INT_EN. High Speed Timer 1 Interrupt Enable. 0: No effect 1: High Speed Timer 1 Interval Value reached interrupt enable.
0	R/W1S	0x0	HS_TMR0_INT_EN. High Speed Timer 0 Interrupt Enable. 0: No effect 1: High Speed Timer 0 Interval Value reached interrupt enable.

3.8.6.2. HSTimer IRQ Status Register(Default Value: 0x0000_0000)

Offset:0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W1C	0x0	HS_TMR3_IRQ_PEND. High Speed Timer 3 IRQ Pending. Setting 1 to the bit will clear it.

Offset:0x0004			Register Name: HS_TMR_IRQ_STAS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No effect 1: Pending, High speed timer 3 interval value is reached.
2	R/W1C	0x0	HS_TMR2_IRQ_PEND. High Speed Timer 2 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 2 interval value is reached.
1	R/W1C	0x0	HS_TMR1_IRQ_PEND. High Speed Timer 1 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 1 interval value is reached.
0	R/W1C	0x0	HS_TMR0_IRQ_PEND. High Speed Timer 0 IRQ Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending, High speed timer 0 interval value is reached.

3.8.6.3. HSTimer 0 Control Register(Default Value: 0x0000_0000)

Offset:0x0010			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR0_TEST. High speed timer 0 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode.
30:8	/	/	/
7	R/W	0x0	HS_TMR0_MODE. High Speed Timer 0 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W1S	0x0	HS_TMR0_RELOAD. High Speed Timer 0 Reload.

Offset:0x0010			Register Name: HS_TMR0_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No effect 1: Reload High Speed Timer 0 Interval Value.
0	R/W	0x0	HS_TMR0_EN. High Speed Timer 0 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.4. HSTimer 0 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset:0x0014			Register Name: HS_TMR0_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_INTV_VALUE_LO. High Speed Timer 0 Interval Value [31:0].

3.8.6.5. HSTimer 0 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset:0x0018			Register Name: HS_TMR0_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR0_INTV_VALUE_HI. High Speed Timer 0 Interval Value [55:32].

NOTE

The interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or written firstly. And the Hi register should be written after the Lo register.

3.8.6.6. HSTimer 0 Current Value Lo Register(Default Value: 0x0000_0000)

Offset:0x001C			Register Name: HS_TMR0_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR0_CUR_VALUE_LO. High Speed Timer 0 Current Value [31:0].

3.8.6.7. HSTimer 0 Current Value Hi Register(Default Value: 0x0000_0000)

Offset:0x0020			Register Name: HS_TMR0_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

23:0	R/W	0x0	HS_TMR0_CUR_VALUE_HI. High Speed Timer 0 Current Value [55:32].

NOTE

HSTimer 0 current value is a 56-bit down-counter (from interval value to 0).
The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or written firstly.

3.8.6.8. HSTimer 1 Control Register(Default Value: 0x0000_0000)

Offset:0x0030			Register Name:HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR1_TEST. High speed timer 1 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode.
30:8	/	/	/
7	R/W	0x0	HS_TMR1_MODE. High Speed Timer 1 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR1_CLK_SRC. Select the pre-scale of the high speed timer 1 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR1_RELOAD. High Speed Timer 1 Reload. 0: No effect 1: Reload High Speed Timer 1 Interval Value.
0	R/W	0x0	HS_TMR1_EN. High Speed Timer 1 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1.

Offset:0x0030			Register Name:HS_TMR1_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.9. HSTimer 1 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset:0x0034			Register Name: HS_TMR1_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_INTV_VALUE_LO. High Speed Timer 1 Interval Value [31:0].

3.8.6.10. HSTimer 1 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset:0x0038			Register Name: HS_TMR1_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_INTV_VALUE_HI. High Speed Timer 1 Interval Value [55:32].

NOTE

The interval value register is a 56-bit register. When reading or writing the interval value, the Lo register should be read or written firstly. And the Hi register should be written after the Lo register.

3.8.6.11. HSTimer 1 Current Value Lo Register(Default Value: 0x0000_0000)

Offset:0x003C			Register Name: HS_TMR1_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR1_CUR_VALUE_LO. High Speed Timer 1 Current Value [31:0].

3.8.6.12. HSTimer 1 Current Value Hi Register(Default Value: 0x0000_0000)

Offset:0x0040			Register Name: HS_TMR1_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR1_CUR_VALUE_HI. High Speed Timer 1 Current Value [55:32].

NOTE

HSTimer 1 current value is a 56-bit down-counter (from interval value to 0).

The current value register is a 56-bit register. When reading or writing the current value, the Low register should be read or written firstly.

3.8.6.13. HSTimer 2 Control Register(Default Value: 0x0000_0000)

Offset:0x0050			Register Name: HS_TMR2_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS_TMR2_TEST. High speed timer 2 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode.
30:8	/	/	/
7	R/W	0x0	HS_TMR2_MODE. High Speed Timer 2 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR0_CLK Select the pre-scale of the high speed timer 0 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR2_RELOAD. High Speed Timer 2 Reload. 0: No effect 1: Reload High Speed Timer 2 Interval Value.
0	R/W	0x0	HS_TMR2_EN. High Speed Timer 2 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.14. HSTimer 2 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset:0x0054			Register Name: HS_TMR2_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset:0x0054			Register Name: HS_TMR2_INTV_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR2_INTV_VALUE_LO. High Speed Timer 2 Interval Value [31:0].

3.8.6.15. HSTimer 2 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset:0x0058			Register Name: HS_TMR2_INTV_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR2_INTV_VALUE_HI. High Speed Timer 2 Interval Value [55:32].

NOTE

The interval value register is a 56-bit register. When reading or writing the interval value, the Lo register should be read or written firstly. And the Hi register should be written after the Lo register.

3.8.6.16. HSTimer 2 Current Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x005C			Register Name: HS_TMR2_CURNT_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	HS_TMR2_CUR_VALUE_LO. High Speed Timer 2 Current Value [31:0].

3.8.6.17. HSTimer 2 Current Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: HS_TMR2_CURNT_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	HS_TMR2_CUR_VALUE_HI. High Speed Timer 2 Current Value [55:32].

NOTE

High speed timer 2 current value is a 56-bit down-counter (from interval value to 0).
The current value register is a 56-bit register. When reading or writing the current value, the Lo register should be read or written firstly.

3.8.6.18. HSTimer 3 Control Register(Default Value: 0x0000_0000)

Offset: 0x0070			Register Name:HS_TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS_TMR3_TEST. High speed timer 3 test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded. 0: Normal mode 1: Test mode.
30:8	/	/	/
7	R/W	0x0	HS_TMR3_MODE.

Offset: 0x0070			Register Name:HS_TMR3_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			High Speed Timer 3 mode. 0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.
6:4	R/W	0x0	HS_TMR3_CLK_SRC. Select the pre-scale of the high speed timer 3 clock sources. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	HS_TMR3_RELOAD. High Speed Timer 3 Reload. 0: No effect 1: Reload High Speed Timer 3 Interval Value.
0	R/W	0x0	HS_TMR3_EN. High Speed Timer 3 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”, the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

3.8.6.19. HSTimer 3 Interval Value Lo Register(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: HS_TMR3_INTV_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HS_TMR3_INTV_VALUE_LO. High Speed Timer 3 Interval Value [31:0].

3.8.6.20. HSTimer 3 Interval Value Hi Register(Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: HS_TMR3_INTV_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	HS_TMR3_INTV_VALUE_HI. High Speed Timer 3 Interval Value [55:32].

NOTE

The interval value register is a 56-bit register. When reading or writing the interval value, the Lo register should be read or written firstly. And the Hi register should be written after the Lo register.

3.8.6.21. HSTimer 3 Current Value Lo Register(Default Value: UDF)

Offset: 0x007C			Register Name: HS_TMR3_CURNT_LO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	UDF	HS_TMR3_CUR_VALUE_LO. High Speed Timer 3 Current Value [31:0].

3.8.6.22. HSTimer 3 Current Value Hi Register(Default Value: UDF)

Offset: 0x0080			Register Name: HS_TMR3_CURNT_HI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	UDF	HS_TMR3_CUR_VALUE_HI. High Speed Timer 3 Current Value [55:32].

NOTE

High speed timer 1 current value is a 56-bit down-counter (from interval value to 0).
The current value register is a 56-bit register. When reading or writing the current value, the Low register should be read or written firstly.

3.9. GIC

Interrupt Source	SRC	Description
SGI 0	0	SGI 0 interrupt
SGI 1	1	SGI 1 interrupt
SGI 2	2	SGI 2 interrupt
SGI 3	3	SGI 3 interrupt
SGI 4	4	SGI 4 interrupt
SGI 5	5	SGI 5 interrupt
SGI 6	6	SGI 6 interrupt
SGI 7	7	SGI 7 interrupt
SGI 8	8	SGI 8 interrupt
SGI 9	9	SGI 9 interrupt
SGI 10	10	SGI 10 interrupt
SGI 11	11	SGI 11 interrupt
SGI 12	12	SGI 12 interrupt
SGI 13	13	SGI 13 interrupt
SGI 14	14	SGI 14 interrupt
SGI 15	15	SGI 15 interrupt
PPI 0	16	PPI 0 interrupt
PPI 1	17	PPI 1 interrupt
PPI 2	18	PPI 2 interrupt
PPI 3	19	PPI 3 interrupt
PPI 4	20	PPI 4 interrupt
PPI 5	21	PPI 5 interrupt
PPI 6	22	PPI 6 interrupt
PPI 7	23	PPI 7 interrupt
PPI 8	24	PPI 8 interrupt
PPI 9	25	PPI 9 interrupt
PPI 10	26	PPI 10 interrupt
PPI 11	27	PPI 11 interrupt
PPI 12	28	PPI 12 interrupt
PPI 13	29	PPI 13 interrupt
PPI 14	30	PPI 14 interrupt
PPI 15	31	PPI 15 interrupt
NMI	32	NMI interrupt
UART 0	33	UART 0 interrupt
UART 1	34	UART 1 interrupt
UART 2	35	UART 2 interrupt
UART 3	36	UART 3 interrupt
CIR 0	37	CIR 0 interrupt
CIR 1	38	CIR 1 interrupt
TWI 0	39	TWI 0 interrupt
TWI 1	40	TWI 1 interrupt
TWI 2	41	TWI 2 interrupt
SPI 0	42	SPI 0 interrupt
SPI 1	43	SPI 1 interrupt
SPI 2	44	SPI 2 interrupt
OWA	45	OWA interrupt
AC97	46	AC97 interrupt
TS	47	TS interrupt

Interrupt Source	SRC	Description
I2S/PCM0	48	I2S/PCM 0 interrupt
UART 4	49	UART 4 interrupt
UART 5	50	UART 5 interrupt
UART 6	51	UART 6 interrupt
UART 7	52	UART 7 interrupt
Keypad	53	Keypad interrupt
Timer 0	54	Timer 0 interrupt
Timer 1	55	Timer 1interrupt
Timer 2/Alarm/WD	56	Timer 2 , Alarm, Watchdog interrupt
Timer 3	57	Timer 3 interrupt
/	58	/
DMA	59	DMA interrupt
PIO	60	PIO interrupt
Touch Panel	61	Touch Panel interrupt
Audio Codec	62	Audio Codec interrupt
KEYADC	63	KEYADC interrupt
SD/MMC 0	64	SD/MMC Host Controller 0 interrupt
SD/MMC 1	65	SD/MMC Host Controller 1 interrupt
SD/MMC 2	66	SD/MMC Host Controller 2 interrupt
SD/MMC 3	67	SD/MMC Host Controller 3 interrupt
THS	68	Thermal Sensor interrupt
NAND	69	NAND Flash Controller (NFC) interrupt
USB 0_OTG	70	USB 0_OTG interrupt
USB 0_EHCI	71	USB 0_EHCI interrupt
USB 0_OHCI	72	USB 0_OHCI interrupt
SCR	73	SCR interrupt
CSI 0	74	CSI 0 interrupt
CSI 1	75	CSI 1 interrupt
TCON_LCD0	76	TCON_LCD0 interrupt
TCON_LCD1	77	TCON_LCD1 interrupt
MP	78	MP interrupt
PWM	79	PWM interrupt
/	80	/
PMU	81	PMU interrupt
SPI3	82	SPI3 interrupt
TCON_TV0	83	TCON_TV0 interrupt
TCON_TV1	84	TCON_TV1 interrupt
VE	85	VE interrupt
CE Secure	86	Security System Secure interrupt.
EMAC	87	EMAC interrupt
SATA	88	SATA interrupt
MIPI_DSI	89	MIPI DSI interrupt
HDMI	90	HDMI interrupt
TVE 0	91	TV encoder 0 interrupt
TVE 1	92	TV encoder 1 interrupt
TVD	93	TV decoder interrupt
PS2-0	94	PS2-0 interrupt
PS2-1	95	PS2-1 interrupt
USB 1 OHCI	96	USB 1 OHCI interrupt
USB 2 OHCI	97	USB 2 OHCI interrupt
DRAM MDFS	98	Dram MDFS interrupt
Timer 4	99	Timer 4 interrupt
Timer 5	100	Timer 5 interrupt

Interrupt Source	SRC	Description
GPU-GP	101	GPU-GP interrupt
GPU-GPMMU	102	GPU-GPMMU interrupt
GPU-PP0	103	GPU-PP0 interrupt
GPU-PPMMU0	104	GPU-PPMMU0 interrupt
GPU-PMU	105	GPU-PMU interrupt
GPU-PP1	106	GPU-PP1 interrupt
GPU-PPMMU1	107	GPU-PPMMU1 interrupt
USB1 EHCI	108	USB1 EHCI interrupt
/	109	/
USB2 EHCI	110	USB2 EHCI interrupt
/	111	/
/	112	/
HSTimer 0	113	HSTimer 0 interrupt
HSTimer 1	114	HSTimer 1 interrupt
HSTimer 2	115	HSTimer 2 interrupt
HSTimer 3	116	HSTimer 3 interrupt
GMAC	117	GMAC interrupt
/	118	/
I2S/PCM1	119	I2S/PCM 1 interrupt
TWI 3	120	TWI 3 interrupt
TWI 4	121	TWI 4 interrupt
I2S/PCM2	122	I2S/PCM 2 interrupt
/	123	/
/	124	/
DE-interlace	125	DE-interlace interrupt
CE Non-Secure	126	CE Non-Secure interrupt
DE	127	DE interrupt
ROT	128	DE ROTATE interrupt
TVD0	129	TVD0 interrupt
TVD1	130	TVD1 interrupt
TVD2	131	TVD2 interrupt
TVD3	132	TVD3 interrupt

For complete GIC information, refer to the ***IHI0048B_b_gic_architecture_specification***.

3.10. DMA

3.10.1. Overview

The DMA enables data transfers between peripheral I/O devices and memories without using the CPU .This avoids the CPU intervention and helps maximize system performance by off-loading the CPU. There are 16 DMA channels in the chip. Each DMA channel can generate interrupts. According to different pending status, the referenced DMA channel generates corresponding interrupt. And the configuration information of every DMA channel are storing in the DDR or SRAM. When starting a DMA transferring, the **DMA Channel Descriptor Address Register** contains the address information in the DDR or SRAM, where has the relevance configuration information of the DMA transferring.

The DMA includes the following features:

- DMA transfer supports in either direction between memory and peripheral, or between memory and memory
- Transfers data width of 8/16/32/64-bit
- 16 DMA channels
- Programs the DMA burst size
- Flexible data source and destination address generation
- Supports linear and IO address modes
- Interrupt generated for each DMA channel

3.10.2. Block Diagram

Figure 3-19 shows a block diagram of the DMA.

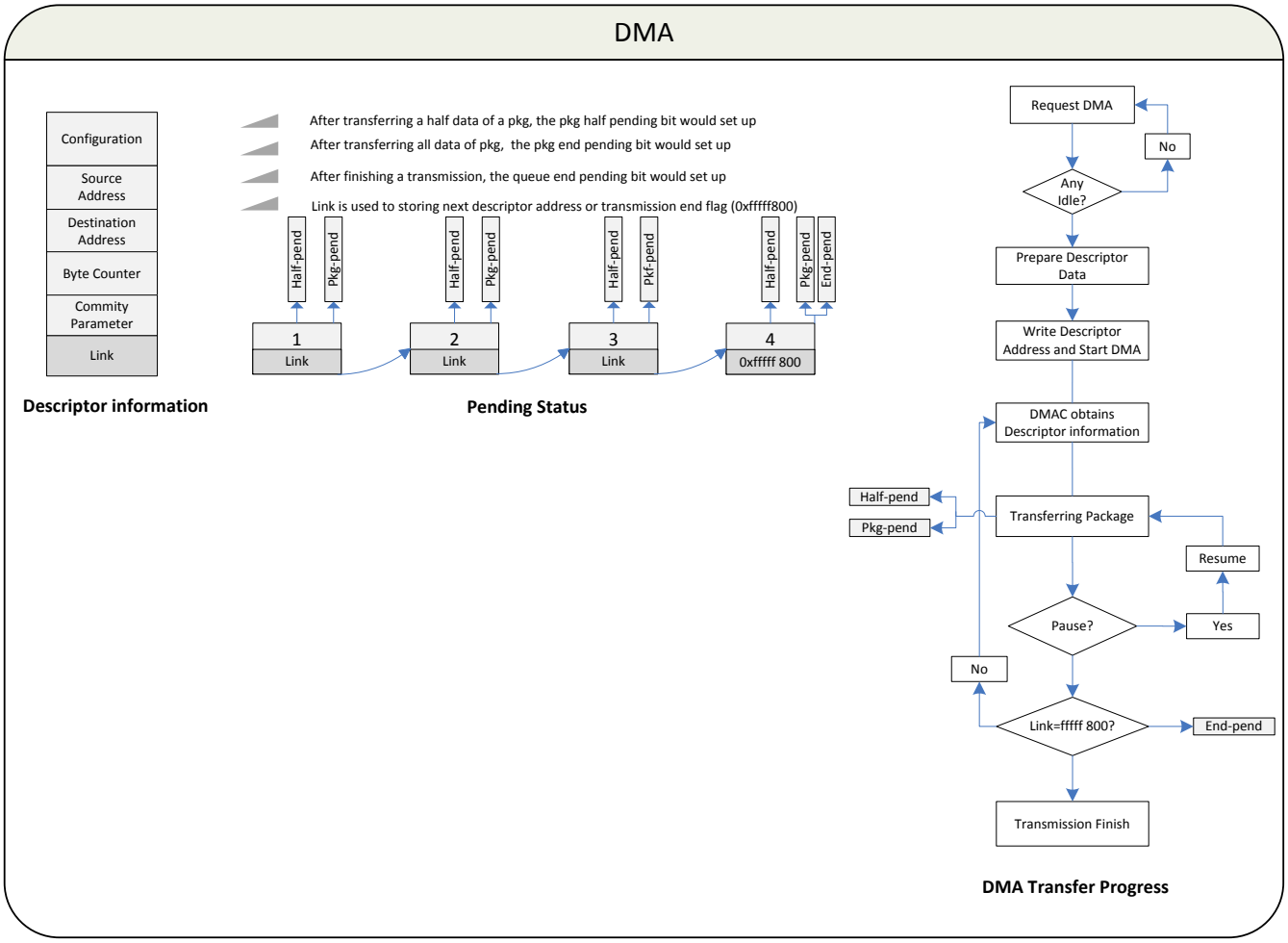


Figure 3-19. DMA Block Diagram

3.10.3. Operations and Functional Descriptions

3.10.3.1. DMA Description

In this section, the DMA descriptor registers will be introduced in detail.

When starting a DMA transmission, the module data are transferred as packages, which have the link data information. And by reading **DMA Status Register**, the status of a DMA channel could be known. Reading back **DMA Channel Descriptor Address Register**, the value is the link data in the transferring package. If only the value is equal to 0xfffff800, then it can be regarded as NULL, which means the package is the last package in this DMA transmission. Otherwise, the value means the start address of the next package. And **DMA Channel Descriptor Address Register** can be changed during a package transferring.

When transferring the half of a package, the relevant pending bit will be set up automatically, and if the corresponding interrupt is enabled, DMA generates an interrupt to the system. The similar thing would occur when transferring a package completely. Meanwhile, if DMA has transferred the last package in the data, the relevant pending bit would be set up, and generates an interrupt if the corresponding interrupt is enabled. The flow-process diagram is shown in **DMA Block Diagram**.

During a DMA transmission, the configuration could be obtained via **DMA Channel Configuration Register**. And behind the address of the configuration register in DDR or SRAM, there are some registers including other information of a DMA transmission. The structure chart is shown in **DMA Block Diagram**. Also other information of a transferring data can be obtained by reading the **DMA Channel Current Source Address Register**, **DMA Channel Current Destination**

Address Register and **DMA Channel Byte Counter Left Register**. The configuration must be word-aligning.

The transferring data would be paused when setting up the relevant **DMA Channel Pause Register**, if coming up emergency. And the pausing data could be presumable when setting 0 to the same bit in **DMA Channel Pause Register**.

Table 3-3. DRQ Type and Port Corresponding Relation

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	SDRAM	port1	SDRAM
port2		port2	OWA_TX
port3	I2S/PCM0_RX	port3	I2S/PCM0_TX
port4	I2S/PCM1_RX	port4	I2S/PCM1_TX
port5	AC97_RX	port5	AC97_TX
port6	I2S/PCM2_RX	port6	I2S/PCM2_TX
port7	NAND	port7	NAND
port8	UART0_RX	port8	UART0_TX
port9	UART1_RX	port9	UART1_TX
port10	UART2_RX	port10	UART2_TX
port11	UART3_RX	port11	UART3_TX
port12	UART4_RX	port12	UART4_TX
port13	UART5_RX	port13	UART5_TX
port14	UART6_RX	port14	UART6_TX
port15	UART7_RX	port15	UART7_TX
port16		port16	
port17	OTG_EP1	port17	OTG_EP1
port18		port18	
port19	Audio Codec_ADC	port19	Audio Codec_DAC
port20	CIR0_RX	port20	CIR0_TX
port21	CIR1_RX	port21	CIR1_TX
port22	EMAC_RX	port22	EMAC_TX
port23	RTP_RX	port23	
port24	SPI0_RX	port24	SPI0_TX
port25	SPI1_RX	port25	SPI1_TX
port26	SPI2_RX	port26	SPI2_TX
port27	SPI3_RX	port27	SPI3_TX
port28	OTG_EP2	port28	OTG_EP2
port29	OTG_EP3	port29	OTG_EP3
Port30	OTG_EP4	port30	OTG_EP4
Port31	OTG_EP5	port31	OTG_EP5

3.10.3.2. Programming Guidelines

(1) When the DMA transfer is paused, this is equivalent to invalid DRQ.Because DMA transfer command has a certain time delay, DMA will not stop transfer immediately until the current command and the command in Arbiter finished, at most 32byte data.

DMA application example :
writel(0x00000000, mem_address + 0x00); //Setting configuration, mem_address must be word-aligned


```
writel(0x00001000, mem_address + 0x04);    // Setting the start address for the source device
writel(0x20000000, mem_address + 0x08);    //Setting the start address for the destination device
writel(0x00000020, mem_address + 0x0C);    // Setting data package size
writel(0x00000000, mem_address + 0x10);    //Setting parameter
writel(0xFFFFF800, mem_address + 0x14);          //Setting the start address for the next descriptor
writel(mem_address, 0x01C02000+ 0x100 + 0x08); //Setting the start address for the DMA channel0 descriptor
do{
If(mem_address == readl(0x01C02000 + 0x100 + 0x08));
break;
}while(1);              //Make sure writing operation valid
writel(0x000000001, 0x01C02000 + 0x100 + 0x00);       // Enable DMA channel0 transfer
```

(2) DMA supports increase data package in transfer, there are a few points to note here.

When the value of **DMA Channel Descriptor Address Register** is 0xFFFFF800, it indicates that DMA channel has got back the descriptor of the last package. When DMA channel completed the package data transfer, DMA channel will stop automatically data transfer.

If needing increase data package,then at first it is essential to judge that whether DMA channel has got back the descriptor of the last package,if DMA channel has got back the descriptor of the last package, then this is impossible for increasing data package, DMA channel need start again. If DMA is not transmitting the last package,then the last descriptor address 0xFFFFF800 can be changed to the start address of the next descriptor.

To ensure that the data changed valid, we can read again the value of **DMA Channel Descriptor Address Register** after changed the data. If there is not 0xFFFFF800,then it indicates that increasing data package is succeed, and fail otherwise. Because the process of increasing data package need some time, during this time,DMA channel may get back the descriptor of the last package.At the moment we can read again **DMA Channel Current Source Address Register** and **DMA Channel Current Destination Address Register**, if the increasing memory address accords with the information of the increasing data package, then increasing data package is succeed, and fail otherwise.

To ensure the higher success rate, it is suggested that increase data package before half package interrupt of penultimate data package.

3.10.4. Register List

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_IRQ_EN_REG0	0x0000	DMA IRQ Enable Register0
DMA_IRQ_EN_REG1	0x0004	DMA IRQ Enable Register1
DMA_IRQ_PEND_REG0	0x0010	DMA IRQ Pending Register0
DMA_IRQ_PEND_REG0	0x0014	DMA IRQ Pending Register1
DMA_AUTO_GATE_REG	0x0028	DMA Auto Gating Register
DMA_STA_REG	0x0030	DMA Status Register
DMA_EN_REG	0x0100+N*0x40(N=0~15)	DMA Channel Enable Register
DMA_PAU_REG	0x0100+0x04+N*0x40(N=0~15)	DMA Channel Pause Register
DMA_DESC_ADDR_REG	0x0100+0x08+N*0x40(N=0~15)	DMA Channel Start Address Register
DMA_CFG_REG	0x0100+0x0C+N*0x40(N=0~15)	DMA Channel Configuration Register
DMA_CUR_SRC_REG	0x0100+0x10+N*0x40(N=0~15)	DMA Channel Current Source Register
DMA_CUR_DEST_REG	0x0100+0x14+N*0x40(N=0~15)	DMA Channel Current Destination Register
DMA_BCNT_LEFT_REG	0x0100+0x18+N*0x40(N=0~15)	DMA Channel Byte Counter Left Register
DMA_PARA_REG	0x0100+0x1C+N*0x40(N=0~15)	DMA Channel Parameter Register
DMA_MODE_REG	0x0100+0x28+N*0x40(N=0~15)	DMA Mode Register

Register Name	Offset	Description
DMA_FDESC_ADDR_REG	0x0100+0x2C+N*0x40(N=0~15)	DMA Former Descriptor Address Register
DMA_PKG_NUM_REG	0x0100+0x30+N*0x40(N=0~15)	DMA Package Number Register

3.10.5. Register Description

3.10.5.1. DMA IRQ Enable Register0(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN DMA 5 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA5_HLAF_IRQ_EN

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			DMA 5 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN

Offset: 0x0000			Register Name: DMA_IRQ_EN_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			DMA 1 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA0_HLAF_IRQ_EN DMA 0 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.5.2. DMA IRQ Enable Register1(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	DMA15_QUEUE_IRQ_EN DMA 15 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
29	R/W	0x0	DMA15_PKG_IRQ_EN DMA 15 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
28	R/W	0x0	DMA15_HLAF_IRQ_EN DMA 15 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
27	/	/	/

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
26	R/W	0x0	DMA14_QUEUE_IRQ_EN DMA 14 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
25	R/W	0x0	DMA14_PKG_IRQ_EN DMA 14 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
24	R/W	0x0	DMA14_HLAF_IRQ_EN DMA 14 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
23	/	/	/
22	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
21	R/W	0x0	DMA13_PKG_IRQ_EN DMA 13 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
20	R/W	0x0	DMA13_HLAF_IRQ_EN DMA 13 Half package Transfer Interrupt Enable. 0: Disable 1: Enable
19	/	/	/
18	R/W	0x0	DMA13_QUEUE_IRQ_EN DMA 13 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
17	R/W	0x0	DMA12_PKG_IRQ_EN DMA 12 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
16	R/W	0x0	DMA12_HLAF_IRQ_EN DMA 12 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
15	/	/	/
14	R/W	0x0	DMA11_QUEUE_IRQ_EN DMA 11 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
13	R/W	0x0	DMA11_PKG_IRQ_EN DMA 11Package End Transfer Interrupt Enable.

Offset: 0x0004			Register Name: DMA_IRQ_EN_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Disable 1: Enable
12	R/W	0x0	DMA11_HLAF_IRQ_EN DMA 11 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
11	/	/	/
10	R/W	0x0	DMA10_QUEUE_IRQ_EN DMA 10 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
9	R/W	0x0	DMA10_PKG_IRQ_EN DMA 10 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
8	R/W	0x0	DMA10_HLAF_IRQ_EN DMA 10 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
7	/	/	/
6	R/W	0x0	DMA9_QUEUE_IRQ_EN DMA 9 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
5	R/W	0x0	DMA9_PKG_IRQ_EN DMA 9 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
4	R/W	0x0	DMA9_HLAF_IRQ_EN DMA 9 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	DMA8_QUEUE_IRQ_EN DMA 8 Queue End Transfer Interrupt Enable. 0: Disable 1: Enable
1	R/W	0x0	DMA8_PKG_IRQ_EN DMA 8 Package End Transfer Interrupt Enable. 0: Disable 1: Enable
0	R/W	0x0	DMA8_HLAF_IRQ_EN DMA 8 Half Package Transfer Interrupt Enable. 0: Disable 1: Enable

3.10.5.3. DMA IRQ Pending Status Register 0(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA7_PKG_IRQ_ PEND DMA 7 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA6_PKG_IRQ_ PEND DMA 6 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA5_PKG_IRQ_ PEND DMA 5 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it.

Offset: 0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No effect 1: Pending
20	R/W1C	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA4_PKG_IRQ_ PEND DMA 4 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA3_PKG_IRQ_ PEND DMA 3 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA2_PKG_IRQ_ PEND

Offset: 0x0010			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			DMA 2 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
8	R/W1C	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA1_PKG_IRQ_ PEND DMA 1 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA0_PKG_IRQ_ PEND DMA 0 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.10.5.4. DMA IRQ Pending Status Register 1(Default Value: 0x0000_0000)

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W1C	0x0	DMA15_QUEUE_IRQ_PEND. DMA 15 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
29	R/W1C	0x0	DMA15_PKG_IRQ_ PEND DMA 15 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
28	R/W1C	0x0	DMA15_HLAF_IRQ_PEND. DMA 15 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
27	/	/	/
26	R/W1C	0x0	DMA14_QUEUE_IRQ_PEND. DMA 14 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
25	R/W1C	0x0	DMA14_PKG_IRQ_ PEND DMA 14 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
24	R/W1C	0x0	DMA14_HLAF_IRQ_PEND. DMA 14 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
23	/	/	/
22	R/W1C	0x0	DMA13_QUEUE_IRQ_PEND. DMA 13 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
21	R/W1C	0x0	DMA13_PKG_IRQ_ PEND DMA 13 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
20	R/W1C	0x0	DMA13_HLAF_IRQ_PEND.

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			DMA 13 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
19	/	/	/
18	R/W1C	0x0	DMA12_QUEUE_IRQ_PEND. DMA 12 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
17	R/W1C	0x0	DMA12_PKG_IRQ_ PEND DMA 12 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
16	R/W1C	0x0	DMA12_HLAF_IRQ_PEND. DMA 12 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
15	/	/	/
14	R/W1C	0x0	DMA11_QUEUE_IRQ_PEND. DMA 11 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending.
13	R/W1C	0x0	DMA11_PKG_IRQ_ PEND DMA 11 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
12	R/W1C	0x0	DMA11_HLAF_IRQ_PEND. DMA 11 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
11	/	/	/
10	R/W1C	0x0	DMA10_QUEUE_IRQ_PEND. DMA 10 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
9	R/W1C	0x0	DMA10_PKG_IRQ_ PEND DMA 10 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it.

Offset:0x0014			Register Name: DMA_IRQ_PEND_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No effect 1: Pending
8	R/W1C	0x0	DMA10_HLAF_IRQ_PEND. DMA 10 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
7	/	/	/
6	R/W1C	0x0	DMA9_QUEUE_IRQ_PEND. DMA 9 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
5	R/W1C	0x0	DMA9_PKG_IRQ_ PEND DMA 9 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
4	R/W1C	0x0	DMA9_HLAF_IRQ_PEND. DMA 9 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
3	/	/	/
2	R/W1C	0x0	DMA8_QUEUE_IRQ_PEND. DMA 8 Queue End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
1	R/W1C	0x0	DMA8_PKG_IRQ_ PEND DMA 8 Package End Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending
0	R/W1C	0x0	DMA8_HLAF_IRQ_PEND. DMA 8 Half Package Transfer Interrupt Pending. Setting 1 to the bit will clear it. 0: No effect 1: Pending

3.10.5.5. DMA Auto Gating Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: DMA_AUTO_GATE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

Offset: 0x0028			Register Name: DMA_AUTO_GATE_REG
2	R/W	0x0	DMA_MCLK_CIRCUIT. DMA MCLK interface circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
1	R/W	0x0	DMA_COMMON_CIRCUIT. DMA common circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable
0	R/W	0x0	DMA_CHAN_CIRCUIT. DMA channel circuit auto gating bit. 0: Auto gating enable 1: Auto gating disable

3.10.5.6. DMA Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: DMA_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R	0x0	MBUS FIFO Status 0: Empty 1: Not Empty
29:16	/	/	/
15	R	0x0	DMA15_STATUS DMA Channel 15 Status. 0: Idle 1: Busy
14	R	0x0	DMA14_STATUS DMA Channel 14 Status. 0: Idle 1: Busy
13	R	0x0	DMA13_STATUS DMA Channel 13 Status. 0: Idle 1: Busy
12	R	0x0	DMA12_STATUS DMA Channel 12 Status. 0: Idle 1: Busy
11	R	0x0	DMA11_STATUS DMA Channel 11 Status. 0: Idle 1: Busy
10	R	0x0	DMA10_STATUS DMA Channel 10 Status.

			0: Idle 1: Busy
9	R	0x0	DMA9_STATUS DMA Channel 9 Status. 0: Idle 1: Busy
8	R	0x0	DMA8_STATUS DMA Channel 8 Status. 0: Idle 1: Busy
7	R	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle 1: Busy
6	R	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle 1: Busy
5	R	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle 1: Busy
4	R	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle 1: Busy
3	R	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle 1: Busy
2	R	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle 1: Busy
1	R	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle 1: Busy
0	R	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle 1: Busy

3.10.5.7. DMA Channel Enable Register(Default Value: 0x0000_0000)

Offset: 0x0100+N*0x40(N=0~15)			Register Name: DMA_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable 1: Enable

3.10.5.8. DMA Channel Pause Register(Default Value: 0x0000_0000)

Offset: 0x0104+N*0x40(N=0~15)			Register Name: DMA_PAU_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring 1: Pause Transferring

3.10.5.9. DMA Channel Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0108+N*0x40(N=0~15)			Register Name: DMA_DESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	DMA_DESC_ADDR DMA Channel Descriptor Address. The Descriptor Address must be word-aligned.

3.10.5.10. DMA Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x010C+N*0x40(N=0~15)			Register Name: DMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:25	R	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
24	/	/	/
23:22	R	0x0	DMA_DEST_BLOCK_SIZE. DMA Destination Block Size. 00: 1 01: 4 10: 8 11: 16
21	R	0x0	DMA_ADDR_MODE.

Offset: 0x010C+N*0x40(N=0~15)			Register Name: DMA_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			DMA Destination Address Mode 0: Linear Mode 1: IO Mode
20:16	R	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details refer to **DRQ Type and Port Corresponding Relation**.
15:11	/	/	/
10:9	R	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: 64-bit
8	/	/	/
7:6	R	0x0	DMA_SRC_BLOCK_SIZE. DMA Source Block Size. 00: 1 01: 4 10: 8 11: 16
5	R	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0: Linear Mode 1: IO Mode
4:0	R	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details refer to **DRQ Type and Port Corresponding Relation**.

3.10.5.11. DMA Channel Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x40(N=0~15)			Register Name: DMA_CUR_SRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

3.10.5.12. DMA Channel Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0114+N*0x40(N=0~15)			Register Name: DMA_CUR_DEST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.

3.10.5.13. DMA Channel Parameter Register(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x40(N=0~15)			Register Name: DMA_PARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x011C+N*0x40(N=0~15)			Register Name: DMA_PARA_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	WAIT_CYC. Wait Clock Cycles

3.10.5.14. DMA Channel Byte Counter Left Register(Default Value: 0x0000_0000)

Offset: 0x0118+N*0x40(N=0~15)			Register Name: DMA_BCNT_LEFT_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R	0x0	DMA_BCNT_LEFT DMA Channel Byte Counter Left,read only

3.10.5.15. DMA Mode Register(Default Value: 0x0000_0000)

Offset: 0x0128+N*0x40(N=0~15)			Register Name: DMA_MODE_REG
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	DMA_DST_MODE. 0: Wait mode. 1: Handshake mode.
2	R/W	0x0	DMA_SRC_MODE. 0: Wait mode. 1: Handshake mode.
1:0	/	/	/

3.10.5.16. DMA Former Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x012C+N*0x40(N=0~15)			Register Name: DMA_FDESC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_FDESC_ADDR. This register is used to storing the former value of DMA Channel Descriptor Address Register.

3.10.5.17. DMA Package Number Register(Default Value: 0x0000_0000)

Offset: 0x0130+N*0x40(N=0~15)			Register Name: DMA_PKG_NUM_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DMA_PKG_NUM. This register will record the number of packages which has been completed in one transmission.

3.11. RTC

3.11.1. Overview

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator and a independent power pin (RTC_VIO).

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated. In this section, there are two kinds of alarm. Alarm 0 is a general alarm, its counter is based on second. Alarm 1 is a weekly alarm, its counter is based on the real time.

The 32768Hz oscillator is used only to provide a low power, accurate reference for the RTC.

General Purpose Register can be flag register, and it will save the value all the time when the VDD_RTC is not power off.

3.11.2. Block Diagram

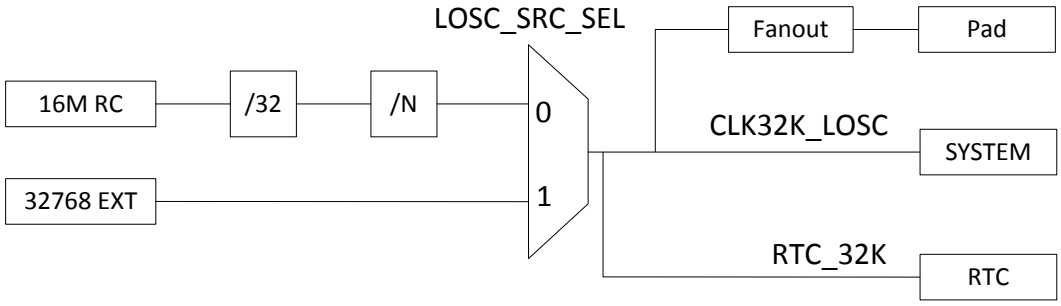


Figure 3-20. RTC Block Diagram

3.11.3. Operations and Functional Descriptions

3.11.3.1. External Signals

Table 3-4. RTC External Signals

Signal	Description
X32KIN	32768Hz crystal input
X32KOUT	32768Hz crystal drive output
NMI	Alarm wakeup generates low level into NMI
RTC-VIO	RTC low voltage,generated via internal LDO
VCC-RTC	RTC high voltage,generated via external power

3.11.3.2. Clock and Reset

The RTC module has the independent reset signal, the signal follows VCC-RTC. When VCC-RTC powers on, the reset signal resets the RTC module; after VCC-RTC reaches stable, the reset signal always holds high level.

3.11.3.3. Typical Application

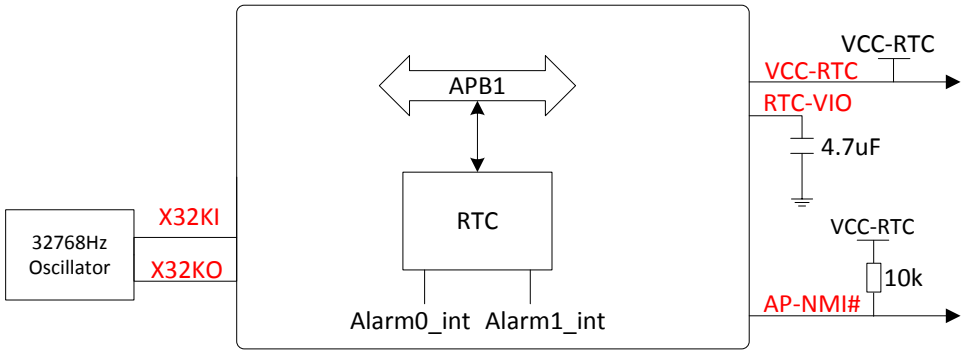


Figure 3-21. RTC Application Diagram

The system accesses RTC register by APB1 to generate the real time.
The external low-frequency oscillator must be 32.768 kHz.
AP-NMI# and alarm0 in common generate low level signal.

3.11.3.4. Function Implementation

3.11.3.4.1. Clock Sources

The RTC has two clock sources: internal RC , external low frequency oscillator.
The internal RC can change RTC clock by changing division ratio ;the external clock can not change clock.
The RTC selects the internal RC by default, when the system starts, the RTC can select by software the external low frequency oscillator to provide much accuracy clock.
The clock accurate of the RTC is related to the accurate of the external low frequency oscillator. The external oscillator usually selects 32.768 kHz oscillator with ±20ppm frequency tolerance.

3.11.3.4.2. Real Time Clock

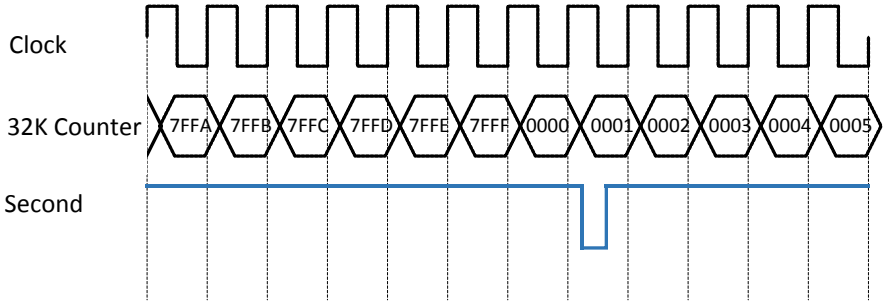


Figure 3-22. RTC Counter

The 32K counter adds 1 on each rising edge of the clock. When the clock number reaches 0x8000, 32KHz counter starts to count again from 0, and the second counter adds 1. The 32KHz counter block diagram is as follows.

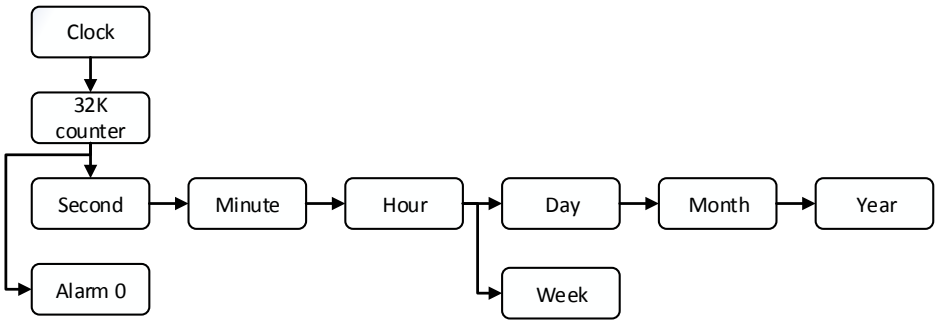


Figure 3-23. RTC 32KHz Counter Block Diagram

According to above implementation, the changing range of each counter is as follows.

Table 3-5. RTC Counter Changing Range

Counter	Range
Second	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Minute	If the counter value is not in the range from 0 to 59, then the counter value can change to 59 automatically.
Hour	If the counter value is not in the range from 0 to 23, then the counter value can change to 23 automatically.
Week	If the counter value is not in the range from 0 to 6, then the counter value can change to 6 automatically.
Day	If the counter value is not in the range from 1 to 31, then the counter value can change to the maximum value of that month automatically.
Month	If the counter value is not in the range from 1 to 12, then the counter value can change to 12 automatically.
Year	The software can set a reference year, the leap year can only set by software.

3.11.3.4.3. Alarm0

The principle of alarm0 is similar to the second counter, the difference is that alarm0 is a 32-bit down counter. When the counter decreases to 0 from the initial value, the RTC generates the interrupt, or outputs low level signal by NMI pin to wakeup power management chip.

3.11.3.4.4. Alarm1

The alarm1 can set alarm response time and the response cycle. When the system real time satisfies the setting time, the RTC generates alram1 interrupt to handle alarm interrupt function.

3.11.3.4.5. Power-off Storage

The RTC provides eight 32-bit general purpose register to store power-off information.

Because VCC-RTC always holds non-power-off state after VCC-RTC cold starts, when the system is in shutdown or standby scene, CPU can judge software process by the storing information.

3.11.3.4.6. RTC-VIO

The RTC module has a LDO ,the input source of the LDO is VCC-RTC,the output of the LDO is RTC-VIO,the value of RTC-VIO is adjustable,it is mainly used for internal digital logic.

3.11.3.5. Operating Mode

3.11.3.5.1. RTC Clock Control

(1) Select clock source: Select clock source by the bit0 of **LOSC_CTRL_REG**, the clock source is the internal RC oscillator by default, when the system starts, the clock source can be switched to the external 32K oscillator by software.
(2) Auto switch: After enabled the bit[14] of **LOSC_CTRL_REG**, the RTC automatically switches clock source to the internal oscillator when the external oscillator could not output waveform, the switch status can query by the bit[1] of **LOSC_AUTO_SWT_STA_REG**.
(3) After auto switch is valid, the clock source status bit cannot be changed, because the two functions are independent.

3.11.3.5.2. RTC Calendar

(1) Write time initial value: Write the current time to **RTC_HH_MM_SS_REG** and **RTC_YY_MM_DD_REG**.
(2) After update time, the RTC restarts to count again .The software can read the current time anytime.
(3) The leap year function can be set only by the software.

3.11.3.5.3. Alarm0

(1) Enable alram0 interrupt by writing **ALARM0_IRQ_EN**.
(2) Set the counter initial value, write the count-down second number to **ALARM0_COUNTER_REG**.
(3) Enable alarm0 function by writing **ALARM0_ENABLE_REG**, then the software can query alarm count value in real time.
(4) After enter the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(5) Resume the interrupt and continue to execute the interrupted process.
(6) Power-off wakeup is generated via SoC hardware and PMIC, software only need set pending condition of alarm0, and set 1 to **ALARM0_CONFIG_REG**.

3.11.3.5.4. Alarm1

(1) Set alarm1 initial value : write the hour,minute,second of alarm1 to **ALARM1_WK_HH_MM_SS**.
(2) Write alarm week number enable bit to **ALARM1_EN_REG**.
(3) When the bit[20:0] of **RTC_HH_MM_SS_REG** is equal to **ALARM1_WK_HH_MM-SS,** and the bit[31:29] of **RTC_HH_MM_SS_REG** is equal to the week number of **ALARM1_EN_REG**, then the condition of alarm 1 is satisfied, pending is set automatically by hardware.
(4) When **ALARM0_IRQ_EN** is set to 1, the RTC enters into the interrupt process, write **ALARM0_IRQ_STA_REG** to clear the interrupt pending, and execute the process of waiting for the interrupt.
(5) Resume the interrupt and continue to execute the interrupted process.

3.11.4. Programming Guidelines

3.11.4.1. RTC Clock Sources Setting

```
writel(0x16aa4000,LOSC_CTRL);       //write key field
writel(0x16aa4001,LOSC_CTRL);           //select external clock
```


3.11.4.2. Real Time Clock

```
writel(0x00173b3b,RTC_HMS);
writel(1<<22|1<<8|31<<0,RTC_YMD);
readl(RTC_HMS);
readl(RTC_YMD);
```

3.11.4.3. Alarm 0

```
irq_request(GIC_SRC_R_ALM0,ALM0_HANDLER);
irq_enable(GIC_SRC_R_ALM0);
writel(1,ALM0_COUNTER);                    //set 1 second corresponding to normal mode
writel(1,ALM0_EN);
writel(1,ALM_CONFIG); //NMI output
while(!readl(ALM0_IRQ_STA));
writel(1,ALM0_IRQ_EN);
while(readl(ALM0_IRQ_STA));
```

3.11.4.4. Alarm 1

```
irq_request(GIC_SRC_R_ALM1,ALM1_HANDLER);
irq_enable(GIC_SRC_R_ALM1);
writel(0,ALM1_WK_HMS);
writel(0x7f,ALM1_EN);
writel(1,ALM1_IRQ_STA);
writel(0x00173b3b | week<<29,RTC_HMS);  //set 1 second corresponding to normal mode
while(readl(RTC_HMS)&0xff);
while(!readl(ALM1_IRQ_STA));
writel(1,ALM1_IRQ_EN);
while(readl(ALM1_IRQ_STA));
```

3.11.5. Register List

Module Name	Base Address
RTC	0x01C20400

Register Name	Offset	Description
LOSC_CTRL_REG	0x0000	Low Oscillator Control Register
LOSC_AUTO_SWT_STA_REG	0x0004	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x0008	Internal OSC Clock Prescalar Register
INTOSC_CLK_AUTO_CALI_REG	0x000C	Internal OSC Clock Auto Calibration Register
RTC_YY_MM_DD_REG	0x0010	RTC Year-Month-Day Register
RTC_HH_MM_SS_REG	0x0014	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x0020	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x0024	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x0028	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x002C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x0030	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM_SS	0x0040	Alarm 1 Week HMS Register

Register Name	Offset	Description
ALARM1_ENABLE_REG	0x0044	Alarm 1 Enable Register
ALARM1_IRQ_EN	0x0048	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	0x004C	Alarm 1 IRQ Status Register
ALARM_CONFIG_REG	0x0050	Alarm Configuration Register
GP_DATA_REG	0x0100 + N*0x04	General Purpose Register (N=0~7)
VDD_RTC_REG	0x0190	VDD RTC Regulate Register
IC_CHARA_REG	0x01F0	IC Characteristic Register
VDD_SYS_PWROFF_GATING_REG	0x01F4	VDD_SYS Power Off Gating Register
SUP_STAN_FLAG_REG	0x01F8	Super Standby Flag Register
CPU_SOFT_ENT_REG	0x01FC	CPU Software Entry Register

3.11.6. Register Description

3.11.6.1. LOSC Control Register(Default Value: 0x0000_4000)

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AA, and then the bit 0 can be written with the new value.
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN. LOSC auto switch enable. 0: Disable 1: Enable.
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE. ALARM DD-HH-MM-SS access. After wrote the **Alarm 1 Week HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After wrote the **RTC HH-MM-SS Register**, this bit is set and it will be cleared until the real writing operation is finished. After wrote the **RTC HH-MM-SS Register**, the **RTC HH-MM-SS Register** will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After wrote the **RTC YY-MM-DD Register**, this bit is set and it will be cleared until the real writing operation is finished. After wrote the **RTC YY-MM-DD Register**, the **RTC YY-MM-DD Register** will be refreshed for at most one second.
6:4	/	/	/
3:2	R/W	0x0	EXT_LOSC_GSM. External 32768Hz Crystal GSM. 00: Low 01: / 10: /

Offset: 0x0000			Register Name: LOSC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			11 High
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL. LOSC Clock source Select. 'N' is the value of Internal OSC Clock Prescalar register. 0: 32KHz 1: External 32.768kHz OSC.

NOTE

If the bit[9:7] of LOSC_CTRL_REG is set, the corresponding Alarm 1 Week HH-MM-SS Register, RTC HH-MM-SS Register, RTC YY-MM-DD Register can not be written.

3.11.6.2. LOSC Auto Switch Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	LOSC_AUTO_SWT_PEND. LOSC auto switch pending. 0: No effect 1: Auto switches pending Writing 1 to this bit will clear it.
0	RO	0x0	LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar register. 0: 32KHz 1: External 32.768kHz OSC

3.11.6.3. Internal OSC Clock Prescalar Register(Default Value: 0x0000_000F)

Offset: 0x0008			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
4:0	R/W	0xF	INTOSC_CLK_PRESCAL. Internal OSC Clock Prescalar value N. 00000: 1 00001: 2 00010: 3 ..... 11111: 512

3.11.6.4. Internal OSC Clock Auto Calibration Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x000C			Register Name: INTOSC_CLK_AUTO_CALI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R	0x0	32k calibration lock count.
15:2	/	/	/
1	R/W	0x0	RC calibration enable
0	R/W	0x0	RC calibration function enable

3.11.6.5. RTC YY-MM-DD Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: RTC_YY_MM_DD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	LEAP. Leap Year. 0: Not 1: Leap year. This bit can not set by hardware. It should be set or cleared by software.
22:16	R/W	0x0	YEAR. Year. Range from 0~127.
14:12	/	/	/
11:8	R/W	0x0	MONTH. Month. Range from 1~12.
7:5	/	/	/
4:0	R/W	0x0	DAY. Day. Range from 1~31.

NOTE

If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area.
The number of days in different month may be different.

3.11.6.6. RTC HH-MM-SS Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /

Offset: 0x0014			Register Name: RTC_HH_MM_SS_REG
Bit	Read/Write	Default/Hex	Description
28:21	/	/	/
20:16	R/W	0x0	HOUR. Range from 0~23
15:14	/	/	/
13:8	R/W	0x0	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	0x0	SECOND. Range from 0~59

NOTE

If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.11.6.7. Alarm 0 Counter Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: ALARM0_COUNTER_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	ALARM0_COUNTER. Alarm 0 Counter is Based on Second. If the second is set to 0, it will be 1 second in fact.

3.11.6.8. Alarm 0 Current Value Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: ALARM0_CUR_VAL_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	ALARM0_CUR_VLU. Check Alarm 0 Counter Current Values. If the second is set to 0, it will be 1 second in fact.

3.11.6.9. Alarm 0 Enable Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: ALARM0_ENABLE_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. If this bit is set to “1”, the valid bits of **Alarm 0 Counter Register** will down count to zero, and the alarm pending bit will be set to “1”. 0: Disable 1: Enable

3.11.6.10. Alarm 0 IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: ALARM0_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x002C			Register Name: ALARM0_IRQ_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN. Alarm 0 IRQ Enable. 0: Disable 1: Enable

3.11.6.11. Alarm 0 IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: ALARM0_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W1C	0x0	ALARM0_IRQ_PEND. Alarm 0 IRQ Pending bit. 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.11.6.12. Alarm 1 Week HH-MM-SS Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: ALARM1_WK_HH_MM_SS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:16	R/W	0x0	HOUR. Range from 0~23.
15:14	/	/	/
13:8	R/W	0x0	MINUTE. Range from 0~59.
7:6	/	/	/
5:0	R/W	0x0	SECOND. Range from 0~59.

NOTE

If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

3.11.6.13. Alarm 1 Enable Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	WK6_ALM1_EN. Week 6 (Sunday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the valid bits of **Alarm 1 Week**

Offset: 0x0044			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			HH-MM-SS Register is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 6, the week 6 alarm irq pending bit will be set to "1".
5	R/W	0x0	WK5_ALM1_EN. Week 5 (Saturday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 5, the week 5 alarm irq pending bit will be set to "1".
4	R/W	0x0	WK4_ALM1_EN. Week 4 (Friday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 4, the week 4 alarm irq pending bit will be set to "1".
3	R/W	0x0	WK3_ALM1_EN. Week 3 (Thursday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 3, the week 3 alarm irq pending bit will be set to "1".
2	R/W	0x0	WK2_ALM1_EN. Week 2 (Wednesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 2, the week 2 alarm irq pending bit will be set to "1".
1	R/W	0x0	WK1_ALM1_EN. Week 1 (Tuesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week HH-MM-SS Register** is equal to the bit[20:0] of **RTC HH-MM-SS Register** and the bit[31:29] of **RTC HH-MM-SS Register** is 1, the week 1 alarm irq pending bit will be set to "1".
0	R/W	0x0	WK0_ALM1_EN. Week 0 (Monday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to "1", only when the valid bits of **Alarm 1 Week**

Offset: 0x0044			Register Name: ALARM1_EN_REG
Bit	Read/Write	Default/Hex	Description
			HH-MM-SS Register is equal to the bit[20:0] of RTC HH-MM-SS Register and the bit[31:29] of RTC HH-MM-SS Register is 0, the week 0 alarm irq pending bit will be set to "1".

3.11.6.14. Alarm 1 IRQ Enable Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: ALARM1_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN. Alarm 1 IRQ Enable. 0: Disable 1: Enable

3.11.6.15. Alarm 1 IRQ Status Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: ALARM1_IRQ_STA_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W1C	0x0	ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect 1: Pending, week counter value is reached If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

3.11.6.16. Alarm Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: ALARM_CONFIG_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

3.11.6.17. General Purpose Register(Default Value: 0x0000_0000)

Offset: 0x0100+N*0x04 (N=0~7)			Register Name: GP_DATA_REGn
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	GP_DATA. Data [31:0].

NOTE

The value of General Purpose Register can be stored if the VDD_RTC is larger than 1.0V.

3.11.6.18. VDD RTC Regulation Register(Default Value: 0x0000_0004)

Offset: 0x0190			Register Name: VDD_RTC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x4	VDD_RTC_REGU. These bits are useful for regulating the RTC_VIO from 0.7V to 1.4V, and the regulation step is 0.1V. 000: 0.7V 001: 0.8V 010: 0.9V 011: 1.0V 100: 1.1V 101: 1.2V 110: 1.3V 111: 1.4V

3.11.6.19. IC Characteristic Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: IC_CHARA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	IC_CHARA. Key Field. The field should be written to 0x16AA. Writing any other value in this field aborts the write operation.
15:0	R/W	0x0	ID_DATA. Return 0x16AA only if the **Key Field** is set as 0x16AA when read those bits, otherwise return 0x0.

3.11.6.20. VDD_SYS Power Off Gating Register(Default Value: 0x0000_0000)

Offset: 0x01F4			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x1	/
11:9	/	/	/
8	R/W	0x0	WAIT_MODE_ENABLE
7:6	R/W	0x0	RTC_GATING_WAIT_TIME_CONTROL_BIT
5	R/W	0x0	RTC_GATING_MODE_BIT 0: Wait mode 1: VDD Off clear mode
4	R/W	0x0	ENABLE_RTC_GATING
3	/	/	/
2	R/W	0x0	AVCC_A_GATING Gating the corresponding modules to the AVCC_A Power Domain when VDD_SYS power off.

Offset: 0x01F4			Register Name: VDD_SYS_PWROFF_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Invalid 1: Valid **This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.**
1	R/W	0x0	DRAM_ZQ_PAD_HOLD. Hold the pad of DRAM channel 0: Not hold 1: Hold DRAM ZQ Pad **This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.**
0	R/W	0x0	DRAM_CH_PAD_HOLD. Hold the pad of DRAM channel 0: Not hold 1: Hold DRAM Pad **This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.**

3.11.6.21. Super Standby Flag Register(Default Value: 0x0000_0000)

Offset: 0x01F8			Register Name:
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	SUP_STANDBY_FLAG. Key Field. Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only fellow the appropriate process, the super standby flag can be written in the lower 16 bits. Refer to Description and Diagram.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA. Refer to Description and Diagram

NOTE

When system is turned on, the low 16 bits of Super Standby Flag Register should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written 0x16AA at first. Then, software programmer must write 0xAA16XXXX in Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID.

3.11.6.22. CPU Software Entry Register(Default Value: 0x0000_0000)

Offset: 0x01FC			Register Name: CPU_SOFT_ENT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CPU_SOFT_ENT. CPU software entry register when acting from super standby.

3.12. Audio Codec

3.12.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplifier.

Features:

- Two audio digital-to-analog(DAC) channels
  - Up to 100±3dB SNR
  - Supports DAC sample rate from 8kHz to 192kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Two audio analog-to-digital(ADC) channels
  - Up to 93±3dB SNR
  - Supports ADC sample rate from 8kHz to 48kHz
  - Supports 16-bit and 24-bit audio sample resolution
- Four audio inputs:
  - Two mono microphone inputs
  - One stereo line-in input
  - One stereo FM-in input
- Two audio outputs:
  - One differential PHONEOUT output
  - One stereo headphone output
- Supports analog/digital volume control
- Supports dynamic range controller adjusting the DAC playback and ADC capture
- One 128x32 bits FIFO for ADC data transmit, one 32x32 bits FIFO for DAC data receive
- Programmable FIFO thresholds
- Interrupt and DMA support

3.12.2. Block Diagram

Figure 3-24 shows a block diagram of the Audio Codec.

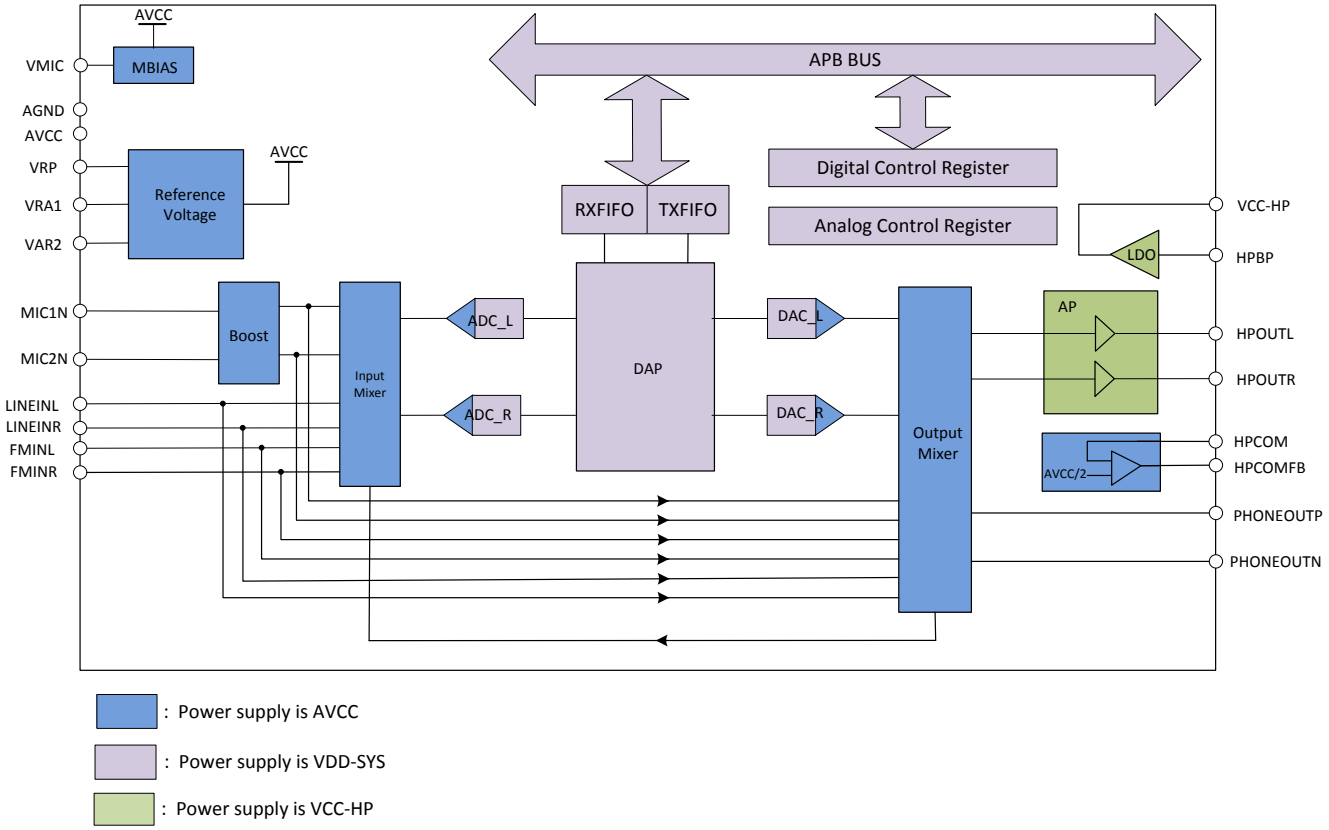


Figure 3-24. Audio Codec Block Diagram

3.12.3. Operations and Functional Descriptions

3.12.3.1. Data Path

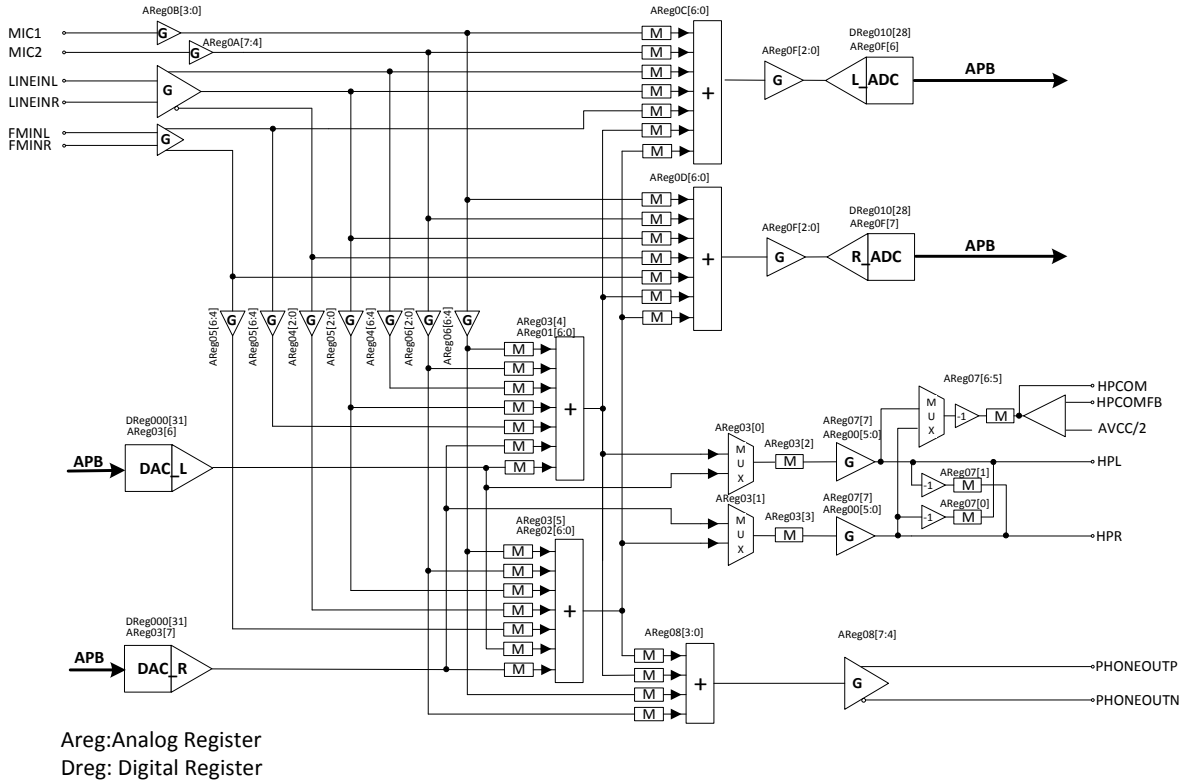


Figure 3-25. Audio Codec Data Path

3.12.3.2. Clock Sources

Figure 3-26 describes the Audio Codec clock source. Users can see **CCU** for clock setting, configuration and gating information.

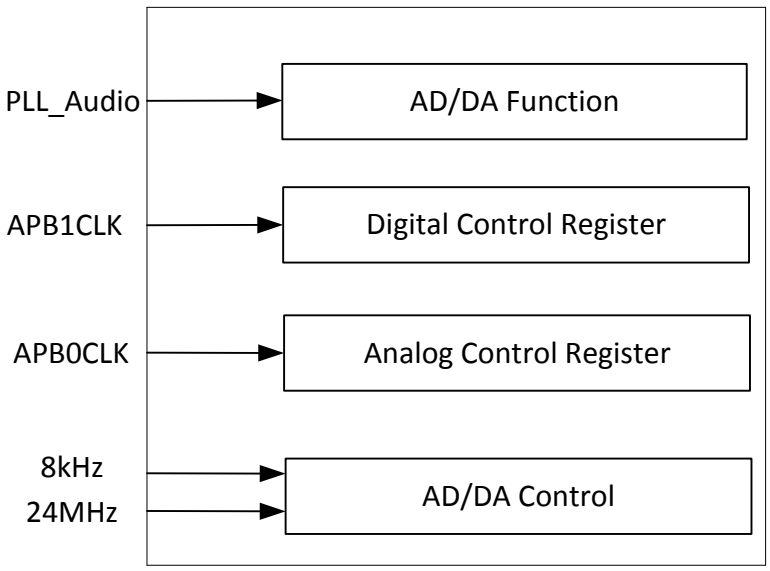


Figure 3-26. Audio Codec Clock Sources Diagram

3.12.4. Register List

Module Name	Base Address
Audio Codec	0x01C22C00

Register Name	Offset	Description
AC_DAC_DPC	0x0000	DAC Digital Part Control Register
AC_DAC_FIFOC	0x0004	DAC FIFO Control Register
AC_DAC_FIFOS	0x0008	DAC FIFO Status Register
AC_ADC_FIFOC	0x0010	ADC FIFO Control Register
AC_ADC_FIFOS	0x0014	ADC FIFO Status Register
AC_ADC_RXDATA	0x0018	ADC RX Data Register
AC_DAC_TXDATA	0x0020	DAC TX Data Register
AC_DAC_CNT	0x0040	DAC TX FIFO Counter Register
AC_ADC_CNT	0x0044	ADC RX FIFO Counter Register
AC_DAC_DG	0x0048	DAC Debug Register
AC_ADC_DG	0x004C	ADC Debug Register
AC_DAC_DAP_CTRL	0x0060	DAC DAP Control Register
AC_DAC_DRC_HHPFC	0x0100	DAC DRC High HPF Coef Register
AC_DAC_DRC_LHPFC	0x0104	DAC DRC Low HPF Coef Register
AC_DAC_DRC_CTRL	0x0108	DAC DRC Control Register
AC_DAC_DRC_LPFHAT	0x010C	DAC DRC Left Peak Filter High Attack Time Coef Register
AC_DAC_DRC_LPFLAT	0x0110	DAC DRC Left Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_RPFHAT	0x0114	DAC DRC Right Peak Filter High Attack Time Coef Register
AC_DAC_DRC_RPFLAT	0x0118	DAC DRC Peak Filter Low Attack Time Coef Register
AC_DAC_DRC_LPFHRT	0x011C	DAC DRC Left Peak Filter High Release Time Coef Register
AC_DAC_DRC_LPFLRT	0x0120	DAC DRC Left Peak Filter Low Release Time Coef Register
AC_DAC_DRC_RPFHRT	0x0124	DAC DRC Right Peak Filter High Release Time Coef Register
AC_DAC_DRC_RPFLRT	0x0128	DAC DRC Right Peak Filter Low Release Time Coef Register
AC_DAC_DRC_LRMSHAT	0x012C	DAC DRC Left RMS Filter High Coef Register
AC_DAC_DRC_LRMSLAT	0x0130	DAC DRC Left RMS Filter Low Coef Register
AC_DAC_DRC_RRMSHAT	0x0134	DAC DRC Right RMS Filter High Coef Register
AC_DAC_DRC_RRMSLAT	0x0138	DAC DRC Right RMS Filter Low Coef Register
AC_DAC_DRC_HCT	0x013C	DAC DRC Compressor Theshold High Setting Register
AC_DAC_DRC_LCT	0x0140	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_HKC	0x0144	DAC DRC Compressor Slope High Setting Register
AC_DAC_DRC_LKC	0x0148	DAC DRC Compressor Slope Low Setting Register
AC_DAC_DRC_HOPC	0x014C	DAC DRC Compressor High Output at Compressor Threshold Register
AC_DAC_DRC_LOPC	0x0150	DAC DRC Compressor Low Output at Compressor Threshold Register
AC_DAC_DRC_HLT	0x0154	DAC DRC Limiter Theshold High Setting Register
AC_DAC_DRC_LLT	0x0158	DAC DRC Limiter Theshold Low Setting Register
AC_DAC_DRC_HKl	0x015C	DAC DRC Limiter Slope High Setting Register
AC_DAC_DRC_LKl	0x0160	DAC DRC Limiter Slope Low Setting Register
AC_DAC_DRC_HOPL	0x0164	DAC DRC Limiter High Output at Limiter Threshold
AC_DAC_DRC_LOPL	0x0168	DAC DRC Limiter Low Output at Limiter Threshold
AC_DAC_DRC_HET	0x016C	DAC DRC Expander Theshold High Setting Register
AC_DAC_DRC_LET	0x0170	DAC DRC Expander Theshold Low Setting Register
AC_DAC_DRC_HKE	0x0174	DAC DRC Expander Slope High Setting Register
AC_DAC_DRC_LKE	0x0178	DAC DRC Expander Slope Low Setting Register

Register Name	Offset	Description
AC_DAC_DRC_HOPE	0x017C	DAC DRC Expander High Output at Expander Threshold
AC_DAC_DRC_LOPE	0x0180	DAC DRC Expander Low Output at Expander Threshold
AC_DAC_DRC_HKN	0x0184	DAC DRC Linear Slope High Setting Register
AC_DAC_DRC_LKN	0x0188	DAC DRC Linear Slope Low Setting Register
AC_DAC_DRC_SFHAT	0x018C	DAC DRC Smooth Filter Gain High Attack Time Coef Register
AC_DAC_DRC_SFLAT	0x0190	DAC DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DAC_DRC_SFHRT	0x0194	DAC DRC Smooth Filter Gain High Release Time Coef Register
AC_DAC_DRC_SFLRT	0x0198	DAC DRC Smooth Filter Gain Low Release Time Coef Register
AC_DAC_DRC_MXGHS	0x019C	DAC DRC MAX Gain High Setting Register
AC_DAC_DRC_MXGLS	0x01A0	DAC DRC MAX Gain Low Setting Register
AC_DAC_DRC_MNGHS	0x01A4	DAC DRC MIN Gain High Setting Register
AC_DAC_DRC_MNGLS	0x01A8	DAC DRC MIN Gain Low Setting Register
AC_DAC_DRC_EPSHC	0x01AC	DAC DRC Expander Smooth Time High Coef Register
AC_DAC_DRC_EPSLC	0x01B0	DAC DRC Expander Smooth Time Low Coef Register
AC_DAC_DRC_OPT	0x01B4	DAC DRC Optimum Register
AC_ADC_DRC_HHPFC	0x0200	ADC DRC High HPF Coef Register
AC_ADC_DRC_LHPFC	0x0204	ADC DRC Low HPF Coef Register
AC_ADC_DRC_CTRL	0x0208	ADC DRC Control Register
AC_ADC_DRC_LPFHAT	0x020C	ADC DRC Left Peak Filter High Attack Time Coef Register
AC_ADC_DRC_LPFLAT	0x0210	ADC DRC Left Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_RPFHAT	0x0214	ADC DRC Right Peak Filter High Attack Time Coef Register
AC_ADC_DRC_RPFLAT	0x0218	ADC DRC Peak Filter Low Attack Time Coef Register
AC_ADC_DRC_LPFHRT	0x021C	ADC DRC Left Peak Filter High Release Time Coef Register
AC_ADC_DRC_LPFLRT	0x0220	ADC DRC Left Peak Filter Low Release Time Coef Register
AC_ADC_DRC_RPFHRT	0x0224	ADC DRC Right Peak Filter High Release Time Coef Register
AC_ADC_DRC_RPFLRT	0x0228	ADC DRC Right Peak Filter Low Release Time Coef Register
AC_ADC_DRC_LRMSHAT	0x022C	ADC DRC Left RMS Filter High Coef Register
AC_ADC_DRC_LRMSLAT	0x0230	ADC DRC Left RMS Filter Low Coef Register
AC_ADC_DRC_RRMSHAT	0x0234	ADC DRC Right RMS Filter High Coef Register
AC_ADC_DRC_RRMSLAT	0x0238	ADC DRC Right RMS Filter Low Coef Register
AC_ADC_DRC_HCT	0x023C	ADC DRC Compressor Theshold High Setting Register
AC_ADC_DRC_LCT	0x0240	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_HKC	0x0244	ADC DRC Compressor Slope High Setting Register
AC_ADC_DRC_LKC	0x0248	ADC DRC Compressor Slope Low Setting Register
AC_ADC_DRC_HOPC	0x024C	ADC DRC Compressor High Output at Compressor Threshold Register
AC_ADC_DRC_LOPC	0x0250	ADC DRC Compressor Low Output at Compressor Threshold Register
AC_ADC_DRC_HLT	0x0254	ADC DRC Limiter Theshold High Setting Register
AC_ADC_DRC_LLT	0x0258	ADC DRC Limiter Theshold Low Setting Register
AC_ADC_DRC_HKl	0x025C	ADC DRC Limiter Slope High Setting Register
AC_ADC_DRC_LKl	0x0260	ADC DRC Limiter Slope Low Setting Register
AC_ADC_DRC_HOPL	0x0264	ADC DRC Limiter High Output at Limiter Threshold
AC_ADC_DRC_LOPL	0x0268	ADC DRC Limiter Low Output at Limiter Threshold
AC_ADC_DRC_HET	0x026C	ADC DRC Expander Theshold High Setting Register
AC_ADC_DRC_LET	0x0270	ADC DRC Expander Theshold Low Setting Register
AC_ADC_DRC_HKE	0x0274	ADC DRC Expander Slope High Setting Register
AC_ADC_DRC_LKE	0x0278	ADC DRC Expander Slope Low Setting Register
AC_ADC_DRC_HOPE	0x027C	ADC DRC Expander High Output at Expander Threshold
AC_ADC_DRC_LOPE	0x0280	ADC DRC Expander Low Output at Expander Threshold
AC_ADC_DRC_HKN	0x0284	ADC DRC Linear Slope High Setting Register
AC_ADC_DRC_LKN	0x0288	ADC DRC Linear Slope Low Setting Register
AC_ADC_DRC_SFHAT	0x028C	ADC DRC Smooth filter Gain High Attack Time Coef Register
AC_ADC_DRC_SFLAT	0x0290	ADC DRC Smooth filter Gain Low Attack Time Coef Register

Register Name	Offset	Description
AC_ADC_DRC_SFHRT	0x0294	ADC DRC Smooth filter Gain High Release Time Coef Register
AC_ADC_DRC_SFLRT	0x0298	ADC DRC Smooth filter Gain Low Release Time Coef Register
AC_ADC_DRC_MXGHS	0x029C	ADC DRC MAX Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A0	ADC DRC MAX Gain Low Setting Register
AC_ADC_DRC_MNGLS	0x02A4	ADC DRC MIN Gain High Setting Register
AC_ADC_DRC_MXGLS	0x02A8	ADC DRC MIN Gain Low Setting Register
AC_ADC_DRC_EPSHC	0x02AC	ADC DRC Expander Smooth Time High Coef Register
AC_ADC_DRC_EPSLC	0x02B0	ADC DRC Expander Smooth Time Low Coef Register
AC_ADC_DRC_OPT	0x02AC	ADC DRC Optimum Register
AC_PR_CFG	0x0300	AC Parameter Configuration Register
Analog domain Register		
AC_PAG_HPV	0x00	PA clock gating and Headphone Volume Control
AC_LOMIXSC	0x01	Left Output Mixer Source Select Control Register
AC_ROMIXSC	0x02	Right Output Mixer Source Select Control Register
DAC_PA_SRC	0x03	DAC Analog Enable and PA Source Control Register
PHONE_GAIN	0x04	Phone Gain Control Regsiter
LINEIN_PHONE_GCTR	0x05	LINEIN and PHONE Gain Control Register
MIC_GCTR	0x06	MIC1 And MIC2 Gain Control Register
HP_CTRL	0x07	HP Control
PHONEOUT	0x08	PHONEOUT Boost and MIXER Control
LOUT_PH_GAIN	0x09	LINEOUT and PHONE Gain Control
MIC2_LINE_CTRL	0x0A	MIC2 Boost LINE-OUT Enable and Source select
BIAS_MIC_CTRL	0x0B	BIAS and MIC2 Source and MIC1 boost
LADC_MIX_MUTE	0x0C	Left ADC Mixer Mute Control
RADC_MIX_MUTE	0x0D	Right ADC Mixer Mute Control
PA_ANTI_POP_CTRL	0x0E	PA Anti-pop Time Control
AC_ADC_CTRL	0x0F	ADC Analog Control Register
OPADC_CTRL	0x10	OPDR and OPCOM and OPADC Control
OPMIC_CTRL	0x11	OPMIC and OPVR and OPADC Control
ZERO_CROSS_CTRL	0x12	Zero Cross Control
ADC_FUN_CTRL	0x13	ADC Function Control
CALIBRATION_CTRL	0x14	Bias & DA16 Calibration Control Register
DA16CALI_DATA	0x15	DA16 Calibration Data
DA16CALI_NULL	0x16	DA16 Calibration Data
BIAS16CALI_DATA	0x17	Bias Calibration Data
BIAS16CALI_SET	0x18	Bias Register Setting Data

3.12.5. Register Description

3.12.5.1. DAC Digital Part Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: AC_DAC_DPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	EN_DAC DAC Digital Part Enable 0 : Disable 1 : Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15

24:19	/	/	/
18	R/W	0x0	HPF_EN High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL Digital Volume Control DVC, ATT=DVC[5:0]*(-1.16Db) 64 steps, -1.16Db/step
11:1	/	/	/
0	R/W	0x0	HUB_EN Audio Hub Enable 0:Disable 1:Enable

3.12.5.2. DAC FIFO Control Register(Default Value: 0x0000_4000)

Offset: 0x004			**Register Name: AC_DAC_FIFOC**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	DAC_FS Sample Rate Of DAC 000: 48kHz 010: 24kHz 100: 12kHz 110: 192kHz 001: 32kHz 011: 16kHz 101: 8kHz 111: 96kHz 44.1kHz/22.05kHz/11.025kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	FIR_VER FIR Version 0: 64-Tap FIR 1: 32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25:24	R/W	0x0	FIFO_MODE For 24-bits transmitted audio sample 00/10: FIFO_I[23:0] = {TXDATA[31:8]} 01/11: Reserved For 16-bits transmitted audio sample: 00/10: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 01/11: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT When TX FIFO Available Room Less Than Or Equal N, DRQ Request Will Be

			De-Asserted. N Is Defined Here: 00: IRQ/DRQ De-Asserted When WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Trigger Level (TXTL[12:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ≤ TXTL **NOTE** **WLEVEL represents the number of valid samples in the TX FIFO.** **Only TXTL[6:0] valid when TXMODE = 0.**
7	R/W	0x0	ADDA_LOOP_EN ADDA Loop Enable 0: Disable 1: Enable
6	R/W	0x0	DAC_MONO_EN DAC Mono Enable 0: Stereo, 64 Levels FIFO 1: Mono, 128 Levels FIFO When Enabled, L & R Channel Send Same Data
5	R/W	0x0	TX_SAMPLE_BITS Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN DAC FIFO Under Run IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W1C	0x0	FIFO_FLUSH DAC FIFO Flush Write ‘1’ to flush TX FIFO, Self clear to ‘0’

3.12.5.3. DAC FIFO Status Register(Default Value: 0x0080_0088)

Offset: 0x0008			Register Name: AC_DAC_FIFOS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x1	TX_EMPTY TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatically clear if interrupt condition fails
2	R/W1C	0x0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

3.12.5.4. ADC FIFO Control Register(Default Value: 0x0000_0F00)

Offset: 0x0010			Register Name: AC_ADC_FIFOC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	R/W	0x0	ADFS Sample Rate of ADC 000: 48kHz 010: 24kHz 100: 12kHz 110: Reserved 001: 32kHz 011: 16kHz 101: 8kHz 111: Reserved 44.1kHz/22.05kHz/11.025kHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD ADC Digital Part Enable 0: Disable 1: Enable

27:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE RX FIFO Output Mode (Mode 0, 1) 0: Expanding '0' at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0} Mode 1: Reserved For 16-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:19	/	/	/
18:17	R/W	0x0	ADCFDT ADC FIFO Delay Time for writing Data after EN_AD 00:5ms 01:10ms 10:20ms 11:30ms
16	R/W	0x0	ADCDFEN ADC FIFO Delay Function for writing Data after EN_AD 0: Disable 1: Enable
15:13	/	/	/
12:8	R/W	0xF	RX_FIFO_TRG_LEVEL RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for RX FIFO normal condition IRQ/DRQ Generated when WLEVEL > RXTL[4:0] **NOTE** **WLEVEL represents the number of valid samples in the RX FIFO.**
7	R/W	0x0	ADC_MONO_EN ADC Mono Enable 0: Stereo, 16 levels FIFO 1: mono, 32 levels FIFO When set to '1', Only left channel samples are recorded
6	R/W	0x0	RX_SAMPLE_BITS Receiving Audio Sample Resolution 0: 16 bit 1: 24 bit
5	/	/	/
4	R/W	0x0	ADC_DRQ_EN ADC FIFO Data Available DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC_IRQ_EN ADC FIFO Data Available IRQ Enable 0: Disable

			1: Enable
2	/	/	
1	R/W	0x0	ADC_OVERRUN_IRQ_EN ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W1C	0x0	ADC_FIFO_FLUSH ADC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

3.12.5.5. ADC FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: AC_ADC_FIFOS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:14	/	/	/
13:8	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W1C	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails
2	/	/	/
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

3.12.5.6. ADC RX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: AC_ADC_RXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

3.12.5.7. DAC TX DATA Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_DAC_TXDATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

3.12.5.8. DAC TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: AC_DAC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **NOTE** **It is used for Audio/ Video Synchronization.**

3.12.5.9. ADC RX Counter Register(Default Value : 0x0000_0000)

Offset: 0x0044			Register Name: AC_ADC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. **NOTE** **It is used for Audio/ Video Synchronization.**

3.12.5.10. DAC Debug Register(Default Value : 0x0000_0000)

Offset: 0x0048			Register Name: AC_DAC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11	R/W	0x0	DAC_MODU_SELECT DAC Modulator Debug 0: DAC Modulator Normal Mode 1: DAC Modulator Debug Mode
10:9	R/W	0x0	DAC_PATTERN_SELECT. DAC Pattern Select 00: Normal (Audio Sample from TX FIFO)

			01: -6 dB Sin wave 10: -60 dB Sin wave 11: Silent wave
8	R/W	0x0	CODEC_CLK_SELECT CODEC Clock Source Select 0: CODEC Clock from PLL 1: CODEC Clock from OSC (for Debug)
7	/	/	/
6	R/W	0x0	DA_SWP DAC output channel swap enable 0: Disable 1: Enable
5:0	/	/	/

3.12.5.11. ADC Debug Register(Default Value : 0x0000_0000)

Offset: 0x004C			Register Name: AC_ADC_DG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	AD_SWP ADC Output Channel Swap Enable (for digital filter) 0: Disable 1: Enable
23:0	/	/	/

3.12.5.12. HMIC Control Register(Default Value : 0x0000_0000)

Offset: 0x0050			Register Name: HMIC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HMIC_M Debounce when key down or key up
27:24	R/W	0x0	HMIC_N Debounce when earphone plug in or pull out
23	R/W	0x0	HMIC_DATA_IRQ_MODE HMIC Data Irq Mode Select 0: HMIC data irq once after key down 1: HMIC data irq from key down, until key up
22:21	R/W	0x0	HMIC_TH1_HYSTERESIS HMIC Hysteresis Threshold1 00: No Hysteresis 01: Pull Out when Data <= (Hmic_th2-1) 10: Pull Out when Data <= (Hmic_th2-2) 11: Pull Out when Data <= (Hmic_th2-3)
20	R/W	0x0	HMIC_PULLOUT_IRQ HMIC Earphone Pull out Irq Enable 0: Disable 1: Enable

19	R/W	0x0	HMIC_PLUGIN_IRQ HMIC Earphone Plug in Irq Enable 0: Disable 1: Enable
18	R/W	0x0	HMIC_KEYUP_IRQ HMIC Key Up Irq Enable 0: Disable 1: Enable
17	R/W	0x0	HMIC_KEYDOWN_IRQ HMIC Key Down Irq Enable 0: Disable 1: Enable
16	R/W	0x0	HMIC_DATA_IRQ_EN HMIC Data Irq Enable 0: Disable 1: Enable
15:14	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11: Down by 8, 16Hz
13	R/W	0x0	HMIC_TH2_HYSTERESIS Hmic Hysteresis Threshold2 0: No Hysteresis 1: Key up when Data <= (Hmic_th2-1)
12:8	R/W	0x0	HMIC_TH2 HMIC_th2 for detecting key down or key up.
7:6	R/W	0x0	HMIC_SF HMIC Smooth Filter Setting 00: by pass 01: (x1+x2)/2 10: (x1+x2+x3+x4)/4 11: (x1+x2+x3+x4+x5+x6+x7+x8)/8
5	R/W	0x0	KEYUP_CLEAR Key up irq pending bit auto clear when key down Irq 0: Don't clear 1: Auto clear
4:0	R/W	0x0	HMIC_TH1 HMIC_th1[4:0], detecting eraphone plug in or pull out.

3.12.5.13. HMIC Data Register(Default Value : 0x0000_0000)

Offset: 0x0054			Register Name: HMIC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/

20	R/W1C	0x0	HMIC_PULLOUT_PENDING HMIC earphone pull out Irq pending bit, write 1 to clear it 0: No pending interrupt 1: Pull out irq pending interrupt
19	R/W1C	0x0	HMIC_PLUGIN_PENDING HMIC earphone plug in irq pending bit, write 1 to clear it 0: No pending interrupt 1: Plug in irq pending interrupt
18	R/W1C	0x0	HMIC_KEYUP_PENDING HMIC key up irq pending bit, write 1 to clear it 0: No pending interrupt 1: Key up irq pending interrupt
17	R/W1C	0x0	HMIC_KEYDOWN_PENDING HMIC key down irq pending bit, write 1 to clear it 0: No pending interrupt 1: Key down irq pending interrupt
16	R/W1C	0x0	HMIC_DATA_PENDING HMIC data irq pending bit, write 1 to clear it 0: No pending interrupt 1: Data irq pending interrupt
15:5	/	/	/
4:0	R	0x0	HMIC_DATA HMIC ADC Data

3.12.5.14. DAC DAP Control Register(Default Value : 0x6000_0000)

Offset: 0x0060			**Register Name: AC_DAC_DAP_CTR**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DDAP _EN DAP for dac Enable 0 : Bypass 1 : Enable
30:16	/	/	/
15	R/W	0x0	DDAP_DRC_EN DRC enable control 0: Disable 1: Enable
14	R/W	0x0	DDAP_HPF_EN HPF enable control 0: Disable 1: Enable
13:7	/	/	/
6:0	R/W	0x0	RAM_ADDR Ram address It will increase by one when the APB reading or writing the ram. When the APB writing or reading the ram, it must enable DAP (0x60.bit31) and disable

			BQ, DRC, DE, HPF firstly.

3.12.5.15. ADC DAP Control Register(Default Value : 0x0000_0000)

Offset: 0x0070			Register Name: AC_ADC_DAP_CTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	ENADC_DRC DRC for ADC enable 0 : Bypass 1 : Enable
25	R/W	0x0	ADC_DRC_EN ADC DRC function enable 0 : Disable 1 : Enable
24	R/W	0x0	ADC_DRC_HPF_EN ADC DRC HPF function enable 0 : Disable 1 : Enable
23:0	/	/	/

3.12.5.16. DAC DRC High HPF Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0100			Register Name: AC_DAC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

3.12.5.17. DAC DRC Low HPF Coef Register(Default Value: 0x0000_FAC1)

Offset: 0x0104			Register Name: AC_DAC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

3.12.5.18. DAC DRC Control Register(Default Value: 0x0000_0080)

Offset: 0x0108			Register Name: AC_DAC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enble and the drc funciton disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0. 0 : Not complete 1 : Complete
14	/	/	/

13:8	R/W	0x0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc disable and the drc buffer data output completely 0 : Don't use the buffer 1 : Use the buffer
6	R/W	0x0	DRC gain max limit enable 0 : Disable 1 : Enable
5	R/W	0x0	DRC gain min limit enable. when this fuction enable, it will overwrite the noise detect funciton. 0 : Disable 1 : Enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0 : Disable 1 : Enable
3	R/W	0x0	Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0 : Disable 1 : Enable When the Delay function enable is disabled, the Signal delay time is unused.
1	R/W	0x0	DRC LT enable 0 : Disable 1 : Enable When the DRC LT is disabled the LT, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0 : Disable 1 : Enable When the DRC ET is disabled the ET, Ke and OPE parameter is unused.

3.12.5.19. DAC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x010C			Register Name: AC_DAC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.20. DAC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0110			Register Name: AC_DAC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.21. DAC DRC Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x0114			Register Name: AC_DAC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.22. DAC DRC Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0118			Register Name: AC_DAC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.23. DAC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x011C			Register Name: AC_DAC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0FF	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.24. DAC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0120			Register Name: AC_DAC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.25. DAC DRC Right Peak filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0124			Register Name: AC_DAC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0FF	The left peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.26. DAC DRC Right Peak filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0128			Register Name: AC_DAC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.27. DAC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x012C			Register Name: AC_DAC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x001	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.28. DAC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0130			Register Name: AC_DAC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.29. DAC DRC Right RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x0134			Register Name: AC_DAC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x001	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.30. DAC DRC Right RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0138			Register Name: AC_DAC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.31. DAC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x013C			Register Name: AC_DAC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

3.12.5.32. DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0140			Register Name: AC_DAC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

3.12.5.33. DAC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0144			Register Name: AC_DAC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 6.24. (2 : 1)

3.12.5.34. DAC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0148			Register Name: AC_DAC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 6.24. (2 : 1)

3.12.5.35. DAC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)

Offset: 0x014C			Register Name: AC_DAC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The output of the compressor which determine by the equation -OPC/6.0206 The format is 8.24 (-40dB)

3.12.5.36. DAC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0150	Register Name: AC_DAC_DRC_LOPC

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor which determine by the equation OPC/6.0206 The format is 8.24 (-40dB)

3.12.5.37. DAC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0154			Register Name: AC_DAC_DRC_HLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

3.12.5.38. DAC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0158			Register Name: AC_DAC_DRC_LLT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

3.12.5.39. DAC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x015C			Register Name: AC_DAC_DRC_HKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter which determine by the equation that Kl = 1/R, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

3.12.5.40. DAC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0160			Register Name: AC_DAC_DRC_LKl
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

3.12.5.41. DAC DRC Limiter High Output at Limiter Threshold(Default Value: 0x0000_FBD8)

Offset: 0x0164			Register Name: AC_DAC_DRC_HOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

3.12.5.42. DAC DRC Limiter Low Output at Limiter Threshold(Default Value: 0x0000_FBA7)

Offset: 0x0168			Register Name: AC_DAC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

3.12.5.43. DAC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x016C			Register Name: AC_DAC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

3.12.5.44. DAC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0170			Register Name: AC_DAC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

3.12.5.45. DAC DRC Expander Slope High Setting Register(Default Value: 0x0000_0500)

Offset: 0x0174			Register Name: AC_DAC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0500	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

3.12.5.46. DAC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0178			Register Name: AC_DAC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

3.12.5.47. DAC DRC Expander High Output at Expander Threshold(Default Value: 0x0000_F45F)

Offset: 0x017C			Register Name: AC_DAC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

3.12.5.48. DAC DRC Expander Low Output at Expander Threshold(Default Value: 0x0000_8D6E)

Offset: 0x0180			Register Name: AC_DAC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

3.12.5.49. DAC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0184			Register Name: AC_DAC_DRC_HKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0100	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 6.24. (1:1)

3.12.5.50. DAC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: AC_DAC_DRC_LKN
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 6.24. (1:1)

3.12.5.51. DAC DRC Smooth filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x018C			Register Name: AC_DAC_DRC_SFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x002	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

3.12.5.52. DAC DRC Smooth filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0190			Register Name: AC_DAC_DRC_SFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

3.12.5.53. DAC DRC Smooth filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: AC_DAC_DRC_SFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/

10:0	R/W	0x000	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

3.12.5.54. DAC DRC Smooth filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0198			Register Name: AC_DAC_DRC_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

3.12.5.55. DAC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x019C			Register Name: AC_DAC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

3.12.5.56. DAC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x01A0			Register Name: AC_DAC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

3.12.5.57. DAC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x01A4			Register Name: AC_DAC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

3.12.5.58. DAC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x01A8			Register Name: AC_DAC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting which determine by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

3.12.5.59. DAC DRC Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x01AC			Register Name: AC_DAC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	/	/	/

11:0	R/W	0x000	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

3.12.5.60. DAC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x01B0			Register Name: AC_DAC_DRC_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

3.12.5.61. DAC DRC Optimum Register (internal use)(Default Value: 0x0000_0000)

Offset: 0x01B4			Register Name: AC_DAC_DRC_OPT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10	R/W	0x0	The gain smooth use the expander coiffcient when the energy in expander range 0 : use the normal smooth coeffcient 1 : use the expander coeffcient
9	R/W	0x0	The gain normal smooth coefficeint selection mode set 0 : both release and attack coeffcient use hysteresis 1 : only the attack coeffcient use hysteresis
8	R/W	0x0	The min of energy set in Peak detect mode 0 : -120dB 1 : -210dB
7	R/W	0x0	The energy mode select in rms detect mode 0 : the energy is RMS 1 : the energy is square of RMS
6	R/W	0x0	DRC data ouput when DRC disable and DRC delay data output complete 0 : the ouput is the input music data; 1 : the output is 0
5	R/W	0x0	DRC gain defaut value setting 0: The default gain is 1 1: The default gain is 0
4:0	R/W	0x00	The hysteresis of the gain smooth filter to use the decay time coefficient or the attack time coefficient. When in the decay time state, if g(n-1)-g(n)>hysteresis, then the state will change to attack time state, and when in the attack time, if g(n)-g(n-1)>hysteresis, then the state will change to decay time state. Note the hysteresis of 0x00 and 0x04 is the same. 00000: 2^(-20)

			00001: 2^(-19) 00010: 2^(-18) ---------- 10011: 2^(-1) 10100 ~11111: 1 hysteresis = 2^(n-20) ,except n=0x00, and n less 0x14.

3.12.5.62. DAC DRC HPF Gain High Coef Register(Default Value: 0x0000_0100)

Offset: 0x01B8			Register Name: AC_DAC_DRC_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

3.12.5.63. DAC DRC HPF Gain Low Coef Register(Default Value: 0x0000_0000)

Offset: 0x01BC			Register Name: AC_DAC_DRC_HPFLGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

3.12.5.64. ADC DRC High HPF Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0200			Register Name: AC_ADC_DRC_HHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

3.12.5.65. ADC DRC Low HPF Coef Register(Default Value: 0x0000_FAC1)

Offset: 0x0204			Register Name: AC_ADC_DRC_LHPFC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

3.12.5.66. ADC DRC Control Register(Default Value: 0x0000_0080)

Offset: 0x0208			Register Name: AC_ADC_DRC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x0	DRC delay buffer data output state when drc delay function is enble and the drc funciton disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0 0 : Not complete 1 : Complete
14	/	/	/
13:8	R/W	0x0	Signal delay time setting

			6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc disable and the drc buffer data output completely 0 : Don't use the buffer 1 : Use the buffer
6	R/W	0x0	DRC gain max limit enable 0 : Disable 1 : Enable
5	R/W	0x0	DRC gain min limit enable. when this fuction enable, it will overwrite the noise detect function 0 : Disable 1 : Enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0 : Disable 1 : Enable
3	R/W	0x0	Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused. (AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0 : Disable 1 : Enable When the bit is disabled, the signal delay time is unused.
1	R/W	0x0	DRC LT enable 0 : Disable 1 : Enable When the DRC LT is disabled the LT, KI and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0 : Disable 1 : Enable When the DRC ET is disabled the ET, Ke and OPE parameter is unused.

3.12.5.67. ADC DRC Left Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x020C			Register Name: AC_ADC_DRC_LPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.68. ADC DRC Left Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0210			Register Name: AC_ADC_DRC_LPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.69. ADC DRC Right Peak Filter High Attack Time Coef Register(Default Value: 0x0000_000B)

Offset: 0x0214			Register Name: AC_ADC_DRC_RPFHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x00B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.70. ADC DRC Peak Filter Low Attack Time Coef Register(Default Value: 0x0000_77BF)

Offset: 0x0218			Register Name: AC_ADC_DRC_RPFLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

3.12.5.71. ADC DRC Left Peak Filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x021C			Register Name: AC_ADC_DRC_LPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0FF	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.72. ADC DRC Left Peak Filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0220			Register Name: AC_ADC_DRC_LPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.73. ADC DRC Right Peak filter High Release Time Coef Register(Default Value: 0x0000_00FF)

Offset: 0x0224			Register Name: AC_ADC_DRC_RPFHRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x0FF	The left peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.74. ADC DRC Right Peak filter Low Release Time Coef Register(Default Value: 0x0000_E1F8)

Offset: 0x0228			Register Name: AC_ADC_DRC_RPFLRT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

3.12.5.75. ADC DRC Left RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x022C			Register Name: AC_ADC_DRC_LRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x001	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.76. ADC DRC Left RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0230			Register Name: AC_ADC_DRC_LRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.77. ADC DRC Right RMS Filter High Coef Register(Default Value: 0x0000_0001)

Offset: 0x0234			Register Name: AC_ADC_DRC_RRMSHAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x001	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.78. ADC DRC Right RMS Filter Low Coef Register(Default Value: 0x0000_2BAF)

Offset: 0x0238			Register Name: AC_ADC_DRC_RRMSLAT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/

15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

3.12.5.79. ADC DRC Compressor Theshold High Setting Register(Default Value: 0x0000_06A4)

Offset: 0x023C			Register Name: AC_ADC_DRC_HCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x06A4	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

3.12.5.80. ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_D3C0)

Offset: 0x0240			Register Name: AC_ADC_DRC_LCT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xD3C0	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

3.12.5.81. ADC DRC Compressor Slope High Setting Register(Default Value: 0x0000_0080)

Offset: 0x0244			Register Name: AC_ADC_DRC_HKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0080	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 6.24. (2 : 1)

3.12.5.82. ADC DRC Compressor Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0248			Register Name: AC_ADC_DRC_LKC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 6.24. (2 : 1)

3.12.5.83. ADC DRC Compressor High Output at Compressor Threshold Register(Default Value: 0x0000_F95B)

Offset: 0x024C			Register Name: AC_ADC_DRC_HOPC
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xF95B	The output of the compressor which determine by the equation -OPC/6.0206 The format is 8.24 (-40dB)

3.12.5.84. ADC DRC Compressor Low Output at Compressor Threshold Register(Default Value: 0x0000_2C3F)

Offset: 0x0250			Register Name: AC_ADC_DRC_LOPC
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15:0	R/W	0x2C3F	The output of the compressor which determine by the equation OPC/6.0206 The format is 8.24 (-40dB)

3.12.5.85. ADC DRC Limiter Theshold High Setting Register(Default Value: 0x0000_01A9)

Offset: 0x0254			Register Name: AC_ADC_DRC_HLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x01A9	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

3.12.5.86. ADC DRC Limiter Theshold Low Setting Register(Default Value: 0x0000_34F0)

Offset: 0x0258			Register Name: AC_ADC_DRC_LLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x34F0	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

3.12.5.87. ADC DRC Limiter Slope High Setting Register(Default Value: 0x0000_0005)

Offset: 0x025C			Register Name: AC_ADC_DRC_HKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0005	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

3.12.5.88. ADC DRC Limiter Slope Low Setting Register(Default Value: 0x0000_1EB8)

Offset: 0x0260			Register Name: AC_ADC_DRC_LKl
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x1EB8	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 6.24. (50 :1)

3.12.5.89. ADC DRC Limiter High Output at Limiter Threshold(Default Value: 0x0000_FBD8)

Offset: 0x0264			Register Name: AC_ADC_DRC_HOPL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFBD8	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

3.12.5.90. ADC DRC Limiter Low Output at Limiter Threshold(Default Value: 0x0000_FBA7)

Offset: 0x0268			Register Name: AC_ADC_DRC_LOPL
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xFBA7	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

3.12.5.91. ADC DRC Expander Theshold High Setting Register(Default Value: 0x0000_0BA0)

Offset: 0x026C			Register Name: AC_ADC_DRC_HET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0BA0	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

3.12.5.92. ADC DRC Expander Theshold Low Setting Register(Default Value: 0x0000_7291)

Offset: 0x0270			Register Name: AC_ADC_DRC_LET
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x7291	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

3.12.5.93. ADC DRC Expander Slope High Setting Register(Default Value: 0x0000_0500)

Offset: 0x0274			Register Name: AC_ADC_DRC_HKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0500	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

3.12.5.94. ADC DRC Expander Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0278			Register Name: AC_ADC_DRC_LKE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x0000	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 1/50. The format is 6.24. (1:5)

3.12.5.95. ADC DRC Expander High Output at Expander Threshold(Default Value: 0x0000F45F)

Offset: 0x027C			Register Name: AC_ADC_DRC_HOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0xF45F	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

3.12.5.96. ADC DRC Expander Low Output at Expander Threshold(Default Value: 0x0000_8D6E)

Offset: 0x0280			Register Name: AC_ADC_DRC_LOPE
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0x8D6E	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

3.12.5.97. ADC DRC Linear Slope High Setting Register(Default Value: 0x0000_0100)

Offset: 0x0284			**Register Name: AC_ADC_DRC_HKN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	/	/	/
13:0	R/W	0x0100	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

3.12.5.98. ADC DRC Linear Slope Low Setting Register(Default Value: 0x0000_0000)

Offset: 0x0288			**Register Name: AC_ADC_DRC_LKN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

3.12.5.99. ADC DRC Smooth filter Gain High Attack Time Coef Register(Default Value: 0x0000_0002)

Offset: 0x028C			**Register Name: AC_ADC_DRC_SFHAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x002	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

3.12.5.100. ADC DRC Smooth filter Gain Low Attack Time Coef Register(Default Value: 0x0000_5600)

Offset: 0x0290			**Register Name: AC_ADC_DRC_SFLAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

3.12.5.101. ADC DRC Smooth filter Gain High Release Time Coef Register(Default Value: 0x0000_0000)

Offset: 0x0294			**Register Name: AC_ADC_DRC_SFHRT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/

10:0	R/W	0x000	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

3.12.5.102. ADC DRC Smooth filter Gain Low Release Time Coef Register(Default Value: 0x0000_0F04)

Offset: 0x0298			Register Name: AC_ADC_DRC_SFLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

3.12.5.103. ADC DRC MAX Gain High Setting Register(Default Value: 0x0000_FE56)

Offset: 0x029C			Register Name: AC_ADC_DRC_MXGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFE56	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

3.12.5.104. ADC DRC MAX Gain Low Setting Register(Default Value: 0x0000_CB0F)

Offset: 0x02A0			Register Name: AC_ADC_DRC_MXGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xCB0F	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

3.12.5.105. ADC DRC MIN Gain High Setting Register(Default Value: 0x0000_F95B)

Offset: 0x02A4			Register Name: AC_ADC_DRC_MNGHS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xF95B	The min gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

3.12.5.106. ADC DRC MIN Gain Low Setting Register(Default Value: 0x0000_2C3F)

Offset: 0x02A8			Register Name: AC_ADC_DRC_MNGLS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x2C3F	The min gain setting which determine by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -40dB (-40dB)

3.12.5.107. ADC DAP Expander Smooth Time High Coef Register(Default Value: 0x0000_0000)

Offset: 0x02AC			Register Name: AC_ADC_DRC_EPSHC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:12	/	/	/

11:0	R/W	0x000	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

3.12.5.108. ADC DRC Expander Smooth Time Low Coef Register(Default Value: 0x0000_640C)

Offset: 0x02B0			Register Name: AC_ADC_DRC_EPSLC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

3.12.5.109. ADC DRC Optimum Register (internal use)(Default Value: 0x0000_0000)

Offset: 0x02B4			Register Name: AC_ADC_DRC_OPT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10	R/W	0x0	The gain smooth use the expander coefficient when the energy in expander range 0 : Use the normal smooth coefficient 1 : Use the expander coefficient
9	R/W	0x0	The gain normal smooth coefficient selection mode set 0 : Both release and attack coefficient use hysteresis 1 : Only the attack coefficient use hysteresis
8	R/W	0x0	The min of energy set in peak detect mode 0 : -120dB 1 : -210dB
7	R/W	0x0	The energy mode select in rms detect mode 0 : The energy is RMS 1 : The energy is square of RMS
6	R/W	0x0	DRC data output when DRC disable and DRC delay data output complete. 0 : The output is the input music data 1 : The output is 0
5	R/W	0x0	DRC gain default value setting 0: The default gain is 1 1: The default gain is 0
4:0	R/W	0x00	The hysteresis of the gain smooth filter to use the decay time coefficient or the attack time coefficient. When in the decay time state, if g(n-1)-g(n)>hysteresis, then the state will change to attack time state, and when in the attack time, if g(n)-g(n-1)>hysteresis, then the state will change to decay time state. Note the hysteresis of 0x00 and 0x04 is the same. 00000: 2^(-20)

			00001: 2^(-19) 00010: 2^(-18) ---------- 10011: 2^(-1) 10100 ~11111: 1 hysteresis = 2^(n-20),except n=0x00, and n less 0x14.

3.12.5.110. ADC DRC HPF Gain High(Default Value: 0x0000_0100)

Offset: 0x02B8			Register Name: AC_ADC_DRC_HPFHGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:11	/	/	/
10:0	R/W	0x100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

3.12.5.111. ADC DRC HPF Gain Low(Default Value: 0x0000_0000)

Offset: 0x02BC			Register Name: AC_ADC_DRC_HPFLGAIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

3.12.5.112. ADDA_PR Configuration Register(Default Value: 0x1000_0000)

Address: 0x0300			Register Name: ADDA_PR_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	ADDA_PR_RST. ADDA_PR Reset. 0: Assert 1: De-assert
27:25	/	/	/
24	R/W	0x0	ADDA_PR_RW. ADDA_PR Read or Write. 0: Read 1: Write
23:21	/	/	/
20:16	R/W	0x0	ADDA_PR _ADDR. ADDA_PR Address[4:0].
15:8	R/W	0x0	ADDA_PR _WDAT. ADDA_PR Write Data [7:0].
7:0	R/W	0x0	ADDA_PR _RDAT. ADDA_PR Read Data[7:0].

3.12.6. Audio Codec Analog Part Configuration IO Register Description

The Audio Codec Analog Part is configured by the **ADDA_PR_CFG_REG** Register which definition is below.

The **ADDA_PR_RST** bit can reset this register. **ADDA_PR_CFG_REG** defines the analog register address which we would control, and the **ADDA_PR_RW** decides the operation is to read or write. When the operation is to read, we would read the analog register's data from the **ADDA_PR_RDAT**. When the operation is to write, we would write the **ADDA_PR_WDAT** value to the **ADDA_PR_CFG_REG** register.

Address: 0x01c22f00			**Register Name: ADDA_PR_CFG_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x1	ADDA_PR_RST. ADDA_PR Reset. 0: Assert 1: De-assert
27:25	/	/	/
24	R/W	0x0	ADDA_PR_RW. ADDA_PR Read or Write. 0: Read 1: Write
23:21	/	/	/
20:16	R/W	0x0	ADDA_PR_ADDR. ADDA_PR Address[4:0].
15:8	R/W	0x0	ADDA_PR_WDAT. ADDA_PR Write Data [7:0].
7:0	R/W	0x0	ADDA_PR_RDAT. ADDA_PR Read Data[7:0].

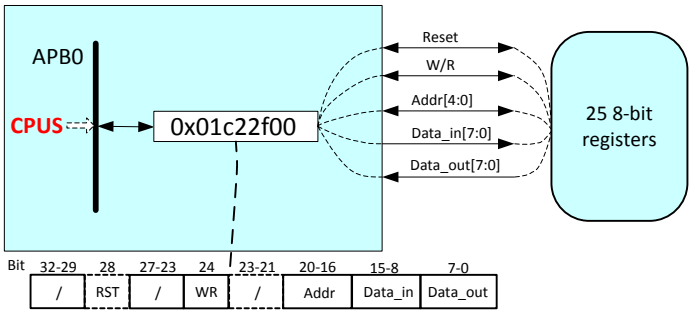


Figure 3-27. ADDA_PR_ADDR Analog Register

3.12.6.1. 00h Headphone Volume Control Register(Default Value: 0x00)

Offset: 0x00			**Register Name: HP_VOLC**
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	PA clock gating control when system VDD is off and Audio analog channel is working, this bit must be set to 1, because the PA clock come from system VDD domain. When this bit is 1, the Zero cross over function will be disabled automatically. 0: Not gating

Offset: 0x00			Register Name: HP_VOLC
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Gating
6	R/W	0x0	/
5:0	R/W	0x0	HPVOL Headphone Volume Control: Total 64 level, from 0dB to -62dB, 1dB/step, mute when 000000

3.12.6.2. 01h Left Output Mixer Source Control Register(Default Value: 0x00)

Offset: 0x01			Register Name: LOMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	/
6:0	R/W	0x0	LMIXMUTE Left Output Mixer Mute Control 0: Mute 1: Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEN Bit 2: LINEINL Bit 1: Left channel DAC Bit 0: Right channel DAC

3.12.6.3. 02h Right Output Mixer Source Control Register(Default Value: 0x00)

Offset: 0x02			Register Name: LOMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	RMIXMUTE Right Output Mixer Mute Control 0: Mute 1: Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEP Bit 2: LINEINR Bit 1: Right channel DAC Bit 0: Left channel DAC

3.12.6.4. 03h DAC Analog Enable and PA Source Control Register(Default Value: 0x00)

Offset: 0x03			Register Name: DAC_PA_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x03			Register Name: DAC_PA_SRC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	DACAREN Internal Analog Right channel DAC Enable 0:Disable 1:Enable
6	R/W	0x0	DACALEN Internal Analog Left channel DAC Enable 0:Disable 1:Enable
5	R/W	0x0	RMIXEN Right Analog Output Mixer Enable 0:Disable 1:Enable
4	R/W	0x0	LMIXEN Left Analog Output Mixer Enable 0:Disable 1:Enable
3	R/W	0x0	RHPPAMUTE All input source to Right Headphone PA mute, including Right Output mixer and Internal Right channel DAC 0:Mute 1: Not mute
2	R/W	0x0	LHPPAMUTE All input source to Left Headphone PA mute, including Left Output mixer and Internal Left channel DAC 0:Mute 1: Not mute
1	R/W	0x0	RHPIS Right Headphone Power Amplifier (PA) Input Source Select 0: Right channel DAC 1: Right Analog Mixer
0	R/W	0x0	LHPIS Left Headphone Power Amplifier (PA) Input Source Select 0: Left channel DAC 1: Left Analog Mixer

3.12.6.5. 04h Phonein Stereo Gain Control Register(Default Value: 0x33)

Offset: 0x04			Register Name: PHONEIN_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	/
6:4	R/W	0x3	PHONEPG, (volpnp) PHONEP to Right output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

Offset: 0x04			Register Name: PHONEIN_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	/
2:0	R/W	0x3	PHONENG, (volpnn) PHONEN to Left output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

3.12.6.6. 05h Linein and Phone Gain Control Register(Default Value: 0x33)

Offset: 0x05			Register Name: LINEIN_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x3	LINEING, (volln) LINEINL/R to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	/	/	/
2:0	R/W	0x3	PHONEG, (volpg) PHONE(P-N) gain stage to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

3.12.6.7. 06h MIC1 and MIC2 Gain Control Register(Default Value: 0x33)

Offset: 0x06			Register Name: MICIN_GCTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	/
6:4	R/W	0x3	MIC1G (volm1) MIC1 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	/
2:0	R/W	0x3	MIC2G (volm2) MIC2 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

3.12.6.8. 07h PA Enable and HP Control Register(Default Value: 0x14)

Offset: 0x07			Register Name: PAEN_HP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	HPPAEN Right & Left Headphone Power Amplifier Enable 0: Disable 1: Enable
6:5	R/W	0x0	HPCOM_FC HPCOM function control 00: HPCOM off & output is floating 01: HPL inverting output

Offset: 0x07			Register Name: PAEN_HP_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			10: HPR inverting output 11: Direct driver for HPL & HPR
4	R/W	0x1	COMPTEN HPCOM output protection enable when it is set as Direct driver for HPL/R 0: Protection disable 1: Protection enable
3:2	R/W	0x1	PA_ANTI_POP_CTRL (slopelengthsel) PA Anti-pop time Control 00:131ms 01: 262ms 10: 393ms 11:524ms
1	R/W	0x0	LTRNMUTE (hprisinvhpl) Left HPOUT Negative to Right HPOUT Mute 0: Mute 1: Not mute
0	R/W	0x0	RTLNMUTE (hplisinvhpr) Right HPOUT Negative to Left HPOUT Mute 0: Mute 1: Not mute

3.12.6.9. 08h Phoneout Control Register(Default Value: 0x60)

Offset: 0x08			Register Name: PHONEOUT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:5	R/W	0x3	PHONEOUTG Phone-out Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
4	R/W	0x0	PHONEOUT enable 0: Disable 1:Enable
3	R/W	0x0	PHONEOUTS3 MIC1 Boost stage to Phone out mute 0: Mute 1: Not mute
2	R/W	0x0	PHONEOUTS2 MIC2 Boost stage to Phone out mute 0: Mute 1: Not mute
1	R/W	0x0	PHONEOUTS1 Right Output mixer to Phone out mute

Offset: 0x08			Register Name: PHONEOUT_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Mute 1: Not mute
0	R/W	0x0	PHONEOUTS0 Left Output mixer to Phone out mute 0: Mute 1: Not mute

3.12.6.10. 0Ah Mic2 Boost and Lineout Enable Control Register(Default Value: 0x40)

Offset: 0x0A			Register Name: MIC2G_LINEEN_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0: Disable 1: Enable
6:4	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, the default is 33dB
3	/	/	/

3.12.6.11. 0Bh Mic1 Boost and MICBIAS Control Register(Default Value: 0x14)

Offset: 0x0B			Register Name: MIC1G_MICBIAS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	HMICBIASEN Headset Microphone Bias enable 0: Disable 1: Enable
6	R/W	0x0	MMICBIASEN Master Microphone Bias enable 0: Disable 1: Enable
5	R/W	0x0	HMICBIAS MODE Headset MIC Bias Mode select 0: HMICBIAS auto suspend when HMIC is absent 1: HMICBIAS always on when 0B_[7] is 1
4	R/W	0x1	MIC2 Source select 0: MICIN3 1: MICIN2

Offset: 0x0B			Register Name: MIC1G_MICBIAS_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0: Disable 1: Enable
2:0	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, the default is 33dB

3.12.6.12. 0Ch Left ADC Mixer Source Control Register(Default Value: 0x00)

Offset: 0x0C			Register Name: LADCMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:0	R/W	0x0	LADCMIXMUTE Left ADC Mixer Mute Control 0: Mute 1: Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEN Bit 2: LINEINL Bit 1: Left output mixer Bit 0: Right output mixer

3.12.6.13. 0Dh Right ADC Mixer Source Control Register(Default Value: 0x00)

Offset: 0x0D			Register Name: RADCMIXSC
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	/
6:0	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control 0: Mute 1: On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEP Bit 2: LINEINR Bit 1: Right output mixer Bit 0: Left output mixer

3.12.6.14. 0Eh PA Anti-pop Time Control Register(Default Value: 0x04)

Offset: 0x0E			Register Name: PAANTIPOPTC
Bit	**Read/Write**	**Default/Hex**	**Description**
7:3	/	/	/
2:0	R/W	0x4	PA_ANTI_POP_CTRL (slopelengthsel) PA Anti-pop time Control 000: 131ms 001: 262ms 010: 393ms 011: 524ms 100: 655ms 101: 786ms 110: 786ms 111: 1048ms

3.12.6.15. 0Fh ADC Analog Part Enable Register(Default Value: 0x03)

Offset: 0x0F			Register Name: ADC_AP_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	ADCREN ADC Right Channel Enable 0: Disable 1: Enable
6	R/W	0x0	ADCLEN ADC Left Channel Enable 0: Disable 1: Enable
5:3	/	/	/
2:0	R/W	0x3	ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB

3.12.6.16. 10h ADDA Analog Performance Turning 0 Register(Default Value: 0x55)

Offset: 0x10			Register Name: ADDA_APT0
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x1	OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting
5:4	R/W	0x1	OPADC1_BIAS_CUR. OPADC1 Bias Current Select
3:2	R/W	0x1	OPADC2_BIAS_CUR. OPADC2 Bias Current Select
1:0	R/W	0x1	OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select

3.12.6.17. 11h ADDA Analog Performance Turning 1 Register(Default Value: 0x55)

Offset: 0x11			Register Name: ADDA_APT1
Bit	**Read/Write**	**Default/Hex**	**Description**
7:6	R/W	0x1	OPMIC_BIAS_CUR OPMIC Bias Current Control
5:4	R/W	0x1	OPVR_BIAS_CUR. OPVR Bias Current Control Especially, bit 5 can also control HPCOMFB 0: HPCOMFB pin can be used to PA when R07_[6:5] is not 11 1: HPCOMFB pin always can not be used to PA
3:2	R/W	0x1	OPDAC_BIAS_CUR. OPDAC Bias Current Control
1:0	R/W	0x1	OPMIX_BIAS_CUR. OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control

3.12.6.18. 12h ADDA Analog Performance Turning 2 Register(Default Value: 0x42)

Offset: 0x12			Register Name: ADDA_APT2
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	Function enable for master volume change at zero cross over 0: Disable 1: Enable
6	R/W	0x1	Timeout control for master volume change at zero cross over 0: 32ms 1: 64ms
5:4	R/W	0x0	PTDBS HPCOM protect de-bounce time setting 00: 2-3ms 01: 4-6ms 10: 8-12ms 11: 16-24ms
3	R/W	0x0	PA_SLOPE_SELECT PA slope select cosine or ramp 0: Select cosine 1: Select ramp
2:0	R/W	0x2	USB_BIAS_CUR. USB bias current tuning From 23uA to 30uA, Default is 25uA

3.12.6.19. 13h Chopper& Dither Control Register(Default Value: 0xD6)

Offset: 0x13			Register Name: Bias_CD_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x1	MMIC BIAS chopper enable 0: Disable

Offset: 0x13			Register Name: Bias_CD_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable
6:5	R/W	0x2	MMIC BIAS chopper clock select 00: 250kHz 01: 500kHz 10: 1MHz 11: 2MHz
4	R/W	0x1	DITHER ADC dither on/off control 0: Dither off 1: Dither on
3:2	R/W	0x1	DITHER_CLK_SELECT ADC dither clock select 00: ADC FS * (8/9), about 43kHz when FS=48kHz 01: ADC FS * (16/15), about 51kHz when FS=48kHz 10: ADC FS * (4/3), about 64kHz when FS=48kHz 11: ADC FS * (16/9), about 85kHz when FS=48kHz
1:0	R/W	0x2	BIHE_CTRL, BIHE control 00: no BIHE 01: BIHE=7.5 HOSC 10: BIHE=11.5 HOSC 11: BIHE=15.5 HOSC

3.12.6.20. 14h Bias & DA16 Calibration Control Register(Default Value: 0x00)

Offset: 0x14			Register Name: Bias_DA16_CAL_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
7	R/W	0x0	PA_SPEED_SELECT PA setup speed control (for testing) 0: slow 1: fast
6	R/W	0x0	CURRENT_TEST_SELECT Internal current sink test enable (from LINEIN pin) 0:Normal 1: For Debug
5	R/W	0x0	/
4	R/W	0x0	BIAS and DA16 calibration clock select 0: 1kHz 1: 500Hz
3	R/W	0x0	BIAS calibration mode select 0: Average 1: Single
2	R/W	0x0	BIAS and DA16 calibration control Write 1 to this bit, the calibration will be done again. Then this bit will

Offset: 0x14			Register Name: Bias_DA16_CAL_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			be reseted to zero automatically
1	R/W	0x0	BIASCALIVERIFY Bias Calibration Verify 0: Calibration 1: Register setting
0	/	/	/

3.12.6.21. 15h DA16 Calibration Data Register(Default Value: 0x80)

Offset: 0x15			Register Name: DA16_CALI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x80	DA16CALI DA16 Calibration Data

3.12.6.22. 16h DA16 Setting Data Register(Default Value: 0x80)

Offset: 0x16			Register Name: DA16_SET_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x80	/

3.12.6.23. 17h Bias Calibration Data Register(Default Value: 0x20)

Offset: 0x17			Register Name: BIAS_CALI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x20	BIASCALI Bias Calibration Data, 6bit

3.12.6.24. 18h Bias Setting Data Register(Default Value: 0x20)

Offset: 0x18			Register Name: BIAS_SET_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x20	BIASVERIFY Bias Register Setting Data, 6bit

3.13. KEYADC

3.13.1. Overview

KEYADC is 6-bit resolution ADC for key application. The KEYADC can work up to 250Hz conversion rate.

Features:

- Supports interrupt
- Supports Hold Key and General Key
- Supports Single Key and Continue key mode
- 6-bit resolution
- Sample rate up to 250Hz
- Up to two channels
- Supports voltage input range from 0V to 2V

3.13.2. Block Diagram

Figure 3-28 shows a block diagram of the KEYADC.

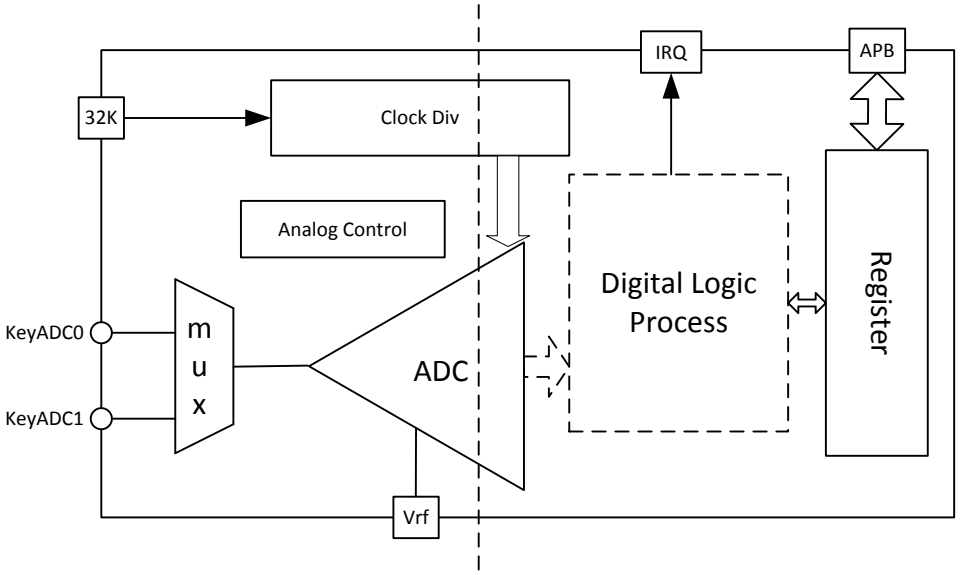


Figure 3-28. KEYADC Block Diagram

3.13.3. Operations and Functional Descriptions

3.13.3.1. External Signals

Table 3-6 describes the external signals of KEYADC. The KEYADC0 and KEYADC1 are the analog input signals for two channels.

Table 3-6. KEYADC External Signals

Signal	Description	Type

KEYADC0	ADC channel0 for key application	AI
KEYADC1	ADC channel1 for key application	AI

3.13.3.2. Clock Sources

KEYADC get one clock source. Table 3-7 describes the clock source for KEYADC. Users can see **CCU** for clock setting, configuration and gating information.

Table 3-7. KEYADC Clock Sources

Clock Sources	Description
LOSC	32KHz Clock, default is External 32.768kHz OSC

3.13.3.3. KEYADC Work Mode

(1). Normal Mode

ADC gathers 8 samples, the average of the 8 samples is updated in data register, and the data interrupt sign is enabled. It is sampled repeatedly according to this mode until ADC stop.

(2). Continue Mode

ADC gathers 8 samples every other 8*(N+1) sample cycle. The average of the 8 samples gathered at every time is updated in the data register, and the data interrupt sign is enabled.(N is defined in the bit[19:16] of **KEYADC_CTRL_REG**).

(3). Single Mode

ADC gathers 8 samples, the average of the 8 samples is updated in data register, and the data interrupt sign is enabled, since then ADC stops sample.

3.13.4. Programming Guidelines

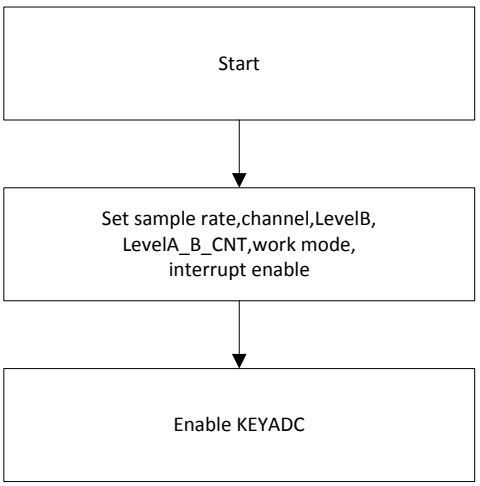


Figure 3-29. KEYADC Initial Process

(1). Set CONTINUE_TIME_SELECT when KEYADC works in continue mode.
(2).The input voltage need be controlled in the range from 0 to LEVELB_VOL(LEVELB_VOL is defined in the bit[5:4] of **KEYADC_CTRL**).

(3).KEYADC formula: KEYADC_DATA = Vin/V_{REF}*63 (V_{REF}=2.0V).
(4).KEYADC has 6-bit resolution, 1-bit offset error, 1-bit quantizing error. After KEYADC calibrates 1-bit offset error, KEYADC has 5-bit resolution.

The initial process of KEYADC has 2 modes.

(1). Query Mode
Step1: Write 0x2 to the bit[23:22] of KEYADC_CTRL to set ADC channel select mode.
Step2: Write 0x0 to the bit[13:12] of KEYADC_CTRL to set normal mode.
Setp3: Write 0x2 to the bit[3:2] of KEYADC_CTRL to set KEYADC sample rate.
Step4: Write 0x1 to the bit[0] of KEYADC_CTRL to enable ADC_EN.
Step5: Read the bit[8]/bit[0] of KEYADC_INT, when the data flag is 1, then data conversion is complete.
Step6: Read the bit[5:0] of KEYADC_DATA0/KEYADC_DATA1, calculate voltage value based on KEYADC formula.

(2). Interrupt Mode
Step1: Write 0x2 to the bit[23:22] of KEYADC_CTRL to set ADC channel select mode.
Step2: Write 0x0 to the bit[13:12] of KEYADC_CTRL to set normal mode.
Step3: Write 0x2 to the bit[3:2] of KEYADC_CTRL to set KEYADC sample rate.
Step4: Write 0x1 to the bit[8]/bit[0] of KEYADC_INTC to enable ADC1_DATA_IRQ_EN/ADC0_DATA_IRQ_EN.
Step5: Set GIC interface based on IRQ 63, write 0x1 to the bit[31] of the **0x01C81104** register.
Step6: Put interrupt handler address into interrupt vector table based on IRQ 63.
Step7: Write 0x1 to the bit[0] of KEYADC_CTRL to enable ADC_EN.
Step8: Read the bit[8]/bit[0] of **KEYADC_INT** in interrupt handler, if the value is 1, temperature conversion is complete.
Step9: Read the bit[5:0] of KEYADC_DATA0/KEYADC_DATA1 in interrupt handler, calculate voltage value based on KEYADC formula.

3.13.5. Register List

Module Name	Base Address
KEYADC	0x01C24400

Register Name	Offset	Description
KEYADC_CTRL	0x0000	KEYADC Control Register
KEYADC_INTC	0x0004	KEYADC Interrupt Control Register
KEYADC_INTS	0x0008	KEYADC Interrupt Status Register
KEYADC_DATA0	0x000C	KEYADC Data Register 0
KEYADC_DATA1	0x0010	KEYADC Data Register 1

3.13.6. Register Description

3.13.6.1. KEYADC Control Register(Default Value: 0x0100_0168)

Offset: 0x0000			Register Name: KEYADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 24	R/W	0x1	FIRST_CONCERT_DLY. ADC First Convert Delay Setting. ADC conversion is delayed by n samples
23:22	R/W	0x0	ADC_CHAN_SELECT. ADC channel select

Offset: 0x0000			Register Name: KEYADC_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			00: ADC0 channel 01: ADC1 channel 1x: ADC0&ADC1 channel
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode Time Select. Every other 8*(N+1) sample as a valuable sample data.
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B Time Threshold Select. Judge ADC convert value from level A to level B in n+1 samples.
7	/	/	/
6	R/W	0x1	KEYADC_CHANNEL_EN. KEYADC Channel Enable 0: Disable 1: Enable
5:4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value Setting (the real voltage value) 00: 0x3C (~1.9V) 01: 0x39 (~1.8V) 10: 0x36 (~1.7V) 11: 0x33 (~1.6V)
3: 2	R/W	0x2	KEYADC_SAMPLE_RATE. KEYADC Sample Rate 00: 250Hz 01: 125Hz 10: 62.5Hz 11: 32.25Hz
1	/	/	/
0	R/W	0x0	KEYADC_EN. KEYADC Enable 0: Disable 1: Enable

3.13.6.2. KEYADC Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: KEYADC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
12	R/W	0x0	ADC1_KEYUP_IRQ_EN. ADC1 Key Up IRQ Enable 0: Disable

Offset: 0x0004			Register Name: KEYADC_INTC
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN. ADC1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC1_HOLD_IRQ_EN. ADC1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYIRQ_EN. ADC1 Key IRQ Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN. ADC1 DATA IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN. ADC0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN. ADC0 Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN. ADC0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC 0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN. ADC 0 Data IRQ Enable 0: Disable 1: Enable

3.13.6.3. KEYADC Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: KEYADC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/

Offset: 0x0008			Register Name: KEYADC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
12	R/W1C	0x0	ADC1_KEYUP_PENDING. ADC 1 Key up Pending When the General Key pulls up, the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
11	R/W1C	0x0	ADC1_ALRDY_HOLD_PENDING. ADC 1 Already Hold Pending When Hold key is in the pull-down state, at this time the general key is pulled down, then **ADC1_ALRDY_HOLD_PENDING** is set 1 by hardware if the **ADC1_ALRDY_HOLD_IRQ_EN** bit is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled
10	R/W1C	0x0	ADC1_HOLDKEY_PENDING. ADC 1 Hold Key Pending When the hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt bit is enabled. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
9	R/W1C	0x0	ADC1_KEYDOWN_IRQ_PENDING. ADC 1 Key Down IRQ Pending When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
8	R/W1C	0x0	ADC1_DATA_IRQ_PENDING. ADC 1 Data IRQ Pending 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
7:5	/	/	/
4	R/W1C	0x0	ADC0_KEYUP_PENDING. ADC 0 Key up Pending When general key pull up, the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W1C	0x0	ADC0_ALRDY_HOLD_PENDING. ADC 0 Already Hold Pending

Offset: 0x0008			Register Name: KEYADC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
			When Hold key is in the pull-down state, at this time the general key is pulled down, then **ADC0_ALRDY_HOLD_PENDING** is set 1 by hardware if the **ADC0_ALRDY_HOLD_IRQ_EN** bit is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W1C	0x0	ADC0_HOLDKEY_PENDING. ADC 0 Hold Key Pending When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W1C	0x0	ADC0_KEYDOWN_PENDING. ADC 0 Key Down IRQ Pending When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	ADC0_DATA_PENDING. ADC 0 Data IRQ Pending 0: No IRQ 1: IRQ Pending Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

3.13.6.4. KEYADC Data 0 Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: KEYADC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x0	KEYADC0_DATA. KEYADC 0 Data

3.13.6.5. KEYADC Data 1 Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: KEYADC_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R	0x0	KEYADC1_DATA. KEYADC 1 Data

3.14. RTP

3.14.1. Overview

The RTP controller is a 4-wire resistive touch screen controller, including 12-bit resolution A/D converter. Especially, it provides the ability of dual touch detection. The controller through the implementation of the two A/D conversions has been identified by the location of the screen of single touch, in addition to measurable increase in pressure on the touch screen.

Features:

- 12-bit SAR type A/D converter
- 4-wire I/F
- Dual touch detection
- Touch-pressure measurement (Supports programmable threshold)
- Sampling frequency up to 2MHz
- Single-ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Supports X, Y change

3.14.2. Operations and Functional Descriptions

3.14.2.1. Clock Tree

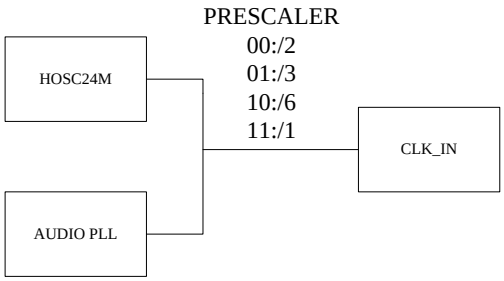


Figure 3-30. RTP Clock Tree

3.14.2.2. A/D Conversion Time

When the clock source is 24MHz and the prescaler value is 6, total 12-bit conversion time is as following:

CLK_IN = 24MHz/6 = 4MHz

Conversion Time = 1/(4MHz/13Cycles) = 3.25us

FS_TIME (Frequency Scan Time) bases on TACQ and Touch Mode, they must meet the following inequation: FS_TIME >= M*(TACQ + Conversion Time)

For example, if touch acquire time divider is 15, then TACQ = 4MHz /(16*(15+1)) = 64us. When RTP mode is dual and pressure measurement mode, then M=6, and the FS_TIME must be no less than 6*(64 + 3.25) us.

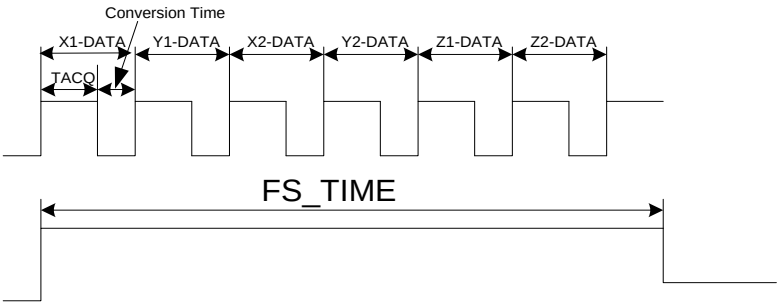


Figure 3-31. Dual Touch and Pressure Measurement

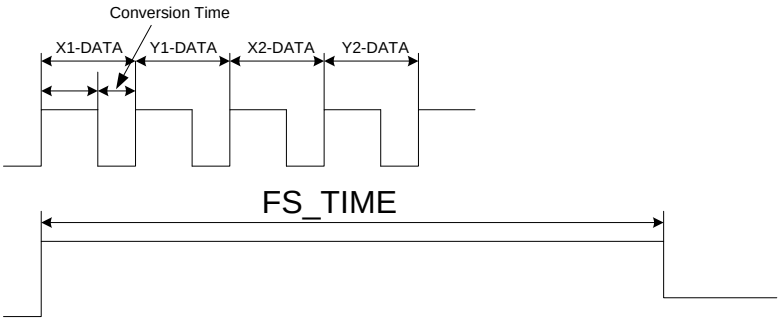


Figure 3-32. Dual Touch No Pressure Measurement

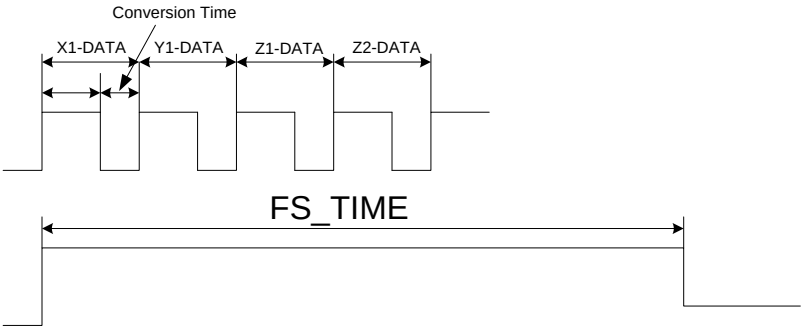


Figure 3-33. Single Touch and Pressure Measurement Mode

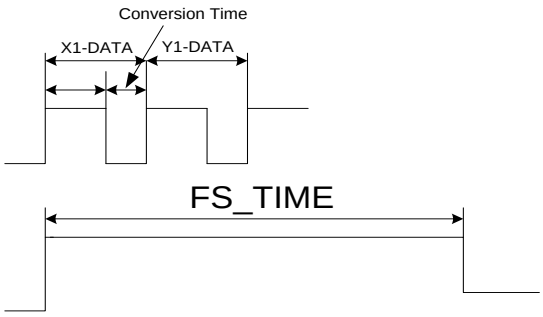


Figure 3-34. Single Touch No Pressure Measurement Mode

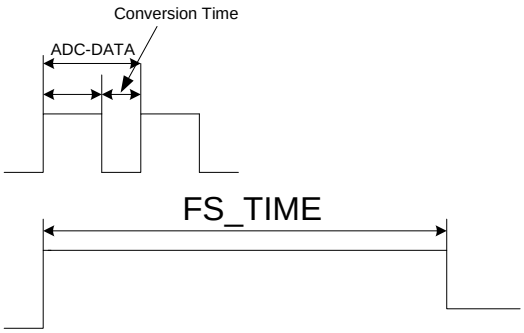


Figure 3-35. General ADC Mode

3.14.2.3. Principle of Operation

(1). Basic Principle

The controller is a typical type of successive approximation ADC (SAR ADC), contains a sample/hold, analog-to-digital conversion, serial data output functions. The analog inputs (X+,X-,Y+,Y-) via control register enter the ADC, ADC can work in single-ended or differential mode. Selecting Aux ADC or temperature should work in single-ended mode; as a touch screen application, it works in a differential mode, which can effectively eliminate the impact on conversion accuracy caused by the parasitic resistance of the driver switch and external interference.

(2). Single-Ended Mode

When the RTP controller is in the measurement mode of AUX or Temp, the internal ADC is in single-ended mode, using the 3V reference source as the ADC reference voltage, application of the principle of single-ended mode is shown below:

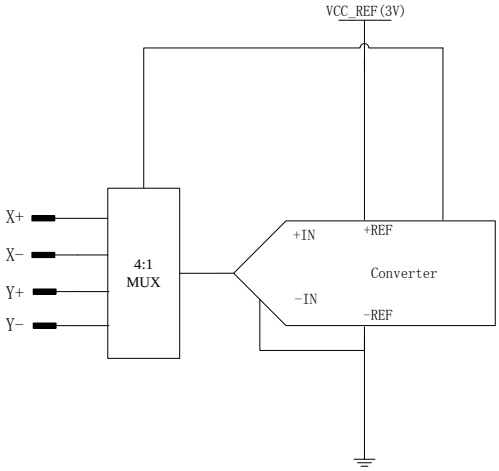


Figure 3-36. Simplified Diagram of Single-Ended Reference

(3). Differential Mode

When the RTP controller is in the measurement mode of X,Y,Z, the internal ADC is in differential mode. The advantage of differential mode is that +REF and –REF can input directly to the Y+, Y-, which can eliminate measurement error because of the switch on resistance. The disadvantage is that during both the sample and conversion process, the driver will need to be on, which will increase the power consumption.

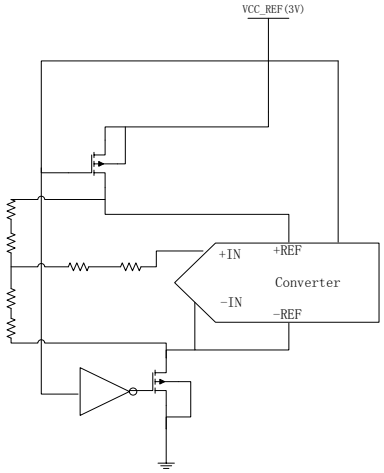


Figure 3-37. Simplified Diagram of Differential Reference

(4). Single Touch Detection

The principle of operation is illustrated below, for an X coordinate measurement, the X+ pin is internally switched to VCC_REF and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the Y+, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. Y coordinate measurements are similar to X coordinate measurements, with the X and Y plates interchanged. In Single Touch mode, only need to test X+, Y+ signal. But In Dual Touch mode, it need to test X+, X-,Y+,Y- signal.

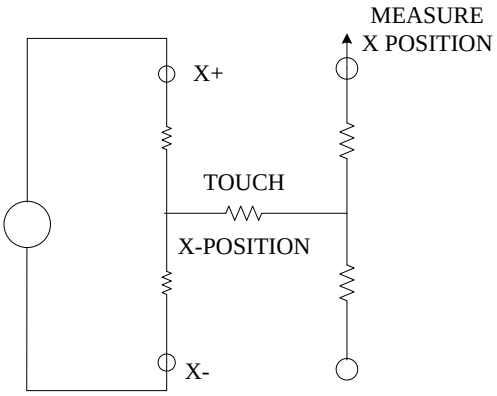


Figure 3-38. Single Touch X-Position Measurement

(5). Dual Touch Detection

The principle of operation is illustrated below, for an X coordinate measurement, the X+ pin is internally switched to 3V and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X coordinate. This voltage is measured on the Y+ and Y-, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. the controller will need to test X+,X-,Y+,Y- , and record ΔX=|X+ - X-|, ΔY= | Y+ - Y-|. In practice, we can set a threshold. If ΔX or ΔY greater than the threshold, we consider it as a dual touch, otherwise as a single touch.

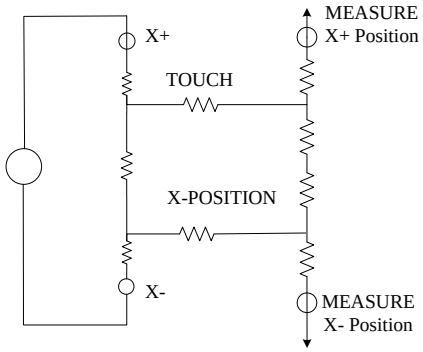


Figure 3-39. Dual Touch X-Position Measurements

(6). Touch-Pressure Measurement

The pressure applied to the touch screen by a pen or finger to filter unavailable can also be measured by the controller using some simple calculations. The contact resistance between the X and Y plates is measured, provide a good indication of the size of the depressed area and the applied pressure. The area of the touch spot t is proportional to the size of the object touching it. And the value of this resistance (R_{touch}) can be calculated using two different methods.

(7). First Method

The first method requires the user to know the total resistance of the X plate tablet (R_{XPLATE}). Three touch screen conversions are required: measurement of the X position, $X_{POSITION}$(Y+ input); measurement of the X+ input with the excitation voltage applied to Y+ and X− (Z1 measurement); and measurement of the Y− input with the excitation voltage applied to Y+ and X− (Z2 measurement). These three measurements are illustrated in Figure 3-40. The controller have two special ADC channel settings to configure the X and Y switches for the Z1 and Z2 measurements and store the results in the Z1 and Z2 result registers. The touch resistance (R_{TOUCH}) can then be calculated using the

following equation:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION} /4096) \times [(Z2/Z1) - 1] \quad (1)$$

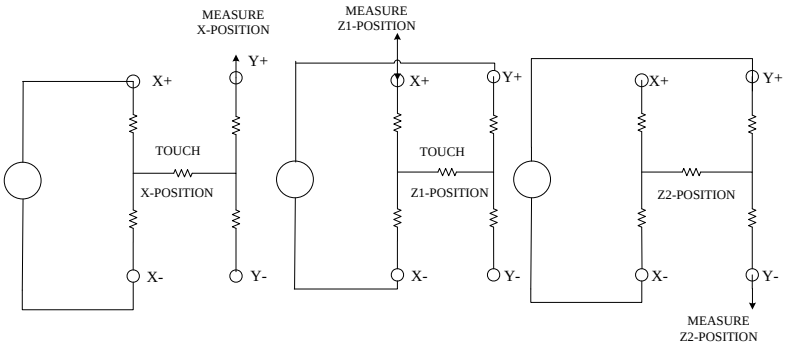


Figure 3-40. Pressure Measurement Block Diagram

(8). Second Method

The second method requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position. The following equation also calculates the touch resistance (R_{TOUCH}):

$$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times [(4096/Z1) - 1] - R_{YPLATE} \times [1 - (Y_{POSITION}/4096)] \quad (2)$$

(9). Median and Averaging Filter

As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements. The controller contain a filtering block to process the data and discard the spurious noise before sending the information to the host. The purpose of this block is not only the suppression of noise; the on-chip filtering also greatly reduces the host processing loading. The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter. The median filter suppresses the isolated out-of-range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Then the averaging filter size determines the number of values to average. There are four choises which is configured by RTP_CTRL3 register (bit 1 and bit 0) to filtrate the ADC sampling data. It is shown in following table.

Table 3-8. Median and Averaging Filter Size (RTP_CTRL3)

bit1	bit0	Averaging Filter Size	Median Filter Size
0	0	2	4
0	1	3	5
1	0	4	8
1	1	8	16

In this example, the RTP_CTRL3 register bit 1 and bit 0 is configured as 2'b11. So the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array. The averaging window size in this example is 8. The output is the average of the middle eight values of the 16 measurements taken with the median filter.

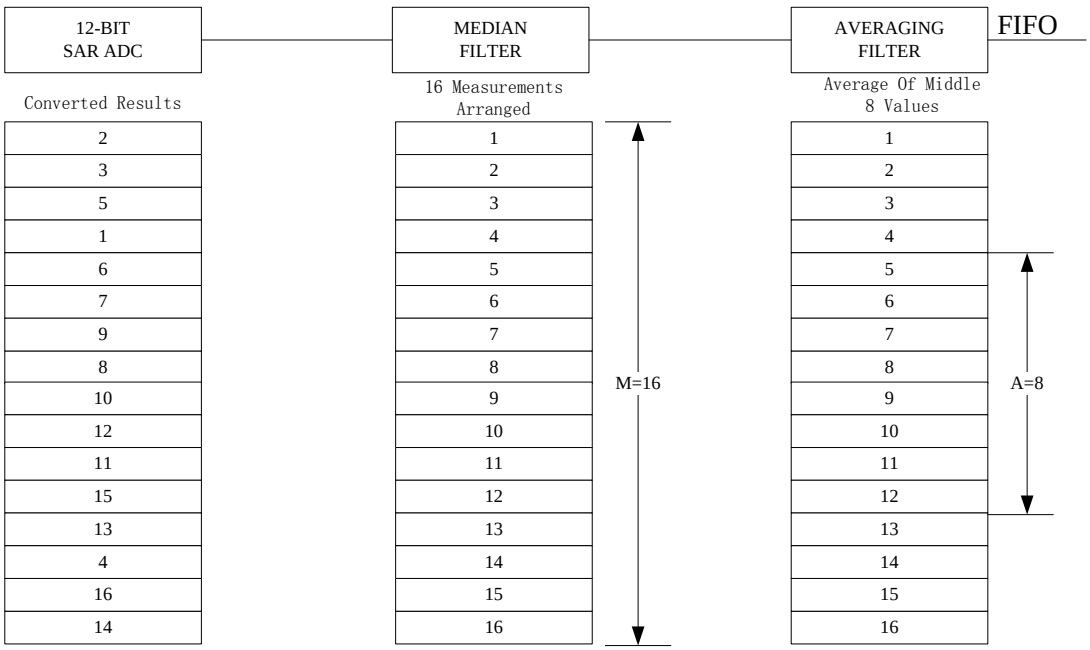


Figure 3-41. Median and Averaging Filter Example

3.14.3. Register List

Module Name	Base Address
RTP	0x01C25000

Register Name	Offset	Description
RTP_CTRL0	0x0000	RTP Control Register0
RTP_CTRL1	0x0004	RTP Control Register1
RTP_CTRL2	0x0008	RTP Pressure Measurement and Touch Sensitive Control Register
RTP_CTRL3	0x000C	Median and Averaging Filter Controller Register
RTP_INT_FIFOC	0x0010	RTP Interrupt FIFO Control Register
RTP_INT_FIFOS	0x0014	RTP Interrupt FIFO Status Register
RTP_CDAT	0x001C	RTP Common Data
RTP_DATA	0x0024	RTP Data Register
RTP_IO_CONFIG	0x0028	RTP IO Configuration
RTP_PORT_DATA	0x002C	RTP IO Port Data

3.14.4. Register Description

3.14.4.1. RTP Control Register 0(Default Value:0x0F80_0000)

Offset: 0x0000			Register Name: RTP_CTRL0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0xF	ADC_FIRST_DLY. ADC First Convert Delay Time(T_FCDT)setting

Offset: 0x0000			Register Name: RTP_CTRL0
Bit	**Read/Write**	**Default/Hex**	**Description**
			Based on ADC First Convert Delay Mode select (Bit 23) T_FCDT = **ADC_FIRST_DLY** * **ADC_FIRST_DLY_MODE**
23	R/W	0x1	ADC_FIRST_DLY_MODE. ADC First Convert Delay Mode Select 0: CLK_IN/16 1: CLK_IN/16*256
22	R/W	0x0	ADC_CLK_SELECT. ADC Clock Source Select 0: HOSC(24MHz) 1: Audio PLL
21:20	R/W	0x0	ADC_CLK_DIVIDER. ADC Clock Divider(CLK_IN) 00: CLK/2 01: CLK/3 10: CLK/6 11: CLK/1
19:16	R/W	0x0	FS_DIV. ADC Sample Frequency Divider 0000: CLK_IN/$2^{(20-n)}$ 0001: CLK_IN/$2^{(20-n)}$ 0010: CLK_IN/$2^{(20-n)}$ .... 1111: CLK_IN/32
15:0	R/W	0x0	TACQ. Touch panel ADC acquire time CLK_IN/(16*(N+1))

3.14.4.2. RTP Control Register 1(Default Value:0x0000_0101)

Offset: 0x0004			Register Name: RTP_CTRL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:12	R/W	0x0	STYLUS_UP_DEBOUNCE. Stylus up De-bounce Time Setting 0x00: 0 .... 0xff: 2N*(CLK_IN/16*256)
11:10	/	/	/
9	R/W	0x0	STYLUS_UP_DEBOUCE_EN. Stylus up De-bounce Function Select 0: Disable 1: Enable

8	R/W	0x1	CHOP_TEMP_EN Chop Temperature Calibration Enable 0: Disable 1: Enable
7	R/W	0x0	TOUCH_PAN_CALI_EN. Touch Panel Calibration 1: Start calibration, it is cleared to 0 after calibration
6	R/W	0x0	RTP_DUAL_EN. Touch Panel Double Point Enable 0: Disable 1: Enable
5	R/W	0x0	RTP_MODE_EN. RTP Mode Function Enable 0: Disable 1: Enable
4	R/W	0x0	RTP_ADC_SELECT. Touch Panel and ADC Select 0: TP 1: ADC
3	R/W	0x0	ADC_CHAN3_SELECT Analog Input Channel 3 Select 0: Disable 1: Enable
2	R/W	0x0	ADC_CHAN2_SELECT Analog Input Channel 2 Select 0: Disable 1: Enable
1	R/W	0x0	ADC_CHAN1_SELECT Analog Input Channel 1 Select 0: Disable 1: Enable
0	R/W	0x1	ADC_CHAN0_SELECT Analog Input Channel 0 Select 0: Disable 1: Enable

3.14.4.3. RTP Control Register 2(Default Value:0x8000_0FFF)

Offset: 0x0008			**Register Name: RTP_CNT2**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x8	RTP_SENSITIVE_ADJUST. Internal Pull-up Resistor Control 0000: least sensitive …… 1111: most sensitive

Offset: 0x0008			Register Name: RTP_CNT2
Bit	**Read/Write**	**Default/Hex**	**Description**
			Used to adjust sensitivity of pen down detection.
27:26	R/W	0x0	RTP_FIFO_MODE_SELECT. RTP FIFO Access Data Mode Select 00: FIFO store X1,Y1 data for single touch no pressure mode 01: FIFO store X1,Y1, ΔX, ΔY data for dual touch no pressure mode 10: FIFO store X1,Y1, X2,Y2 data for dual touch no pressure mode 11: FIFO store X1,Y1, X2,Y2,Z1,Z2 data for dual touch and pressure mode **NOTE** **The ADC output data in single touch mode can store in FIFO with TP_FIFO_MODE_SELECT configured as 01,10,11. But the data ΔX, ΔY is theoretically equal to X1,Y1 , and X2,Y2 is equal to 0.**
25	/	/	/
24	R/W	0x0	PRE_MEA_EN. RTP Pressure Measurement Enable Control 0: Disable 1: Enable
23:0	R/W	0xFFF	PRE_MEA_THRE_CNT. RTP Pressure Measurement threshold Control 0x000000:least sensitive 0xFFFFFF: most sensitive **Used to adjust sensitivity of touch.**

3.14.4.4. Median and Averaging Filter Control Register(Default Value:0x0000_0001)

Offset: 0x000C			Register Name: RTP_CTRL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Filter Type 00: 4/2 01: 5/3 10: 8/4 11: 16/8

3.14.4.5. RTP Interrupt& FIFO Control Register(Default Value:0x0000_0F00)

Offset: 0x0010			Register Name: RTP_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	TEMP_IRQ_EN.

Offset: 0x0010			Register Name: RTP_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
			Temperature IRQ Enable 0: Disable 1: Enable
17	R/W	0x0	RTP_OVERRUN_IRQ_EN. RTP FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	RTP_DATA_IRQ_EN. RTP FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13	R/W	0x0	RTP_DATA_XY_CHANGE. RTP FIFO X,Y Data interchange Function Select 0: Disable 1: Enable
12:8	R/W	0xF	RTP_FIFO_TRIG_LEVEL. RTP FIFO Data Available Trigger Level Interrupt and DMA request trigger level for TP or Auxiliary ADC Trigger Level = TXTL + 1
7	R/W	0x0	RTP_DATA_DRQ_EN. RTP FIFO Data Available DRQ Enable 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	RTP_FIFO_FLUSH. RTP FIFO Flush Write ‘1’ to flush TX FIFO, self clear to ‘0’
3:2	/	/	/
1	R/W	0x0	RTP_UP_IRQ_EN. Touch Panel Last Touch (Stylus Up) IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	RTP_DOWN_IRQ_EN. Touch Panel First Touch (Stylus Down) IRQ Enable 0: Disable 1: Enable

3.14.4.6. RTP Interrupt& FIFO Status Register(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: RTP_FIFOCS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W1C	0x0	TEMP_IRQ_PENDING. Temperature IRQ Pending

			0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
17	R/W1C	0x0	FIFO_OVERRUN_PENDING. RTP FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
16	R/W1C	0x0	FIFO_DATA_PENDING. RTP FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
15:13	/	/	/
12:8	R	0x0	RXA_CNT. RTP FIFO available Sample Word Counter
7:3	/	/	/
2	R	0x0	RTP_IDLE_FLG. Touch Panel Idle Flag 0: idle 1: not idle
1	R/W1C	0x0	RTP_UP_PENDING. Touch Panel Last Touch (Stylus Up) IRQ Pending bit 0: No IRQ 1: IRQ Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W1C	0x0	RTP_DOWN_PENDING. Touch Panel First Touch (Stylus Down) IRQ Pending bit 0: No IRQ 1: IRQ Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

3.14.4.7. Common Data Register(Default Value:0x0000_0800)

Offset: 0x001C			**Register Name: RTP_CDAT**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x800	TP_CDAT. TP Common Data Used to adjust the tolerance of the internal ADC

3.14.4.8. RTP Data Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: RTP_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	TP_DATA. Touch Panel X ,Ydata or Auxiliary analog input data converted by the internal ADC

3.14.4.9. RTP PORT IO Configure Register(Default Value:0x0000_2222)

Offset: 0x0028			Register Name: RTP_IO_CONFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x2	TY_N_SELECT TY_N Port Function Select 000: Input 001:Output 010: TP_YN 011:/ 100: / 101:/ 110: / 111:/
11	/	/	/
10:8	R/W	0x2	TY_P_SELECT TY_P Port Function Select 000: Input 001:Output 010: TP_YP 011:/ 100: / 101:/ 110: / 111:/
7	/	/	/
6:4	R/W	0x2	TX_N_SELECT TX_P Port Function Select 000: Input 001:Output 010: TP_XN 011:/ 100: / 101:/ 110: / 111:/
3	/	/	/
2:0	R/W	0x2	TX_P_SELECT TX_P Port Function Select 000: Input 001:Output

Offset: 0x0028			Register Name: RTP_IO_CONFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
			010: TP_XP 011:/ 100: / 101:/ 110: / 111:/

3.14.4.10. RTP Port Data Register(Default Value:0x0000_0000)

Offset: 0x002C			Register Name: RTP_PORT_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
3:0	R/W	0x0	RTP_PORT_DATA RTP Port Data Value, TP_YN,TP_YP, TP_XN, TP_XP(y2/y1/x2/x1)

3.15. Thermal Sensor

3.15.1. Overview

The thermal sensor(THS) has become common elements in wide range of modern system on chip (SOC) platform. Thermal sensor is used to constantly monitor the temperature on the chip.

A40i embeds 2 thermal sensors in possible hot spots on the die, sensor0 located in the CPU, sensor1 located in the GPU. The thermal sensor generates interrupt to SW to lower temperature via DVFS, on reaching a certain thermal threshold.

Features:

- Temperature Accuracy : ±3℃ from 0℃ to +100℃, ±5℃ from -20℃ to +125℃
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Supports 2 sensors: sensor0 for CPU,sensor1 for GPU

3.15.2. Block Diagram

Figure 3-42 shows the block diagram of the thermal sensor.

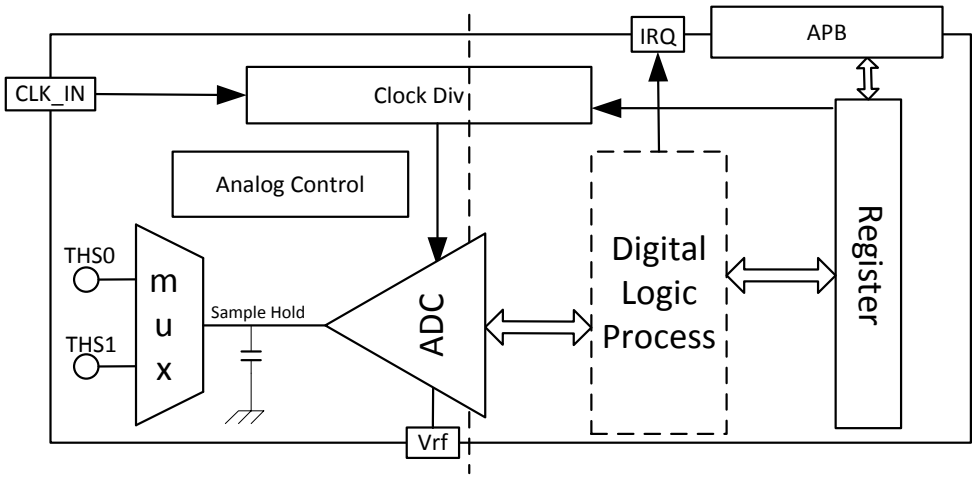


Figure 3-42. Thermal Sensor Block Diagram

3.15.3. Operations and Functional Descriptions

3.15.3.1. Clock Sources

Thermal Sensor has one clock source. Table 3-9 describes the clock source for Thermal Sensor. Users can see **CCU** for clock setting, configuration and gating information.

Table 3-9. Thermal Sensor Clock Sources

Clock Sources	Description
OSC24M	24MHz Clock

3.15.3.2. Temperature Conversion Formula

T= (sensor_data - 2266)/(-8.532), the unit of T is Celsius.
sensor_data: read from sensor data register.

3.15.4. Programming Guidelines

The initial process of the THS is as follows.

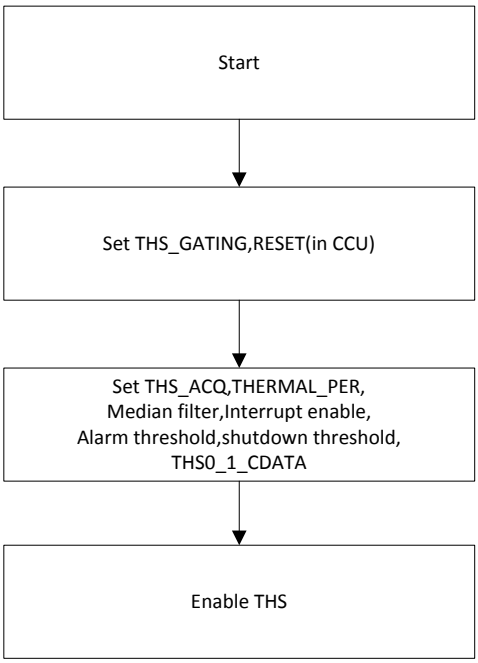


Figure 3-43. THS Initial Process

The formula of THS is y=-ax+b. In FT stage, THS is calibrated through ambient temperature, the calibration value is written in EFUSE. Please refer to SID Spec about EFUSE information.

Before enabling THS, read EFUSE value and write the value to **THS0_1_CDATA**.

The initial process of THS has 2 modes.

(1).Query Mode

Step1: Write 0x1 to the bit31 of **THS_CLK_REG(0x01C20074 register)** to enable clock.
Step2: Write 0x1 to the bit8 of **BUS_SOFT_RST_REG3(0x01C202D0 register)** to dessert reset, write 0x1 to the bit8 of **BUS_CLK_GATING_REG2(0x01C20068 register)** to enable THS clock.
Step3: Write 0x1DF to the bit[15:0] of **THS_CTRL0** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL1** to set Sensor acquire time.
Step5: Write 0x3A to the bit[31:12] of **THS_INTC** to set THS work period.
Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.
Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.
Step8: Read THS efuse value from SID, then write the efuse value to **THS0_1_CDATA** to calibrate THS0/THS1.
Step9: Write 0x3 to the bit[1:0] 0f **THS_CTRL1** to enable THS0/THS1.
Step10: Read the bit[9:8] of **THS_INTS**, if the value is 1, temperature conversion is complete.
Step11: Read the bit[11:0] of **THS0_DATA/THS1_DATA**, calculate THS0/THS1 temperature based on THS Temperature Conversion Formula in **Section 3.15.3.2**.

(2). Interrupt Mode

Step1: Write 0x1 to the bit31 of **THS_CLK_REG(0x01C20074 register)** to enable clock.
Step2: Write 0x1 to the bit8 of **BUS_SOFT_RST_REG3(0x01C202D0 register)** to dessert reset, write 0x1 to the bit8 of **BUS_CLK_GATING_REG2(0x01C20068 register)** to enable THS clock.
Step3: Write 0x1DF to the bit[15:0] of **THS_CTRL0** to set ADC acquire time.
Step4: Write 0x1DF to the bit[31:16] of **THS_CTRL1** to set Sensor acquire time.
Step5: Write 0x3A to the bit[31:12] of **THS_INTC** to set THS work period.
Step6: Write 0x1 to the bit2 of **THS_FILTER** to enable temperature convert filter.
Step7: Write 0x1 to the bit[1:0] of **THS_FILTER** to select filter type.
Step8: Read THS efuse value from SID, then write the efuse value to **THS_CDATA** to calibrate THS0/THS1.
Step9: Write 0x3 to the bit[9:8] of **THS_INTC** to enable the data interrupt of THS0/THS1.
Step10: Set GIC interface based on IRQ 68, write 0x1 to the bit[4] of the **0x01C81108** register.
Step11: Put interrupt handler address into interrupt vector table based on IRQ 68.
Step12: Write 0x3 to the bit[1:0] 0f **THS_CTRL1** to enable THS0/THS1.
Step13: Read the bit[3:0] of **THS_DATA_INTS** in interrupt handler, if the value is 1, temperature conversion is complete.
Step14: Read the bit[11:0] of **THS0_DATA/THS1_DATA** in interrupt handler, calculate THS0/THS1 temperature based on THS Temperature Conversion Formula in **Section 3.15.3.2**.

3.15.5. Register List

Module Name	Base Address
Thermal Sensor	0x01C24C00

Register Name	Offset	Description
THS_CTRL0	0x0000	THS Control Register0
THS_CTRL1	0x0040	THS Control Register1
THS_INTC	0x0044	THS Interrupt Control Register
THS_INTS	0x0048	THS Interrupt Status Register
THS0_ALARM_CTRL	0x0050	THS0 Alarm Threshold Control Register
THS1_ALARM_CTRL	0x0054	THS1 Alarm Threshold Control Register
THS0_SHUTDOWN_CTRL	0x0060	THS0 Shutdown Threshold Control Register
THS1_SHUTDOWN_CTRL	0x0064	THS0 Shutdown Threshold Control Register
THS_FILTER	0x0070	Median Filter Control Register
THS0_1_CDATA	0x0074	Thermal Sensor 0/1 Calibration Data
THS0_DATA	0x0080	THS0 Data Register
THS1_DATA	0x0084	THS1 Data Register

3.15.6. Register Description

3.15.6.1. THS Control Register0 (Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: THS_CTRL_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	THS_ACQ Sensor acquire time CLK_IN/(N+1)

3.15.6.2. THS Control Register1 (Default Value: 0x0004_0000)

Offset: 0x0040			Register Name: THS_CTRL_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	R/W	0x4	ADC_ACQ ADC acquire time CLK_IN/(N+1)
15:2	/	/	/
1	R/W	0x0	SENSE1_EN Enable temperature measurement sensor1 0:Disable 1:Enable
0	R/W	0x0	SENSE0_EN Enable temperature measurement sensor0 0:Disable 1:Enable

3.15.6.3. THS Interrupt Control Register (Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: THS_INTC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	THERMAL_PER 4096*(n+1)/CLK_IN
11:10	/	/	/
9	R/W	0x0	THS1_DATA_IRQ_EN Selects temperature measurement data of sensor1 0: No select 1: Select
8	R/W	0x0	THS0_DATA_IRQ_EN Selects temperature measurement data of sensor0 0: No select 1: Select
7:6	/	/	/
5	R/W	0x0	SHUT_INT1_EN Selects shutdown interrupt for sensor1 0: No select 1: Select
4	R/W	0x0	SHUT_INT0_EN Selects shutdown interrupt for sensor0 0: No select 1: Select
3:2	/	/	/
1	R/W	0x0	ALARM_INT1_EN Selects alarm interrupt for sensor1 0: No select 1: Select
0	R/W	0x0	ALARM_INT0_EN Selects alarm interrupt for sensor0 0: No select 1: Select

3.15.6.4. THS Interrupt Status Register (Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: THS_INTS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	ALARM_OFF1_STS Alarm interrupt off pending for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
12	R/W1C	0x0	ALARM_OFF0_STS Alarm interrupt off pending for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
11:10	/	/	/
9	R/W1C	0x0	THS1_DATA_IRQ_STS Data interrupt status for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
8	R/W1C	0x0	THS0_DATA_IRQ_STS Data interrupt status for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
7:6	/	/	/
5	R/W1C	0x0	SHUT_INT1_STS Shutdown interrupt status for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
4	R/W1C	0x0	SHUT_INT0_STS Shutdown interrupt status for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	ALARM_INT1_STS Alarm interrupt pending for sensor1 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.
0	R/W1C	0x0	ALARM_INT0_STS Alarm interrupt pending for sensor0 Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

3.15.6.5. THS0 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0050			Register Name: THS0_ALARM_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x5A0	ALARM0_T_HOT Thermal sensor0 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM0_T_HYST Thermal sensor0 alarm threshold for hysteresis temperature

3.15.6.6. THS1 Alarm Threshold Control Register (Default Value: 0x05A0_0684)

Offset: 0x0054			Register Name: THS1_ALARM_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5A0	ALARM1_T_HOT Thermal sensor1 alarm threshold for hot temperature
15:12	/	/	/
11:0	R/W	0x684	ALARM1_T_HYST Thermal sensor1 alarm threshold for hysteresis temperature

3.15.6.7. THS0 Shutdown Threshold Control Register (Default Value: 0x04E9_0000)

Offset: 0x0060			Register Name: THS0_SHUTDOWN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x4E9	SHUT0_T_HOT Thermal sensor0 shutdown threshold for hot temperature
15:0	/	/	/

3.15.6.8. THS1 Shutdown Threshold Control Register (Default Value: 0x04E9_0000)

Offset: 0x0064			Register Name: THS1_SHUTDOWN_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x4E9	SHUT1_T_HOT Thermal sensor1 shutdown threshold for hot temperature
15:0	/	/	/

3.15.6.9. Median Filter Control Register (Default Value: 0x0000_0001)

Offset: 0x0070			Register Name: THS_FILTER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Average Filter Type 00: 2 01: 4 10: 8 11: 16

3.15.6.10. Thermal Sensor 0 &1 Calibration Data Register (Default Value: 0x0800_0800)

Offset: 0x0074			Register Name: THS0_1_CDATA_REG
Bit	Read/Write	Default/Hex	Description

31:28	/	/	/
27:16	R/W	0x800	THS1_CDATA. Thermal Sensor1 calibration data
15:12	/	/	/
11:0	R/W	0x800	THS0_CDATA. Thermal Sensor0 calibration data

3.15.6.11. Thermal Sensor 0 Data Register (Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: THS0_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS0_DATA. Temperature measurement data of sensor0

3.15.6.12. Thermal Sensor 1 Data Register (Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: THS1_DATA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R	0x0	THS1_DATA. Temperature measurement data of sensor1

3.16. Crypto Engine

3.16.1. Overview

The Crypto Engine(CE) module is one encryption/decryption algorithms accelerator. It supports kinds of symmetric, asymmetric, HASH, and RNG algorithms. There are two software interfaces for secure and non-secure world. The software interface is simple for configuration, only setting interrupt control, task description address and load tag. Algorithm control information is written in memory in task descriptor, then CE automatically reads it when executing request. It supports parallel requests from 4 channels each world, and has an internal DMA controller to transfer data between CE and memory.

Features:

- Supports symmetrical algorithm: AES, DES, 3DES
- Supports Hash algorithms: MD5, SHA-1, SHA-224, SHA-256, SHA384, SHA512, HMAC
- Supports asymmetrical algorithm: RSA512-/1024-/2048-bit
- Supports 160-bit hardware PRNG with 175-bit seed
- Supports 256-bit hardware TRNG
- Supports ECB, CBC, CTR, CTS, OFB, CFB modes for AES
- Supports ECB, CBC, CTR modes for DES/3DES
- Supports 16-bit,32-bit,64-bit and 128-bit wide size for AES CTR
- Supports 1-bit, 8-bit, 64-bit and 128-bit width for AES CFB
- Supports 16-bit,32-bit and 64-bit wide size for DES/3DES CTR
- Supports 128-bit, 192-bit and 256-bit key size for AES
- Supports internal DMA Controller for data transfer with memory
- Supports secure and non-secure interfaces respectively

3.16.2. Block Diagram

The following figure shows the block diagram of Crypto Engine.

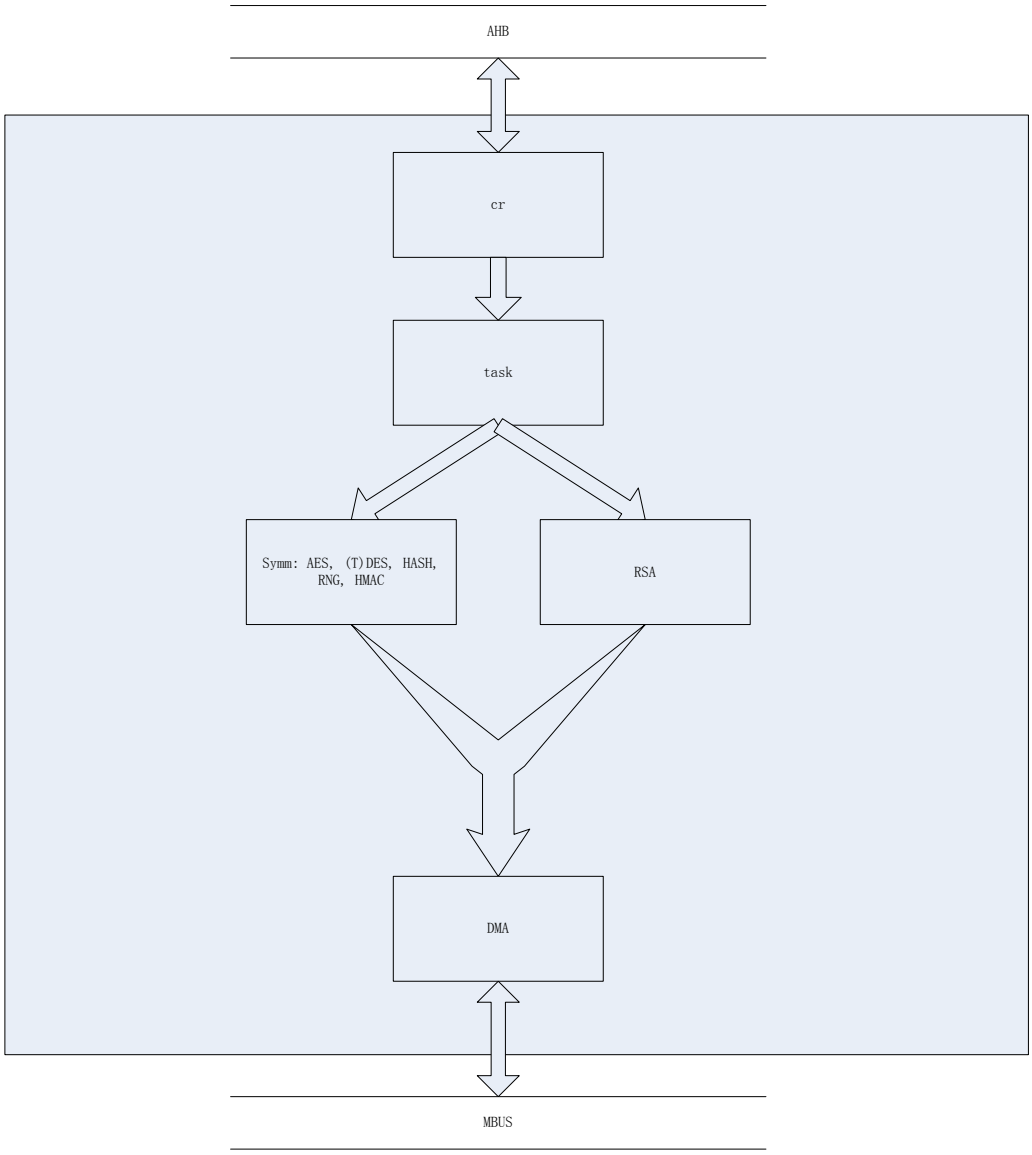


Figure 3-44. CE Block Diagram

3.16.3. Task Descriptor

Software make request through task descriptor, providing algorithm type, mode, key address, source/destination address and size, etc. The task descriptor is as follows.

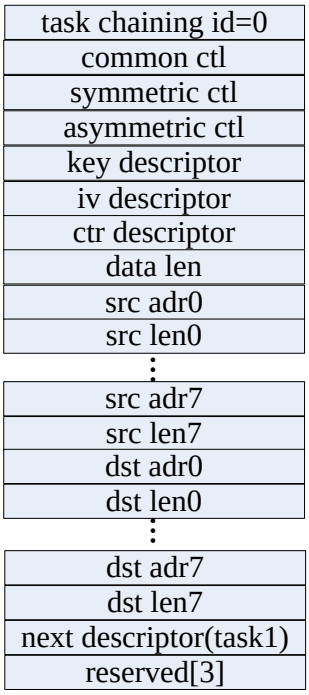


Figure 3-45. CE Task Chaining

3.16.3.1. Common Control

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	INTERRUPT ENABLE Interrupt enable for current task 0: Disable interrupt 1: Enable interrupt
30:17	/	/	/
16	R/W	0x0	IV MODE IV mode for SHA-1/SHA-224/SHA-256/SHA384/SHA512/MD5 or constants 0: Use initial constants defined in FIPS-180 1: Use input iv
15	R/W	0x0	HMAC PLAINTEXT LAST FLAG 0: Not the last HMAC plaintext package 1: The last HMAC plaintext package
14:9	/	/	/
8	R/W	0x0	OP DIR Algorithm Operation Direction 0: Encryption 1: Decryption
7	/	/	/
6:0	R/W	0x0	ALGORITHM TYPE 0: AES 1: DES 2: Triple DES (3DES) 3~15: Reserved

			16: MD5 17: SHA-1 18: SHA-224 19: SHA-256 20: SHA-384 21: SHA-512 22: HMAC-SHA1 23: HMAC-SHA256 24~31: Reserved 32: RSA 33~47: Reserved 48: TRNG 49: PRNG 50~62: Reserved

3.16.3.2. Symmetric Control

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:20	R/W	0x0	KEY SELECT key select for AES 0000: Select input CE_KEYx (Normal Mode) 0001: Select {SSK} 0010: Select {HUK} 0011: Select {RSSK} 0100-0111: Reserved 1000-1111: Select internal Key n (n from 0 to 7)
19:18	R/W	0x0	CFB_WIDTH For AES-CFB width 00: CFB1 01: CFB8 10: CFB64 11: CFB128
17	R/W	0x0	PRNG LD Load new 15bits key into lfsr for PRNG
16	R/W	0x0	AES CTS LAST PACKAGE FLAG When set to '1', it means this is the last package for AES-CTS mode. (the size of the last package >128bit)
15:12	/	/	/
11:8	R/W	0x0	ALGORITHM MODE CE Operation Mode 0000: Electronic Code Book (ECB) mode 0001: Cipher Block Chaining (CBC) mode 0010: Counter (CTR) mode 0011: Ciphertext Stealing (CTS) mode 0100: Output FeedBack(OFB) mode 0101: Cipher FeedBack(CFB) mode Other: Reserved
7:4	/	/	/

3:2	R/W	0x0	CTR WIDTH Counter Width for CTR Mode 00: 16-bit Counter 01: 32-bit Counter 10: 64-bit Counter 11: 128-bit Counter
1:0	R/W	0x0	AES KEY SIZE 00: 128-bit 01: 192-bit 10: 256-bit 11: Reserved

3.16.3.3. Asymmetric Control

Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x0	RSA WIDTH RSA Pubic Modulus Width 000: 512 bit 001: 1024 bit 010: 2048 bit Other: Reserved
27:0	/	/	/

3.16.4. Operations and Functional Descriptions

3.16.4.1. Task Request

Basically, there are 4 steps for one task handling from software. Firstly, software should configure task descriptor in memory, including all fields in descriptor. Channel id corresponds to one channel in CE, from 0 to 3 for secure and non secure world respectively. According to algorithm type, software should set the fields in common control, symmetric control, asymmetric control, then provide key/iv/ctr address and the data length of this task. Source and destination sg address and size are set based on upper application. If there is another task concatenating after this task, then set its descriptor address at next descriptor field. Secondly, software should set registers, including task descriptor address, interrupt control. Thirdly, software read load register to ensure that the bit0 is zero, then starts request by pulled up the bit0 of the load register. Lastly, wait interrupt status.

3.16.4.2. Data Length Setting

Data length field in task descriptor has different meaning for different algorithms. For AES-CTS algorithms mode data length field indicates valid source data byte number, for others indicate source data words number. For PRNG, data length should be 5 words aligned, For TRNG should be 8 words aligned. Data size in source and destination sg is as words, whose value should corresponds with data length field, or else CE will report error and stop execution.

3.16.4.3. Security Operation

When CPU issues request to CE module, CE module will register CPU's secure mode state. When executing this request,

this state bit works as access flag for inner and system resource. For HUK/RSSK/SSK from SID, only secure mode can access, or else these keys will be used as 0. For access to SID and keysram module through AHB bus, only secure mode can success, or else will read 0 or can not write. When issuing MBUS read and write requests, CE will use this secure state bit as mprot signal, so certain secure state accesses corresponding memory space, namely secure request can access secure and non secure space, but non secure request only can access non secure space.

3.16.4.4. Error Check

CE module includes error detection for task configuration, data computing error, and authentication invalid. When algorithm type in task description is read into module, CE will check if this type is supported through checking algorithm type field in common ctrl. If type value is out of support scope, CE will issue interrupt signal and set error state. Each type has certain input and output data size. After getting task descriptor, input size and output size configuration will be checked to avoid size error. If size configuration is wrong, CE will issue interrupt signal and set error state. To protect keys would be put into keysram from disclose, if the request using RSSK is for AES decryption and destination address is not in keysram space, CE would not execute this task. It will issue interrupt signal and set error state.

3.16.4.5. Clock Requirement

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	24MHz ~ 200MHz
m_clk	MBUS clk	24MHz ~ 400MHz
ce_clk	CE work clock	24MHz ~ 300MHz

3.16.5. Register List

Module Name	Base Address
CE_NS	0x01C15000
CE_S	0x01C15800

Register Name	Offset	Description
CE_TDA	0x0000	Task Descriptor Address
CE_CTL	0x0004	Control Register
CE_ICR	0x0008	Interrupt Control Register
CE_ISR	0x000C	Interrupt Status Register
CE_TLR	0x0010	Task Load Register
CE_TSR	0x0014	Task Status Register
CE_ESR	0x0018	Error Status Register
CE_CSA	0x0024	DMA Current Source Address
CE_CDA	0x0028	DMA Current Destination Address
CE_TPR	0x002C	Throughput Register

3.16.6. Register Description

3.16.6.1. CE Task Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CE_TDA
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CE_TDA

Offset: 0x0000			Register Name: CE_TDA
Bit	Read/Write	Default/Hex	Description
			Task Descriptor Address

3.16.6.2. CE Control Register(Default Value: UDF)

Offset: 0x0004			Register Name: CE_CTL
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3	R/W	0x0	RSA_CLK_GATING RSA CLK Gating Enable(only for S world) 0: RSA clk gating enable 1: RSA clk gating disable
2:0	R	UDF	DIE_ID Die Bonding ID

3.16.6.3. CE Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CE_ICR
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	TASK_INT_EN Task channel0-3 interrupt enable 0: interrupt disable 1: interrupt enable

3.16.6.4. CE Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: CE_ISR
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	TASK_END_PENDING Task channel0-3 end pending 0: Not finished 1: Finished It indicates if task has been completed . Write ‘1’ to clear it.

3.16.6.5. CE Task Load Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: CE_TLR
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	TASK_LOAD

Offset: 0x0010			Register Name: CE_TLR
Bit	Read/Write	Default/Hex	Description
			Task Load When set, CE can load the descriptor of task if task FIFO is not full.

3.16.6.6. CE Task Status Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: CE_TSR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R	0x0	TASK_CHANNEL Indicate which channel is running 00: Task channel0 01: Task channel1 10: Task channel2 11: Task channel3

3.16.6.7. CE Error Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: CE_ESR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:12	R	0x0	CH3_ERROR Task channel3 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write ‘1’ to clear it. 1xxx: Reserved
11:8	R	0x0	CH2_ERR Task channel2 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write ‘1’ to clear it. 1xxx: Reserved
7:4	R	0x0	CH1_ERR Task channel1 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write ‘1’ to clear it. 1xxx: Reserved
3:0	R	0x0	CH0_ERR Task channel0 error type xxx1: Algorithm not support xx1x: Data length error x1xx: Keysram access error for AES. Write ‘1’ to clear it. 1xxx: Reserved

3.16.6.8. CE Current Source Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: CE_CSA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	SRC_ADR Current source address

3.16.6.9. CE Current Destination Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: CE_CDA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DES_ADR Current destination address

3.16.6.10. CE Throughput Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CE_TPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	THROUGHPUT It indicates the throughput of the last time to this register. Writing 0 to this register will clear it.

3.17. Security ID (SID)

3.17.1. Overview

There is one 2048 bits on chip eFuse, which provides different size electrical fuses for security application. eFuse mapping address is from 0x00 to 0xff.

Features:

- 128-bit electrical fuses for chip id
- 32-bit electrical fuses for thermal sensor
- Others for security application

For complete SID information, refer to the ***Allwinner A40i SID Specification***.

3.18. Port Controller

3.18.1. Overview

The chip has 9 ports for multi-functional input/output pins. They are shown below:

- Port A(PA): 18 input/output port
- Port B(PB): 24 input/output port
- Port C(PC): 25 input/output port
- Port D(PD): 28 input/output port
- Port E(PE) : 12 input/output port
- Port F(PF) : 6 input/output port
- Port G(PG) : 12 input/output port
- Port H(PH) : 28 input/output port
- Port I(PI) : 22 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions not used. 32 external PIO interrupt sources are supported and interrupt mode can be configured by software.

3.18.2. Block Diagram

The block diagram of port controller is shown in Figure 3-46.

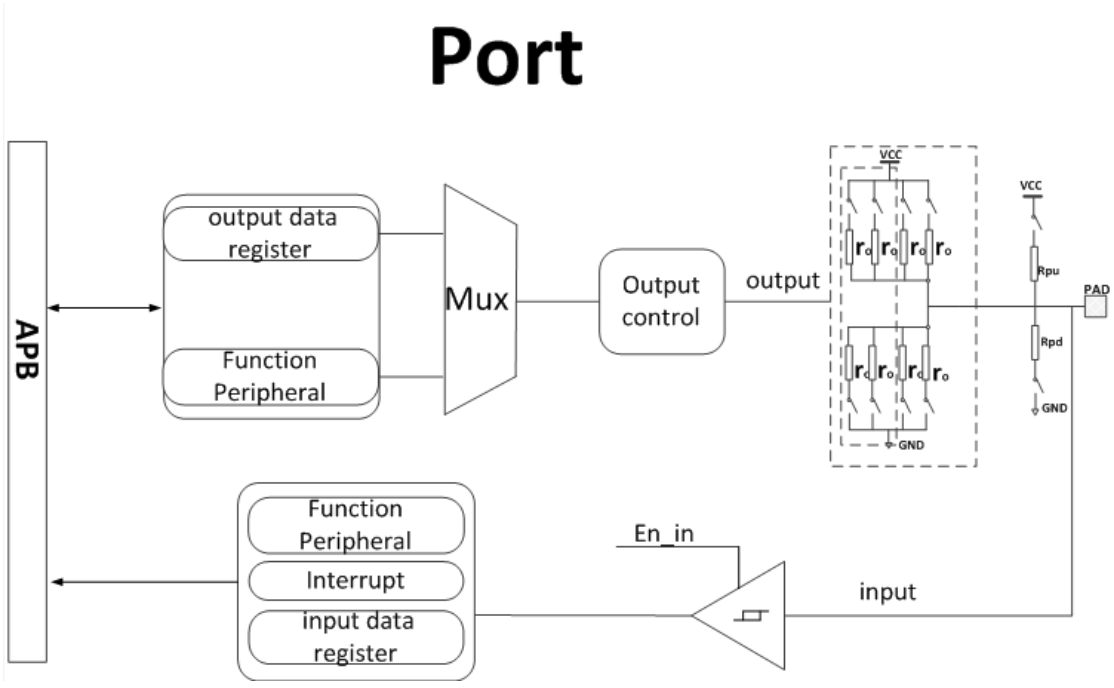


Figure 3-46. Port Controller Block Diagram

Port controller consists of digital part(GPIO, external interface) and IO analog part(output buffer, dual pull down, pad, etc). Digital part can select output interface by MUX switch; analog part can configure pull up/down, buffer strength.

When executing GPIO read state, the port controller reads the current level of pin into internal register bus. When not executing GPIO read state, external pin and internal register bus is off-status, that is high-impedance.

3.18.3. Operations and Functional Descriptions

3.18.3.1. Multi-function Port

A40i includes 175 multi-functional input/output port pins.There are 9 ports as listed below:

Table 3-10. Multi-function Port

Port Name	Number of Pins	Input Driver	Output Driver	Multiplex Pins	Power
PA	18	Schmitt	CMOS	EMAC/SPI/UART/GMAC/I2S	1.8V/2.5V/3.3V
PB	24	Schmitt	CMOS	TWI/PWM/OWA/CIR/I2S/AC97/SPI/UART/JTAG	3.3V
PC	25	Schmitt	CMOS	NAND/SPI/SMHC	1.8V/3.3V
PD	28	Schmitt	CMOS	LCD/LVDS/SCR	3.3V
PE	12	Schmitt	CMOS	TSC/CSI	1.8V/2.8V/3.3V
PF	6	Schmitt	CMOS	SMHC/UART/JTAG	3.3V
PG	12	Schmitt	CMOS	TSC/CSI/SMHC/UART	1.8V/2.8V/3.3V
PH	28	Schmitt	CMOS	LCD/EMAC/UART/KEYPAD/PS2/SCR/SMHC/CSI	3.3V
PI	22	Schmitt	CMOS	TWI/PWM/SMHC/SPI/UART/PS2	3.3V

3.18.3.2. Port Configuration Table

Table 3-11. Port A(PA) Multiplex Function Select Table

Port A(PA)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PA0	ERXD3	SPI1_CS0	UART2_RTS	GRXD3	
PA1	ERXD2	SPI1_CLK	UART2_CTS	GRXD2	
PA2	ERXD1	SPI1_MOSI	UART2_TX	GRXD1	
PA3	ERXD0	SPI1_MISO	UART2_RX	GRXD0	
PA4	ETXD3	SPI1_CS1		GTXD3	
PA5	ETXD2	SPI3_CS0		GTXD2	
PA6	ETXD1	SPI3_CLK		GTXD1	
PA7	ETXD0	SPI3_MOSI		GTXD0	
PA8	ERXCK	SPI3_MISO		GRXCK	
PA9	ERXERR	SPI3_CS1		GNULL/ERXERR	I2S1_MCLK
PA10	ERXDV		UART1_TX	GRXCTL/RXDV	
PA11	EMDC		UART1_RX	GMDC	
PA12	EMDIO	UART6_TX	UART1_RTS	GMDIO	
PA13	ETXEN	UART6_RX	UART1_CTS	GTXCTL/ETXEN	
PA14	ETXCK	UART7_TX	UART1_DTR	GNULL/ETXCK	I2S1_BCLK
PA15	ECRS	UART7_RX	UART1_DSR	GTXCK/ECRS	I2S1_LRCK
PA16	ECOL		UART1_DCD	GCLKIN/ECOL	I2S1_DO
PA17	ETXERR		UART1_RING	GNULL/ETXERR	I2S1_DI

Table 3-12. Port B(PB) Multiplex Function Select Table

Port B(PB)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PB0	TWI0_SCK	PLL_LOCK_DBG			
PB1	TWI0_SDA				
PB2		PWM0			
PB3		PWM1	OWA_MCLK		
PB4	CIR0_RX				
PB5	I2S_MCLK	AC97_MCLK			
PB6	I2S_BCLK	AC97_BCLK			
PB7	I2S_LRCK	AC97_SYNC			
PB8	I2S_DO0	AC97_DO			
PB9	I2S_DO1		PWM6		
PB10	I2S_DO2		PWM7		
PB11	I2S_DO3				
PB12	I2S_DI	AC97_DI			
PB13	SPI2_CS1		OWA_DO		
PB14	SPI2_CS0	JTAG_MS0			
PB15	SPI2_CLK	JTAG_CK0			
PB16	SPI2_MOSI	JTAG_DO0			
PB17	SPI2_MISO	JTAG_DI0			
PB18	TWI1_SCK				
PB19	TWI1_SDA				
PB20	TWI2_SCK		PWM4		
PB21	TWI2_SDA		PWM5		
PB22	UART0_TX				
PB23	UART0_RX	CIR1_RX			

Table 3-13. Port C(PC) Multiplex Function Select Table

Port C(PC)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PC0	NWE	SPI0_MOSI			
PC1	NALE	SPI0_MISO			
PC2	NCLE	SPI0_CLK			
PC3	NCE1				
PC4	NCE0				
PC5	NRE	SDC2_DS			
PC6	NRB0	SDC2_CMD			
PC7	NRB1	SDC2_CLK			
PC8	NDQ0	SDC2_D0			
PC9	NDQ1	SDC2_D1			
PC10	NDQ2	SDC2_D2			
PC11	NDQ3	SDC2_D3			

Port C(PC)	Multiplex Function Select				
PC12	NDQ4	SDC2_D4			
PC13	NDQ5	SDC2_D5			
PC14	NDQ6	SDC2_D6			
PC15	NDQ7	SDC2_D7			
PC16	NWP				
PC17	NCE2				
PC18	NCE3				
PC19	NCE4	SPI2_CS0			
PC20	NCE5	SPI2_CLK			
PC21	NCE6	SPI2_MOSI			
PC22	NCE7	SPI2_MISO			
PC23		SPI0_CS0			
PC24	NDQS	SDC2_RST			

Table 3-14. Port D(PD) Multiplex Function Select Table

Port D(PD)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PD0	LCD0_D0	LVDS0_VP0			
PD1	LCD0_D1	LVDS0_VN0			
PD2	LCD0_D2	LVDS0_VP1			
PD3	LCD0_D3	LVDS0_VN1			
PD4	LCD0_D4	LVDS0_VP2			
PD5	LCD0_D5	LVDS0_VN2			
PD6	LCD0_D6	LVDS0_VPC			
PD7	LCD0_D7	LVDS0_VNC			
PD8	LCD0_D8	LVDS0_VP3			
PD9	LCD0_D9	LVDS0_VN3			
PD10	LCD0_D10	LVDS1_VP0			
PD11	LCD0_D11	LVDS1_VN0			
PD12	LCD0_D12	LVDS1_VP1			
PD13	LCD0_D13	LVDS1_VN1			
PD14	LCD0_D14	LVDS1_VP2			
PD15	LCD0_D15	LVDS1_VN2			
PD16	LCD0_D16	LVDS1_VPC			
PD17	LCD0_D17	LVDS1_VNC			
PD18	LCD0_D18	LVDS1_VP3			
PD19	LCD0_D19	LVDS1_VN3			
PD20	LCD0_D20	CSI1_MCLK			
PD21	LCD0_D21	SMC_VPPEN			
PD22	LCD0_D22	SMC_VPPPP			
PD23	LCD0_D23	SMC_DET			
PD24	LCD0_CLK	SMC_VCCEN			
PD25	LCD0_DE	SMC_RST			

Port D(PD)	Multiplex Function Select				
PD26	LCD0_HSYNC	SMC_SLK			
PD27	LCD0_VSYNC	SMC_SDA			

Table 3-15. Port E(PE) Multiplex Function Select Table

Port E(PE)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PE0	TS0_CLK	CSI0_PCLK			
PE1	TS0_ERR	CSI0_MCLK			
PE2	TS0_SYNC	CSI0_HSYNC			
PE3	TS0_DLVD	CSI0_VSYNC			
PE4	TS0_D0	CSI0_D0			
PE5	TS0_D1	CSI0_D1			
PE6	TS0_D2	CSI0_D2			
PE7	TS0_D3	CSI0_D3			
PE8	TS0_D4	CSI0_D4			
PE9	TS0_D5	CSI0_D5			
PE10	TS0_D6	CSI0_D6			
PE11	TS0_D7	CSI0_D7			

Table 3-16. Port F(PF) Multiplex Function Select Table

Port F(PF)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PF0	SDC0_D1		JTAG_MS1		
PF1	SDC0_D0		JTAG_DI1		
PF2	SDC0_CLK		UART0_TX		
PF3	SDC0_CMD		JTAG_DO1		
PF4	SDC0_D3		UART0_RX		
PF5	SDC0_D2		JTAG_CK1		

Table 3-17. Port G(PG) Multiplex Function Select Table

Port G(PG)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PG0	TS1_CLK	CSI1_PCLK	SDC1_CMD		
PG1	TS1_ERR	CSI1_MLCK	SDC1_CLK		
PG2	TS1_SYNC	CSI1_HSYNC	SDC1_D0		
PG3	TS1_DVLD	CSI1_VSYNC	SDC1_D1		
PG4	TS1_D0	CSI1_D0	SDC1_D2	CSI0_D8	
PG5	TS1_D1	CSI1_D1	SDC1_D3	CSI0_D9	
PG6	TS1_D2	CSI1_D2	UART3_TX	CSI0_D10	
PG7	TS1_D3	CSI1_D3	UART3_RX	CSI0_D11	

Port G(PG)	Multiplex Function Select				
PG8	TS1_D4	CSI1_D4	UART3_RTS	CSI0_D12	
PG9	TS1_D5	CSI1_D5	UART3_CTS	CSI0_D13	BIST_RESULT0
PG10	TS1_D6	CSI1_D6	UART4_TX	CSI0_D14	BIST_RESULT1
PG11	TS1_D7	CSI1_D7	UART4_RX	CSI0_D15	

Table 3-18. Port H(PH) Multiplex Function Select Table

Port H(PH)	Multiplex Function Select					
	Function2	Function3	Function4	Function5	Function6	Function7
PH0	LCD1_D0		UART3_TX		EINT0	CSI1_D0
PH1	LCD1_D1		UART3_RX		EINT1	CSI1_D1
PH2	LCD1_D2		UART3_RTS		EINT2	CSI1_D2
PH3	LCD1_D3		UART3_CTS		EINT3	CSI1_D3
PH4	LCD1_D4		UART4_TX		EINT4	CSI1_D4
PH5	LCD1_D5		UART4_RX		EINT5	CSI1_D5
PH6	LCD1_D6		UART5_TX		EINT6	CSI1_D6
PH7	LCD1_D7		UART5_RX		EINT7	CSI1_D7
PH8	LCD1_D8	ERXD3	KP_IN0		EINT8	CSI1_D8
PH9	LCD1_D9	ERXD2	KP_IN1		EINT9	CSI1_D9
PH10	LCD1_D10	ERXD1	KP_IN2		EINT10	CSI1_D10
PH11	LCD1_D11	ERXD0	KP_IN3		EINT11	CSI1_D11
PH12	LCD1_D12		PS2_SCK1		EINT12	CSI1_D12
PH13	LCD1_D13		PS2_SDA1	SMC_RST	EINT13	CSI1_D13
PH14	LCD1_D14	ETXD3	KP_IN4	SMC_VPPEN	EINT14	CSI1_D14
PH15	LCD1_D15	ETXD2	KP_IN5	SMC_VPPPP	EINT15	CSI1_D15
PH16	LCD1_D16	ETXD1	KP_IN6	SMC_DET	EINT16	CSI1_D16
PH17	LCD1_D17	ETXD0	KP_IN7	SMC_VCCEN	EINT17	CSI1_D17
PH18	LCD1_D18	ERXCK	KP_OUT0	SMC_SLK	EINT18	CSI1_D18
PH19	LCD1_D19	ERXERR	KP_OUT1	SMC_SDA	EINT19	CSI1_D19
PH20	LCD1_D20	ERXDV			EINT20	CSI1_D20
PH21	LCD1_D21	EMDC			EINT21	CSI1_D21
PH22	LCD1_D22	EMDIO	KP_OUT2	SDC1_CMD		CSI1_D22
PH23	LCD1_D23	ETXEN	KP_OUT3	SDC1_CLK		CSI1_D23
PH24	LCD1_CLK	ETXCK	KP_OUT4	SDC1_D0		CSI1_PCLK
PH25	LCD1_DE	ECRS	KP_OUT5	SDC1_D1		CSI1_FIELD
PH26	LCD1_HSYNC	ECOL	KP_OUT6	SDC1_D2		CSI1_HSYNC
PH27	LCD1_VSYNC	ETXERR	KP_OUT7	SDC1_D3		CSI1_VSYNC

Table 3-19. Port I(PI) Multiplex Function Select Table

Port I(PI)	Multiplex Function Select				
	Function2	Function3	Function4	Function5	Function6
PI0		TWI3_SCK			

Port I(PI)	Multiplex Function Select				
PI1		TWI3_SDA			
PI2		TWI4_SCK			
PI3	PWM1	TWI4_SDA			
PI4	SDC3_CMD				
PI5	SDC3_CLK				
PI6	SDC3_D0				
PI7	SDC3_D1				
PI8	SDC3_D2				
PI9	SDC3_D3				
PI10	SPI0_CS0	UART5_TX			EINT22
PI11	SPI0_CLK	UART5_RX			EINT23
PI12	SPI0_MOSI	UART6_TX	CLK_OUT_A		EINT24
PI13	SPI0_MISO	UART6_RX	CLK_OUT_B		EINT25
PI14	SPI0_CS1	PS2_SCK1	TCLKIN0		EINT26
PI15	SPI1_CS1	PS2_SDA1	TCLKIN1		EINT27
PI16	SPI1_CS0	UART2_RTS			EINT28
PI17	SPI1_CLK	UART2_CTS			EINT29
PI18	SPI1_MOSI	UART2_TX			EINT30
PI19	SPI1_MISO	UART2_RX			EINT31
PI20	PS2_SCK0	UART7_TX			PWM2
PI21	PS2_SDA0	UART7_RX			PWM3

3.18.3.3. Port Function

Port Controller supports 9 GPIOs, every GPIO can configure as Input,Output,Function Peripheral,IO disable or Interrupt function. The configuration instruction of every function is as follows.

Table 3-20. Port Function

	Function	Buffer Strength	Pull Up	Pull Down
Input	GPIO/Multiplexing Input	/	X	X
Output	GPIO/Multiplexing Output	Y	X	X
Disable	Pull Up	/	Y	N
	Pull Down	/	N	Y
Interrupt	Trigger	/	X	X

/: non-configure, configuration is invalid
Y: configure
X: Select configuration according to actual situation
N: Forbid to configure

3.18.3.4. Pull Up/Down and High-Impedance Logic

Each IO pin can configure the internal pull-up/down function or high-impedance.

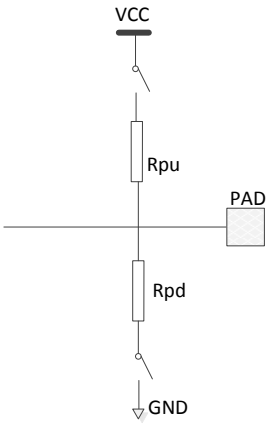


Figure 3-47. Pull up/down Logic

High-impedance, the output is float state, all buffer is off, the level is decided by external high/low level. When high-impedance, software configures the switch on Rpu and Rpd as off ,and the multiplexing function of IO is set as IO disable or input by software.

Pull-up, an uncertain signal is pulled high by a resistance, the resistance has current-limiting function. When pulling up, the switch on Rpu is breakover by software configuration, IO is pulled up to VCC by Rpu.

Pull-down, an uncertain signal is pulled low by a resistance. When pulling down, the switch on Rpd is breakover by software configuration, IO is pulled down to GND by Rpd.

The pull-up/down of each IO is weak pull-up/down, the resistance is 100kΩ±50%.

The setting of pull-down,pull-up,high-impledance is decided by external circuit.

3.18.3.5. Buffer Strength

Each IO can be set as different buffer strength.The IO buffer diagram is as follows.

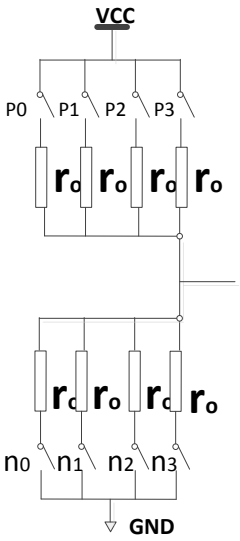


Figure 3-48. IO Buffer Strength Diagram

When output high level, the n0,n1,n2,n3 of NMOS is off, the p0,p1,p2,p3 of PMOS is on. When buffer strength is set to 0(buffer strength is weakest), only p0 is on, the output impedance is maximum ,the impedance value is r0. When buffer

strength is set to 1, only p0 and p1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2.When buffer strength is 2, only p0,p1 and p2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3.When buffer strength is 3, p0,p1,p2 and p3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When output low level, the p0,p1,p2,p3 of PMOS is off, the n0,n1,n2,n3 of NMOS is on. When buffer strength is set to 0(buffer strength is weakest), only n0 is on, the output impedance is maximum ,the impedance value is r0. When buffer strength is set to 1, only n0 and n1 is on, the output impedance is equivalent to two r0 in parallel, the impedance value is r0/2. When buffer strength is 2, only n0,n1 and n2 is on, the output impedance is equivalent to three r0 in parallel, the impedance value is r0/3. When buffer strength is 3, n0,n1,n2 and n3 is on, the output impedance is equivalent to four r0 in parallel, the impedance value is r0/4.

When GPIO is set to input or interrupt function, between output driver circuit and port is unconnected, driver configuration is invalid.

3.18.3.6. Interrupt

Each group IO has independent interrupt number.IO within group uses one interrupt number, when one IO generates interrupt, Port Controller sent interrupt request to GIC. External Interrupt Status Register is used to query which IO generates interrupt.

Interrupt trigger of GPIO supports the following trigger types.

- Positive Edge : When low level changes to high level, the interrupt will generate. No matter how long high level keeps, the interrupt generates only once.
- Negative Edge: When high level changes to low level, the interrupt will generate. No matter how long low level keeps, the interrupt generates only once.
- High Level : Just keep high level and the interrupt will always generate.
- Low Level : Just keep low level and the interrupt will always generate.
- Double Edge : Positive and negative edge.

External Interrupt Configure Register is used to configure trigger type.

GPIO interrupt supports hardware debounce function by setting External Interrupt Debounce Register. Sample trigger signal using lower sample clock, to reach the debounce effect because of the dither frequency of signal is higher than sample frequency.

Set sample clock source by PIO_INT_CLK_SELECT and prescale factor by DEB_CLK_PRE_SCALE.

3.18.4. Programming Guidelines

LVDS interface has LVDS0 and LVDS1, the external pins of LVDS0 is PD0~PD9, the external pins of LVDS1 is PD10~PD19. If you use only LVDS0, then PD0~PD9 need configure to Function3 and PD10 need configure to other function except Function3. If you use only LVDS1, then PD10~PD19 need configure to Function3 and PD0 need configure to other function except Function3. If you use LVDS0 and LVDS1, then PD0~PD19 need configure to Function3.

3.18.5. Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	0x0000+N*0x24	Port n Configure Register 0 (N from 0 to 8)
Pn_CFG1	0x0004+N*0x24	Port n Configure Register 1 (N from 0 to 8)
Pn_CFG2	0x0008+N*0x24	Port n Configure Register 2 (N from 0 to 8)
Pn_CFG3	0x000C+N*0x24	Port n Configure Register 3 (N from 0 to 8)
Pn_DAT	0x0010+N*0x24	Port n Data Register (N from 0 to 8)
Pn_DRV0	0x0014+N*0x24	Port n Multi-Driving Register 0 (N from 0 to 8)
Pn_DRV1	0x0018+N*0x24	Port n Multi-Driving Register 1 (N from 0 to 8)
Pn_PUL0	0x001C+N*0x24	Port n Pull Register 0 (N from 0 to 8)
Pn_PUL1	0x0020+N*0x24	Port n Pull Register 1 (N from 0 to 8)
PIO_INT_CFG0	0x0200	PIO Interrupt Configure Register 0
PIO_INT_CFG1	0x0204	PIO Interrupt Configure Register 1
PIO_INT_CFG2	0x0208	PIO Interrupt Configure Register 2
PIO_INT_CFG3	0x020C	PIO Interrupt Configure Register 3
PIO_INT_CTL	0x0210	PIO Interrupt Control Register
PIO_INT_STA	0x0214	PIO Interrupt Status Register
PIO_INT_DEB	0x0218	PIO Interrupt Debounce Register

3.18.6. Register Description

3.18.6.1. PA Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PA7_SELECT 000: Input 001: Output 010: ETXD0 011: SPI3_MOSI 100: Reserved 101: GTXD0 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PA6_SELECT 000: Input 001: Output 010: ETXD1 011: SPI3_CLK 100: Reserved 101: GTXD1 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PA5_SELECT 000: Input 001: Output 010: ETXD2 011: SPI3_CS0 100: Reserved 101: GTXD2 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PA4_SELECT 000: Input 001: Output

Offset: 0x0000			Register Name: PA_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			010: ETXD3 011: SPI1_CS1 100: Reserved 101: GTXD3 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PA3_SELECT 000: Input 001: Output 010: ERXD0 011: SPI1_MISO 100: UART2_RX 101: GRXD0 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PA2_SELECT 000: Input 001: Output 010: ERXD1 011: SPI1_MOSI 100: UART2_TX 101: GRXD1 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PA1_SELECT 000: Input 001: Output 010: ERXD2 011: SPI1_CLK 100: UART2_CTS 101: GRXD2 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PA0_SELECT 000: Input 001: Output 010: ERXD3 011: SPI1_CS0 100: UART2_RTS 101: GRXD3 110: Reserved 111: IO Disable

3.18.6.2. PA Configure Register 1(Default Value: 0x7777_7777)

Offset: 0x0004			Register Name: PA_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PA15_SELECT 000: Input 001: Output 010: ECRS 011: UART7_RX 100: UART1_DSR 101: GTXCK/ECRS 110: I2S1_LRCK 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PA14_SELECT 000: Input 001: Output 010: ETXCK 011: UART7_TX 100: UART1_DTR 101: GNULL/ETXCK 110: I2S1_BCLK 111: IO Disable

Offset: 0x0004			Register Name: PA_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
23	/	/	/	
22:20	R/W	0x7	PA13_SELECT 000: Input 010: ETXEN 100: UART1_CTS 110: Reserved	001: Output 011: UART6_RX 101: GTXCTL/ETXEN 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PA12_SELECT 000: Input 010: EMDIO 100: UART1_RTS 110: Reserved	001: Output 011: UART6_TX 101: GMDIO 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PA11_SELECT 000: Input 010: EMDC 100: UART1_RX 110: Reserved	001: Output 011: Reserved 101: GMDC 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PA10_SELECT 000: Input 010: ERXDV 100: UART1_TX 110: Reserved	001: Output 011: Reserved 101: GRXCTL/ERXDV 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PA9_SELECT 000: Input 010: ERXERR 100: Reserved 110: I2S1_MCLK	001: Output 011: SPI3_CS1 101: GNULL/ERXERR 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PA8_SELECT 000: Input 010: ERXCK 100: Reserved 110: Reserved	001: Output 011: SPI3_MISO 101: GRXCK 111: IO Disable

3.18.6.3. PA Configure Register 2(Default Value: 0x0000_0077)

Offset: 0x0008			Register Name: PA_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x7	PA17_SELECT

Offset: 0x0008			Register Name: PA_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
			000: Input 001: Output 010: ETXERR 011: Reserved 100: UART1_RING 101: GNULL/ETXERR 110: I2S1_DI 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PA16_SELECT 000: Input 001: Output 010: ECOL 011: Reserved 100: UART1_DCD 101: GCLKIN/ECOL 110: I2S1_DO 111: IO Disable

3.18.6.4. PA Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: PA_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.5. PA Data Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PA_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:0	R/W	0x0	PA_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.6. PA Multi-Driving Register 0(Default Value: 0x5555_5555)

Offset: 0x0014			Register Name: PA_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.7. PA Multi-Driving Register 1(Default Value: 0x0000_0005)

Offset: 0x0018			Register Name: PA_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/

Offset: 0x0018			Register Name: PA_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~1)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.8. PA Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: PA_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.9. PA Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: PA_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

3.18.6.10. PB Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x0024			Register Name: PB_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PB7_SELECT 000: Input 001: Output 010: I2S_LRCK 011: AC97_SYNC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PB6_SELECT 000: Input 001: Output 010: I2S_BCLK 011: AC97_BCLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PB5_SELECT

Offset: 0x0024			Register Name: PB_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
			000: Input 010: I2S_MCLK 100: Reserved 110: Reserved	001: Output 011: AC97_MCLK 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PB4_SELECT 000: Input 010: CIR0_RX 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PB3_SELECT 000: Input 010: Reserved 100: OWA_MCLK 110: Reserved	 001: Output 011: PWM1 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PB2_SELECT 000: Input 010: Reserved 100: Reserved 110: Reserved	 001: Output 011: PWM0 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PB1_SELECT 000: Input 010: TWI0_SDA 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PB0_SELECT 000: Input 010: TWI0_SCK 100: Reserved 110: Reserved	 001: Output 011: PLL_LOCK_DBG 101: Reserved 111: IO Disable

3.18.6.11. PB Configure Register 1(Default Value: 0x7777_7777)

Offset: 0x0028			Register Name: PB_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PB15_SELECT 000: Input 010: SPI2_CLK	 001: Output 011: JTAG_CK0

Offset: 0x0028			Register Name: PB_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
			100: Reserved 110: Reserved	101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PB14_SELECT 000: Input 010: SPI2_CS0 100: Reserved 110: Reserved	 001: Output 011: JTAG_MS0 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PB13_SELECT 000: Input 010: SPI2_CS1 100: OWA_DO 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PB12_SELECT 000: Input 010: I2S_DI 100: Reserved 110: Reserved	 001: Output 011: AC97_DI 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PB11_SELECT 000: Input 010: I2S_DO3 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PB10_SELECT 000: Input 010: I2S_DO2 100: PWM7 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PB9_SELECT 000: Input 010: I2S_DO1 100: PWM6 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PB8_SELECT 000: Input 010: I2S_DO0 100: Reserved 110: Reserved	 001: Output 011: AC97_DO 101: Reserved 111: IO Disable

3.18.6.12. PB Configure Register 2(Default Value: 0x7777_7777)

Offset: 0x002C			Register Name: PB_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PB23_SELECT 000: Input 001: Output 010: UART0_RX 011: CIR1_RX 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PB22_SELECT 000: Input 001: Output 010: UART0_TX 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PB21_SELECT 000: Input 001: Output 010: TWI2_SDA 011: Reserved 100: PWM5 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PB20_SELECT 000: Input 001: Output 010: TWI2_SCK 011: Reserved 100: PWM4 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PB19_SELECT 000: Input 001: Output 010: TWI1_SDA 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PB18_SELECT 000: Input 001: Output 010: TWI1_SCK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PB17_SELECT 000: Input 001: Output 010: SPI2_MISO 011: JTAG_DI0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/

Offset: 0x002C			Register Name: PB_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x7	PB16_SELECT 000: Input 001: Output 010: SPI2_MOSI 011: JTAG_DO0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.13. PB Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: PB_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.14. PB Data Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: PB_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	PB_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.15. PB Multi-Driving Register 0(Default Value: 0x5555_5555)

Offset: 0x0038			Register Name: PB_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.16. PB Multi-Driving Register 1(Default Value: 0x0000_5555)

Offset: 0x003C			Register Name: PB_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 16~23) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.17. PB Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: PB_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.18. PB Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: PB_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 16~23) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.19. PC Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x0048			Register Name: PC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000: Input 001: Output 010: NRB1 011: SDC2_CLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PC6_SELECT 000: Input 001: Output 010: NRB0 011: SDC2_CMD 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PC5_SELECT 000: Input 001: Output 010: NRE 011: SDC2_DS 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PC4_SELECT

Offset: 0x0048			Register Name: PC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			000: Input 001: Output 010: NCE0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PC3_SELECT 000: Input 001: Output 010: NCE1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PC2_SELECT 000: Input 001: Output 010: NCLE 011: SPI0_CLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC1_SELECT 000: Input 001: Output 010: NALE 011: SPI0_MISO 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PC0_SELECT 000: Input 001: Output 010: NWE 011: SPI0_MOSI 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.20. PC Configure Register 1(Default Value: 0x7777_7777)

Offset: 0x004C			Register Name: PC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PC15_SELECT 000: Input 001: Output 010: NDQ7 011: SDC2_D7 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PC14_SELECT 000: Input 001: Output 010: NDQ6 011: SDC2_D6

Offset: 0x004C			Register Name: PC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PC13_SELECT 000: Input 001: Output 010: NDQ5 011: SDC2_D5 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PC12_SELECT 000: Input 001: Output 010: NDQ4 011: SDC2_D4 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PC11_SELECT 000: Input 001: Output 010: NDQ3 011: SDC2_D3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PC10_SELECT 000: Input 001: Output 010: NDQ2 011: SDC2_D2 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC9_SELECT 000: Input 001: Output 010: NDQ1 011: SDC2_D1 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PC8_SELECT 000: Input 001: Output 010: NDQ0 011: SDC2_D0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.21. PC Configure Register 2(Default Value: 0x7777_7777)

Offset: 0x0050			Register Name: PC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/

Offset: 0x0050			Register Name: PC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
30:28	R/W	0x7	PC23_SELECT 000: Input 001: Output 010: Reserved 011: SPI0_CS0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
17	/	/	/
26:24	R/W	0x7	PC22_SELECT 000: Input 001: Output 010: NCE7 011: SPI2_MISO 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PC21_SELECT 000: Input 001: Output 010: NCE6 011: SPI2_MOSI 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PC20_SELECT 000: Input 001: Output 010: NCE5 011: SPI2_CLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PC19_SELECT 000: Input 001: Output 010: NCE4 011: SPI2_CS0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PC18_SELECT 000: Input 001: Output 010: NCE3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC17_SELECT 000: Input 001: Output 010: NCE2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000: Input 001: Output

Offset: 0x0050			Register Name: PC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
			010: NWP 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.22. PC Configure Register 3(Default Value: 0x0000_0007)

Offset: 0x0054			Register Name: PC_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x7	PC24_SELECT 000: Input 001: Output 010: NDQS 011: SDC2_RST 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.23. PC Data Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: PC_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	PC_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.24. PC Multi-Driving Register 0(Default Value: 0x5555_5555)

Offset: 0x005C			Register Name: PC_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.25. PC Multi-Driving Register 1(Default Value: 0x0001_5555)

Offset: 0x0060			Register Name: PC_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x1	PC_DRV PC[n] Multi-Driving Select (n = 16~24)

Offset: 0x0060			Register Name: PC_DRV1
Bit	Read/Write	Default/Hex	Description
			00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.26. PC Pull Register 0(Default Value: 0x0000_5140)

Offset: 0x0064			Register Name: PC_PULL0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x5140	PC_PULL PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.27. PC Pull Register 1(Default Value: 0x0000_4016)

Offset: 0x0068			Register Name: PC_PULL1
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
[2i+1:2i] (i=0~8)	R/W	0x4016	PC_PULL PC[n] Pull-up/down Select (n = 16~24) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.28. PD Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x006C			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000: Input 001: Output 010: LCD0_D7 011: LVDS0_VNC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PD6_SELECT 000: Input 001: Output 010: LCD0_D6 011: LVDS0_VPC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PD5_SELECT 000: Input 001: Output

Offset: 0x006C			Register Name: PD_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
			010: LCD0_D5 100: Reserved 110: Reserved	011: LVDS0_VN2 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD4_SELECT 000: Input 010: LCD0_D4 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP2 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PD3_SELECT 000: Input 010: LCD0_D3 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VN1 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000: Input 010: LCD0_D2 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP1 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD1_SELECT 000: Input 010: LCD0_D1 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VN0 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD0_SELECT 000: Input 010: LCD0_D0 100: Reserved 110: Reserved	 001: Output 011: LVDS0_VP0 101: Reserved 111: IO Disable

3.18.6.29. PD Configure Register 1(Default Value: 0x7777_7777)

Offset: 0x0070			Register Name: PD_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PD15_SELECT 000: Input 010: LCD0_D15 100: Reserved 110: Reserved	 001: Output 011: LVDS1_VN2 101: Reserved 111: IO Disable

Offset: 0x0070			Register Name: PD_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
27	/	/	/
26:24	R/W	0x7	PD14_SELECT 000: Input 001: Output 010: LCD0_D14 011: LVDS1_VP2 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PD13_SELECT 000: Input 001: Output 010: LCD0_D13 011: LVDS1_VN1 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PD12_SELECT 000: Input 001: Output 010: LCD0_D12 011: LVDS1_VP1 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PD11_SELECT 000: Input 001: Output 010: LCD0_D11 011: LVDS1_VN0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PD10_SELECT 000: Input 001: Output 010: LCD0_D10 011: LVDS1_VP0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PD9_SELECT 000: Input 001: Output 010: LCD0_D9 011: LVDS0_VN3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PD8_SELECT 000: Input 001: Output 010: LCD0_D8 011: LVDS0_VP3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.30. PD Configure Register 2(Default Value: 0x7777_7777)

Offset: 0x0074			Register Name: PD_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PD23_SELECT 000: Input 001: Output 010: LCD0_D23 011: SMC_DET 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PD22_SELECT 000: Input 001: Output 010: LCD0_D22 011: SMC_VPPPP 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PD21_SELECT 000: Input 001: Output 010: LCD0_D21 011: SMC_VPPEN 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PD20_SELECT 000: Input 001: Output 010: LCD0_D20 011: CSI1_MCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved
15	/	/	/
14:12	R/W	0x7	PD19_SELECT 000: Input 001: Output 010: LCD0_D19 011: LVDS1_VN3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PD18_SELECT 000: Input 001: Output 010: LCD0_D18 011: LVDS1_VP3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PD17_SELECT 000: Input 001: Output 010: LCD0_D17 011: LVDS1_VNC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/

Offset: 0x0074			Register Name: PD_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x7	PD16_SELECT 000: Input 001: Output 010: LCD0_D16 011: LVDS1_VPC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.31. PD Configure Register 3(Default Value: 0x0000_7777)

Offset: 0x0078			Register Name: PD_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x7	PD27_SELECT 000: Input 001: Output 010: LCD0_VSYNC 011: SMC_SDA 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PD26_SELECT 000: Input 001: Output 010: LCD0_HSYNC 011: SMC_SLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PD25_SELECT 000: Input 001: Output 010: LCD0_DE 011: SMC_RST 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PD24_SELECT 000: Input 001: Output 010: LCD0_CLK 011: SMC_VCCEN 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.32. PD Data Register(Default Value: 0x0000_0000)

Offset: 0x007C			Register Name: PD_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:0	R/W	0x0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by

Offset: 0x007C			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
			software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.33. PD Multi-Driving Register 0(Default Value: 0x5555_5555)

Offset: 0x0080			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.34. PD Multi-Driving Register 1(Default Value: 0x0055_5555)

Offset: 0x0084			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.35. PD Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: PD_PULL0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.36. PD Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: PD_PULL1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.37. PE Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x0090			Register Name: PE_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PE7_SELECT 000: Input 001: Output 010: TS0_D3 011: CSI0_D3 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PE6_SELECT 000: Input 001: Output 010: TS0_D2 011: CSI0_D2 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PE5_SELECT 000: Input 001: Output 010: TS0_D1 011: CSI0_D1 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PE4_SELECT 000: Input 001: Output 010: TS0_D0 011: CSI0_D0 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PE3_SELECT 000: Input 001: Output 010: TS0_DVLD 011: CSI0_VSYNC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PE2_SELECT 000: Input 001: Output 010: TS0_SYNC 011: CSI0_HSYNC 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PE1_SELECT 000: Input 001: Output 010: TS0_ERR 011: CSI0_MCLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/

Offset: 0x0090			Register Name: PE_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
2:0	R/W	0x7	PE0_SELECT 000: Input 001: Output 010: TS0_CLK 011: CSI0_PCLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.38. PE Configure Register 1(Default Value: 0x0000_7777)

Offset: 0x0094			Register Name: PE_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x7	PE11_SELECT 000: Input 001: Output 010: TS0_D7 011: CSI0_D7 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PE10_SELECT 000: Input 001: Output 010: TS0_D6 011: CSI0_D6 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PE9_SELECT 000: Input 001: Output 010: TS0_D5 011: CSI0_D5 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PE8_SELECT 000: Input 001: Output 010: TS0_D4 011: CSI0_D4 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

3.18.6.39. PE Configure Register 2(Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: PE_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.40. PE Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: PE_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.41. PE Data Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.42. PE Multi-Driving Register 0(Default Value: 0x0055_5555)

Offset: 0x00A4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.43. PE Multi-Driving Register 1(Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: PE_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.44. PE Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: PE_PULL0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.45. PE Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: PE_PULL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.46. PF Configure Register 0(Default Value: 0x0077_7777)

Offset: 0x00B4			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:20	R/W	0x7	PF5_SELECT 000: Input 001: Output 010: SDC0_D2 011: Reserved 100: JTAG_CK1 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PF4_SELECT 000: Input 001: Output 010: SDC0_D3 011: Reserved 100: UART0_RX 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PF3_SELECT 000: Input 001: Output 010: SDC0_CMD 011: Reserved 100: JTAG_DO1 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PF2_SELECT 000: Input 001: Output 010: SDC0_CLK 011: Reserved 100: UART0_TX 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PF1_SELECT 000: Input 001: Output 010: SDC0_D0 011: Reserved 100: JTAG_DI1 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PF0_SELECT 000: Input 001: Output 010: SDC0_D1 011: Reserved 100: JTAG_MS1 101: Reserved 110: Reserved 111: IO Disable

3.18.6.47. PF Configure Register 1(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: PF_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.48. PF Configure Register 2(Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: PF_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.49. PF Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: PF_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.50. PF Data Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0x0	PF_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.51. PF Multi-Driving Register 0(Default Value: 0x0000_0555)

Offset: 0x00C8			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x1	PF_DRV PF[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.52. PF Multi-Driving Register 1(Default Value: 0x0000_0000)

Offset: 0x00CC			Register Name: PF_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

3.18.6.53. PF Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: PF_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~5) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.54. PF Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x00D4			Register Name: PF_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.55. PG Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x00D8			Register Name: PG_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PG7_SELECT 000: Input 001: Output 010: TS1_D3 011: CSI1_D3 100: UART3_RX 101: CSI0_D11 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000: Input 001: Output 010: TS1_D2 011: CSI1_D2 100: UART3_TX 101: CSI0_D10 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000: Input 001: Output 010: TS1_D1 011: CSI1_D1 100: SDC1_D3 101: CSI0_D9 110: Reserved 111: IO Disable

Offset: 0x00D8			Register Name: PG_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000: Input 001: Output 010: TS1_D0 011: CSI1_D0 100: SDC1_D2 101: CSI0_D8 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PG3_SELECT 000: Input 001: Output 010: TS1_DVLD 011: CSI1_VSYNC 100: SDC1_D1 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PG2_SELECT 000: Input 001: Output 010: TS1_SYNC 011: CSI1_HSYNC 100: SDC1_D0 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PG1_SELECT 000: Input 001: Output 010: TS1_ERR 011: CSI1_MCLK 100: SDC1_CLK 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PG0_SELECT 000: Input 001: Output 010: TS1_CLK 011: CSI1_PCLK 100: SDC1_CMD 101: Reserved 110: Reserved 111: IO Disable

3.18.6.56. PG Configure Register 1(Default Value: 0x0000_7777)

Offset: 0x00DC			Register Name: PG_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x7	PG11_SELECT 000: Input 001: Output 010: TS1_D7 011: CSI1_D7 100: UART4_RX 101: CSI0_D15 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PG10_SELECT

Offset: 0x00DC			Register Name: PG_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			000: Input 001: Output 010: TS1_D6 011: CSI1_D6 100: UART4_TX 101: CSI0_D14 110: BIST_RESULT1 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PG9_SELECT 000: Input 001: Output 010: TS1_D5 011: CSI1_D5 100: UART3_CTS 101: CSI0_D13 110: BIST_RESULT0 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PG8_SELECT 000: Input 001: Output 010: TS1_D4 011: CSI1_D4 100: UART3_RTS 101: CSI0_D12 110: Reserved 111: IO Disable

3.18.6.57. PG Configure Register 2(Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: PG_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.58. PG Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x00E4			Register Name: PG_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.59. PG Data Register(Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: PG_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.60. PG Multi-Driving Register 0(Default Value: 0x0055_5555)

Offset: 0x00EC			Register Name: PG_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PG_DRV PG[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.61. PG Multi-Driving Register 1(Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: PG_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

3.18.6.62. PG Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x00F4			Register Name: PG_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.63. PG Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: PG_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

3.18.6.64. PH Configure Register 0(Default Value: 0x3333_3333)

Offset: 0x00FC			Register Name: PH_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x3	PH7_SELECT 000: Input 001: Output 010: LCD1_D7 011: IO Disable 100: UART5_RX 101: Reserved 110: EINT7 111: CSI1_D7
27	/	/	/
26:24	R/W	0x3	PH6_SELECT

Offset: 0x00FC			Register Name: PH_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			000: Input 001: Output 010: LCD1_D6 011: IO Disable 100: UART5_TX 101: Reserved 110: EINT6 111: CSI1_D6
23	/	/	/
22:20	R/W	0x3	PH5_SELECT 000: Input 001: Output 010: LCD1_D5 011: IO Disable 100: UART4_RX 101: Reserved 110: EINT5 111: CSI1_D5
19	/	/	/
18:16	R/W	0x3	PH4_SELECT 000: Input 001: Output 010: LCD1_D4 011: IO Disable 100: UART4_TX 101: Reserved 110: EINT4 111: CSI1_D4
15	/	/	/
14:12	R/W	0x3	PH3_SELECT 000: Input 001: Output 010: LCD1_D3 011: IO Disable 100: UART3_CTS 101: Reserved 110: EINT3 111: CSI1_D3
11	/	/	/
10:8	R/W	0x3	PH2_SELECT 000: Input 001: Output 010: LCD1_D2 011: IO Disable 100: UART3_RTS 101: Reserved 110: EINT2 111: CSI1_D2
7	/	/	/
6:4	R/W	0x3	PH1_SELECT 000: Input 001: Output 010: LCD1_D1 011: IO Disable 100: UART3_RX 101: Reserved 110: EINT1 111: CSI1_D1
3	/	/	/
2:0	R/W	0x3	PH0_SELECT 000: Input 001: Output 010: LCD1_D0 011: IO Disable 100: UART3_TX 101: Reserved 110: EINT0 111: CSI1_D0

3.18.6.65. PH Configure Register 1(Default Value: 0x0033_0000)

Offset: 0x0100	Register Name: PH_CFG1

Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x0	PH15_SELECT 000: Input 010: LCD1_D15 100: KP_IN5 110: EINT15 001: Output 011: ETXD2 101: SMC_VPPPP 111: CSI1_D15
27	/	/	/
26:24	R/W	0x0	PH14_SELECT 000: Input 010: LCD1_D14 100: KP_IN4 110: EINT14 001: Output 011: ETXD3 101: SMC_VPPEN 111: CSI1_D14
23	/	/	/
22:20	R/W	0x3	PH13_SELECT 000: Input 010: LCD1_D13 100: PS2_SDA1 110: EINT13 001: Output 011: IO Disable 101: SMC_RST 111: CSI1_D13
19	/	/	/
18:16	R/W	0x3	PH12_SELECT 000: Input 010: LCD1_D12 100: PS2_SCK1 110: EINT12 001: Output 011: IO Disable 101: Reserved 111: CSI1_D12
15	/	/	/
14:12	R/W	0x0	PH11_SELECT 000: Input 010: LCD1_D11 100: KP_IN3 110: EINT11 001: Output 011: ERXD0 101: Reserved 111: CSI1_D11
11	/	/	/
10:8	R/W	0x0	PH10_SELECT 000: Input 010: LCD1_D10 100: KP_IN2 110: EINT10 001: Output 011: ERXD1 101: Reserved 111: CSI1_D10
7	/	/	/
6:4	R/W	0x0	PH9_SELECT 000: Input 010: LCD1_D9 100: KP_IN1 110: EINT9 001: Output 011: ERXD2 101: Reserved 111: CSI1_D9
3	/	/	/
2:0	R/W	0x0	PH8_SELECT 000: Input 001: Output

Offset: 0x0100			Register Name: PH_CFG1	
Bit	Read/Write	Default/Hex	Description	
			010: LCD1_D8 100: KP_IN0 110: EINT8	011: ERXD3 101: Reserved 111: CSI1_D8

3.18.6.66. PH Configure Register 2(Default Value: 0x6655_0005)

Offset: 0x0104			Register Name: PH_CFG2	
Bit	Read/Write	Default/Hex	Description	
31	/	/	/	
30:28	R/W	0x6	PH23_SELECT 000: Input 010: LCD1_D23 100: KP_OUT3 110: IO Disable	 001: Output 011: ETXEN 101: SDC1_CLK 111: CSI1_D23
27	/	/	/	
26:24	R/W	0x6	PH22_SELECT 000: Input 010: LCD1_D22 100: KP_OUT2 110: IO Disable	 001: Output 011: EMDIO 101: SDC1_CMD 111: CSI1_D22
23	/	/	/	
22:20	R/W	0x5	PH21_SELECT 000: Input 010: LCD1_D21 100: Reserved 110: EINT21	 001: Output 011: EMDC 101: IO Disable 111: CSI1_D21
19	/	/	/	
18:16	R/W	0x5	PH20_SELECT 000: Input 010: LCD1_D20 100: Reserved 110: EINT20	 001: Output 011: ERXDV 101: IO Disable 111: CSI1_D20
15	/	/	/	
14:12	R/W	0x0	PH19_SELECT 000: Input 010: LCD1_D19 100: KP_OUT1 110: EINT19	 001: Output 011: ERXERR 101: SMC_SDA 111: CSI1_D19
11	/	/	/	
10:8	R/W	0x0	PH18_SELECT 000: Input 010: LCD1_D18 100: KP_OUT0 110: EINT18	 001: Output 011: ERXCK 101: SMC_SCK 111: CSI1_D18

Offset: 0x0104			Register Name: PH_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6:4	R/W	0x0	PH17_SELECT 000: Input 001: Output 010: LCD1_D17 011: ETXD0 100: KP_IN7 101: SMC_VCCEN 110: EINT17 111: CSI1_D17
3	/	/	/
2:0	R/W	0x5	PH16_SELECT 000: Input 001: Output 010: LCD1_D16 011: ETXD1 100: KP_IN6 101: SMC_DET 110: EINT16 111: CSI1_D16

3.18.6.67. PH Configure Register 3(Default Value: 0x0000_6666)

Offset: 0x0108			Register Name: PH_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:12	R/W	0x6	PH27_SELECT 000: Input 001: Output 010: LCD1_VSYNC 011: ETXERR 100: KP_OUT7 101: SDC1_D3 110: IO Disable 111: CSI1_VSYNC
11	/	/	Reserved
10:8	R/W	0x6	PH26_SELECT 000: Input 001: Output 010: LCD1_HSYNC 011: ECOL 100: KP_OUT6 101: SDC1_D2 110: IO Disable 111: CSI1_HSYNC
7	/	/	/
6:4	R/W	0x6	PH25_SELECT 000: Input 001: Output 010: LCD1_DE 011: ECRS 100: KP_OUT5 101: SDC1_D1 110: IO Disable 111: CSI1_FIELD
3	/	/	/
2:0	R/W	0x6	PH24_SELECT 000: Input 001: Output 010: LCD1_CLK 011: ETXCK 100: KP_OUT4 101: SDC1_D0 110: IO Disable 111: CSI1_PCLK

3.18.6.68. PH Data Register(Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: PH_DAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:0	R/W	0x0	PH_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.69. PH Multi-Driving Register 0(Default Value: 0x5555_5555)

Offset: 0x0110			Register Name: PH_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.70. PH Multi-Driving Register 1(Default Value: 0x0055_5555)

Offset: 0x0114			Register Name: PH_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PH_DRV PH[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.71. PH Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: PH_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PH_PULL PH[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.72. PH Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: PH_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x011C			Register Name: PH_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~11)	R/W	0x0	PH_PULL PH[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.73. PI Configure Register 0(Default Value: 0x7777_7777)

Offset: 0x0120			Register Name: PI_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x7	PI7_SELECT 000: Input 001: Output 010: SDC3_D1 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PI6_SELECT 000: Input 001: Output 010: SDC3_D0 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PI5_SELECT 000: Input 001: Output 010: SDC3_CLK 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PI4_SELECT 000: Input 001: Output 010: SDC3_CMD 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PI3_SELECT 000: Input 001: Output 010: PWM1 011: TWI4_SDA 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PI2_SELECT 000: Input 001: Output 010: Reserved 011: TWI4_SCK

Offset: 0x0120			Register Name: PI_CFG0	
Bit	**Read/Write**	**Default/Hex**	**Description**	
			100: Reserved 110: Reserved	101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PI1_SELECT 000: Input 010: Reserved 100: Reserved 110: Reserved	 001: Output 011: TWI3_SDA 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PI0_SELECT 000: Input 010: Reserved 100: Reserved 110: Reserved	 001: Output 011: TWI3_SCK 101: Reserved 111: IO Disable

3.18.6.74. PI Configure Register 1(Default Value: 0x7777_7777)

Offset: 0x0124			Register Name: PI_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31	/	/	/	
30:28	R/W	0x7	PI15_SELECT 000: Input 010: SPI1_CS1 100: TCLKIN1 110: EINT27	 001: Output 011: PS2_SDA1 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PI14_SELECT 000: Input 010: SPI0_CS1 100: TCLKIN0 110: EINT26	 001: Output 011: PS2_SCK1 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PI13_SELECT 000: Input 010: SPI0_MISO 100: CLK_OUT_B 110: EINT25	 001: Output 011: UART6_RX 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PI12_SELECT 000: Input 010: SPI0_MOSI 100: CLK_OUT_A 110: EINT24	 001: Output 011: UART6_TX 101: Reserved 111: IO Disable
15	/	/	/	

Offset: 0x0124			Register Name: PI_CFG1	
Bit	**Read/Write**	**Default/Hex**	**Description**	
14:12	R/W	0x7	PI11_SELECT 000: Input 010: SPI0_CLK 100: Reserved 110: EINT23	 001: Output 011: UART5_RX 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PI10_SELECT 000: Input 010: SPI0_CS0 100: Reserved 110: EINT22	 001: Output 011: UART5_TX 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PI9_SELECT 000: Input 010: SDC3_D3 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PI8_SELECT 000: Input 010: SDC3_D2 100: Reserved 110: Reserved	 001: Output 011: Reserved 101: Reserved 111: IO Disable

3.18.6.75. PI Configure Register 2(Default Value: 0x0077_7777)

Offset: 0x0128			Register Name: PI_CFG2	
Bit	**Read/Write**	**Default/Hex**	**Description**	
31:23	/	/	/	
22:20	R/W	0x7	PI21_SELECT 000: Input 010: PS2_SDA0 100: Reserved 110: PWM3	 001: Output 011: UART7_RX 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PI20_SELECT 000: Input 010: PS2_SCK0 100: Reserved 110: PWM2	 001: Output 011: UART7_TX 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PI19_SELECT 000: Input	 001: Output

Offset: 0x0128			Register Name: PI_CFG2
Bit	Read/Write	Default/Hex	Description
			010: SPI1_MISO 011: UART2_RX 100: Reserved 101: Reserved 110: EINT31 111: IO Disable
11	/	/	/
10:8	R/W	0x7	PI18_SELECT 000: Input 001: Output 010: SPI1_MOSI 011: UART2_TX 100: Reserved 101: Reserved 110: EINT30 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PI17_SELECT 000: Input 001: Output 010: SPI1_CLK 011: UART2_CTS 100: Reserved 101: Reserved 110: EINT29 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PI16_SELECT 000: Input 001: Output 010: SPI1_CS0 011: UART2_RTS 100: Reserved 101: Reserved 110: EINT28 111: IO Disable

3.18.6.76. PI Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: PI_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

3.18.6.77. PI Data Register(Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: PI_DAT
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
21:0	R/W	0x0	PI_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

3.18.6.78. PI Multi-Driving Register 0(Default Value: 0x5555_5555)

Offset: 0x0134			Register Name: PI_DRV0
Bit	Read/Write	Default/Hex	Description

Offset: 0x0134			Register Name: PI_DRV0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x1	PI_DRV PI[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.79. PI Multi-Driving Register 1(Default Value: 0x0000_0555)

Offset: 0x0138			Register Name: PI_DRV1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x1	PI_DRV PI[n] Multi-Driving Select (n = 16~21) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

3.18.6.80. PI Pull Register 0(Default Value: 0x0000_0000)

Offset: 0x013C			Register Name: PI_PULL0
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R/W	0x0	PI_PULL PI[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.81. PI Pull Register 1(Default Value: 0x0000_0000)

Offset: 0x0140			Register Name: PI_PULL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PI_PULL PI[n] Pull-up/down Select (n = 16~21) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

3.18.6.82. PIO Interrupt Configure Register 0(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: PIO_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	PIO_INT_CFG External INTn Mode (n = 0~7) 0000: Positive Edge

Offset: 0x0200			Register Name: PIO_INT_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
			0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.18.6.83. PIO Interrupt Configure Register 1(Default Value: 0x0000_0000)

Offset: 0x204			Register Name: PIO_INT_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	PIO_INT_CFG External INTn Mode (n = 8~15) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.18.6.84. PIO Interrupt Configure Register 2(Default Value: 0x0000_0000)

Offset: 0x208			Register Name: PIO_INT_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	PIO_INT_CFG External INTn Mode (n = 16~23) 0000: Positive Edge 0001: Negative Edge 0010: High Level 0011: Low Level 0100: Double Edge (Positive/ Negative) Others: Reserved

3.18.6.85. PIO Interrupt Configure Register 3(Default Value: 0x0000_0000)

Offset: 0x20C			Register Name: PIO_INT_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
[4i+3:4i] (i=0~7)	R/W	0x0	PIO_INT_CFG External INTn Mode(n=24~31) 0: Positive Edge 1: Negative Edge

3.18.6.86. PIO Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x210			Register Name: PIO_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
[n] (n=0~31)	R/W	0x0	PIO_INT_CTL External INTn Enable (n = 0~31) 0: Disable 1: Enable

3.18.6.87. PIO Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x214			Register Name: PIO_INT_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
[n] (n=0~31)	R/W	0x0	PIO_INT_STATUS External INTn Pending Bit (n = 0~31) 0: No IRQ pending 1: IRQ pending Write ‘1’ to clear it

3.18.6.88. PIO Interrupt Debounce Register(Default Value: 0x0000_0000)

Offset: 0x218			Register Name: PIO_INT_DEB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0x0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32KHz 1: HOSC 24MHz

Chapter 4. Memory

This chapter details the A40i external memory.

- DRAMC
- NAND Flash Controller
- SD-MMC Host Controller

4.1. DRAMC

4.1.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industy-standard double data rate II (DDR2) ordinary SDRAM and double data rate III (DDR3) ordinary SDRAM. It supports up to 16G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

Features:

- Supports DDR2/DDR3/DDR3L/LPDDR2/LPDDR3 SDRAM
- Supports power voltage of 1.8V,1.5V,1.35V and 1.2V for different memory device
- DDR3/DDR3L interface with the maximum frequency of 576MHz
- LPDDR3 interface with the maximum frequency of 480MHz
- LPDDR2 interface with the maximum frequency of 432MHz
- Supports memory capacity up to 16Gbits (2GB)
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different applications
- Priority of transferring through multiple ports is programmable
- Random read or write operations

For complete DRAMC information, refer to the ***Allwinner A40i DRAMC Specification***.

4.2. NAND Flash Controller(NDFC)

4.2.1. Overview

The NAND Flash Controller(NDFC) supports all NAND/MLC flash memory available in the market now. New type flash can be supported by software reconfiguration. The NDFC can support 8 NAND flash with 1.8/3.3V voltage supply. There are 8 separate chip select lines (CE#) for connecting up to 8 flash chips with 2 R/B signals.

The On-the-fly error correction code (ECC) is built-in NFC for enhancing reliability. BCH is implemented and it can detect and correct up to 64 bit error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NDFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

Features:

- Complies with ONFI 2.3 and Toggle 1.0
- Up to 64-bit ECC per 512 bytes or 1024 bytes
- Supports 8-bit data bus width
- Supports 1K/2K/4K/8K/16KB page size
- Supports 8 chip selects, and 2 ready_busy signals
- Supports system boot from NAND flash
- Supports SLC/MLC NAND and EF-NAND
- Supports SDR/DDR NAND interface

4.2.2. Block Diagram

Figure 4-1 shows the block diagram of NDFC.

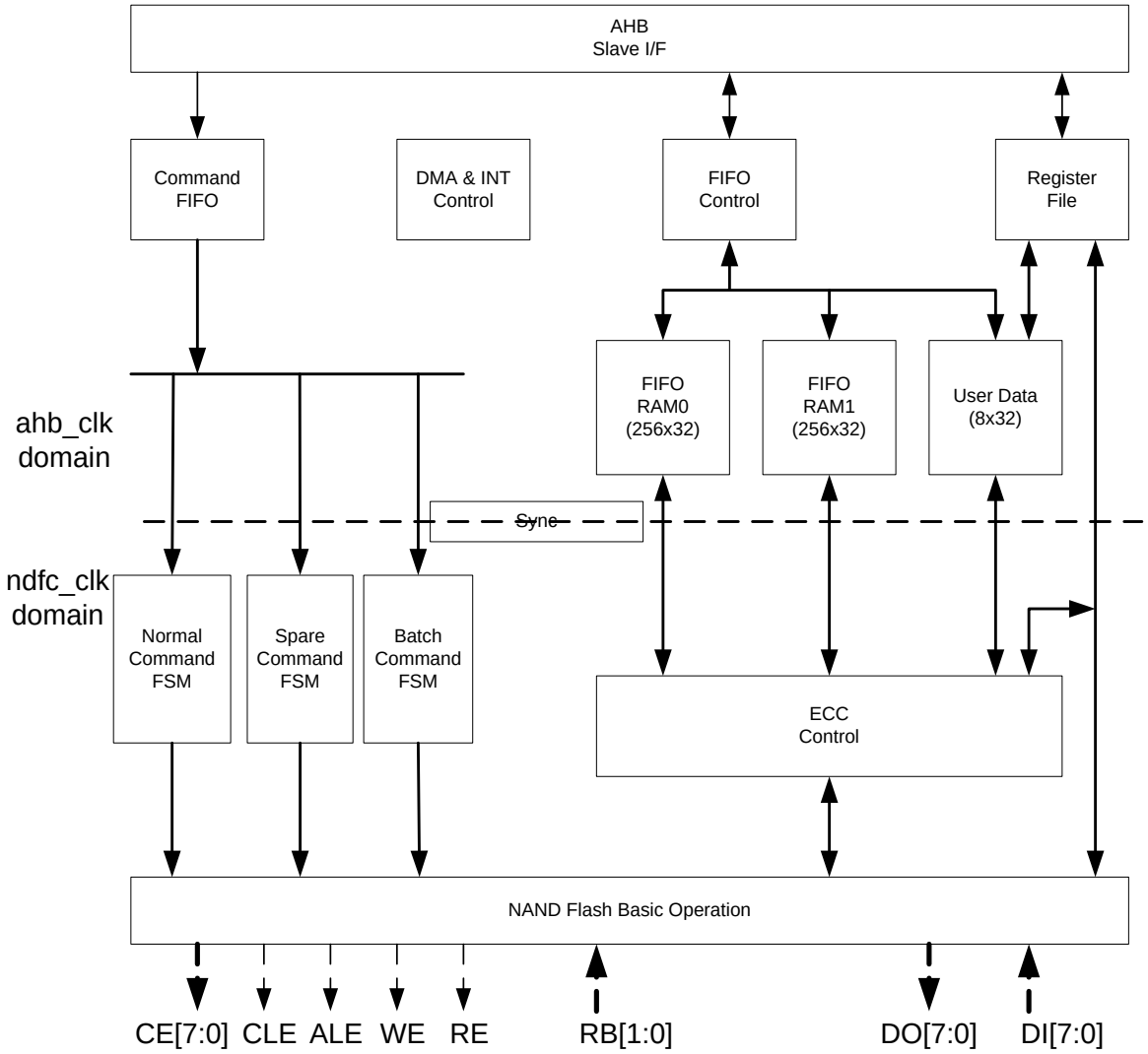


Figure 4-1. NDFC Block Diagram

4.2.3. Operations and Functional Descriptions

4.2.3.1. External Signals

The following table describes the external signals of NDFC.

Table 4-1. NDFC External Signals

Signal	Description	Type
NWE	Write Enable	O
NALE	Address Latch Enable	O
NCLE	Command Latch Enable	O
NCE[7:0]	Chip Enable	O
NRE	Read Enable	O
NRB[1:0]	Ready/Busy	I
NDQ0	Data Input / Output	I/O
NDQ1	Data Input / Output	I/O
NDQ2	Data Input / Output	I/O
NDQ3	Data Input / Output	I/O

NDQ4	Data Input / Output	I/O
NDQ5	Data Input / Output	I/O
NDQ6	Data Input / Output	I/O
NDQ7	Data Input / Output	I/O
NDQS	Data Strobe	I/O
NWP	Write Protection	O

4.2.3.2. Clock Sources

NAND Flash controller get three different clocks, Users can select one of them to make NDFC Clock Source. The following table describes the clock sources for NDFC.

Table 4-2. NDFC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0(1X)	Peripheral Clock, default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock, default value is 600MHz

4.2.3.3. NDFC Timing Diagram

Typically, there are two kinds of serial access method. One method is conventional method which fetching data at the rise edge of NFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NFC_RE# signal line.

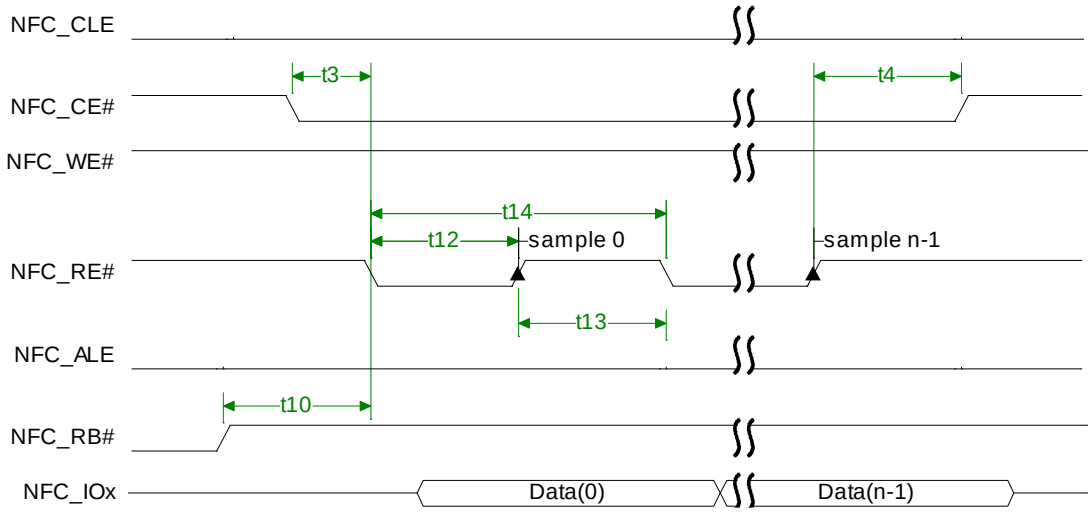


Figure 4-2. Conventional Serial Access after Read Cycle (SAM0)

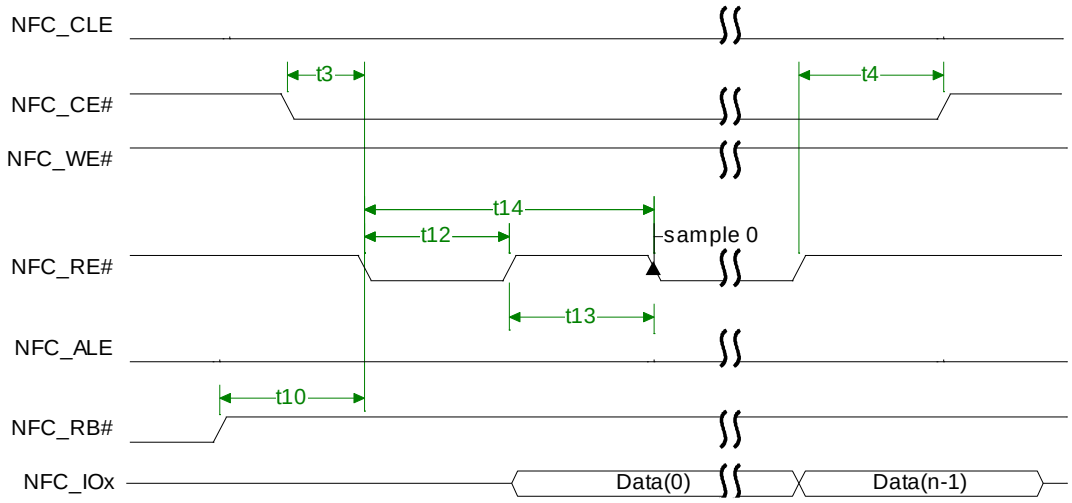


Figure 4-3. EDO type Serial Access after Read Cycle (SAM1)

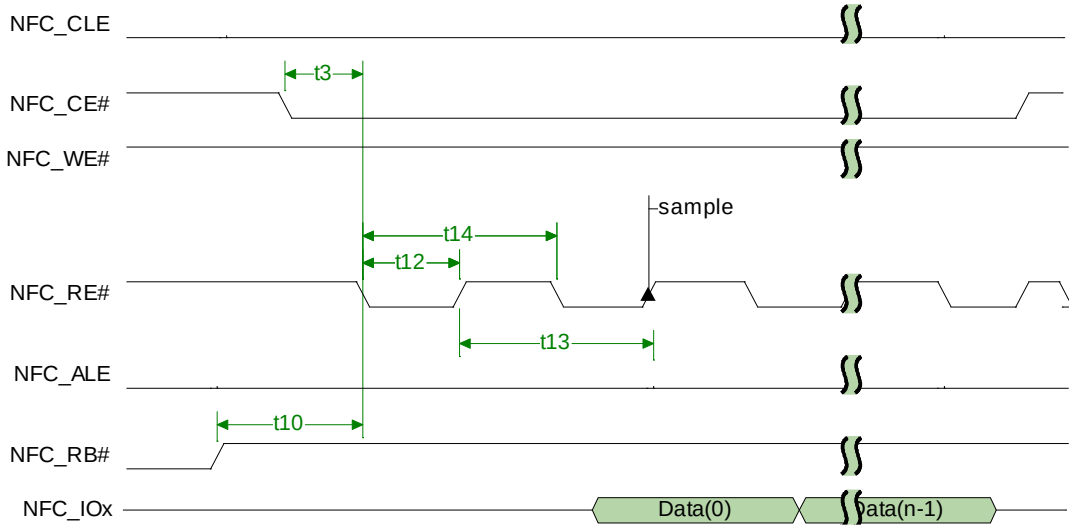


Figure 4-4. Extending EDO type Serial Access Mode (SAM2)

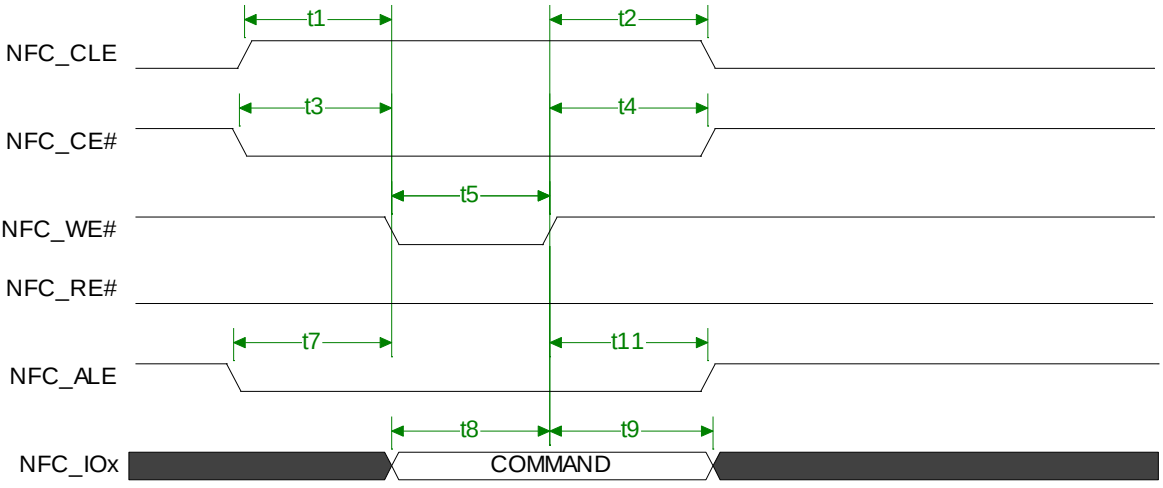


Figure 4-5. Command Latch Cycle

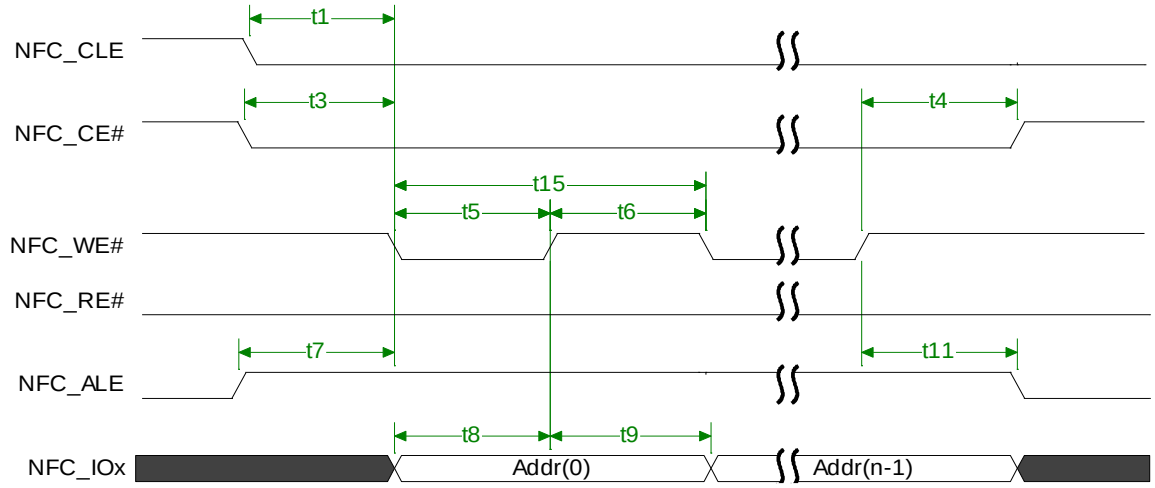


Figure 4-6. Address Latch Cycle

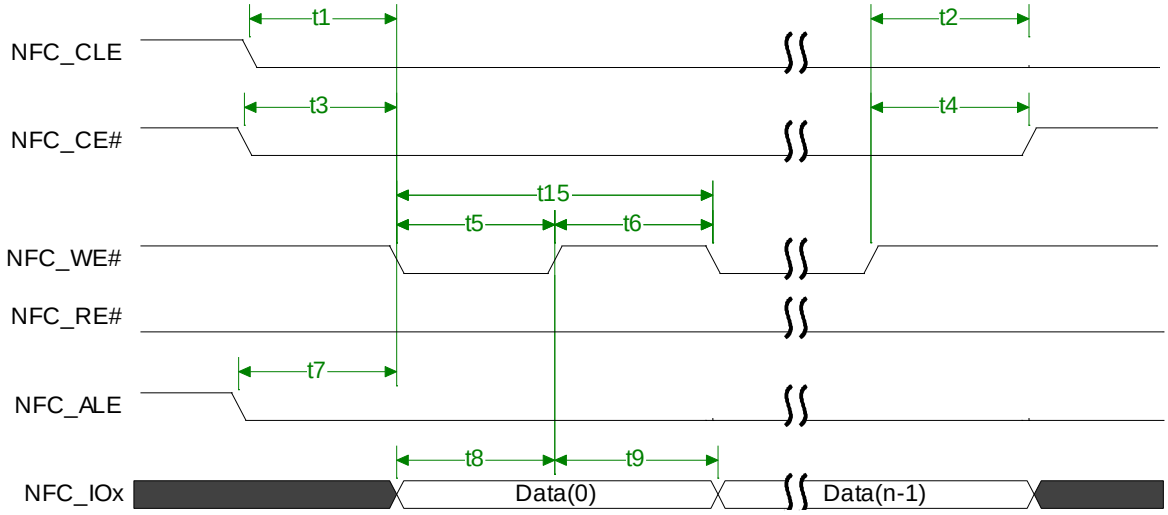


Figure 4-7. Write Data to Flash Cycle

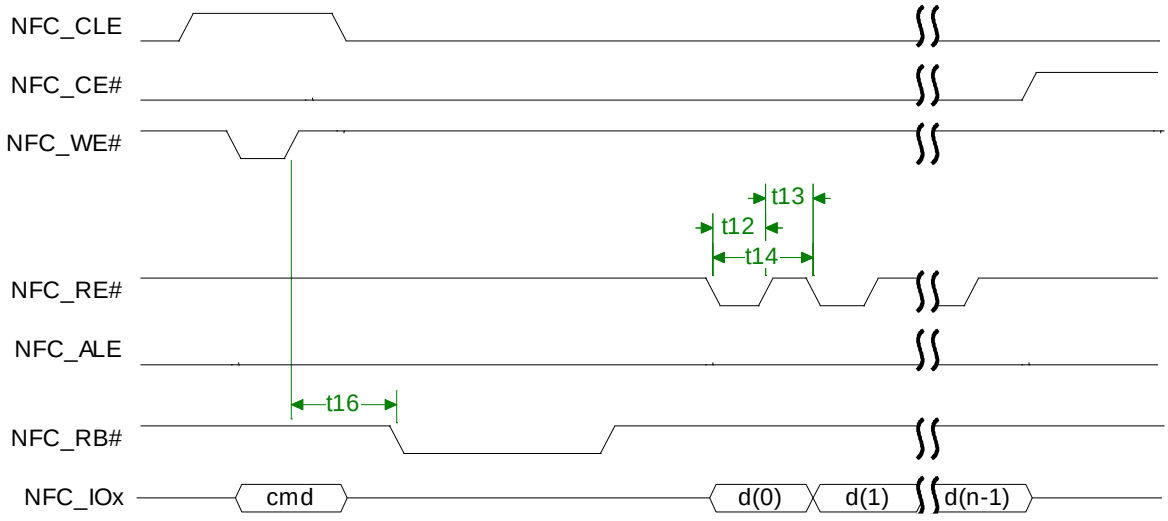


Figure 4-8. Waiting R/B# ready Diagram

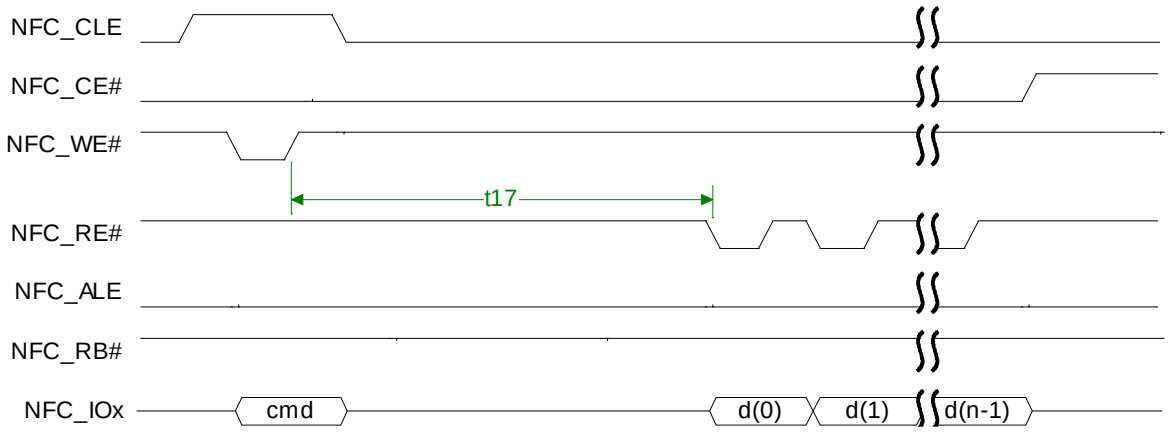


Figure 4-9. WE# high to RE# low Timing Diagram

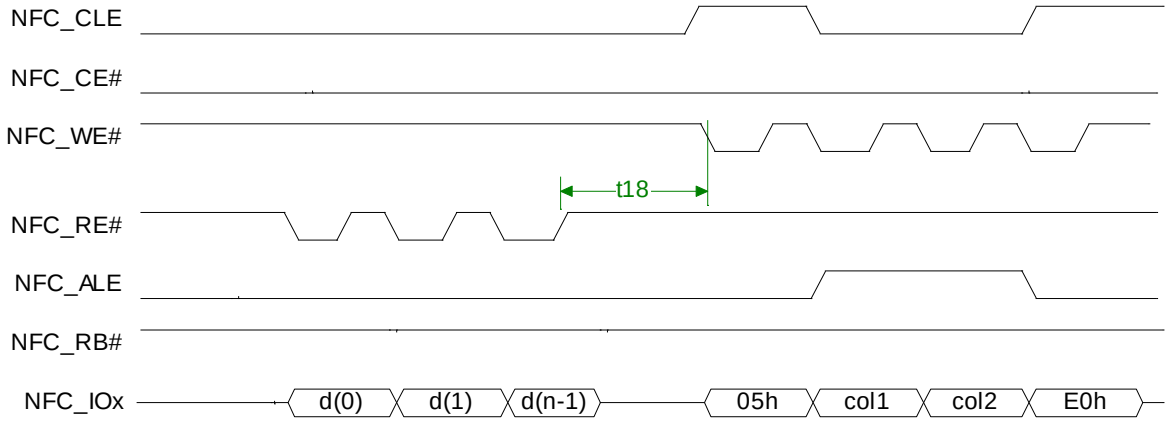


Figure 4-10. RE# high to WE# low Timing Diagram

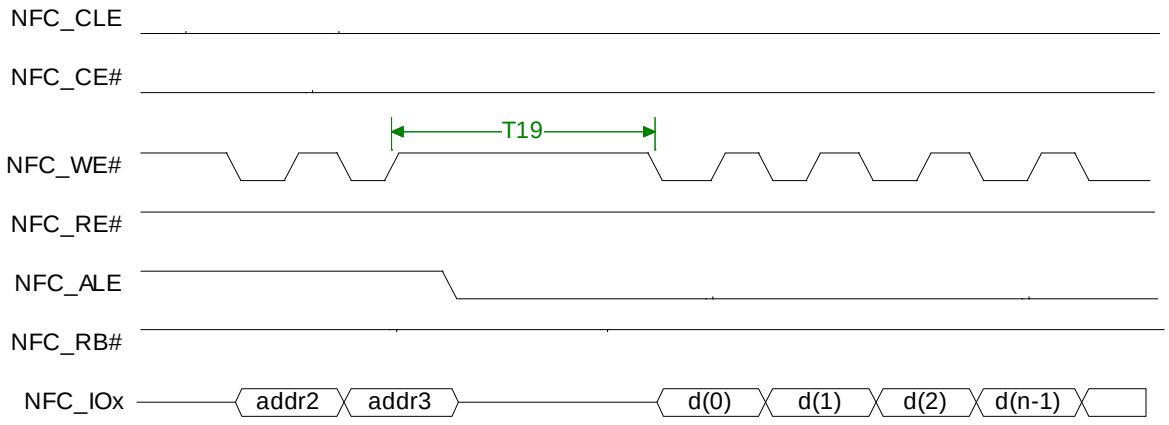


Figure 4-11. Address to Data Loading Timing Diagram

Timing Cycle List:

ID	Parameter	Timing	Notes
T1	NFC_CLE setup time	T	
T2	NFC_CLE hold time	T	

ID	Parameter	Timing	Notes
T3	NFC_CE setup time	T	
T4	NFC_CE hold time	T	
T5	NFC_WE# pulse width	T	
T6	NFC_WE# hold time	T	
T7	NFC_ALE setup time	T	
T8	Data setup time	T	
T9	Data hold time	T	
T10	Ready to NFC_RE# low	3T	
T11	NFC_ALE hold time	T	
T12	NFC_RE# pulse width	T	
T13	NFC_RE# hold time	T	
T14	Read cycle time	2T	
T15	Write cycle time	2T	
T16	NFC_WE# high to R/B# busy	tWB	Specified by timing configure register(NFC_TIMING_CFG)
T17	NFC_WE# high to NFC_RE# low	tWHR	Specified by timing configure register(NFC_TIMING_CFG)
T18	NFC_RE# high to NFC_WE# low	tRHW	Specified by timing configure register(NFC_TIMING_CFG)
T19	Address to Data Loading time	tADL	Specified by timing configure register(NFC_TIMING_CFG)

NOTE

T is the clock period duration of NFC_CLK (x2).

4.2.3.4. NDFC Operation Guide

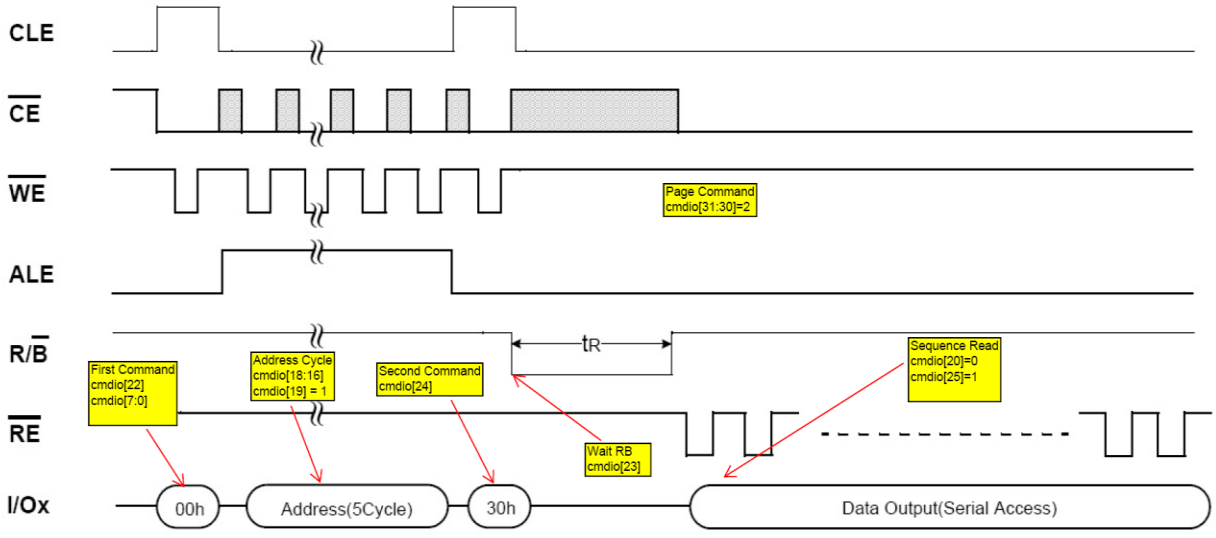


Figure 4-12. Page Read Command Diagram

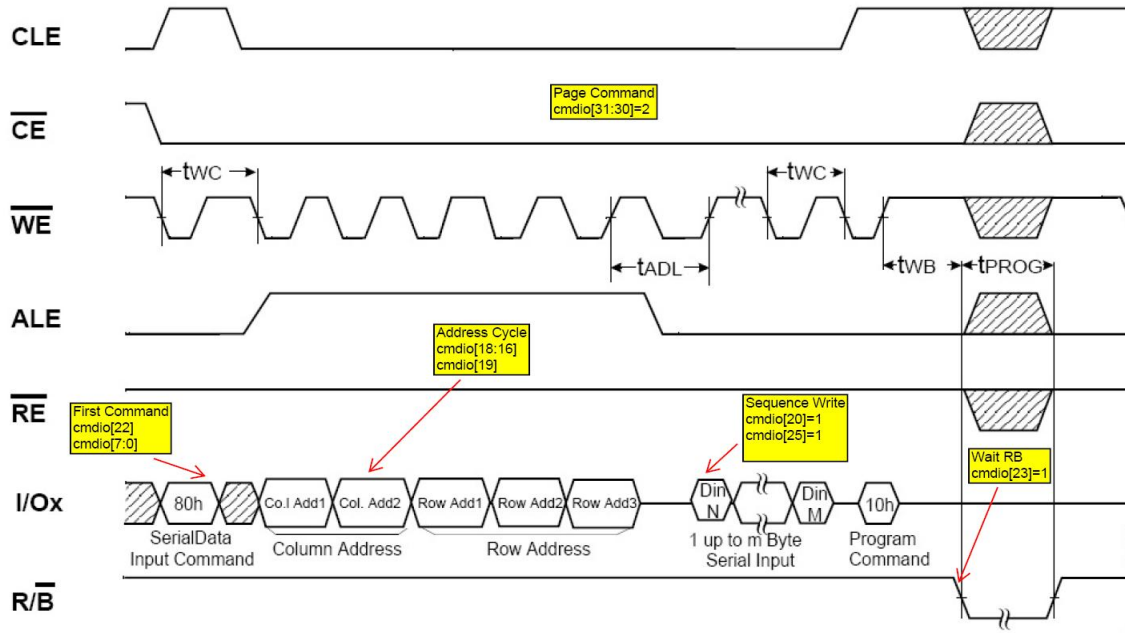


Figure 4-13. Page Program Diagram

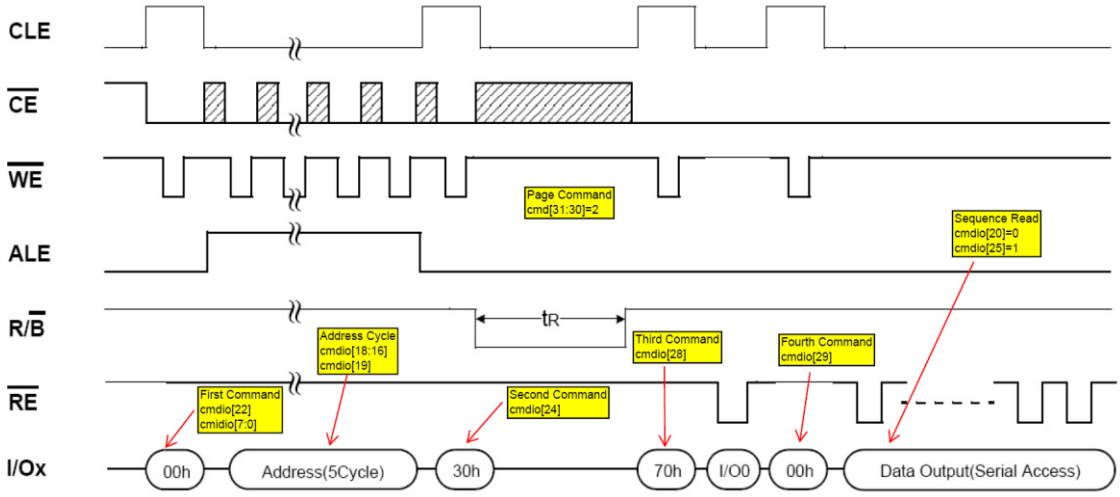


Figure 4-14. EF-NAND Page Read Diagram

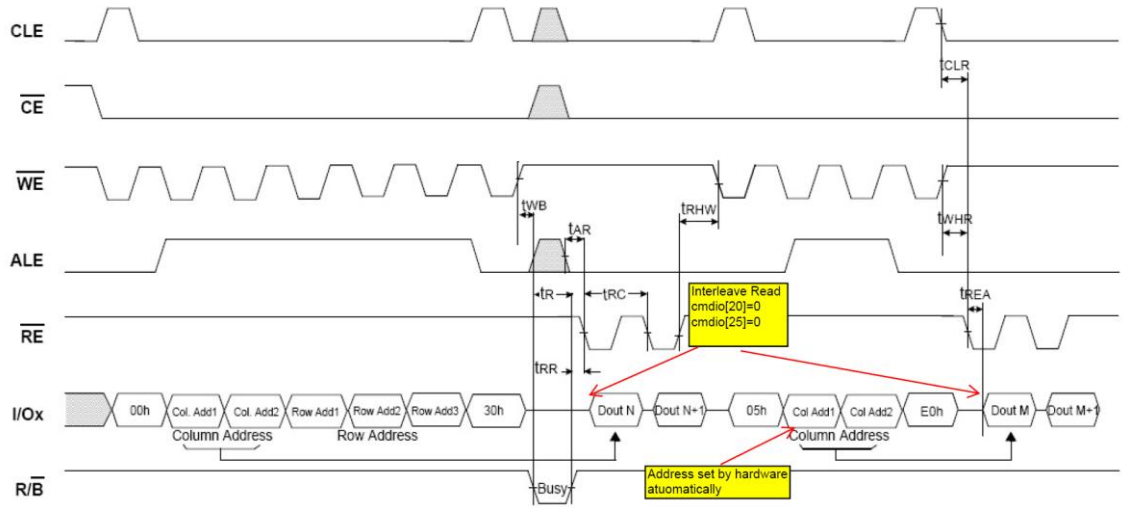


Figure 4-15. Interleave Page Read Diagram

4.2.4. Programming Guidelines

4.2.4.1. Initializing Nand Flash

The NAND Flash is initialized as follows:

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step2:Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; write 0xFF to NDFC_CMD[NDFC_CMD_LOW_BYTE] to send reset command.
Step3: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

4.2.4.2. Erasing Nand Flash

The NAND Flash is erased as follows:

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step2: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB;
Configure NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of address to be transferred;
Write the address of the block to be erased in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;
Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x60 to send block erase command.
Step3: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.
Step4: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step5: Set NDFC_CMD[NDFC_WAIT_FLAG] to 1 to ensure wait RB, set NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command; set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0xD0 to send erasing command.
Step6: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.
Step7: Read flash state until flash is ready, configure NDFC_CNT[NDFC_DATA_CNT] to set 1byte transfer data, set NDFC_CMD[NDFC_SEND_FIRST_CMD, NDFC_DATA_TRANS] to 0x3 to send the first command and transfer data. Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x70 to send read status command, read RAM0_BASE to wait ready status.

4.2.4.3. Writing Nand Flash

Step1: Erase the address of the block to be operated.
Step2: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step3: Configure RAM0_BASE to write data to RAM0.
Step4: Configure NDFC_CNT[NDFC_DATA_CNT] to set transferred data;
Set NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_DATA_TRANS, NDFC_ACCESS_DIR] to 0x3 to set access direction as writing;
Set NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of the address to be transferred, write the address of the block to be operated in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;
Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x80 to send page program command.
Step5: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step6: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; configure NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x10 to send end command.
Step7: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

4.2.4.4. Reading Nand Flash

Step1: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step2: Configure NDFC_CNT[NDFC_DATA_CNT] to set transferred data;
Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command;
Configure NDFC_CMD[NDFC_ACCESS_DIR] to 0 to set access direction as reading;
Set NDFC_CMD[NDFC_SEND_ADR] to 1 to enable transfer address, configure NDFC_CMD[NDFC_ADR_NUM] to set the number of the address to be transferred, write the address of the block to be operated in NDFC_ADDR_LOW and NDFC_ADDR_HIGH;
Set NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x00 to send page read command.
Step3: Read NDFC_ST[NDFC_RB_STATE0] to wait flash in the idle status.
Step4: Configure NDFC_CMD[NDFC_SEND_FIRST_CMD] to 1 to send the first command, configure NDFC_CMD[NDFC_WAIT_FLAG] to 1 to set wait RB; configure NDFC_CMD[NDFC_CMD_LOW_BYTE] to 0x30 to send end command.
Step5: Read RAM0_BASE to get data from flash.
Step6: Read NDFC_ST[NDFC_CMD_INT_FLAG] to wait *transfer command end interrupt flag* pending, after pending, write 1 to clear the flag.

4.2.5. Register List

Module Name	Base Address
NDFC	0x01C03000

Register Name	Offset	Description
NDFC_CTL	0x0000	NDFC Configure and Control Register
NDFC_ST	0x0004	NDFC Status Information Register
NDFC_INT	0x0008	NDFC Interrupt Control Register
NDFC_TIMING_CTL	0x000C	NDFC Timing Control Register
NDFC_TIMING_CFG	0x0010	NDFC Timing Configure Register
NDFC_ADDR_LOW	0x0014	NDFC Low Word Address Register
NDFC_ADDR_HIGH	0x0018	NDFC High Word Address Register
NDFC_BLOCK_NUM	0x001C	NDFC Data Block Number Register

NDFC_CNT	0x0020	NDFC Data Counter for Data Transfer Register
NDFC_CMD	0x0024	Set up NDFC Commands Register
NDFC_RCMD_SET	0x0028	Read Command Set Register for Vendor's NAND Memory
NDFC_WCMD_SET	0x002C	Write Command Set Register for Vendor's NAND Memory
NDFC_ECC_CTL	0x0034	ECC Configure and Control Register
NDFC_ECC_ST	0x0038	ECC Status and Operation Information Register
NDFC_EFR	0x003C	Enhanced Feature Register
NDFC_ERR_CNT0	0x0040	Corrected Error Bit Counter Register 0
NDFC_ERR_CNT1	0x0044	Corrected Error Bit Counter Register 1
NDFC_USER_DATAn	0x0050+N*0x04	User Data Field Register n (n from 0 to 15)
NDFC_EFNAND_STA	0x0090	EFNAND Status Register
NDFC_SPARE_AREA	0x00A0	Spare Area Configure Register
NDFC_PAT_ID	0x00A4	Pattern ID Register
NDFC_RDATA_STA_CTL	0x00A8	Read Data Status Control Register
NDFC_RDATA_STA_0	0x00AC	Read Data Status Register 0
NDFC_RDATA_STA_1	0x00B0	Read Data Status Register 1
NDFC_MDMA_ADDR	0x00C0	MBUS DMA Address Register
NDFC_MDMA_CNT	0x00C4	MBUS DMA Data Counter Register
NDFC_NDMA_MODE_CTL	0x00D0	NDFC Normal DMA Mode Control Register
NDFC_IO_DATA	0x0300	Data Input/Output Port Address Register
RAM0_BASE	0x0400	1024 Bytes RAM0 Base
RAM1_BASE	0x0800	1024 Bytes RAM1 Base

4.2.6. Register Description

4.2.6.1. NDFC Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			**Register Name: NDFC_CTL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0x0	NDFC_CE_SEL Chip Select for 8 NAND Flash Chips 0000 ~ 0111: NDFC Chip Select Signal 0-7 is selected 1000 ~ 1111: NDFC CS[7:0] is not selected. GPIO pins can be used for CS.
23:22	/	/	/
21	R/W	0x0	NDFC_DDR_RM DDR Repeat Data Mode 0: Lower byte 1: Higher byte
20	R/W	0x0	NDFC_DDR_REN DDR Repeat Enable 0: Disable 1: Enable
19:18	R/W	0x0	NF_TYPE NAND Flash Type 00: Normal SDR NAND 01: Reserved 10: ONFI DDR NAND 11: Toggle DDR NAND

17	R/W	0x0	NDFC_CLE_POL NDFC Command Latch Enable (CLE) Signal Polarity Select 0: High active 1: Low active
16	R/W	0x0	NDFC_ALE_POL NDFC Address Latch Enable (ALE) Signal Polarity Select 0: High active 1: Low active
15	R/W	0x0	NDFC_DMA_TYPE 0: Dedicated DMA 1: Normal DMA
14	R/W	0x0	NDFC_RAM_METHOD Access Internal RAM Method 0: Access internal RAM by AHB bus 1: Access internal RAM by DMA bus
13:12	/	/	/
11:8	R/W	0x0	NDFC_PAGE_SIZE 0000: 1024 bytes 0001: 2048 bytes 0010: 4096 bytes 0011: 8192 bytes 0100: 16384 bytes The page size is for main field data.
7	/	/	/
6	R/W	0x0	NDFC_CE_ACT Chip Select Signal CE# Control during NAND Operation 0: De-active Chip Select Signal NDFC_CE# during data loading, serial access and other no operation stage for power consumption. NDFC automatic control Chip Select Signals. 1: Chip select signal NDFC_CE# is always active after NDFC is enabled.
5	/	/	/
4:3	R/W	0x0	NDFC_RB_SEL NDFC external R/B Signal select The value 0-3 selects the external R/B signal. The same R/B signal can be used for multiple chip select flash.
2	R/W	0x0	NDFC_BUS_WIDTH 0: 8-bit bus 1: 16-bit bus
1	R/W	0x0	NDFC_RESET NDFC Reset Write 1 to reset NDFC and clear to 0 after reset
0	R/W	0x0	NDFC_EN NDFC Enable Control 0: Disable NDFC 1: Enable NDFC

4.2.6.2. NDFC Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: NDFC_ST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R	0x0	NDFC_RDATA_STA_0 0: The number of bit 1 during current read operation is greater threshold value. 1: The number of bit 1 during current read operation is less than or equal to threshold value. This field only is valid when **NDFC_RDATA_STA_EN** is 1. The threshold value is configured in **NDFC_RDATA_STA_TH**.
12	R	0x0	NDFC_RDATA_STA_1 0: The number of bit 0 during current read operation is greater threshold value. 1: The number of bit 0 during current read operation is less than or equal to than threshold value. This field only is valid when **NDFC_RDATA_STA_EN** is 1. The threshold value is configured in **NDFC_RDATA_STA_TH**.
11	R	0x0	NDFC_RB_STATE3 NAND Flash R/B 3 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
10	R	0x0	NDFC_RB_STATE2 NAND Flash R/B 2 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
9	R	0x0	NDFC_RB_STATE1 NAND Flash R/B 1 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
8	R	0x0	NDFC_RB_STATE0 NAND Flash R/B 0 Line State 0: NAND Flash in BUSY State 1: NAND Flash in READY State
7:5	/	/	/
4	R	0x0	NDFC_STA 0: NDFC FSM in IDLE State 1: NDFC FSM in BUSY State When NDFC_STA is 0, NDFC can accept new command and process command.
3	R	0x0	NDFC_CMD_FIFO_STATUS 0: Command FIFO not full and can receive new command 1: Full and waiting NDFC to process commands in FIFO Since there is only one 32-bit FIFO for command. When NDFC latches one command, command FIFO is free and can accept another new command.
2	R/W	0x0	NDFC_DMA_INT_FLAG

			When it is 1, it means that a pending DMA is completed. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing an new command.
1	R/W	0x0	NDFC_CMD_INT_FLAG When it is 1, it means that NDFC has finished one Normal Command Mode or one Batch Command Work Mode. It will be cleared after writing 1 to this bit or it will be automatically cleared before FSM processing a new command.
0	R/W	0x0	NDFC_RB_B2R When it is 1, it means that NDFC_R/B# signal is transferred from BUSY state to READY state. It will be cleared after writing 1 to this bit.

4.2.6.3. NDFC Interrupt and DMA Enable Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: NDFC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	NDFC_DMA_INT_ENABLE Enable or disable interrupt when a pending DMA is completed.
1	R/W	0x0	NDFC_CMD_INT_ENABLE Enable or disable interrupt when NDFC has finished the procession of a single command in Normal Command Work Mode or one Batch Command Work Mode. 0: Disable 1: Enable
0	R/W	0x0	NDFC_B2R_INT_ENABLE Enable or disable interrupt when NDFC_RB# signal is transferring from BUSY state to READY state. 0: Disable 1: Enable

4.2.6.4. NDFC Timing Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: NDFC_TIMING_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	NDFC_READ_PIPE In SDR mode: 0000: Normal 0001: EDO 0010: E-EDO Other : Reserved In DDR mode: 0001~1111 is valid.(These bits configure the number of clock when data is valid after RE#'s falling edge)
7:6	/	/	/
5:0	R/W	0x0	NDFC_DC_CTL NDFC Delay Chain Control. (These bits are only valid in DDR data interface,

			and configure the relative phase between DQS and DQ[0…7])

4.2.6.5. NDFC Timing Configure Register(Default Value: 0x0000_0095)

Offset: 0x0010			Register Name: NDFC_TIMING_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:18	R/W	0x0	T_WC Write Cycle Time 00: 1*2T 01: 2*2T 10: 3*2T 11: 4*2T
17:16	R/W	0x0	T_CCS Change Column Setup Time 00: 16*2T 01: 24*2T 10: 32*2T 11: 64*2T
15:14	R/W	0x0	T_CLHZ CLE High to Output Hi-z 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
13:12	R/W	0x0	T_CS CE Setup Time 00: 2*2T 01: 8*2T 10: 16*2T 11: 31*2T
11	R/W	0x0	T_CDQSS DQS Setup Time for Data Input Start 0: 8*2T 1: 24*2T
10:8	R/W	0x0	T_CAD Command, Address, Data Delay 000: 4*2T 001: 8*2T 010: 12*2T 011: 16*2T 100: 24*2T 101: 32*2T 110/111: 64*2T
7:6	R/W	0x2	T_RHW RE# High to WE# Low Cycle Number 00: 4*2T

			01: 8*2T 10: 12*2T 11: 20*2T
5:4	R/W	0x1	T_WHR WE# High to RE# Low Cycle Number 00: 8*2T 01: 16*2T 10: 24*2T 11: 32*2T
3:2	R/W	0x1	T_ADL Address to Data Loading Cycle Number 00: 0*2T 01: 8*2T 10: 16*2T 11: 24*2T
1:0	R/W	0x1	T_WB WE# High to Busy Cycle Number 00: 14*2T 01: 22*2T 10: 30*2T 11: 38*2T

4.2.6.6. NDFC Address Low Word Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: NDFC_ADDR_LOW
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA4 NAND Flash 4th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA3 NAND Flash 3rd Cycle Address Data
15:8	R/W	0x0	ADDR_DATA2 NAND Flash 2nd Cycle Address Data
7:0	R/W	0x0	ADDR_DATA1 NAND Flash 1st Cycle Address Data

4.2.6.7. NDFC Address High Word Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: NDFC_ADDR_HIGH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	ADDR_DATA8 NAND Flash 8th Cycle Address Data
23:16	R/W	0x0	ADDR_DATA7 NAND Flash 7th Cycle Address Data
15:8	R/W	0x0	ADDR_DATA6 NAND Flash 6th Cycle Address Data
7:0	R/W	0x0	ADDR_DATA5 NAND Flash 5th Cycle Address Data

4.2.6.8. NDFC Data Block Number Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: NDFC_DATA_BLOCK_NUM
Bit	**R/W**	**Default/Hex**	**Description**
31:6	/	/	/
4:0	R/W	0x0	NDFC_DATA_BLOCK_NUM DATA BLOCK Number It is used for batch command procession. 00000: no data 00001: 1 data block 00010: 2 data blocks … 10000: 16 data blocks Others: Reserved **NOTE** **1 data block = 512 or 1024 bytes main field data.**

4.2.6.9. NDFC Data Counter Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: NDFC_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	NDFC_DATA_CNT Transfer Data Byte Counter The length can be set from 1 byte to 1024 bytes. However, 1024 bytes is set when it is zero.

4.2.6.10. NDFC Command IO Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: NDFC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x0	NDFC_CMD_TYPE 00: Common Command for normal operation 01: Special Command for Flash Spare Field Operation 10: Page Command for batch process operation 11: Reserved
29	R/W	0x0	NDFC_SEND_FOURTH_CMD 0: Don’t send third set command 1: Send it on the external memory’s bus It is used for EF-NAND page read.
28	R/W	0x0	NDFC_SEND_THIRD_CMD 0: Don’t send third set command 1: Send it on the external memory’s bus It is used for EF-NAND page read.
27	R/W	0x0	NDFC_ROW_ADDR_AUTO Row Address Auto Increase for Page Command

			0: Normal operation 1: Row address increasing automatically
26	R/W	0x0	NDFC_DATA_METHOD Data swap method when the internal RAM and system memory It is only active for Common Command and Special Command. 0: No action 1: DMA transfer automatically It only is active when **NDFC_RAM_METHOD** is 1. If this bit is set to 1, NDFC should setup DRQ to fetching data before output to Flash or NDFC should setup DRQ to sending out to system memory after fetching data from Flash. If this bit is set to 0, NDFC output the data in internal RAM or do nothing after fetching data from Flash.
25	R/W	0x0	NDFC_SEQ User data & BCH check word position. It only is active for Page Command, don't care about this bit for other two commands 0: Interleave Method (on page spare area) 1: Sequence Method (following data block)
24	R/W	0x0	NDFC_SEND_SECOND_CMD 0: Don't send second set command 1: Send it on the external memory's bus
23	R/W	0x0	NDFC_WAIT_FLAG 0: NDFC can transfer data regardless of the internal NDFC_RB wire 1: NDFC can transfer data when the internal NDFC_RB wire is READY; otherwise it can't when the internal NDFC_RB wire is BUSY.
22	R/W	0x0	NDFC_SEND_FIRST_CMD 0: Don't send first set command 1: Send it on the external memory's bus
21	R/W	0x0	NDFC_DATA_TRANS 0: No data transfer on external memory bus 1: Data transfer and direction is decided by the field **NDFC_ACCESS_DIR**
20	R/W	0x0	NDFC_ACCESS_DIR 0: Read NAND Flash 1: Write NAND Flash
19	R/W	0x0	NDFC_SEND_ADR 0: Don't send ADDRESS 1: Send N cycles ADDRESS, the number N is specified by **NDFC_ADR_NUM**
18:16	R/W	0x0	NDFC_ADR_NUM Address Cycles' Number 000: 1 cycle address field 001: 2 cycles address field 010: 3 cycles address field 011: 4 cycles address field 100: 5 cycles address field 101: 6 cycles address field 110: 7 cycles address field 111: 8 cycles address field

15:8	R/W	0x0	NDFC_CMD_HIGH_BYTE NDFC Command high byte data If 8-bit command is supported, the high byte should be zero for 16-bit bus width NAND Flash. For 8-bit bus width NAND Flash, high byte command is discarded.
7:0	R/W	0x0	NDFC_CMD_LOW_BYTE NDFC Command low byte data This command will be sent to external Flash by NDFC.

4.2.6.11. NDFC Command Set Register 0(Default Value: 0x00E0_0530)

Offset: 0x0028			Register Name: NDFC_CMD_SET0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0xE0	NDFC_RANDOM_READ_CMD1 Used for Batch Read Operation
15:8	R/W	0x05	NDFC_RANDOM_READ_CMD0 Used for Batch Read Operation
7:0	R/W	0x30	NDFC_READ_CMD Used for Batch Read Operation

4.2.6.12. NDFC Command Set Register 1(Default Value: 0x7000_8510)

Offset: 0x002C			Register Name: NDFC_CMD_SET1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x70	NDFC_READ_CMD0 Used for EF-NAND Page Read Operation
23:16	R/W	0x00	NDFC_READ_CMD1 Used for EF-NAND Page Read Operation
15:8	R/W	0x85	NDFC_RANDOM_WRITE_CMD Used for Batch Write Operation
7:0	R/W	0x10	NDFC_PROGRAM_CMD Used for Batch Write Operation

4.2.6.13. NDFC ECC Control Register(Default Value: 0x4A80_0008)

Offset: 0x0034			Register Name: NDFC_ECC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x4a80	NDFC_RANDOM_SEED The seed value for randomize engine. It is only active when **NDFC_RANDOM_EN** is set to '1'.
15:12	R/W	0x0	NDFC_ECC_MODE 0000: BCH-16 for one ECC Data Block 0001: BCH-24 for one ECC Data Block 0010 : BCH-28 for one ECC Data Block 0011 : BCH-32 for one ECC Data Block 0100 : BCH-40 for one ECC Data Block 0101 : BCH-48 for one ECC Data Block 0110 : BCH-56 for one ECC Data Block

			0111 : BCH-60 for one ECC Data Block 1000 : BCH-64 for one ECC Data Block Others: Reserved
11	R/W	0x0	NDFC_RANDOM_SIZE 0: ECC block size 1: Page size
10	R/W	0x0	NDFC_RANDOM_DIRECTION 0: LSB first 1: MSB first
9	R/W	0x0	NDFC_RANDOM_EN 0: Disable Data Randomize 1: Enable Data Randomize
8:6	/	/	/
5	R/W	0x0	NDFC_ECC_BLOCK_SIZE 0: 1024 bytes of one ECC data block 1: 512 bytes of one ECC data block
4	R/W	0x0	NDFC_ECC_EXCEPTION 0: Normal ECC 1: For ECC, there is an exception. If all data is 0xff or 0x00 for the block. When reading this page, ECC assumes that it is right. For this case, no error information is reported. **NOTE** **It is only active when ECC is ON.**
3	R/W	0x1	NDFC_ECC_PIPELINE Pipeline function enable or disable for batch command 0: Error Correction function no pipeline with next block operation 1: Error Correction pipeline
2:1	/	/	/
0	R/W	0x0	NDFC_ECC_EN 0: ECC is OFF 1: ECC is ON

4.2.6.14. NDFC ECC Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			**Register Name: NDFC_ECC_ST**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	NDFC_PAT_FOUND Special pattern (all 0x00 or all x0ff) Found Flag for 16 Data Blocks 0: No Found 1: Special pattern is found When this field is '1', this means that the special data is found for reading external NAND flash. The register of **NDFC_PAT_ID** would indicate which pattern is found.
15:0	R	0x0	NDFC_ECC_ERR Error information bit of 16 Data Blocks

			0: ECC can correct these error bits or there is no error bit 1: Error bits number beyond of ECC correction capability and can not correct them **NOTE** **The LSB of this register is corresponding the 1st ECC data block. 1 ECC Data Block = 512 or 1024 byte.**

4.2.6.15. NDFC Enhanced Feature Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: NDFC_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	NDFC_WP_CTRL NAND Flash Write Protect Control 0: Write Protect is active 1: Write Protect is not active When the bit is '0', WP signal line is low level and external NAND flash is on protected state.
7	/	/	/
6:0	R/W	0x0	NDFC_ECC_DEBUG For the purpose of debugging ECC engine, special bit error is inserted before writing external Flash Memory. 0: No error is inserted (ECC Normal Operation) n: N bits error are inserted

4.2.6.16. NDFC Error Counter Register 0(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: NDFC_ERR_CNT0
Bit	**Read/Write**	**Default/Hex**	**Description**
[8i+7:8i] (i=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 0 to 3) 0: No corrected bit 1: 1 corrected bit 2: 2 corrected bit … 64: 64 corrected bit Others: Reserved **NOTE** **1 ECC Data Block = 512 or 1024 byte**

4.2.6.17. NDFC Error Counter Register 1(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: NDFC_ERR_CNT1
Bit	**Read/Write**	**Default/Hex**	**Description**
[8i+7:8i] (i=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 4 to 7)

			0000000: No corrected bit 0000001: 1 corrected bit 0000010: 2 corrected bit … 1000000: 64 corrected bit Others: Reserved **NOTE** **1 ECC Data Block = 512 or 1024 byte**

4.2.6.18. NDFC Error Counter Register 2(Default Value: 0x00000000)

Offset: 0x0048			Register Name: NDFC_ERR_CNT2
Bit	**Read/Write**	**Default/Hex**	**Description**
[8i+7:8i] (i=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 8 to 11) 0000000: No corrected bit 0000001: 1 corrected bit 0000010: 2 corrected bit … 1000000: 64 corrected bit Others: Reserved **NOTE** **1 ECC Data Block = 512 or 1024 byte**

4.2.6.19. NDFC Error Counter Register 3(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: NDFC_ERR_CNT3
Bit	**Read/Write**	**Default/Hex**	**Description**
[8i+7:8i] (i=0~3)	R	0x0	ECC_COR_NUM ECC Corrected Bits Number for ECC Data Block[n] (n from 12 to 15) 0000000: No corrected bit 0000001: 1 corrected bit 0000010: 2 corrected bit … 1000000: 64 corrected bit Others: Reserved **NOTE** **1 ECC Data Block = 512 or 1024 byte**

4.2.6.20. NDFC User Data Register [n](Default Value:0xFFFF_FFFF)

Offset: 0x0050 + N*0x04			Register Name: NDFC_USER_DATAn(n=0~15)
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	USER_DATA User Data for ECC Data Block[n] (n from 0 to 15)

			NOTE 1 ECC Data Block = 512 or 1024 bytes

4.2.6.21. NDFC EFNAND Status Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: NDFC_EFNAND_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	EF_NAND_STATUS The Status Value for EF-NAND Page Read operation

4.2.6.22. NDFC Spare Area Register(Default Value: 0x0000_0400)

Offset: 0x00A0			Register Name: NDFC_SPARE_AREA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x400	NDFC_SPARE_ADR This value indicates the spare area first byte address for NDFC interleave page operation.

4.2.6.23. NDFC Pattern ID Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: NDFC_PAT_ID
Bit	**Read/Write**	**Default/Hex**	**Description**
[2i+1:2i] (i=0~15)	R	0x0	PAT_ID Special Pattern ID for 16 ECC data block 0: All 0x00 is found 1: All 0xFF is found Others: Reserved

4.2.6.24. NDFC Read Data Status Control Register(Default Value: 0x0100_0000)

Offset: 0x00A8			Register Name: NDFC_RDATA_STA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x1	NDFC_RDATA_STA_EN 0: Disable to count the number of bit 1 and bit 0 during current read operation 1: Enable to count the number of bit 1 and bit 0 during current read operation The number of bit 1 and bit 0 during current read operation can be used to check whether a page is blank or bad.
23:18	/	/	/
17:0	R/W	0x0	NDFC_RDATA_STA_TH The threshold value to generate data status. If the number of bit 1 during current read operation is less than or equal to

			threshold value, **NDFC_RDATA_STA_0** will be set. If the number of bit 0 during current read operation is less than or equal to threshold value, **NDFC_RDATA_STA_1** will be set.

4.2.6.25. NDFC Read Data Status Register 0(Default Value: 0x0000_0000)

Offset: 0x00AC			Register Name: NDFC_RDATA_STA_0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_1 The number of input bit 1 during current command. It will be cleared automatically when next command is executed.

4.2.6.26. NDFC Read Data Status Register 1(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: NDFC_RDATA_STA_1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	BIT_CNT_0 The number of input bit 0 during current command. It will be cleared automatically when next command is executed.

4.2.6.27. NDFC MBUS DMA Address Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: NDFC_MDMA_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MDMA_ADDR MBUS DMA address

4.2.6.28. NDFC MBUS DMA Byte Counter Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: NDFC_MDMA_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
14:0	R/W	0x0	MDMA_CNT MBUS DMA data counter

4.2.6.29. NDFC Normal DMA Mode Control Register(Default Value: 0x0000_00A5)

Offset: 0x00D0			Register Name: NDFC_NDMA_MODE_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R/W	0xA5	NDMA_MODE_CTL 0xEA:NDMA handshake mode **NOTE** **NDMA wait mode don't care this value. 0xA5 can be used in handshake mode, but 0xEA is better.**

4.2.6.30. NDFC IO Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: NDFC_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	NDFC_IO_DATA Read/Write data into internal RAM Access unit is 32-bit.

4.3. SD-MMC Host Controller(SMHC)

4.3.1. Overview

The SD-MMC Host Controller(SMHC) can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card.

Features:

- Supports Secure Digital memory protocol commands (up to SD3.0)
- Supports Secure Digital I/O protocol commands(up to SDIO2.0)
- Supports Multimedia Card protocol commands (up to MMC5.0)
- Supports eMMC boot operation and alternative boot operation
- Supports Command Completion signal and interrupt to host processor and Command Completion signal disable feature
- Supports hardware CRC generation and error detection
- Supports host pull-up control
- Supports SDIO interrupt in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 1024 bytes FIFO for data transfer

4.3.2. Block Diagram

Figure 4-16 shows the block diagram of SMHC.

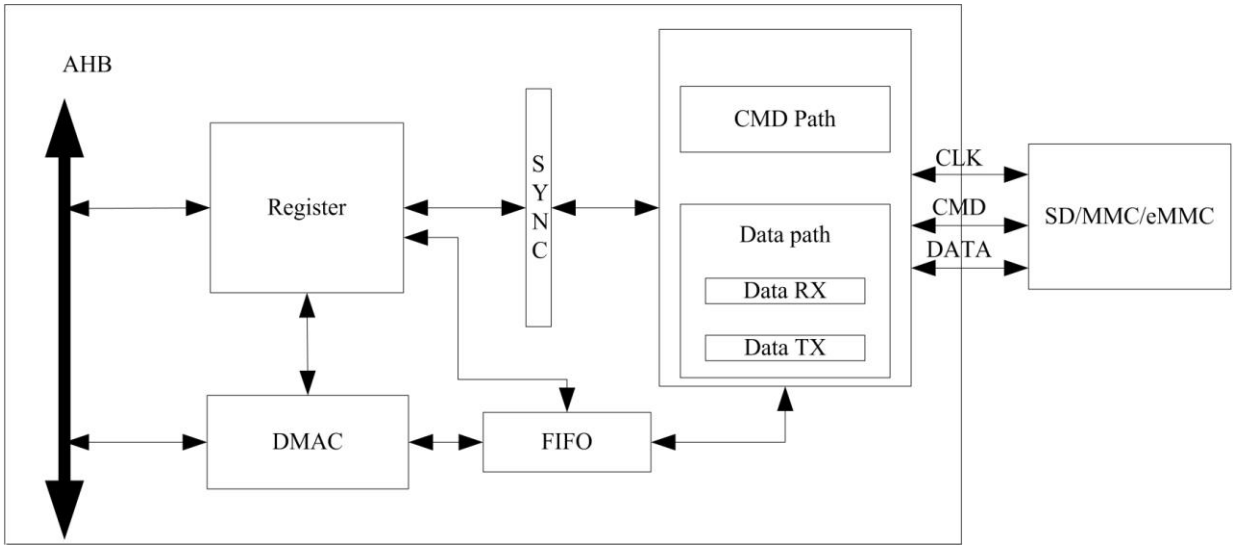


Figure 4-16. SMHC Block Diagram

4.3.3. Operations and Functional Descriptions

4.3.3.1. External Signals

The following table describes the external signals of SMHC.

Table 4-3. SMHC External Signals

Port Name	Width	Type	Description
SDC0			
SDC0_CLK	1	O	Clock signal for card
SDC0_CMD	1	I/O	Command line for card
SDC0_D[3:0]	4	I/O	Data lines for card
SDC1			
SDC1_CLK	1	O	Clock signal for SDIO WIFI
SDC1_CMD	1	I/O	Command line for SDIO WIFI
SDC1_D[3:0]	4	I/O	Data lines for SDIO WIFI
SDC2			
SDC2_CLK	1	O	Clock signal for eMMC
SDC2_CMD	1	I/O	Command line for eMMC
SDC2_D[7:0]	8	I/O	Data lines for eMMC
SDC2_DS	1	I	Data strobe signal for eMMC
SDC2_RST	1	O	Reset signal for eMMC
SDC3			
SDC3_CLK	1	O	Clock signal for card
SDC3_CMD	1	I/O	Command line for card
SDC3_D[3:0]	4	I/O	Data lines for card

4.3.3.2. Clock Sources

The following table describes the clock sources of SMHC. Users can select one of them as SMHC's clock source.

Table 4-4. SMHC Clock Sources

Clock Sources	Description
OSC24M	24M Crystal
PLL_PERIPH0(2X)	Peripheral Clock, default value is 1.2GHz
PLL_PERIPH1(2X)	Peripheral Clock, default value is 1.2GHz

4.3.3.3. Timing Diagram

- Physical Layer Specification Ver3.00 Final, 2009.04.16
- SDIO Specification Ver2.00
- Multimedia Cards (MMC : version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard
- JEDEC Standard – JESD84-B45, Embedded Multimedia Card (eMMC) Electrical Standard(4.5 Device)
- JEDEC Standard – JESD84-B50, Embedded Multimedia Card (eMMC) Electrical Standard(5.0)

4.3.3.4. Calibrate Delay Chain

The sample clock delay chain and Data Strobe delay chain(only in SMHC2) are used to generate delay to make proper timing between sample clock/data strobe and data signals. Each delay chain is made up with 64 delay cells. The delay

time of one delay cell can be estimated through delay chain calibration.

The steps to calibrate delay chain are as follows:

Step1: Enable SMHC. In order to calibrate delay chain by operation registers in SMHC, SMHC must be enabled through **Bus Software Reset Register 0** and **Bus Clock Gating Register0**.

Step2: Configure a proper clock for SMHC. Calibration delay chain is based on the clock for SMHC from Clock Control Unit(**CCU**). Calibration delay chain a internal function in SMHC and don't need device. So, it is unnecessary to open clock signal for device. The recommended clock frequency is 200MHz.

Step3: Set proper initial delay value. Writing 0xA0 to **delay control register** enables **Delay Software Enable (bit[7])** and sets initial delay value 0x20 to **Delay chain(bit[5:0])**. Then write 0x0 to **delay control register** to clear the value.

Step4: Write 0x8000 to **delay control register** to start calibrate delay chain.

Step5: Wait until the flag(Bit14 in **delay control register**) of calibration done is set. The number of delay cells is shown at Bit8~Bit13 in **delay control register**. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This value is the result of calibration.

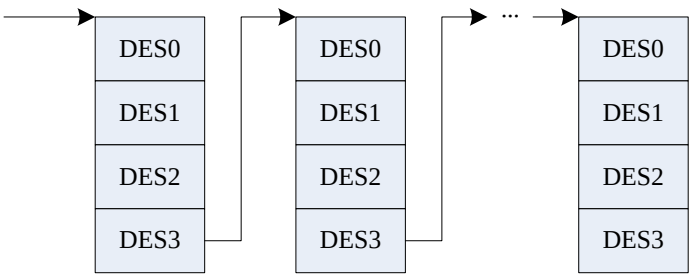
Step6: Calculate the delay time of one delay cell according to the cycle of SMHC's clock and the result of calibration.

4.3.3.5. SMHC DMA Controller Description

SMHC controller has an internal DMA controller (IDMAC) to transfer data between host memory and SDMMC port. With a descriptor, IDMAC can efficiently move data from source to destination by automatically loading next DMA transfer arguments, which need less CPU intervention. Before transfer data in IDMAC, host driver should construct a descriptor list, configure arguments of every DMA transfer, then launch the descriptor and start the DMA. IDMAC has an interrupt controller, when enabled, it can interrupt the HOST CPU in situations such as data transmission completed or some errors happened.

(1) IDMAC Descriptor Structure

The IDMAC uses a descriptor with a chain structure, and each descriptor points to a unique buffer and the next descriptor.



This figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit buses. Each descriptor contains 16 bytes of control and status information.

DES0 is a notation used to denote the [31:0] bits, **DES1** to denote [63:32] bits, **DES2** to denote [95:64]bits, and **DES3** to denote [127:96]bits in a descriptor.

(2) DES0 Definition

Bits	Name	Descriptor
31	HOLD	DES_OWN_FLAG When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the host. This bit is cleared when transfer is over.
30	ERROR	ERR_FLAG When some error happened in transfer, this bit will be set.
29:6	/	/
5	/	Not used
4	Chain Flag	CHAIN_MOD When set, this bit indicates that the second address in descriptor is the next descriptor address. Must be set 1.
3	First DES Flag	FIRST_FLAG When set, this bit indicates that this descriptor contains the first buffer of data. Must be set to 1 in first DES.
2	Last DES Flag	LAST_FLAG When set, this bit indicates that the buffers pointed to by this descriptor are the last data buffer.
1	Disable Interrupt on completion	CUR_TXRX_OVER_INT_DIS When set, this bit will prevent the setting of the TX/RX interrupt bit of the IDMAC status register for data that ends in the buffer pointed to by this descriptor.
0	/	/

(3) DES1 Definition

Bits	Name	Descriptor
31:16	/	/
15:0	Buffer size	BUFF_SIZE These bits indicate the data buffer byte size, which must be a multiple of 4 bytes. If this filed is 0, the DMA ignores this buffer and proceeds to the next descriptor. **NOTE** **Only bit[12:0] is valid for SMHC2.**

(4) DES2 Definition

Bits	Name	Descriptor
31:0	Buffer address pointer	BUFF_ADDR These bits indicate the physical address of data buffer. The IDMAC ignores DES2[1:0], corresponding to the bus width of 32.

(5) DES3 Definition

Bits	Name	Descriptor
31:0	Next descriptor address	NEXT_DESP_ADDR These bits indicate the pointer to the physical memory where the next descriptor is present.

4.3.4. Programming Guidelines

4.3.4.1. Initialization

Before data and command are exchanged between a card and the SMHC, the SMHC need to be initialized .The SMHC is initialized as follows.

Step1: Configure GPIO register as SMHC function by Port Controller module; reset clock by writing 1 to the bit8 ~bit11 of Bus Software Reset Register 0, enable clock gating by writing 1 to the bit8~bit11 of Bus Clock Gating Register 0 ; select clock sources and set division factor by configuring the SMHCx_CLK_REG(x=0,1,2,3) register.

Step2: Configure SMHC_CTRL to enable total interrupt; configure SMHC_INTMASK to 0xFFCE to enable normal interrupt and error abnormal interrupt, and register interrupt function.

Step3: Configure SMHC_CLKDIV to open clock for device; configure SMHC_CMD as change clock command(for example 0x80202000); send update clock command to deliver clock to device.

Step4: Configure SMHC_CMDARG, configure SMHC_CMD to set response type,etc, then command can send. According to initial process in the protocol, you can finish SMHC initializing by sending corresponding command one by one.

4.3.4.2. Writing a Single Data Block

To Write a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write 0x82 to SMHC_IDMAC to enable IDMAC interrupt, configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 1 data block to the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD24(Single Data Block Write) to 0x1, write 0x80002758 to SMHC_CMD, send CMD24 command to write data to device.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD24 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234, first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

4.3.4.3. Reading a Single Data Block

To read a single data block, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 1 data block from the sector 1, then SMHC_BYCNT[BYTE_CNT] need be set to 0x200, the descriptor is set based on data size; set the data sector address of CMD17(Single Data Block Read) to 0x1, write 0x80002351 to SMHC_CMD , send CMD17 command to read data from device to DRAM/SRAM.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD17 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

4.3.4.4. Writing Open-ended Multiple Data Blocks(CMD25+Auto CMD12)

To write open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks to the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25(Multiple Data Blocks Write) to 0x0, write 0x80003759 to SMHC_CMD, send CMD25 command to write data to device, when data transfer is complete, CMD12 will be sent automatically .

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step7: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD, go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

4.3.4.5. Reading Open-ended Multiple Data Blocks(CMD18+Auto CMD12)

To read open-ended multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15, RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks from the sector 0, then SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80003352 to SMHC_CMD , send CMD18 command to read data to device, when data transfer is complete, CMD12 will be sent automatically.

Step4: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step5: Check whether SMHC_IDST_REG[RX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to

SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_RINTSTS[ACD] and SMHC_RINTSTS[DTC] are all 1. If yes, data transfer is complete, CMD12 transfer is complete and CMD18 reading operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

4.3.4.6. Writing Pre-defined Multiple Data Blocks(CMD23+CMD25)

To write pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If writing 3 data blocks, then set SMHC_CMDARG to 0x3 to ensure the block number to be operated, send CMD23 command by writing 0x80000157 to SMHC_CMD .Check whether SMHC_RINTSTS[CC] is 1.If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD25(Multiple Data Blocks Write) to 0x0, write 0x80002759 to SMHC_CMD, send CMD25 command to write data to device.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD25 writing operation is complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

Step8: Send CMD13 command to query whether device writing operation is complete and whether return to idle status. For example, device RCA is 0x1234,first set SMHC_CMDARG to 0x12340000, write 0x8000014D to SMHC_CMD,go to step4 to ensure command transfer completed, then check whether the highest bit of SMHC_RESP0(CMD13 response) is 1. If yes, device is in Idle status,then the next command can be sent. If no, device is in busy status, then continue to send CMD13 to wait device in the idle status until timeout exit.

4.3.4.7. Reading Pre-defined Multiple Data Blocks(CMD23+CMD18)

To read pre-defined multiple data blocks, perform the following steps:

Step1: Write 0x1 to SMHC_CTRL[DMA_RST] to reset internal DMA controller; write SMHC_IDMAC to 0x82 to enable IDMAC interrupt and configure AHB master burst transfers; configure SMHC_IDIE to enable transfer interrupt,receive interrupt, and abnormal interrupt.

Step2: Configure SMHC_FIFOTH to determine burst size, TX/RX trigger level. For example, if SMHC_FIFOTH is configured as 0x300F00F0, which indicates that Burst size is 16, TX_TL is 15,RX_TL is 240. Configure SMHC_DLBA to determine the start address of DMA descriptor.

Step3: If reading 3 data blocks, then set SMHC_CMDARG to 0x3 to ensure the block number to be operated, send CMD23 command by writing 0x80000157 to SMHC_CMD .Check whether SMHC_RINTSTS[CC] is 1.If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step4: SMHC_BYCNT[BYTE_CNT] need be set to 0x600, the descriptor is set based on data size; set the data sector address of CMD18(Multiple Data Blocks Read) to 0x0, write 0x80002352 to SMHC_CMD, send CMD18 command to read data from device to DRAM/SRAM.

Step5: Check whether SMHC_RINTSTS[CC] is 1. If yes, command sends successful; if no, continue to wait until timeout, then exit process.

Step6: Check whether SMHC_IDST_REG[TX_INT] is 1. If yes, writing DMA data transfer is complete, then write 0x337 to SMHC_IDST_REG to clear interrupt flag; if no, continue to wait until timeout, then exit process.

Step7: Check whether SMHC_RINTSTS[DTC] is 1. If yes, data transfer is complete and CMD18 writing operation is

complete. If no, that is, abnormity exists. Read SMHC_RINTSTS,SMHC_STATUS to query existing abnormity.

4.3.5. Register List

Module Name	Base Address
SMHC0	0x01C0F000
SMHC1	0x01C10000
SMHC2	0x01C11000
SMHC3	0x01C12000

Register Name	Offset	Description
SMHC_CTRL	0x0000	Control Register
SMHC_CLKDIV	0x0004	Clock Control Register
SMHC_TMOUT	0x0008	Time Out Register
SMHC_BUSWID	0x000C	Bus Width Register
SMHC_BLKSIZ	0x0010	Block Size Register
SMHC_BYTCNT	0x0014	Byte Count Register
SMHC_CMD	0x0018	Command Register
SMHC_CMDARG	0x001C	Command Argument Register
SMHC_RESP0	0x0020	Response 0 Register
SMHC_RESP1	0x0024	Response 1 Register
SMHC_RESP2	0x0028	Response 2 Register
SMHC_RESP3	0x002C	Response 3 Register
SMHC_INTMASK	0x0030	Interrupt Mask Register
SMHC_MINTSTS	0x0034	Masked Interrupt Status Register
SMHC_RINTSTS	0x0038	Raw Interrupt Status Register
SMHC_STATUS	0x003C	Status Register
SMHC_FIFOTH	0x0040	FIFO Water Level Register
SMHC_FUNS	0x0044	Function Select Register
SMHC_TCBCNT	0x0048	Transferred Byte Count between Controller and Card
SMHC_TBBCNT	0x004C	Transferred Byte Count between Host Memory and Internal FIFO
SMHC_CSDC	0x0054	CRC Status Detect Control Register
SMHC_A12A	0x0058	Auto Command 12 Argument Register
SMHC_NTSR	0x005C	SD New Timing Set Register
SMHC_SDBG	0x0060	SD New Timing Set Debug Register
SMHC_HWRST	0x0078	Hardware Reset Register
SMHC_DMAC	0x0080	DMA Control Register
SMHC_DLBA	0x0084	Descriptor List Base Address Register
SMHC_DST	0x0088	DMAC Status Register
SMHC_IDIE	0x008C	DMAC Interrupt Enable Register
SMHC_CHDA	0x0090	Current Host Descriptor Address Register
SMHC_CBDA	0x0094	Current Buffer Descriptor Address Register
SMHC_THLD	0x0100	Card Threshold Control Register
SMHC_EDSD	0x010C	eMMC4.5 DDR Start Bit Detection Control Register
SMHC_RES_CRC	0x0110	Response CRC from Device
SMHC_D7_CRC	0x0114	CRC in Data7 from Device
SMHC_D6_CRC	0x0118	CRC in Data6 from Device
SMHC_D5_CRC	0x011C	CRC in Data5 from Device
SMHC_D4_CRC	0x0120	CRC in Data4 from Device
SMHC_D3_CRC	0x0124	CRC in Data3 from Device
SMHC_D2_CRC	0x0128	CRC in Data2 from Device
SMHC_D1_CRC	0x012C	CRC in Data1 from Device

SMHC_D0_CRC	0x0130	CRC in Data0 from Device
SMHC_CRC_STA	0x0134	CRC Status from Device in Write Operation
SMHC_DRV_DL	0x0140	Drive Delay Control Register
SMHC_SMAP_DL	0x0144	Sample Delay Control Register
SMHC_DS_DL	0x0148	Data Strobe Delay Control Register
SMHC_FIFO	0x0200	Read/ Write FIFO

4.3.6. Register Description

4.3.6.1. SMHC Global Control Register(Default Value: 0x0000_0100)

Offset: 0x0000			**Register Name: SMHC_CTRL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	FIFO_AC_MOD FIFO Access Mode 0: DMA bus 1: AHB bus
30:13	/	/	/
12	R/W	0x0	TIME_UNIT_CMD Time unit for command line Time unit used to calculate command line time out value defined in RTO_LMT. 0: 1 card clock period 1: 256 card clock period
11	R/W	0x0	TIME_UNIT_DAT Time unit for data line Time unit used to calculate data line time out value defined in **DTO_LMT**. 0: 1 card clock period 1: 256 card clock period
10	R/W	0x0	DDR_MOD_SEL DDR Mode Select 0: SDR mode 1: DDR mode
9	/	/	/
8	R/W	0x1	CD_DBC_ENB Card Detect (Data[3] status) De-bounce Enable 0: Disable de-bounce 1: Enable de-bounce
7:6	/	/	/
5	R/W	0x0	DMA_ENB DMA Global Enable 0: Disable DMA to transfer data, using AHB bus 1: Enable DMA to transfer data
4	R/W	0x0	INT_ENB Global Interrupt Enable 0: Disable interrupts 1: Enable interrupts

Offset: 0x0000			Register Name: SMHC_CTRL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
3	/	/	/
2	R/W	0x0	DMA_RST DMA Reset
1	R/W	0x0	FIFO_RST FIFO Reset 0: No change 1: Reset FIFO This bit is auto-cleared after completion of reset operation.
0	R/W	0x0	SOFT_RST Software Reset 0: No change 1: Reset SD/MMC controller This bit is auto-cleared after completion of reset operation.

4.3.6.2. SMHC Clock Control Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SMHC_CLKDIV_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MASK_DATA0 0: Do not mask data0 when update clock 1: Mask data0 when update clock
30:18	/	/	/
17	R/W	0x0	CCLK_CTRL Card Clock Output Control 0: Card clock always on 1: Turn off card clock when FSM in IDLE state
16	R/W	0x0	CCLK_ENB Card Clock Enable 0: Card Clock off 1: Card Clock on
15:8	/	/	/
7:0	R/W	0x0	CCLK_DIV Card clock divider n: Source clock is divided by 2*n.(n=0~255)

4.3.6.3. SMHC Timeout Register(Default Value: 0xFFFF_FF40)

Offset: 0x0008			Register Name: SMHC_TMOUT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R/W	0xffffff	DTO_LMT Data Timeout Limit
7:0	R/W	0x40	RTO_LMT Response Timeout Limit

4.3.6.4. SMHC Bus Width Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: SMHC_BUSWID_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	CARD_WID Card width 00: 1-bit width 01: 4-bit width 1x: 8-bit width

4.3.6.5. SMHC Block Size Register(Default Value: 0x0000_0200)

Offset: 0x0010			Register Name: SMHC_BLKSIZ_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x200	BLK_SZ Block size

4.3.6.6. SMHC Byte Count Register(Default Value: 0x0000_0200)

Offset: 0x0014			Register Name: SMHC_BYTCNT_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x200	BYTE_CNT Byte counter Number of bytes to be transferred It should be integer multiple of Block Size for block transfers.

4.3.6.7. SMHC Command Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SMHC_CMD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CMD_LOAD Start Command. This bit is automatically cleared when current command is sent. If there is no any response error happened, a command complete interrupt bit (CMD_OVER) will be set in interrupt register. You should not write any other command before this bit is cleared, or a command busy interrupt bit (CMD_BUSY) will be set in interrupt register.
30:29	/	/	/
28	R/W	0x0	VOL_SW Voltage Switch 0: Normal command 1: Voltage switch command, set for CMD11 only
27	R/W	0x0	BOOT_ABT Boot Abort Setting this bit will terminate the boot operation.
26	R/W	0x0	EXP_BOOT_ACK Expect Boot Acknowledge.

Offset: 0x0018			Register Name: SMHC_CMD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			When Software sets this bit along in mandatory boot operation, controller expects a boot acknowledge start pattern of 0-1-0 from the selected card.
25:24	R/W	0x0	BOOT_MOD Boot Mode 00: Normal command 01: Mandatory Boot operation 10: Alternate Boot operation 11: Reserved
23:22	/	/	/
21	R/W	0x0	PRG_CLK Change Clock 0: Normal command 1: Change Card Clock; when this bit is set, controller will change clock domain and clock output. No command will be sent.
20:16	/	/	/
15	R/W	0x0	SEND_INIT_SEQ Send Initialization 0: Normal command sending 1: Send initialization sequence before sending this command.
14	R/W	0x0	STOP_ABT_CMD Stop Abort Command 0: Normal command sending 1: Send Stop or abort command to stop current data transfer in progress.(CMD12, CMD52 for writing “I/O Abort” in SDIO CCCR)
13	R/W	0x0	WAIT_PRE_OVER Wait Data Transfer Over 0: Send command at once, do not care of data transferring 1: Wait for data transfer completion before sending current command
12	R/W	0x0	STOP_CMD_FLAG Send Stop CMD Automatically (CMD12) 0: Do not send stop command at end of data transfer 1: Send stop command automatically at end of data transfer
11	R/W	0x0	TRANS_MODE Transfer Mode 0: Block data transfer command 1: Stream data transfer command
10	R/W	0x0	TRANS_DIR Transfer Direction 0: Read operation 1: Write operation
9	R/W	0x0	DATA_TRANS Data Transfer 0: Without data transfer 1: With data transfer
8	R/W	0x0	CHK_RESP_CRC

Offset: 0x0018			Register Name: SMHC_CMD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Check Response CRC 0: Do not check response CRC 1: Check response CRC
7	R/W	0x0	LONG_RESP Response Type 0: Short Response (48 bit) 1: Long Response (136 bit)
6	R/W	0x0	RESP_RCV Response Receive 0: Command without Response 1: Command with Response
5:0	R/W	0x0	CMD_IDX CMD Index Command index value

4.3.6.8. SMHC Command Argument Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SMHC_CMDARG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CMD_ARG Command argument

4.3.6.9. SMHC Response 0 Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SMHC_RESP0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP0 Response 0 Bit[31:0] of response

4.3.6.10. SMHC Response 1 Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: SMHC_RESP1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP1 Response 1 Bit[63:31] of response

4.3.6.11. SMHC Response 2 Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: SMHC_RESP2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP2 Response 2 Bit[95:64] of response

4.3.6.12. SMHC Response 3 Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: SMHC_RESP3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CMD_RESP3 Response 3 Bit[127:96] of response

4.3.6.13. SMHC Interrupt Mask Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SMHC_INTMASK_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CARD_REMOVAL_INT_EN Card Removed Interrupt Enable
30	R/W	0x0	CARD_INSERT_INT_EN Card Inserted Interrupt Enable
29:17	/	/	/
16	R/W	0x0	SDIO_INT_EN SDIO Interrupt Enable
15	R/W	0x0	DEE_INT_EN Data End-bit Error Interrupt Enable
14	R/W	0x0	ACD_INT_EN Auto Command Done Interrupt Enable
13	R/W	0x0	DSE_BC_INT_EN Data Start Error Interrupt Enable
12	R/W	0x0	CB_IW_INT_EN Command Busy and Illegal Write Interrupt Enable
11	R/W	0x0	FU_FO_INT_EN FIFO Underrun/Overflow Interrupt Enable
10	R/W	0x0	DSTO_VSD_INT_EN Data Starvation Timeout/V1.8 Switch Done Interrupt Enable
9	R/W	0x0	DTO_BDS_INT_EN Data Timeout/Boot Data Start Interrupt Enable
8	R/W	0x0	RTO_BACK_INT_EN Response Timeout/Boot ACK Received Interrupt Enable
7	R/W	0x0	DCE_INT_EN Data CRC Error Interrupt Enable
6	R/W	0x0	RCE_INT_EN Response CRC Error Interrupt Enable
5	R/W	0x0	DRR_INT_EN Data Receive Request Interrupt Enable
4	R/W	0x0	DTR_INT_EN Data Transmit Request Interrupt Enable
3	R/W	0x0	DTC_INT_EN Data Transfer Complete Interrupt Enable
2	R/W	0x0	CC_INT_EN Command Complete Interrupt Enable
1	R/W	0x0	RE_INT_EN Response Error Interrupt Enable
0	/	/	/

4.3.6.14. SMHC Masked Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SMHC_MINTSTS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	M_CARD_REMOVAL_INT Card Removed
30	R/W	0x0	M_CARD_INSERT Card Inserted
29:17	/	/	/
16	R/W	0x0	M_SDIO_INT SDIO Interrupt
15	R/W	0x0	M_DEE_INT Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken or received CRC status taken is negative.
14	R/W	0x0	M_ACD_INT Auto Command Done When set, it means auto stop command(CMD12) completed.
13	R/W	0x0	M_DSE_BC_INT Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared.
12	R/W	0x0	M_CB_IW_INT Command Busy and Illegal Write
11	R/W	0x0	M_FU_FO_INT FIFO Underrun/Overflow
10	R/W	0x0	M_DSTO_VSD_INT Data Starvation Timeout/V1.8 Switch Done
9	R/W	0x0	M_DTO_BDS_INT Data Timeout/Boot Data Start
8	R/W	0x0	M_RTO_BACK_INT Response Timeout/Boot ACK Received
7	R/W	0x0	M_DCE_INT Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative.
6	R/W	0x0	M_RCE_INT Response CRC Error
5	R/W	0x0	M_DRR_INT Data Receive Request When set, it means that there are enough data in FIFO during receiving data.
4	R/W	0x0	M_DTR_INT Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data.
3	R/W	0x0	M_DTC_INT Data Transfer Complete
2	R/W	0x0	M_CC_INT Command Complete
1	R/W	0x0	M_RE_INT

Offset: 0x0034			Register Name: SMHC_MINTSTS_REG
Bit	Read/Write	Default/Hex	Description
			Response Error (no response or response CRC error) When set, Transmit Bit error or End Bit error or CMD Index error may occur.
0	/	/	/

4.3.6.15. SMHC Raw Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SMHC_RINTSTS_REG
Bit	Read/Write	Default/Hex	Description
31	R/W1C	0x0	CARD_REMOVAL Card Removed This is write-1-to-clear bit.
30	R/W1C	0x0	CARD_INSERT Card Inserted This is write-1-to-clear bit.
29:17	/	/	/
16	R/W1C	0x0	SDIOI_INT SDIO Interrupt This is write-1-to-clear bit.
15	R/W1C	0x0	DEE Data End-bit Error When set during receiving data, it means that host controller does not receive valid data end bit. When set during transmitting data, it means that host controller does not receive CRC status taken. This is write-1-to-clear bit.
14	R/W1C	0x0	ACD Auto Command Done When set, it means auto stop command(CMD12) completed. This is write-1-to-clear bit.
13	R/W1C	0x0	DSE_BC Data Start Error When set during receiving data, it means that host controller found a error start bit. When set during transmitting data, it means that busy signal is cleared. This is write-1-to-clear bit.
12	R/W1C	0x0	CB_IW Command Busy and Illegal Write This is write-1-to-clear bit.
11	R/W1C	0x0	FU_FO FIFO Underrun/Overflow This is write-1-to-clear bit.
10	R/W1C	0x0	DSTO_VSD Data Starvation Timeout/V1.8 Switch Done This is write-1-to-clear bit.
9	R/W1C	0x0	DTO_BDS Data Timeout/Boot Data Start This is write-1-to-clear bit.
8	R/W1C	0x0	RTO_BACK Response Timeout/Boot ACK Received This is write-1-to-clear bit.
7	R/W1C	0x0	DCE

Offset: 0x0038			Register Name: SMHC_RINTSTS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Data CRC Error When set during receiving data, it means that the received data have data CRC error. When set during transmitting data, it means that the received CRC status taken is negative. This is write-1-to-clear bit.
6	R/W1C	0x0	RCE Response CRC Error This is write-1-to-clear bit.
5	R/W1C	0x0	DRR Data Receive Request When set, it means that there are enough data in FIFO during receiving data. This is write-1-to-clear bit.
4	R/W1C	0x0	DTR Data Transmit Request When set, it means that there is enough space in FIFO during transmitting data. This is write-1-to-clear bit.
3	R/W1C	0x0	DTC Data Transfer Complete This is write-1-to-clear bit.
2	R/W1C	0x0	CC Command Complete This is write-1-to-clear bit.
1	R/W1C	0x0	RE Response Error (no response or response CRC error) When set, Transmit Bit error or End Bit error or CMD Index error may occur. This is write-1-to-clear bit.
0	/	/	/

4.3.6.16. SMHC Status Register(Default Value: 0x0000_0006)

Offset: 0x003C			Register Name: SMHC_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	DMA_REQ DMA Request DMA request signal state
30:26	/	/	/
25:17	R	0x0	FIFO_LEVEL FIFO Level Number of filled locations in FIFO
16:11	R	0x0	RESP_IDX Response Index Index of previous response, including any auto-stop sent by controller
10	R	0x0	FSM_BUSY Data FSM Busy Data transmit or receive state-machine is busy
9	R	0x0	CARD_BUSY Card data busy Inverted version of DATA[0]

Offset: 0x003C			Register Name: SMHC_STATUS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Card data not busy 1: Card data busy
8	R	0x0	CARD_PRESENT Data[3] status level of DATA[3]; checks whether card is present 0: Card not present 1: Card present
7:4	R	0x0	FSM_STA Command FSM states 0000: Idle 0001: Send init sequence 0010: TX CMD start bit 0011: TX CMD TX bit 0100: TX CMD index + argument 0101: TX CMD CRC7 0110: TX CMD end bit 0111: RX response start bit 1000: RX response IRQ response 1001: RX response TX bit 1010: RX response CMD index 1011: RX response data 1100: RX response CRC7 1101: RX response end bit 1110: CMD path wait NCC 1111: Wait; CMD-to-response turnaround
3	R	0x0	FIFO_FULL FIFO full 0: FIFO not full 1: FIFO full
2	R	0x1	FIFO_EMPTY FIFO Empty 0: FIFO not empty 1: FIFO empty
1	R	0x1	FIFO_TX_LEVEL FIFO TX Water Level flag 0: FIFO didn’t reach transmit trigger level 1: FIFO reached transmit trigger level
0	R	0x0	FIFO_RX_LEVEL FIFO TX Water Level flag 0: FIFO didn’t reach receive trigger level 1: FIFO reached receive trigger level

4.3.6.17. SMHC FIFO Water Level Register(Default Value: 0x000F_0000)

Offset: 0x0040	Register Name: SMHC_FIFOTH_REG

Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x0	BSIZE_OF_TRANS Burst size of multiple transaction 000: 1 transfers 001: 4 010: 8 011: 16 (only SMHC2 support) Others: Reserved Should be programmed same as DMA controller multiple transaction size. The units for transfers are the DWORD. A single transfer would be signaled based on this value. Value should be sub-multiple of (RX_TL + 1) and (FIFO_DEPTH - TX_TL) Recommended: MSize = 16, TX_TL = 240, RX_TL = 15(SMHC2) MSize = 8, TX_TL = 248, RX_TL = 7(for SMHC0/1)
27:24	/	/	/
23:16	R/W	0xF	RX_TL RX Trigger Level 0x0~0xFE: RX Trigger Level is 0~254 0xFF reserved FIFO threshold when FIFO request host to receive data from FIFO. When FIFO data level is greater than this value, DMA request is raised if DMA enabled, or RX interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 15 (means greater than 15)(SMHC2)
15:8	/	/	/
7:0	R/W	0x0	TX_TL TX Trigger Level 0x1~0xFF: TX Trigger Level is 1~255 0x0: no trigger FIFO threshold when FIFO requests host to transmit data to FIFO. When FIFO data level is less than or equal to this value, DMA TX request is raised if DMA enabled, or TX request interrupt bit is set if interrupt enabled. At the end of packet, if the last transfer is less than this level, the value is ignored and relative request will be raised as usual. Recommended: 240(means less than or equal to 240)(SMHC2)

4.3.6.18. SMHC Function Select Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: SMHC_FUNS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	ABT_RDATA Abort Read Data 0: Ignored 1: After suspend command is issued during read-transfer, software polls

Offset: 0x0044			Register Name: SMHC_FUNS_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			card to find when suspend happened. Once suspend occurs, software sets the bit to reset data state-machine, which is waiting for next block of data. Used in SDIO card suspends sequence. This bit is auto-cleared once controller reset to idle state.
1	R/W	0x0	READ_WAIT Read Wait 0: Clear SDIO read wait 1: Assert SDIO read wait
0	R/W	0x0	HOST_SEND_MMC_IRQRESQ Host Send MMC IRQ Response 0: Ignored 1: Send auto IRQ response When host is waiting MMC card interrupt response, setting this bit will make controller cancel wait state and return to idle state, at which time, controller will receive IRQ response sent by itself. This bit is auto-cleared after response is sent.

4.3.6.19. SMHC Transferred Byte Count Register0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: SMHC_TBC_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC0 Transferred Count 0 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.3.6.20. SMHC Transferred Byte Count Register1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: SMHC_TBC_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	TBC1 Transferred Count 1 Number of bytes transferred between card and internal FIFO. The register should be accessed in full to avoid read-coherency problems and read only after data transfer completes.

4.3.6.21. SMHC CRC Status Detect Control Register(Default Value: 0x0000_0003)

Offset: 0x0054			Register Name: SMHC_CSDC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:0	R/W	0x3	CRC_DET_PARA 0110: HS400 speed mode 0011: Other speed mode

4.3.6.22. SMHC Auto Command 12 Argument Register(Default Value: 0x0000_FFFF)

Offset: 0x0058			Register Name: SMHC_A12A_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xffff	SD_A12A. SD_A12A set the argument of command 12 automatically send by controller

4.3.6.23. SMHC New Timing Set Register(Default Value: 0x8171_0000)

Offset: 0x005C			Register Name: SMHC_NTSR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	MODE_SELEC 0: Old mode of Sample/Output Timing 1: New mode of Sample/Output Timing
30:25	/	/	/
24	R/W	0x1	CMD_DAT_RX_PHASE_CLR During update clock , command and data rx phase clear 0: Disable 1: Enable
23	/	/	/
22	R/W	0x1	DAT_CRC_STATUS_RX_PHASE_CLR Before receive CRC status, data rx phase clear 0: Disable 1: Enable
21	R/W	0x1	DAT_TRANS_RX_PHASE_CLR Before transfer data , data rx phase clear 0: Disable 1: Enable
20	R/W	0x1	DAT_RECV_RX_PHASE_CLR Before receive data , data rx phase clear 0: Disable 1: Enable
19:17	/	/	/
16	R/W	0x1	CMD_SEND_RX_PHASE_CLR Before send command, command rx phase clear 0: Disable 1: Enable
15:10	/	/	/
9:8	R/W	0x0	DAT_SAMPLE_TIMING_PHASE(RX) 00: Sample timing phase offset 90° 01: Sample timing phase offset 180° 10: Sample timing phase offset 270° 11: Ignore
7:6	/	/	/
5:4	R/W	0x0	CMD_SAMPLE_TIMING_PHASE(RX)

Offset: 0x005C			Register Name: SMHC_NTSR_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			00: Sample timing phase offset 90° 01: Sample timing phase offset 180° 10: Sample timing phase offset 270° 11: Ignore
3:0	/	/	/

NOTE

This register is for SMHC0 ,SMHC1 ,SMHC3 only.

4.3.6.24. SMHC Hardware Reset Register(Default Value: 0x0000_0001)

Offset: 0x0078			Register Name: SMHC_HWRST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x1	HW_RST. 0: Reset 1: Active mode These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

4.3.6.25. SMHC DMAC Control Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: SMHC_DMAC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	W	0x0	DES_LOAD_CTRL When DMAC fetches a descriptor, if the valid bit of a descriptor is not set, DMAC FSM will go to the suspend state. Setting this bit will make DMAC re-fetch descriptor again and do the transfer normally.
30:11	/	/	/
10:8	R	0x0	PRG_BURST_LEN Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows. 000: 1 transfers 001: 4 transfers 010: 8 transfers 011: 16 transfers Transfer unit is 32bits. PBL is a read-only value.
7	R/W	0x0	IDMAC_ENB IDMAC Enable. When set, the IDMAC is enabled. DE is read/write.
6:2	R/W	0x0	DES_SKIP_LEN Descriptor Skip Length.

Offset: 0x0080			Register Name: SMHC_DMAC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			Specifies the number of Word to skip between two unchained descriptors. This is applicable only for dual buffer structure. Default value is set to 4 DWORD.
1	R/W	0x0	FIX_BUST_CTRL Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	R/W	0x0	IDMAC_RST DMA Reset. When set, the DMA Controller resets all its internal registers. SWR is read/write. It is automatically cleared after 1 clock cycle.

4.3.6.26. SMHC Descriptor List Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: SMHC_DLBA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DES_BASE_ADDR Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bit[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

4.3.6.27. SMHC DMAC Status Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: SMHC_DST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16:13	R	0x0	DMAC_FSM_STA DMAC FSM present state. 0000: DMA_IDLE 0001: DMA_SUSPEND 0010: DESC_RD 0011: DESC_CHK 0100: DMA_RD_REQ_WAIT 0101: DMA_WR_REQ_WAIT 0110: DMA_RD 0111: DMA_WR 1000: DESC_CLOSE This bit is read-only.
12:10	R	0x0	DMAC_ERR_STA Error Bits. Indicates the type of error that caused a Bus Error. Valid only with Fatal Bus Error bit (**FATAL_BERR_INT**) set. This field does not generate an interrupt. 001: Host Abort received during transmission 010: Host Abort received during reception Others: Reserved EB is read-only.

Offset: 0x0088			Register Name: SMHC_DST_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
9	R/W1C	0x0	ABN_INT_SUM Abnormal Interrupt Summary. Logical OR of the following: IDSTS[2]: Fatal Bus Interrupt IDSTS[4]: DU bit Interrupt IDSTS[5]: Card Error Summary Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit.
8	R/W1C	0x0	NOR_INT_SUM Normal Interrupt Summary. Logical OR of the following: IDSTS[0]: Transmit Interrupt IDSTS[1]: Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit.
7:6	/	/	/
5	R/W1C	0x0	ERR_FLAG_SUM Card Error Summary. Indicates the status of the transaction to/from the card; also present in RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot ACK Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit.
4	R/W1C	0x0	DES_UNAVL_INT Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	/	/	/
2	R/W1C	0x0	FATAL_BERR_INT Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (**DMAC_ERR_STA**). When this bit is set, the DMA disables all its bus accesses. Writing a '1' clears this bit.
1	R/W1C	0x0	RX_INT Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a '1' clears this bit.
0	R/W1C	0x0	TX_INT Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing a '1' clears this bit.

4.3.6.28. SMHC DMAC Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: SMHC_IDIE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	ABN_INT_ENB Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: IDINTEN[2]: Fatal Bus Error Interrupt IDINTEN[4]: DU Interrupt IDINTEN[5]: Card Error Summary Interrupt
8	R/W	0x0	NOR_INT_ENB Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: IDINTEN[0]: Transmit Interrupt IDINTEN[1]: Receive Interrupt
7:6	/	/	/
5	R/W	0x0	ERR_SUM_INT_ENB Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary.
4	R/W	0x0	DES_UNAVL_INT_ENB Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled.
3	/	/	/
2	R/W	0x0	FERR_INT_ENB Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled.
1	R/W	0x0	RX_INT_ENB Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled.
0	R/W	0x0	TX_INT_ENB Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled.

4.3.6.29. SMHC Current Host Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: SMHC_CHDA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_DES_ADDR Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC.

4.3.6.30. SMHC Current Buffer Descriptor Address Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: SMHC_CBDA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CUR_BUFF_ADDR Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC.

4.3.6.31. SMHC Card Threshold Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SMHC_THLD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	CARD_RD_THLD Card Read Threshold Size
15:3	/	/	/
2	R/W	0x0	CARD_WR_THLD_ENB (only for SMHC2) Card Write Threshold Enable(HS400) 0: Card Write Threshold Disable 1: Card Write Threshold Enabled Host controller initiates write transfer only if card threshold amount of data is available in transmit FIFO
1	R/W	0x0	BCIG (only for SMHC2) Busy Clear Interrupt Generation 0: Busy Clear Interrupt Disabled 1: Busy Clear Interrupt Enabled The application can disable this feature if it does not want to wait for a Busy Clear Interrupt.
0	R/W	0x0	CARD_RD_THLD_ENB Card Read Threshold Enable 0: Card Read Threshold Disable 1: Card Read Threshold Enable Host controller initiates Read Transfer only if **CARD_RD_THLD** amount of space is available in receive FIFO

4.3.6.32. SMHC eMMC4.5 DDR Start Bit Detection Control Register(Default Value: 0x0000_0000)

Offset: 0x010C			Register Name: SMHC_EDSD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable It is required to set **HS400_MD_EN** to '1' before initiating any data transfer CMD in HS400 mode.
30:1	/	/	/
0	R/W	0x0	HALF_START_BIT

Offset: 0x010C			Register Name: SMHC_EDSD_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	HS400_MD_EN(for SMHC2 only) HS400 Mode Enable 0: Disable 1: Enable It is required to set **HS400_MD_EN** to '1' before initiating any data transfer CMD in HS400 mode.
			Control for start bit detection mechanism inside mstorage based on duration of start bit. For eMMC 4.5, start bit can be: 0: Full cycle 1: Less than one full cycle Set **HALF_START_BIT** to 1 for eMMC 4.5 and above; set to 0 for SD applications.

4.3.6.33. SMHC Response CRC Register(Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: SMHC_RESP_CRC_REG
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0x0	RESP_CRC Response CRC Response CRC from device.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.34. SMHC Data7 CRC Register(Default Value: 0x0000_0000)

Offset: 0x0114			Register Name: SMHC_DATA7_CRC_REG
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	DAT7_CRC Data[7] CRC CRC in data[7] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.35. SMHC Data6 CRC Register(Default Value: 0x0000_0000)

Offset: 0x0118			Register Name: SMHC_DATA6_CRC_REG
Bit	Read/Write	Default/Hex	Description

31:0	R	0x0	DAT6_CRC Data[6] CRC CRC in data[6] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.36. SMHC Data5 CRC Register(Default Value: 0x0000_0000)

Offset: 0x011C			Register Name: SMHC_DATA5_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT5_CRC Data[5] CRC CRC in data[5] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.37. SMHC Data4 CRC Register(Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: SMHC_DATA4_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT4_CRC Data[4] CRC CRC in data[4] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.38. SMHC Data3 CRC Register(Default Value: 0x0000_0000)

Offset: 0x0124			Register Name: SMHC_DATA3_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R	0x0	DAT3_CRC Data[3] CRC CRC in data[3] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.39. SMHC Data2 CRC Register(Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: SMHC_DATA2_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT2_CRC Data[2] CRC CRC in data[2] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.40. SMHC Data1 CRC Register(Default Value: 0x0000_0000)

Offset: 0x012C			Register Name: SMHC_DATA1_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	DAT1_CRC Data[1] CRC CRC in data[1] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.41. SMHC Data0 CRC Register(Default Value: 0x0000_0000)

Offset: 0x0130			Register Name: SMHC_DATA0_CRC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:0	R	0x0	DAT0_CRC Data[0] CRC CRC in data[0] from device. In 8-bit DDR mode, the higher 16-bit indicates the CRC of even data, and the lower 16-bit indicates the CRC of odd data. In 4-bit DDR mode, it is not used. In SDR mode, the higher 16-bit indicates the CRC of all data.

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.42. SMHC CRC Status Register(Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: SMHC_CRC_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	CRC_STA CRC Status CRC status from device in write operation 010: Positive CRC status token 101: Negative CRC status token

NOTE

This register is for SMHC0,SMHC1,SMHC3 only.

4.3.6.43. SMHC Drive Delay Control Register(Default Value: 0x0001_0000)

Offset: 0x0140			Register Name: SMHC_DRV_DL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17	R/W	0x0	DAT_DRV_PH_SEL Data Drive Phase Select 0: Data drive phase offset is 90 ° at SDR mode, 45 ° at DDR mode, 90 ° at HS400 mode. 1: Data drive phase offset is 180 ° at SDR mode, 90 ° at DDR mode, 0 ° at HS400 mode.
16	R/W	0x1	CMD_DRV_PH_SEL Command Drive Phase Select 0: Command drive phase offset is 90 ° at SDR mode, 45 ° at DDR mode, 90 ° at HS400 mode. 1: Command drive phase offset is 180 ° at SDR mode, 90 ° at DDR mode, 180 ° at HS400 mode.
15:0	/	/	/

4.3.6.44. SMHC Sample Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0144			Register Name: SMHC_SAMP_DL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31:16	/	/	/
15	R/W	0x0	SAMP_DL_CAL_START Sample Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	SAMP_DL_CAL_DONE Sample Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in **SAMP_DL**.
13:8	R	0x20	SAMP_DL Sample Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of card clock nearly. Generally, it is necessary to do drive delay calibration when card clock is changed. This bit is valid only when **SAMP_DL_CAL_DONE** is set.
7	RW	0x0	SAMP_DL_SW_EN Sample Delay Software Enable When set, enable sample delay specified at **SAMP_DL_SW**.
6	/	/	/
5:0	RW	0x0	SAMP_DL_SW Sample Delay Software The relative delay between clock line and command line, data lines. It can be determined according to the value of **SAMP_DL**, the cycle of card clock and device's input timing requirement.

4.3.6.45. SMHC Data Strobe Delay Control Register(Default Value: 0x0000_2000)

Offset: 0x0148			**Register Name: SMHC_DS_DL_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	RW	0x0	DS_DL_CAL_START Data Strobe Delay Calibration Start When set, start sample delay chain calibration.
14	R	0x0	DS_DL_CAL_DONE Data Strobe Delay Calibration Done When set, it means that sample delay chain calibration is done and the result of calibration is shown in **DS_DL**.
13:8	R	0x20	DS_DL Data Strobe Delay It indicates the number of delay cells corresponding to current card clock. The delay time generated by these delay cells is equal to the cycle of SMHC's clock nearly. This bit is valid only when **SAMP_DL_CAL_DONE** is set.
7	RW	0x0	DS_DL_SW_EN Sample Delay Software Enable
6	/	/	/
5:0	RW	0x0	DS_DL_SW Data Strobe Delay Software

NOTE

This register is for SMHC2 only.

4.3.6.46. SMHC FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SMHC_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX/RX_FIFO Data FIFO

Chapter 5. Graphic

This chapter mainly details the mixer processor in A40i.

5.1. Mixer Processor

5.1.1. Overview

The mixer processor (MP) is a hardware accelerator for 2D graphic. It includes Format Transform,Rotate,Scaler,ROP, Alpha and Color Key function.

Features:

- Supports output size up to 2048 x 2048
- Supports memory scan order option
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate
- Supports input formats: ARG8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565/YUV422/YUV420/YUV411 UV combine
- Supports output formats: ARGB8888/XRGB8888/RGB888/ ARGB4444/ARGB1555/RGB565/YUV422/YUV420/YUV411 UV combine and planer
- Supports any format convert function device
- Supports 4 x 4 taps 32 phase bilinear scaler
- Supports pixel/plane and multiply alpha
- Supports source over and destination over blending and color key operation
- Supports FillRectangle BitBlit and StretchBlit

5.1.2. Block Diagram

Figure 5-1 shows a block diagram of MP.

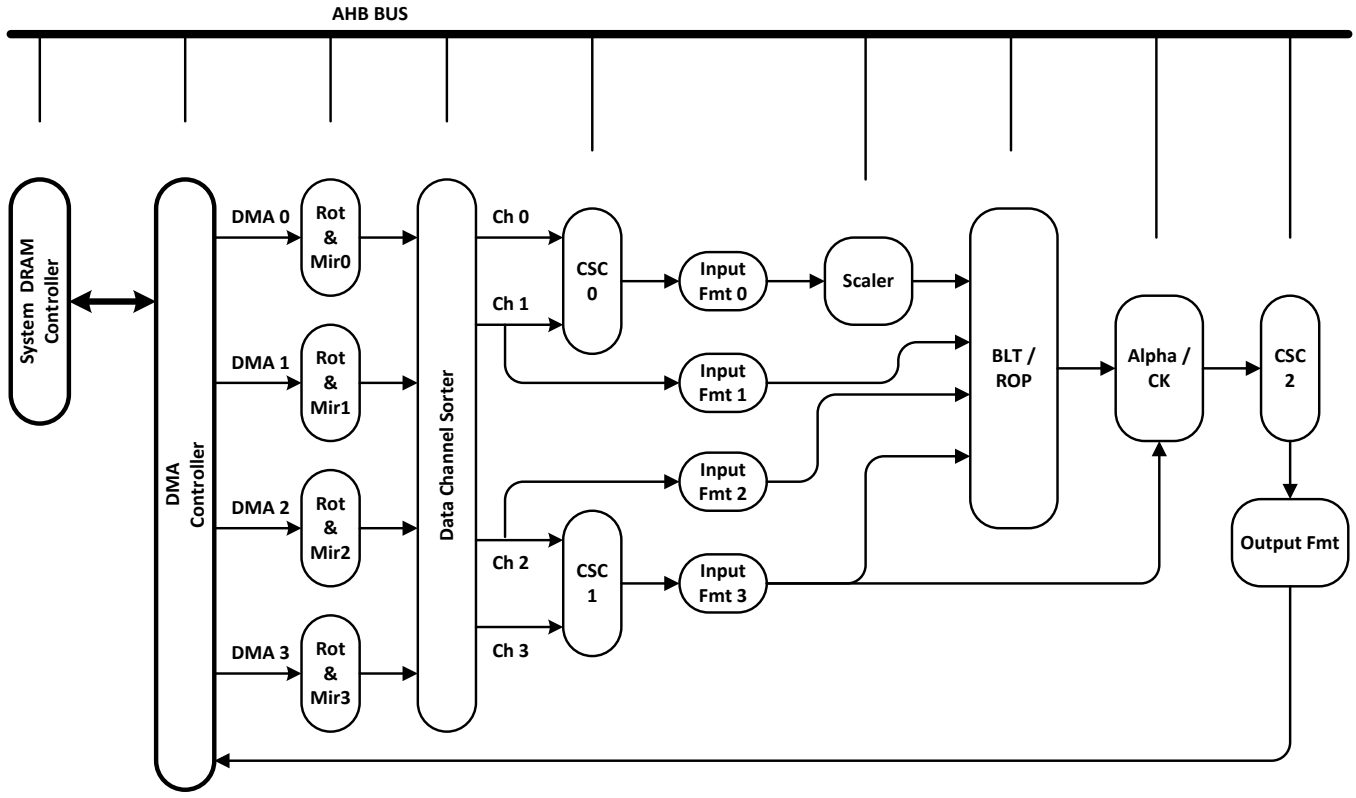


Figure 5-1. MP Block Diagram

5.1.3. Clock Sources

MP gets two different clocks,users can select one of them to make MP Clock Source.The following table describes the clock sources for MP.Users can see **CCU** in chapter3 for clock setting,configuration and gating information.

Table 5-1. MP Clock Sources

Clock Sources	Description
PLL_DE	PLL_DE,default value is 200MHz for MP.
PLL_PERIPH0(2x)	Peripheral Clock0 source, divide to about 200MHz for MP.

5.1.4. Register List

Module name	Base address
MP	0x01E80000

Register name	Offset	Description
MP_CTL	0x0000	Mixer Control Register
MP_STATUS	0x0004	Mixer Status Register
MP_DMA_ORDER	0x0008	Mixer Input DMA Scan Order Register

Register name	Offset	Description
MP_IDMA_HADDR	0x000C	Mixer Input DMA High 4 bits Address Register
MP_IDMA_LADDR	0x0010+N*0x04 (N=0~3)	Mixer Input DMA Low 32 bits Address Register
MP_IDMA_PITCH	0x0020+N*0x04 (N=0~3)	Mixer Input DMA Pitch Register
MP_IDMA_SIZE	0x0030+N*0x04 (N=0~3)	Mixer Input DMA Memory Block Size Register
MP_IDMA_COOR	0x0040+N*0x04 (N=0~3)	Mixer Input DMA Memory Block Coordinate Register
MP_IDMA_SETTING	0x0050+N*0x04 (N=0~3)	Mixer Input DMA Setting Register
MP_IDMA_FILLCOLOR	0x0060+N*0x04 (N=0~3)	Mixer Input DMA Fillcolor Register
/	0x0070	/
MP_CSC0_CTL	0x0074	Mixer Color Space Converter0 Register
MP_CSC1_CTL	0x0078	Mixer Color Space Converter1 Register
/	0x007C	/
MP_SCALER_CTL	0x0080	Mixer Scaling Control Register
MP_SCALER_OSIZE	0x0084	Mixer Scaling Output Size Register
MP_SCALER_HFACTOR	0x0088	Mixer Scaling Horizontal Factor Register
MP_SCALER_VFACTOR	0x008C	Mixer Scaling Vertical Factor Register
MP_SCALER_HPHASE	0x0090	Mixer Scaling Horizontal Start Phase Register
MP_SCALER_VPHASE	0x0094	Mixer Scaling Vertical Start Phase Register
/	0x0098~0x00AC	/
MP_ROP_CTL	0x00B0	Mixer ROP Control Register
/	0x00B4	/
MP_ROP_INDEX0	0x00B8	Mixer ROP Channel3 Index0 Setting Register
MP_ROP_INDEX1	0x00BC	Mixer ROP Channel3 Index1 Setting Register
MP_CK_CTL	0x00C0	Mixer Alpha Color Key Control Register
MP_CK_MIN	0x00C4	Mixer Color Key Min Color Register
MP_CK_MAX	0x00C8	Mixer Color Key Max Color Register
/	0x00CC	/
MP_CSC2_CTL	0x00D0	Mixer Color Space Converter2 Register
/	0x00D4~0x00DC	/
MP_OUTPUT_CTL	0x00E0	Mixer Output Control Register
/	0x00E4	/
MP_OUTPUT_SIZE	0x00E8	Mixer Output Size Register
MP_OUTPUT_HADDR	0x00EC	Mixer Output High 4 bits Address Register
MP_OUTPUT_LADDR	0x00F0+N*0x04 (N=0~2)	Mixer Output Low 32 bits Address Register
/	0x00FC	/
MP_OUTPUT_PITCH	0x0100+N*0x04 (N=0~2)	Mixer Output Pitch Register
/	0x010C~0x011C	/
MP_OUTPUT_ALPHA	0x0120	Mixer Output Alpha Control Register
/	0x0124~0x017C	/
MP_ICSC0_YGCOEF	0x0180	Mixer CSC0/1 Y/G Coefficient Register
MP_ICSC1_YGCOEF	0x0184	Mixer CSC0/1 Y/G Coefficient Register
MP_ICSC2_YGCOEF	0x0188	Mixer CSC0/1 Y/G Coefficient Register
MP_ICSC_YGCONS	0x018C	Mixer CSC0/1 Y/G Constant Register
MP_ICSC0_YGCOEF	0x0190	Mixer CSC0/1 U/R Coefficient0 Register
MP_ICSC1_YGCOEF	0x0194	Mixer CSC0/1 U/R Coefficient1 Register
MP_ICSC2_YGCOEF	0x0198	Mixer CSC0/1 U/R Coefficient2 Register
MP_ICSC_URCONS	0x019C	Mixer CSC0/1 U/R Constant Register

Register name	Offset	Description
MP_ICSC0_URCOEF	0x01A0	Mixer CSC0/1 V/B Coefficient0 Register
MP_ICSC1_URCOEF	0x01A4	Mixer CSC0/1 V/B Coefficient1 Register
MP_ICSC2_URCOEF	0x01A8	Mixer CSC0/1 V/B Coefficient2 Register
MP_ICSC_VBCONS	0x01AC	Mixer CSC0/1 V/B Constant Register
/	0x01B0~0x01BC	/
MP_ICSC_VBCOEF	0x01C0+N*0x04 (N=0~2)	Mixer CSC2 Y/G Coefficient Register
MP_OCSC_YGCONS	0x01CC	Mixer CSC2 Y/G Constant Register
MP_OCSC_YGCOEF	0x01D0+N*0x04 (N=0~2)	Mixer CSC2 U/R Coefficient Register
MP_OCSC_URCONS	0x01DC	Mixer CSC2 U/R Constant Register
MP_OCSC_URCOEF	0x01E0+N*0x04 (N=0~2)	Mixer CSC2 V/B Coefficient Register
MP_OCSC_VBCONS	0x01EC	Mixer CSC2 V/B Constant Register
/	0x01F0~0x01FC	/
MP_SCALER_HCOEFF	0x0200~0x027C	Mixer Scaling Horizontal Filtering Coefficient RAM
MP_SCALER_VCOEFF	0x0280~0x02FC	Mixer Scaling Vertical Filtering Coefficient RAM
/	0x0300~0x03FC	/
MP_PALETTE_TAB	0x0400~0x07FC	Mixer Palette Table RAM

5.1.5. Register Description

5.1.5.1. Mixer Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: MP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	HWERRIRQ_EN Hardware error IRQ enable control 0:Disable 1:Enable
8	R/W	0x0	FINISHIRQ_EN Mission finish IRQ enable control 0:Disable 1:Enable
7:2	/	/	/
1	R/W	0x0	START_CTL Start control If the bit is set, the module will start 1 frame operation and stop automatically.
0	R/W	0x0	MP_EN Enable control 0:Disable 1:Enable

5.1.5.2. Mixer Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: MP_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0004			Register Name: MP_STATUS
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13	R	0x0	HWERR_FLAG Hardware error status
12	R	0x0	BUSY_FLAG Module working status 0:Idle 1:Running
11:10	/	/	/
9	R/W	0x0	HWERRIRQ_FLAG Hardware error IRQ It will be set when hardware error occurs, and cleared by writing 1.
8	R/W	0x0	FINISHIRQ_FLAG Mission finish IRQ It will be set when 1 frame operation accomplished, and cleared by writing 1.
7:0	/	/	/

5.1.5.3. Mixer Input DMA Scan Order Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: MP_DMA_ORDER
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9:8	R/W	0x0	MEMSCANORDER Memory scan order selection 00: Top to down, Left to right 01: Top to down, Right to left 10: Down to top, Left to right 11: Down to top, Right to left **NOTE** **Four input DMA channel use the same scan rule.** **The each output DMA channel should match the same memory scan order rule with the input DMA channel.**
7:0	/	/	/

5.1.5.4. Mixer Input DMA High 4bit Address Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: MP_IDMA_HADDR
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0x0	IDMA3_H4ADDR High 4bit address in bit
23:20	/	/	/
19:16	R/W	0x0	IDMA2_H4ADDR High 4bit address in bit
15:12	/	/	/
11:8	R/W	0x0	IDMA1_H4A High 4bit address in bit

Offset: 0x000C			Register Name: MP_IDMA_HADDR
Bit	Read/Write	Default/Hex	Description
7:4	/	/	/
3:0	R/W	0x0	IDMA0_H4ADDR High 4bit address in bit

5.1.5.5. Mixer Input DMA Low 32bit Address Register(Default Value: 0x0000_0000)

Offset: 0x0010 + N*0x04(N= 0~3)			Register Name: MP_IDMA_LADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	IDMA_L32ADDR Low 32bit address in bit

5.1.5.6. Mixer Input DMA Pitch Register(Default Value: 0x0000_0000)

Offset: 0x0020 + N*0x04(N= 0~3)			Register Name: MP_IDMA_PITCH
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	IDMA_PITCH Pitch in bit

5.1.5.7. Mixer Input DMA Memory Block Size Register(Default Value: 0x0000_0000)

Offset: 0x0030 + N*0x04(N= 0~3)			Register Name: MP_IDMA_SIZE
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	IDMA_HEIGHT Memory block height in pixels The height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IDMA_WIDTH Memory block width in pixels The width = The value of these bits add 1

5.1.5.8. Mixer Input DMA Memory Block Coordinate Register(Default Value: 0x0000_0000)

Offset: 0x0040 + N*0x04(N= 0~3)			Register Name: MP_IDMA_COOR
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	IDMA_YCOOR Y coordinate Y is the left-top y coordinate of layer on output window in pixels The Y represent the two's complement
15:0	R/W	0x0	IDMA_XCOOR X coordinate X is left-top x coordinate of the layer on output window in pixels The X represent the two's complement

5.1.5.9. Mixer Input DMA Setting Register(Default Value: 0x0000_0000)

Offset: 0x0050 + N*0x04(N= 0~3)			Register Name: MP_IDMA_SETTING
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	Globe alpha value
23:16	/	/	/
15:12	R/W	0x0	Input data pixel sequence Reference input pixel sequence table
11:8	R/W	0x0	Input data format 0000:32bpp – A8R8G8B8 or interleaved AYUV8888 0001:16bpp – A4R4G4B4 0010:16bpp – A1R5G5B5 0011:16bpp – R5G6B5 0100:16bpp – interleaved YUV422 0101:16bpp – U8V8 0110:8bpp – Y8 0111:8bpp – MONO or palette 1000:4bpp – MONO or palette 1001:2bpp – MONO or palette 1010:1bpp – MONO or palette Other: reserved **NOTE** **If the input data format is 16 or 32bpp, and the work mode is palette mode, only the low 8 bits input data is valid.**
7:4	R/W	0x0	Rotation and mirroring control 0000:normal 0001:X 0010:Y 0011:XY 0100:A 0101:AX 0110:AY 0111:AXY Other: reserved
3:2	R/W	0x0	Alpha control 0:Ignore Output alpha value = pixels alpha, if no pixel alpha, the alpha value equal 0xff 01:Globe alpha enable Ignore pixel alpha value Output alpha value = globe alpha value 10: Globe alpha mix pixel alpha Output alpha value = globe alpha value * pixels alpha value 11:Reserved **NOTE** **The output alpha value here means the input alpha value of the ALU following the DMA controller.**
1	R/W	0x0	Work mode selection 0: normal mode (non-palette mode)

Offset: 0x0050 + N*0x04(N= 0~3)			Register Name: MP_IDMA_SETTING
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: palette mode
0	R/W	0x0	Input DMA enable control 0:disable input DMA channel, the respective fill-color value will stead of the input data. 1:enable

5.1.5.10. Mixer Input DMA Fill-color Register(Default Value: 0x0000_0000)

Offset: 0x0060 + N*0x4 (N= 0~3)			Register Name: MP_IDMA_FILLCOLOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	IDMA_FCALPHA Alpha
23:16	R/W	0x0	IDMA_FCRED Red
15:8	R/W	0x0	IDMA_FCGREEN Green
7:0	R/W	0x0	IDMA_FCBLUE Blue

5.1.5.11. Mixer Color Space Converter 0 Register(Default Value: 0x0000_0000)

Offset: 0x0074			Register Name: MP_IDMA_CSC0_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	CSC0_DATAMOD Data mode control 0000: Interleaved AYUV8888 mode 0001: Interleaved YUV422 mode In mode 0 and mode 1, only the channel 0 data path is valid for this module, the channel 1 data flow will by-pass the csc0 module, and direct to input formatter 1. 0010: Planar YUV422 mode (UV combined only) 0011: Planar YUV420 mode (UV combined only) 0100: Planar YUV411 mode (UV combined only) In mode 2/3/4, following rule: In this mode, the output data of the input formatter 1 will be stead of the respective fill-color value.
3:1	/	/	/
0	R/W	0x0	CSC0_EN Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

5.1.5.12. Mixer Color Space Converter 1 Register(Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: MP_IDMA_CSC1_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:4	R/W	0x0	CSC1_DATAMOD Data mode control 0000: Interleaved AYUV8888 mode 0001: Interleaved YUV422 mode In mode 0 and mode 1, only the channel 3 data path is valid for this module, the channel 2 data flow will by-pass the csc1 module, and direct to input formatter 2. 0010: Planar YUV422 mode (UV combined only) 0011: Planar YUV420 mode (UV combined only) 0100: Planar YUV411 mode (UV combined only) In mode 2/3/4, following rule: In this mode, the output data of the input formatter 2 will be stead of the respective fill-color value.
3:1	/	/	/
0	R/W	0x0	CSC1_EN Enable control 0: Disable color space function, ignore the control setting, and the data flow will by-pass the module. 1: Enable color space converting function.

5.1.5.13. Mixer Scaling Control Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: MP_SCALER_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x0	SCA_ALGSEL Scaling algorithm selection 00: bi-cubic(4 taps in vertical and horizontal) 01: linear in vertical and bi-linear in horizontal(2 taps in vertical and 4 taps in horizontal) 10: extractive in vertical and bi-linear in horizontal(1 tap in vertical and 4 taps in horizontal) 11: Reserved
3:1	/	/	/
0	R/W	0x0	SCA_EN Enable control 0: Disable scaler, ignore the whole scaling setting, and the data flow will by-pass the module. 1: Enable scaling function

5.1.5.14. Mixer Scaling Output Size Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: MP_SCALER_OUTSIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SCA_OUTHEIGHT Output height The output height = The value of these bits add 1 The minimum output height is 8 pixels.
15:13	/	/	/
12:0	R/W	0x0	SCA_OUTWIDTH Output width The output width = The value of these bits add 1 The minimum output width is 16 pixels.

5.1.5.15. Mixer Scaling Horizontal Factor Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: MP_SCALER_HFACTOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	HFACTOR0 The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	HFACTOR1 The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width The input width is the memory block width of respective iDMA channel.

5.1.5.16. Mixer Scaling Vertical Factor Register(Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: MP_SCALER_VFACTOR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	VFACTOR0 The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	VFACTOR1 The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height The input height is the memory block height of respective iDMA channel.

5.1.5.17. Mixer Scaling Horizontal Start Phase Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: MP_SCALER_HPHASE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	HPHASE Start phase in horizontal (complement) This value equals to start phase * 2^{16}

5.1.5.18. Mixer Scaling Vertical Start Phase Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: MP_SCALER_VPHASE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:0	R/W	0x0	SCA_VERPHASE Start phase in vertical (complement) This value equals to start phase * 2^{16}

5.1.5.19. Mixer ROP Control Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: MP_ROP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:14	R/W	0x0	ROP_ALPHABYPASSSEL ROP output Alpha channel selection 00: Channel 0 01: Channel 1 10: Channel 2 11: Reserved The bit is only valid in by-pass mode of Alpha channel
13:12	R/W	0x0	ROP_REDBYPASSSEL ROP output Red channel selection 00: Channel 0 01: Channel 1 10: Channel 2 11: Reserved The bit is only valid in by-pass mode of Red channel
11:10	R/W	0x0	ROP_GREENBYPASSSEL ROP output Green channel selection 00: Channel 0 01: Channel 1 10: Channel 2 11: Reserved The bit is only valid in by-pass mode of Green channel
9:8	R/W	0x0	ROP_BLUEBYPASSSEL ROP output Blue channel selection 00: Channel 0 01: Channel 1 10: Channel 2 11: Reserved The bit is only valid in by-pass mode of Blue channel
7	R/W	0x0	ROP_ALPHABYPASSEN ROP Alpha channel by-pass enable control 0: Pass through 1: By-pass
6	R/W	0x0	ROP_REDBYPASSEN ROP Red channel by-pass enable control 0: Pass through

Offset: 0x00B0			Register Name: MP_ROP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: By-pass
5	R/W	0x0	ROP_GREENBYPASSEN ROP Green channel by-pass enable control 0: Pass through 1: By-pass
4	R/W	0x0	ROP_BLUEBYPASSEN ROP Blue channel by-pass enable control 0: Pass through 1: By-pass
3:1	/	/	/
0	R/W	0x0	ROP_MOD ROP type selection 0: ROP3 1: ROP4 In ROP3 mode, only the value of channel 3 index 0 control table setting register will be selected. In ROP3 mode, the channel 3 data will by-pass the ROP module. In ROP3 mode, the channel 3 data will direct to Alpha/CK module. In ROP4 mode, the respective input DMA channel fill color of channel 3 will transfer to Alpha/CK module.

5.1.5.20. Mixer ROP Channel 3 Index 0 Setting Register(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: MP_ROP_INDEX0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	NOD7_CTL Index 0 node7 setting (channel 0’ and channel 1’ and channel 2’ mix not logic) 0: By-pass 1: Not
14:11	R/W	0x0	NOD6_CTL Index 0 node6 setting (channel 0’ and channel 1’ and channel 2’ mix logic) 0000: And 0001: OR 0010: XOR 0011: Add in byte 0100: Add in word (32bit) 0101: Multiply in byte 0110: Multiply in word (32bit) 0111: Channel 0’ mix channel 1’ then sub channel 2’ in byte 1000: Channel 0’ mix channel 1’ then sub channel 2’ in word (32bit) Other: Reserved
10	R/W	0x0	NOD5_CTL Index 0 node5 setting (channel 0’ and channel 1’ mix not logic)

Offset: 0x00B8			Register Name: MP_ROP_INDEX0
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: By-pass 1: Not
9:6	R/W	0x0	NOD4_CTL Index 0 node4 setting (channel 0’ and channel 1’ mix logic) 0000: And 0001: OR 0010: XOR 0011: Add in byte 0100: Add in word (32bit) 0101: Multiply in byte 0110: Multiply in word (32bit) 0111: Channel 0’ sub channel 1’ in byte 1000: Channel 0’ sub channel 1’ in word (32bit) Other: Reserved
5	R/W	0x0	NOD3_CTL Index 0 node3 setting (channel 2’ not logic) 0: By-pass 1: Not
4	R/W	0x0	NOD2_CTL Index 0 node2 setting (channel 1’ not logic) 0: By-pass 1: Not
3	R/W	0x0	NOD1_CTL Index 0 node1 setting (channel 0’ not logic) 0: By-pass 1: Not
2:0	R/W	0x0	NOD0_CTL Index 0 node0 setting (sorting control) 000: 012 001: 021 010: 102 011: 120 100: 201 101: 210 Other: Reserved

NOTE

The result of add or multiply operation will select the high 8-bit (byte operation) or 32-bit (word operation).

5.1.5.21. Mixer ROP Channel 3 Index 1 Setting Register(Default Value: 0x0000_0000)

Offset: 0x00BC			Register Name: MP_ROP_INDEX1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	NOD7_CTL Index 1 node7 setting (channel 0’ and channel 1’ and channel 2’ mix not logic)

Offset: 0x00BC			Register Name: MP_ROP_INDEX1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: By-pass 1: Not
14:11	R/W	0x0	NOD6_CTL Index 1 node6 setting (channel 0’ and channel 1’ and channel 2’ mix logic) 0000: And 0001: OR 0010: XOR 0011: Add in byte 0100: Add in word (32bit) 0101: Multiply in byte 0110: Multiply in word (32bit) 0111: Channel 0’ mix channel 1’ then sub channel 2’ in byte 1000: Channel 0’ mix channel 1’ then sub channel 2’ in word (32bit) Other: Reserved
10	R/W	0x0	NOD5_CTL Index 1 node5 setting (channel 0’ and channel 1’ mix not logic) 0: By-pass 1: Not
9:6	R/W	0x0	NOD4_CTL Index 1 node4 setting (channel 0’ and channel 1’ mix logic) 0000: And 0001: OR 0010: XOR 0011: Add in byte 0100: Add in word (32bit) 0101: Multiply in byte 0110: Multiply in word (32bit) 0111: Channel 0’ sub channel 1’ in byte 1000: Channel 0’ sub channel 1’ in word (32bit) Other: Reserved
5	R/W	0x0	NOD3_CTL Index 1 node3 setting (channel 2’ not logic) 0: By-pass 1: Not
4	R/W	0x0	NOD2_CTL Index 1 node2 setting (channel 1’ not logic) 0: By-pass 1: Not
3	R/W	0x0	NOD1_CTL Index 1 node1 setting (channel 0’ not logic) 0: By-pass 1: Not
2:0	R/W	0x0	NOD0_CTL Index 1 node0 setting (sorting control) 000: 012

Offset: 0x00BC			Register Name: MP_ROP_INDEX1
Bit	Read/Write	Default/Hex	Description
			001: 021 010: 102 011: 120 100: 201 101: 210 Other: Reserved

NOTE

The result of add or multiply operation will select the high 8-bit (byte operation) or 32-bit (word operation).

5.1.5.22. Mixer Alpha Color Key Control Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: MP_CK_CTL
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	CK_REDCON Red control condition 0: If (R value of ck min color) <= (R value of layer0) <= (R value of ck max color), The red control condition is true, else the condition is false. 1: If (R value of ck min color) > (R value of layer0) or (R value of layer0) > (R value of ck max color), The red control condition is true, else the condition is false.
9	R/W	0x0	CK_GREENCON Green control condition 0: If (G value of ck min color) <= (G value of layer0) <= (G value of ck max color), The green control condition is true, else the condition is false. 1: If (G value of ck min color) > (G value of layer0) or (G value of layer0) > (G value of ck max color), The green control condition is true, else the condition is false.
8	R/W	0x0	CK_BLUECON Blue control condition 0: If (B value of ck min color) <= (B value of layer0) <= (B value of ck max color), The blue control condition is true, else the condition is false. 1: If (B value of ck min color) > (B value of layer0) or (B value of layer0) > (B value of ck max color), The blue control condition is true, else the condition is false.
7:5	/	/	/
4	R/W	0x0	PRI Priority selection 0: ROP output channel is higher than channel 3 1: Channel 3 is higher than ROP output channel
3	/	/	/

Offset: 0x00C0			Register Name: MP_CK_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
2:1	R/W	0x0	ALPHACK_MOD Alpha / Color key mode selection 00: Alpha mode 01: Color key mode, using the high priority layer as matching condition, if it is true, the low priority layer pass. 10: color key mode, using the low priority layer as matching condition, if it is true, the high priority layer pass. 11: Reserved
0	R/W	0x0	ALPHACK_EN Enable control 0: The ROP data will by-pass the alpha/ck module 1: Enable If the module is disabled, the data of channel 3 will be ignored, and only the ROP data will pass through to CSC2 module.

5.1.5.23. Mixer Color key Min Color Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: MP_CK_MIN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CKMIN_R Red
15:8	R/W	0x0	CKMIN_G Green
7:0	R/W	0x0	CKMIN_B Blue

5.1.5.24. Mixer Color key Max Color Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: MP_CK_MAX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CKMAX_R Red
15:8	R/W	0x0	CKMAX_G Green
7:0	R/W	0x0	CKMAX_B Blue

5.1.5.25. Mixer Color Space Converter 2 Control Register(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: MP_CSC2_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	CSC2_EN Enable control 0: Disable color space function, ignore the control setting, and the

Offset: 0x00D0			Register Name: MP_CSC2_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			data flow will by-pass the module. 1: Enable color space converting function.

5.1.5.26. Mixer Output Control Register(Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: MP_OUTPUT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:8	R/W	0x0	OUT_PS Output data pixel sequence Reference output pixel sequence table
7	R/W	0x0	RND_EN Round enable 0: Disabled 1: Enabled
6:4	/	/	/
3:0	R/W	0x0	OUT_FMT Output data format 0000: 32bpp – A8R8G8B8 or interleaved AYUV8888 0001: 16bpp – A4R4G4B4 0010: 16bpp – A1R5G5B5 0011: 16bpp – R5G6B5 0100: 16bpp – interleaved YUV422 0101: planar YUV422 (UV combined) 0110: planar YUV422 0111: 8bpp – MONO 1000: 4bpp – MONO 1001: 2bpp – MONO 1010: 1bpp – MONO 1011: planar YUV420 (UV combined) 1100: planar YUV420 1101: planar YUV411 (UV combined) 1110: planar YUV411 Other: Reserved **NOTE** **In all YUV output data format, the CSC2 must be enabled, otherwise the output data mode will be 32bpp A8R8G8B8 mode.**

Output data mode and output data ports mapping:

Output data mode	Output data channel selection		
	Channel 0	Channel 1	Channel 2
A8R8G8B8 or interleaved AYUV8888	ARGB or AYUV	Ignore	Ignore
A4R4G4B4	ARGB	Ignore	Ignore
A1R5G5B5	ARGB	Ignore	Ignore
R5G6B5	RGB	Ignore	Ignore
interleaved YUV422	YUV	Ignore	Ignore
planar YUV422 (UV combined)	Y	UV	Ignore
planar YUV422	Y	U	V
8bpp – MONO	MONO	Ignore	Ignore
4bpp – MONO	MONO	Ignore	Ignore
2bpp – MONO	MONO	Ignore	Ignore
1bpp – MONO	MONO	Ignore	Ignore
planar YUV420 (UV combined)	Y	UV	Ignore
planar YUV420	Y	U	V
planar YUV411 (UV combined)	Y	UV	Ignore
planar YUV411	Y	U	V

5.1.5.27. Mixer Output Size Register(Default Value: 0x0000_0000)

Offset: 0x00E8			Register Name: MP_OUTPUT_SIZE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Height The value add 1 equal the actual output image height
15:11	/	/	/
12:0	R/W	0x0	OUT_WIDTH Width The value add 1 equal the actual output image width

5.1.5.28. Mixer Output High 4bit Address Register(Default Value: 0x0000_0000)

Offset: 0x00EC			Register Name: MP_OUTPUT_HADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	OUTCH2_H4ADDR Output channel 2 High 4bit address in bit
15:12	/	/	/
11:8	R/W	0x0	OUTCH1_H4ADDR Output channel 1 High 4bit address in bit
7:4	/	/	/
3:0	R/W	0x0	OUTCH0_H4ADDR Output channel 0 High 4bit address in bit

5.1.5.29. Mixer Output Low 32bit Address Register(Default Value: 0x0000_0000)

Offset: 0x00F0 + N*0x04 (N=0~2)			Register Name: MP_OUTPUT_LADDR
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	OUT_L32ADDR Output channel Low 32bit address in bit

5.1.5.30. Mixer Output Pitch Register(Default Value: 0x0000_0000)

Offset: 0x0100 + N*0x04 (N=0~2)			Register Name: MP_OUTPUT_PITCH
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	OUT_LINEWIDTH Output channel Pitch in bit

5.1.5.31. Mixer Output Alpha Control Register(Default Value: 0x0000_0000)

Offset: 0x0120			Register Name: MP_OUTPUT_ALPHA
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	IMG_ALPHA Output image area alpha value, the image area include A0,A1 and overlapping area A2.
23:16	R/W	0x0	NONIMG_ALPHA Output non-image area alpha value, the non-image area means the pure fill color area.
15:8	/	/	/
7:6	R/W	0x0	A2ALPHACTL A2 area alpha value control 00: using A0 self pixel alpha (A0pA) 01: using A1 self pixel alpha (A1pA) 10: the alpha value = A0pA + A1pA * (1 - A0pA) 11: using the Output image area alpha value (bit31:24)
5:4	R/W	0x0	A3ALPHACTL A3 area alpha value control 00: 0xff 01: using the Output non-image area alpha value (bit23:16) Other: reserved
3:2	R/W	0x0	A1ALPHACTL A1 area alpha value control 00: using A1 self pixel alpha 01: using the Output image area alpha value (bit31:24) Other: reserved
1:0	R/W	0x0	A0ALPHACTL A0 area alpha value control 00: using A0 self pixel alpha 01: using the Output image area alpha value (bit31:24) Other: reserved

NOTE

The register is only valid in ARGB or AYUV mode.
There is some area in output memory block:
Only the channel 0,1,2 mixed area is called A0.
Only the channel 3 area is called A1.
The channel 0,1,2 mixed area and channel 3 mixed area is called A2.
The other area is called A3.
And the A0,A1,A2 is called image area,the A3 is called non-image area.

5.1.5.32. Mixer CSC0/1 Y/G Coefficient0 Register(Default Value: 0x04A7_04A7)

Offset: 0x0180			Register Name: MP_CSC_YGCOEF0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7	CSC1_YGCOEF0 The Y/G coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x4a7	CSC0_YGCOEF0 The Y/G coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.33. Mixer CSC0/1 Y/G Coefficient1 Register(Default Value: 0x1E6F_1E6F)

Offset: 0x0184			Register Name: MP_CSC_YGCOEF1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1e6f	CSC1_YGCOEF1 The Y/G coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x1e6f	CSC0_YGCOEF1 The Y/G coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.34. Mixer CSC0/1 Y/G Coefficient2 Register(Default Value: 0x1CBF_1CBF)

Offset: 0x0188			Register Name: MP_CSC_YGCOEF2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1cbf	CSC1_YGCOEF2 The Y/G coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x1cbf	CSC0_YGCOEF2 The Y/G coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.35. Mixer CSC0/1 Y/G Constant Register(Default Value: 0x0877_0877)

Offset: 0x018C			Register Name: MP_CSC_YGCONS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x877	CSC1_YGCONS The Y/G constant for CSC1 The value equals to coefficient*2^4
15:14	/	/	/
13:0	R/W	0x877	CSC0_YGCONS The Y/G constant for CSC0 The value equals to coefficient*2^4

5.1.5.36. Mixer CSC0/1 U/R Coefficient0 Register(Default Value: 0x04A7_04A7)

Offset: 0x0190			Register Name: MP_CSC_URCOEF0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7	CSC1_URCOEF0 The U/R coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x4a7	CSC0_URCOEF0 The U/R coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.37. Mixer CSC0/1 U/R Coefficient1 Register(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: MP_CSC_URCOEF1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	CSC1_URCOEF1 The U/R coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x0	CSC0_URCOEF1 The U/R coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.38. Mixer CSC0/1 U/R Coefficient2 Register(Default Value: 0x0662_0662)

Offset: 0x0198			Register Name: MP_CSC_URCOEF2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x662	CSC1_URCOEF2 The U/R coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x662	CSC0_URCOEF2 The U/R coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.39. Mixer CSC0/1 U/R Constant Register(Default Value: 0x3211_3211)

Offset: 0x019C			Register Name: MP_CSC_URCONS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:16	R/W	0x3211	CSC1_URCONS The U/R constant for CSC1 The value equals to coefficient*2^4
15:14	/	/	/
13:0	R/W	0x3211	CSC0_URCONS The U/R constant for CSC0 The value equals to coefficient*2^4

5.1.5.40. Mixer CSC0/1 V/B Coefficient0 Register(Default Value: 0x04A7_04A7)

Offset: 0x01A0			Register Name: MP_CSC_VBCOEF0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x4a7	CSC1_VBCOEF0 The V/B coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x4a7	CSC0_VBCOEF0 The V/B coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.41. Mixer CSC0/1 V/B Coefficient1 Register(Default Value: 0x0812_0812)

Offset: 0x01A4			Register Name: MP_CSC_VBCOEF1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x812	CSC1_VBCOEF1 The V/B coefficient for CSC1 The value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x812	CSC0_VBCOEF1 The V/B coefficient for CSC0 The value equals to coefficient*2^{10}

5.1.5.42. Mixer CSC0/1 V/B Coefficient2 Register(Default Value: 0x0000_0000)

Offset: 0x01A8			Register Name: MP_CSC_VBCOEF2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	CSC1_VBCOEF2 the V/B coefficient for CSC1 the value equals to coefficient*2^{10}
15:13	/	/	/
12:0	R/W	0x0	CSC0_VBCOEF2

Offset: 0x01A8			Register Name: MP_CSC_VBCOEF2
Bit	Read/Write	Default/Hex	Description
			the V/B coefficient for CSC0 the value equals to coefficient*2^{10}

5.1.5.43. Mixer CSC0/1 V/B Constant Register(Default Value: 0x0000_0000)

Offset: 0x1AC			Register Name: MP_CSC_VBCONS
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:16	R/W	0x2eb1	CSC1_VBCONS The V/B constant for CSC1 The value equals to coefficient*2^4
15:14	/	/	/
13:0	R/W	0x2eb1	CSC0_VBCONS The V/B constant for CSC0 The value equals to coefficient*2^4

5.1.5.44. Mixer CSC2 Y/G Coefficient Register(Default Value: 0x0000_0000)

Offset: 0x01C0 + N*0x04 (N=0~2)			Register Name: MP_OCSC_YGCOEF
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CSC2_YGCOEF The Y/G coefficient The value equals to coefficient*2^{10}

5.1.5.45. Mixer CSC2 Y/G Constant Register(Default Value: 0x0000_0000)

Offset: 0x01CC			Register Name: MP_OCSC_YGCONS
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	CSC2_YGCONS The Y/G constant The value equals to coefficient*2^4

5.1.5.46. CSC2 U/R Coefficient Register(Default Value: 0x0000_0000)

Offset: 0x01D0 + N*0x04 (N=0~2)			Register Name: MP_OCSC_URCOEF
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CSC2_URCOEF The U/R coefficient The value equals to coefficient*2^{10}

5.1.5.47. Mixer CSC2 U/R Constant Register(Default Value: 0x0000_0000)

Offset: 0x01DC			Register Name: MP_OCSC_URCONS
Bit	Read/Write	Default/Hex	Description

Offset: 0x01DC			Register Name: MP_OCSC_URCONS
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	CSC2_URCONS The U/R constant The value equals to coefficient*2^4

5.1.5.48. Mixer CSC2 V/B Coefficient Register(Default Value: 0x0000_0000)

Offset: 0x01E0 + N*0x4 (N=0~2)			Register Name: MP_OCSC_VBCOEF
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CSC2_VBCOEF The V/B coefficient The value equals to coefficient*2^{10}

5.1.5.49. Mixer CSC2 V/B Constant Register(Default Value: 0x0000_0000)

Offset: 0x01EC			Register Name: MP_OCSC_VBCONS
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	CSC2_VBCONS The V/B constant The value equals to coefficient*2^4

5.1.5.50. Mixer Scaling Horizontal Filtering Coefficient RAM Register(Default Value: 0x0000_0000)

Offset: 0x0200 ~ 0x027C			Register Name:MP_SCALER_HCOEFF
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	Horizontal tap0 coefficient The value equals to coefficient*2^6

5.1.5.51. Mixer Scaling Vertical Filtering Coefficient RAM Register(Default Value: 0x0000_0000)

Offset: 0x0280 ~ 0x02FC			Register Name:MP_SCALER_VCOEFF
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	Vertical tap2 coefficient The value equals to coefficient*2^6
15:08	R/W	0x0	Vertical tap1 coefficient The value equals to coefficient*2^6
07:00	R/W	0x0	Vertical tap0 coefficient The value equals to coefficient*2^6

5.1.5.52. Mixer Palette Table RAM

Offset: 0x0400 ~ 0x07FC			Register Name:MP_PALETTE_TAB
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

Chapter 6. Image

This chapter introduces the image section of A40i processor.

- CSI
- TV Decoder

Here is the CMOS sensor and TV decoder with YUV data process diagram.

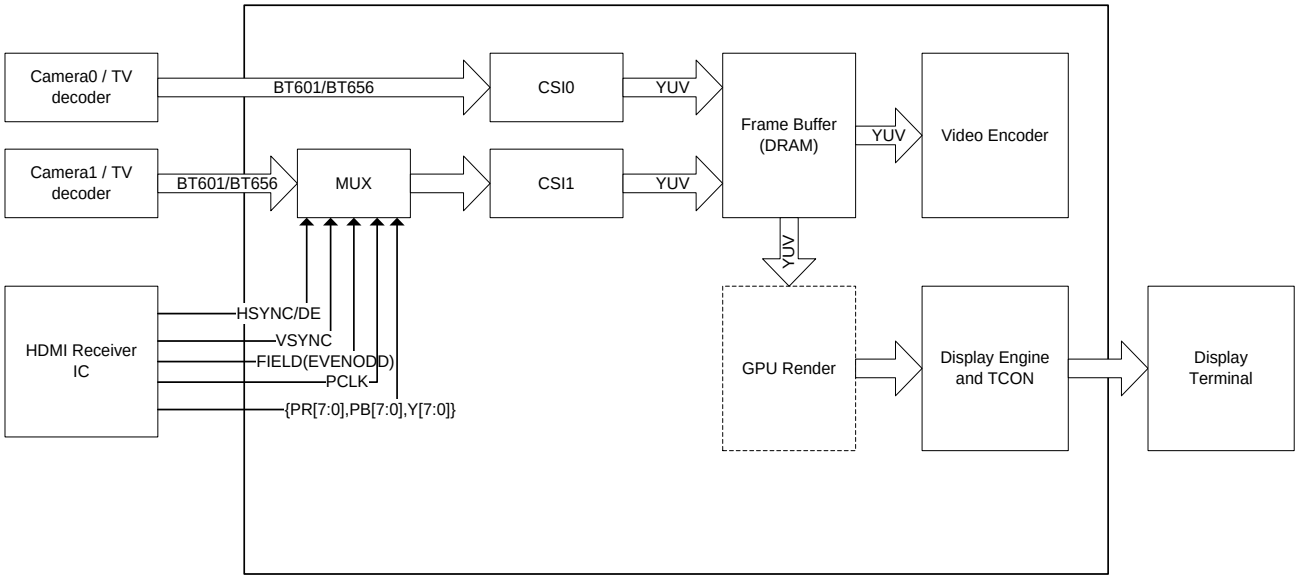


Figure 6-1. CSI and TV Decoder Data Processor Diagram

6.1. CSI

6.1.1. Overview

There are two CSI controllers(CSI0/CSI1). The two controllers are different.

CSI0 features:

- Supports 8-bit YUV422 CMOS sensor interface
- Supports 8-bit BT656 interface
- Supports 16-bit BT1120 interface
- Supports CCIR656 protocol for NTSC and PAL
- Supports multi-channel ITU-R BT.656 time-multiplexed format
- Supports still capture resolution up to 5M,video capture resolution up to 1080p@30fps

CSI1 features:

- Supports 8-bit YUV422 CMOS sensor interface
- Supports 8-bit BT656 interface
- Supports CCIR656 protocol for NTSC and PAL
- Supports 24-bit RGB/YUV444 input
- Supports still capture resolution up to 5M,video capture resolution up to 720p@30fps

6.1.2. Block Diagram

Figure 6-2 shows a block diagram of the CSI0.

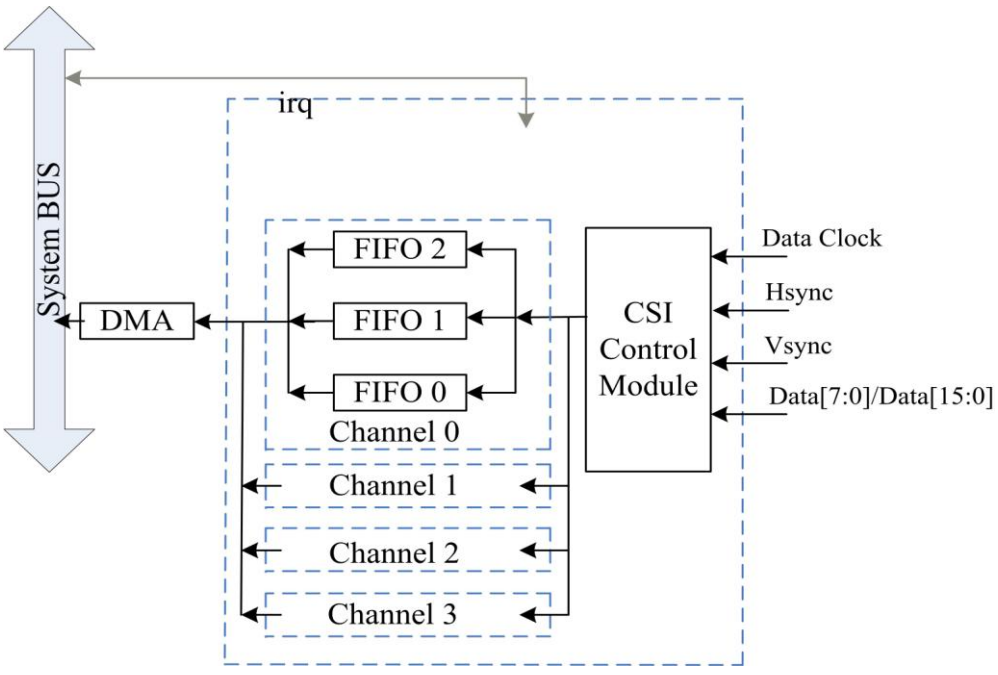


Figure 6-2. CSI0 Block Diagram

Figure 6-3 shows a block diagram of the CSI1.

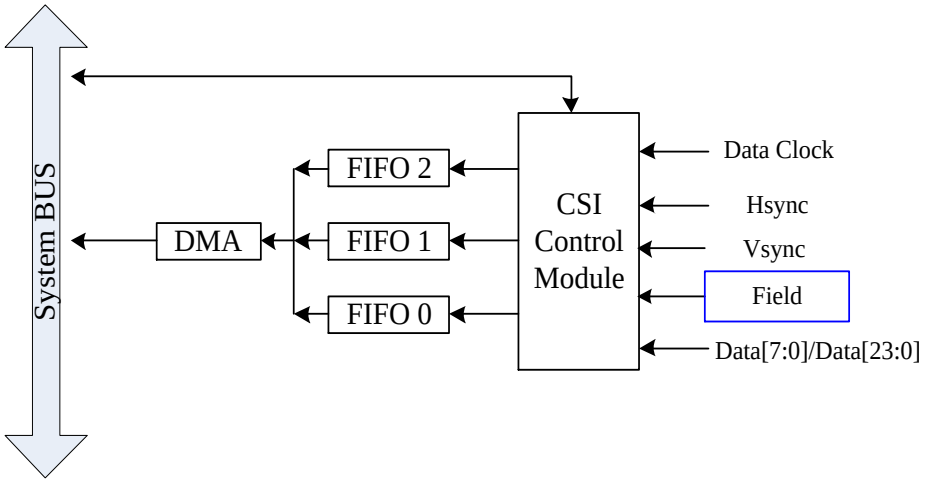


Figure 6-3. CSI1 Block Diagram

6.1.3. Operations and Functional Descriptions

6.1.3.1. External Signals

Table 6-1 describes the external signals of CSI. CSI_PCLK is pixel sample clock. CSI_MCLK is master clock output to sensor or other devices. The unused CSI ports are used as General Purpose I/O ports. For information about General Purpose I/O ports, see **Port Controller** in chapter3.

Table 6-1. CSI External Signals

Signal	Description	Type
CSI0_D[15:0]	CSI0 Data bit[15:0]	I
CSI1_D[23:0]	CSI1 Data bit[23:0]	I
CSI0/1_PCLK	CSI0/1 Pixel Clock	I
CSI0/1_MCLK	CSI0/1 Master Clock	O
CSI0/1_VSYNC	CSI0/1 Vertical SYNC	I
CSI0/1_HSYNC	CSI0/1 Horizontal SYNC	I

6.1.3.2. Clock Sources

Two Clocks need to be configured for CSI controller.CSI0/1_MCLK provides the master clock for sensor and other devices. CSI_SCLK is the top clock for the whole CSI module. They also have some clock source to select. Table 6-2 describes the clock sources for CSI0/1_MCLK, Table 6-3 describes the clock sources for CSI_SCLK. Users can see **CCU** in chapter3 for clock setting, configuration and gating information.

Table 6-2. CSI0/1_MCLK Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_VIDEO1	VIDEO Clock,default value is 297MHz
PLL_PERIPH1	Peripheral Clock,default value is 600MHz

Table 6-3. CSI_SCLK Sources

Clock Sources	Description
PLL_PERIPH0	Peripheral Clock,default value is 600MHz
PLL_PERIPH1	Peripheral Clock,default value is 600MHz

6.1.3.3. CSI FIFO Distribution

Table 6-4 describes the FIFO distribution of CSI.

Table 6-4. CSI FIFO Distribution

Interface	YUYV422 Interleaved/Raw			BT656/BT1120 Interface		YUV444	
Input format	YUV422		Raw	YUV422		YUV444	
Output format	Planar	UV combined/ MB	Raw/RGB /PRGB	Planar	UV combined/ MB	Planar	UV combined/ MB
CH0_FIFO0	Y pixel data	Y pixel data	All pixels data	Y	Y	Y pixel data	Y pixel data
CH0_FIFO1	Cb (U) pixel data	Cb (U) Cr (V) pixel data	-	Cb (U)	CbCr (UV)	Cb (U) pixel data	Cb (U) Cr (V) pixel data
CH0_FIFO2	Cr (V) pixel data	-	-	Cr (V)		Cr (V) pixel data	-

6.1.3.4. CCIR656 Head Code

Table 6-5 describes the definition of CCIR656 Header Data.

Table 6-5. CCIR656 Header Data Bit Definition

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	1	0	0	1
CS D[8]	1	0	0	F
CS D[7]	1	0	0	V
CS D[6]	1	0	0	H
CS D[5]	1	0	0	P3
CS D[4]	1	0	0	P2
CS D[3]	1	0	0	P1
CS D[2]	1	0	0	P0

CS D[1]	x	x	x	x
CS D[0]	x	x	x	x

For compatibility with an 8-bit interface, CS D[1] and CS D[0] are not defined.

Table 6-6. CSI Decode Definition

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

Multi-Channel:

Table 6-7. CSI Multi-channel Definition

Condition			656FVH Value			SAV-EAV Code						
Field	V-time	H-time	F	V	H	First	Second	Third	Fourth			
									Ch1	Ch2	Ch3	Ch4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	BLANK	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	BLANK	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

6.1.4. Register List

Module Name	Base Address
CSI0	0x01C09000
CSI1	0x01C1D000

Register Name	Offset	Description
CSI0		
CSI0_EN_REG	0x0000	CSI Enable Register
CSI0_CFG_REG	0x0004	CSI Configuration Register
CSI0_CAP_REG	0x0008	CSI Capture Control Register
CSI0_SCALE_REG	0x000C	CSI Scale Register
CSI0_C0_F0_BUFA_REG	0x0010	CSI Channel_0 FIFO 0 Output Buffer-A Address Register
CSI0_C0_F0_BUFB_REG	0x0014	CSI Channel_0 FIFO 0 Output Buffer-B Address Register
CSI0_C0_F1_BUFA_REG	0x0018	CSI Channel_0 FIFO 1 Output Buffer-A Address Register
CSI0_C0_F1_BUFB_REG	0x001C	CSI Channel_0 FIFO 1 Output Buffer-B Address Register
CSI0_C0_F2_BUFA_REG	0x0020	CSI Channel_0 FIFO 2 Output Buffer-A Address Register
CSI0_C0_F2_BUFB_REG	0x0024	CSI Channel_0 FIFO 2 Output Buffer-B Address Register
CSI0_C0_BUF_CTL_REG	0x0028	CSI Channel_0 Output Buffer Control Register
CSI0_C0_BUF_STA_REG	0x002C	CSI Channel_0 Status Register
CSI0_C0_INT_EN_REG	0x0030	CSI Channel_0 Interrupt Enable Register
CSI0_C0_INT_STA_REG	0x0034	CSI Channel_0 Interrupt Status Register
/	0x0038	Reserved
/	0x003C	Reserved
CSI0_C0_HSIZE_REG	0x0040	CSI Channel_0 Horizontal Size Register
CSI0_C0_VSIZE_REG	0x0044	CSI Channel_0 Vertical Size Register
CSI0_C0_BUF_LEN_REG	0x0048	CSI Channel_0 Line Buffer Length Register
/	0x004C~0x010C	Reserved
CSI0_C1_F0_BUFA_REG	0x0110	CSI Channel_1 FIFO 0 Output Buffer-A Address Register
CSI0_C1_F0_BUFB_REG	0x0114	CSI Channel_1 FIFO 0 Output Buffer-B Address Register
CSI0_C1_F1_BUFA_REG	0x0118	CSI Channel_1 FIFO 1 Output Buffer-A Address Register
CSI0_C1_F1_BUFB_REG	0x011C	CSI Channel_1 FIFO 1 Output Buffer-B Address Register
CSI0_C1_F2_BUFA_REG	0x0120	CSI Channel_1 FIFO 2 Output Buffer-A Address Register
CSI0_C1_F2_BUFB_REG	0x0124	CSI Channel_1 FIFO 2 Output Buffer-B Address Register
CSI0_C1_BUF_CTL_REG	0x0128	CSI Channel_1 Output Buffer Control Register
CSI0_C1_BUF_STA_REG	0x012C	CSI Channel_1 Status Register
CSI0_C1_INT_EN_REG	0x0130	CSI Channel_1 Interrupt Enable Register
CSI0_C1_INT_STA_REG	0x0134	CSI Channel_1 Interrupt Status Register
/	0x0138	Reserved
/	0x013C	Reserved
CSI0_C1_HSIZE_REG	0x0140	CSI Channel_1 Horizontal Size Register
CSI0_C1_VSIZE_REG	0x0144	CSI Channel_1 Vertical Size Register
CSI0_C1_BUF_LEN_REG	0x0148	CSI Channel_1 Line Buffer Length Register
/	0x014C~0x020C	Reserved
CSI0_C2_F0_BUFA_REG	0x0210	CSI Channel_2 FIFO 0 Output Buffer-A Address Register

CSI0_C2_F0_BUFB_REG	0x0214	CSI Channel_2 FIFO 0 Output Buffer-B Address Register
CSI0_C2_F1_BUFA_REG	0x0218	CSI Channel_2 FIFO 1 Output Buffer-A Address Register
CSI0_C2_F1_BUFB_REG	0x021C	CSI Channel_2 FIFO 1 Output Buffer-B Address Register
CSI0_C2_F2_BUFA_REG	0x0220	CSI Channel_2 FIFO 2 Output Buffer-A Address Register
CSI0_C2_F2_BUFB_REG	0x0224	CSI Channel_2 FIFO 2 Output Buffer-B Address Register
CSI0_C2_BUF_CTL_REG	0x0228	CSI Channel_2 Output Buffer Control Register
CSI0_C2_BUF_STA_REG	0x022C	CSI Channel_2 Status Register
CSI0_C2_INT_EN_REG	0x0230	CSI Channel_2 Interrupt Enable Register
CSI0_C2_INT_STA_REG	0x0234	CSI Channel_2 Interrupt Status Register
/	0x0238	Reserved
/	0x023C	Reserved
CSI0_C2_HSIZE_REG	0x0240	CSI Channel_2 Horizontal Size Register
CSI0_C2_VSIZE_REG	0x0244	CSI Channel_2 Vertical Size Register
CSI0_C2_BUF_LEN_REG	0x0248	CSI Channel_2 Line Buffer Length Register
/	0x024C~0x030C	Reserved
CSI0_C3_F0_BUFA_REG	0x0310	CSI Channel_3 FIFO 0 Output Buffer-A Address Register
CSI0_C3_F0_BUFB_REG	0x0314	CSI Channel_3 FIFO 0 Output Buffer-B Address Register
CSI0_C3_F1_BUFA_REG	0x0318	CSI Channel_3 FIFO 1 Output Buffer-A Address Register
CSI0_C3_F1_BUFB_REG	0x031C	CSI Channel_3 FIFO 1 Output Buffer-B Address Register
CSI0_C3_F2_BUFA_REG	0x0320	CSI Channel_3 FIFO 2 Output Buffer-A Address Register
CSI0_C3_F2_BUFB_REG	0x0324	CSI Channel_3 FIFO 2 Output Buffer-B Address Register
CSI0_C3_BUF_CTL_REG	0x0328	CSI Channel_3 Output Buffer Control Register
CSI0_C3_BUF_STA_REG	0x032C	CSI Channel_3 Status Register
CSI0_C3_INT_EN_REG	0x0330	CSI Channel_3 Interrupt Enable Register
CSI0_C3_INT_STA_REG	0x0334	CSI Channel_3 Interrupt Status Register
/	0x0338	Reserved
/	0x033C	Reserved
CSI0_C3_HSIZE_REG	0x0340	CSI Channel_3 Horizontal Size Register
CSI0_C3_VSIZE_REG	0x0344	CSI Channel_3 Vertical Size Register
CSI0_C3_BUF_LEN_REG	0x0348	CSI Channel_3 Line Buffer Length Register
CSI1		
CSI1_EN_REG	0x0000	CSI Enable Register
CSI1_CFG_REG	0x0004	CSI Configuration Register
CSI1_CAP_REG	0x0008	CSI Capture Control Register
CSI1_SCALE_REG	0x000C	CSI Scale Register
CSI1_F0_BUFA_REG	0x0010	CSI FIFO 0 Output Buffer-A Address Register
CSI1_F0_BUFB_REG	0x0014	CSI FIFO 0 Output Buffer-B Address Register
CSI1_F1_BUFA_REG	0x0018	CSI FIFO 1 Output Buffer-A Address Register
CSI1_F1_BUFB_REG	0x001C	CSI FIFO 1 Output Buffer-B Address Register
CSI1_F2_BUFA_REG	0x0020	CSI FIFO 2 Output Buffer-A Address Register
CSI1_F2_BUFB_REG	0x0024	CSI FIFO 2 Output Buffer-B Address Register
CSI1_BUF_CTL_REG	0x0028	CSI Output Buffer Control Register
CSI1_BUF_STA_REG	0x002C	CSI Status Register
CSI1_INT_EN_REG	0x0030	CSI Interrupt Enable Register
CSI1_INT_STA_REG	0x0034	CSI Interrupt Status Register
/	0x0038	Reserved

/	0x003C	Reserved
CSI1_HSIZE_REG	0x0040	CSI Horizontal Size Register
CSI1_VSIZE_REG	0x0044	CSI Vertical Size Register
CSI1_BUF_LEN_REG	0x0048	CSI Line Buffer Length Register

6.1.5. Register Description

6.1.5.1. CSI0 Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CSI0_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	PCLK_CNT Pclk count per frame
8	R/W	0x0	LUMA_EN Luma enable
7:5	/	/	/
4	R/W	0x0	NON16_ADD Non-16 add 0x00
3	R/W	0x0	RD_FIFO_EN Read fifo [3]fifo enable, fifo address[01c09800~01c09ffc]
2	R/W	0x0	FIELD_REV CCIR656 field_reverse
1	/	/	/
0	R/W	0x0	CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module

6.1.5.2. CSI0 Configuration Register(Default Value: 0x0030_0205)

Offset: 0x0004			Register Name: CSI0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x3	INPUT_FMT Input data format 000: RAW stream 001: reserved 010: CCIR656(one channel） 011: YUV422 100: YUV422 16bit data bus 101: two channel CCIR656 110: reserved 111: four channel CCIR656
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: pass-through

Offset: 0x0004			Register Name: CSI0_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			When the input format is set CCIR656 interface 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1111: interlaced interleaved YCbCr422. In this mode, capturing interlaced input and output the interlaced fields from individual ports. Field 1 data will be written to FIFO0 output buffer and field 2 data will be written to FIFO1 output buffer. 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 When the input format is set YUV422 0000: planar YUV 422 0001: planar YUV 420 0100: planar YUV 422 UV combined 0101: planar YUV 420 UV combined 1000: MB YUV 422 1001: MB YUV 420
15:12	/	/	/
11:10	R/W	0x0	FIELD_SEL Field selection. Applies to CCIR656 interface only. 00: start capturing with field 1. 01: start capturing with field 2. 10: start capturing with either field. 11: reserved
9:8	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 mode. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
7:3	/	/	/
2	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
1	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
0	R/W	0x1	CLK_POL

Offset: 0x0004			Register Name: CSI0_CFG_REG
Bit	Read/Write	Default/Hex	Description
			Data clock type 0: active in rising edge 1: active in falling edge

6.1.5.3. CSI0 Capture Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CSI0_CAP_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	VCAP_ON Video capture control: Capture the video image data stream. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/W	0x0	SCAP_ON Still capture control: Capture a single still image frame. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared, and it always reads as a 0.

6.1.5.4. CSI0 Horizontal Scale Register(Default Value: 0x0F00_FFFF)

Offset: 0x000C			Register Name: CSI0_SCALE_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0xF	VER_MASK Vertical (line) mask. Every 4-line is a mask group. Bit 24 mask the first line, bit 25 mask the second line, and so on. Mask bit = 0 means discarding this line data.
23:16	/	/	/
15:0	R/W	0xFFFF	HOR_MASK Horizontal (datastream) mask. Every 16-byte is a mask group. Bit 0 masks the first byte, bit 1 masks the second byte, and so on. Mask bit = 0 means discarding this byte from the datastream.

6.1.5.5. CSI0 Channel_0~3 FIFO 0 Output Buffer-A Address Register(Default Value: 0x0000_0000)

Offset: 0x0010+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F0_BUFA

Offset: 0x0010+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F0_BUFA_REG
Bit	Read/Write	Default/Hex	Description
			FIFO 0 output buffer-A address

6.1.5.6. CSI0 Channel_0~3 FIFO 0 Output Buffer-B Address Register(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F0_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F0_BUFB FIFO 0 output buffer-B address

6.1.5.7. CSI0 Channel_0~3 FIFO 1 Output Buffer-A Address Register(Default Value: 0x0000_0000)

Offset: 0x0018+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F1_BUFA FIFO 1 output buffer-A address

6.1.5.8. CSI0 Channel_0~3 FIFO 1 Output Buffer-B Address Register(Default Value: 0x0000_0000)

Offset: 0x001C+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F1_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F1_BUFB FIFO 1 output buffer-B address

6.1.5.9. CSI0 Channel_0~3 FIFO 2 Output Buffer-A Address Register(Default Value: 0x0000_0000)

Offset: 0x0020+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F2_BUFA FIFO 2 output buffer-A address

6.1.5.10. CSI0 Channel_0~3 FIFO 2 Output Buffer-B Address Register(Default Value: 0x0000_0000)

Offset: 0x0024+N*0x100(N=0~3)			Register Name: CSI0_C0~3_F2_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F2_BUFB FIFO 2 output buffer-B address

6.1.5.11. CSI0 Channel_0~3 Output Buffer Control Register(Default Value: 0x0000_0000)

Offset: 0x0028+N*0x100(N=0~3)			Register Name: CSI0_C0~3_BUF_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DBN

			Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
1	R	0x0	DBS Output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
0	R/W	0x0	DBE Double buffer mode enable 0: Disable 1: Enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

6.1.5.12. CSI0 Channel_0~3 Status Register(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x100(N=0~3)			Register Name: CSI0_C0_BUF_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	R	0x0	LUM_STATIS luminance statistical value When frame done interrupt flag come, the value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
7:2	/	/	/
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabled video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabled still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.5.13. CSI0 Channel_0~3 Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0030+N*0x100(N=0~3)			Register Name: CSI0_C0~3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame

Offset: 0x0030+N*0x100(N=0~3)			Register Name: CSI0_C0~3_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	/	/	/
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.14. CSI0 Channel_0~3 Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034+N*0x100(N=0~3)			Register Name: CSI0_C0~3_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	/	/	/
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.5.15. CSI0 Channel_0~3 Horizontal Size Register(Default Value: 0x0500_0000)

Offset: 0x0040+N*0x100(N=0~3)			Register Name: CSI0_C0~3_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

6.1.5.16. CSI0 Channel_0~3 Vertical Size Register(Default Value: 0x01E0_0000)

Offset: 0x0044+N*0x100(N=0~3)			Register Name: CSI0_C0~3_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. Data is valid from this line.

6.1.5.17. CSI0 Channel_0~3 Buffer Length Register(Default Value: 0x0000_0280)

Offset: 0x0048+N*0x100(N=0~3)			Register Name: CSI0_C0~3_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

6.1.5.18. CSI1 Enable Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CSI1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	PCLK_CNT Pclk count per frame
8	R/W	0x0	LUMA_EN Luma enable
7:5	/	/	/
4	R/W	0x0	NON16_ADD Non-16 add 0x00
3	R/W	0x0	RD_FIFO_EN Read fifo [3]fifo enable, fifo address[01c09800~01c09ffc]
2	R/W	0x0	FIELD_REV CCIR656 field_reverse
1	/	/	/
0	R/W	0x0	CSI_EN Enable

Offset: 0x0000			Register Name: CSI1_EN_REG
Bit	Read/Write	Default/Hex	Description
			0: Reset and disable the CSI module 1: Enable the CSI module

6.1.5.19. CSI1 Configuration Register(Default Value: 0x0030_0205)

Offset: 0x0004			Register Name: CSI1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	/
22:20	R/W	0x3	INPUT_FMT Input data format 000: RAW stream 001: reserved 010: CCIR656(one channel) 011: YUV422 100: YUV444({R, B, G} or {Pr, Pb, Y}) 101: two channel CCIR656 110: reserved 111: four channel CCIR656
19:16	R/W	0x0	OUTPUT_FMT Output data format When the input format is set RAW stream 0000: pass-through When the input format is set CCIR656 interface 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1111: interlaced interleaved YCbCr422. In this mode, capturing interlaced input and output the interlaced fields from individual ports. Field 1 data will be written to FIFO0 output buffer and field 2 data will be written to FIFO1 output buffer. 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 When the input format is set YUV422 0000: planar YUV 422 0001: planar YUV 420 0100: planar YUV 422 UV combined 0101: planar YUV 420 UV combined 1000: MB YUV 422 1001: MB YUV 420 When the input format is set YUV444 1100: field planar YUV 444

Offset: 0x0004			Register Name: CSI1_CFG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1101: field planar YUV 422 UV combined 1110: frame planar YUV 444 1111: frame planar YUV 422 UV combined
15:12	/	/	/
11:10	R/W	0x0	FIELD_SEL Field selection. Applies to CCIR656 interface only. 00: start capturing with field 1. 01: start capturing with field 2. 10: start capturing with either field. 11: reserved
9:8	R/W	0x2	INPUT_SEQ Input data sequence, only valid for YUV422 mode. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
7:5	/	/	/
4	R/W	0x0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames
3	R/W	0x0	FIELD_POL Field polarity 0: negative(field=0 indicate odd, field=1 indicate even) 1: positive(field=1 indicate odd, field=0 indicate even) This register is not applied to CCIR656 interface.
2	R/W	0x1	VREF_POL Vref polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
1	R/W	0x0	HERF_POL Href polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
0	R/W	0x1	CLK_POL Data clock type 0: active in rising edge 1: active in falling edge

6.1.5.20. CSI1 Capture Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: CSI1_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/

Offset: 0x0008			Register Name: CSI1_CAP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	VCAP_ON Video capture control: Capture the video image data stream. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
0	R/W	0x0	SCAP_ON Still capture control: Capture a single still image frame. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared ,and it always reads as a 0.

6.1.5.21. CSI1 Horizontal Scale Register(Default Value: 0x0F00_FFFF)

Offset: 0x000C			Register Name: CSI1_SCALE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:24	R/W	0xF	VER_MASK Vertical (line) mask. Every 4-line is a mask group. Bit 24 masks the first line, bit 25 masks the second line, and so on. Mask bit = 0 means discarding this line data.
23:16	/	/	/
15:0	R/W	0xFFFF	HOR_MASK Horizontal (datastream) mask. Every 16-byte is a mask group. Bit 0 masks the first byte, bit 1 masks the second byte, and so on. Mask bit = 0 means discarding this byte from the datastream.

6.1.5.22. CSI1 Channel_0 FIFO 0 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0010			Register Name: CSI1_C0_F0_BUFA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	C0F0_BUFA FIFO 0 output buffer-A address

6.1.5.23. CSI1 Channel_0 FIFO 0 Output Buffer-B Address Register(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: CSI1_C0_F0_BUFB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	C0F0_BUFB FIFO 0 output buffer-B address

6.1.5.24. CSI1 Channel_0 FIFO 1 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: CSI1_C0_F1_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F1_BUFA FIFO 1 output buffer-A address

6.1.5.25. CSI1 Channel_0 FIFO 1 Output Buffer-B Address Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: CSI1_C0_F1_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F1_BUFB FIFO 1 output buffer-B address

6.1.5.26. CSI1 Channel_0 FIFO 2 Output Buffer-A Address Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: CSI1_C0_F2_BUFA_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F2_BUFA FIFO 2 output buffer-A address

6.1.5.27. CSI1 Channel_0 FIFO 2 Output Buffer-B Address Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: CSI1_F2_BUFB_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	C0F2_BUFB FIFO 2 output buffer-B address

6.1.5.28. CSI1 Channel_0 Output Buffer Control Register(Default Value:0x0000_0000)

Offset: 0x0028			Register Name: CSI1_C0_BUF_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	DBN Buffer selected at next storing for CSI 0: Next buffer selection is buffer-A 1: Next buffer selection is buffer-B
1	R	0x0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
0	R/W	0x0	DBE Double buffer mode enable 0: Disable 1: Enable

Offset: 0x0028			Register Name: CSI1_C0_BUF_CTL_REG
Bit	Read/Write	Default/Hex	Description
			If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

6.1.5.29. CSI1 Channel_0 Status Register(Default Value:0x0000_0000)

Offset: 0x002C			Register Name: CSI1_C0_BUF_STA_REG
Bit	Read/Write	Default/Hex	Description
31:8	R	0x0	LUM_STATIS Luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
7:2	/	/	/
1	R	0x0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
0	R	0x0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.

6.1.5.30. CSI1 Channel_0 Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CSI1_C0_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	VS_INT_EN vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame
6	R/W	0x0	HB_OF_INT_EN Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
5	/	/	/
4	R/W	0x0	FIFO2_OF_INT_EN FIFO 2 overflow The bit is set when the FIFO 2 become overflow.
3	R/W	0x0	FIFO1_OF_INT_EN FIFO 1 overflow The bit is set when the FIFO 1 become overflow.
2	R/W	0x0	FIFO0_OF_INT_EN

Offset: 0x0030			Register Name: CSI1_C0_INT_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			FIFO 0 overflow The bit is set when the FIFO 0 become overflow.
1	R/W	0x0	FD_INT_EN Frame done Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
0	R/W	0x0	CD_INT_EN Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.

6.1.5.31. CSI1 Channel_0 Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: CSI1_C0_INT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W1C	0x0	VS_PD vsync flag
6	R/W1C	0x0	HB_OF_PD Hblank FIFO overflow
5	/	/	/
4	R/W1C	0x0	FIFO2_OF_PD FIFO 2 overflow
3	R/W1C	0x0	FIFO1_OF_PD FIFO 1 overflow
2	R/W1C	0x0	FIFO0_OF_PD FIFO 0 overflow
1	R/W1C	0x0	FD_PD Frame done
0	R/W1C	0x0	CD_PD Capture done

6.1.5.32. CSI1 Channel_0 Horizontal Size Register(Default Value: 0x0500_0000)

Offset: 0x0040			Register Name: CSI1_C0_HSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:0	R/W	0x0	HOR_START Horizontal pixel clock start.Pixel data is valid from this clock.

6.1.5.33. CSI Channel_0 Vertical Size Register(Default Value: 0x01E0_0000)

Offset: 0x0044			Register Name: CSI1_C0_VSIZE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:0	R/W	0x0	VER_START Vertical line start. data is valid from this line.

6.1.5.34. CSI Channel_0 Buffer Length Register

Offset: 0x0048			Register Name: CSI1_C0_BUF_LEN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x280	BUF_LEN Buffer length of a line. Unit is byte. It is the max of the 3 FIFOs

6.2. TV Decoder

6.2.1. Overview

The Television Decoder (TVD) is an interface transforms Composite Video Broadcast Signal (CVBS) into YUV data.

Features:

- 4-channel CVBS input or 1-channel YPbPr and 1-channel CVBS
- 1-channel YPbPr input, 576p/480p/576i/480i supported
- Accept NTSC and PAL
- Supports YUV422, YUV420 format
- With 3D comb filter
- Programmable brightness, contrast, saturation
- 10-bit video ADCs

6.2.2. Block Diagram

Figure 6-4 shows a block diagram of TVD.

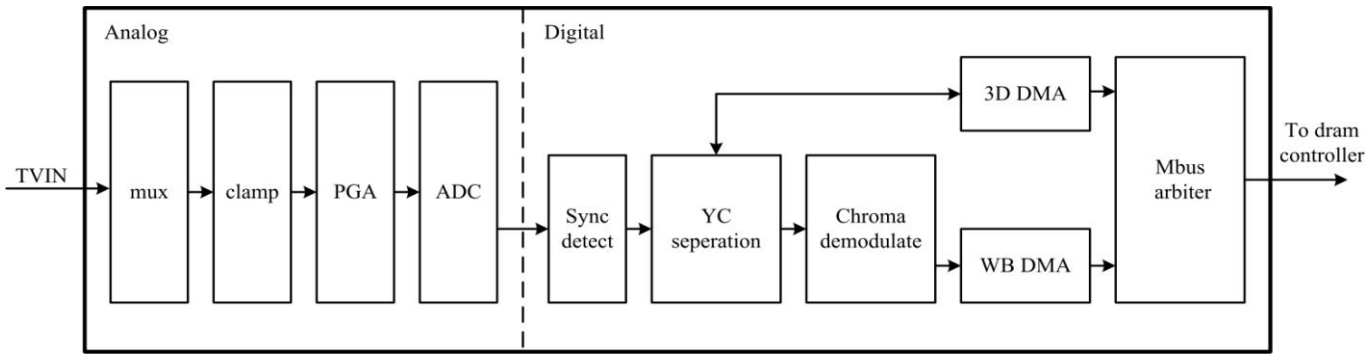


Figure 6-4. TVD Block Diagram

3D DMA is used for 3D comb filter.

WB DMA is used for TVD capture image writeback data.

Figure 6-5 shows the typical application diagrams of TVD.

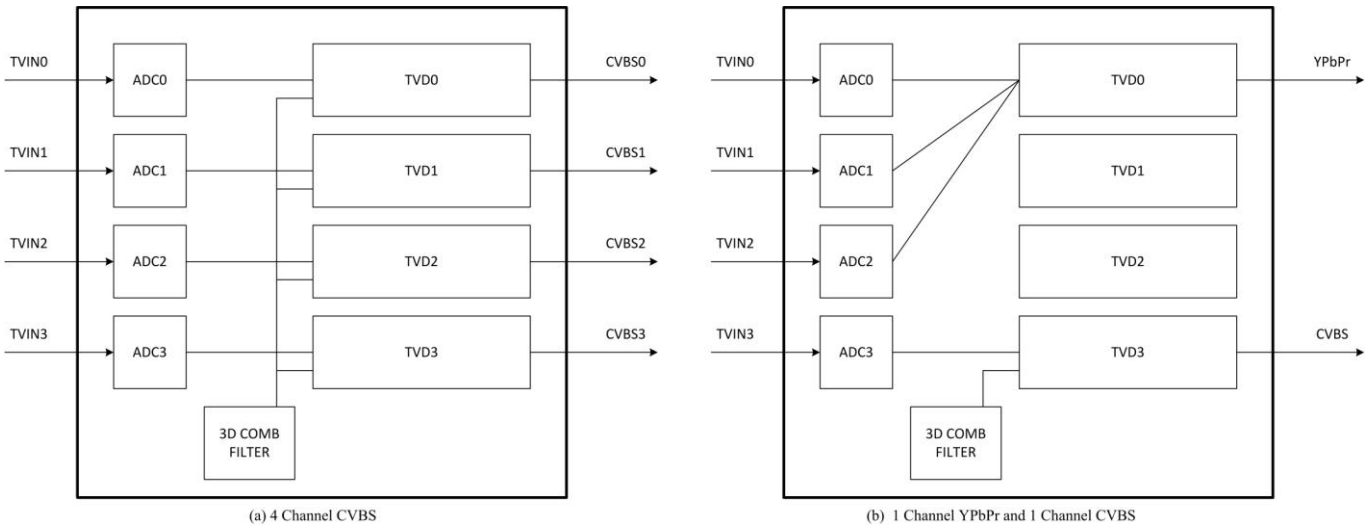


Figure 6-5. TVD Application Diagram

6.2.3. Operations and Functional Descriptions

6.2.3.1. External Signals

Table 6-8 describes the external signals of TVD.

Table 6-8. TVD External Signals

Signal	Description	Type
VCC-TVIN	TV ADC Power	P
GND-TVIN	TV ADC Ground	G
TVADCVRP	TV ADC Positive Reference Voltage	P
TVADCVRN	TV ADC negative Reference Voltage	P
TVIN0	TV Input Channel 0	AI
TVIN1	TV Input Channel 1	AI
TVIN2	TV Input Channel 2	AI
TVIN3	TV Input Channel 3	AI

6.2.3.2. Clock Sources

TVD module requires one 27MHz clock, which is 50% duty. ADC and digital circuit get this one clock.

6.2.3.3. Timing Diagram

The timing of CVBS shows in Figure 6-6.

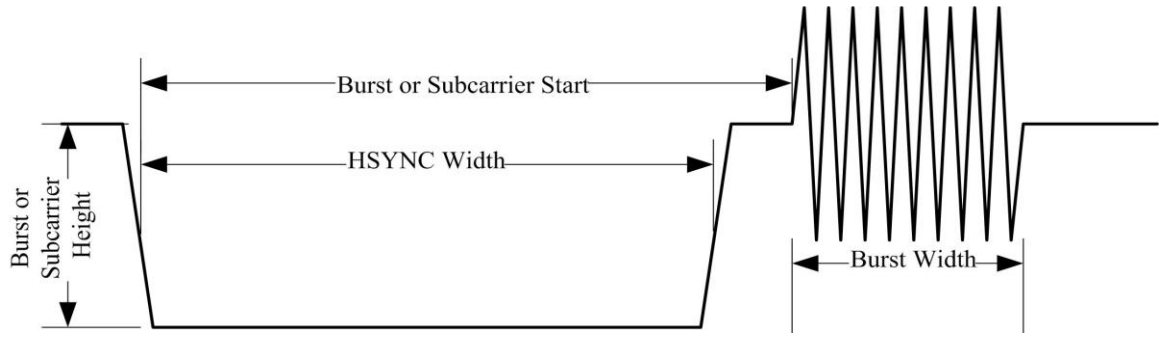


Figure 6-6. CVBS Timing

The timing parameters of CVBS shows in Table 6-9.

Table 6-9. CVBS Timing Constants

	Video Standard					
Paramter Description	NTSC-M	NTSC-J	PAL-M	PAL-B,D, G,H,I	PAL-N	PAL-Nc
HSYNC Width (us)	4.7	4.7	4.7	4.7	4.7	4.7
HSYNC VSYNC Height (V)	0.286	0.286	0.2857	0.3	0.2857	0.3
HSYNC Rise/Fall Time (10% to 90%) (ns)	150	150	150	200	200	200
Burst or Subcarrier Start (us)	5.3	5.3	5.8	5.6	5.6	5.6
Burst Width (us)	2.514 (9 cycle)	2.514 (9 cycle)	2.52 (9 cycle)	2.25 (10 cycle)	2.25 (10 cycle)	2.51 (9 cycle)
Subcarrier Frequency (Hz)	3579545	3579545	3579611.49	4433618.75	4433618.75	3582056.25
Burst or Subcarrier Height (V)	0.2857	0.2857	0.306	0.3	0.3	0.3
Phase Alternation	NO	NO	YES	YES	YES	YES
Number of Lines per Frame	525	525	525	625	625	625
Line Frequency (Hz)	15734.264	15734.264	15734.264	15625	15625	15625
Field Frequency (Hz)	59.94	59.94	59.94	50	50	50
Setup	YES	NO	YES	YES	YES	NO
First Active Line	22	22	22	23	23	23

Last Active Line	262	262	262	309	309	309
HSYNC to Blank End (us)	9.2	9.2	9.2	10.5	9.2	10.5
Blank Begin to HSYNC (us)	1.5	1.5	1.5	1.5	1.5	1.5
Blank to 100% White (V)	0.661	0.714	0.661	0.7	0.661	0.7
Number of Lines each for Vertical Serration, Equalization	3	3	3	2.5	3	2.5

6.2.4. Register List

Module Name	Base Address
TVD_TOP	0x01C30000
TVD0	0x01C31000
TVD1	0x01C32000
TVD2	0x01C33000
TVD3	0x01C34000

Register Name	Offset	Description
TVD_TOP		
TVD_TOP_MAP	0x0000	TVD TOP MAP Register
TVD_3D_CTL1	0x0008	TVD 3D DMA Control Register1
TVD_3D_CTL2	0x000C	TVD 3D DMA Control Register2
TVD_3D_CTL3	0x0010	TVD 3D DMA Control Register3
TVD_3D_CTL4	0x0014	TVD 3D DMA Control Register4
TVD_3D_CTL5	0x0018	TVD 3D DMA Control Register5
TVD_TOP _CTL	0x0024+N*0x20(N=0~3)	TVD TOP Control Register
TVD_ADC_CTL	0x0028+N*0x20(N=0~3)	TVD ADC Control Register
TVD_ADC_CFG	0x002C+N*0x20(N=0~3)	TVD ADC Configuration Register
TVD		
TVD_EN	0x0000	TVD Module Control Register
TVD_MODE	0x0004	TVD Mode Control Register
TVD_CLAMP_AGC1	0x0008	TVD CLAMP & AGC Control Register1
TVD_CLAMP_AGC2	0x000C	TVD CLAMP & AGC Control Register2
TVD_HLOCK1	0x0010	TVD HLOCK Control Register1
TVD_HLOCK2	0x0014	TVD HLOCK Control Register2
TVD_HLOCK3	0x0018	TVD HLOCK Control Register3
TVD_HLOCK4	0x001C	TVD HLOCK Control Register4
TVD_HLOCK5	0x0020	TVD HLOCK Control Register5
TVD_VLOCK1	0x0024	TVD VLOCK Control Register1
TVD_VLOCK2	0x0028	TVD VLOCK Control Register2

TVD_CLOCK1	0x002C	TVD Chroma Lock Control Register1
TVD_CLOCK2	0x0030	TVD Chroma Lock Control Register2
TVD_YC_SEP1	0x0040	TVD YC Seperation Control Register1
TVD_YC_SEP2	0x0044	TVD YC Seperation Control Register2
TVD_ENHANCE1	0x0050	TVD Enhancement Control Register1
TVD_ENHANCE2	0x0054	TVD Enhancement Control Register2
TVD_ENHANCE3	0x0058	TVD Enhancement Control Register3
TVD_WB1	0x0060	TVD WB DMA Control Register1
TVD_WB2	0x0064	TVD WB DMA Control Register2
TVD_WB3	0x0068	TVD WB DMA Control Register3
TVD_WB4	0x006C	TVD WB DMA Control Register4
TVD_IRQ_CTL	0x0080	TVD DMA Interrupt Control Register
TVD_IRQ_STATUS	0x0090	TVD DMA Interrupt Status Register
TVD_DEBUG1	0x0100	TVD Debug Control Register1
TVD_STATUS1	0x0180	TVD Debug Status Register1
TVD_STATUS2	0x0184	TVD Debug Status Register2
TVD_STATUS3	0x0188	TVD Debug Status Register3
TVD_STATUS4	0x018C	TVD Debug Status Register4
TVD_STATUS5	0x0190	TVD Debug Status Register5
TVD_STATUS6	0x0194	TVD Debug Status Register6

6.2.5. Register Description

6.2.5.1. TVD Top Map Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVD_TOP_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	TVD_ADC_MAP 00: NO MAP 01: 4 CVBS 10: 1 YPbPr and 1 CVBS 11: Reserved

6.2.5.2. TVD 3D DMA Control Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TVD_3D_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:4	R/W	0x1	COMB_3D_SEL 00: TVD0 01: TVD1 10: TVD2 11: TVD3
3:2	/	/	/
1	R/W	0x1	COMB_3D_EN

Offset: 0x0008			Register Name: TVD_3D_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Disable 1: Enable
0	R/W	0x0	TVD_EN_3D_DMA 0: Disable 1: Enable Set 0x1 when enable 3D comb filter.

6.2.5.3. TVD 3D DMA Control Register2(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: TVD_3D_CTL2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DRAM_TRIG

6.2.5.4. TVD 3D DMA Control Register3(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: TVD_3D_CTL3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_ADDR0

6.2.5.5. TVD 3D DMA Control Register4(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TVD_3D_CTL4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_ADDR1

6.2.5.6. TVD 3D DMA Control Register5(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: TVD_3D_CTL5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	COMB_3D_SIZE

6.2.5.7. TVD Top Control Register(Default Value: 0x0000_0000)

Offset: 0x0024+N*0x20(N=0~3)			Register Name: TVD_TOP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	LPF_SEL 0: 6M 1: 8M
23:5	/	/	/
4	R/W	0x0	LPF_DIG_EN 0: Disable

Offset: 0x0024+N*0x20(N=0~3)			Register Name: TVD_TOP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable
3:0	/	/	/

6.2.5.8. TVD ADC Control Register(Default Value: 0x0000_0000)

Offset: 0x0028+N*0x20(N=0~3)			Register Name: TVD_ADC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	Reserved
4:3	R/W	0x0	LPF_SEL 0: 11M 1: 16M
2	R/W	0x0	LPF_EN 0: Disable LPF circuit 1: Enable LPF circuit
1	R/W	0x0	AFE_EN 0: Disable AFE circuit 1: Enable AFE circuit
0	R/W	0x0	ADC_EN 0: Disable ADC circuit 1: Enable ADC circuit

6.2.5.9. TVD ADC Configuration Register(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x20(N=0~3)			Register Name: TVD_ADC_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	ADC_TEST adc_test signal en_adctest=1 adc test for ch1
30:29	/	/	/
28	R/W	0x0	DATA_DLY 0: no delay 1: delay ADC output data for half circle for ch1
27:19	/	/	/
18:16	R/W	0x0	CLP_STEP up/dn step size of dc_level
15:14	R/W	0x0	STAGE8_IBIAS
13:12	R/W	0x0	STAGE7_IBIAS
11:10	R/W	0x0	STAGE6_IBIAS
9:8	R/W	0x0	STAGE5_IBIAS
7:6	R/W	0x0	STAGE4_IBIAS
5:4	R/W	0x0	STAGE3_IBIAS
3:2	R/W	0x0	STAGE2_IBIAS
1:0	R/W	0x0	STAGE1_IBIAS

6.2.5.10. TVD Module Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVD_EN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26	R/W	0x0	en lock disable write back2(when unlocked,auto disable wb)
25	R/W	0x0	en lock disable write back1(only start wb when locked)
24:16	/	/	/
15	R/W	0x0	CLR_RSMP_FIFO 0: release 1: clear Set 0x1 then 0x0 to reset resample FIFO.
14:1	/	/	/
0	R/W	0x0	TVD_EN_CH 0:disable 1: enable

6.2.5.11. TVD Mode Control Register(Default Value: 0x0000_0020)

Offset: 0x0004			Register Name: TVD_MODE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	BLUE_MODE_COLOR 0: blue 1: black
7:6	/	/	/
5:4	R/W	0x2	BLUE DISPLAY MODE 00: Disabled 01: Enabled 10: Auto 11: reserved
3	/	/	/
2	R/W	0x0	PROGRESSIVE_MODE 0: interlace mode 1: progressive mode
1	R/W	0x0	SVIDEO_MODE 0: cvbs 1: S-Video
0	R/W	0x0	YPBPR_MODE 0: Disable the component input 1: Enable the component input

6.2.5.12. TVD Clamp & AGC Control Register1(Default Value: 0xA001_DD02)

Offset: 0x0008			Register Name: TVD_CLAMP_AGC1
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0008			Register Name: TVD_CLAMP_AGC1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0xA0	CAGC_TARGET These bits set the chroma AGC target
23:17	/	/	/
16	R/W	0x1	CAGC_EN 0: off 1: on
15:8	R/W	0xDD	AGC_TARGET When AGC_EN = 1 , the AGC_TARGET is used to directly digital AGC circuit. When AGC_EN = 0 , the AGC_TARGET is used to directly drive the analog PGA. (64 represents 1x, 32 represents 0.5x).
7:2	/	/	/
1	R/W	0x1	AGC_FREQUENCE 0: AGC gain update once per line 1: AGC gain update once per frame
0	R/W	0x0	AGC_EN 0: AGC disable 1: AGC enable

6.2.5.13. TVD Clamp & AGC Control Register2(Default Value: 0x8682_6440)

Offset: 0x000C			Register Name: TVD_CLAMP_AGC2
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	BLACK_LEVEL_CLAMP 0: subtraction 0 1: subtraction 16
30:29	/	/	/
28:16	R/W	0x682	AGC_GATE_BEGIN Count from hsync to the next line AGC gate
15:8	R/W	0x64	AGC_BACKPORCH_DELAY Count from sync tip to back porch gate
7	/	/	/
6:0	R/W	0x40	AGC_GATE_WIDTH AGC gate width

6.2.5.14. TVD HLOCK Control Register1(Default Value: 0x2000_0000)

Offset: 0x0010			Register Name: TVD_HLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x20000000	H_SAMPLE_STEP H_SAMPLE_STEP = F_{out}/F_{in} * 2^30

6.2.5.15. TVD HLOCK Control Register2(Default Value: 0x0000_0000)

Offset: 0x0014	Register Name: TVD_HLOCK2

Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x4E	HSYNC_FILTER_GATE_END_TIME These bits specify the end of the horizontal-blank-interval window. Default = 78
23:16	R/W	0xD6	HSYNC_FILTER_GATE_START_TIME These bits specify the beginning of the horizontal-blank-interval window. Default = -42
15:4	/	/	/
3:0	R/W	0x0	HTOL 0000: 858 0001: 864 0010~0111: Reserved Horizontal total pixels per line.

6.2.5.16. TVD HLOCK Control Register3(Default Value: 0x0FE9_502D)

Offset: 0x0018			Register Name: TVD_HLOCK3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0F	Hsync tip detect window end time
23:16	R/W	0xE9	Hsync tip detect window start time
15:8	R/W	0x50	Hsync rising detect window end time
7:0	R/W	0x2D	Hsync rising detect window start time

6.2.5.17. TVD HLOCK Control Register4(Default Value: 0x3E3E_8000)

Offset: 0x001C			Register Name: TVD_HLOCK4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x3E	Hsync fine to coarse offset
23:16	R/W	0x3E	Hsync rising time for fine detect
15:8	R/W	0x80	Hsync detect window end time for corase detect
7:0	R/W	0x00	Hsync detect window start time for coarse detection

6.2.5.18. TVD HLOCK Control Register5(Default Value: 0x4E22_5082)

Offset: 0x0020			Register Name: TVD_HLOCK5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x4E	Backporch detect window end time
23:16	R/W	0x22	Backporch detect window start time
15:8	R/W	0x50	HACTIVE_WIDTH
7:0	R/W	0x82	HACTIVE_START

6.2.5.19. TVD VLOCK Control Register1(Default Value: 0x0061_0220)

Offset: 0x0024			Register Name: TVD_VLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	Reserved
26:16	R/W	0x61	VACTIVE_HEIGHT
15	/	/	Reserved
14:4	R/W	0x22	VACTIVE_START

Offset: 0x0024			Register Name: TVD_VLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
3	/	/	Reserved
2:0	R/W	0x0	VTOL 000: 525 line 001: 625 line

6.2.5.20. TVD VLOCK Control Register2(Default Value: 0x000E_0070)

Offset: 0x0028			Register Name: TVD_VLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	Reserved
20:16	R/W	0xE	Hsync detector disable end line
15:7	/	/	Reserved
6:0	R/W	0x70	Hsync dectector disable start line

6.2.5.21. TVD Chroma Lock Control Register1(Default Value: 0x0046_3201)

Offset: 0x0030			Register Name: TVD_CLOCK1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	COLOR_STD_NTSC 0: NTSC358 1: NTSC443 Only valid when COLOR_STD set as NTSC
27:26	R/W	0x0	CHROMA_LPF 00: Narrow 01: Middle 10: Wide 11: Reserved
25	/	/	Reserved
24	R/W	0x0	wide_burst_gate 0: Narrow burst gate 1: Wide burst gate
23:16	R/W	0x46	Burst gate end time
15:8	R/W	0x32	Burst gate start time
7:4	/	/	Reserved
3:1	R/W	0x0	COLOR_STD 000: NTSC 001: PAL (I,B,G,H,D,N) 010: PAL (M) 011: PAL (CN) 100: SECAM
0	R/W	0x1	COLOR KILL EN 1: Disable color when chroma unlock

6.2.5.22. TVD Chroma Lock Control Register2(Default Value: 0x21F0_7C1F)

Offset: 0x0034			Register Name: TVD_CLOCK2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21F07C1F	C_SAMPLE_STEP C_SAMPLE_STEP = F_{sc}/Fin * 2^30

6.2.5.23. TVD YC Seperation Control Register1(Default Value: 0x0000_4209)

Offset: 0x0040			Register Name: TVD_YC_SEP1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	Reserved
29	R/W	0x0	CHROMA_CORING_ENABLE
28:26	R/W	0x0	3D_COMB_FACTOR
25:23	R/W	0x0	2D_COMB_FACTOR
22:20	R/W	0x0	NOTCH_FACTOR
19:17	/	/	Reserved
16	R/W	0x0	COMB_FILTER_BUFFER_CLEAR 0: not clear 1: clear
15:10	R/W	0x10	PAL_CHROMA_LEVEL Chroma level threshold for chroma comb filter select
9	R/W	0x1	CHROMA_BANDPASS_FILTER_EN
8	R/W	0x0	SECAM_NOTCH_WIDE Notch bandwidth 0: narraw 1: wide
7:4	R/W	0x0	2D_COMB_FILTER_MODE For NTSC 0000: 2D comb 0001,0010: Reserved 0011: 1D comb 0100,0101,0110,0111,1000: Reserved For PAL 0= 2D comb filter1 1= 1D comb filter1 2= 2D comb filter2 3= 1D comb filter2 4= 1D comb filter3 5=Reserved 6= 2D comb filter3 7,8= Reserved
3	R/W	0x1	3D_COMB_FILTER_DIS 0: Enable 3D comb filter 1: Disable 3D comb filter
2:0	R/W	0x1	3D_COMB_FILTER_MODE 000: 2D mode 001: 3D YC separation mode1

Offset: 0x0040			Register Name: TVD_YC_SEP1
Bit	**Read/Write**	**Default/Hex**	**Description**
			010,011: Reserved 100: 3D YC separation mode2

6.2.5.24. TVD YC Seperation Control Register2(Default Value: 0xFF00_00AF)

Offset: 0x0044			Register Name: TVD_YC_SEP2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	R/W	0x3	VERTICAL_NOISE_FACTOR
29:28	R/W	0x3	BURST_NOISE_FACTOR
27:26	R/W	0x3	CHROMA_NOISE_FACTOR
25:24	R/W	0x3	LUMA_NOISE_FACTOR
23:17	R/W	0x32	NOISE_THRESHOLD
16	R/W	0x0	NOISE_DETECT_EN
15:9	R/W	0x20	MOTION_DETECT_NOISE_THRESHOLD
8	R/W	0x0	MOTION_DETECT_NOISE_DETECT_EN
7:6	R/W	0x2	CHROMA_VERTICAL_FILTER_GAIN
5:4	R/W	0x2	LUMA_VERTICAL_FILTER_GAIN
3:2	R/W	0x3	HORIZONTAL_CHROMA_FILTER_GAIN
1:0	R/W	0x3	HORIZONTAL_LUMA_FILTER_GAIN

6.2.5.25. TVD Enhancement Control Register1(Default Value: 0x1420_8000)

Offset: 0x0050			Register Name: TVD_ENHANCE1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	Reserved
29:28	R/W	0x1	SHARP_COEF2
27:25	R/W	0x2	SHARP_COEF1 Y_{sharp} = Y + YH *(SHARP_COEF1/SHARP_COEF2)
24	R/W	0x0	SHARP_EN 0: Disable 1: Enable
23:16	R/W	0x20	BRIGHT_OFFSET Set 0x00, brightness offset is -32. Set 0x20, brightness offset is 0. Set 0xFF, brightness offset is max.
15:8	R/W	0x80	CONTRAST_GAIN Set 0x00, contrast gain is min. Set 0x80, contrast gain is 1. Set 0xFF, contrast gain is max.
7:4	/	/	Reserved
3:0	R/W	0x0	YC_DELAY 0000: Y and C no delay 0001: Y delay 1 cycle to C 0010: Y delay 2 cycle to C 0011: Y delay 3 cycle to C 0100: Y delay 4 cycle to C

Offset: 0x0050			Register Name: TVD_ENHANCE1
Bit	Read/Write	Default/Hex	Description
			0101: Y delay 5 cycle to C 0110: Y delay 6 cycle to C 0111: Y delay 7 cycle to C 1000: Reserved 1001: Reserved 1010: Reserved 1011: C delay 5 cycle to Y 1100: C delay 4 cycle to Y 1101: C delay 3 cycle to Y 1110: C delay 2 cycle to Y 1111: C delay 1 cycle to Y

6.2.5.26. TVD Enhancement Control Register2(Default Value: 0x0000_0680)

Offset: 0x0054			Register Name: TVD_ENHANCE2
Bit	Read/Write	Default/Hex	Description
31:11	/	/	Reserved
10:9	R/W	0x3	CHROMA_ENHANCE_STRENGTH 00: mild 01: low 10: middle 11: high
8	R/W	0x0	CHROMA_ENHANCE_EN 0: disable 1: enable
7:0	R/W	0x80	SATURATION_GAIN Set 0x00, saturation gain is min. Set 0x80, saturation gain is 1. Set 0xFF, saturation gain is max.

6.2.5.27. TVD Enhancement Control Register3(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: TVD_ENHANCE3
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	CB_CR_GAIN_EN
27:16	R/W	0x0	CR_GAIN
15:12	/	/	/
11:0	R/W	0x80	CB_GAIN

6.2.5.28. TVD WB DMA Control Register1(Default Value: 0x02D0_0020)

Offset: 0x0060			Register Name: TVD_WB1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	Reserved
27:16	R/W	0x2D0	HACTIVE_STRIDE

Offset: 0x0060			Register Name: TVD_WB1
Bit	**Read/Write**	**Default/Hex**	**Description**
			Horizontal active line stride.
15:9	/	/	Reserved
8	R/W	0x0	WB_ADDR_VALID 0: invalid 1: valid
7	/	/	Reserved
6	R/W	0x0	flip_field This bit flips even/odd fields
5	R/W	0x1	WB_FRAME_MODE 0: odd field or even field(desided by bit2) 1: frame
4	R/W	0x0	WB_MB_MODE 0: planar mode 1: mb mode
3	R/W	0x0	hyscale en
2	R/W	0x0	FIELD_SEL 0: field 0 only 1: filed 1 only
1	R/W	0x0	WB_FORMAT 0: YUV420 1: YUV422
0	R/W	0x0	WB_EN 0: disable 1: enable

6.2.5.29. TVD WB DMA Control Register2(Default Value: 0x00F0_02D0)

Offset: 0x0064			Register Name: TVD_WB2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	Reserved
26:16	R/W	0xF0	VACTIVE_NUM Vertical active line number.
15:12	/	/	Reserved
11:0	R/W	0x2D0	HACTIVE_NUM Horizontal active pixel number.

6.2.5.30. TVD WB DMA Control Register3(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: TVD_WB3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CH1_Y_ADDR

6.2.5.31. TVD WB DMA Control Register4(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: TVD_WB4
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CH1_C_ADDR

6.2.5.32. TVD DMA Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: TVD_IRQ_CTL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	FIFO_3D_TX_O_EN 0: IRQ disable 1: IRQ enable
30	R/W	0x0	FIFO_3D_TX_U_EN 0: IRQ disable 1: IRQ enable
29	R/W	0x0	FIFO_3D_RX_O_EN 0: IRQ disable 1: IRQ enable
28	R/W	0x0	FIFO_3D_RX_U_EN 0: IRQ disable 1: IRQ enable
27:25	/	/	Reserved
24	R/W	0x0	CHANNEL1_FRAME_END
23:9	/	/	Reserved
8	R/W	0x0	FIFO_Y_U_EN 0: IRQ disable 1: IRQ enable
7	R/W	0x0	FIFO_PB_U_EN 0: IRQ disable 1: IRQ enable
6	R/W	0x0	FIFO_PR_U_EN 0: IRQ disable 1: IRQ enable
5	R/W	0x0	FIFO_Y_O_EN 0: IRQ disable 1: IRQ enable
4	R/W	0x0	FIFO_PB_O_EN 0: IRQ disable 1: IRQ enable
3	R/W	0x0	FIFO_PR_O_EN 0: IRQ disable 1: IRQ enable
2	/	/	Reserved

Offset: 0x0080			Register Name: TVD_IRQ_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
1	R/W	0x0	UNLOCK_EN 0: IRQ disable 1: IRQ enable
0	R/W	0x0	LOCK_EN 0: IRQ disable 1: IRQ enable

6.2.5.33. TVD DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TVD_IRQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W1C	0x0	FIFO_3D_TX_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
30	R/W1C	0x0	FIFO_3D_TX_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
29	R/W1C	0x0	FIFO_3D_RX_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
28	R/W1C	0x0	FIFO_3D_RX_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
27:25	/	/	/
24	R/W1C	0x0	FRAME_FINISH_FLAG This bit automatically set every write back frame. Set 0x1 to clear this bit.
23:17	/	/	/
16	R/W	0x0	WB_ADDR_CHANGE_ERR Write back address change error
15:9	/	/	/
8	R/W1C	0x0	FIFO_Y_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
7	R/W1C	0x0	FIFO_C_U 0: FIFO work normal 1: FIFO underflow Write 0x1 to clear this bit.
6	/	/	/
5	R/W1C	0x0	FIFO_Y_O

Offset: 0x0090			Register Name: TVD_IRQ_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
4	R/W1C	0x0	FIFO_C_O 0: FIFO work normal 1: FIFO overflow Write 0x1 to clear this bit.
3:2	/	/	/
1	R/W	0x0	UNLOCK 0: TVD status no change 1: TVD status change from lock to unlock
0	R/W	0x0	LOCK 0: TVD status no change 1: TVD status change from unlock to lock

6.2.5.34. TVD Debug Control Register1(Default Value: 0x0010_0000)

Offset: 0x0100			Register Name: TVD_DEBUG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	R/W	0x0	CLAMP_UPDN_CYCLES
24	R/W	0x0	CLAMP_DN_START Write 0x1 to make clamp up, clamp up value is determined by **CLAMP_UPDN_CYCLES**. Note that this bit is only valid when **CLAMP_MODE** is set as 0x1.
23	R/W	0x0	CLAMP_UP_START Write 0x1 to make clamp up, clamp up value is determined by **CLAMP_UPDN_CYCLES**. Note that this bit is only valid when **CLAMP_MODE** is set as 0x1.
22	R/W	0x0	CLAMP_MODE 0: normal, auto clamp control 1: debug mode, clamp control by register
21	R/W	0x0	AFE_GAIN_MODE 0: auto gain mode 1: debug mode, AFE gain is determined by **AFE_GAIN_VALUE.**
20	R/W	0x1	UNLOCK_RESET_GAIN_ENABLE
19	R/W	0x0	TRUNCATION_RESET_GAIN_ENABLE
18	R/W	0x0	TRUNCATION2_RESET_GAIN_ENABLE
17	R/W	0x0	TVIN LOCK_HIGH
16	R/W	0x0	TVIN LOCK_DEBUG
15:8	R/W	0x0	AFE_GAIN_VALUE
7:0	/	/	/

6.2.5.35. TVD Debug Status Register1(Default Value: 0x0000_0000)

Offset: 0x0180	Register Name: TVD_STATUS1

Bit	Read/Write	Default/Hex	Description
31:24	/	/	Reserved
23:16	R	0x0	CHROMA_MAGNITUDE_STATUS These bits contain the chroma magnitude.
15:8	R	0x0	AGC_DIGITAL_GAIN_STATUS These bits contain the digital AGC gain value.
7:0	R	0x0	AGC_ANALOG_GAIN_STATUS These bits contain the analog AGC gain value.

6.2.5.36. TVD Debug Status Register2(Default Value: 0x0000_0000)

Offset: 0x0184			Register Name: TVD_STATUS2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	CHROMA_SYNC_DTO_INCREMENT_STATUS

6.2.5.37. TVD Debug Status Register3(Default Value: 0x0000_0000)

Offset: 0x0188			Register Name: TVD_STATUS3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	Reserved
29:0	R	0x0	HORIZONTAL_SYNC_DTO_INCREMENT_STATUS

6.2.5.38. TVD Debug Status Register4(Default Value: 0x0000_0001)

Offset: 0x018C			Register Name: TVD_STATUS4
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	Reserved
23	R	0x0	VCR_REW VCR Rewind Detected
22	R	0x0	VCR_FF VCR Fast-Forward Detected
21	R	0x0	VCR_TRICK VCR Trick-Mode Detected
20	R	0x0	VCR VCR Detected
19	R	0x0	NOISY Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the “noise_thresh” register (05h).
18	R	0x0	625LINES_DETECTED 625 Scan Lines Detected
17	R	0x0	SECAM_DETECTED SECAM Colour Mode Detected
16	R	0x0	PAL_DETECTED PAL Colour Mode Detected
15:11	R	0x0	Reserved
10	R	0x0	VNON_STANDARD Vertical frequency non-standard input signal Detected
9	R	0x0	HNON_STANDARD Horizontal frequency non-standard input signal Detected
8	R	0x0	PROSCAN_DETECTED

Offset: 0x018C			Register Name: TVD_STATUS4
Bit	**Read/Write**	**Default/Hex**	**Description**
			Progressive Scan Detected
7:5	R	0x0	MACROVISION_COLOUR_STRIPES_DETECTED. The number indicates the number of colour stripe lines in each group
4	R	0x0	MACROVISION_VBI_PSEUDO-SYNC_PULSES_DETECTION 1: Detected 0: Undetected
3	R	0x0	CHROMA_PLL_LOCKED_TO_COLOUR_BURST 1: Locked 0: Unlocked
2	R	0x0	VERTICAL_LOCK 1: Locked 0: Unlocked
1	R	0x0	HORIZONTAL_LINE_LOCKED 1: Locked 0: Unlocked
0	R	0x1	NO_SIGNAL_DETECTION 1: No Signal Detected 0: Signal Detected

6.2.5.39. TVD Debug Status Register5(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: TVD_STATUS5
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	R	0	BLANK_LEVEL
21:12	R	0	SYNC_LEVEL
11	R/W	0x0	ADC_DATA_SHOW
10	/	/	/
9:0	R	0x0	ADC_DATA_VALUE

6.2.5.40. TVD Debug Status Register6(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: TVD_STATUS6
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	MASK_UNKNOWN
9	R/W	0x0	MASK_SECAM
8	R/W	0x0	MASK_NTSC443
7	R/W	0x0	MASK_PAL60
6	R/W	0x0	MASK_PALCN
5	R/W	0x0	MASK_PALM
4	R/W	0x0	AUTO_DETECT_EN 0: disable 1: enable
3:1	R	0x0	TV STANDARD

Offset: 0x0194			Register Name: TVD_STATUS6
Bit	**Read/Write**	**Default/Hex**	**Description**
			001: V525_NTSC 010: V625_PAL 011: V525_PALM 100: V625_PALN 101: V525_PAL60 110: V525_NTSC443 111: V625_SECAM
0	R	0x0	AUTO_DETECT_FINISH

Chapter 7. Display

This chapter provides a detailed description of the display feature of A40i processor from following aspects.

- DE2.0
- TCON
- HDMI
- MIPI DSI
- TV Encoder

Here is the application block diagram of display module.

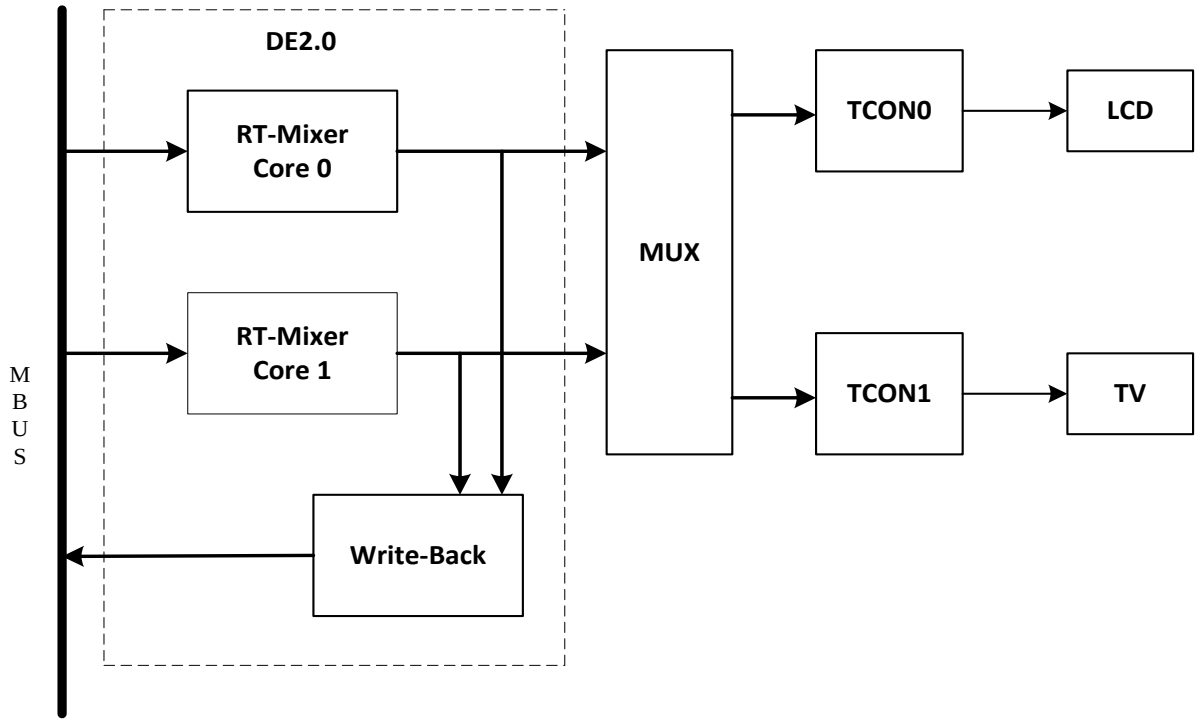


Figure 7-1. Display Module Block Diagram

7.1. DE2.0

- Supports output size up to 2048 x 2048
- Supports four alpha blending channels for main display, two channels for aux display
- Supports four overlay layers in each channel, and has an independent scaler
- Supports potter-duff compatible blending operation
- Supports motion-adaptive de-interlacer for 480i, 576i and 1080i inputs
- Supports input format YUV422/YUV420/YUV411/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555 and RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports SmartColor2.0 for excellent display experience
  - Adaptive edge sharping
  - Adaptive color enhancement
  - Adaptive contrast enhancement and fresh tone rectify
- Supports SmartColor2.0 for excellent display experience

For complete DE information, refer to the ***Allwinner A40i DE Specification***.

7.2. TCON

7.2.1. Overview

Features:

- Supports dual LVDS interface with single/dual link, up to 1920x1080@60fps
- Supports RGB interface with DE/SYNC mode, up to 1920x1080@60fps
- Supports serial RGB/dummy RGB/CCIR656 interface, up to 800x480@60fps
- Supports i80 interface with 18/16/9/8 bits, up to 800x480@60fps
- Supports HDMI 1.4 transmitter with HDCP 1.2, up to 1080p@60fps
- Supports 4 lanes MIPI DSI up to 1080p@60fps
- Supports TV output
- Supports CCIR656 interface for NTSC and PAL
- Dither function for RGB666/RGB565/RGB888
- Gamma correction with R/G/B channel independence

7.2.2. Block Diagram

TCON has two controllers including TCON0 for LCD and TCON1 for TV.

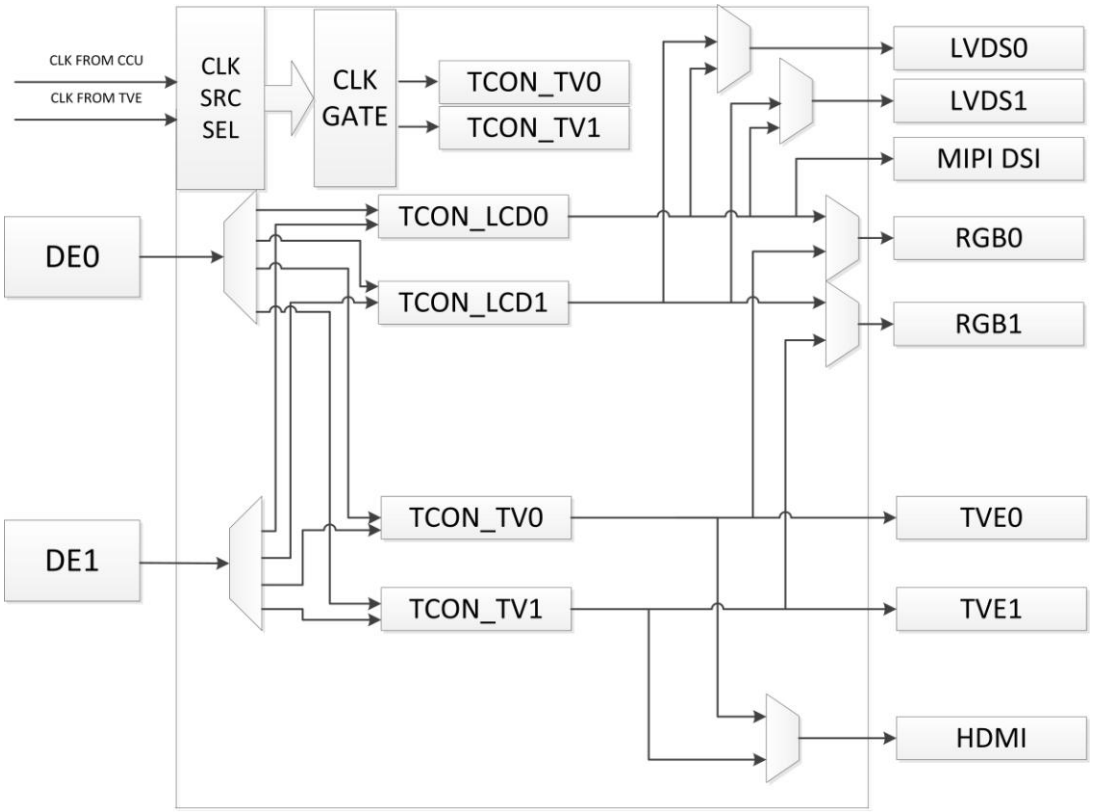


Figure 7-2. TCON Top Block Diagram

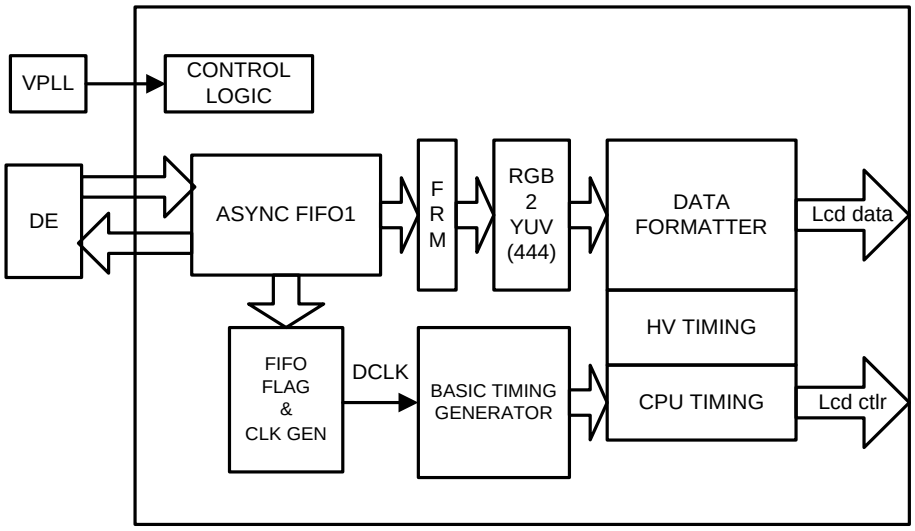


Figure 7-3. TCON_LCD Block Diagram

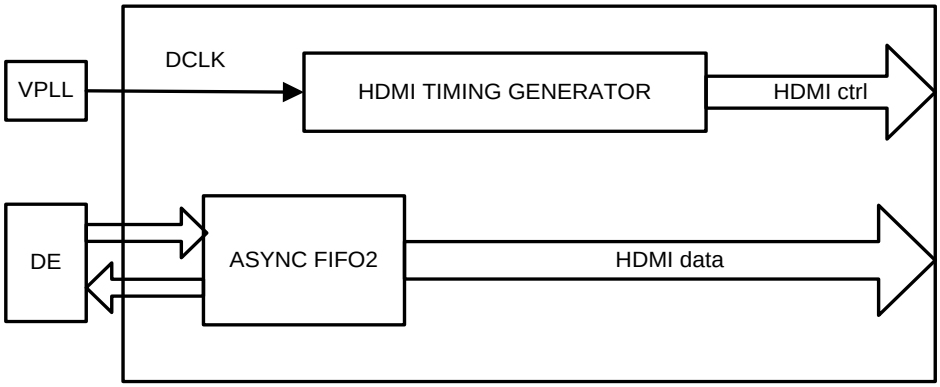


Figure 7-4. TCON_TV Block Diagram

7.2.3. Operations and Functional Descriptions

7.2.3.1. Panel Interface

(1) HV_I/F(Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications. Its signals are defined as:

Table 7-1. HV Panel Signals

Signal	Description	Type
Vsync	Vertical sync, indicates one new frame	O
Hsync	Horizontal sync, indicate one new scan line	O

DCLK	Dot clock, pixel data are sync by this clock	O
LDE	LCD data enable	O
LD[23..0]	18Bit RGB/YUV output from input FIFO for panel	O

HV control signals are active low.

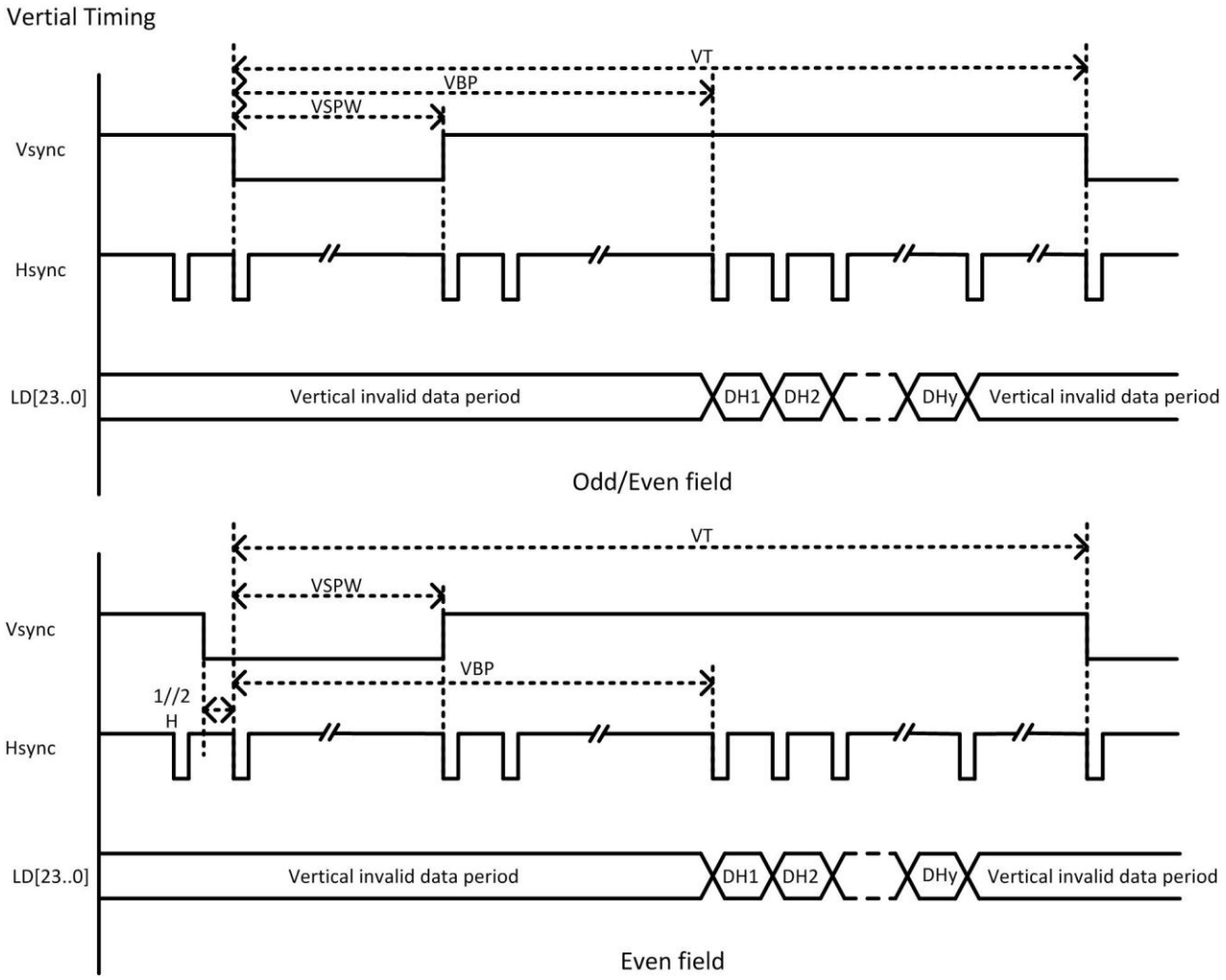


Figure 7-5. HV Interface Vertical Timing

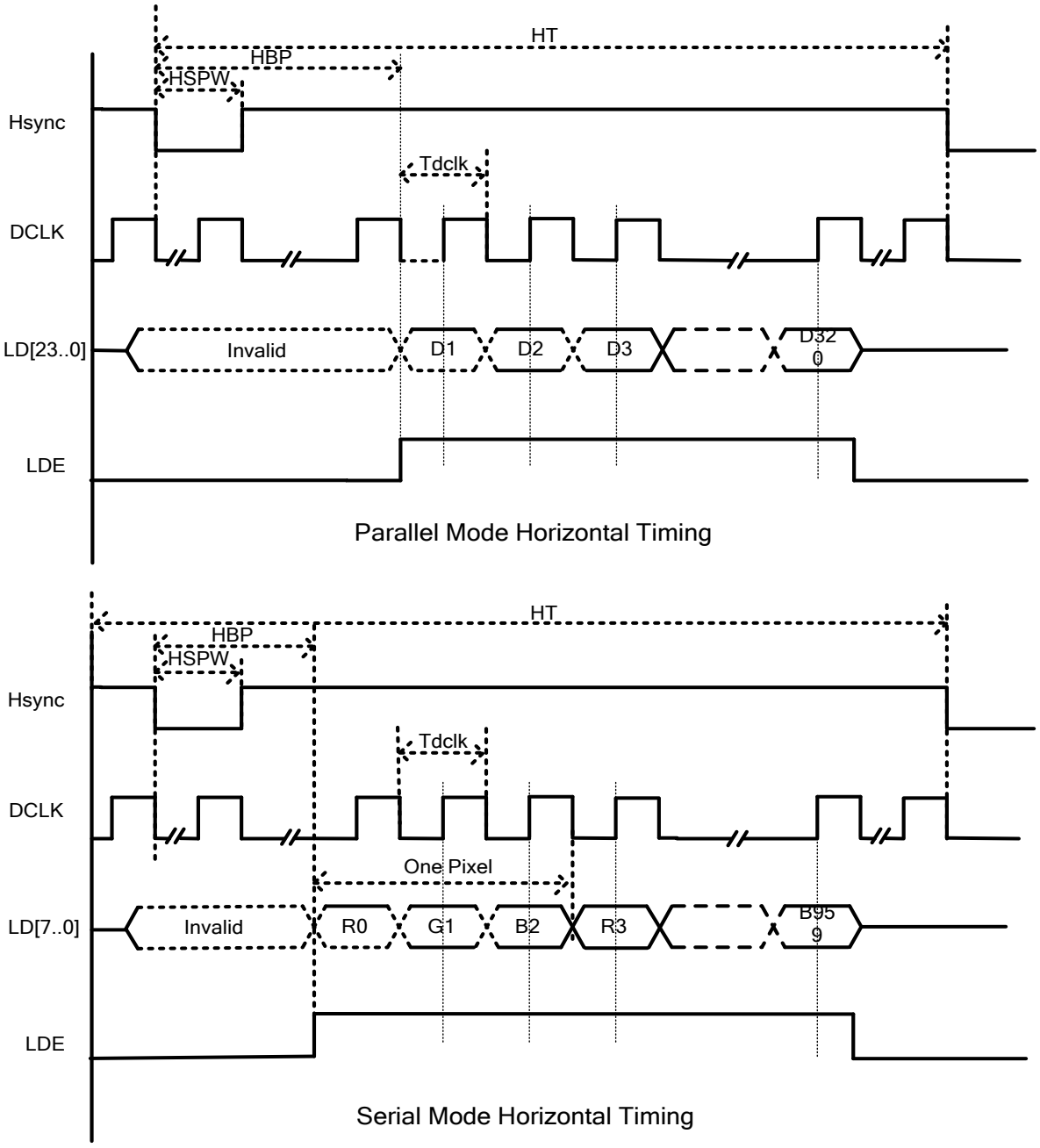


Figure 7-6. HV Interface Horizontal Timing

(2) CCIR output SAV/EAV sync signal

When in HV serial YUV output mode, its timing is CCIR656/601 compatible. SAV add right before active area every line; EAV add right after active area every line.

Its logic are:

F = “0” for Field 1 F = “1” for Field 2

V = “1” during vertical blanking

H = “0” at SAV H = “1” at EAV

P3-P0 = protection bits

P3 = V ⊕H

P2 = F ⊕H

P1 = F ⊕V

P0 = F ⊕V ⊕H

Where ⊕represents the exclusive-OR function

The 4 byte SAV/EAV sequences are:

Table 7-2. EAV and SAV Sequence

	8-bit Data								10-bit Data	
	D9 (MSB)	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

(3) CPU_I/F

CPU I/F LCD panel is most common interface for small size, low resolution LCD panels.

CPU control signals are active low.

Table 7-3. CPU Panel Signals

Main Signal	Description	Type
CS	Chip select, active low	O
WR	Write strobe, active low	O
RD	Read strobe, active low	O
A1	Address bit, controlled by "LCD_CPUI/F" BIT26/25	O
D[23..0]	Digital RGB output signal	I/O

The following figure relationship between basic timing and CPU timing. WR is 180 degree delay of DCLK; CS is active when pixel data are valid; RD is always set to 1; A1 is set by “**Lcd_CPUI/F**”.

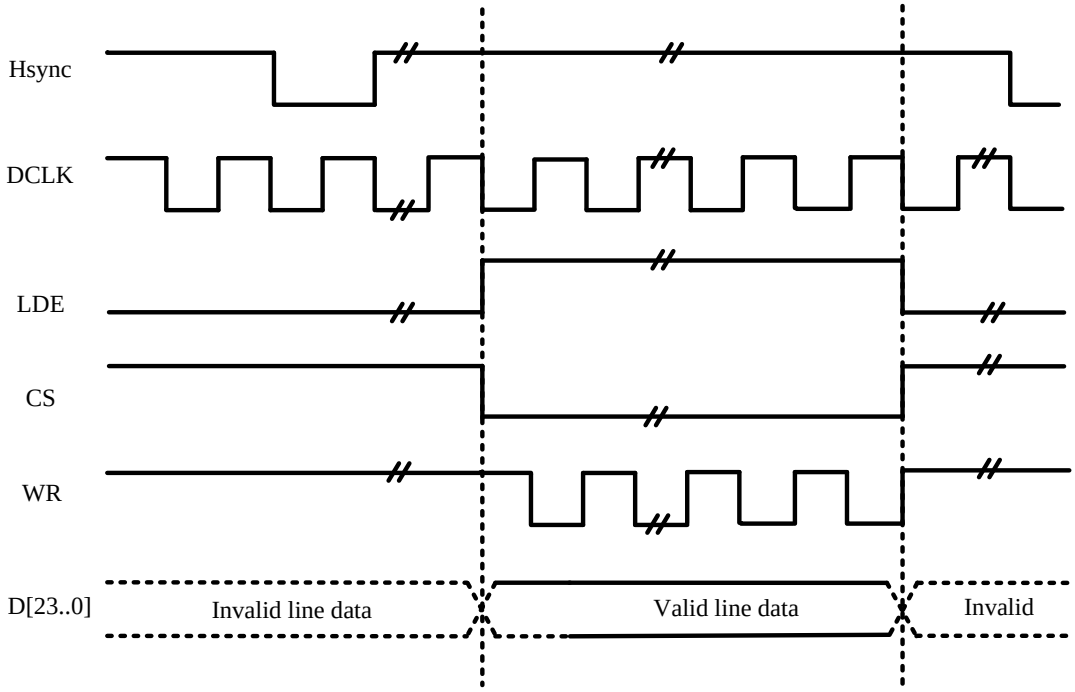


Figure 7-7. CPU Interface Timing

When CPU I/F is in IDLE state, it can generate WR/RD timing by setting "**Lcd_CPUI/F**". CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

7.2.3.2. LVDS Interface

(1) JEDIA mode

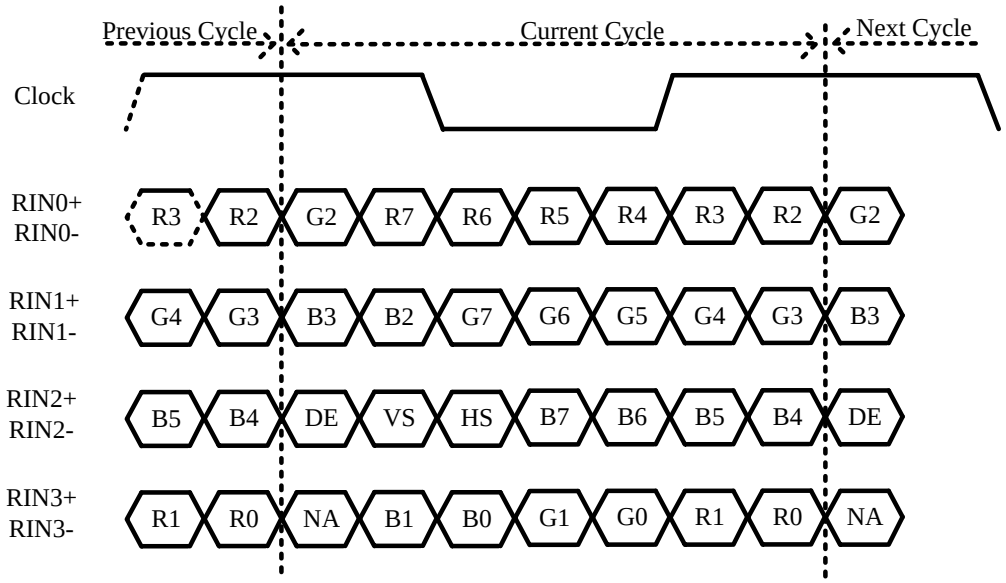


Figure 7-8. LVDS Single Link JEDIA Mode Interface Timing

(2) NS mode

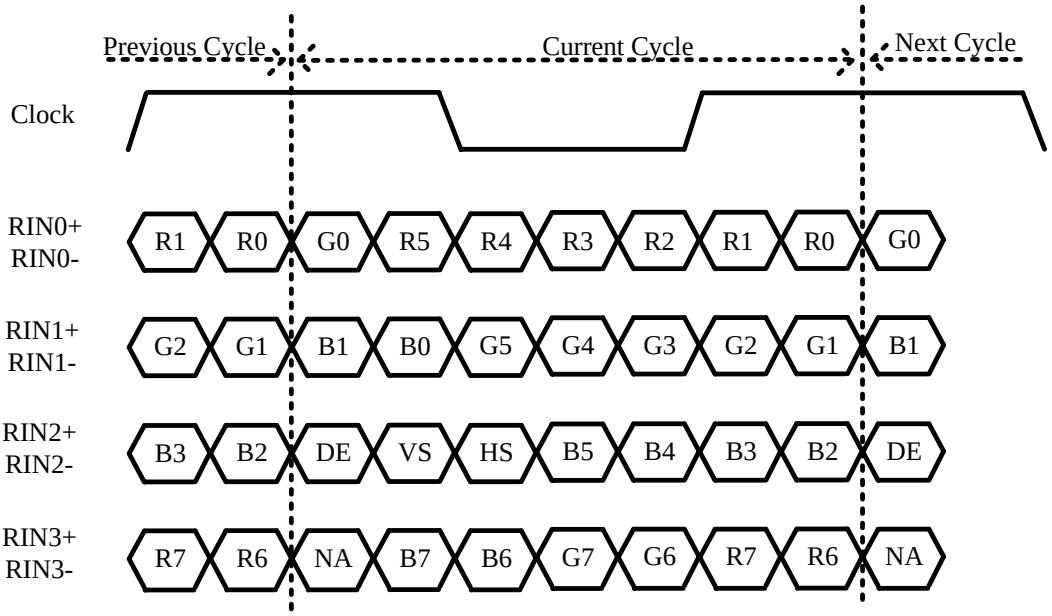


Figure 7-9. LVDS Single Link NS Mode Interface Timing

(3) Dual Links NS Mode

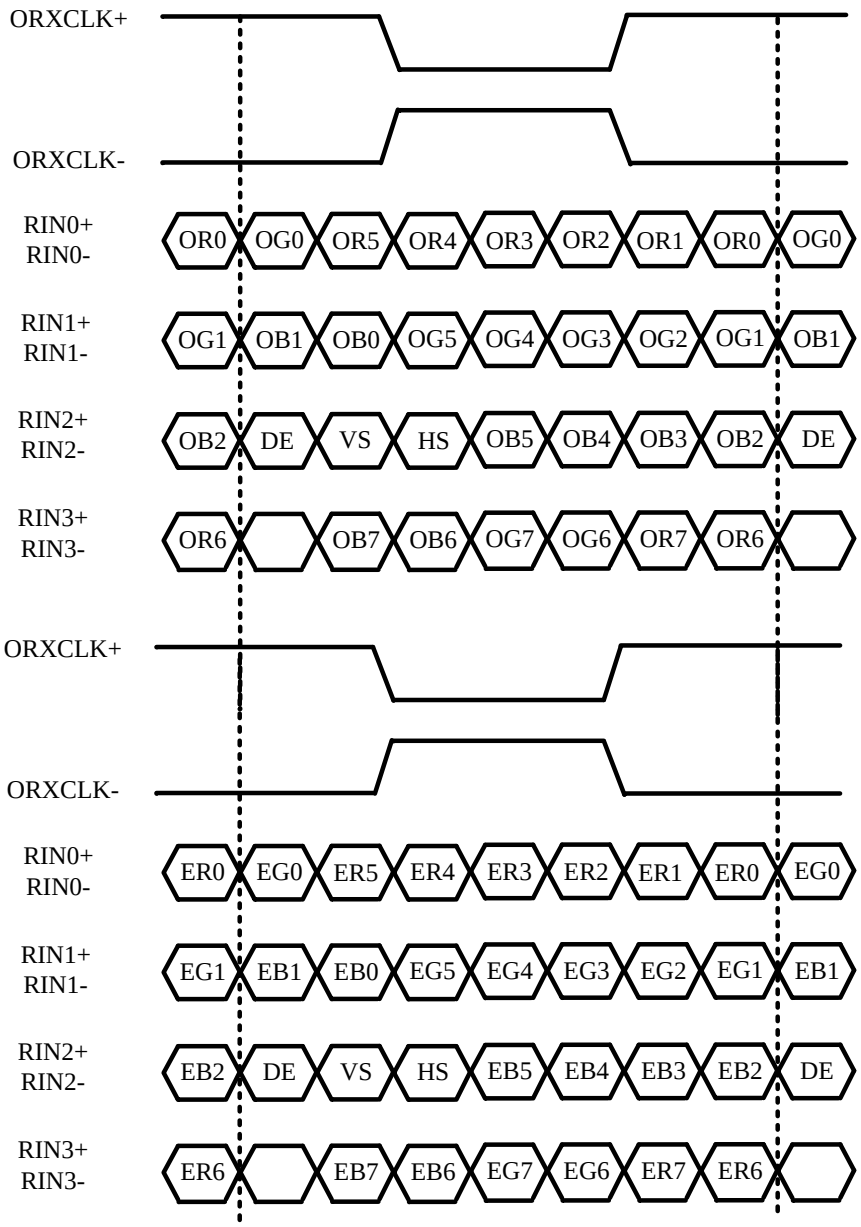


Figure 7-10. LVDS Dual Link NS Mode Interface Timing

7.2.3.3. RGB Gamma Correction

Function: This module corrects the RGB input data of DE0.

A 256*8*3 Byte register file is used to store the gamma table.

Table 7-4. RGB Gamma Correction Table

Offset	Value
0x400, 0x401, 0x402	{ B0[7:0], G0[7:0], R0[7:0] }
0x404,	{ B1[7:0], G1[7:0], R1[7:0] }
.....	.....
0x4FC	{ B255[7:0], G255[7:0], R255[7:0] }

7.2.3.4. CEU Module

Function: This module enhance color data from DE0.

R' = Rr*R + Rg*G + Rb*B + Rc
G' = Gr*R + Gg*G + Gb*B +Gc
B' = Br*R + Bg*G + Bb*B + Bc

Rr, Rg, Rb, ,Gr, Gg, Gb, Br, Bg, Bb s13(-16,16)
Rc, Gc, Bc s19 (-16384, 16384)
R, G, B u8 [0-255]
R' have the range of [Rmin ,Rmax]
G' have the range of [Rmin ,Rmax]
B' have the range of [Rmin ,Rmax]

7.2.3.5. CMAP Module

Function: This module map color data from DE.

Every 4 input pixels as an unit. an unit is divided into 12 bytes. Output byte can select one of those 12 bytes. Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduce to 6 bytes(2 pixels).

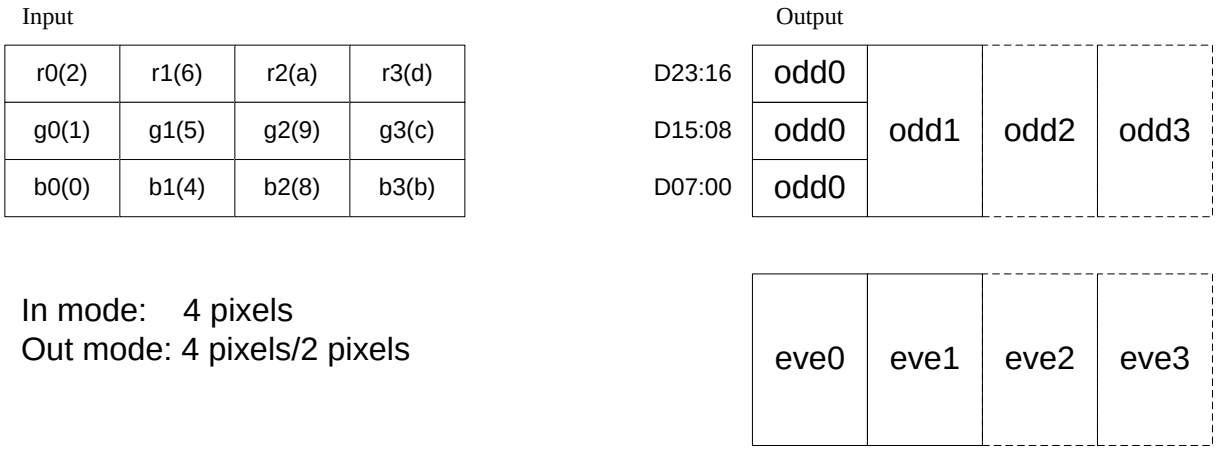


Figure 7-11. CMAP Module

7.2.4. BT656 Using Guides

7.2.4.1. BT656 Pinout

The RGB output can be multiplexed to BT656 output, so the pin correspondence between LCD0 and BT656 is as follows.

Table 7-5. BT656 Pinout

LCD Pin	BT656 Pin
LCD0_D3	VD0
LCD0_D4	VD1
LCD0_D5	VD2
LCD0_D6	VD3
LCD0_D7	VD4
LCD0_D10	VD5
LCD0_D11	VD6

LCD0_D12	VD7

7.2.4.2. Code Configuration

(1).1080p@30Hz: IO running clock = 148.5MHz
First, configure the frequency of TCON_LCD as 148.5MHz, and then configure the following registers.

```
tcon_lcd->lcd_hv_ctl->hv_mode = 12;          //Select BT656 output mode
tcon_lcd->lcd_hv_ctl->syuv_seq = 2;          //Set output sequence as UYVY. There can be selected as needed.
tcon_lcd->lcd_hv_ctl->f_line_dly = 0;        //Set to 0 in progressive scan mode
tcon_lcd->lcd_basic0->x = 1920-1;
tcon_lcd->lcd_basic0->y = 1080-1;
tcon_lcd->lcd_basic1->ht = 2200*2-1;
tcon_lcd->lcd_basic1->hbp = 192*2-1;
tcon_lcd->lcd_basic2->vt = 1125*2;
tcon_lcd->lcd_basic2->vbp = 41-1;
tcon_lcd->lcd_basic3->hspw = 44*2-1;
tcon_lcd->lcd_basic3->vspw = 5-1;
```

The rest of the configuration conforms to RGB mode.

(2).720p@30Hz: IO running clock = 74.25MHz
First, configure the frequency of TCON_LCD as 74.25MHz, and then configure the following registers.

```
tcon_lcd->lcd_hv_ctl->hv_mode = 12;          //Select BT656 output mode
tcon_lcd->lcd_hv_ctl->syuv_seq = 2;          //Set output sequence as UYVY. There can be selected as needed
tcon_lcd->lcd_hv_ctl->f_line_dly = 0;        //Set to 0 in progressive scan mode
tcon_lcd->lcd_basic0->x = 1280-1;
tcon_lcd->lcd_basic0->y = 800-1;
tcon_lcd->lcd_basic1->ht = 1650*2-1;
tcon_lcd->lcd_basic1->hbp = 260*2-1;
tcon_lcd->lcd_basic2->vt = 750*2;
tcon_lcd->lcd_basic2->vbp = 25-1;
tcon_lcd->lcd_basic3->hspw = 40*2-1;
tcon_lcd->lcd_basic3->vspw = 5-1;
```

The rest of the configuration conforms to RGB mode.

(3).720p@60Hz: IO running clock = 148.5MHz
First, configure the frequency of TCON_LCD as 148.5MHz, and then configure the following registers.

```
tcon_lcd->lcd_hv_ctl->hv_mode = 12;          //Select BT656 output mode
tcon_lcd->lcd_hv_ctl->syuv_seq = 2;          //Set output sequence as UYVY. There can be selected as needed
tcon_lcd->lcd_hv_ctl->f_line_dly = 0;        //Set to 0 in progressive scan mode
tcon_lcd->lcd_basic0->x = 1280-1;
tcon_lcd->lcd_basic0->y = 800-1;
tcon_lcd->lcd_basic1->ht = 1650*2-1;
tcon_lcd->lcd_basic1->hbp = 260*2-1;
tcon_lcd->lcd_basic2->vt = 750*2;
tcon_lcd->lcd_basic2->vbp = 25-1;
tcon_lcd->lcd_basic3->hspw = 40*2-1;
tcon_lcd->lcd_basic3->vspw = 5-1;
```

The rest of the configuration conforms to RGB mode.

(4).NTSC@59.94Hz: IO running clock = 27MHz
First, configure the frequency of TCON_LCD as 27MHz, and then configure the following registers.

```
tcon_lcd->lcd_hv_ctl->hv_mode = 12;          //Select BT656 output mode
tcon_lcd->lcd_hv_ctl->syuv_seq = 2;          //Set output sequence as UYVY. There can be selected as needed
tcon_lcd->lcd_hv_ctl->f_line_dly = 3;        //Set to 3 in NTSC mode
tcon_lcd->lcd_basic0->x = 720-1;
```



```
tcon_lcd->lcd_basic0->y = 480-1;
tcon_lcd->lcd_basic1->ht = 858*2-1;
tcon_lcd->lcd_basic1->hbp = 122*2-1;
tcon_lcd->lcd_basic2->vt = 525;
tcon_lcd->lcd_basic2->vbp = 18-1;
tcon_lcd->lcd_basic3->hspw = 62*2-1;
tcon_lcd->lcd_basic3->vspw = 3-1;
```

The rest of the configuration conforms to RGB mode.

(5).PAL@50Hz: IO running clock = 27MHz

First, configure the frequency of TCON_LCD as 27MHz, and then configure the following registers.

```
tcon_lcd->lcd_hv_ctl->hv_mode = 12;          //Select BT656 output mode
tcon_lcd->lcd_hv_ctl->syuv_seq = 2;          //Set output sequence as UYVY. There can be selected as needed
tcon_lcd->lcd_hv_ctl->f_line_dly = 2;        //Set to 2 in PAL mode
tcon_lcd->lcd_basic0->x = 720-1;
tcon_lcd->lcd_basic0->y = 576-1;
tcon_lcd->lcd_basic1->ht = 864*2-1;
tcon_lcd->lcd_basic1->hbp = 132*2-1;
tcon_lcd->lcd_basic2->vt = 625;
tcon_lcd->lcd_basic2->vbp = 22-1;
tcon_lcd->lcd_basic3->hspw = 64*2-1;
tcon_lcd->lcd_basic3->vspw = 3-1;
```

The rest of the configuration conforms to RGB mode.

NOTE

The phase of the output clock(DCLK) needs to be configured according to the requirements of the BT656 receiver. Please check the datasheet of the BT656 receiver chip to confirm that the data sampling occurs on the rising edge or the falling edge, and then configure the output phase of the DCLK to ensure that the data can be sampled correctly.

7.2.4.3. Application Case

Taking PT1000K as an example, describe the schematic design method of BT656 to AHD.

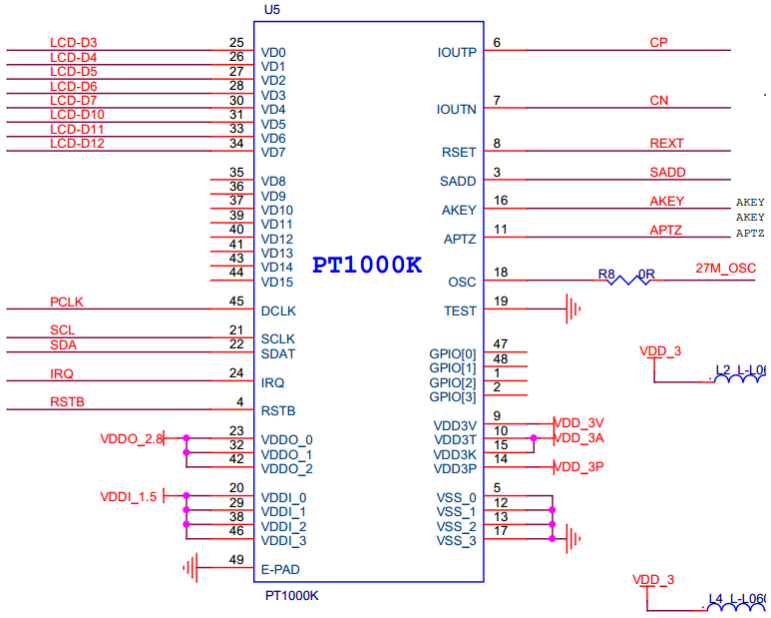


Figure 7-12. PT1000K Schematic Connection

The above diagram shows the schematic connection for PT1000K. Note the correspondence between LCD-Dx and VDx.

At the same time, it should be noted that the clock homology of PT1000K is very strict, so PCLK and 27M_OSC must be homologous.

In the T3, PCLK uses DCLK of TCON_LCD0, OSC_27M uses DCLK of TCON_LCD1. The software driver opens TCON_LCD0 normally and configures to output BT656 signals. Then TCON_LCD1 output clock of 27MHz is configured and output through PH24, the 27MHz output clock is as the input of OSC_27M at the same time. TCON_LCD0 and TCON_LCD1 need the same PLL.

Other BT656 external chips are used similarly and need to be adjusted according to the datasheet of the external chip.

7.2.5. Register List

Module Name	Base Address
TCON_TOP	0x01C70000
TCON_LCD0	0x01C71000
TCON_LCD1	0x01C72000
TCON_TV0	0x01C73000
TCON_TV1	0x01C74000

Register Name	Offset	Description
TCON_TOP		
TCON_TV_SETUP	0x0000	Setup TV CLK Source and Select GPIO to Output
DE_PORT_PERH_SEL	0x001C	Select Data Source of 4 TCONs
TCON_CLK_GATE_AND_HDMI_SRC_SEL	0x0020	Setup TV and DSI CLK Gating and Select Data Source of HDMI
TCON_LCD0,TCON_LCD1		
TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON0_FRM_CTL_REG	0x0010	TCON FRM Control Register
TCON0_FRM_SEED_REG	0x0014+N*0x04	TCON FRM Seed Register (N=0,1,2,3,4,5)
TCON0_FRM_TAB_REG	0x002C+N*0x04	TCON FRM Table Register (N=0,1,2,3)
TCON0_3D_FIFO_REG	0x003C	TCON0 3D FIFO Register
TCON0_CTL_REG	0x0040	TCON0 Control Register
TCON0_DCLK_REG	0x0044	TCON0 Data Clock Register
TCON0_BASIC0_REG	0x0048	TCON0 Basic Timing Register0
TCON0_BASIC1_REG	0x004C	TCON0 Basic Timing Register1
TCON0_BASIC2_REG	0x0050	TCON0 Basic Timing Register2
TCON0_BASIC3_REG	0x0054	TCON0 Basic Timing Register3
TCON0_HV_IF_REG	0x0058	TCON0 HV Panel Interface Register
TCON0_CPU_IF_REG	0x0060	TCON0 CPU Panel Interface Register
TCON0_CPU_WR_REG	0x0064	TCON0 CPU Panel Write Data Register
TCON0_CPU_RD0_REG	0x0068	TCON0 CPU Panel Read Data Register0
TCON0_CPU_RD1_REG	0x006C	TCON0 CPU Panel Read Data Register1
TCON0_IO_POL_REG	0x0088	TCON0 IO Polarity Register
TCON0_IO_TRI_REG	0x008C	TCON0 IO Control Register

Register Name	Offset	Description
TCON_DEBUG_REG	0x00FC	TCON Debug Register
TCON_CEU_CTL_REG	0x0100	TCON CEU Control Register
TCON_CEU_COEF_MUL_REG	0x0110+N*0x04	TCON CEU Coefficient Register0 (N=0,1,2,4,5,6,8,9,10)
TCON_CEU_COEF_ADD_REG	0x011C+N*0x10	TCON CEU Coefficient Register1 (N=0,1,2)
TCON_CEU_COEF_RANG_REG	0x0140+N*0x04	TCON CEU Coefficient Register2 (N=0,1,2)
TCON0_CPU_TRI0_REG	0x0160	TCON0 CPU Panel Trigger Register0
TCON0_CPU_TRI1_REG	0x0164	TCON0 CPU Panel Trigger Register1
TCON0_CPU_TRI2_REG	0x0168	TCON0 CPU Panel Trigger Register2
TCON0_CPU_TRI3_REG	0x016C	TCON0 CPU Panel Trigger Register3
TCON0_CPU_TRI4_REG	0x0170	TCON0 CPU Panel Trigger Register4
TCON0_CPU_TRI5_REG	0x0174	TCON0 CPU Panel Trigger Register5
TCON_CMAP_CTL_REG	0x0180	TCON Color Map Control register
TCON_CMAP_ODD0_REG	0x0190	TCON Color Map Odd Line Register0
TCON_CMAP_ODD1_REG	0x0194	TCON Color Map Odd Line Register1
TCON_CMAP_EVEN0_REG	0x0198	TCON Color Map Even Line Register0
TCON_CMAP_EVEN1_REG	0x019C	TCON Color Map Even Line Register1
TCON_SAFE_PERIOD_REG	0x01F0	TCON Safe Period Register
TCON0_LVDS_ANA0_REG	0x0220	TCON LVDS Analog Register0
TCON0_LVDS_ANA1_REG	0x0224	TCON LVDS Analog Register1
TCON0_GAMMA_TABLE_REG	0x0400-0x07FF	TCON Gamma Table Register
TCON0_3D_FIFO_BIST_REG	0x0FF4	TCON 3D FIFO Test Entry Address
TCON_TRI_FIFO_BIST_REG	0x0FF8	TCON TRI FIFO Test Entry Address
TCON_TV0,TCON_TV1		
TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON1_CTL_REG	0x0090	TCON1 Control Register
TCON1_BASIC0_REG	0x0094	TCON1 Basic Timing Register0
TCON1_BASIC1_REG	0x0098	TCON1 Basic Timing Register1
TCON1_BASIC2_REG	0x009C	TCON1 Basic Timing Register2
TCON1_BASIC3_REG	0x00A0	TCON1 Basic Timing Register3
TCON1_BASIC4_REG	0x00A4	TCON1 Basic Timing Register4
TCON1_BASIC5_REG	0x00A8	TCON1 Basic Timing Register5
TCON1_PS_SYNC_REG	0x00B0	TCON1 Sync Register
TCON1_IO_POL_REG	0x00F0	TCON1 IO Polarity Register
TCON1_IO_TRI_REG	0x00F4	TCON1 IO Control Register
TCON_ECC_FIFO_REG	0x00F8	TCON ECC FIFO Register
TCON_DEBUG_REG	0x00FC	TCON Debug Register
TCON_CEU_CTL_REG	0x0100	TCON CEU Control Register
TCON_CEU_COEF_MUL_REG	0x0110+N*0x04	TCON CEU Coefficient Register0 (N=0,1,2,4,5,6,8,9,10)
TCON_CEU_COEF_ADD_REG	0x011C+N*0x10	TCON CEU Coefficient Register1 (N=0,1,2)
TCON_CEU_COEF_RANG_REG	0x0140+N*0x04	TCON CEU Coefficient Register2 (N=0,1,2)
TCON_SAFE_PERIOD_REG	0x01F0	TCON Safe Period Register
TCON1_FILL_CTL_REG	0x0300	TCON1 Fill Data Control Register

Register Name	Offset	Description
TCON1_FILL_BEGIN_REG	0x0304+N*0x0C	TCON1 Fill Data Begin Register (N=0,1,2)
TCON1_FILL_END_REG	0x0308+N*0x0C	TCON1 Fill Data End Register (N=0,1,2)
TCON1_FILL_DATA0_REG	0x030C+N*0x0C	TCON1 Fill Data Value Register (N=0,1,2)
TCON1_GAMMA_TABLE_REG	0x0400-0x07FF	
TCON_ECC_FIFO_BIST_REG	0x0FFC	
TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON1_CTL_REG	0x0090	TCON1 Control Register
TCON1_BASIC0_REG	0x0094	TCON1 Basic Timing Register0
TCON1_BASIC1_REG	0x0098	TCON1 Basic Timing Register1
TCON1_BASIC2_REG	0x009C	TCON1 Basic Timing Register2
TCON1_BASIC3_REG	0x00A0	TCON1 Basic Timing Register3
TCON1_BASIC4_REG	0x00A4	TCON1 Basic Timing Register4
TCON1_BASIC5_REG	0x00A8	TCON1 Basic Timing Register5
TCON1_PS_SYNC_REG	0x00B0	TCON1 Sync Register

7.2.6. TCON_TOP Register Description

7.2.6.1. TCON TV Setup Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TCON_TV_SETUP_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	
12	R/W	0x0	TCON_TV1_OUTSEL 0: LCD1 output to GPIOH 1: TV1 output to GPIOH
11:9	/	/	
8	R/W	0x0	TCON_TV0_OUTSEL 0: LCD0 output to GPIOD 1: TV0 output to GPIOD
7:5	/	/	
4	R/W	0x0	TCON_TV1_CLK_SRC 0: Clock from CCU 1: Clock from TVE1
3:1	/	/	/
0	R/W	0x0	TCON_TV0_CLK_SRC 0: Clock from CCU 1: Clock from TVE0

7.2.6.2. DE Port Select Register(Default Value: 0x0000_0000)

Offset: 0x001C	Register Name: DE_PORT_SELECT_REG

Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:4	R/W	0x0	DE_PORT1 PERH Select. 00:TCON_LCD0 01:TCON_LCD1 10:TCON_TV0 11:TCON_TV1 The priority of DE0 is higher than DE1. If TCON_LCD0 selects DE0 and DE1 as source at the same time, then DE0 will be used for the source of TCON_LCD0.
3:2	/	/	/
1:0	R/W	0x0	DE_PORT0 PERH Select. 00:TCON_LCD0 01:TCON_LCD1 10:TCON_TV0 11:TCON_TV1 The priority of DE0 is higher than DE1. If TCON_LCD0 selects DE0 and DE1 as source at the same time, then DE0 will be used for the source of TCON_LCD0.

7.2.6.3. TCON Clock Gate and HDMI Source Select Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TCON_CLK_GATE_AND_HDMI_SRC_SEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	
29:28	R/W	0x0	HDMI Source select. 00:Disable 01:TCON_TV0 10:TCON_TV1 11:Reserved
27:25	/	/	/
24	R/W	0x0	TCON_TV1_CLK_GATE 0:Disable clk 1:Enable clk
23:21	/	/	/
20	R/W	0x0	TCON_TV0_CLK_GATE 0:Disable clk 1:Enable clk
19:17	/	/	/
16	R/W	0x0	DSI_CLK_GATE 0:Disable clk 1:Enable clk
15:0	/	/	/

7.2.7. TCON_LCD Register Description

7.2.7.1. TCON Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TCON_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON_EN 0: Disable 1: Enable When it's disabled, the module will be reset to idle state.
30	R/W	0x0	TCON_GAMMA_EN 0: Disable 1: Enable
29:1	/	/	/
0	R/W	0x0	IO_MAP_SEL 0: TCON0 1: TCON1 **NOTE** **This bit determined which IO_INV/IO_TRI are valid.**

7.2.7.2. TCON Global Interrupt Register0(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TCON_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON0_VB_INT_EN 0: Disable 1: Enable
30	/	/	/
29	R/W	0x0	TCON0_LINE_INT_EN 0: Disable 1: Enable
28	/	/	/
27	R/W	0x0	TCON0_TRI_FINISH_INT_EN 0: Disable 1: Enable
26:	R/W	0x0	TCON0_TRI_COUNTER_INT_EN 0: Disable 1: Enable
25:16	/	/	/
15	R/W0C	0x0	TCON0_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
14	/	/	/
13	R/W0C	0x0	TCON0_LINE_INT_FLAG Trigger when SY0 match the current TCON0 scan line Write 0 to clear it.
12	/	/	/

Offset: 0x0004			Register Name: TCON_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W0C	0x0	TCON0_TRI_FINISH_INT_FLAG Trigger when cpu trigger mode finish Write 0 to clear it.
10	R/W0C	0x0	TCON0_TRI_COUNTER_INT_FLAG Trigger when tri counter reaches this value Write 0 to clear it.
9	R/W0C	0x0	TCON0_TRI_UNDERFLOW_FLAG only used in dsi video mode, tri when sync by dsi but not finish. Write 0 to clear it.
8:0	/	/	/

7.2.7.3. TCON Global Interrupt Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TCON_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON0_LINE_INT_NUM scan line for TCON0 line trigger(including inactive lines) Setting it for the specified line for trigger0. **NOTE** **SY0 is writable only when LINE_TRG0 disable.**
15:0	/	/	/

7.2.7.4. TCON0 FRM Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: TCON0_FRM_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON0_FRM_EN 0:Disable 1:Enable
30:7	/	/	/
6	R/W	0x0	TCON0_FRM_MODE_R 0: 6-bit frm output 1: 5-bit frm output
5	R/W	0x0	TCON0_FRM_MODE_G 0: 6-bit frm output 1: 5-bit frm output
4	R/W	0x0	TCON0_FRM_MODE_B 0: 6-bit frm output 1: 5-bit frm output
3:2	/	/	/
1:0	R/W	0x0	TCON0_FRM_TEST 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM

			11: half 8bit, half 5/6bit

7.2.7.5. TCON0 FRM Seed Register(Default Value: 0x0000_0000)

Offset: 0x0014+N*0x04(N=0,1,2,3,4,5)			Register Name: TCON0_FRM_SEED_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:0	R/W	0x0	SEED_VALUE N=0: Pixel_Seed_R N=1: Pixel_Seed_G N=2: Pixel_Seed_B N=3: Line_Seed_R N=4: Line_Seed_G N=5: Line_Seed_B **NOTE** **Avoid setting it to 0.**

7.2.7.6. TCON0 FRM Table Register(Default Value: 0x0000_0000)

Offset: 0x002C+N*0x04(N=0,1,2,3)			Register Name: TCON0_FRM_TAB_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FRM_TABLE_VALUE

7.2.7.7. TCON0 3D FIFO Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: TCON0_3D_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	3D_FIFO_BIST_EN 0: Disable 1: Enable
30:14	/	/	/
13:4	R/W	0x0	3D_FIFO_HALF_LINE_SIZE The number of data in half line=3D_FIFO_HALF_LINE_SIZE+1. Only valid when 3D_FIFO_SETTING set as 2
3:2	/	/	/
1:0	R/W	0x0	3D_FIFO_SETTING 00: by pass 01: used as normal FIFO 10: used as 3D interlace FIFO 11: reserved

7.2.7.8. TCON0 Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TCON0_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

31	R/W	0x0	TCON0_EN 0: Disable 1: Enable **NOTE** **It executes at the beginning of the first blank line of TCON0 timing.**
30:29	/	/	/
28	R/W	0x0	TCON0_WORK_MODE 0: Normal 1: Dynamic freq
27:26	/	/	/
25:24	R/W	0x0	TCON0_IF 00: HV(Sync+DE) 01: 8080 I/F 1x: Reservd
23	R/W	0x0	TCON0_RB_SWAP 0: Default 1: Swap RED and BLUE data at FIFO1
22	R/W	0x0	TCON0_TEST_VALUE 0:all 0s 1:all 1s
21	R/W	0x0	TCON0_FIFO1_RST Writing 1 and then 0 at this bit will reset FIFO 1 **NOTE** **1 holding time must more than 1 DCLK.**
20	R/W	0x0	TCON0_INTERLACE_EN 0:Disable 1:Enable This flag is valid only when TCON0_EN = 1
19:9	/	/	/
8:4	R/W	0x0	TCON0_START_DELAY STA delay This flag is valid only when TCON0_EN = 1
3	/	/	/
2:0	R/W	0x0	TCON0_SRC_SEL 000: DE0 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Test Data all 0 101: Test Data all 1 111: Gridding Check

7.2.7.9. TCON0 Data Clock Register(Default Value: 0x0000_0000)

Offset: 0x0044	**Register Name: TCON0_DCLK_REG**

Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x0	TCON0_DCLK_EN LCLK_EN[3:0] :TCON0 clock enable 4'h0, 'h4,4'h6,4'ha7:dclk_en=0;dclk1_en=0;dclk2_en=0;dclkm2_en=0; 4'h1: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0; 4'h2: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1; 4'h3: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0; 4'h5: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0; 4'h8,4'h9,4'ha,4'hb,4'hc,4'hd,4'he,4'hf: dclk_en = 1; dclk1_en = 1; dclk2_en = 1; dclkm2_en = 1;
27:7	/	/	/
6:0	R/W	0x0	TCON0_DCLK_DIV Tdclk = Tsclk * DCLKDIV If dclk1&dclk2 used， DCLKDIV >=6 If dclk only， DCLKDIV >=1

7.2.7.10. TCON0 Basic Timing Register0(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: TCON0_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON0_X Panel width is X+1
15:12	/	/	/
11:0	R/W	0x0	TCON0_Y Panel height is Y+1

7.2.7.11. TCON0 Basic Timing Register1(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: TCON0_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:29	/	/	/
28:16	R/W	0x0	HT Thcycle = (HT+1) * Tdclk Computation 1) parallel:HT = X + BLANK Limitation: 1) parallel :HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch (in dclk) Thbp = (HBP +1) * Tdclk

7.2.7.12. TCON0 Basic Timing Register2(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: TCON0_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	VT TVT = (VT)/2 * Thsync VT/2 >= (VBP+1) + (Y+1) +2
15:12	/	/	/
11:0	R/W	0x0	VBP Tvbp = (VBP +1) * Thsync

7.2.7.13. TCON0 Basic Timing Register3(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: TCON0_BASIC3_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	HSPW Thspw = (HSPW+1) * Tdclk HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW Tvspw = (VSPW+1) * Thsync VT/2 > (VSPW+1)

7.2.7.14. TCON0 HV Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: TCON0_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	HV_MODE 0000: 24bit/1cycle parallel mode 1000: 8bit/3cycle RGB serial mode(RGB888) 1010: 8bit/4cycle Dummy RGB(DRGB) 1011: 8bit/4cycle RGB Dummy(RGBD) 1100: 8bit/2cycle YUV serial mode(CCIR656)
27:26	R/W	0x0	RGB888_SM0 serial RGB888 mode output sequence at odd lines of the panel (line 1, 3, 5, 7…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0x0	RGB888_SM1 serial RGB888 mode output sequence at even lines of the panel (line 2, 4, 6, 8…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0x0	YUV_SM

Offset: 0x0058			Register Name: TCON0_HV_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			serial YUV mode output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0x0	YUV EAV/SAV F LINE DELAY 00:F toggle right after active video line 01:delay 2 line(CCIR PAL) 10:delay 3 line(CCIR NTSC) 11:reserved
19	R/W	0x0	CCIR_CSC_DIS 0: Enable 1: Disable Only valid when HV mode is “1100”, select ‘0’ TCON convert source from RGB to YUV
18:0	/	/	/

7.2.7.15. TCON0 CPU Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0060			Register Name: TCON0_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	CPU_MODE 0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI
27	/	/	/
26	R/W	0x0	DA pin A1 value in 8080 mode auto/flash states
25	R/W	0x0	CA pin A1 value in 8080 mode WR/RD execute
24	/	/	/
23	R	0x0	WR_FLAG 0:Write operation is finishing 1:Write operation is pending
22	R	0x0	Rd_Flag 0:Read operation is finishing 1:Read operation is pending
21:18	/	/	/
17	R/W	0x0	AUTO auto Transfer Mode:

Offset: 0x0060			Register Name: TCON0_CPU_IF_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			If it is 1, all the valid data during this frame are written to panel. **NOTE** **This bit is sampled by Vsync.**
16	R/W	0x0	FLUSH direct transfer mode If it is enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
15:4	/	/	/
3	R/W	0x0	TRIGGER_FIFO_BIST_EN 0: Disable 1: Enable Entry addr is 0xFF8
2	R/W	0x0	TRIGGER_FIFO_EN 0:Enable 1:Disable
1	R/W1S	0x0	TRIGGER_START Write '1' to start a frame flush, writing'0' has no effect. This flag indicated frame flush is running. Software must make sure that write '1' only when this flag is '0'.
0	R/W	0x0	Trigger_EN 0: Trigger mode disable 1: Trigger mode enable

7.2.7.16. TCON0 CPU Panel Write Data Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: TCON0_CPU_WRITE_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	W	0x0	DATA_WRITE Data write on 8080 bus, launch a write operation on 8080 bus

7.2.7.17. TCON0 CPU Panel Read Data Register0(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: TCON0_CPU_RD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R	0x0	DATA_READ0 Data read on 8080 bus, launch a new read operation on 8080 bus

7.2.7.18. TCON0 CPU Panel Read Data Register1(Default Value: 0x0000_0000)

Offset: 0x006C			Register Name: TCON0_CPU_RD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x006C			Register Name: TCON0_CPU_RD1_REG
Bit	Read/Write	Default/Hex	Description
23:0	R	0x0	Data_READ1 Data read on 8080 bus, without a new read operation on 8080 bus

7.2.7.19. TCON0 LVDS Panel Interface Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: TCON0_LVDS_IF_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	TCON0_LVDS_EN 0: Disable 1: Enable
30:29	/	/	/
28	R/W	0x0	TCON0_LVDS_DIR LVDS direction 0: Normal 1: Reversed
27	R/W	0x0	TCON0_LVDS_MODE 0: NS mode 1: JEIDA mode
26	R/W	0x0	TCON0_LVDS_BITWIDTH 0: 24bit 1: 18bit
25:24	/	/	/
23	R/W	0x0	TCON0_LVDS_CORRECT_MODE 0: Mode0 1: Mode1
22:0	/	/	/

7.2.7.20. TCON0 IO Polarity Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TCON0_IO_POL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IO_OUTPUT_SEL 0: normal output 1: register output when set as '1', d[23:0], io0, io1,io3 sync to dclk
30:28	R/W	0x0	DCLK_SEL 000: used DCLK0(normal phase offset) 001: used DCLK1(1/3 phase offset) 010: used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 Others: Reserved
27	R/W	0x0	IO3_INV

Offset: 0x0088			Register Name: TCON0_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: not invert 1: invert
26	R/W	0x0	IO2_ INV 0: not invert 1: invert
25	R/W	0x0	IO1_INV 0: not invert 1: invert
24	R/W	0x0	IO0_INV 0: not invert 1: invert
23:0	R/W	0x0	Data_INV TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

7.2.7.21. TCON0 IO Control Register(Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: TCON0_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R/W	0x0	RGB_ENDIAN 0: Normal 1: Bits_invert
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	Data_OUTPUT_TRI_EN TCON0 output port D[23:0] output enable, with independent bit control: 1s: Disable

Offset: 0x008C			Register Name: TCON0_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0s: Enable

7.2.7.22. TCON Debug Register(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TCON_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON0_FIFO_Under_Flow
30	/	/	/
29	R	0x0	TCON0_Field_Polarity 0: Second field 1: First field
28	/	/	/
27:16	R	0x0	TCON0_Current_Line
15:0	/	/	/

7.2.7.23. TCON CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TCON_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: Bypass 1: Enable
30:0	/	/	/

7.2.7.24. TCON CEU Coefficient MUL Register(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TCON_CEU_COEF_MUL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE Signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

7.2.7.25. TCON CEU Coefficient ADD Register(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10(N=0,1,2)			Register Name: TCON_CEU_COEF_ADD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE Signed 19bit value, range of (-16384, 16384) N=0: Rc N=1: Gc N=2: Bc

7.2.7.26. TCON CEU Coefficient RANG Register(Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04(N=0,1,2)			Register Name: TCON_CEU_COEF_RANG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN Unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU COEF_RANGE_MAX Unsigned 8bit value, range of [0,255]

7.2.7.27. TCON0 CPU TRI0 Register(Default Value: 0x0000_0000)

Offset: 0x0160			Register Name: TCON0_CPU_TRI0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BLOCK_SPACE should be set >20*pixel_cycle
15:12	/	/	/
11:0	R/W	0x0	BLOCK_SIZE

7.2.7.28. TCON0 CPU TRI1 Register(Default Value: 0x0000_0000)

Offset: 0x0164			Register Name: TCON0_CPU_TRI1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R	0x0	BLOCK_CURRENT_NUM
15:0	R/W	0x0	BLOCK_NUM

7.2.7.29. TCON0 CPU TRI2 Register(Default Value: 0x0000_0000)

Offset: 0x0168			Register Name: TCON0_CPU_TRI2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x20	START_DELAY Tdly = (Start_Delay +1) * be_clk*8
15	R/W	0x0	Trans_Start_Mode 0: ecc_fifo+tri_fifo 1: tri_fifo

Offset: 0x0168			Register Name: TCON0_CPU_TRI2_REG
Bit	Read/Write	Default/Hex	Description
14:13	R/W	0x0	SYNC_MODE 0x: auto 10: 0 11: 1
12:0	R/W	0x0	TRANS_START_SET

7.2.7.30. TCON0 CPU TRI3 Register(Default Value: 0x0000_0000)

Offset: 0x016C			Register Name: TCON0_CPU_TRI3_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0x0	TRI_INT_MODE 00: disable 01: counter mode 10: te rising mode 11: te falling mode when set as 01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. when set as 10 or 11, io0 is map as TE input.
27:24	/	/	/
23:8	R/W	0x0	COUNTER_N
7:0	R/W	0x0	COUNTER_M

7.2.7.31. TCON0 CPU TRI4 Register(Default Value: 0x0000_0000)

Offset: 0x0170			Register Name: TCON0_CPU_TRI4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	PLUG_MODE_EN 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x0	A1 Valid in first Block
23:0	R/W	0x0	D23-D0 Valid in first Block

7.2.7.32. TCON0 CPU TRI5 Register(Default Value: 0x0000_0000)

Offset: 0x0174			Register Name: TCON0_CPU_TRI5_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0x0	A1 Valid in Block except first
23:0	R/W	0x0	D23-D0 Valid in Block except first

7.2.7.33. TCON CMAP Control Register(Default Value: 0x0000_0000)

Offset: 0x0180			Register Name: TCON_CMAP_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	COLOR_MAP_EN 0: bypass 1: enable This module only work when X is divided by 4
30:1	/	/	/
0	R/W	0x0	OUT_FORMAT 0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3 1: 2 pixel output mode: Out0 -> Out1

7.2.7.34. TCON CMAP ODD0 Register(Default Value: 0x0000_0000)

Offset: 0x0190			Register Name: TCON_CMAP_ODD0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD1
15:0	R/W	0x0	OUT_ODD0 bit15-12: Reserved bit11-08: Out_Odd0[23:16] bit07-04: Out_Odd0[15:8] bit03-00: Out_Odd0[7:0] 0x0: in_b0 0x1: in_g0 0x2: in_r0 0x3: Reserved 0x4: in_b1 0x5: in_g1 0x6: in_r1 0x7: Reserved 0x8: in_b2 0x9: in_g2GIC 0xa: in_r2 0xb: Reserved 0xc: in_b3 0xd: in_g3 0xe: in_r3 0xf: Reserved

7.2.7.35. TCON CMAP ODD1 Register(Default Value: 0x0000_0000)

Offset: 0x0194			Register Name: TCON_CMAP_ODD1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_ODD3
15:0	R/W	0x0	OUT_ODD2

7.2.7.36. TCON CMAP EVEN0 Register(Default Value: 0x0000_0000)

Offset: 0x0198			Register Name: TCON_CMAP_EVEN0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN1
15:0	R/W	0x0	OUT_EVEN0

7.2.7.37. TCON CMAP EVEN1 Register(Default Value: 0x0000_0000)

Offset: 0x019C			Register Name: TCON_CMAP_EVEN1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	OUT_EVEN3
15:0	R/W	0x0	OUT_EVEN2

7.2.7.38. TCON Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TCON_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM
15:4	R/W	0x0	SAFE_PERIOD_LINE
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at ecc_fifo_curr_num > safe_period_fifo_num 011: safe at 2 and safe at sync active 100: safe at line

7.2.7.39. LCD LVDS0 Analog Register(Default Value: 0x0000_0000)

Offset: 0x0220			Register Name: LCD_LVDS0_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LVDS0_EN_MB Enable the bias circuit of the LVDS_Ana module
30	R/W	0x0	LVDS0_EN_LDO
29:25	/	/	/
24	R/W	0x0	LVDS0_EN_DRVC Enable all circuits working when transmitting the data in channel clock of LVDS_tx0
23:20	R/W	0x0	LVDS0_EN_DRV Enable all circuits working when transmitting the data in channel<3:0> of LVDS_tx0
19	R/W	0x0	LVDS0_REG_DRAM_TEST 0:dram test clk disable 1:dram test clk enable
18:17	R/W	0x0	LVDS0_REG_C Adjust current flowing through Rload of Rx to change the differential signals amplitude

Offset: 0x0220			Register Name: LCD_LVDS0_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			00:250mV 01:300mV 10:350mV 11:400mV
16	R/W	0x0	LVDS0_REG_DENC Choose data output or PLL test clock output in LVDS_tx
15:12	R/W	0x0	LVDS0_REG_DEN Choose data output or PLL test clock output in LVDS_tx
11:10	/	/	/
9:8	R/W	0x0	LVDS0_REG_V Adjust common mode voltage of the differential signals in five channels. single signal high level: 00:1.1V 01:1.19V 10:1.3V 11:1.43V
7:6	/	/	/
5:4	R/W	0x0	LVDS0_REG_PD Fine adjust the slew rate of output data
3:2	/	/	/
1	R/W	0x0	LVDS0_REG_PWSLV Adjust voltage amplitude of low power in LVDS_Ana
0	R/W	0x0	LVDS0_REG_PWSMB Adjust voltage amplitude of mbias voltage reference in LVDS_Ana

7.2.7.40. LCD LVDS1 Analog Register(Default Value: 0x0000_0000)

Offset: 0x0224			Register Name: LCD_LVDS1_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	LVDS1_EN_MB Enable the bias circuit of the LVDS_Ana module
30	R/W	0x0	LVDS1_EN_LDO
29:25	/	/	/
24	R/W	0x0	LVDS1_EN_DRVC Enable all circuits working when transmitting the data in channel clock of LVDS_tx0
23:20	R/W	0x0	LVDS1_EN_DRV Enable all circuits working when transmitting the data in channel<3:0> of LVDS_tx0
19	R/W	0x0	LVDS1_REG_DRAM_TEST 0:dram test clk disable 1:dram test clk enable
18:17	R/W	0x0	LVDS1_REG_C Adjust current flowing through Road of Rx to change the differential signals amplitude 00:250mV 01:300mV 10:350mV

Offset: 0x0224			Register Name: LCD_LVDS1_ANA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			11:400mV
16	R/W	0x0	LVDS1_REG_DENC Choose data output or PLL test clock output in LVDS_tx
15:12	R/W	0x0	LVDS1_REG_DEN Choose data output or PLL test clock output in LVDS_tx
11:10	/	/	/
9:8	R/W	0x0	LVDS1_REG_V Adjust common mode voltage of the differential signals in five channels. single signal high level: 00:1.1V 01:1.19V 10:1.3V 11:1.43V
7:6	/	/	/
5:4	R/W	0x0	LVDS1_REG_PD Fine adjust the slew rate of output data
3:2	/	/	/
1	R/W	0x0	LVDS1_REG_PWSLV Adjust voltage amplitude of low power in LVDS_Ana
0	R/W	0x0	LVDS1_REG_PWSMB Adjust voltage amplitude of mbias voltage reference in LVDS_Ana

7.2.8. TCON_TV Register Description

7.2.8.1. TCON Global Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TCON_GCTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON_EN 0: Disable 1: Enable When it's disabled, the module will be reset to idle state.
30	R/W	0x0	TCON_GAMMA_EN 0: Disable 1: Enable
29:0	/	/	/

7.2.8.2. TCON Global Interrupt0 Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TCON_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	TCON1_VB_INT_EN 0: Disable 1: Enable
29	/	/	/

Offset: 0x0004			Register Name: TCON_GINT0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
28	R/W	0x0	TCON1_LINE_INT_EN 0: Disable 1: Enable
27:15	/	/	/
14	R/W	0x0	TCON1_VB_INT_FLAG Asserted during vertical no-display period every frame. Write 0 to clear it.
13	/	/	/
12	R/W	0x0	TCON1_LINE_INT_FLAG Trigger when SY1 match the current TCON1 scan line Write 0 to clear it.
11:0	/	/	/

7.2.8.3. TCON Global Interrupt1 Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TCON_GINT1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x0	TCON1_LINE_INT_NUM scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. **NOTE** **SY1 is writable only when LINE_TRG1 disable.**

7.2.8.4. TCON1 Source Control Register(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: TCON1_SRC_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x0	TCON1_SRC_SEL 000: DE 001: Color Check 010: Grayscale Check 011: Black by White Check 100: Reserved 101: Reserved 111: Gridding Check

7.2.8.5. TCON1 Control Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: TCON1_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON1_EN 0: Disable 1: Enable
30:9	/	/	/

Offset: 0x0090			Register Name: TCON1_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
8:4	R/W	0x0	START_DELAY This is for DE0 and DE1
3:2	/	/	/
1	R/W	0x0	TCON1_SRC_SEL 0: Reserved 1: BLUE data(FIFO2 disable, RGB=0000FF) **NOTE** **The priority of the bit is higher than TCON1_SRC_SEL.**
0	/	/	/

7.2.8.6. TCON1 Basic0 Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: TCON1_BASIC0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON1_XI source width is X+1
15:12	/	/	/
11:0	R/W	0x0	TCON1_YI source height is Y+1

7.2.8.7. TCON1 Basic1 Register(Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: TCON1_BASIC1_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	LS_XO width is LS_XO+1
15:12	/	/	/
11:0	R/W	0x0	LS_YO width is LS_YO+1 This version LS_YO = TCON1_YI

7.2.8.8. TCON1 Basic2 Register(Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: TCON1_BASIC2_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	TCON1_XO width is TCON1_XO+1
15:12	/	/	/
11:0	R/W	0x0	TCON1_YO height is TCON1_YO+1

7.2.8.9. TCON1 Basic3 Register(Default Value: 0x0000_0000)

Offset: 0x00A0			Register Name: TCON1_BASIC3_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	HT horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0x0	HBP horizontal back porch Thbp = (HBP +1) * Thdclk

7.2.8.10. TCON1 Basic4 Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: TCON1_BASIC4_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	VT horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0x0	VBP horizontal back porch (in HD line) Tvbp = (VBP +1) * Th

7.2.8.11. TCON1 Basic5 Register(Default Value: 0x0000_0000)

Offset: 0x00A8			Register Name: TCON1_BASIC4_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0x0	HSPW horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk HT > (HSPW+1)
15:10	/	/	/
9:0	R/W	0x0	VSPW vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th VT/2 > (VSPW+1)

7.2.8.12. TCON1 SYNC Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: TCON1_PS_SYNC_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	SYNC_X
15:0	R/W	0x0	SYNC_Y

7.2.8.13. TCON1 IO Polarity Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: TCON1_IO_POL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x0	IO3_INV 0: not invert 1: invert
26	R/W	0x0	IO2_INV 0: not invert 1: invert
25	R/W	0x0	IO1_INV 0: not invert 1: invert
24	R/W	0x0	IO0_INV 0: not invert 1: invert
23:0	R/W	0x0	DATA_INV TCON1 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

7.2.8.14. TCON1 IO Trigger Register(Default Value: 0x0FFF_FFFF)

Offset: 0x008C			Register Name: TCON1_IO_TRI_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27	R/W	0x1	IO3_OUTPUT_TRI_EN 1: Disable 0: Enable
26	R/W	0x1	IO2_OUTPUT_TRI_EN 1: Disable 0: Enable
25	R/W	0x1	IO1_OUTPUT_TRI_EN 1: Disable 0: Enable
24	R/W	0x1	IO0_OUTPUT_TRI_EN 1: Disable 0: Enable
23:0	R/W	0xFFFFFF	DATA_OUTPUT_TRI_EN TCON1 output port D[23:0] output enable, with independent bit control: 1s: Disable 0s: Enable

7.2.8.15. TCON ECC FIFO Register(Default Value: UDF)

Offset: 0x00F8			Register Name: TCON_ECC_FIFO_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	UDF	ECC_FIFO_BIST_EN 0: Disable 1: Enable
30	R/W	UDF	ECC_FIFO_ERR_FLAG
29:24	/	/	/
23:16	R/W	UDF	ECC_FIFO_ERR_BITS
15:9	/	/	/
8	R/W	UDF	ECC_FIFO_BLANK_EN 0: Disable ecc function in blanking 1: Enable ecc function in blanking ECC function is tent to trigger in blanking area at hv mode, set '0' when in hv mode
7:0	R/W	UDF	ECC_FIFO_SETTING bit3 0:Enable 1:Disable

7.2.8.16. TCON Debug Register(Default Value: UDF)

Offset: 0x00FC			Register Name: TCON_DEBUG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	UDF	TCON1_FIFO_Under_Flow
29	/	/	/
28	R	UDF	TCON1_FIELD_POLARITY 0: second field 1: first field
27:14	/	/	/
13	R/W	0x0	ECC_FIFO_Bypass 0: used 1: bypass
12	/	/	/
11:0	R	UDF	TCON1_Current_Line

7.2.8.17. TCON CEU Control Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: TCON_CEU_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CEU_EN 0: bypass 1: enable

Offset: 0x0100			Register Name: TCON_CEU_CTL_REG
Bit	Read/Write	Default/Hex	Description
30:0	/	/	/

7.2.8.18. TCON CEU Coefficient MUL Register(Default Value: 0x0000_0000)

Offset: 0x0110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TCON_CEU_COEF_MUL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	CEU_COEF_MUL_VALUE signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg N=10: Bb

7.2.8.19. TCON CEU Coefficient ADD Register(Default Value: 0x0000_0000)

Offset: 0x011C+N*0x10 (N=0,1,2)			Register Name: TCON_CEU_COEF_ADD_REG
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:0	R/W	0x0	CEU_COEF_ADD_VALUE signed 19bit value, range of (-16384, 16384) N=0: Rc N=1: Gc N=2: Bc

7.2.8.20. TCON CEU Coefficient Range Register(Default Value: 0x0000_0000)

Offset: 0x0140+N*0x04 (N=0,1,2)			Register Name: TCON_CEU_COEF_RANGE_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	CEU_COEF_RANGE_MIN unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0x0	CEU_COEF_RANGE_MAX unsigned 8bit value, range of [0,255]

7.2.8.21. TCON Safe Period Register(Default Value: 0x0000_0000)

Offset: 0x01F0			Register Name: TCON_SAFE_PERIOD_REG
Bit	Read/Write	Default/Hex	Description

Offset: 0x01F0			Register Name: TCON_SAFE_PERIOD_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28:16	R/W	0x0	SAFE_PERIOD_FIFO_NUM
15:4	R/W	0x0	SAFE_PERIOD_LINE
3	/	/	/
2:0	R/W	0x0	SAFE_PERIOD_MODE 000: unsafe 001: safe 010: safe at ecc_fifo_curr_num > safe_period_fifo_num 011: safe at 2 and safe at sync active 100: safe at line

7.2.8.22. TCON1 Fill Data Control Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: TCON1_FILL_CTL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TCON1_FILL_EN 0: bypass 1: enable
30:0	/	/	/

7.2.8.23. TCON1 Fill Begin Register(Default Value: 0x0000_0000)

Offset: 0x0304+N*0x0C (N=0,1,2)			Register Name: TCON1_FILL_BEGIN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_BEGIN

7.2.8.24. TCON1 Fill Data End Register(Default Value: 0x0000_0000)

Offset: 0x0308+N*0x0C (N=0,1,2)			Register Name: TCON1_FILL_END_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_END

7.2.8.25. TCON1 Fill Data Value Register(Default Value: 0x0000_0000)

Offset: 0x030C+N*0x0C (N=0,1,2)			Register Name: TCON1_FILL_DATA0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	FILL_VALUE

7.3. HDMI

7.3.1. Overview

Features:

- Compatible with HDMI 1.4 specification
- Compatible with HDCP 1.2 for HDMI
- Supports Video formats with only 8bit color depth
  - 720x576@50Hz
  - 720x480@60Hz
  - 1280x720@50/60Hz
  - 1920x1080i@50/60Hz
  - 1920x1080p@24Hz
  - 1920x1080p@50/60Hz
  - 3D Frame Packing 1920x1080p@24Hz
- Supports Audio formats
  - L-PCM audio format
  - IEC-61937 compressed audio format

7.3.2. Block Diagram

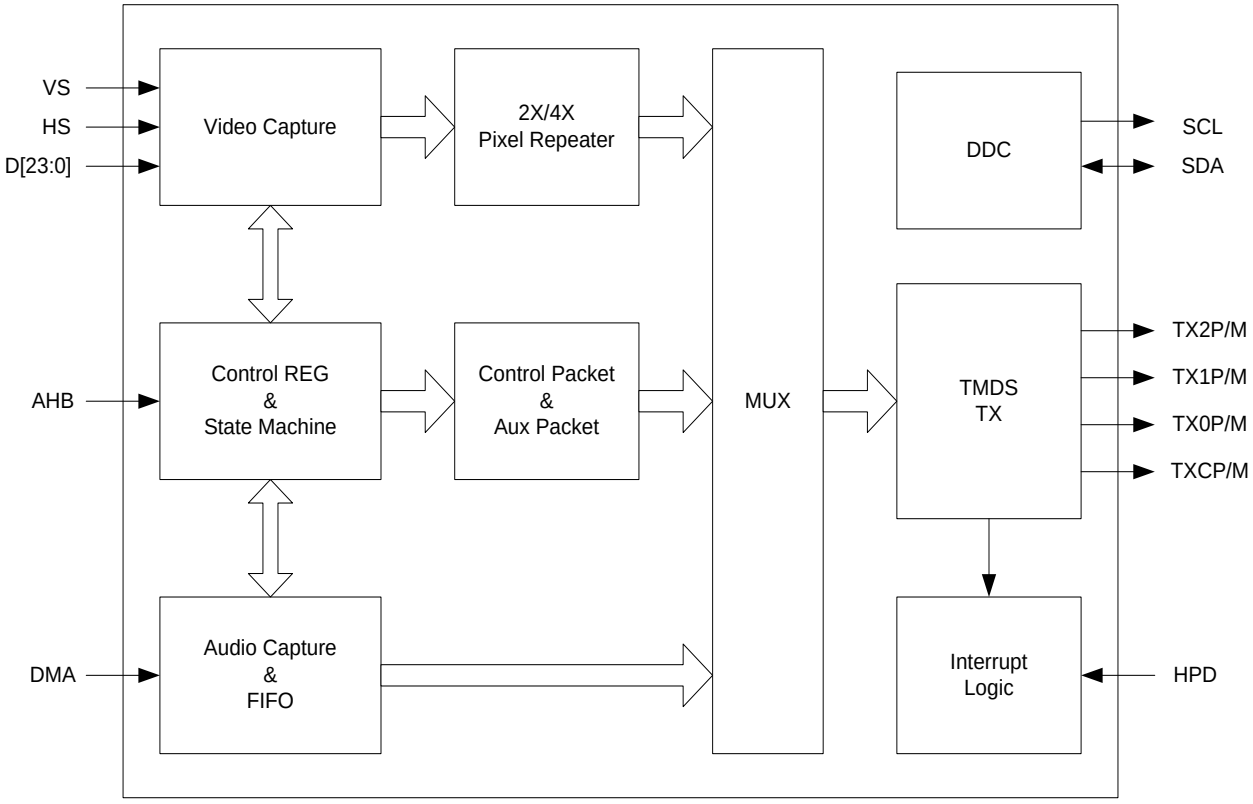


Figure 7-13. HDMI Block Diagram

For complete HDMI information, refer to the ***Allwinner A40i HDMI Specification***.

7.4. MIPI DSI

7.4.1. Overview

Features:

- Compliance with MIPI DSI v1.01 and MIPI D-PHY v1.00
- 1/2/3/4 data lane configuration and up to 1Gbps per lane
- ECC, CRC generation and EOT package support
- Supports up to 1080p@60fps with 4 data lanes
- Supports video mode with sync pulse/sync event
- Supports video burst mode
- Supports command mode
- Supports pixel format: RGB888, RGB666, RGB666 packed, and RGB565
- Supports bidirectional configuration in LP

7.4.2. Block Diagram

Figure 7-14 shows the block diagram of MIPI DSI.

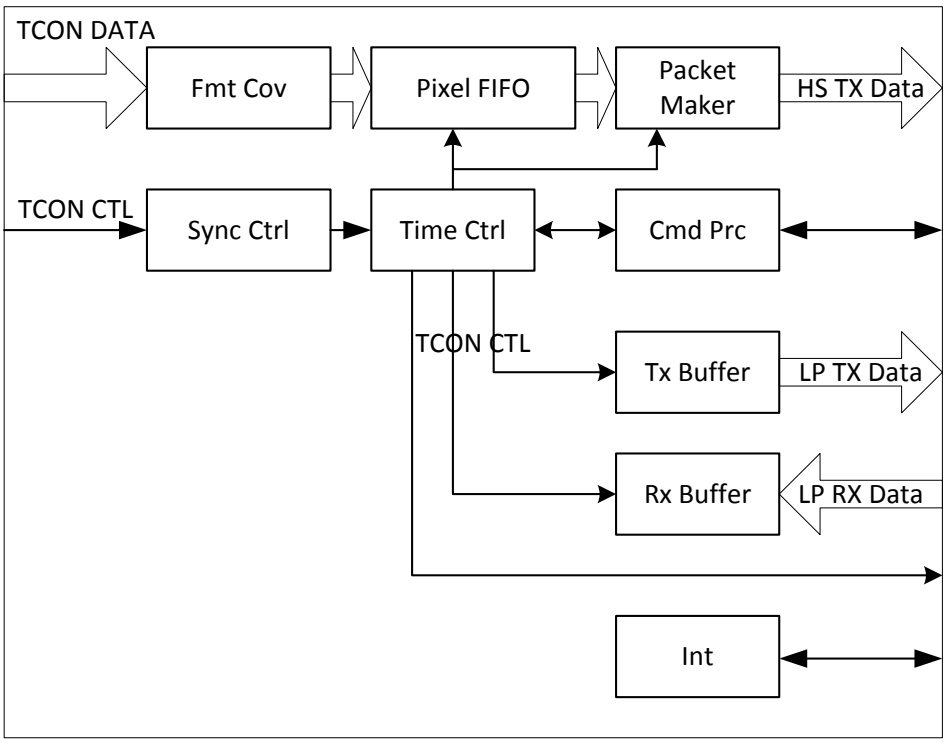


Figure 7-14. MIPI DSI Block Diagram

For complete MIPI DSI information, refer to the ***Allwinner A40i MIPI DSI Specification***.

7.5. TV Encoder

7.5.1. Overview

Features:

- 4-channel CVBS output , supports NTSC and PAL
- 1-channel YPbPr, supports 1080p60,1080p50,720p60,720p50,576p,480p,576i,480i
- 1-channel VGA, up to 1080p@60fps
- Plug status auto detection for CVBS and YPbPr

7.5.2. Block Diagram

Figure 7-15 shows the top block diagram of TV Encoder (TVE).

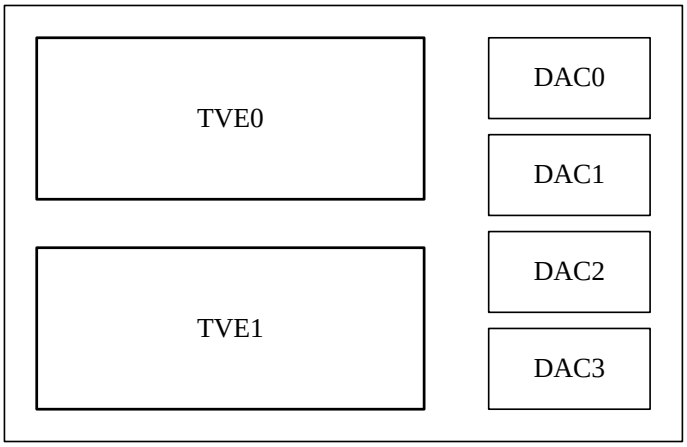


Figure 7-15. TVE Top Block Diagram

Figure 7-16 shows the detail block diagram of TVE.

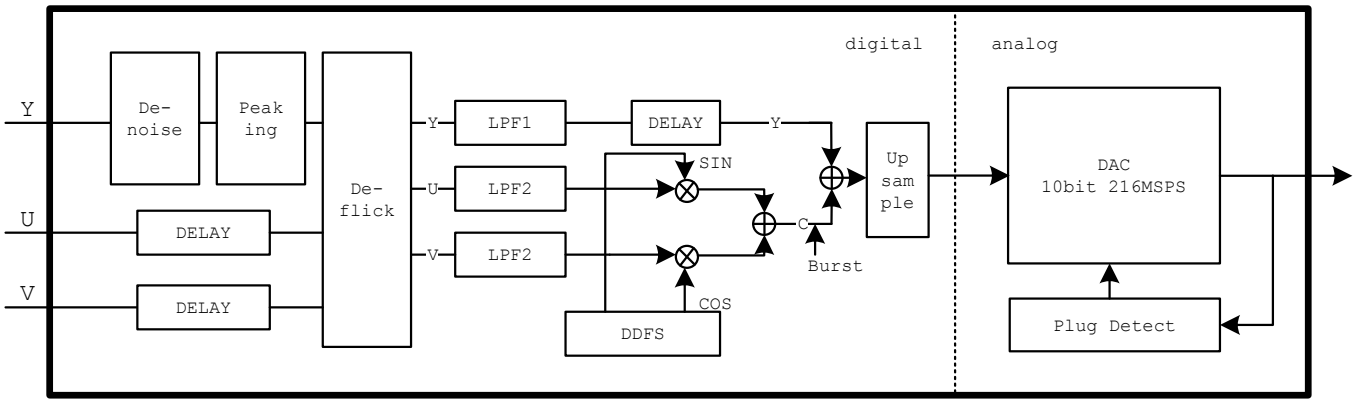


Figure 7-16. TVE Block Diagram

7.5.3. Register List

Module Name	Base Address
TVE_TOP	0x01C90000
TVE0	0x01C94000
TVE1	0x01C98000

Register Name	Offset	Description
TVE_TOP		
TVE_DAC_MAP	0x0020+N*0x20 (N=0~3)	TV Encoder DAC MAP Register
TVE_DAC_STATUS	0x0024+N*0x20 (N=0~3)	TV Encoder DAC STAUTS Register
TVE_DAC_CFG0	0x0028+N*0x20 (N=0~3)	TV Encoder DAC CFG0 Register
TVE_DAC_CFG1	0x002C+N*0x20 (N=0~3)	TV Encoder DAC CFG1 Register
TVE_DAC_CFG2	0x0030+N*0x20 (N=0~3)	TV Encoder DAC CFG2 Register
TVE_DAC_CFG3	0x0034+N*0x20 (N=0~3)	TV Encoder DAC CFG2 Register
TVE_DAC_TEST	0x00F0	TV Encoder DAC TEST Register
TVE		
TVE_000_REG	0x0000	TV Encoder Clock Gating Register
TVE_004_REG	0x0004	TV Encoder Configuration Register
TVE_008_REG	0x0008	TV Encoder DAC Register1
TVE_00C_REG	0x000C	TV Encoder Notch and DAC Delay Register
TVE_010_REG	0x0010	TV Encoder chroma frequency Register
TVE_014_REG	0x0014	TV Encoder Front/Back Porch Register
TVE_018_REG	0x0018	TV Encoder HD mode VSYNC Register
TVE_01C_REG	0x001C	TV Encoder Line Number Register
TVE_020_REG	0x0020	TV Encoder Level Register
TVE_024_REG	0x0024	TV Encoder DAC Register2
TVE_030_REG	0x0030	TV Encoder Auto Detection Enable Register
TVE_034_REG	0x0034	TV Encoder Auto Detection Interrupt Status Register
TVE_038_REG	0x0038	TV Encoder Auto Detection Status Register
TVE_03C_REG	0x003C	TV Encoder Auto Detection de-bounce Setting Register
TVE_0F8_REG	0x00F8	TV Encoder Auto Detect Configuration Register0
TVE_0FC_REG	0x00FC	TV Encoder Auto Detect Configuration Register1
TVE_100_REG	0x0100	TV Encoder Color Burst Phase Reset Configuration Register
TVE_104_REG	0x0104	TV Encoder VSYNC Number Register
TVE_108_REG	0x0108	TV Encoder Notch Filter Frequency Register
TVE_10C_REG	0x010C	TV Encoder Cb/Cr Level/Gain Register
TVE_110_REG	0x0110	TV Encoder Tint and Color Burst Phase Register
TVE_114_REG	0x0114	TV Encoder Burst Width Register
TVE_118_REG	0x0118	TV Encoder Cb/Cr Gain Register
TVE_11C_REG	0x011C	TV Encoder Sync and VBI Level Register
TVE_120_REG	0x0120	TV Encoder White Level Register
TVE_124_REG	0x0124	TV Encoder Video Active Line Register
TVE_128_REG	0x0128	TV Encoder Video Chroma BW and CompGain Register
TVE_12C_REG	0x012C	TV Encoder Register

Register Name	Offset	Description
TVE_130_REG	0x0130	TV Encoder Re-sync parameters Register
TVE_134_REG	0x0134	TV Encoder Slave Parameter Register
TVE_138_REG	0x0138	TV Encoder Configuration Register0
TVE_13C_REG	0x013C	TV Encoder Configuration Register1
TVE_380_REG	0x0380	TV Encoder Low Pass Control Register
TVE_384_REG	0x0384	TV Encoder Low Pass Filter Control Register
TVE_388_REG	0x0388	TV Encoder Low Pass Gain Register
TVE_38C_REG	0x038C	TV Encoder Low Pass Gain Control Register
TVE_390_REG	0x0390	TV Encoder Low Pass Shoot Control Register
TVE_394_REG	0x0394	TV Encoder Low Pass Coring Register
TVE_3A0_REG	0x03A0	TV Encoder Noise Reduction Register

7.5.4. Register Description

7.5.4.1. TV Encoder DAC MAP Register(Default Value: 0x0000_0000)

Offset: 0x0020+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_MAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:4	R/W	0x0	DAC_MAP 000: OUT0 001: OUT1 010: OUT2 011: OUT3 Others: Reserved
3:2	/	/	/
1:0	R/W	0x0	DAC_SEL 00: NO 01: TVE0 10: TVE1 11: Reserved

7.5.4.2. TV Encoder DAC Status Register(Default Value: 0x0000_0000)

Offset: 0x0024+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_STATUS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x0	DAC_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

7.5.4.3. TV Encoder DAC Configuration0 Register(Default Value: 0x8000_4000)

Offset: 0x0028+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_CFG0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x1	DAC_CLOCK_INVERT 0: Not invert 1: Invert
30:26	/	/	/
25:16	R/W	0x0	CALI_IN
15:12	R/W	0x4	LOW_BIAS 500uA to 4mA
11:10	/	/	/
9	R/W	0x0	BIAS_EXT_SEL 0: Disable 1: Enable (a_sel_bias_adda)
8	R/W	0x0	BIAS_INT_SEL 0: Disable 1: Enable (a_sel_bias_res)
7:5	/	/	/
4	R/W	0x0	BIAS_REF_INT_EN 0: Disable 1: Enable (a_en_resref)
3:1	/	/	/
0	R/W	0x0	DAC_EN 0: Disable 1: Enable

7.5.4.4. TV Encoder DAC Configuration1 Register(Default Value: 0x0000_003A)

Offset: 0x002C+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	REF_EXT_SEL 0: Disable 1: Enable (a_sel_detref_ldo)
8	R/W	0x0	REF_INT_SEL 0: Disable 1: Enable (a_sel_detref_res)
7:6	/	/	/
5:4	R/W	0x3	REF2_SEL

Offset: 0x002C+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default/Hex**	**Description**
			00: 0.25V 01: 0.30V 10: 0.35V 11: 0.40V (a_refslct2<1:0>)
3:0	R/W	0xA	REF1_SEL 0000: 0.50V 0001: 0.55V 0010: 0.60V 0011: 0.65V 0100: 0.70V 0101: 0.75V 0110: 0.80V 0111: 0.85V 1000: 0.90V 1001: 0.95V 1010: 1.00V 1011: 1.05V 1100: 1.10V 1101: 1.15V 1110: 1.20V 1111: 1.25V (a_refslct1<3:0>)

7.5.4.5. TV Encoder DAC Configuration2 Register(Default Value: 0x8000_4000)

Offset: 0x0030+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_CFG2
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:8	R/W	0x0	B (I config output current for different peak voltage)
7:6	R/W	0x0	S2S1
5:0	R/W	0x10	R_SET

7.5.4.6. TV Encoder DAC Configuration3 Register(Default Value: 0x8000_4000)

Offset: 0x0034+N*0x20(N=0,1,2,3)			Register Name: TVE_DAC_CFG3
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	FORCE_DATA_SET Force DAC input data
15:1	/	/	/
0	R/W	0x0	FORCE_DATA_EN 0:DAC input data from TVE 1: DAC input data from FORCE_DATA_SET

7.5.4.7. TV Encoder DAC Test Register(Default Value: 0x0000_0000)

Offset: 0x00F0			Register Name: TVE_DAC_TEST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	DAC_TEST_LENGTH DAC TEST DATA LENGTH
15:6	/	/	/
5:4	R/W	0x0	DAC_TEST_SEL 00: DAC0 01: DAC1 10: DAC2 11: DAC3
3:1	/	/	/
0	R/W	0x0	DAC_TEST_ENABLE 0: Reserved 1: Repeat DAC data from DAC sram

7.5.4.8. TV Encoder Clock Gating Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TVE_000_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CLOCK_GATE_DIS 0: Enable 1: Disable
30:29	/	/	/
28	R/W	0x0	BIST_EN 0: Normal mode 1: Bist mode
27:23	/	/	/
22	R/W	0x0	upsample for YPbPr 0:1x 1:2x
21:20	R/W	0x0	upsample for CVBS Out up sample 00: 27MHz 01: 54MHz 10: 108MHz 11: 216MHz
19:4	/	/	/
3:1	/	/	/
0	R/W	0x0	TVE_EN 0: Disable 1: Enable Video Encoder enable, default disable, write 1 to take it out of the reset state

7.5.4.9. TV Encoder Configuration Register(Default Value: 0x0001_0000)

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29	R/W	0x0	BYPASS_TV 0: Disable 1: Enable
28:27	R/W	0x0	DAC_SRC_SEL 00: TV Encoder 01: LCD controller, override all other TV encoder setting, the DAC clock can from LCD controller. 10: DAC test mode,DAC using DAC clock 11: DAC test mode, DAC using AHB clock
26	R/W	0x0	DAC_CONTROL_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
25	R/W	0x0	CORE_DATAPATH_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
24	R/W	0x0	CORE_CONTROL_LOGIC_CLOCK_SEL 0: Using 27MHz clock or 74.25MHz clock depend on CCU setting 1: Using 54MHz clock or 148.5MHz clock depend on CCU setting
23:21	/	/	/
20	R/W	0x0	CB_CR_SEQ_FOR_422_MODE 0: Cb first 1: Cr first
19	R/W	0x0	INPUT_CHROMA_DATA_SAMPLING_RATE_SEL 0: 4:4:4 1: 4:2:2
18	R/W	0x0	YUV_RGB_OUTPUT_EN 0: CVBS or/and Y/C 1: YUV (or RGB) **NOTE** **Only apply to SD interlace mode, when in progressive mode, output YPbPr (RGB) only.**
17	R/W	0x0	YC_EN S-port Video enable Selection 0: Y/C is disable 1: Y/C enable This bit selects whether the S-port(Y/C) video output is enabled or disabled.
16	R/W	0x1	CVBS_EN Composite Video enable Selection

Offset: 0x0004			Register Name: TVE_004_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Composite video is disabled, Only Y/C is enable 1: Composite video is enabled., CVBS and Y/C enable This bit selects whether the composite video output (CVBS) is enabled or disabled.
15:10	/	/	/
9	R/W	0x0	COLOR_BAR_TYPE 0: 75/7.5/75/7.5 (NTSC), 100/0/75/0(PAL) 1: 100/7.5/100/7.5(NTSC), 100/0/100/0(PAL)
8	R/W	0x0	COLOR_BAR_MODE Standard Color bar input selection 0: The Video Encoder input is coming from the Display Engineer 1: The Video Encoder input is coming from an internal standard color bar generator. This bit selects whether the Video Encoder video data input is replaced by an internal standard color bar generator or not.
7:5	/	/	/
4	R/W	0x0	MODE_1080I_1250LINE_SEL 0: 1125 Line mode 1: 1250 Line mode
3:0	R/W	0x0	TVMODE_SELECT 0000: 480i 0001: 576i 0010: 480p 0011: 576p 01xx: Reserved 100x: Reserved 101x: 720p 110x: 1080i 111x: 1080p **NOTE** **Changing this register value will cause some relative register setting to relative value.**

7.5.4.10. TV Encoder DAC Register1(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: TVE_008_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:13	R/W	0x0	DAC3_SRC_SEL 000: Composite 001: Luma 010: Chroma 011: Reserved 100: Y/Green 101: U/Pb/Blue

Offset: 0x0008			Register Name: TVE_008_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			110: V/Pr/Red 111: Reserved
12:10	R/W	0x0	DAC2_SRC_SEL 000: Composite 001: Luma 010: Chroma 011: Reserved 100: Y/Green 101: U/Pb/Blue 110: V/Pr/Red 111: Reserved
9:7	R/W	0x0	DAC1_SRC_SEL 000: Composite 001: Luma 010: Chroma 011: Reserved 100: Y/Green 101: U/Pb/Blue 110: V/Pr/Red 111: Reserved
6:4	R/W	0x0	DAC0_SRC_SEL 000: Composite 001: Luma 010: Chroma 011: Reserved 100: Y/Green 101: U/Pb/Blue 110: V/Pr/Red 111: Reserved
3:0	/	/	/

7.5.4.11. TV Encoder Notch and DAC Delay Register(Default Value: 0x0201_4924)

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	CHROMA_FILTER_ACTIVE_VALID 0: Disable 1: Enable
30	R/W	0x0	LUMA_FILTER_LTI_ENABLE 0: Disable Luma filter lti 1: Enable Luma filter lti
27:25	R/W	0x1	Y_DELAY_BEFORE_DITHER
24	R/W	0x0	HD_MODE_CB_FILTER_BYPASS 0: Bypass Enable 1: Bypass Disable

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
23	R/W	0x0	HD_MODE_CR_FILTER_BYPASS 0: Bypass Enable 1: Bypass Disable
22	R/W	0x0	CHROMA_FILTER_1_444_EN 0: Chroma Filter 1 444 Disable 1: Chroma Filter 1 444 Enable
21	R/W	0x0	CHROMA_HD_MODE_FILTER_EN 0: Chroma HD Filter Disable 1: Chroma HD Filter Enable
20	R/W	0x0	CHROMA_FILTER_STAGE_1_BYPASS 0: Chroma Filter Stage 1 Enable 1: Chroma Filter Stage 1 bypass
19	R/W	0x0	CHROMA_FILTER_STAGE_2_BYPASS 0: Chroma Filter Stage 2 Enable 1: Chroma Filter Stage 2 bypass
18	R/W	0x0	CHROMA_FILTER_STAGE_3_BYPASS 0: Chroma Filter Stage 3 Enable 1: Chroma Filter Stage 3 bypass
17	R/W	0x0	LUMA_FILTER_BYPASS 0: Luma Filter Enable 1: Luma Filter bypass
16	R/W	0x1	NOTCH_EN 0: The luma notch filter is bypassed 1: The luma notch filter is operating Luma notch filter on/off selection **NOTE** **This bit selects if the luma notch filter is operating or bypassed.**
15:12	R/W	0x4	C_DELAY_BEFORE_DITHER
11:9	R/W	0x4	DAC3_DELAY 000: The DAC3 lags DAC0 by 4 encoder clock cycles 001: The DAC3 lags DAC0 by 3 encoder clock cycles 010: The DAC3 lags DAC0 by 2 encoder clock cycles 011: The DAC3 lags DAC0 by 1 encoder clock cycle 100: There is no delay between the DAC0 and DAC3 signals 001: The DAC0 lags DAC3 by 1 encoder clock cycle 010: The DAC0 lags DAC3 by 2 encoder clock cycles 011: The DAC0 lags DAC3 by 3 encoder clock cycles DAC3 and DAC0 paths relative delays (default=4 stages) Relative delay between DAC3 and DAC0 selection. These bits select the relative delay between the DAC3 samples and DAC0 samples. The delay range from 4 encoder clock cycles of DAC3 lagging the DAC0 samples to 3 encoder clock cycles of DAC3 preceding the DAC0 samples.

Offset: 0x000C			Register Name: TVE_00C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
8:6	R/W	0x4	DAC2_DELAY 000: The DAC2 lags DAC0 by 4 encoder clock cycles 001: The DAC2 lags DAC0 by 3 encoder clock cycles 010: The DAC2 lags DAC0 by 2 encoder clock cycles 011: The DAC2 lags DAC0 by 1 encoder clock cycle 100: There is no delay between the DAC0 and DAC2 signals 001: The DAC0 lags DAC2 by 1 encoder clock cycle 010: The DAC0 lags DAC2 by 2 encoder clock cycles 011: The DAC0 lags DAC2 by D encoder clock cycles DAC2 and DAC0 paths relative delays (default=4 stages) Relative delay between DAC2 and DAC0 selection. These bits select the relative delay between the DAC2 samples and DAC0 samples. The delay range from 4 encoder clock cycles of DAC2 lagging the DAC0 samples to 3 encoder clock cycles of DAC2 preceding the DAC0 samples.
5:3	R/W	0x4	DAC1_DELAY 000: The DAC1 lags DAC0 by 4 encoder clock cycles 001: The DAC1 lags DAC0 by 3 encoder clock cycles 010: The DAC1 lags DAC0 by 2 encoder clock cycles DAC1 and DAC0 paths relative delays (default=4 stages) Relative delay between DAC1 and DAC0 selection. These bits select the relative delay between the DAC1 samples and DAC0 samples. The delay range from 4 encoder clock cycles of DAC1 lagging the DAC0 samples to 3 encoder clock cycles of DAC1 preceding the DAC0 samples. 011: The DAC1 lags DAC0 by 1 encoder clock cycle 100: There is no delay between the DAC1 and DAC0 signals 001: The DAC0 lags DAC1 by 1 encoder clock cycle 010: The DAC0 lags DAC1 by 2 encoder clock cycles 011: The DAC0 lags DAC1 by D encoder clock cycles
2:0	R/W	0x4	YC_DELAY luma and chroma paths relative delays (default=4 stages) Relative delay between U/V and Y selection. These bits select the relative delay between the U and V samples and Y samples. The delay range from 4 encoder clock cycles of Y lagging the U and V samples to 3 encoder clock cycles of Y preceding the U and V samples. 000: The Y lags C by 4 encoder clock cycles 001: The Y lags C by 3 encoder clock cycles 010: The Y lags C by 2 encoder clock cycles 011: The Y lags C by 1 encoder clock cycle 100: There is no delay between the Y and C signals 101: The C lags Y by 1 encoder clock cycle 110: The C lags Y by 2 encoder clock cycles 111: The C lags Y by 3 encoder clock cycles

7.5.4.12. TV Encoder Chroma Frequency Register(Default Value: 0x21F0_7C1F)

Offset: 0x0010			Register Name: TVE_010_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x21f07c1f	Chroma_Freq Specify the ratio between the color burst frequency. 32 bits unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455 MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'): PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

7.5.4.13. TV Encoder Front/Back Porch Register(Default Value: 0x0076_0020)

Offset: 0x0014			Register Name: TVE_014_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24:16	R/W	0x76	BACK_PORCH Specify the width of the back porch in encoder clock cycles. Min value is (*burst_width+breeze_way*+17). 8 bits unsigned integer. Default value is 118. 720p mode, is 260 1080i/p mode, is 192
15:12	/	/	/
11:0	R/W	0x20	FRONT_PORCH Must be even. Specify the width of the front porch in encoder clock cycles. 6 bits unsigned even integer. Allowed range is 10 to 62. Default value is 32 in 1080i mode is 44.

7.5.4.14. TV Encoder HD Mode VSYNC Register(Default Value: 0x0000_0016)

Offset: 0x0018			Register Name: TVE_018_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	/	/	/
27:16	R/W	0x0	BROAD_PLUS_CYCLE_NUMBER_IN_HD_MODE_VSYNC
15:12	/	/	/
11:0	R/W	0x16	FRONT_PORCH_LIKE_IN_HD_MODE_VSYNC

7.5.4.15. TV Encoder Line Number Register(Default Value: 0x0016_020D)

Offset: 0x001C			Register Name: TVE_01C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x16	FIRST_VIDEO_LINE Specify the index of the first line in a field/frame to have active video. 8 bits unsigned integer. For interlaced video: When VSync5=B'0', FirstVideoLine is restricted to

Offset: 0x001C			Register Name: TVE_01C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			be greater than 7. When VSync5=B'1', FirstVideoLine is restricted to be greater than 9. Default value is 21.
15:11	/	/	/
10:0	R/W	0x20D	NUM_LINES Specify the total number of lines in a video frame. 11 bits unsigned integer. Allowed range is 0 to 2048. Default value is 525. For interlaced video: When NTSC, and FirstVideoLine is greater than 20, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When NTSC, and FirstVideoLine is not greater than 20, then NumLines is restricted to be greater than 77. When PAL, and FirstVideoLine is greater than 22, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When PAL, and FirstVideoLine is not greater than 22, then NumLines is restricted to be greater than 81. If NumLines is even, then it is restricted to be divisible by 4. If NumLines is odd, then it is restricted to be divisible by 4 with a remainder of 1.

7.5.4.16. TV Encoder Level Register(Default Value: 0x00F0_011A)

Offset: 0x0020			Register Name: TVE_020_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0xf0	BLANK_LEVEL Specify the blank level setting for active lines. 10 bits unsigned integer. Allowed range 0 to 1023. Default value is 0xF0(dec240).
15:10	/	/	/
9:0	R/W	0x11a	BLACK_LEVEL Specify the black level setting. 10 bits unsigned integer. Allowed range is 240 to 1023. Default value is 282.

7.5.4.17. TV Encoder Auto Detection Enable Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: TVE_030_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	DAC3_AUTO_DETECT_INTERRUPT_EN
18	R/W	0x0	DAC2_AUTO_DETECT_INTERRUPT_EN
17	R/W	0x0	DAC1_AUTO_DETECT_INTERRUPT_EN
16	R/W	0x0	DAC0_AUTO_DETECT_INTERRUPT_EN
15:4	/	/	/
3	R/W	0x0	DAC3_AUTO_DETECT_ENABLE
2	R/W	0x0	DAC2_AUTO_DETECT_ENABLE
1	R/W	0x0	DAC1_AUTO_DETECT_ENABLE
0	R/W	0x0	DAC0_AUTO_DETECT_ENABLE

7.5.4.18. TV Encoder Auto Detection Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: TVE_034_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	DAC3_AUTO_DETECT_INTERRUPT_ACTIVE_FLAG Write 1 to inactive DAC3 auto detection interrupt
2	R/W	0x0	DAC2_AUTO_DETECT_INTERRUPT_ACTIVE_FLAG Write 1 to inactive DAC2 auto detection interrupt
1	R/W	0x0	DAC1_AUTO_DETECT_INTERRUPT_ACTIVE_FLAG Write 1 to inactive DAC1 auto detection interrupt
0	R/W	0x0	DAC0_AUTO_DETECT_INTERRUPT_ACTIVE_FLAG Write 1 to inactive DAC0 auto detection interrupt

7.5.4.19. TV Encoder Auto Detection Status Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: TVE_038_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	DAC3_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved
23:18	/	/	/
17:16	R/W	0x0	DAC2_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved
15:10	/	/	/
9:8	R/W	0x0	DAC1_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved
7:2	/	/	/
1:0	R/W	0x0	DAC0_STATUS 00: Unconnected 01: Connected 11: Short to ground 10: Reserved

7.5.4.20. TV Encoder Auto Detection Debounce Setting Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: TVE_03C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x003C			Register Name: TVE_03C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x0	DAC_Test_Register
15:12	R/W	0x0	DAC3_De_Bounce_Times
11:8	R/W	0x0	DAC2_De_Bounce_Times
7:4	R/W	0x0	DAC1_De_Bounce_Times
3:0	R/W	0x0	DAC0_De_Bounce_Times

7.5.4.21. TV Encoder Auto Detection Configuration Register0(Default Value: 0x0000_0000)

Offset: 0x00F8			Register Name: TVE_0F8_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:0	R/W	0x0	DETECT_Pulse_Value Use for DAC data input at auto detect pluse

7.5.4.22. TV Encoder Auto Detection Configuration Register1(Default Value: 0x0000_0000)

Offset: 0x00FC			Register Name: TVE_0FC_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:16	R/W	0x0	DETECT_PULSE_PERIODS Use 32K clock
15	/	/	/
14:0	R/W	0x0	DETECT_PULSE_START

7.5.4.23. TV Encoder Color Burst Phase Reset Configuration Register (Default Value: 0x0000_0001)

Offset: 0x0100			Register Name: TVE_100_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1:0	R/W	0x1	COLOR_PHASE_RESET Color burst phase period selection These bits select the number of fields or lines after which the color burst phase is reset to its initial value as specified by the ChromaPhase parameter, This parameter is application only for interlaced video. 00: 8 field 01: 4 field 10: 2 lines 11: only once

7.5.4.24. TV Encoder VSYNC Number Register (Default Value: 0x0000_0000)

Offset: 0x0104			Register Name: TVE_104_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0104			Register Name: TVE_104_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	VSync5 Number of equalization pulse selection This bit selects whether the number of equalization pulses is 5 or 6. This parameter is applicable only for interlaced video. 0: 5 equalization pulse(default) 1: 6 equalization pulses

7.5.4.25. TV Encoder Notch Filter Frequency Register (Default Value: 0x0000_0002)

Offset: 0x0108			Register Name: TVE_108_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R/W	0x2	NOTCH_FREQ Luma notch filter center frequency selection These bits select the luma notch filter (which is a band-reject filter) center frequency. In two of the selections, the filter width affects also the selection of the center frequency. 000: 1.1875 001: 1.1406 010: 1.0938 when notch_wide value is B‘1’ (this selection is proper for CCIR-NTSC), or 1.0000 when notch_wide value is B‘0’ 011: 0.9922. This selection is proper for NTSC with square pixels 100: 0.9531. This selection is proper for PAL with square pixel 101: 0.8359 when notch_wide value is B‘1’ (this selection is proper for CCIR-PAL), or 0.7734 when notch_wide value is B‘0’ 110: 0.7813 111: 0.7188

7.5.4.26. TV Encoder Cb/Cr Level/Gain Register (Default Value: 0x0000_004F)

Offset: 0x010C			Register Name: TVE_10C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x0	Cr_Burst_Level Specify the amplitude of the Cr burst. 8 bit 2’s complement integer. Allowed range is (-127) to 127. Default value is 0.
7:0	R/W	0x4f	Cb_Burst_Level Specify the amplitude of the Cb burst. 8 bit 2’s complement integer. Allowed range is (-127) to 127. Default value is 60.

7.5.4.27. TV Encoder Tint and Color Burst Phase Register (Default Value: 0x0000_0000)

Offset: 0x0110			Register Name: TVE_110_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/

Offset: 0x0110			Register Name: TVE_110_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
23:16	R/W	0x0	TINT Specify the tint adjustment of the chroma signal for CVBS and Y/C outputs. The adjustment is effected by setting the sub-carrier phase to the value of this parameter. 8.8 bit unsigned fraction. Units are cycles of the color burst frequency. Default value is 0.
15:8	/	/	/
7:0	R/W	0x0	CHROMA_PHASE Specify the color burst initial phase (*ChromaPhase)*. 8 bit unsigned fraction. Units are cycles of the color burst frequency. Default value is X'00'. The color burst is set to this phase at the first *HSYNC* and then reset to the same value at further *HSYNC*s as specified by the *CPhaseRset* bits of the *EncConfig5* parameter (see above)

7.5.4.28. TV Encoder Burst Width Register (Default Value: 0x0016_447E)

Offset: 0x0114			Register Name: TVE_114_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	BACK_PORCH Breezeway like in HD mode VSync 720p mode, is 220 2080i/p mode is 88(default)
23	/	/	/
22:16	R/W	0x16	BREEZEWAY Must be even. Specify the width of the breezeway in encoder clock cycles. 5 bit unsigned integer. Allowed range is 0 to 31. Default value is 22 In 1080i mode, is 44 In 1080p mode, is 44 In 720p mode,is 40
15	/	/	/
14:8	R/W	0x44	BURST_WIDTH Specify the width of the color frequency burst in encoder clock cycles. 7 bit unsigned integer. Allowed range is 0 to 127. Default value is 68. In hd mode, ignored
7:0	R/W	0x7e	HSYNC_WIDTH Specify the width of the horizontal sync pulse in encoder clock cycles. Min value is 16. Max value is (*FrontPorch + ActiveLine - BackPorch*). Default value is 126. The sum of *HSyncSize* and *BackPorch* is restricted to be divisible by 4. In 720p mode, is 40 In 1080i/p mode, is 44

7.5.4.29. TV Encoder Cb/Cr Gain Register (Default Value: 0x0000_A0A0)

Offset: 0x0118			Register Name: TVE_118_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/

Offset: 0x0118			Register Name: TVE_118_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0xa0	CR_GAIN Specify the Cr color gain. 8 bit unsigned fraction. Default value is 139.
7:0	R/W	0xa0	CB_GAIN Specify the Cb color gain. 8 bit unsigned fraction. Default value is 139.

7.5.4.30. TV Encoder Cb/Cr Gain Register (Default Value: 0x0010_00F0)

Offset: 0x011C			Register Name: TVE_11C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:16	R/W	0x10	Sync_Level Specify the sync pulse level setting. 8 bit unsigned integer. Allowed range is 0 to *ABlankLevel*-1 or *VBlankLevel*-1 (whichever is smaller).
15:10	/	/	/
9:0	R/W	0xf0	VBlank_Level Specify the blank level setting for non active lines. 10 bit unsigned integer. Allow range 0 to 1023.

7.5.4.31. TV Encoder White Level Register (Default Value: 0x01E8_0320)

Offset: 0x0120			Register Name: TVE_120_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31::26	/	/	/
25:16	R/W	0x1e8	HD_SYNC_BREEZEWAY_LEVEL Specify the breezeway level setting. 10 bit unsigned integer. Allowed range is 0 to 1023. Default value is 488.
15:10	/	/	/
9:0	R/W	0x320	WHITE_LEVEL Specify the white level setting. 10 bit unsigned integer. Allowed range is black_level+1 or vbi_blank_level +1 (whichever is greater) to 1023. Default value is 800.

7.5.4.32. TV Encoder Video Active Line Register (Default Value: 0x0000_05A0)

Offset: 0x0124			Register Name: TVE_124_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	/	/	/
11:0	R/W	0x5A0	ACTIVE_LINE Specify the width of the video line in encoder clock cycles. 12 bit unsigned multiple of 4 integer. Allowed range is 0 to 4092 Default value is 1440.

7.5.4.33. TV Encoder Video Chroma BW and CompGain Register (Default Value: 0x0000_0000)

Offset: 0x0128			Register Name: TVE_128_REG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0128			Register Name: TVE_128_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:18	/	/	/
17:16	R/W	0x0	CHROMA_BW Chroma filter bandwidth selection This bit specifies whether the bandwidth of the chroma filter is: 00: Narrow width, 0.6MHz 01: Wide width 1.2MHz. 10: Extra width 1.8MHz 11: Ultra width 2.5MHz Default is 0.6MHz(value 0)
15:2	/	/	/
1:0	R/W	0x0	COMP_CH_GAIN Chroma gain selection for the composite video signal. These bits specify the gain of the chroma signal for composing with the luma signal to generate the composite video signal: 00: 100% (B'00'), 01: 25% 10: 50% 11: 75%

7.5.4.34. TV Encoder Register (Default Value: 0x0000_0101)

Offset: 0x012C			Register Name: TVE_12C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x1	NOTCH_WIDTH Luma notch filter width selection This bit selects the luma notch filter (which is a band-reject filter) width. 0: Narrow 1: Wide
7:1	/	/	/
0	R/W	0x1	COMP_YUV_EN This bit selects if the components video output are the RGB components or the YUV components. 0: The three component outputs are the RGB components. 1: The three component outputs are the YUV components, (i.e. the color conversion unit is by-passed)

7.5.4.35. TV Encoder Re-sync Parameters Register (Default Value: 0x0010_0001)

Offset: 0x0130			Register Name: TVE_130_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RE_SYNC_FIELD
30	R/W	0x0	RE_SYNC_DIS 0: Re-Sync Enable

Offset: 0x0130			Register Name: TVE_130_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Re-Sync Disable
29:27	/	/	/
26:16	R/W	0x10	RE_SYNC_LINE_NUM
15:11	/	/	/
10:0	R/W	0x1	RE_SYNC_PIXEL_NUM

7.5.4.36. TV Encoder Slave Parameter Register (Default Value: 0x0000_0000)

Offset: 0x0134			Register Name: TVE_134_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	Slave_Thresh Horizontal line adjustment threshold selection This bit selects whether the number of lines after which the Video Encoder starts the horizontal line length adjustment is slave mode is 0 or 30. 0: Number of lines is 0 1: Number of lines is 30
7:1	/	/	/
0	R/W	0x0	Slave_Mode Slave mode selection This bit selects whether the Video Encoder is sync slave, partial slave or sync master. It should be set to B‘0’. 0: The Video Encoder is not a full sync slave (i.e. it is a partial sync slave or a sync master) 1: Reserved

7.5.4.37. TV Encoder Configuration Register0 (Default Value: 0x0000_0000)

Offset: 0x0138			Register Name: TVE_138_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	INVERT_TOP Field parity input signal (top_field) polarity selection. This bit selects whether the top field is indicated by a high level of the field parity signal or by the low level. The bit is applicable both when the Video Encoder is the sync master and when the Video Encoder is the sync slave. 0: Top field is indicated by low level 1: Top field is indicated by high level
7:1	/	/	/
0	R/W	0x0	UV_ORDER This bit selects if the sample order at the chroma input to the Video Encoder is Cb first (i.e. Cb 0 Cr 0 Cb 1 Cr 1) or Cr first (i.e. Cr 0 Cb 0 Cr 1 Cb 1).

Offset: 0x0138			Register Name: TVE_138_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: The chroma sample input order is Cb first 1: The chroma sample input order is Cr first

7.5.4.38. TV Encoder Configuration Register1 (Default Value: 0x0000_0001)

Offset: 0x013C			Register Name: TVE_13C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:27	/	/	/
26:24	R/W	0x0	RGB_SYNC R, G and B signals sync embedding selection. These bits specify whether the sync signal is added to each of the R, G and B components (B'1') or not (B'0'). Bit [26] specify if the R signal have embedded syncs, bit [25] specify if the G signal have embedded syncs and bit [24] specify if the B signal have embedded syncs. When comp_yuv is equal to B'1', these bits are N.A. and should be set to B'000'. When the value is different from B'000', **RGB_SETUP** should be set to B'1'.
23:17	/	/	/
16	R/W	0x0	RGB_SETUP "Set-up" enable for RGB outputs. This bit specifies if the "set-up" implied value (black_level – blank_level) specified for the CVBS signal is used also for the RGB signals. 0: The "set-up" is not used, or N.A. i.e. comp_yuv is equal to B'1'. 1: The implied "set-up" is used for the RGB signals
15:1	/	/	/
0	R/W	0x1	BYPASS_YCLAMP Y input clamping selection This bit selects whether the Video Encoder Y input is clamped to 64 to 940 or not. When not clamped the expected range is 0 to 1023. The U and V inputs are always clamped to the range 64 to 960. 0: The Video Encoder Y input is clamped 1: The Video Encoder Y input is not clamped

7.5.4.39. TV Encoder Low Pass Control Register(Default Value: 0x0000_0000)

Offset: 0x0380			Register Name: TVE_380_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:10	R/W	0x0	USER_DEFLICKER_COEF up : coef/32 Center :1-coef/16 Down :coef/32
9	R/W	0x0	FIX_COEF_DEFLICKER 0: Auto deflicker 1: User deflicker

Offset: 0x0380			Register Name: TVE_380_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
8	R/W	0x0	ENABLE_DEFLICKER 0: Disable deflicker 1: Enable deflicker
7:1	/	/	/
0	R/W	0x0	EN LP function enable 0: Disable 1: Enable

7.5.4.40. TV Encoder Low Pass Filter Control Register(Default Value: 0x0000_0000)

Offset: 0x0384			Register Name: TVE_384_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/	/	/
21:16	R/W	0x0	HP_RATIO Default high-pass filter ratio In two's complement. Range from -31 to 31.
15:14	/	/	/
13:8	R/W	0x0	BP0_RATIO Default band-pass filter0 ratio In two's complement. Range from -31 to 31.
7:6	/	/	/
5:0	R/W	0x0	BP1_RATIO Default band-pass filter1 ratio In two's complement. Range from -31 to 31.

7.5.4.41. TV Encoder Low Pass Gain Register(Default Value: 0x0000_0000)

Offset: 0x0388			Register Name: TVE_388_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	GAIN Peaking gain setting.

7.5.4.42. TV Encoder Low Pass Gain Control Register(Default Value: 0x0000_0000)

Offset: 0x038C			Register Name: TVE_38C_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	DIF_UP Gain control: limitation threshold.
15:8	/	/	/
4:0	R/W	0x0	BETA Gain control: large gain limitation.

7.5.4.43. TV Encoder Low Pass Shoot Control Register(Default Value: 0x0000_0000)

Offset: 0x0390			Register Name: TVE_390_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5:0	R/W	0x0	NEG_GAIN Undershoot gain control.

7.5.4.44. TV Encoder Low Pass Coring Register(Default Value: 0x0000_0000)

Offset: 0x0394			Register Name: TVE_394_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	CORTHR Coring threshold.

7.5.4.45. TV Encoder Noise Reduction Register(Default Value: 0x0000_0000)

Offset: 0x03A0			Register Name: TVE_3A0_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	T_Value
15:1	/	/	/
0	R/W	0x0	EN

Chapter 8. Interfaces

This section details the interfaces that provided in A40i, mainly includes:

- TWI
- SPI
- UART
- PS2
- CIR
- USB OTG
- USB Host
- I2S/PCM
- AC97 Interface
- EMAC
- GMAC
- Transport Stream Controller
- Smart Card Reader
- SATA Host
- Keypad
- OWA

8.1. TWI

8.1.1. Overview

The TWI is designed to be used as an interface between CPU host and the serial 2-Wire bus. It can support all standard 2-Wire transfer, including slave and master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This TWI can be operated in standard mode (100kbit/s) or fast-mode, supporting data rate up to 400kbit/s. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in slave mode.

Features:

- 5 TWI controllers
- Software-programmable for Slave or Master
- Supports Repeated START signal
- Supports multi-master systems
- Allows 10-bit addressing with 2-Wire bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speed up to 400kbit/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

8.1.2. Operations and Functional Descriptions

8.1.2.1. External Signals

Table 8-1 describes the external signals of TWI. TWI_SCK and TWI_SDA are bidirectional I/O, When TWI is configured as Master device, TWI_SCK is output pin; when TWI is configurable as Slave device, TWI_SCK is input pin. The unused TWI ports are used as General Purpose I/O ports. For information about General Purpose I/O ports, see **Port Controller** in chapter3.

Table 8-1. TWI External Signals

Signal	Description	Type
TWIx_SCK (x=0~4)	TWI Clock Signal	I/O
TWIx_SDA (x=0~4)	TWI Serial Data	I/O

8.1.2.2. Clock Sources

TWI is on APB2 BUS, APB2 BUS has three different clocks. Table 8-2 describes the clock sources for TWI. Users can see **CCU** in chapter3 for clock setting, configuration and gating information.

Table 8-2. TWI Clock Sources

Clock Sources		Description
APB2	LOSC	32KHz Crystal
	OSC24M	24MHz Crystal
	PLL_PERIPH0(2X)	Peripheral Clock,default value of 2X is 1.2GHz

8.1.2.3. TWI Master and Slave Mode

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupted the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

8.1.2.4. TWI Timing Diagram

Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each byte. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a “not acknowledge”) to the transmitter.

When a slave receiver doesn’t acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Following diagram provides an illustration the relation of SDA signal line and SCL signal line on the TWI serial bus.

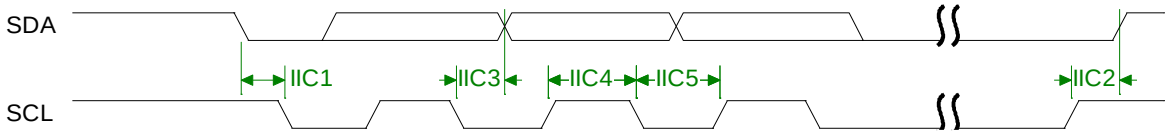


Figure 8-1. TWI Timing Diagram

8.1.3. Register List

Module Name	Base Address
TWI0	0x01C2AC00

Module Name	Base Address
TWI1	0x01C2B000
TWI2	0x01C2B400
TWI3	0x01C2B800
TWI4	0x01C2C000

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave Address
TWI_XADDR	0x0004	TWI Extended Slave Address
TWI_DATA	0x0008	TWI Data Byte
TWI_CNTR	0x000C	TWI Control Register
TWI_STAT	0x0010	TWI Status Register
TWI_CCR	0x0014	TWI Clock Control Register
TWI_SRST	0x0018	TWI Software Reset
TWI_EFR	0x001C	TWI Enhance Feature Register
TWI_LCR	0x0020	TWI Line Control Register

8.1.4. Register Description

8.1.4.1. TWI Slave Address Register(Default Value:0x0000_0000)

Offset: 0x0000			Register Name: TWI_ADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:1	R/W	0x0	SLA Slave address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0x0	GCE General call address enable 0: Disable 1: Enable

NOTE

For 7-bit addressing: SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the 2-Wire bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing: When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

8.1.4.2. TWI Extend Address Register(Default Value:0x0000_0000)

Offset: 0x0004			Register Name: TWI_XADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SLAX Extend Slave Address SLAX[7:0]

8.1.4.3. TWI Data Register(Default Value:0x0000_0000)

Offset: 0x0008			Register Name: TWI_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	TWI_DATA Data byte for transmitting or received

8.1.4.4. TWI Control Register(Default Value:0x0000_0000)

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt line always low 1: The interrupt line will go high when **INT_FLAG** is set.
6	R/W	0x0	BUS_EN TWI Bus Enable 0: The TWI bus inputs ISDA/ISCL are ignored and the TWI Controller will not respond to any address on the bus 1: The TWI will respond to calls to its slave address and the general call address if the **GCE** bit in the **TWI_ADDR** is set. **NOTE** **In master operation mode, this bit should be set to '1'.**
5	R/WAC	0x0	M_STA Master Mode Start When **M_STA** is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the **M_STA** bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the **M_STA** bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The **M_STA** bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect.
4	R/W1C	0x0	M_STP Master Mode Stop

Offset: 0x000C			Register Name: TWI_CNTR
Bit	**Read/Write**	**Default/Hex**	**Description**
			If **M_STP** is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the **M_STP** bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and **M_STP** bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition. The **M_STP** bit is cleared automatically, writing a '0' to this bit has no effect.
3	R/W1C	0x0	INT_FLAG Interrupt Flag **INT_FLAG** is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see '**TWI_STAT**' below). The only state that does not set **INT_FLAG** is state F8h. If the **INT_EN** bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when **INT_FLAG** is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to **INT_FLAG**. The TWI clock line is then released and the interrupt line goes low.
2	R/W	0x0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if: (1). Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. (2). The general call address has been received and the **GCE** bit in the **TWI_ADDR** register is set to '1'. (3). A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the **TWI_DATA** register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when **INT_FLAG** is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

8.1.4.5. TWI Status Register(Default Value:0x0000_00F8)

Offset: 0x0010			Register Name: TWI_STAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0xF8	STA Status Information Byte **Code Status** 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received

Offset: 0x0010			Register Name: TWI_STAT
Bit	**Read/Write**	**Default/Hex**	**Description**
			0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

8.1.4.6. TWI Clock Register(Default Value:0x0000_0000)

Offset: 0x0014			Register Name: TWI_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:3	R/W	0x0	CLK_M
2:0	R/W	0x0	CLK_N The TWI bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48MHz/2^2=12Mhz, F1= F0/(10*(2+1)) = 0.4MHz For 100kHz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48MHz/2^2=12Mhz, F1=F0/(10*(11+1)) = 0.1MHz

8.1.4.7. TWI Soft Reset Register(Default Value:0x0000_0000)

Offset: 0x0018			Register Name: TWI_SRST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/WAC	0x0	SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation.

8.1.4.8. TWI Enhance Feature Register(Default Value:0x0000_0000)

Offset: 0x001C			Register Name: TWI_EFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
0:1	R/W	0x0	DBN Data Byte number follow Read Command Control 00: No Data Byte to be written after read command 01: Only 1 byte data to be written after read command 10: 2 bytes data can be written after read command 11: 3 bytes data can be written after read command

8.1.4.9. TWI Line Control Register(Default Value:0x0000_0000)

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R	0x1	SCL_STATE Current state of TWI_SCL 0: Low 1: High
4	R	0x1	SDA_STATE Current state of TWI_SDA 0: Low 1: High
3	R/W	0x1	SCL_CTL TWI_SCL line state control bit When line control mode is enabled (bit[2] set), the value of this bit decides the output level of TWI_SCL. 0: Output low level 1: Output high level
2	R/W	0x0	SCL_CTL_EN TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3].

Offset: 0x0020			Register Name: TWI_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Disable TWI_SCL line control mode 1: Enable TWI_SCL line control mode
1	R/W	0x1	SDA_CTL TWI_SDA line state control bit When line control mode is enabled (bit[0] set), the value of this bit decides the output level of TWI_SDA. 0: Output low level 1: Output high level
0	R/W	0x0	SDA_CTL_EN TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0: Disable TWI_SDA line control mode 1: Enable TWI_SDA line control mode

8.1.4.10. TWI DVFS Control Register(Default Value:0x0000_0000)

Offset: 0x0024			Register Name: TWI_DVFSCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
2	R/W	0x0	MS_PRIORITY CPU and DVFS BUSY set priority select 0: CPU has higher priority 1: DVFS has higher priority
1	R/W	0x0	CPU_BUSY_SET CPU Busy set
0	R/W	0x0	DVFC_BUSY_SET DVFS Busy set

NOTE

This register is only implemented in TWI0.

8.2. SPI

8.2.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with fewer software interrupts. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode.

Features:

- 4 SPI controllers
- Full-duplex synchronous serial interface
- Master/Slave configurable
- Each SPI has 2 chip select signals
- 8-bit wide by 64-entry FIFO for both transmit and receive date
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Interrupt or DMA supported
- 1-,or 2-wire mode
- The maximum frequency is 100MHz

8.2.2. Block Diagram

Figure 8-2 shows a block diagram of the SPI.

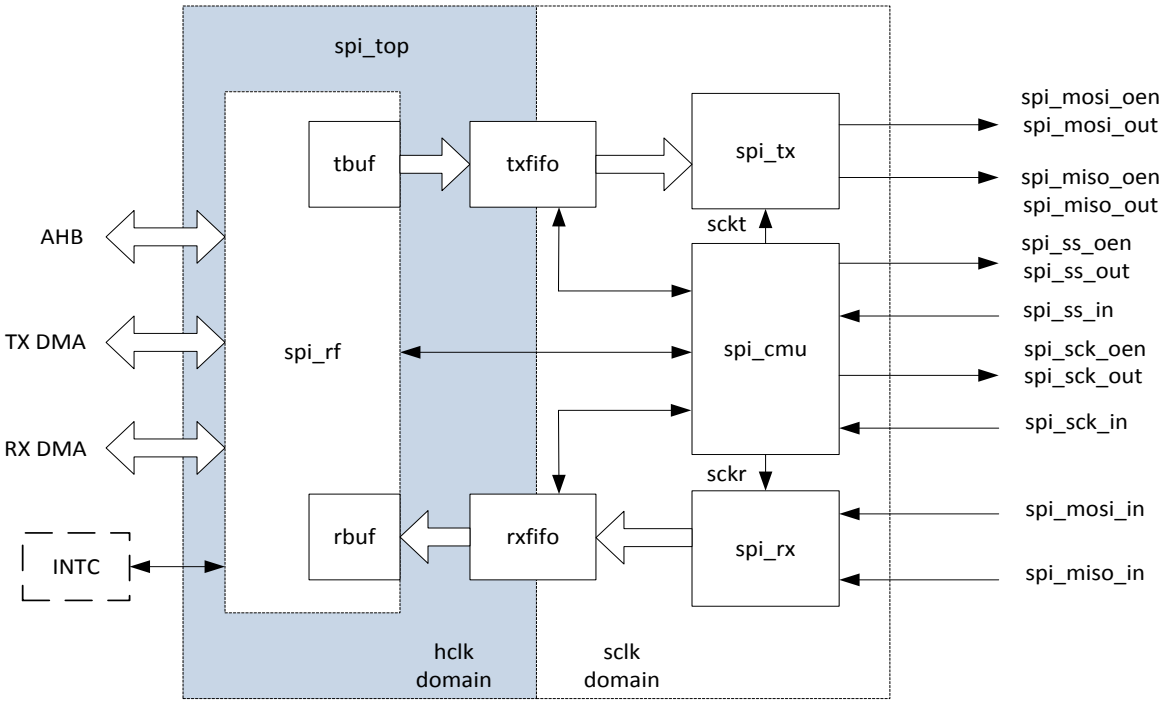


Figure 8-2. SPI Block Diagram

The SPI comprises with:

spi_rf: Responsible for implementing the internal register,interrupt and DMA Request.

spi_tbuf: The data length transmitted from AHB to txfifo is converted into 8bits,then the data is written into the rxfifo.

spi_rbuf: The block is used as converted the rxfifo data into read data length of AHB.

txfifo,rxfifo: For transmit and receive transfers,data transmitted from the SPI to the external serial device is written into the txfifo;data received from the external serial device into SPI is pushed into the rxfifo.

spi_cmu: Responsible for implementing SPI bus clock,chip select,internal sample and the generation of transfer clock.

spi_tx: Responsible for implementing SPI data transfer ,the interface of the internal txfifo and status register.

spi_rx: Responsible for implementing SPI data receive, the interface of the internal rxfifo and status register.

8.2.3. Operations and Functional Descriptions

8.2.3.1. External Signals

Table 8-3 describes the external signals of SPI. MOSI and MISO are bidirectional I/O,When SPI is configured as Master device,CLK and CS is output pin;when SPI is configurable as Slave device,CLK and CS is input pin.The unused SPI ports are used as General Purpose I/O ports.

Table 8-3. SPI External Signals

Signal	Description	Type
SPI0_CS	SPI0 Chip Select Signal,Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI1_CS	SPI1 Chip Select Signal,Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI2_CS[1:0]	SPI2 Chip Select Signal,Low Active	I/O
SPI2_CLK	SPI2 Clock Signal	I/O
SPI2_MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2_MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI3_CS[1:0]	SPI3 Chip Select Signal,Low Active	I/O
SPI3_CLK	SPI3 Clock Signal	I/O
SPI3_MOSI	SPI3 Master Data Out, Slave Data In	I/O
SPI3_MISO	SPI3 Master Data In, Slave Data Out	I/O

8.2.3.2. Clock Sources

Each SPI controller get three different clocks, users can select one of them to make SPI Clock Source. Table 8-4 describes the clock sources for SPI.

Table 8-4. SPI Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal

PLL_PERIPH0(1X)	Peripheral Clock,default value is 600MHz
PLL_PERIPH1(1X)	Peripheral Clock,default value is 600MHz

8.2.3.3. Typical Application

Figure 8-3 shows the application block diagram when the SPI master device is connected to a slave device.

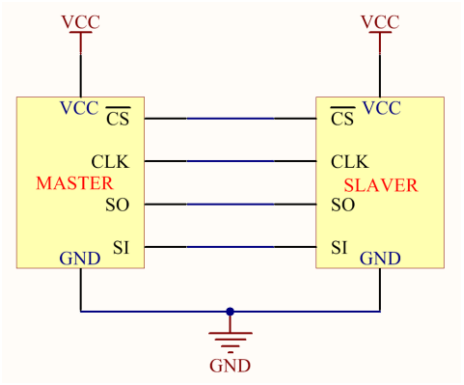


Figure 8-3. SPI Application Block Diagram

8.2.3.4. SPI Transmit Format

The SPI supports 4 different formats for data transfer. Software can select one of the four modes in which the SPI works by setting the bit1(Polarity) and bit0(Phase) of **SPI Transfer Control Register**. The SPI controller master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed in Table 8-5.

Table 8-5. SPI Transmit Mode0~3

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

Figure 8-4 and Figure 8-5 describe four waveforms for SPI.

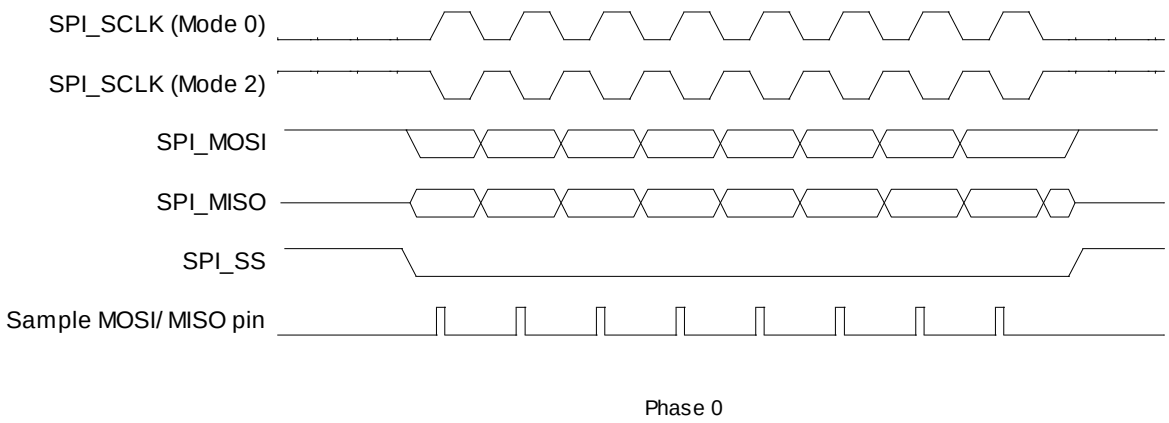


Figure 8-4. SPI Phase 0 Timing Diagram

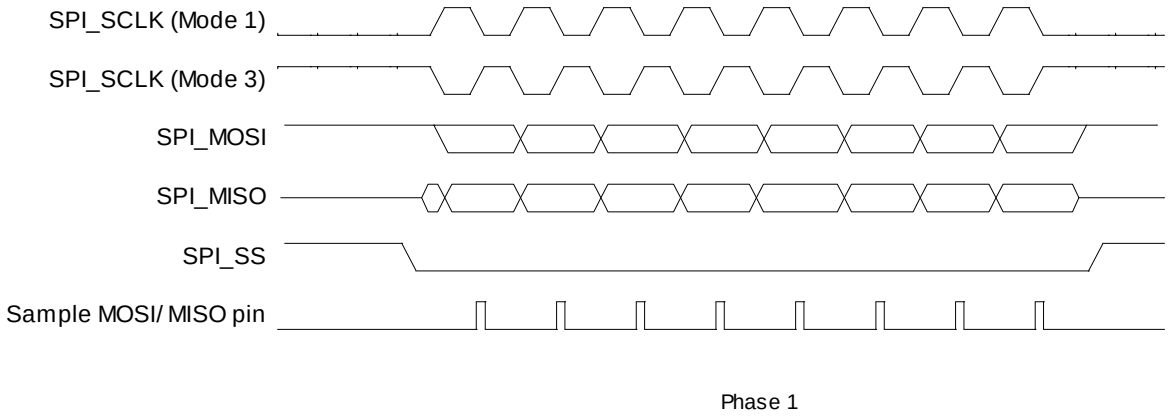


Figure 8-5. SPI Phase 1 Timing Diagram

8.2.3.5. SPI Master and Slave Mode

The SPI controller can be configured to a Master or Slave device.Master mode is selected by setting the **MODE** bit in the **SPI Global Control Register**;Slave mode is selected by clearing the the **MODE** bit in the **SPI Global Control Register**.

In Master mode,SPI_CLK is generated and transmitted to external device,and data from the TX FIFO is transmitted on the MOSI pin,the data from slave is received on the MISO pin and sent to RX FIFO.Chip Select(SPI_SS) is active low signal. SPI_SS must be set low before data are transmitted or received.SPI_SS can be selected SPI auto control or software manual control.When using auto control,**SS_OWNER** (the bit 6 in the **SPI Transfer Control Register**) must be cleared(default value is 0);when using manual control,**SS_OWNER** must be set,Chip Select level is controlled by **SS_LEVEL** bit(the bit 7 in the **SPI Transfer Control Register**).

In Slave mode,After software selects the **MODE** bit to '0',it waits for master initiate a transaction.When the Master assert SPI_SS and SPI_CLK is transmitted to the Slave,the Slave data is transmitted from TX FIFO on MISO pin and data from MOSI pin is received in RX FIFO.

8.2.3.6. SPI Dual Mode

The Dual read mode(SPI x2) is selected when the **DRM**(bit28) is set in the **SPI Master Burst Control Counter Register**.Using the dual mode allows data to be transferred to or from the device at two times the rate of standard single mode SPI devices,data can be read at fast speed using two data bits(MOSI and MISO) at a time.

8.2.4. Programming Guidelines

8.2.4.1. Transmit/Receive Burst in Master Mode

In SPI Master mode,The transmit and receive burst(byte in unit) are configured before the SPI transfers serial data between the processor and external device.The transmit burst write in **MWTC** (bit[23:0]) of **SPI Master Transmit Counter Register**. The transmit burst in single mode before automatically sending dummy burst write in **STC**(bit[23:0]) of **SPI Master Burst Control Counter Register.**For dummy data,SPI controller can automatically sent before receive by writing **DBC**(bit[27:24]) in **SPI Master Burst Control Counter Register**.If users don't use SPI controller to sent automatically dummy,then dummy burst are used as the transmit counters to write together in **MWTC** (bit[23:0]) of **SPI Master Transmit Counter Register**.In Master mode,the total burst numbers write in **MBC**(bit[23:0]) of **SPI Master Burst Counter Register**.When all master transmit burst and receive burst are transferred, SPI controller will send a completed interrupt,at the same time,SPI controller will clear **DBC**,**MWTC** and **MBC**.

8.2.4.2. CPU or DMA Operation

The SPI transfers serial data between the processor and external device. CPU and DMA are the two main operational modes for SPI. For each SPI, data is simultaneously transmitted(shifted out serially) and received (shifted in serially).SPI has 2 channels, TX channel and RX channel. TX channel has the path from TX FIFO to external device. RX channel has the path from external device to RX FIFO.

Write Data: CPU or DMA must write data on the register SPI_TXD, data on the register are automatically moved to TX FIFO.

Read Data: To read data from RX FIFO,CPU or DMA must access the register SPI_RXD and data are automatically sent to the register SPI_RXD.

In CPU or DMA mode, the SPI sends an completed interrupt(the TC bit in SPI Interrupt Status Register) to the processor at the end of each transfer.

(1).CPU Mode

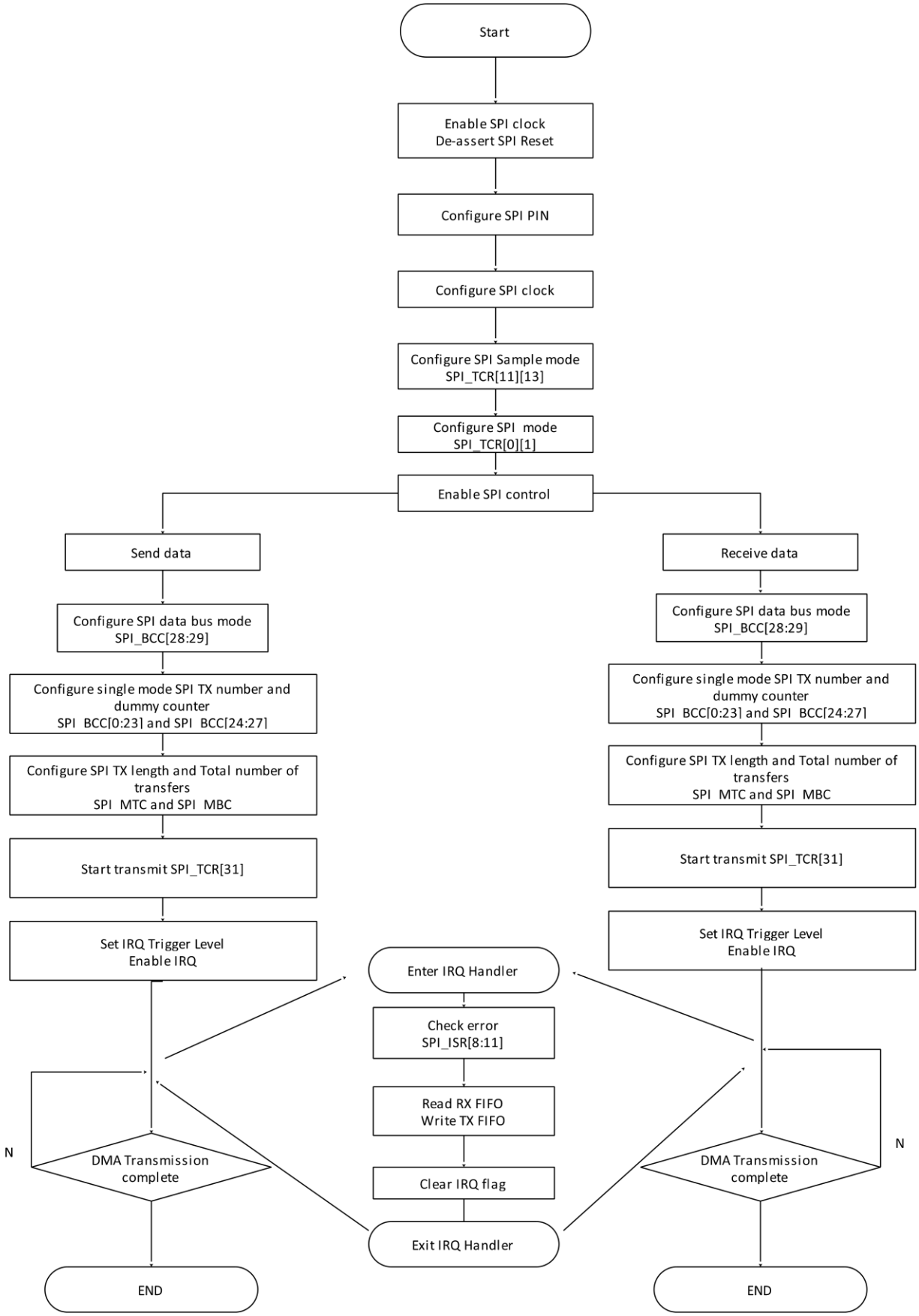


Figure 8-6. SPI Write/Read Data in CPU Mode

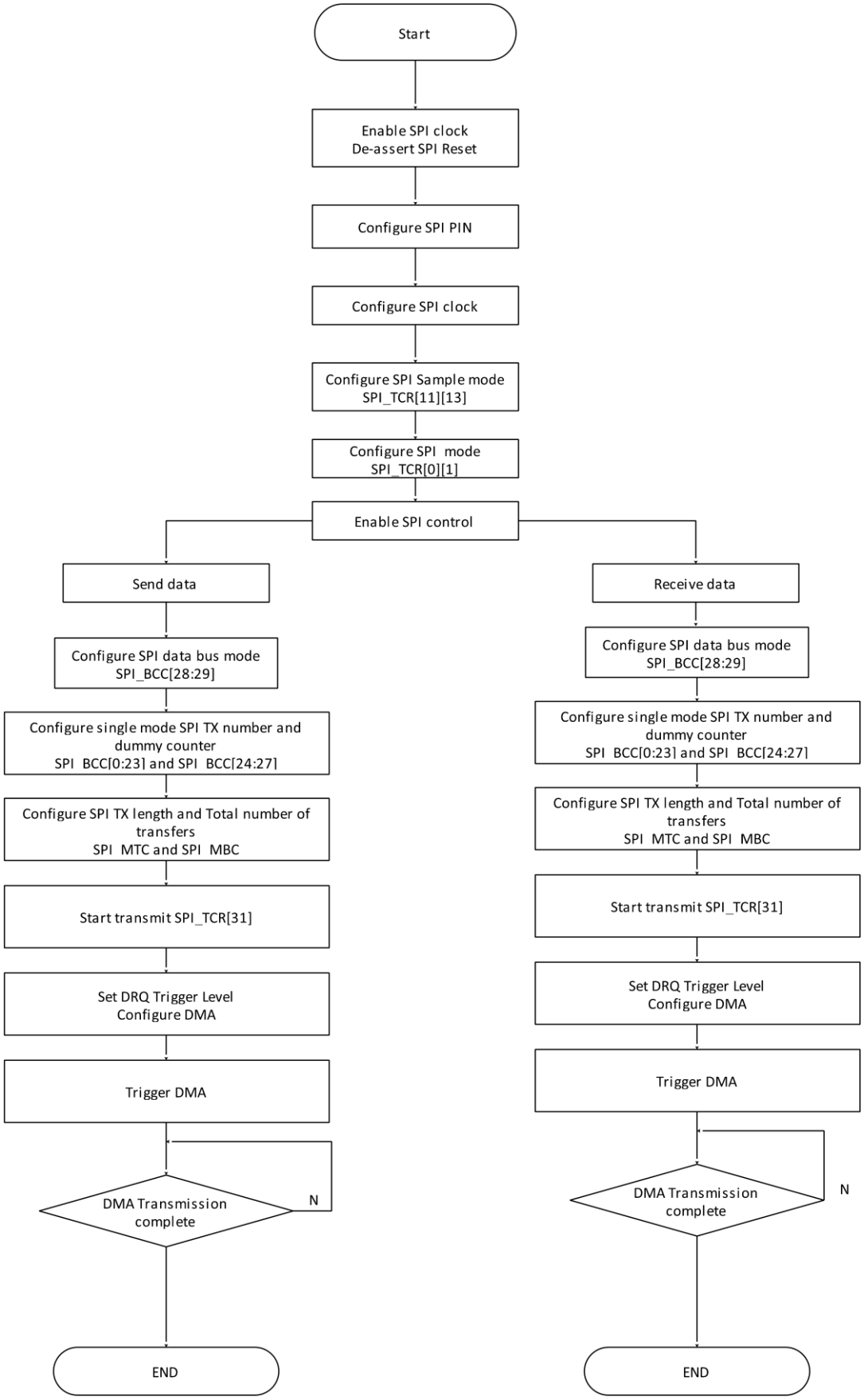


Figure 8-7. SPI Write/Read Data in DMA Mode

8.2.5. Register List

Module Name	Base Address
SPI0	0x01C05000
SPI1	0x01C06000
SPI2	0x01C17000
SPI3	0x01C1F000

Register Name	Offset	Description
SPI_GCR	0x0004	SPI Global Control Register
SPI_TCR	0x0008	SPI Transfer Control Register
/	0x000C	Reserved
SPI_IER	0x0010	SPI Interrupt Control Register
SPI_ISR	0x0014	SPI Interrupt Status Register
SPI_FCR	0x0018	SPI FIFO Control Register
SPI_FSR	0x001C	SPI FIFO Status Register
SPI_WCR	0x0020	SPI Wait Clock Counter Register
SPI_CCR	0x0024	SPI Clock Rate Control Register
/	0x0028	Reserved
/	0x002C	Reserved
SPI_MBC	0x0030	SPI Burst Counter Register
SPI_MTC	0x0034	SPI Transmit Counter Register
SPI_BCC	0x0038	SPI Burst Control Register
SPI_NDMA_MODE_CTL	0x0088	SPI Normal DMA Mode Control Register
SPI_TXD	0x0200	SPI TX Data Register
SPI_RXD	0x0300	SPI RX Data Register

8.2.6. Register Description

8.2.6.1. SPI Global Control Register(Default Value: 0x0000_0080)

Offset: 0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	SRST Soft reset Writing '1' to this bit will clear the SPI controller, and automatically clear to '0' when reset operation completes. Writing '0' has no effect.
30:8	/	/	/
7	R/W	0x1	TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 0 : Normal operation, ignore RXFIFO status 1 : Stop transmit data when RXFIFO full **NOTE** **Can not be written when XCH=1.**
6:2	/	/	/
1	R/W	0x0	MODE SPI Function Mode Select

Offset: 0x0004			Register Name: SPI_GCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Slave Mode 1: Master Mode **NOTE** **Can not be written when XCH=1.**
0	R/W	0x0	EN SPI Module Enable Control 0: Disable 1: Enable

8.2.6.2. SPI Transfer Control Register(Default Value: 0x0000_0087)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Writing “1” to this bit will start the SPI burst, and will automatically clear after finishing the bursts transfer specified by **SPI_BC**. Writing “1” to **SRST** will also clear this bit. Writing ‘0’ to this bit has no effect.
30:15	/	/	/
14	R/W	0x0	SDDM Sending Data Delay Mode 0: Normal sending 1: Delay sending Set the bit to"1" to make the data that should be sent with a delay of half cycle of SPI_CLK in dual IO mode for SPI mode 0.
13	R/W	0x0	SDM Master Sample Data Mode 0: Delay Sample Mode 1: Normal Sample Mode In Normal Sample Mode, SPI master samples the data at the correct edge for each SPI mode; In Delay Sample Mode, SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	FBS First Transmit Bit Select 0: MSB first 1: LSB first
11	R/W	0x0	SDC Master Sample Data Control Set this bit to ‘1’ to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			between master and slave. 0: Normal operation, do not delay internal read sample point 1: Delay internal read sample point
10	R/W	0x0	RPSM Rapids mode select Select Rapids mode for high speed write. 0: Normal write mode 1: Rapids write mode
9	R/W	0x0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one
8	R/W	0x0	DHB Discard Hash Burst In master mode it controls whether discarding unused SPI bursts. 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC.
7	R/W	0x1	SS_LEVEL When control SS signal manually (**SS_OWNER** ==1), set this bit to '1' or '0' to control the level of SS signal. 0: Set SS to low 1: Set SS to high
6	R/W	0x0	SS_OWNER SS Output Owner Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write **SS_LEVEL** to 1 or 0 to control the level of SS signal. 0: SPI controller 1: Software
5:4	R/W	0x0	SS_SEL SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted
3	R/W	0x0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. Only valid when **SS_OWNER** = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle)

Offset: 0x0008			Register Name: SPI_TCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Active low polarity (1 = Idle)
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data)

NOTE

Do not write the bit[31] and bit[12:0] of the SPI_TCR when XCH = 1.

8.2.6.3. SPI Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SPI_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
12	R/W	0x0	TC_INT_EN Transfer Completed Interrupt Enable 0: Disable 1: Enable
11	R/W	0x0	TF_UDR_INT_EN TXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
10	R/W	0x0	TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
9	R/W	0x0	RF_UDR_INT_EN RXFIFO Underrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable

Offset: 0x0010			Register Name: SPI_ICR
Bit	**Read/Write**	**Default/Hex**	**Description**
7	/	/	/
6	R/W	0x0	TF_FUL_INT_EN TX FIFO Full Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TX_EMP_INT_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RF_FUL_INT_EN RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RX_EMP_INT_EN RX FIFO Empty Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable 0: Disable 1: Enable

8.2.6.4. SPI Interrupt Status Register(Default Value: 0x0000_0032)

Offset: 0x0014			Register Name: SPI_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W1C	0x0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
12	R/W1C	0x0	TC Transfer Completed In master mode, it indicates that all bursts specified by **SPI_BC** has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the shift register, and the shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed

Offset: 0x0014			Register Name: SPI_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
11	R/W1C	0x0	TF_UDF TXFIFO Underrun This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
10	R/W1C	0x0	TF_OVF TXFIFO Overflow This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it. 0: TXFIFO is not overflow 1: TXFIFO is overflowed
9	R/W1C	0x0	RX_UDF RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
8	R/W1C	0x0	RX_OVF RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
7	/	/	/
6	R/W1C	0x0	TX_FULL TXFIFO Full This bit is set when if the TXFIFO is full . Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
5	R/W1C	0x1	TX_EMP TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
4	R/W1C	0x1	TX_READY TXFIFO Ready 0: TX_WL > TX_TRIG_LEVEL 1: TX_WL <= TX_TRIG_LEVEL This bit is set any time if TX_WL <= TX_TRIG_LEVEL. Writing “1” to this bit clears it. Where TX_WL is the water level of RXFIFO.
3	/	/	Reserved
2	R/W1C	0x0	RX_FULL RXFIFO Full This bit is set when the RXFIFO is full . Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W1C	0x1	RX_EMP

Offset: 0x0014			Register Name: SPI_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
			RXFIFO Empty This bit is set when the RXFIFO is empty . Writing 1 to this bit clears it. 0: Not empty 1: empty
0	R/W1C	0x0	RX_RDY RXFIFO Ready 0: RX_WL < RX_TRIG_LEVEL 1: RX_WL >= RX_TRIG_LEVEL This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing “1” to this bit clears it. Where RX_WL is the water level of RXFIFO.

8.2.6.5. SPI FIFO Control Register(Default Value: 0x0040_0001)

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/WAC	0x0	TX_FIFO_RST TX FIFO Reset Writing ‘1’ to this bit will reset the control portion of the TX FIFO and automatically clear to ‘0’ when completing reset operation, writing to ‘0’ has no effect.
30	R/W	0x0	TF_TEST TX Test Mode Enable 0: Disable 1: Enable In normal mode, TX FIFO can only be read by SPI controller, writing ‘1’ to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO. **RF_TEST** and **TF_TEST** can not be set at the same time.
29:26	/	/	/
25	/	/	/
24	R/W	0x0	TF_ DRQ_EN TX FIFO DMA Request Enable 0: Disable 1: Enable
23:16	R/W	0x40	TX_TRIG_LEVEL TX FIFO Empty Request Trigger Level
15	R/WAC	0x0	RF_RST RXFIFO Reset Writing ‘1’ to this bit will reset the control portion of the receiver FIFO, and auto clear to ‘0’ when completing reset operation, writing ‘0’ to this bit has no effect.
14	R/W	0x0	RF_TEST RX Test Mode Enable 0: Disable 1: Enable In normal mode, RX FIFO can only be written by SPI controller, write

Offset: 0x0018			Register Name: SPI_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			'1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO. **RF_TEST** and **TF_TEST** can not be set at the same time.
13:9	/	/	/
8	R/W	0x0	RF_ DRQ_EN RX FIFO DMA Request Enable 0: Disable 1: Enable
7:0	R/W	0x1	RX_TRIG_LEVEL RX FIFO Ready Request Trigger Level

8.2.6.6. SPI FIFO Status Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SPI_FSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	/	/	/
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO. 00000000: 0 byte in TX FIFO 00000001: 1 byte in TX FIFO … 01000000: 64 bytes in TX FIFO Others:Reserved
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	/	/	/
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 00000000: 0 byte in RX FIFO 00000001: 1 byte in RX FIFO … 01000000:64 bytes in RX FIFO Others:Reserved

8.2.6.7. SPI Wait Clock Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SPI_WAIT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19:16	R/W	0x0	SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted N: N SPI_SCLK wait states inserted These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by **SWC** for delaying next word data transfer. **NOTE** **Can not be written when XCH=1.**
15:0	R/W	0x0	WCC Wait Clock Counter (In Master mode) 0: No wait states inserted N: N SPI_SCLK wait states inserted These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by **WCC** for delaying next word data transfer.

8.2.6.8. SPI Clock Control Register(Default Value: 0x0000_0002)

Offset: 0x0024			Register Name: SPI_CCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12	R/W	0x0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0x0	CDR1 Clock Divide Rate 1 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / 2^n.
7:0	R/W	0x2	CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = Source_CLK / (2*(n + 1)).

8.2.6.9. SPI Master Burst Counter Register (Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SPI_BC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	MBC Master Burst Counter

Offset: 0x0030			Register Name: SPI_BC
Bit	Read/Write	Default/Hex	Description
			In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts

8.2.6.10. SPI Master Transmit Counter Register (Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: SPI_TC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0x0	MWTC Master Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

8.2.6.11. SPI Master Burst Control Counter Register (Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	DRM Master Dual Mode RX Enable 0: RX use single-bit mode 1: RX use dual mode
27:24	R/W	0x0	DBC Master Dummy Burst Counter In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The device does not care the data. 0: 0 burst 1: 1 burst … N: N bursts
23:0	R/W	0x0	STC Master Single Mode Transmit Counter In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts.

Offset: 0x0038			Register Name: SPI_BCC
Bit	Read/Write	Default/Hex	Description
			0: 0 burst 1: 1 burst … N: N bursts

NOTE

Do not write SPI_BCC when XCH = 1.

8.2.6.12. SPI Normal DMA Mode Control Register(Default Value: 0x0000_00A5)

Offset: 0x0088			Register Name: SPI_NDMA_MODE_CTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0xA5	NDMA_MODE_CTL 0xEA:NDMA handshake mode **NOTE** **NDMA wait mode don't care this value.0xA5 can be used in handshake mode, but 0xEA is better.**

8.2.6.13. SPI TX Data Register(Default Value: 0x0000_0000)

Offset: 0x0200			Register Name: SPI_TXD
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TDATA Transmit Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in RXFIFO, one burst data is written to RXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4. **NOTE** **This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.**

8.2.6.14. SPI RX Data Register(Default Value: 0x0000_0000)

Offset: 0x0300			Register Name: SPI_RXD
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RDATA Receive Data This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is

Offset: 0x0300			Register Name: SPI_RXD
Bit	**Read/Write**	**Default/Hex**	**Description**
			returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4. **NOTE** **This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.**

8.3. UART

8.3.1. Overview

The Universal Asynchronous Receiver and Transmitter(UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

A40i has eight UARTs named UART0,UART1,UART2,UART3,UART4,UART5,UART6 and UART7. Each UART performs serial-to-parallel conversion on data characters received from a peripheral device or a modem and parallel-to-serial conversion on data characters received from the master(CPU).

The interface is fully programmable through 8-bit CPU interface.The registers are 32-bit word aligned. The UARTs can control the character length, baud rate, parity generation/checking, and interrupt generation. It supports word lengths from 5 to 8bits,an optional parity bit,and 1,1.5 or 2 stop bits.If enabled, parity can be odd,even,or no parity. Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

The UARTs support both 16450 and 16550 compatible modes. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled. It also includes a 16-bit programmable baud rate generator and an 8-bit scratch register, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Features:

- 8 UART controllers
- Compatible with industry-standard 16550 UARTs
- Supports for word length from 5 to 8 bits,an optional parity bit,and 1,1.5 or 2 stop bits
- Programmable parity(even,odd and no parity)
- 64 bytes transmit and receive data FIFOs
- DMA controller interface
- Software/ hardware flow control
- Programmable transmit holding register empty interrupt
- Interrupt support for FIFOs, Status Change

8.3.2. Block Diagram

Figure 8-8 shows a block diagram of the UART.

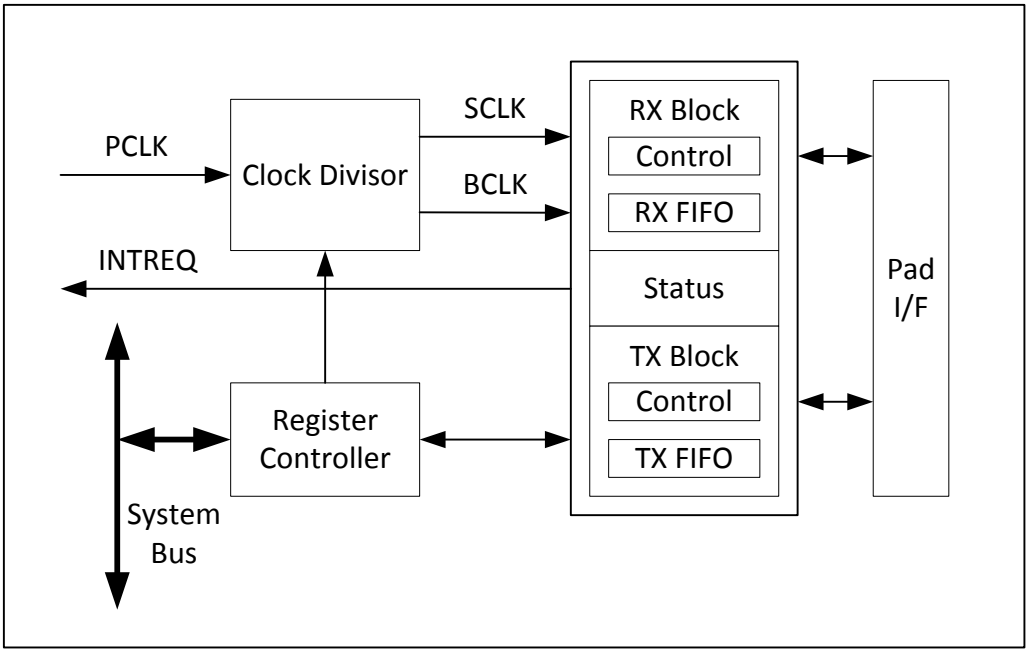


Figure 8-8. UART Block Diagram

8.3.3. Operations and Functional Descriptions

8.3.3.1. External Signals

Table 8-6 describes the external signals of UART.

Table 8-6. UART External Signals

Signal	Description	Type
UART0_TX	UART Serial Bit Output	O
UART0_RX	UART Serial Bit Input	I
UART1_TX	UART Serial Bit Output	O
UART1_RX	UART Serial Bit Input	I
UART1_CTS	UART Clear To End This active low signal is an input signal when modem is ready to accept data	I
UART1_RTS	UART Request To Send This active low output signal informs modem that the UART is ready to send data	O
UART1_DTR	UART Data Terminal Ready	O
UART1_DSR	UART Data Set Ready	I
UART1_DCD	UART Data Carrier Detect	I
UART1_RING	UART Data Ring Indicator	I
UART2_TX	UART Serial Bit Output	O
UART2_RX	UART Serial Bit Input	I
UART2_CTS	UART Clear To End This active low signal is an input signal when modem is ready to accept data	I
UART2_RTS	UART Request To Send This active low output signal informs modem that the UART is ready to send data	O
UART3_TX	UART Serial Bit Output	O

UART3_RX	UART Serial Bit Input	I
UART3_CTS	UART Clear To End This active low signal is an input signal when modem is ready to accept data	I
UART3_RTS	UART Request To Send This active low output signal informs modem that the UART is ready to send data	O
UART4_TX	UART Serial Bit Output	O
UART4_RX	UART Serial Bit Input	I
UART5_TX	UART Serial Bit Output	O
UART5_RX	UART Serial Bit Input	I
UART6_TX	UART Serial Bit Output	O
UART6_RX	UART Serial Bit Input	I
UART7_TX	UART Serial Bit Output	O
UART7_RX	UART Serial Bit Input	I

8.3.3.2. Clock Sources

Table 8-7 describes the clock sources of UART. UART is on APB2 Bus.The clock of APB2 Bus has three sources: LOSC,OSC24M,PLL_PERIPH0(2X).

Table 8-7. UART Clock Sources

Clock Sources		Description
APB2	LOSC	32KHz Crystal
	OSC24M	24MHz Crystal
	PLL_PERIPH0(2X)	Peripheral Clock,default value of 2X is 1.2GHz

8.3.3.3. Typical Application

Figure 8-9 shows the application block diagram of UART.

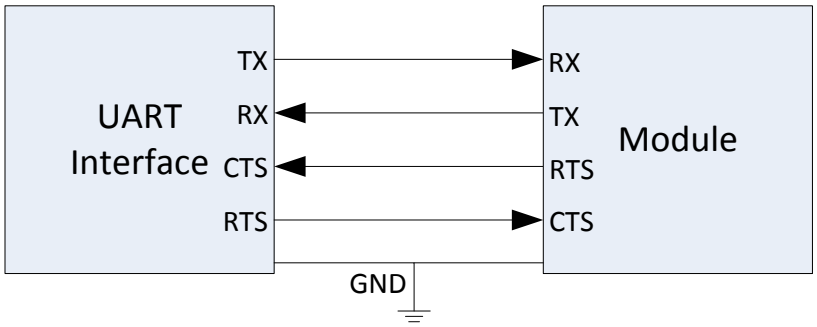


Figure 8-9. UART Application Diagram

8.3.3.4. UART Timing Diagram

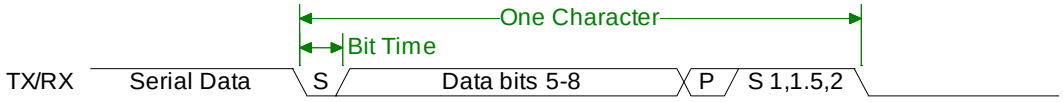


Figure 8-10. UART Serial Data Format

8.3.4. Programming Guidelines

(1) DMA Mode

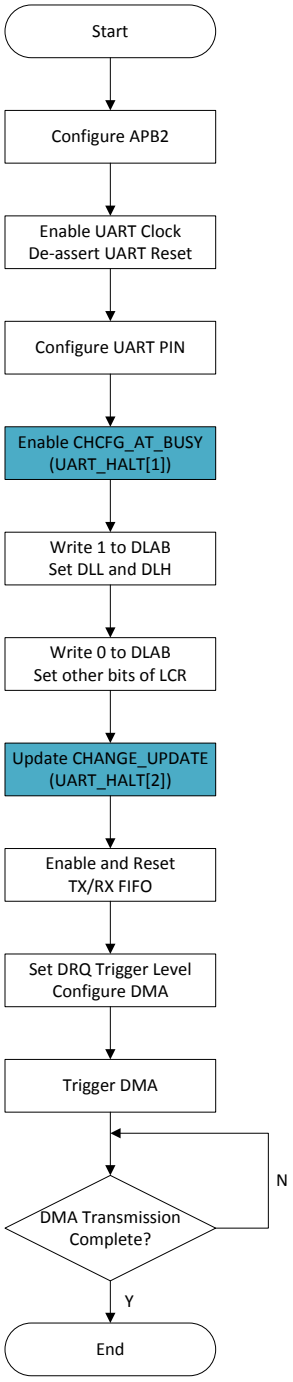


Figure 8-11. UART DRQ Flow Chart

(2) CPU Mode

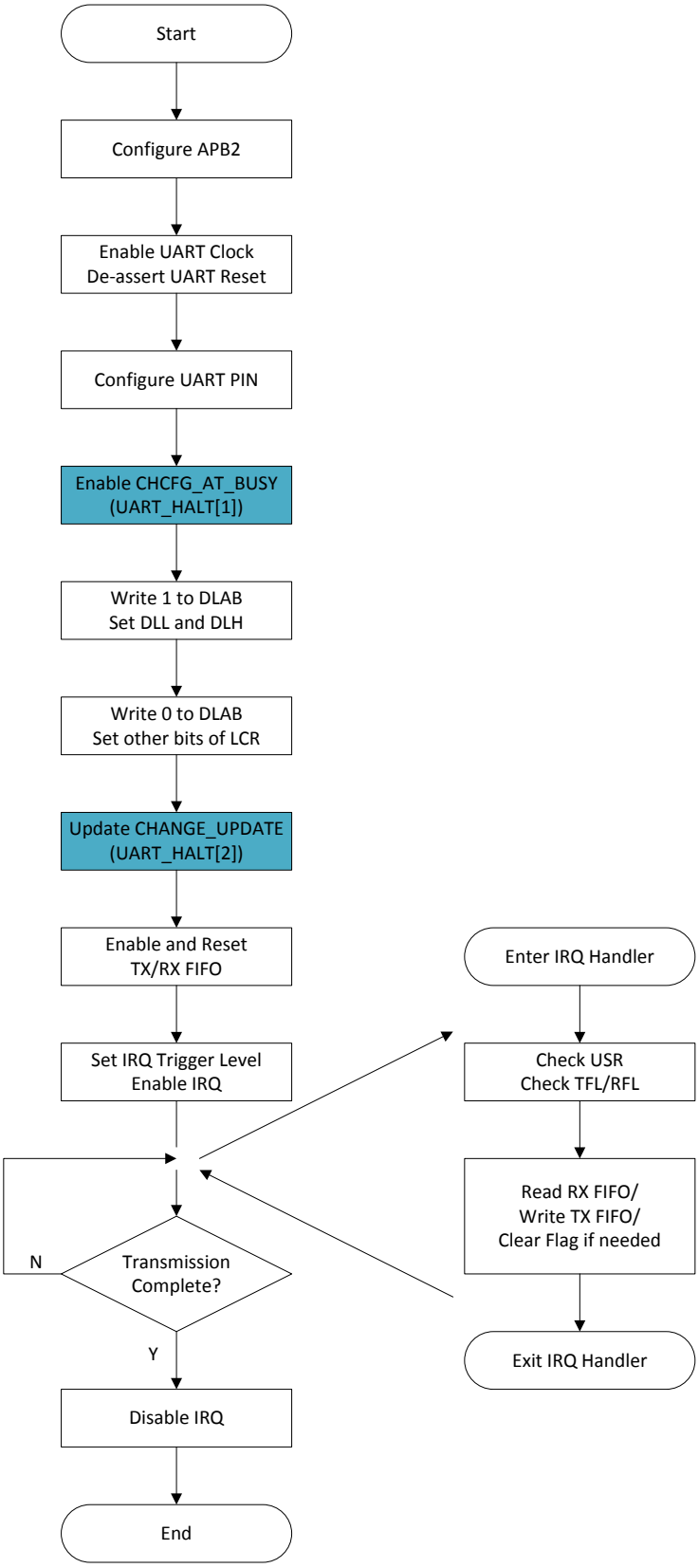


Figure 8-12. UART IRQ Flow Chart

8.3.5. Register List

There are 8 UART controllers. UART1 has full modem control signals, including RTS, CTS, DTR, DSR, DCD and RING signal. UART2/3 has two data flow control singals, including RTS and CTS. Other UART controller has only two data signals, including DIN and DOUT.

Module Name	Base Address
UART0	0x01C28000
UART1	0x01C28400
UART2	0x01C28800
UART3	0x01C28C00
UART4	0x01C29000
UART5	0x01C29400
UART6	0x01C29800
UART7	0x01C29C00

Register Name	Offset	Description
UART_RBR	0x0000	UART Receive Buffer Register
UART_THR	0x0000	UART Transmit Holding Register
UART_DLL	0x0000	UART Divisor Latch Low Register
UART_DLH	0x0004	UART Divisor Latch High Register
UART_IER	0x0004	UART Interrupt Enable Register
UART_IIR	0x0008	UART Interrupt Identity Register
UART_FCR	0x0008	UART FIFO Control Register
UART_LCR	0x000C	UART Line Control Register
UART_MCR	0x0010	UART Modem Control Register
UART_LSR	0x0014	UART Line Status Register
UART_MSR	0x0018	UART Modem Status Register
UART_SCH	0x001C	UART Scratch Register
UART_USR	0x007C	UART Status Register
UART_TFL	0x0080	UART Transmit FIFO Level
UART_RFL	0x0084	UART Receive FIFO Level
UART_HALT	0x00A4	UART Halt TX Register

8.3.6. Register Description

8.3.6.1. UART Receiver Buffer Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0x0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is

Offset: 0x0000			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
			valid only if the **Data Ready** bit in the **UART_LSR** register is set. If in FIFO mode and FIFOs are enabled (**FIFOE** = 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.

8.3.6.2. UART Transmit Holding Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_THR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0x0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to **THR** when the **THRE** bit is set. If in FIFO mode and FIFOs are enabled (**FIFOE** = 1) and **THRE** is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

8.3.6.3. UART Divisor Latch Low Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0x0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the **DLAB** bit is set and the UART is not busy (**UART Busy** = 0). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (**DLL** and **DLH**) set to zero, the baud clock is disabled and no serial communications occur. Also, once the **DLL** is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.3.6.4. UART Divisor Latch High Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_DLH
Bit	Read/Write	Default/Hex	Description

Offset: 0x0004			Register Name: UART_DLH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the **DLAB** bit is set and the UART is not busy (**UART Busy** = 0). The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (**DLL** and **DLH**) set to zero, the baud clock is disabled and no serial communications occur. Also, once the **DLH** is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

8.3.6.5. UART Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: UART_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:4	/	/	/
3	R/W	0x0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0x0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0x0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0x0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available

Offset: 0x0004			Register Name: UART_IER
Bit	**Read/Write**	**Default/Hex**	**Description**
			Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

8.3.6.6. UART Interrupt Identity Register(Default Value: 0x0000_0001)

Offset: 0x0008			Register Name: UART_IIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	R	0x0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received data available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Second	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0010	Third	Transmit holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Fifth	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

8.3.6.7. UART FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:6	W	0x0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0x0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER is disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0x0	DMAM DMA Mode 0: Mode 0 1: Mode 1
2	W	0x0	XFIFOR

Offset: 0x0008			Register Name: UART_FCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0x0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0x0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

8.3.6.8. UART Line Control Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (**UART Busy** = 0) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (**DLL** and **DLH**) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (**UART_RBR**)/TX Holding Register (**UART_THR**) and Interrupt Enable Register(**UART_IER**) 1: Select Divisor Latch Low Register(**UART_DLL**) and Divisor Latch High Register(**UART_DLH**)
6	R/W	0x0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in **Loop Back Mode**, as determined by **UART_MCR[4]**, the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (**UART_MCR[6]** is set to 1) the sir_out_n line is continuously pulsed. When in **Loop Back Mode**, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	/	/	/
4	R/W	0x0	EPS Even Parity Select It is writeable only when UART is not busy (**UART Busy** = 0) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). 0: Odd Parity 1: Even Parity

Offset: 0x000C			Register Name: UART_LCR
Bit	**Read/Write**	**Default/Hex**	**Description**
3	R/W	0x0	PEN Parity Enable It is writeable only when UART is not busy (**UART Busy** = 0) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0x0	STOP Number of stop bits It is writeable only when UART is not busy (**UART Busy** = 0) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If the bit is set to '1' and the **DLS** bit is set to 5, one and a half stop bit is transmitted. Otherwise, two stop bit is transmitted. Note that regardless of the number of stop bit selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bit when **DLS** is zero, else 2 stop bit
1:0	R/W	0x0	DLS Data Length Select It is writeable only when UART is not busy (**UART Busy** = 0) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bit 01: 6 bit 10: 7 bit 11: 8 bit

8.3.6.9. UART Modem Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W	0x0	SIRE SIR Mode Enable 0: IrDA SIR Mode disable 1: IrDA SIR Mode enable
5	R/W	0x0	AFCE Auto Flow Control Enable When FIFOs are enabled and the **AFCE** bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disable 1: Auto Flow Control Mode enable
4	R/W	0x0	LOOP Loop Back Mode

Offset: 0x0010			Register Name: UART_MCR
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (**SIR Mode** is disabled), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in **Loop Back Mode**, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (**SIR Mode** is enabled), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3:2	/	/	/
1	R/W	0x0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (**AFCE** = 0), the rts_n signal is set low by programming **RTS** to high.In Auto Flow Control, AFCE_MODE is enabled and active (**AFCE** = 1) and FIFOs enable (**FIFOE** = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when **RTS** is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (**LOOP** = 1), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0x0	DTR Data Terminal Ready This is used to directly control the **DTR**(dtr_n) output. The value written to this location is inverted and driven out on dtr_n. 0:dtr_n de-asserted (logic 1) 1:dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (**LOOP** = 1), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

8.3.6.10. UART Line Status Register(Default Value: 0x0000_0060)

Offset: 0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO.

Offset: 0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
			It is cleared by a read from the **UART_LSR** register provided there are no subsequent errors in the FIFO.
6	R	0x1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	0x1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to “1” whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to “1” whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0x0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (**SIR Mode** is disabled), it is set whenever the serial input, sin, is held in a logic ‘0’ state for longer than the sum of ***start time + data bits + parity + stop*** *bits*. If in infrared mode (**SIR Mode** is enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic ‘0’ for longer than the sum of ***start time + data bits + parity + stop*** *bits*. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the **BI** bit. In the non-FIFO mode, the **BI** indication occurs immediately and persists until the LSR is read.
3	R	0x0	FE Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the **FE** bit is set if a break interrupt has occurred, as indicated by the **BI** bit. 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	R	0x0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the **Parity Enable** bit is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted

Offset: 0x0014			Register Name: UART_LSR
Bit	**Read/Write**	**Default/Hex**	**Description**
			that the **Parity Error** bit is set if a break interrupt has occurred, as indicated by the **Break Interrupt** bit. 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	R	0x0	OE Overrun Error This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the **OE** bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0x0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

8.3.6.11. UART Modem Status Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R	0x0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the **DCD**(dcd_n) is asserted, it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0x0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the **RI**(ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
5	R	0x0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the **DSR**(dsr_n) bit is asserted, it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In **Loop Back Mode**(UART_MCR[4] is set to 1), **DSR** is the same as **DTR**.
4	R	0x0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In **Loop Back Mode**(UART_MCR[4] is set to 1), **CTS** is the same as **RTS**.
3	R	0x0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. **NOTE** **If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.**
2	R	0x0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0x0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In **Loop Back Mode**(UART_MCR[4] = 1), DDSR reflects changes on **DTR**. **NOTE** **If the DDSR bit is not set and the dsr_n signal is asserted (low) and a**

Offset: 0x0018			Register Name: UART_MSR
Bit	**Read/Write**	**Default/Hex**	**Description**
			reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0x0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In **Loop Back Mode**(UART_MCR[4] = 1), **DCTS** reflects changes on **RTS**. **NOTE** **If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.**

8.3.6.12. UART Scratch Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: UART_SCH
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	SCRATCH_REG Scratch Register This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

8.3.6.13. UART Status Register(Default Value: 0x0000_0006)

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO full This bit is cleared when the RX FIFO is no longer full.
3	R	0x0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	0x1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty.

Offset: 0x007C			Register Name: UART_USR
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	0x1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO is not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0x0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

8.3.6.14. UART Transmit FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: UART_TFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.

8.3.6.15. UART Receive FIFO Level Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: UART_RFL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R	0x0	RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.

8.3.6.16. UART Halt TX Register(Default Value: 0x0000_0000)

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	PTE TX_REQ Transmit In DMA1 mode (**DMA Mode** is 1,FIFO is open),if PTE signal is high, DMA request is sent when TFL is not larger than TRIG. If PTE signal is low, DMA request is sent when FIFO is empty. DMA request could fall when FIFO is full. In DMA0 mode(**DMA Mode** is 0,FIFO is closed),if PTE signal is high and FIFO is open, DMA request is sent when TFL is not larger than TRIG. If

Offset: 0x00A4			Register Name: UART_HALT
Bit	**Read/Write**	**Default/Hex**	**Description**
			these conditions are not satisfied, then DRQ will fall. If PTE signal is high and FIFO is closed, DMA request is sent when THRE is empty. If these conditions are not satisfied, then DRQ will fall. If PTE signal is low, DMA request is sent when FIFO is empty.
6	R/W	0x0	DMA_PTE_RX RX_DRQ Receive In DMA1 mode, when RFL is not less than TRIG or the receiver timeout is happened, DRQ is sent , or else DRQ is low. In DMA0 mode, if DMA_PTE_RX is 1 and FIFO is open, REQ is sent when RFL is not less than TRIG, or else not sent.
5	R/W	0x0	SIR_RX_INVERT SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0x0	SIR_TX_INVERT SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3	/	/	/
2	R/WAC	0x0	CHANGE_UPDATE After the user using **CHCFG_AT_BUSY** to change the baud rate or **UART_LCR** register configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect. 1: Update trigger, Self clear to 0 when finish update.
1	R/W	0x0	CHCFG_AT_BUSY This is an enable bit for the user to change **UART_LCR** register configuration (except for the **DLAB** bit) and baudrate register (**UART_DLH** and **UART_DLL**) when the UART is busy (**UART Busy** is 1). 1: Enable change when busy
0	R/W	0x0	HALT_TX Halt TX This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0: Halt TX disabled 1: Halt TX enabled **NOTE** **If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.**

8.4. PS2

8.4.1. Overview

The PS2 is a dual-role controller that supports both device and host functions. It is fully compliant with IBM PS2 in Personal Computer. It can be configured as a Host to connect PS2 Keyboard or PS2 Mouse, or as a Device to connect computers. The PS2 module can be integrated with industry-standard AMBA Peripheral Bus (APB) for communication with other system modules, such as ARM CPU, and System Memory.

Features:

- 2 PS2 controllers
- Compliant with the AMBA Specification (Rev 2.0) for easy integration into SOC implementation
- Compliant with IBM PS2 and AT-Compatible Keyboard and Mouse Interface
- Dual Role controller, either a PS2 Host or a PS2 Device
- 4-byte TXFIFO and 4-byte RXFIFO for data buffering
- Odd parity generation and checking
- Register bits for override of keyboard clock and data lines
- Internal clock divider for simple clock interface

8.4.2. Block Diagram

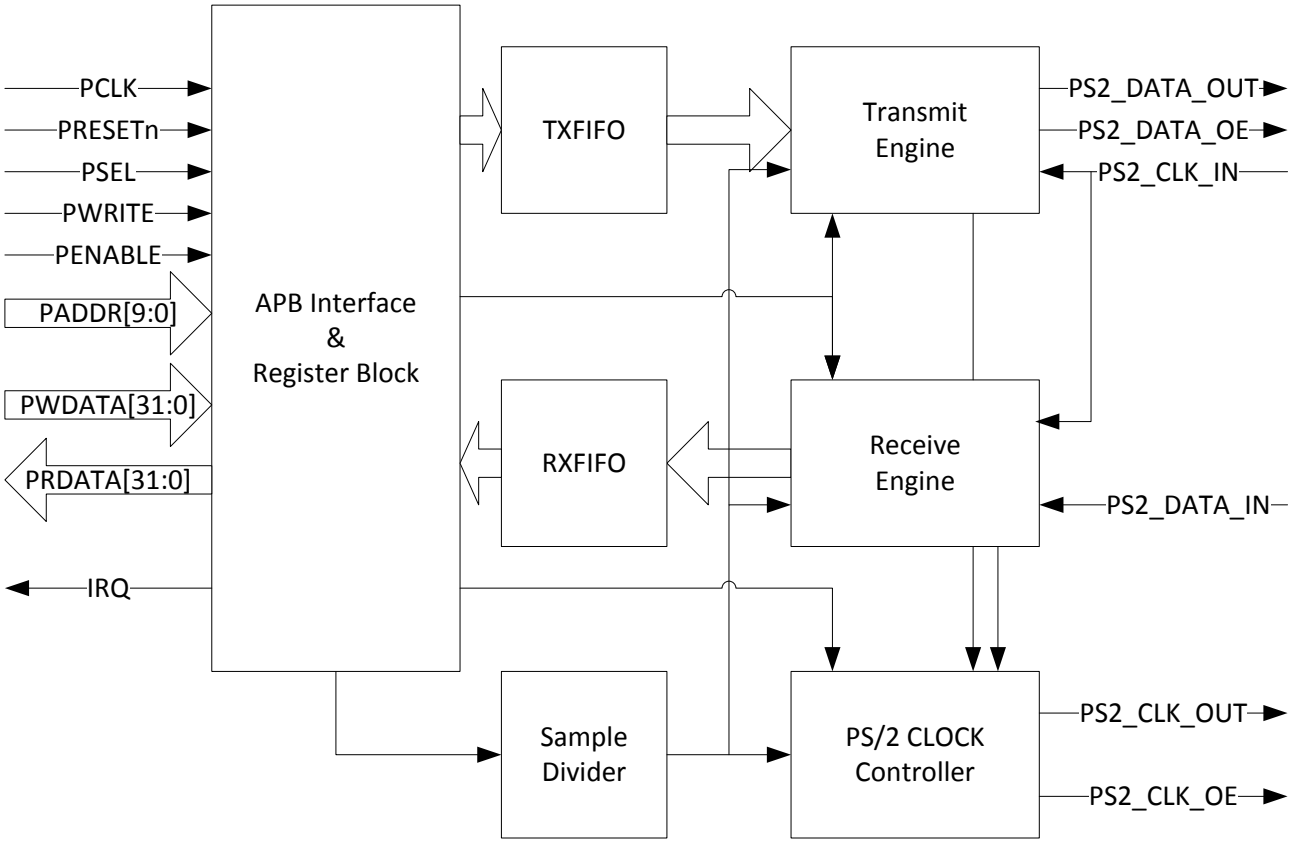


Figure 8-13. PS2 Block Diagram

8.4.3. Operations and Functional Descriptions

8.4.3.1. External Signals

Table 8-8 describes the external signals of PS2.

Table 8-8. PS2 External Signals

Port Name	Width	Type	Description
PS2_SCK0	1	I/O	PS2 clock signal
PS2_SDA0	1	I/O	PS2 data signal
PS2_SCK1	1	I/O	PS2 clock signal
PS2_SDA1	1	I/O	PS2 data signal

8.4.3.2. Clock Requirement

Table 8-9 describes the clock sources of PS2. PS2 is on APB2 Bus.The clock of APB2 Bus has three sources: LOSC,OSC24M,PLL_PERIPH0(2X).

Table 8-9. PS2 Clock Requirement

Clock Name	Description	Requirement
APB2_CLK	APB bus clock	>=1MHz

8.4.3.3. Timing Diagram

The Data and Clock lines of PS2 Bus are both open-collector with pull-up resistors to power, and so, Data and Clock signals on PS2 Bus are both wire-and by corresponding signal of Host and Device. Data is transferred after start bit, starting with the least significant bit(LSB). These are followed by the parity bit, followed by one stop bit. If data is transferred from master to device, there is an additional acknowledge bit(ACK) sent by device, following the stop bit.

Timing for Device Transmit Data and Master Receive Data:

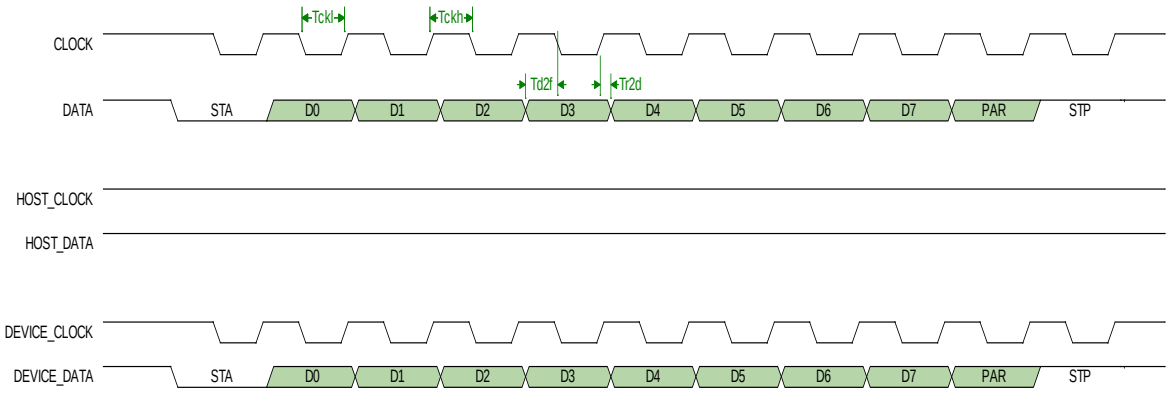


Figure 8-14. Device Transmit and Master Receive Data Timing

Timing for Master Transmit Data and Device Receive Data:

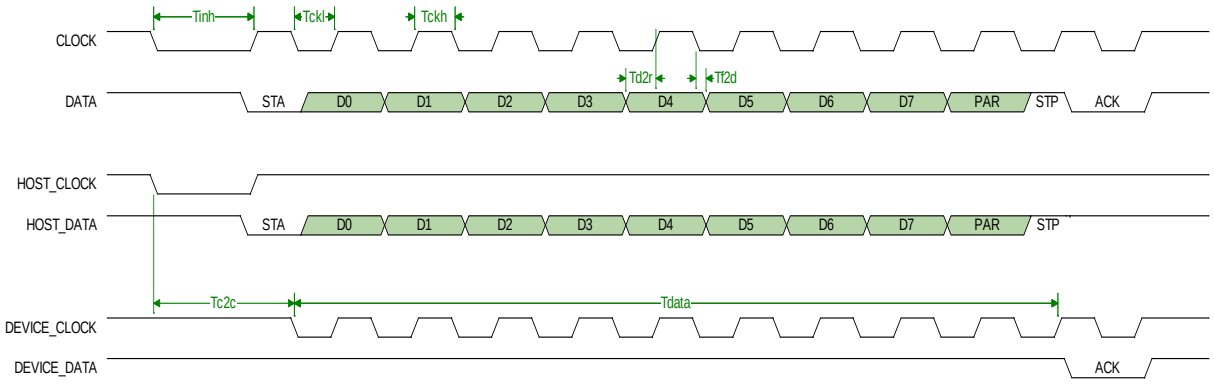


Figure 8-15. Master Transmit and Device Receive Data Timing

Timing for Master sending command then Device sending response

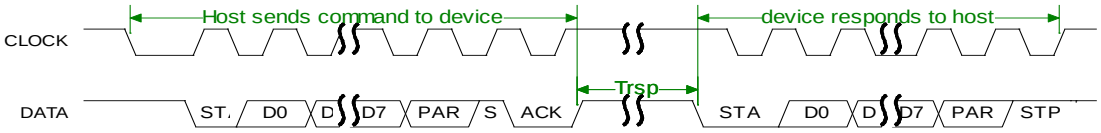


Figure 8-16. Master Send Command Then Device Send Response Timing

Device drive and sample data at rising edge of CLOCK. Master drive and sample data at falling edge of CLOCK.

Name	Comment	Min.	Typical	Max.
Tckl	Clock LOW time	30us	40us	50us
Tckh	Clock HIGH time	30us	40us	50us
Tinh	Time for Host inhibit clock for send data request	100us	-	-
Td2f	Data change to clock falling edge time during device to host transfer	5us	-	Tckh-5us
Tr2d	Clock rising edge to data change time during device to host transfer	5us	-	Tckh-5us
Td2r	Data change to clock rising edge time during host to device transfer	5us	-	Tckl-5us
Tf2d	Clock falling edge to data change time during host to device transfer	5us	-	Tckl-5us
Tc2c	Host pull low Clock to Device drive Clock	-	-	15ms
Tdata	Time for packet to send	-	-	2ms
Trsp	Time for device responding to the host command	-	-	20ms

8.4.4. Register List

Module Name	Base Address
PS2-0	0x01C2A000
PS2-1	0x01C2A400

Register Name	Offset	Description
PS2_GCTL	0x0000	PS2 Module Global Control Register
PS2_DATA	0x0004	PS2 Module Data Register
PS2_LCTL	0x0008	PS2 Module Line Control Register
PS2_LSTS	0x000C	PS2 Module Line Status Register
PS2_FCTL	0x0010	PS2 Module FIFO Control Register

PS2_FSTS	0x0014	PS2 Module FIFO Status Register
PS2_CKDR	0x0018	PS2 Module Clock Divider Register

8.4.5. Register Description

8.4.5.1. PS2 Global Control Register(Default Value: 0x0000_0002)

Offset: 0x0000			Register Name: PS2_GCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	INT_FLAG Interrupt Flag The interrupt flag is set when any bit in FIFO Status and the corresponding enable bit in FIFO Control are set at the same time. This interrupt flag is also set when error flag bit in line status register (**PS2_LSTS**) is set at the same time. **NOTE** **This bit is just a status flag, it can not be cleared directly, it can be cleared by clearing the status bits in FIFO Status Register.**
3	R/W	0x0	INT_EN Interrupt Enable 0: The interrupt signal is always low 1: The interrupt signal will be high when **INT_FLAG** is set
2	R/W	0x0	SOFT_RST Soft Reset Setting this bit will reset transmitter and receiver of PS2 Module, and the status of transmitter and receiver will revert to the default state, but not affect any control bits in register, and data in TXFIFO/RXFIFO. This bit will be cleared by hardware after reset is completed.
1	R/W	0x1	FUNC_SEL Master/Device Function Select 0: Device Function, connect to Computer 1: Master Function, connect to PS2 Keyboard or Mouse
0	R/W	0x0	BUS_EN PS2 Bus Enable 0: Ignore PS2 Bus Input 1: Response to PS2 Bus Input

8.4.5.2. PS2 Data Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: PS2_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	PS2_DATA When write, data will be written into TXFIFO, and will be transmited on to the PS2 Bus. When read, data is read out from RXFIFO, and it is received from PS2 Bus.

Offset: 0x0004			Register Name: PS2_DATA
Bit	Read/Write	Default/Hex	Description
			NOTE After TXFIFO is full, writing does not affect anything except the overflow flag of TXFIFO in FIFO Status Register. After RXFIFO is empty, reading has no effect on anything except the underflow flag of RXFIFO in FIFO Status Register.

8.4.5.3. PS2 Line Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: PS2_LCTL
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	NO_ACK ACK Control 0: In Host function mode, must check ACK after transmitted data; in Device function mode, must send ACK after received data from Host. 1: In Host function mode, don't check ACK after transmitted data; in Device function mode, don't send ACK after received data from Host.
17	R/W	0x0	FORCE_DATA Force Data to Low 0: Data Line works in Normal Mode 1: Data Line is forced to Low
16	R/W	0x0	FORCE_CLK Force Clock to Low 0: Clock Line works in Normal Mode 1: Clock Line is forced to Low
15:9	/	/	/
8	R/W	0x0	TXDTO_IEN TX Data Timeout Interrupt Enable
7:4	/	/	/
3	R/W	0x0	STOP_IEN Stop Error Interrupt Enable
2	R/W	0x0	ACKERR_IEN Acknowledge Error Interrupt Enable
1	R/W	0x0	PARERR_IEN Parity Error Interrupt Enable
0	R/W	0x0	RXDTO_IEN RX Data Timeout Interrupt Enable

8.4.5.4. PS2 Line Status Register(Default Value: 0x0003_0000)

Offset: 0x000C			Register Name: PS2_LSTS
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W1C	0x0	TX_BUSY Transmit Busy

Offset: 0x000C			Register Name: PS2_LSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: PS2 Module Transmit Engine is Idle. 1: PS2 Module is currently sending data. **This bit can be cleared by writing '1'. Writing '0' has no effect.**
18	R/W1C	0x0	RX_BUSY Receive Busy 0: PS2 Module Receive Engine is Idle. 1: PS2 Module is currently receiving data. **This bit can be cleared by writing '1'. Writing '0' has no effect.**
17	R	0x1	LS_DATA Line State of DATA. Invalid before BUS_EN set.
16	R	0x1	LS_CLK Line State of CLOCK. Invalid before BUS_EN set.
15:9	/	/	/
8	R/W1C	0x0	TX_DTO Transmit Data Timeout Timers include: Tc2c<15ms (Host pull low Clock to Device drive Clock) Tdata<2ms (Time for packet to send) Tckl+Tckh<100us(one cycle time, as host) **This bit can be cleared by writing '1'.Writing '0' has no effect.**
7:4	/	/	/
3	R/W1C	0x0	STOP_ERR Stop Bit Error 0: No Error 1: Stop Error This bit can be cleared by writing '1'.Writing '0' has no effect.
2	R/W1C	0x0	ACK_ERR Acknowledge Error 0: ACK is received after data transmitted. 1: ACK is not received after data transmitted. **NOTE** **Only for Master Function; This bit can be cleared by writing '1'. Writing '0' has no effect.**
1	R/W1C	0x0	PAR_ERR Parity Error 0: No Error 1: Parity Error **This bit can be cleared by writing '1'. Writing '0' has no effect.**
0	R/W	0x0	RX_DTO Receive Data Timeout Timers include: Trsp<20ms(time from the host releases the Clock line to device sends corresponding response) Tckl+Tckh<100us(one cycle time, as host) **This bit can be cleared by writing '1'.Writing '0' has no effect.**

8.4.5.5. PS2 FIFO Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: PS2_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
17	R/WAC	0x0	TXFIFO_RST TXFIFO Reset After this bit is set, data in TXFIFO is flushed, and the pointer of TXFIFO is reset. **This bit is cleared automatically after TXFIFO is reset, and writing '0' has no effect.**
16	R/WAC	0x0	RXFIFO_RST RXFIFO Reset After this bit is set, data in RXFIFO is flushed, and the pointer of RXFIFO is reset. **This bit is cleared automatically after RXFIFO is reset, and writing '0' has no effect.**
15:11	/	/	/
10	R/W	0x0	TXUF_IEN TXFIFO Underflow Interrupt Enable
9	R/W	0x0	TXOF_IEN TXFIFO Overflow Interrupt Enable
8	R/W	0x0	TXRDY_IEN TXFIFO Ready Interrupt Enable
7:3	/	/	/
2	R/W	0x0	RXUF_IEN RXFIFO Underflow Interrupt Enable
1	R/W	0x0	RXOF_IEN RXFIFO Overflow Interrupt Enable
0	R/W	0x0	RXRDY_IEN RXFIFO Ready Interrupt Enable

8.4.5.6. PS2 FIFO Status Register(Default Value: 0x0000_0100)

Offset: 0x0014			Register Name: PS2_FSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R	0x0	TX_LEVEL TXFIFO Level The number of 8bit data, which is transmitted to PS2 Bus, in the TXFIFO. The value must be in the range of 0 to 4.
19	/	/	/
18:16	R	0x0	RX_LEVEL RXFIFO Level The number of 8bit data, which is received from PS2 bus, in the RXFIFO. The value must be in the range of 0 to 4.
15:11	/	/	/
10	R/W1C	0x0	TX_UF TXFIFO Underflow When this bit is set, TXFIFO is underflow, and it means that the TXFIFO is read by transmit engine after empty. This bit is just a flag of illegal operation, which should not affect any state of TXFIFO.

Offset: 0x0014			Register Name: PS2_FSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
			This bit can be cleared by writing '1'. Writing '0' has no effect.
9	R/W1C	0x0	TX_OF TXFIFO Overflow When this bit is set, TXFIFO is overflow, and it means that the TXFIFO is written by CPU after TXFIFO is full. This bit is just a flag of illegal operation, which should not affect any state of TXFIFO. **This bit can be cleared by writing '1'.Writing '0' has no effect.**
8	R/W1C	0x1	TX_RDY Transmit Ready 0: TXFIFO is full 1: TXFIFO is not full. **This bit can be cleared by writing '1', writing '0' has no effect.**
7:3	/	/	/
2	R/W1C	0x0	RX_UF RXFIFO Underflow When this bit is set, RXFIFO is underflow, and it means that the RXFIFO is read by CPU after empty. This bit is just a flag of illegal operation, which should not affect any state of RXFIFO. **This bit can be cleared by writing '1'. Writing '0' has no effect.**
1	R/W1C	0x0	RX_OF RXFIFO Overflow When this bit is set, RXFIFO is overflow, and it means that the RXFIFO is written by received engine after RXFIFO is full. This bit is just a flag of illegal operation, which should not affect any state of RXFIFO. **This bit can be cleared by writing '1'. Writing '0' has no effect.**
0	R/W1C	0x0	RX_RDY Receive Ready 0: RXFIFO is empty 1:RXFIFO is not empty, there are at least one byte data, which is received from PS2 bus, in the RXFIFO. **This bit can be cleared by writing '1'.Writing '0' has no effect.**

8.4.5.7. PS2 Clock Divider Register(Default Value: 0x0000_2F4F)

Offset: 0x0018			Register Name: PS2_CKDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R/W	0x2F	SCLK_DIV Sample Clock Divider Factor (SCDF) Sample Clock is a 1MHz clock for internal timing control. SCDF = APB_CLK/SAMPLE_CLK – 1 Frequency of sample clock is constant, and so, frequency of APB_CLK must be in the range of 1MHz to 256MHz.
7	/	/	/
6:0	R/W	0x4F	CLK_DIV PS2 Clock Divider Factor (PCDF) PCDF = SAMPLE_CLK /PS2_CLK – 1 = 1MHz/PS2_CLK – 1 The frequency of PS2_CLK must be in the range of 10kHz to 16.7kHz.

Offset: 0x0018			Register Name: PS2_CKDR
Bit	Read/Write	Default/Hex	Description
			NOTE This factor is used in device mode only.

8.5. CIR

8.5.1. Overview

The CIR (Consumer IR) interface is used for remote control through infra-red light.

The CIR receiver samples the input signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width. The encoded data is buffered in a 64 levels and 8-bit width RX FIFO; the MSB bit is used to record the polarity of the receiving CIR signal. The high level is represented as '1' while the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, another byte is used.

Since there is always some noise in the air, a threshold can be set to filter the noise to reduce system loading and improve system stability.

Features:

- 2 CIR controllers
- Full physical layer implementation
- Supports CIR for remote control
- 64 x 8bit FIFO for data buffer
- Programmable FIFO thresholds

8.5.2. Register List

Module Name	Base Address
CIR0	0x01C21800
CIR1	0x01C21C00

Register Name	Offset	Description
CIR_CTL	0x0000	CIR Control Register
CIR_RXCFG	0x0010	CIR Receiver Configure Register
CIR_RXFIFO	0x0020	CIR Receiver FIFO Register
CIR_RXINT	0x002C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x0030	CIR Receiver Status Register
CIR_CFR	0x0034	CIR Configure Register

8.5.3. Register Description

8.5.3.1. CIR Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	CGPO General Program Output (GPO) Control in CIR mode for TX Pin

Offset: 0x0000			Register Name: CIR_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Low level 1: High level
7:6	R/W	0x0	Active Pulse Accept Mode 00: Start to accept data after detect debounce pulse edge 01: Start to accept data after detect debounce pulse edge 10: Start to accept data after detect low voltage debounce pulse 11: Start to accept data after detect high voltage debounce pulse
5:4	R/W	0x0	CIR ENABLE 00~10: Reserved 11: CIR mode enable
3:2	/	/	/.
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

8.5.3.2. CIR Receiver Configure Register(Default Value: 0x0000_0004)

Offset: 0x0010			Register Name: CIR_RXCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R/W	0x0	RPA Receiver Packet Abort bit. Determines behavior of the RX FIFO upon detection of an illegal symbol. When an illegal symbol is detected, the DDE or CRCE bit in the receiver status register is set. If the RPA bit is set, the RX FIFO pointers are cleared and the receiver starts to search for the PA or STA fields for FIR and MIR mode, respectively. If RPA is cleared, the receiver continues to write to the RX FIFO. 0: Does not clear the RX FIFO upon detection of an illegal symbol 1: Clears the RX FIFO upon detection of illegal symbol
2	R/W	0x1	RPPI Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

8.5.3.3. CIR Receiver FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: CIR_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R	0x0	RX_DATA Receiver Byte FIFO

8.5.3.4. CIR Receiver Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: CIR_RXINT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0x0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when the condition fails.
4	R/W	0x0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to '1', the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when the condition fails.
3:2	/	/	/
1	R/W	0x0	RPEI_EN Receiver Packet End Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

8.5.3.5. CIR Receiver Status Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:8	R	0x0	RAC RX FIFO Available Counter 0000000: No available data in RX FIFO

Offset: 0x0030			Register Name: CIR_RXSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
			0000001: 1 byte available data in RX FIFO 0000010: 2 byte available data in RX FIFO … 1000000: 64 byte available data in RX FIFO
7	R	0x0	STAT Status of CIR 0: Idle 1: Busy
6:5	/	/	/
4	R/W1C	0x0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W1C	0x0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0x0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

8.5.3.6. CIR Configure Register(Default Value: 0x0000_1828)

Offset: 0x0034			Register Name: CIR_CFR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:25	/	/	/
24	R/W	0x0	SCS2 Bit2 of Sample Clock Select for CIR This bit is defined by SCS bits below.
23	R/W	0x0	ATHC Active Threshold Control for CIR 0: ATHR in Unit of (Sample Clock) 1: ATHR in Unit of (128*Sample Clocks)
22:16	R/W	0x0	ATHR Active Threshold for CIR These bits control the duration of CIR from Idle to Active State. The duration can be calculated by ((ATHR + 1)*(ATHC? Sample Clock: 128*Sample Clock)).
15:8	R/W	0x18	ITHR

<table>
<tr><td colspan="3">Offset: 0x0034</td><td>Register Name: CIR_CFR</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td></td><td></td><td></td><td>Idle Threshold for CIR
The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enable, the interrupt line is asserted to CPU.
When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.</td></tr>
<tr><td>7:2</td><td>R/W</td><td>0xa</td><td>NTHR
Noise Threshold for CIR
When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware.

0: All samples are recorded into RX FIFO
1: If the signal is only one sample duration, it is taken as noise and discarded.
2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded.
…
61: If the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.</td></tr>
<tr><td>1:0</td><td>R/W</td><td>0x0</td><td>SCS
Sample Clock Select for CIR
<table>
<tr><td>SCS2</td><td>SCS[1]</td><td>SCS[0]</td><td>Sample Clock</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CIR_CLK/64</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>CIR_CLK/128</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>CIR_CLK/256</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>CIR_CLK/512</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>CIR_CLK</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
</table>

8.6. USB OTG

8.6.1. Overview

The USB OTG is a dual-role device controller, which supports both device and host functions and is full compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a. It can also be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode.

Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. For saving CPU bandwidth, USB OTG DMA interface can support external DMA controller to take care of the data transfer between the memory and USB OTG FIFO. The USB OTG core also supports USB power saving functions.

Features:

- Complies with USB 2.0 Specification
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode and High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the UTMI+ Level 3 interface . The 8-bit bidirectional data buses are used
- Supports bi-directional endpoint0 for Control transfer
- Supports up to 8 User-Configurable Endpoints for Bulk , Isochronousl and Interrupt bi-directional transfers
- Supports up to (8KB+64Bytes) FIFO for EPs (Excluding EP0)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Normal DMA controller for every EPs

8.6.2. Timing Diagram

Please refer USB2.0 Specification and its On-The-Go Supplement to the USB 2.0 Specification.

8.7. USB Host

8.7.1. Overview

USB Host controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host controller, as well as full and low speed through one or more integrated OHCI host controllers.

Features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports bus.
- Supports 32-bit Little Endian AMBA AHB Slave bus for register access
- Supports 32-bit Little Endian AMBA AHB Master bus for memory access.
- An internal DMA Controller for data transfer with memory.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) device
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- Supports only 1 USB Root Port shared between EHCI and OHCI

8.7.2. Block Diagram

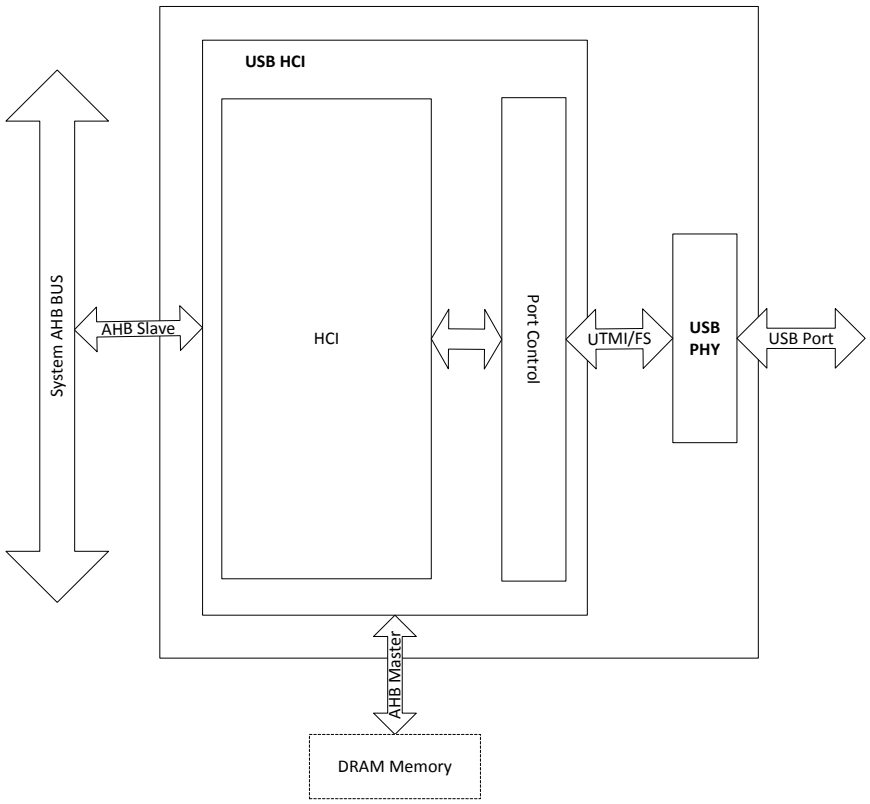


Figure 8-17. USB Host Block Diagram

8.7.3. Timing Diagram

Please refer USB2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

8.7.4. Register List

Module Name	Base Address
USB1_HOST	0x01C19000
USB2_HOST	0x01C1C000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x0000	EHCI Capability Length Register
E_HCIVERSION	0x0002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x0004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x0008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x000C	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x0010	EHCI USB Command Register
E_USBSTS	0x0014	EHCI USB Status Register
E_USBINTR	0x0018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x001C	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x0020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x0024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x0028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x0050	EHCI Configured Flag Register
E_PORTSC	0x0054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x0400	OHCI Revision Register
O_HcControl	0x0404	OHCI Control Register
O_HcCommandStatus	0x0408	OHCI Command Status Register
O_HcInterruptStatus	0x040C	OHCI Interrupt Status Register
O_HcInterruptEnable	0x0410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x0414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x0418	OHCI HCCA Base
O_HcPeriodCurrentED	0x041C	OHCI Period Current ED Base
O_HcControlHeadED	0x0420	OHCI Control Head ED Base
O_HcControlCurrentED	0x0424	OHCI Control Current ED Base
O_HcBulkHeadED	0x0428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x042C	OHCI Bulk Current ED Base
O_HcDoneHead	0x0430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x0434	OHCI Frame Interval Register
O_HcFmRemaining	0x0438	OHCI Frame Remaining Register
O_HcFmNumber	0x043C	OHCI Frame Number Register
O_HcPerioddicStart	0x0440	OHCI Periodic Start Register
O_HcLSThreshold	0x0444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x0448	OHCI Root Hub Descriptor Register A

Register Name	Offset	Description
O_HcRhDesriptorB	0x044C	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x0450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x0454	OHCI Root Hub Port Status Register

8.7.5. EHCI Register Description

8.7.5.1. EHCI Capability Length Register(Default Value: 0x0010)

Offset:0x0000			Register Name: CAPLENGTH
Bit	**Read/Write**	**Default/Hex**	**Description**
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

8.7.5.2. EHCI Host Interface Version Number Register(Default Value: 0x0100)

Offset: 0x0002			Register Name: HCIVERSION
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R	0x0100	**HCIVERSION** This is a 16-bit register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

8.7.5.3. EHCI Host Control Structural Parameter Register(Default Value: 0x0000_1101)

Offset: 0x0004			Register Name: HCSPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:20	R	0x0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	/	/
15:12	R	0x1	N_CC Number of Companion Controller This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0x1	N_PCC Number of Port per Companion Controller This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0x0	PRR Port Routing Rules

Offset: 0x0004			Register Name: HCSPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
			This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation. 0: The first N_PCC ports are routed to the lowest numbered function Companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on 1: The port routing is explicitly enumerated by the first N_PORTS Elements of the HCSP-PORTTOUTE array. This field will always be '0'.
6:4	/	/	/
3:0	R	0x1	N_PORTS This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

8.7.5.4. EHCI Host Control Capability Parameter Register(Default Value: 0x0000_A026)

Offset: 0x0008			Register Name: HCCPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:8	R	0xA0	EECP EHCI Extended Capabilities Pointer This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this class of device. The value of this field is always '00b'.
7:4	R	0x2	IST Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	/	/	/
2	R	0x1	ASPC Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD

Offset: 0x0008			Register Name: HCCPARAMS
Bit	**Read/Write**	**Default/Hex**	**Description**
			register.
1	R	0x1	PFLF Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to configure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	/	/	/

8.7.5.5. EHCI Companion Port Route Description Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: HCSP-PORTROUTE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

8.7.5.6. EHCI USB Command Register(Default Value: 0x0008_0B00)

Offset: 0x0010			Register Name: USBCMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x08	Interrupt Threshold Control The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below: 0x00: Reserved 0x01: 1 micro-frame 0x02: 2 micro-frame

Offset: 0x0010			Register Name: USBCMD
Bit	**Read/Write**	**Default/Hex**	**Description**
			0x04: 4 micro-frame 0x08: 8 micro-frame(default, equates to 1 ms) 0x10: 16 micro-frame(2ms) 0x20: 32 micro-frame(4ms) 0x40: 64 micro-frame(8ms) Any other value in this register yields undefined results. The default value in this field is 0x08 . Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.
15:12	/	/	/
11	R	0x1	Asynchronous Schedule Park Mode Enable(OPTIONAL) If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.
10	/	/	/
9:8	R	0x3	Asynchronous Schedule Park Mode Count(OPTIONAL) Asynchronous Park Capability bit in the HCCPARAMS register is a one, Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid value are 0x1 to 0x3.Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.
7	R/W	0x0	Light Host Controller Reset(OPTIONAL) This control bit is not required. If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships). A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host
6	R/W	0x0	Interrupt on Async Advance Doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one. Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.
5	R/W	0x0	Asynchronous Schedule Enable This bit controls whether the host controller skips processing the

Offset: 0x0010			Register Name: USBCMD
Bit	**Read/Write**	**Default/Hex**	**Description**
			Asynchronous Schedule. Values mean: 0x00: Do not process the Asynchronous Schedule. 0x01: Use the ASYNLISTADDR register to access the Asynchronous schedule. The default value of this field is '0b'.
4	R/W	0x0	Periodic Schedule Enable This bit controls whether the host controller skips processing the Periodic Schedule. Values mean: 0x00: Do not process the Periodic Schedule. 0x01: Use the PERIODICLISTBASE register to access the Periodic Schedule. The default value of this field is '0b'.
3:2	R/W	0x0	Frame List Size This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean: 0x00: 1024 elements(4096bytes)Default value 0x01: 512 elements(2048byts) 0x02: 256 elements(1024bytes)For resource-constrained condition 0x03: Reserved The default value is '00b'.
1	R/W	0x0	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0x0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller

Offset: 0x0010			Register Name: USBCMD
Bit	Read/Write	Default/Hex	Description
			is in the Halt State. The default value is 0x0.

8.7.5.7. EHCI USB Status Register(Default Value: 0x0000_1000)

Offset: 0x0014			Register Name: USBSTS
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R	0x0	ASS Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0x0	PSS Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to *immediately* disable or enable the Periodic Schedule when software transitions the *Periodic Schedule Enable* bit in the USBCMD register. When this bit and the *Periodic Schedule Enable* bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	R	0x0	RECL Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	0x1	HCH HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	/	/
5	R/WC	0x0	IAA Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0x0	HSE Host System Error The Host Controller set this bit to 1 when a serious error occurs during

Offset: 0x0014			Register Name: USBSTS
Bit	**Read/Write**	**Default/Hex**	**Description**
			a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0x0	FLR Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0x0	PCD Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0x0	ERRINT USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0x0	USBINT USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

8.7.5.8. EHCI USB Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: USBINTR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:6	/	/	/
5	R/W	0x0	IAAE Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0x0	HSEE Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is

Offset: 0x0018			Register Name: USBINTR
Bit	**Read/Write**	**Default/Hex**	**Description**
			acknowledged by software clearing the Host System Error bit.
3	R/W	0x0	FLRE Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0x0	PCIE Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0x0	EIE USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0x0	UIE USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

8.7.5.9. EHCI Frame Index Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: FRINDEX
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:0	R/W	0x0	FRIND Frame Index The value in this register increment at the end of each time frame(e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register. USBCMD[Frame List Size] = 0x00: Number Elements = 1024, N = 12 USBCMD[Frame List Size] = 0x01: Number Elements = 512, N = 11 USBCMD[Frame List Size] = 0x02: Number Elements = 256, N = 10 USBCMD[Frame List Size] = 0x03: Reserved

NOTE

This register must be written as a DWord. Byte writes produce undefined results.

8.7.5.10. EHCI Periodic Frame List Base Address Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: PERIODICLISTBASE
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0024			Register Name: PERIODICLISTBASE
Bit	**Read/Write**	**Default/Hex**	**Description**
31:12	R/W	0x0	BADDR Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	/	/

NOTE

Writes must be Dword Writes.

8.7.5.11. EHCI Current Asynchronous List Address Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: ASYNCLISTADDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	R/W	0x0	LP Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	/

NOTE

Write must be DWord Writes.

8.7.5.12. EHCI Configure Flag Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: CONFIGFLAG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	**CF** **Configure Flag(CF)** Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: 0: Port routing control logic default-routs each port to an implementation dependent classic host controller. 1: Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

NOTE

This register is not used in the normal implementation.

8.7.5.13. EHCI Port Status and Control Register(Default Value:0x0000_2000)

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:22	/		
21	R/W	0x0	WDE Wake on Disconnect Enable(WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
20	R/W	0x0	WCE Wake on Connect Enable(WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.
19:16	R/W	0x0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow: 0x00: The port is NOT operating in a test mode. 0x01: Test J_STATE 0x02: Test K_STATE 0x03: Test SE0_NAK 0x04: Test Packet 0x05: Test FORCE_ENABLE Others: Reserved The default value in this field is '0000b'.
15:14	/	/	/
13	R/W	0x1	PO Port Owner This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port. Default Value = 1b.
12	/	/	/
11:10	R	0x0	LS Line Status These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one. The encoding of the bits are: 00: SE0, Not Low-speed device, perform EHCI reset 01: K-state, Low-speed device, release ownership of port

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
			10: J-state, Not Low-speed device, perform EHCI reset 11: Undefined, Not Low-speed device, perform EHCI reset. This value of this field is undefined if Port Power is zero.
9	/	/	/
8	R/W	0x0	PR Port Reset 1=Port is in Reset. 0=Port is not in Reset. Default value = 0. When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. **NOTE** **when software writes this bit to a one , it must also write a zero to the Port Enable bit.** Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero. The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one. This field is zero if Port Power is zero.
7	R/W	0x0	SUSPEND Suspend Port Enabled Bit and Suspend bit of this register define the port states as follows: 00: Disable 01: Disable 10: Enable 11: Suspend When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when: 1) Software sets the Force Port Resume bit to a zero(from a one). 2) Software sets the Port Reset bit to a one(from a zero). If host software sets this bit to a one when the port is not enabled(i.e.

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
			Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'.
6	R/W	0x0	FPR Force Port Resume 1: Resume detected/driven on port. 0: No resume (K-state) detected/ driven on port. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0x0	OCC Over-current Change This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0x0	OCA Over-current Active 0: This port does not have an over-current condition. 1: This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0x0	PEDC Port Enable/Disable Change 1: Port enabled/disabled status has changed. 0: No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0x0	PED Port Enabled/Disabled

Offset: 0x0054			Register Name: PORTSC
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable 0: Disable Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset. The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0x0	CSC Connect Status Change 1: Change in Current Connect Status 0: No change Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0x0	CCS Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the **CSC** bit to be set. This field is zero if Port Power zero.

NOTE

This register is only reset by hardware or in response to a host controller reset.

8.7.6. OHCI Register Description

8.7.6.1. OHCI Revision Register(Default Value: 0x0000_0010)

Offset: 0x0400				Register Name: HcRevision
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:8	/	/	/	/
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of

				0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

8.7.6.2. OHCI Control Register(Default Value: 0x0000_0000)

Offset: 0x0404				Register Name: HcRevision
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:11	/	/	/	/
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in *HcInterruptStatus* is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.
8	R/W	R	0x0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	R/W	0x0	HostControllerFunctionalState for USB 00: USBReset 01: USBResume 10: USBOperational 11: USBSuspend A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	R/W	R	0x0	BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcBulkCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcBulkCurrentED* before re-enabling processing of the list.
4	R/W	R	0x0	ControlListEnable This bit is set to enable the processing of the Control list in the next

				Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If *HcControlCurrentED* is pointing to an ED to be removed, HCD must advance the pointer by updating *HcControlCurrentED* before re-enabling processing of the list.
3	R/W	R	0x0	IsochronousEnable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.

CBSR	No. of Control EDs Over Bulk EDs Served
0	1:1
1	2:1
2	3:1
3	4:1

The default value is 0x0.

8.7.6.3. OHCI Command Status Register(Default Value: 0x0000_0000)

Offset: 0x0408				Register Name: HcCommandStatus
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:18	/	/	/	/
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in *HcInterruptStatus* has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	/	/
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in *HcInterruptStatus*. After the changeover, this bit is cleared and remains so until the next request from OS HCD.

2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BFL to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CLF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g, the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

8.7.6.4. OHCI Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x040C				**Register Name: HcInterruptStatus**
	Read/Write			
Bit	HCD	HC	**Default/Hex**	**Description**
31:7	/	/	/	/
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of *HcRhStatus* or the content of any of *HcRhPortStatus*[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of *HcFmNumber* (bit 15) changes value, from 0 to 1 or from 1 to 0, and after *HccaFrameNumber* has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.

2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written *HcDoneHead* to *HccaDoneHead*. Further updates of the *HccaDoneHead* will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of *HccaDoneHead*.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of *HccaFrameNumber*. A scheduling overrun will also cause the SchedulingOverrunCount of *HcCommandStatus* to be Incremented.

8.7.6.5. OHCI Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0410				**Register Name: HcInterruptEnable**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	R/W	R	0x0	MasterInterruptEnable A '0' writtern to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Write back Done Head
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0: Ignore 1: Enable interrupt generation due to Scheduling Overrun

8.7.6.6. OHCI Interrupt Disable Register(Default Value: 0x0000_0000)

Offset: 0x0414				Register Name: HcInterruptDisable
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	/	/
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Root Hub Status Change
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Frame Number Over Flow
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Unrecoverable Error
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Resume Detected
2	R/W	R	0x0	StartofFrame Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Start of Flame
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Write back Done Head
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0: Ignore 1: Disable interrupt generation due to Scheduling Overrun

8.7.6.7. OHCI HCCA Register(Default Value: 0x0000_0000)

Offset: 0x0418				Register Name: HcHCCA
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R/W	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

8.7.6.8. OHCI Period Current ED Register(Default Value: 0x0000_0000)

Offset: 0x041C				Register Name: HcPeriodCurrentED(PCED)
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	PCED[31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R/W	0x0	PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.7.6.9. OHCI Control Head ED Register(Default Value: 0x0000_0000)

Offset: 0x0420				Register Name: HcControlHeadED[CHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	CHED[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R/W	R	0x0	CHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.7.6.10. OHCI Control Current ED Register(Default Value: 0x0000_0000)

Offset: 0x0424				Register Name: HcControlCurrentED[CCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially , this is set to zero to indicate the end of the Control list.
3:0	R/W	R/W	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the

				PCED, through bit 0 to bit 3 must be zero in this field.

8.7.6.11. OHCI Bulk Head ED Register(Default Value: 0x0000_0000)

Offset: 0x0428				Register Name: HcBulkHeadED[BHED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R	0x0	BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R/W	R	0x0	BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.7.6.12. OHCI Bulk Current ED Register(Default Value: 0x0000_0000)

Offset: 0x042C				Register Name: HcBulkCurrentED[BCED]
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R/W	R/W	0x0	BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of *HcBulkHeadED* to *HcBulkCurrentED* and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of *HcControl* is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R/W	R/W	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.7.6.13. OHCI Done Head Register(Default Value: 0x0000_0000)

Offset: 0x0430				Register Name: HcDoneHead
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of *HcDoneHead* to the NextTD field of the TD. HC then overwrites the content of *HcDoneHead* with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the **WritebackDoneHead** of *HcInterruptStatus*.
3:0	R	R/W	0x0	HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for

				the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

8.7.6.14. OHCI FmInterval Register(Default Value: 0x0000_2EDF)

Offset: 0x0434				Register Name: HcFmInterval Register
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	/	/
13:0	R/W	R	0x2EDF	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of *HcCommandStatus* as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

8.7.6.15. OHCI Frame Remaining Register(Default Value:0x0000_0000)

Offset: 0x0438				Register Name: HcFmRemaining
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of *HcFmInterval* whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	/	/
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in *HcFmInterval* at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of *HcFmInterval* and uses the updated value from the next SOF.

8.7.6.16. OHCI Frame Number Register(Default Value: 0x0000_0000)

Offset: 0x043C				Register Name: HcFmNumber
Bit	Read/Write		Default/Hex	Description
	HCD	HC		
31:16	/	/	/	/

15:0	R	R/W	0x0	FrameNumber This is incremented when *HcFmRemaining* is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the **FrameNumber** at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the **StartofFrame** in *HcInterruptStatus.*

8.7.6.17. OHCI Periodic Start Register(Default Value: 0x0000_0000)

Offset: 0x0440				**Register Name: HcPeriodicStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:14	/	/	/	/
13:0	R/W	R	0x0	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from *HcFmInterval*.. A typical value will be 0x3e67. When *HcFmRemaining* reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

8.7.6.18. OHCI LS Threshold Register(Default Value: 0x0000_0628)

Offset: 0x0444				**Register Name: HcLSThreshold**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:12	/	/	/	/
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the **FrameRemaining** field prior to initiating a Low Speed transaction. The transaction is started only if **FrameRemaining** >= this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.7.6.19. OHCI Root Hub DescriptorA Register(Default Value: 0x0200_1201)

Offset: 0x0448				**Register Name: HcRhDescriptorA**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT] This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13	/	/	/	/
12	R/W	R	0x1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting.

				0: Over-current status is reported collectively for all downstream ports 1: No overcurrent protection supported
11	R/W	R	0x0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0: Over-current status is reported collectively for all downstream ports 1: Over-current status is reported on per-port basis
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	0x1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0: All ports are powered at the same time 1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower)
8	R/W	R	0x0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0: Ports are power switched 1: Ports are always powered on when the HC is powered on
7:0	R	R	0x1	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.

8.7.6.20. OHCI Root Hub DescriptorB Register(Default Value: 0x0000_0000)

Offset: 0x044C				**Register Name: HcRhDescriptorB**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:16	R/W	R	0x0	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when **PowerSwitchingMode** is set. When set, the port's power state is only affected by per-port power control (**Set/ClearPortPower**). When cleared, the port is controlled by the global power switch (**Set/ClearGlobalPower**). If the device is configured to global switching mode (**PowerSwitchingMode** = 0), this field is not valid.

				Bit0: Reserved Bit1: Ganged-power mask on Port #1 Bit2: Ganged-power mask on Port #2 … Bit15: Ganged-power mask on Port #15
15:0	R/W	R	0x0	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0: Reserved Bit1: Device attached to Port #1 Bit2: Device attached to Port #2 … Bit15: Device attached to Port #15

8.7.6.21. OHCI Root Hub Status Register(Default Value: 0x0000_0000)

Offset: 0x0450				Register Name: HcRhStatus Register
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31	W	R	0x0	(write)ClearRemoteWakeupEnable Writing a ‘1’ clears **DeviceRemoteWakeupEnable.** Writing a ‘0’ has no effect.
30:18	/	/	/	/
17	R/W	R	0x0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the **OverCurrentIndicator** field of this register. The HCD clears this bit by writing a ‘1’.Writing a ‘0’ has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’. (write)SetGlobalPower In global power mode (**PowerSwitchingMode**=0), This bit is written to ‘1’ to turn on power to all ports (clear **PortPowerStatus**). In per-port power mode, it sets **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a ‘0’ has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a **ConnectStatusChange** bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the **ResumeDetected** interrupt. 0x0: **ConnectStatusChange** is not a remote wakeup event 0x1: **ConnectStatusChange** is a remote wakeup even (write)SetRemoteWakeupEnable Writing a ‘1’ sets DeviceRemoveWakeupEnable. Writing a ‘0’ has no effect.
14:2	/	/	/	/
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always ‘0’

0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (**PowerSwitchingMode**=0), This bit is written to '1' to turn off power to all ports (clear **PortPowerStatus**). In per-port power mode, it clears **PortPowerStatus** only on ports whose **PortPowerControlMask** bit is not set. Writing a '0' has no effect.

8.7.6.22. OHCI Root Hub Port Status Register(Default Value: 0x0000_0100)

Offset: 0x0454				**Register Name: HcRhPortStatus**
Bit	**Read/Write**		**Default/Hex**	**Description**
	HCD	**HC**		
31:21	/	/	/	/
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: port reset is not complete 1: port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the **PortOverCurrentIndicator** bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: no change in **PortOverCurrentIndicator** 1: **PortOverCurrentIndicator** has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when **ResetStatusChange** is set. 0: resume is not completed 1: resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the **PortEnableStatus** bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0x0: no change in **PortEnableStatus** 0x1: change in **PortEnableStatus**
16	R/W	R/W	0x0	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If **CurrentConnectStatus** is cleared when a **SetPortReset,SetPortEnable**, or **SetPortSuspend** write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if

				the port is disconnected. 0: no change in **PortEnableStatus** 1: change in **PortEnableStatus** **NOTE** **If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.**
15:10	/	/	/	/
9	R/W	R/W	0x0	(read)LowSpeedDeviceAttached This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the **CurrentConnectStatus** is set. 0: full speed device attached 1: low speed device attached (write)ClearPortPower The HCD clears the **PortPowerStatus** bit by writing a '1' to this bit. Writing a '0' has no effect.
8	R/W	R/W	0x1	(read)PortPowerStatus This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing **SetPortPower** or **SetGlobalPower**. HCD clears this bit by writing **ClearPortPower** or **ClearGlobalPower**. Which power control switches are enabled is determined by **PowerSwitchingMode** and **PortPortControlMask[**NumberDownstreamPort**]**. In global switching mode(**PowerSwitchingMode**=0), only **Set/ClearGlobalPower** controls this bit. In per-port power switching (**PowerSwitchingMode**=1), if the **PortPowerControlMask[NDP]** bit for the port is set, only **Set/ClearPortPower** commands are enabled. If the mask is not set, only **Set/ClearGlobalPower** commands are enabled. When port power is disabled, **CurrentConnectStatus**, **PortEnableStatus**, **PortSuspendStatus**, and **PortResetStatus** should be reset. 0: port power is off 1: port power is on (write)SetPortPower The HCD writes a '1' to set the **PortPowerStatus** bit. Writing a '0' has no effect. **NOTE** **This bit is always reads '1b' if power switching is not supported.**
7:5	/	/	/	/
4	R/W	R/W	0x0	(read)PortResetStatus When this bit is set by a write to **SetPortReset**, port reset signaling is asserted. When reset is completed, this bit is cleared when **PortResetStatusChange** is set. This bit cannot be set if **CurrentConnectStatus** is cleared. 0: port reset signal is not active

				1: port reset signal is active (write)SetPortReset The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If **CurrentConnectStatus** is cleared, this write does not set **PortResetStatus**, but instead sets **ConnectStatusChange**. This informs the driver that it attempted to reset a disconnected port.
3	R/W	R/W	0x0	(read)PortOverCurrentIndicator This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal. 0: no overcurrent condition 1: overcurrent condition detected (write)ClearSuspendStatus The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if **PortSuspendStatus** is set.
2	R/W	R/W	0x0	(read)PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. It is set by a **SetSuspendState** write and cleared when **PortSuspendStatusChange** is set at the end of the resume interval. This bit cannot be set if **CurrentConnectStatus** is cleared. This bit is also cleared when **PortResetStatusChange** is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0: port is not suspended 1: port is suspended (write)SetPortSuspend The HCD sets the **PortSuspendStatus** bit by writing a '1' to this bit. Writing a '0' has no effect. If **CurrentConnectStatus** is cleared, this write does not set **PortSuspendStatus**; instead it sets **ConnectStatusChange**. This informs the driver that it attempted to suspend a disconnected port.
1	R/W	R/W	0x0	(read)PortEnableStatus This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes **PortEnabledStatusChange** to be set. HCD sets this bit by writing **SetPortEnable** and clears it by writing **ClearPortEnable**. This bit cannot be set when **CurrentConnectStatus** is cleared. This bit is also set, if not already, at the completion of a port reset when **ResetStatusChange** is set or port suspend when **SuspendStatusChange** is set. 0: port is disabled 1: port is enabled (write)SetPortEnable The HCD sets **PortEnableStatus** by writing a '1'. Writing a '0' has no effect. If **CurrentConnectStatus** is cleared, this write does not set

				PortEnableStatus, but instead sets **ConnectStatusChange**. This informs the driver that it attempted to enable a disconnected Port.
0	R/W	R/W	0x0	(read)CurrentConnectStatus This bit reflects the current state of the downstream port. 0: No device connected 1: Device connected (write)ClearPortEnable The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write. **NOTE** **This bit is always read '1' when the attached device is nonremovalble(DviceRemoveable[NumberDownstreamPort]).**

8.7.7. HCI Controller and PHY Interface Description

8.7.7.1. HCI Interface Register(Default Value:0x1000_0000)

Offset:0x0800			**Register Name: USB_CTRL**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	DMA Transfer Status Enable 0: Disable 1: Enable
27:26	/	/	/
25	R/W	0x0	OHCI count select 0: Normal mode, the counters will count full time 1: Simulation mode, the counters will be much shorter then real time
24	R/W	0x0	Simulation mode 0: No effect 1: Set PHY in a non-driving mode so the EHCI can detect device connection, this is used only for simulation.
23:21	/	/	/
20	R/W	0x0	EHCI HS force Set 1 to this field force the ehci enter the high speed mode during bus reset. This field only valid when the bit 1 is set.
19:13	/	/	/
12	R/W	0x0	PP2VBUS 0: ULPI wrapper will ignore the difference between power status of root hub and ULPI PHY 1: ULPI wrapper interface will automatically set or clear DrvVbus register in ULPI PHY according to the port power status form the root hub
11	R/W	0x0	AHB Master interface INCR16 enable 0: Do not use INCR16,use other enabled INCRX or unspecified length burst INCR

Offset:0x0800			Register Name: USB_CTRL
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Use INCR16 when appropriate
10	R/W	0x0	AHB Master interface INCR8 enable 0: Do not use INCR8,use other enabled INCRX or unspecified length burst INCR 1: Use INCR8 when appropriate
9	R/W	0x0	AHB Master interface burst type INCR4 enable 0: Do not use INCR4,use other enabled INCRX or unspecified length burst INCR 1: Use INCR4 when appropriate
8	R/W	0x0	AHB Master interface INCRX align enable 0: Start burst on any double word boundary 1: start INCRx burst only on burst x-align address **NOTE** **This bit must enable if any bit of bit[11:9] is enabled.**
7:1	/	/	/
0	R/W	0x0	ULPI Bypass Enable 0: Enable ULPI interface, disable UTMI interface 1: Enable UTMI interface, disable ULPI interface

8.8. I2S/PCM

8.8.1. Overview

The I2S/PCM controller is used to transfer streaming audio-data between the system memory and the codec chip. The controller supports standard I2S format, Left-justified Mode format, Right-justified Mode format, PCM Mode format and TDM Mode format. This interface is most commonly used by consumer audio market, including compact disc, digital audio tape, digital sound processors, and digital TV-sound.

Features:

- 2 I2S/PCM controllers
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
- Compliant with Left-justified, Right-justified, PCM mode, and TDM (Time Division Multiplexing) format
- Supports different sample period width in each interface when using LRCK and LRCKR at the same time
- Supports full-duplex synchronous work mode
- Supports Master/Slave mode
- Supports adjustable interface voltage
- Supports clock up to 100MHz
- Supports adjustable audio sample resolution from 8-bit to 32-bit
- Supports up to 8 slots which has adjustable width from 8-bit to 32-bit
- Supports sample rate from 8kHz to 192kHz
- Supports 8-bit u-law and 8-bit A-law companded sample
- One 128 depth x 32-bit width FIFO for data transmit, one 64 depth x 32-bit width FIFO for data receive
- Supports programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Programmable FIFO thresholds
- Interrupt and DMA Support

8.8.2. Block Diagram

The I2S/PCM block diagram is shown below.

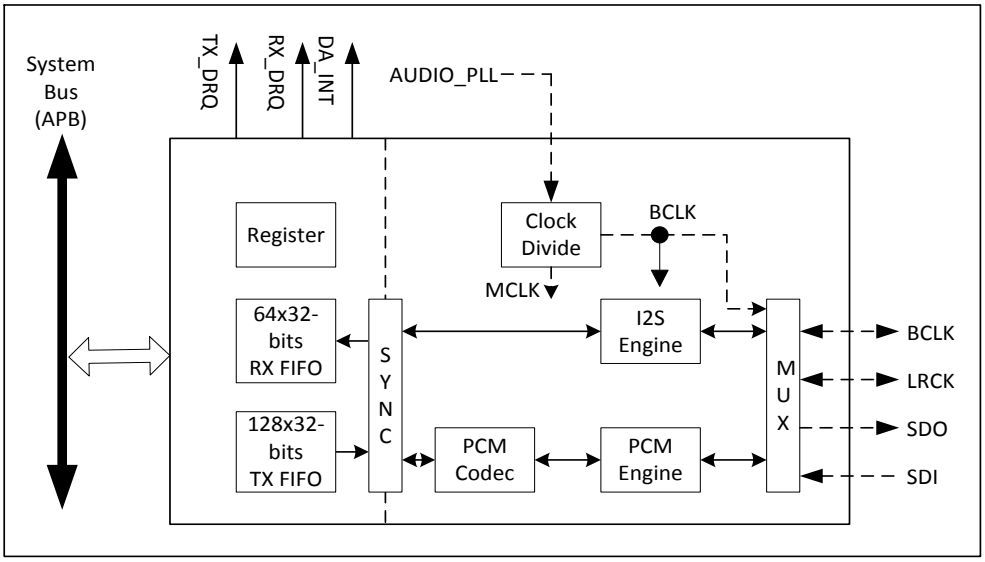


Figure 8-18. I2S/PCM Block Diagram

8.8.3. Operations and Functional Descriptions

8.8.3.1. External Signals

Table 8-10 describes the external signals of I2S/PCM interface. BCLK and LRCK are bidirectional I/O, when I2S/PCM interface is configured as Master device, BCLK and LRCK is output pin; when I2S/PCM interface is configured as slave device, BCLK and LRCK is input pin. MCLK is an output pin for external device. SDO is always the serial data output pin, and SDI is the serial data input. For information about General Purpose I/O port, see **Port Controller**.

Table 8-10. I2S/PCM Interface External Signals

Signal	Description	Type
I2S_MCLK	I2S/PCM Interface Master Clock Output	O
I2S_LRCK	I2S/PCM Interface Left/Right Channel Select Clock	I/O
I2S_BCLK	I2S/PCM Interface Bit Clock	I/O
I2S_DO[3:0]	I2S/PCM Interface Serial Data Output	O
I2S_DI	I2S/PCM Interface Serial Data Input	I
I2S1_MCLK	I2S/PCM1 Interface Master Clock Output	O
I2S1_LRCK	I2S/PCM1 Interface Left/Right Channel Select Clock	I/O
I2S1_BCLK	I2S/PCM1 Interface Bit Clock	I/O
I2S1_DO	I2S/PCM1 Interface Serial Data Output	O
I2S1_DI	I2S/PCM1 Interface Serial Data Input	I

8.8.3.2. Clock Sources

Table 8-11 describes the clock sources for I2S/PCM. Users can see **CCU** for clock setting, configuration and gating information.

Table 8-11. I2S/PCM Clock Sources

Clock Sources	Description
PLL_Audio	24.576MHz or 22.5792MHz generated by PLL_Audio to produce 48kHz or 44.1kHz serial frequency.

8.8.3.3. I2S/PCM Transmit Format

The I2S/PCM supports standard I2S mode, Left-justified I2S mode, Right-justified I2S mode, PCM mode and TDM mode. Software can select one of them by setting **I2S/PCM_CTL** register. The following figures describe the waveforms for LRCK, BCLK and SDO(DOUT), SDI(DIN).

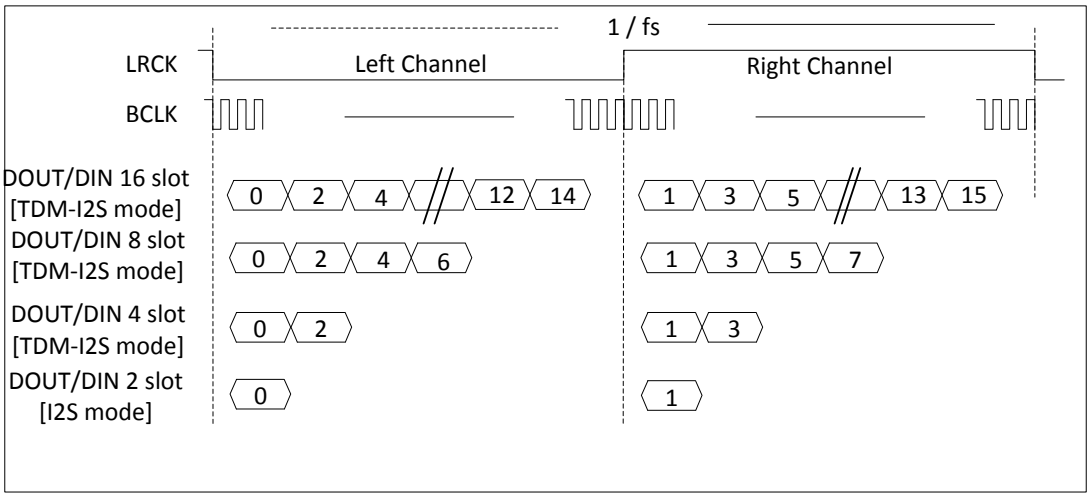


Figure 8-19. Timing Diagram for Standard I2S/TDM-I2S Mode

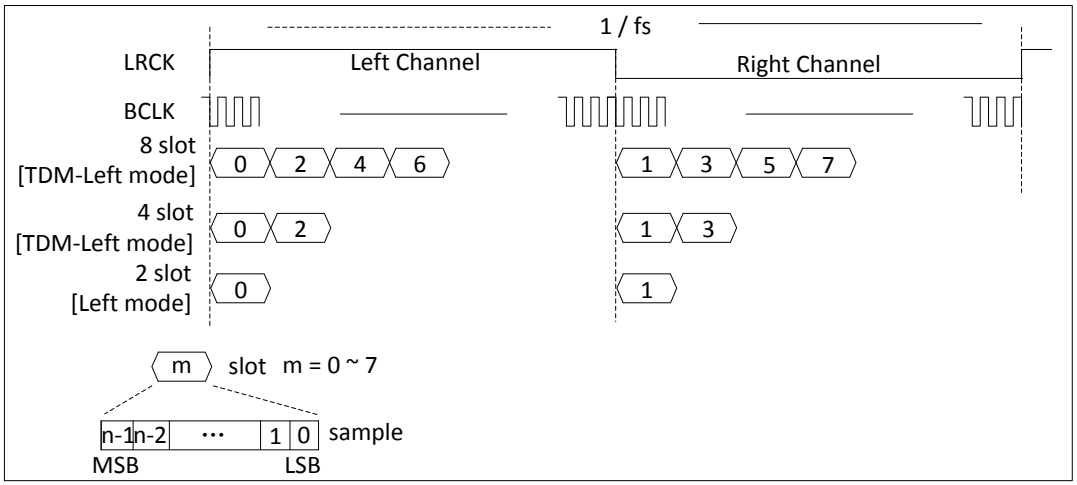


Figure 8-20. Timing Diagram for Left-justified/TDM-Left Mode

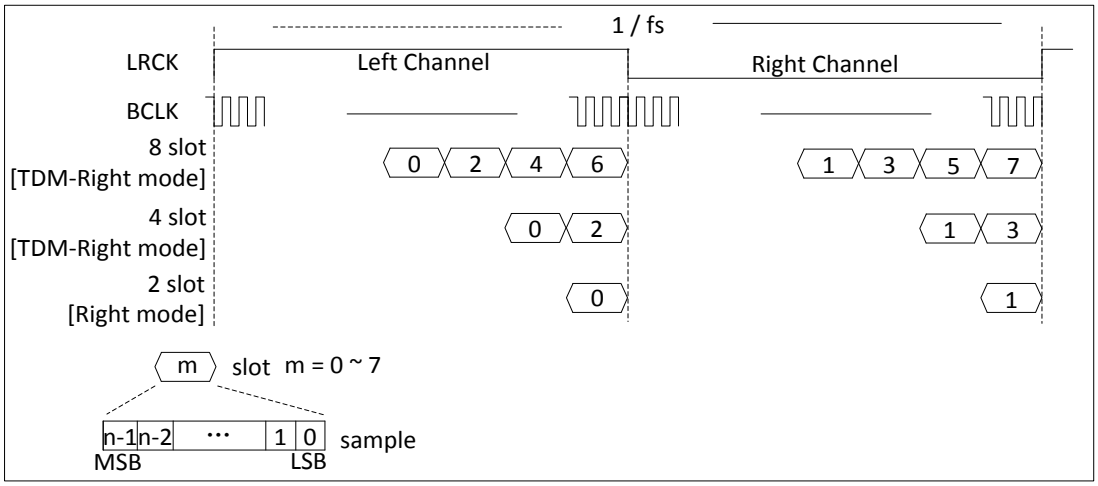


Figure 8-21. Timing Diagram for Right-justified/TDM-Right Mode

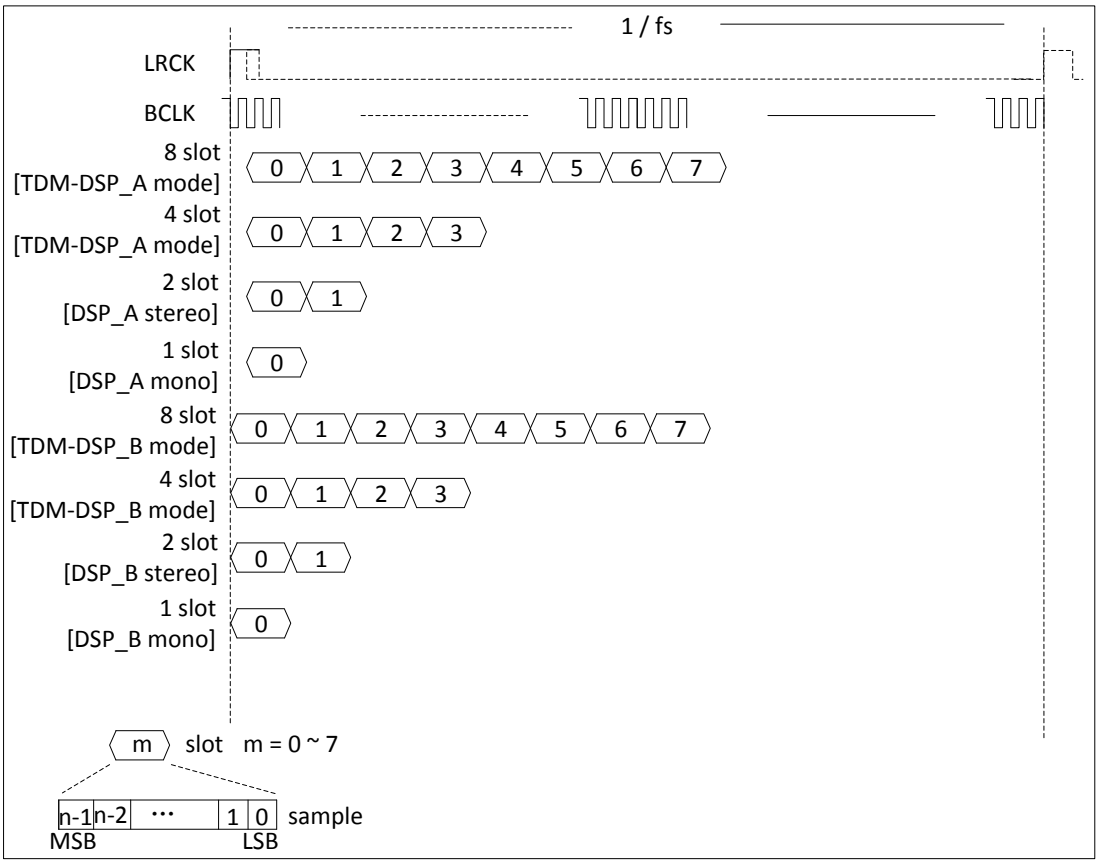


Figure 8-22. Timing Diagram for PCM/TDM-PCM Mode

8.8.3.4. I2S/PCM Operation Modes

The software operation of the I2S/PCM is divided into five steps: system setup, I2S/PCM interface initialization, the channel setup, DMA setup and Enable/Disable module. The five steps are described in detail in the following sections.

(1) System setup and I2S/PCM initialization

The first step in the system setup is properly programming the GPIO. Because the I2S/PCM port is a multiplex pin. You can find the function in **Port Controller**. The clock source for the I2S/PCM should be followed. At first you must reset the Audio PLL through the PLL_ENABLE bit of **PLL_AUDIO Control Register** in the **Chapter 3.3.CCU**. The second step, you must setup the frequency of the Audio PLL in the **PLL_AUDIO Control Register**. After that, you must open the I2S/PCM gating through the **I2S/PCM0 Clock Register**/**I2S/PCM1 Clock Register** when you checkout that the LOCK bit of **PLL_AUDIO Control Register** becomes to 1. At last, you must reset the I2S/PCM by the bit[13:12] of **BUS_SOFT_RST_REG3** and open the I2S/PCM bus gating by the bit[13:12] of **BUS_CLK_GATING_REG2**.

After the system setup, the register of I2S/PCM can be setup. At first, you should initialization the I2S/PCM. You should closed the **Globe Enable** bit(I2S/PCM_CTL[0]) , **Transmitter Block Enable** bit(I2S/PCM_CTL[2]) and **Receiver Block Enable** bit(I2S/PCM_CTL[1]) by writing 0 to it. After that, you must clear the TX/RX FIFO by writing 0 to the bit [25:24] of **I2S/PCM_FCTL**. At last, you can clear the TX/RX FIFO counter by writing 0 to **I2S/PCM_TXCNT**/**I2S/PCM_RXCNT**.

(2) Channel setup and DMA setup

Before the usage and control of I2S/PCM, you must configure the I2C. The configuration of I2C will not describe in this

chapter. But you can only configure I2S/PCM of master and slave through the I2C. The configuration can be referred to the protocol of I2S/PCM. Then, you can set the translation mode, the sample precision, the wide of slot, the frame mode and the trigger level.

The I2S/PCM supports three methods to transfer the data. The most common way is DMA, the setting of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3) Enable and disable the I2S/PCM

To enable the function, you can enable TX/RX by writing the bit[2:1] of the **I2S/PCM_CTL** register. After that, you must enable I2S/PCM by writing the **GEN** bit to 1. Writing the **GEN** bit to 0 to disable I2S/PCM.

8.8.4. Programming Guidelines

The following example assumes that the audio channels are stereo channels in I2S mode, the sampling rate is 48 kHz, the sampling precision is 16 bits. The recording and playback processes are as follows.

----------GPIO configuration----------

Step1: Ensure that I2S/PCM1 GPIO has power supply.
Step2: Configure GPIOA9/GPIOA14/GPIOA15/GPIOA16/GPIOA17 as Function6.

----------Clock configuration----------

Step1: Configure PLL_AUDIO as 24.576MHz, that is, set **PLL_AUDIO Control Register** to 0x810D0D00, set **PLL_AUDIO Pattern Control Register** to 0xC000AC02 (If PLL_AUDIO is set as 22.5792MHz, that is, set **PLL_AUDIO Control Register** to 0x81070600, set **PLL_AUDIO Pattern Control Register** to 0xC0010D84).
Step2: Check whether **PLL_AUDIO Control Register**[LOCK] is 0x1. If is 1, set **I2S/PCM0 Clock Register** to 0x80000000.
Step3: Write 0x1 to the bit13 of **Bus Software Reset Register 3** to dessert I2S/PCM1 reset.
Step4: Write 0x1 to the bit13 of **Bus Clock Gating Register 2** to enable I2S/PCM1 gating.

----------Initialization I2S/PCM----------

Step1: Set the bit[2:0] of **I2S/PCM Control Register** to 0 to close TXEN,RXEN and GEN.
Step2: Set the bit[25:24] of **I2S/PCM FIFO Control Register** to 0x3 to clear TXFIFO and RXFIFO.
Step3: Set **I2S/PCM TX Counter Register** to 0 to clear TX counter, set **I2S/PCM RX Counter Register** to 0 to clear RX counter.

----------Format configuration----------

Step1: Master/slave configuration. In master mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0x3; in slave mode, the bit[18:17] of **I2S/PCM RX Counter Register** is set to 0.
Step2: Configure the[5:4] of **I2S/PCM Control Register** to 0x1 to set standard I2S mode, configure the bit[13:12] of **I2S/PCM TX Channel Select Register** to 0x1, configure the bit[13:12] of **I2S/PCM RX Channel Select Register** to 0x1.
Step3: Configure the bit[6:4] of **I2S/PCM Format Register0** to 0x3 to set sample resolution, configure the bit[2:0] of **I2S/PCM Format Register0** to 0x3 to set channel width.
Step4: Configure the bit[6:4] of **I2S/PCM Channel Configuration Register** to 0x1 to set RX channel number, configure the bit[2:0] of **I2S/PCM Channel Configuration Register** to 0x1 to set TX channel number. Configure the bit[11:4] of **I2S/PCM TX Channel Select Register** to 0x3, configure the bit[1:0] of **I2S/PCM TX Channel Select Register** to 0x1. Configure the bit[2:0] of **I2S/PCM RX Channel Select Register** to 0x1.
Step5: Configure the bit[6:0] of **I2S/PCM TX Channel Mapping Register** to 0x10, configure the bit[6:0] of **I2S/PCM RX Channel Mapping Register** to 0x10.

----------Clock divider configuration----------

Step1: Set MCLK divider. Configure the bit[3:0] of **I2S/PCM Clock Divide Register** to 0x1, that is, MCLK=24.576MHz. Configure the bit8 of **I2S/PCM Clock Divide Register** to 0x1 to enable MCLK.

Step2: Set BCLK divider. Configure the bit[7:4] of **I2S/PCM Clock Divide Register** to 0xF, that is, BCLK=Sample ratio*Slot_Width*Slot_Num=48K*16*2=1.536MHz.

Step3: Set LRCK divider. Configure the bit[17:8] of **I2S/PCM Format Register** to 0xF, that is, N-1=BCLK/Sample ratio/ Slot_Num =16,N=15.

----------DMA configuration----------

Step1: Set data width of both DMA_SRC and DMA_DEST to 16-bit.

Step2: Set DMA BLOCK SIZE,DMA_SRC BLOCK SIZE and DMA_DEST BLOCK SIZE to 8.

Step3: TX DMA configuration. Set DMA_SRC_DRQ_TYPE to DRAM, set DMA_SRC_ADDR_MODE to Linear Mode, set DMA_DEST_DRQ_TYPE to I2S/PCM1-TX, set DMA_DEST_ADDR_MODE to IO Mode, set DMA_SRC_ADDR to DRAM address of storing data, set DMA_DEST_ADDR to **I2S/PCM TXFIFO**.

Step4: RX DMA configuration. Set DMA_SRC_DRQ_TYPE to I2S/PCM1-RX, set DMA_SRC_ADDR_MODE to IO Mode, set DMA_DEST_DRQ_TYPE to DRAM, set DMA_DEST_ADDR_MODE to Linear Mode, set DMA_SRC_ADDR to **I2S/PCM RXFIFO**, set DMA_DEST_ADDR to DRAM address of storing data.

For more details about DMA, please see to DMA in section 3.10.

NOTE

If data is stored in SRAM, then DRAM is modified to SRAM.

----------Recording/playback/pause----------

Step1: Enable globe, set the bit0 of **I2S/PCM Control Register** to 0x1.

Step2: Recording start. Set the bit1 of **I2S/PCM Control Register** to 0x1, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step3: Playback start. Set the bit2 of **I2S/PCM Control Register** to 0x1, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0x1.

Step4: Recording pause. Set the bit1 of **I2S/PCM Control Register** to 0, set the bit3 of **I2S/PCM DMA & Interrupt Control Register** to 0.

Step5: Playback pause. Set the bit2 of **I2S/PCM Control Register** to 0, set the bit7 of **I2S/PCM DMA & Interrupt Control Register** to 0.

8.8.5. Register List

Module Name	Base Address
I2S/PCM0	0x01C22000
I2S/PCM1	0x01C22400
I2S/PCM2(for HDMI)	0x01C22800

Register Name	Offset	Description
I2S/PCM_CTL	0x0000	I2S/PCM Control Register
I2S/PCM_FMT0	0x0004	I2S/PCM Format Register 0
I2S/PCM_FMT1	0x0008	I2S/PCM Format Register 1
I2S/PCM_ISTA	0x000C	I2S/PCM Interrupt Status Register
I2S/PCM_RXFIFO	0x0010	I2S/PCM RX FIFO Register
I2S/PCM_FCTL	0x0014	I2S/PCM FIFO Control Register
I2S/PCM_FSTA	0x0018	I2S/PCM FIFO Status Register
I2S/PCM_INT	0x001C	I2S/PCM DMA & Interrupt Control Register

Register Name	Offset	Description
I2S/PCM_TXFIFO	0x0020	I2S/PCM TX FIFO Register
I2S/PCM_CLKD	0x0024	I2S/PCM Clock Divide Register
I2S/PCM_TXCNT	0x0028	I2S/PCM TX Sample Counter Register
I2S/PCM_RXCNT	0x002C	I2S/PCM RX Sample Counter Register
I2S/PCM_CHCFG	0x0030	I2S/PCM Channel Configuration Register
I2S/PCM_TX0CHSEL	0x0034	I2S/PCM TX0 Channel Select register
I2S/PCM_TX1CHSEL	0x0038	I2S/PCM TX1 Channel Select Register
I2S/PCM_TX2CHSEL	0x003C	I2S/PCM TX2 Channel Select Register
I2S/PCM_TX3CHSEL	0x0040	I2S/PCM TX3 Channel Select Register
I2S/PCM_TX0CHMAP	0x0044	I2S/PCM TX0 Channel Mapping Register
I2S/PCM_TX1CHMAP	0x0048	I2S/PCM TX1 Channel Mapping Register
I2S/PCM_TX2CHMAP	0x004C	I2S/PCM TX2 Channel Mapping Register
I2S/PCM_TX3CHMAP	0x0050	I2S/PCM TX3 Channel Mapping Register
I2S/PCM_RXCHSEL	0x0054	I2S/PCM RX Channel Select register
I2S/PCM_RXCHMAP	0x0058	I2S/PCM RX Channel Mapping Register

8.8.6. Register Description

8.8.6.1. I2S/PCM Control Register(Default Value: 0x0006_0000)

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x1	BCLK_OUT 0: Input 1: Output
17	R/W	0x1	LRCK_OUT 0: Input 1: Output
16:12	/	/	/
11	R/W	0x0	SDO3_EN 0: Disable, Hi-Z state 1: Enable
10	R/W	0x0	SDO2_EN 0: Disable, Hi-Z state 1: Enable
9	R/W	0x0	SDO1_EN 0: Disable, Hi-Z state 1: Enable
8	R/W	0x0	SDO0_EN 0: Disable, Hi-Z state 1: Enable
7	/	/	/
6	R/W	0x0	OUT_MUTE 0: Normal transfer

Offset: 0x0000			Register Name: I2S/PCM_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Force DOUT to output 0
5:4	R/W	0x0	MODE_SEL Mode Selection 00: PCM mode (offset 0: DSP_B; offset 1: DSP_A) 01: Left mode (offset 0: LJ mode; offset 1: I2S mode) 10: Right-Justified mode 11: Reserved
3	R/W	0x0	LOOP Loop back test 0: Normal mode 1: Loop back test When set to '1', connecting the SDO with the SDI
2	R/W	0x0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0x0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

8.8.6.2. I2S/PCM Format Register 0(Default Value: 0x0000_0033)

Offset: 0x0004			Register Name: I2S/PCM_FAT0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30	R/W	0x0	LRCK_WIDTH (only apply in PCM mode) LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame)
29:20	/	/	/
19	R/W	0x0	LRCK_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
18	/	/	/

Offset: 0x0004			Register Name: I2S/PCM_FAT0
Bit	**Read/Write**	**Default/Hex**	**Description**
17:8	R/W	0x0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follows: PCM mode: Number of BCLKs within (Left + Right) channel width I2S/Left-Justified/Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) For example: n = 7: 8 BCLK width … n = 1023: 1024 BCLKs width
7	R/W	0x0	BCLK_POLARITY 0: Normal mode, negative edge drive and positive edge sample 1: Invert mode, positive edge drive and negative edge sample
6:4	R/W	0x3	SR Sample Resolution 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit
3	R/W	0x0	EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the same BCLK edge BCLK_POLARITY = 0, use negative edge BCLK_POLARITY = 1, use positive edge
2:0	R/W	0x3	SW Slot Width Select 000: Reserved 001: 8-bit 010: 12-bit 011: 16-bit 100: 20-bit 101: 24-bit 110: 28-bit 111: 32-bit

8.8.6.3. I2S/PCM Format Register 1(Default Value: 0x0000_0030)

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	
7	R/W	0x0	RX MLS MSB / LSB First Select

Offset: 0x0008			Register Name: I2S/PCM_FMT1
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: MSB First 1: LSB First
6	R/W	0x0	TX MLS MSB / LSB First Select 0: MSB First 1: LSB First
5:4	R/W	0x3	SEXT Sign Extend in slot [sample resolution < slot width] 00: Zeros or audio gain padding at LSB position 01: Sign extension at MSB position 10: Reserved 11: Transfer 0 after each sample in each slot
3:2	R/W	0x0	RX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law
1:0	R/W	0x0	TX_PDM PCM Data Mode 00: Linear PCM 01: Reserved 10: 8-bit u-law 11: 8-bit A-law

8.8.6.4. I2S/PCM Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6	R/W1C	0x0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write ‘1’ to clear this interrupt
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt when data in TX FIFO are less than TX trigger level

Offset: 0x000C			Register Name: I2S/PCM_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
			Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
3	/	/	/
2	R/W1C	0x0	RXU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt Write ‘1’ to clear this interrupt
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write ‘1’ to clear this interrupt
0	R/W1C	0x0	RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ when data in RX FIFO are more than RX trigger level Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.

8.8.6.5. I2S/PCM RX FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: I2S/PCM_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

8.8.6.6. I2S/PCM FIFO Control Register(Default Value: 0x0004_00F0)

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio Hub Enable 0 : Disable 1 : Enable
30:26	/	/	/
25	R/W1C	0x0	FTX Write ‘1’ to flush TX FIFO, self clear to ‘0’.
24	R/W1C	0x0	FRX Write ‘1’ to flush RX FIFO, self clear to ‘0’.
23:19	/	/	/
18:12	R/W	0x40	TXTL TX FIFO Empty Trigger Level

Offset: 0x0014			Register Name: I2S/PCM_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL
11:10	/	/	/
9:4	R/W	0xF	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1
3	/	/	/
2	R/W	0x0	TXIM TX FIFO Input Mode (Mode 0, 1) 0: Valid data at the MSB of TXFIFO register 1: Valid data at the LSB of TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[31:0] = {APB_WDATA[31:12], 12'h0} Mode 1: FIFO_I[31:0] = {APB_WDATA[19:0], 12'h0}
1:0	R/W	0x0	RXOM RX FIFO Output Mode (Mode 0, 1, 2, 3) 00: Expanding '0' at LSB of DA_RXFIFO register. 01: Expanding received sample sign bit at MSB of **I2S/PCM_RXFIFO** register. 10: Truncating received samples at high half-word of **I2S/PCM_RXFIFO** register and low half-word of **I2S/PCM_RXFIFO** register is filled by '0'. 11: Truncating received samples at low half-word of **I2S/PCM_RXFIFO** register and high half-word of **I2S/PCM_RXFIFO** register is expanded by its sign bit. Example for 20-bits received audio sample: Mode 0: APB_RDATA[31:0] = {FIFO_O[31:12], 12'h0} Mode 1: APB_RDATA [31:0] = {12{FIFO_O[31]}, FIFO_O[31:12]} Mode 2: APB_RDATA [31:0] = {FIFO_O[31:16], 16'h0} Mode 3: APB_RDATA [31:0] = {16{FIFO_O[31], FIFO_O[31:16]}

8.8.6.7. I2S/PCM FIFO Status Register(Default Value: 0x1080_0000)

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:29	/	/	/
28	R	0x1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0x0	RXA RX FIFO Available

Offset: 0x0018			Register Name: I2S/PCM_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/
6:0	R	0x0	RXA_CNT RX FIFO Available Sample Word Counter

8.8.6.8. I2S/PCM DMA & Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TX FIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable When set to ‘1’, an interrupt happens when writing new audio data if TX FIFO is full.
4	R/W	0x0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	R/W	0x0	RX_DRQ RX FIFO Data Available DRQ Enable 0: Disable 1: Enable When set to ‘1’, RXFIFO DMA Request line is asserted if Data is available in RX FIFO.
2	R/W	0x0	RXUI_EN RX FIFO Underrun Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable

Offset: 0x001C			Register Name: I2S/PCM_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
0	R/W	0x0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

8.8.6.9. I2S/PCM TX FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: I2S/PCM_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA TX Sample Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

8.8.6.10. I2S/PCM Clock Divide Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8	R/W	0x0	MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output **NOTE** **Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.**
7:4	R/W	0x0	BCLKDIV BCLK Divide Ratio from PLL_AUDIO 0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192
3:0	R/W	0x0	MCLKDIV MCLK Divide Ratio from PLL_AUDIO

Offset: 0x0024			Register Name: I2S/PCM_CLKD
Bit	Read/Write	Default/Hex	Description
			0000: Reserved 0001: Divide by 1 0010: Divide by 2 0011: Divide by 4 0100: Divide by 6 0101: Divide by 8 0110: Divide by 12 0111: Divide by 16 1000: Divide by 24 1001: Divide by 32 1010: Divide by 48 1011: Divide by 64 1100: Divide by 96 1101: Divide by 128 1110: Divide by 176 1111: Divide by 192

8.8.6.11. I2S/PCM TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: I2S/PCM_TXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT TX Sample Counter The field is the audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the **TX_CNT** increases by one. The **TX_CNT** can be set to any initial valve at any time. After been updated by the initial value, the **TX_CNT** should count on base of this initial value.

8.8.6.12. I2S/PCM RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: I2S/PCM_RXCNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT RX Sample Counter The field is the audio sample number of writing into RXFIFO. When one sample is written by I2S/PCM controller, the **RX_CNT** increases by one. The **RX_CNT** can be set to any initial valve at any time. After been updated by the initial value, the **RX_CNT** should count on base of this initial value.

8.8.6.13. I2S/PCM Channel Configuration Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	TX_SLOT_HIZ

Offset: 0x0030			Register Name: I2S/PCM_CHCFG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Normal mode for the last half cycle of BCLK in the slot 1: Turn to hi-z state for the last half cycle of BCLK in the slot
8	R/W	0x0	TXn_STATE 0: Transfer level 0 when not transferring slot 1: Turn to hi-z state (TDM) when not transferring slot
7	/	/	/
6:4	R/W	0x0	RX_SLOT_NUM RX Channel/Slot Number which between CPU/DMA and FIFO 000: 1 channel or slot ... 111: 8 channels or slots
3	/	/	/
2:0	R/W	0x0	TX_SLOT_NUM TX Channel/Slot Number which between CPU/DMA and FIFO 000: 1 channel or slot ... 111: 8 channels or slots

8.8.6.14. I2S/PCM TXn Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: I2S/PCM_TXnCHSEL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:12	R/W	0x0	TXn_OFFSET TXn offset tune, TX data offset to LRCK 00: No offset 01: Data is offset by 1 BCLKs to LRCK 10: Data is offset by 2 BCLKs to LRCK 11: Data is offset by 3 BCLKs to LRCK
11:4	R/W	0x0	TXn_CHEN TXn Channel (slot) enable, bit[11:4] refer to slot[7:0]. When one or more slot(s) is(are) disabled, the affected slot(s) is(are) set to disable state. 0: Disable 1: Enable
3	/	/	/
2:0	R/W	0x0	TXn_CHSEL TXn Channel (slot) number Select for each output 000: 1 channel / slot … 111: 8 channels / slots

8.8.6.15. I2S/PCM TXn Channel Mapping Register(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: I2S/PCM_TXnCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
31	/	/	/
30:28	R/W	0x0	TXn_CH7_MAP TXn Channel7 Mapping 000: 1st sample … 111: 8th sample
27	/	/	/
26:24	R/W	0x0	TXn_CH6_MAP TXn Channel6 Mapping 000: 1st sample … 111: 8th sample
23	/	/	/
22:20	R/W	0x0	TXn_CH5_MAP TXn Channel5 Mapping 000: 1st sample … 111: 8th sample
19	/	/	/
18:16	R/W	0x0	TXn_CH4_MAP TXn Channel4 Mapping 000: 1st sample … 111: 8th sample
15	/	/	/
14:12	R/W	0x0	TXn_CH3_MAP TXn Channel3 Mapping 000: 1st sample … 111: 8th sample
11	/	/	/
10:8	R/W	0x0	TXn_CH2_MAP TXn Channel2 Mapping 000: 1st sample … 111: 8th sample
7	/	/	/
6:4	R/W	0x0	TXn_CH1_MAP TX Channel1 Mapping 000: 1st sample … 111: 8th sample
3	/	/	/

Offset: 0x0044			Register Name: I2S/PCM_TXnCHMAP
Bit	Read/Write	Default/Hex	Description
2:0	R/W	0x0	TXn_CH0_MAP TXn Channel0 Mapping 000: 1st sample … 111: 8th sample

8.8.6.16. I2S/PCM RX Channel Select Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: I2S/PCM_RXCHSEL
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:12	R/W	0x0	RX_OFFSET RX offset tune, RX data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
11:3	/	/	
2:0	R/W	0x0	RX_CHSEL RX Channel (slot) number Select for input 000: 1 channel / slot … 111: 8 channels / slots

8.8.6.17. I2S/PCM RX Channel Mapping Register(Default Value: 0x0000_0000)

Offset: 0x0058			Register Name: I2S/PCM_RXCHMAP
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0x0	RX_CH7_MAP RX Channel7 Mapping 000: 1st sample … 111: 8th sample
27	/	/	/
26:24	R/W	0x0	RX_CH6_MAP RX Channel6 Mapping 000: 1st sample … 111: 8th sample
23	/	/	/
22:20	R/W	0x0	RX_CH5_MAP RX Channel5 Mapping 000: 1st sample …

Offset: 0x0058			Register Name: I2S/PCM_RXCHMAP
Bit	**Read/Write**	**Default/Hex**	**Description**
			111: 8th sample
19	/	/	/
18:16	R/W	0x0	RX_CH4_MAP RX Channel4 Mapping 000: 1st sample … 111: 8th sample
15	/	/	/
14:12	R/W	0x0	RX_CH3_MAP RX Channel3 Mapping 000: 1st sample … 111: 8th sample
11	/	/	/
10:8	R/W	0x0	RX_CH2_MAP RX Channel2 Mapping 000: 1st sample … 111: 8th sample
7	/	/	/
6:4	R/W	0x0	RX_CH1_MAP TX Channel1 Mapping 000: 1st sample … 111: 8th sample
3	/	/	/
2:0	R/W	0x0	RX_CH0_MAP RX Channel0 Mapping 000: 1st sample … 111: 8th sample

8.9. AC97 Interface

8.9.1. Overview

The AC97 interface supports AC97 revision 2.3 features. AC97 controller communicates with AC97 Codec using an audio controller link (AC-link). Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec converts the audio sample to an analog audio waveform. Controller receives the stereo PCM data and the mono Microphone data from Codec then stores in memory.

Features:

- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports APB 32-bit bus width
- Compliant with AC97 2.3 component specification
- Full-duplex synchronous serial interface
- Supports 2 channels, TX (stereo),RX (PCM stereo, MIC mono optional)
- Variable sampling rate AC97 codec interface support, up to 48kHz
- Supports 2-channel and 6-channel audio data output
- DRA mode support
- Only one primary codec support
- Channels support mono or stereo samples of 16(standard), 18(optional) and 20(optional) bit wide
- One 96×20-bit FIFO and one 32×20-bit FIFO for data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

8.9.2. Block diagram

The AC97 provides a bus interface for audio data. This interface is most commonly used by the mainstream PC systems. Figure 8-23 shows a block diagram of the AC97.

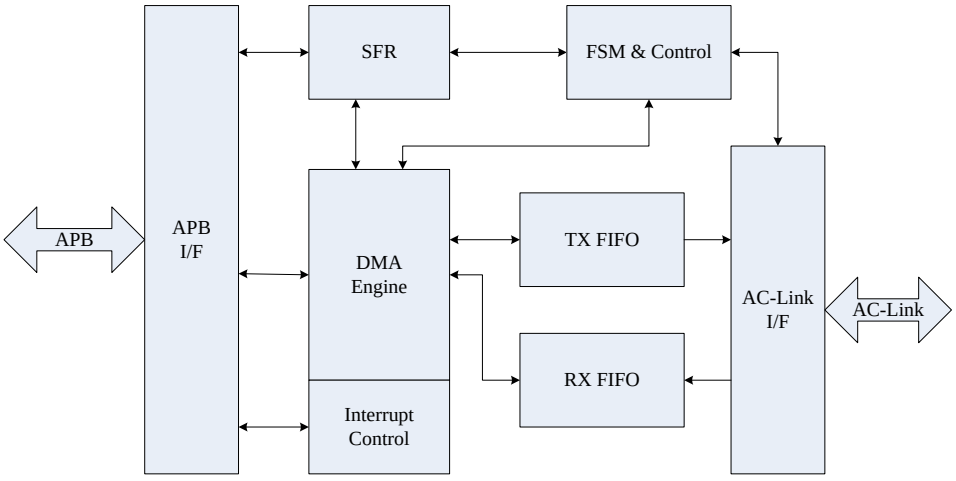


Figure 8-23. AC97 Interface Block Diagram

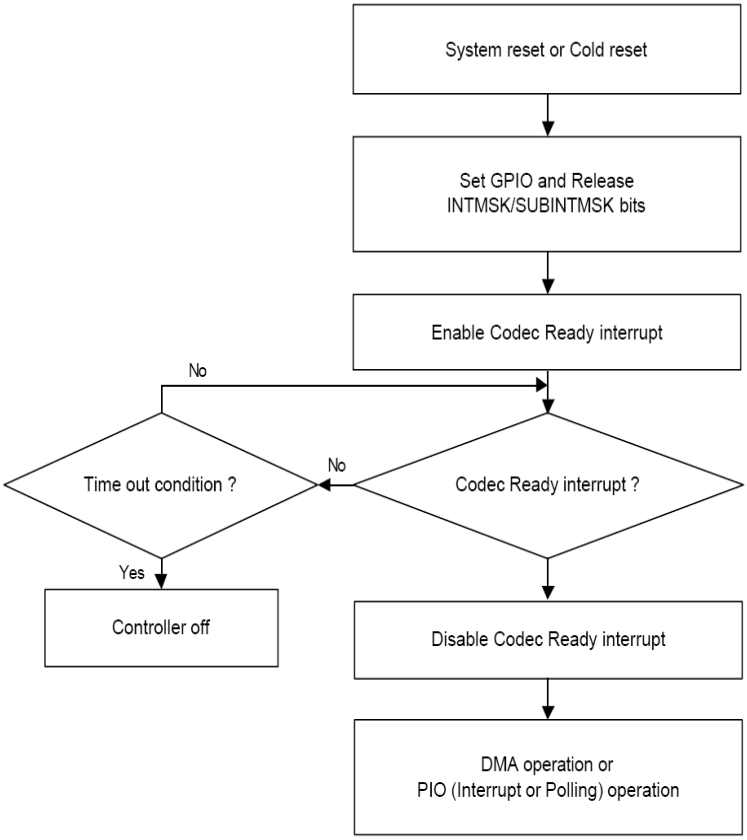


Figure 8-24. AC97 Operation Flow Diagram

8.9.3. Operations and Functional Descriptions

8.9.3.1. External Signals

AC97 is a Digital Audio Transfer protocol. In this protocol, the CLK signal and data signals is transfer in the same line. Table 8-12 describes the external signals of AC97.

Table 8-12. AC97 External Signals

Signal	Description	Type
AC97_BCLK	AC97 Bit Clock	I
AC97_SYNC	AC97 Sample rate/sync	O
AC97_MCLK	AC97 Codec Master Clock	O
AC97_DI	AC97 Data Input	I
AC97_DO	AC97 Data Output	O

8.9.3.2. AC97 Transmit Format

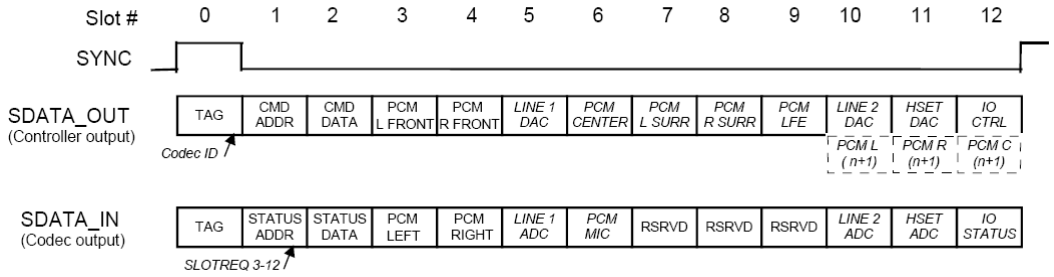


Figure 8-25. Bi-directional AC-link Frame with Slot Assignments

Table 8-13. AC-link Output Slots(transmitted from the Controller)

Slot	Name	Description
0	SDOUT TAG	MSBs indicate which slots contain valid data; LSBs convey Codec ID.
1	Control CMD ADDR write port	Read/write command bit plus 7-bit Codec register address
2	Control DATA write port	16-bit command register write data
3,4	PCM L&R DAC playback	16,18, or 20-bit PCM data for Left and Right channels
5	Modem Line 1 DAC	16-bit modem data for modem Line 1 output
6,7,8,9	PCM Center, Surround L&R, LFE	16,18, or 20-bit PCM data for Center, Surround L&R, LFE channels
10	Modem Line 2 DAC	16-bit modem data for modem Line 2 output
11	Modem handset DAC	16-bit modem data for modem Handset output
12	Modem handset DAC	16-bit data for modem Handset output
10-11	OWA OUT	Optional AC-link bandwidth for OWA output
6-12	Double rate audio	Optional AC-link bandwidth for 88.2 or 96 kHz on L,C,R channels Actual slots used are controlled by the DRSS bits.

Table 8-14. AC-link Input Slots(transmitted from the Codec)

Slot	Name	Description
0	SDATA_IN TAG	MSBs indicate which slots contain valid data
1	STATUS ADDR read port	MSBs echo register address; LSBs indicate which slots request data
2	STATUS DATA read port	16-bit command register read data
3,4	PCM L&R ADC record	16,18 or 20-bit PCM data from Left and Right inputs
5	Modem Line 1 ADC	16-bit modem data from modem Line 1 input
6	Dedicated Microphone ADC	16,18 or 20-bit PCM data from optional 3rd ADC input
7,8,9	Vendor reserved	Vendor specific(enhanced input for docking, array mic, etc)
10	Modem Line 2 ADC	16-bit modem data from modem Line 2 input
11	Modem handset input ADC	16-bit modem data for modem Handset input
12	Modem IO Status	GPIO read port for modem Status

8.9.3.3. Operation Modes

The software operation of the AC97 is divided into five steps: system setup, AC97 initialization, the channel setup, DMA setup and Enable Disable module. These five steps are described in detail in the following sections.

(1) System setup and AC97 initialization

The first step In the AC97 initialization is properly programming the GPIO. Because the AC97 port is a multiplex pin. You can find the function in the **Port Controller**. The clock source for the AC97 should be followed. At first you must reset the audio PLL through the PLL_ENABLE bit of **PLL_AUDIO_CTRL_REG** in the CCU. The second step, you must setup the

frequency of the audio PLL in the **PLL_AUDIO_CTRL_REG**. After that, you must open the AC97 gating through the **AC97_CLK_REG**. At last, you must reset the AC97 by the bit[2] of **BUS_SOFT_RST_REG3** and open the AC97 bus gating by the bit[2] of **BUS_CLK_GATING_REG2**.

After the system setup, the register of AC97 can be setup. At first, you should initialization the AC97. You should close the globe enable bit(**AC-link EN**) , TX enable bit (**TXEN**) and RX enable bit(**RXEN**). After that, you must clear the TX/RX FIFO by writing 0 to register **FTX**/**FRX**. At last, you can clear the TX/RX counter by writing 0 to **AC_TX_CNT**/**AC_RX_CNT**.

(2) Channel setup and DMA setup

Before the usage and control of AC97, you must configure the external codec. Through the **AC_CMD** register you can configure the external codec and get the status by the **AC_CS** register. You can configure the channel and translation mode when the codec are ready. The configuration can be referred to the protocol of AC97. Then, you can set the audio format, the channel selection and the trigger level.

The AC97 supports three methods to transfer the data. The most common way is DMA, the setting of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3) Enable and disable the AC97

To enable the function, you can enable TX/RX by writing the **TXEN**/**RXEN**.After the settings, you can enable AC97 by writing the **GEN** bit to 1. Writing the **GEN** bit to 0 to disable AC97.

8.9.4. Register List

Module Name	Base Address
AC97	0x01C21400

Register Name	Offset	Description
AC_CTL	0x0000	AC97 Control Register
AC_FAT	0x0004	AC97 Format Register
AC_CMD	0x0008	AC97 Command Register
AC_CS	0x000C	AC97 Codec Status Register
AC_RX_FIFO	0x0010	AC97 RX FIFO Register
AC_INT	0x0014	AC97 Interrupt Control Register
AC_FCTL	0x0018	AC97 FIFO Control Register
AC_FSTA	0x001C	AC97 FIFO Status Register
AC_TX_FIFO	0x0020	AC97 TX FIFO Register
AC_ISTA	0x0024	AC97 Interrupt Status Register
AC_TX_CNT	0x0028	AC97 TX Counter Register
AC_RX_CNT	0x002C	AC97 RX Counter Register

8.9.5. Register Description

8.9.5.1. AC97 Control Register(Default Value: 0x0000_0000)

Offset: 0x0000	Register Name: AC_CTL

Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R	0x0	CS_RF CODEC Status Register FLAG 0: Empty 1: Full
17	R	0x0	CMD_RF CMD Register FLAG 0: Empty 1: Full
16	R	0x0	RX_STATUS RX Transfer Status 0: PCM IN 1: MIC IN
15:10	/	/	/
9	R/W	0x0	RX_MODE RX MODE 0: PCM IN 1: MIC IN This bit indicates which mode will be selected when PCM IN and MIC IN slots are available simultaneously
8	R/W	0x0	ASS Audio sample select with TX FIFO under run 0: Sending 0 (invalid frame) 1: Sending the last audio (valid frame)
7	R/W	0x0	TXEN 0: Disable 1: Enable This bit is controlled by **GEN**, we can enable this bit, only after the globe enable bit is enabled.
6	R/W	0x0	RXEN 0: Disable 1: Enable This bit is controlled by **GEN**, we can enable this bit, only after the globe enable bit is enabled.
5	R/W	0x0	AC-link EN 0: Disable 1: Enable(SYNC signal transfer to Codec) This bit is controlled by **GEN**, we can enable this bit, only after the globe enable is enabled.
4	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable
3:2	/	/	/
1	R/W1C	0x0	WARM_RST

Offset: 0x0000			Register Name: AC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
			Warm reset 0: Normal 1: Wake up codec from power down **NOTE** **Self clear to "0".**
0	/	/	/

8.9.5.2. AC97 Format Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: AC_FAT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:9	/	/	/
8:7	R/W	0x0	TX_AUDIO_MODE TX audio mode 00: 2-channel(PCM l/r main) 01: 6-channel(PCM l/r main, l/r surround, center, AFE) 10: Reserved 11: Reserved
6	R/W	0x0	DRA_SLOT_SEL DRA additional slots select (available in 2-channel mode) 0: Select slot 10, slot 11 1: Select slot 7, slot 8
5	R/W	0x0	DRA_MODE DRA mode 0: Non-DRA 1: DRA
4	R/W	0x0	VRA_MODE VRA Mode 0: Non-VRA 1: VRA
3:2	R/W	0x0	TX_RES TX Audio data resolution 00: 16-bit 01: 18-bit 10: 20-bit 11: Reserved
1:0	R/W	0x0	RX_RES RX Audio data resolution 00: 16-bit 01: 18-bit 10: 20-bit 11: Reserved

8.9.5.3. AC97 Codec Command Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: AC_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23	R/W	0x0	OP Read enable 0: Command write 1: Status read
22:16	R/W	0x0	CC_ADDR Codec command address
15:0	R/W	0x0	CC Codec command data

8.9.5.4. AC97 Codec Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: AC_CS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:16	R	0x0	CS_ADDR Codec status address
15:0	R	0x0	CS Codec status data

8.9.5.5. AC97 RX FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: AC_RXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	RX_DATA Host can get one sample by reading this register. If in the PCM IN mode, the left channel sample data is first and then the right channel sample

8.9.5.6. AC97 Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: AC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W	0x0	CODEC_GPIO_EN Codec GPIO interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	CREN Codec Ready interrupt Enable 0: Disable 1: Enable
7	R/W	0x0	TX_DRQ TX FIFO Empty DRQ Enable

Offset: 0x0014			Register Name: AC_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TX FIFO Under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2	R/W	0x0	RX_DRQ RX FIFO Data Available DRQ Enable When set to '1', RX FIFO DMA Request is asserted if data is available in RX FIFO. 0: Disable 1: Enable
1	R/W	0x0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

8.9.5.7. AC97 FIFO Control Register(Default Value: 0x0000_3078)

Offset: 0x0018			Register Name: AC_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio hub enable 0: Disable 1: Enable
30:18	/	/	/
17	R/W1C	0x0	FTX Write '1' to flush TX FIFO, self clear to '0'
16	R/W1C	0x0	FRX Write '1' to flush RX FIFO, self clear to '0'

Offset: 0x0018			Register Name: AC_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R/W	0x30	TXTL TX FIFO empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition Trigger Level = TXTL
7:3	R/W	0x0F	RXTL RX FIFO Trigger Level Interrupt and DMA request trigger level for RX FIFO normal condition Trigger Level =RXTL + 1
2	R/W	0x0	TXIM TX FIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of AC_TXFIFO register 1: Valid data at the LSB of AC_TXFIFO register Example for 18-bit transmitted audio sample: Mode 0: FIFO_I[19:0] = {TXFIFO[31:14], 2'h0} Mode 1: FIFO_I[19:0] = {TXFIFO[17:0], 2'h0}
1:0	R/W	0x0	RXOM RX FIFO Output Mode(Mode 0,1,2,3) 00: Expanding '0' at LSB of AC_RXFIFO register 01: Expanding received sample sign bit at MSB of AC_RXFIFO register 10: Truncating received samples at high half-word of AC_RXFIFO register and low half-word of AC_FIFO register is filled by '0' 11: Truncating received samples at low half-word of AC_RXFIFO register and high half-word of AC_FIFO register is expanded by its sigh bit Example for 18-bit received audio sample: Mode0: RXFIFO[31:0] = {FIFO_O[19:2], 14'h0} Mode 1: RXFIFO[31:0] = {14'FIFO_O[19], FIFO_O[19:2]} Mode 2: RXFIFO[31:0] = {FIFO_O[19:4], 16'h0} Mode 3: RXFIFO[31:0] = {16'FIFO_O[19], FIFO_O[19:4]}

8.9.5.8. AC97 FIFO Status Register(Default Value: 0x0000_C000)

Offset: 0x001C			Register Name: AC_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R	0x1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>=1 word)
14:7	R	0x80	TXE_CNT TX FIFO Empty Space Word counter
6	R	0x0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>=1 word)
5:0	R	0x0	RXA_CNT RX FIFO Available Sample Word counter

8.9.5.9. AC97 TXFIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: AC_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

8.9.5.10. AC97 Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x0024			Register Name: AC_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9	R/W1C	0x0	CODEC_GPIO_INT Codec GPIO interrupt 0: No pending IRQ 1: Codec GPIO interrupt Write ‘1’ to clear this interrupt
8	R/W1C	0x0	CR_INT Codec Ready pending Interrupt 0: No pending IRQ 1: Codec Ready Pending Interrupt Write ‘1’ to clear this interrupt
7	/	/	/
6	R/W1C	0x0	TXU_INT TX FIFO Under run Pending Interrupt 0: No pending IRQ 1: FIFO Under run Pending Interrupt Write ‘1’ to clear this interrupt
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending Interrupt Write ‘1’ to clear this interrupt
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
3:2	/	/	/
1	R/W1C	0x0	RXO_INT RX FIFO Overrun Pending Interrupt 0: FIFO Overrun Pending

Offset: 0x0024			Register Name: AC_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
			Write '1' to clear this interrupt.
0	R/W1C	0x0	RXA_INT RX FIFO Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatically clear if interrupt condition fails.

8.9.5.11. AC97 TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: AC_TX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample counter The audio sample number of writing into TX FIFO. When one sample is written by DMA or by host IO, the TX sample counter register increases by one. The TX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

8.9.5.12. AC97 RX Counter Register(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: AC_RX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_CNT RX Sample counter The audio sample number of writing into RX FIFO. When one sample is written by Codec, the RX sample counter register increases by one. The RX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

8.10. EMAC

8.10.1. Overview

The Ethernet MAC Controller enables the host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M external PHY with MII interface in both full and half duplex mode. A 16KB SRAM is provided to keep continuous data transmission. Besides, the flow control and DA/SA filter are also supported in EMAC module.

Features:

- Supports industry-standard AMBA Host Bus (AHB) and fully comply with the AMBA Specification, Revision 2.0, supports 32-bit Little Endian bus
- Compliant with IEEE 802.3 standard
- Supports 10/100Mbps data rate
- Supports full and half duplex operations
- Supports IEEE 802.3x flow control for full-duplex operation
- Supports back-pressure flow control for half-duplex operation
- Supports DA/SA filter
- Supports loop back operation
- Provides MII Interface for external Ethernet PHY
- 3KB FIFO for TX
- 13KB FIFO for RX

8.10.2. Block Diagram

Figure 8-26 shows a block diagram of the EMAC.

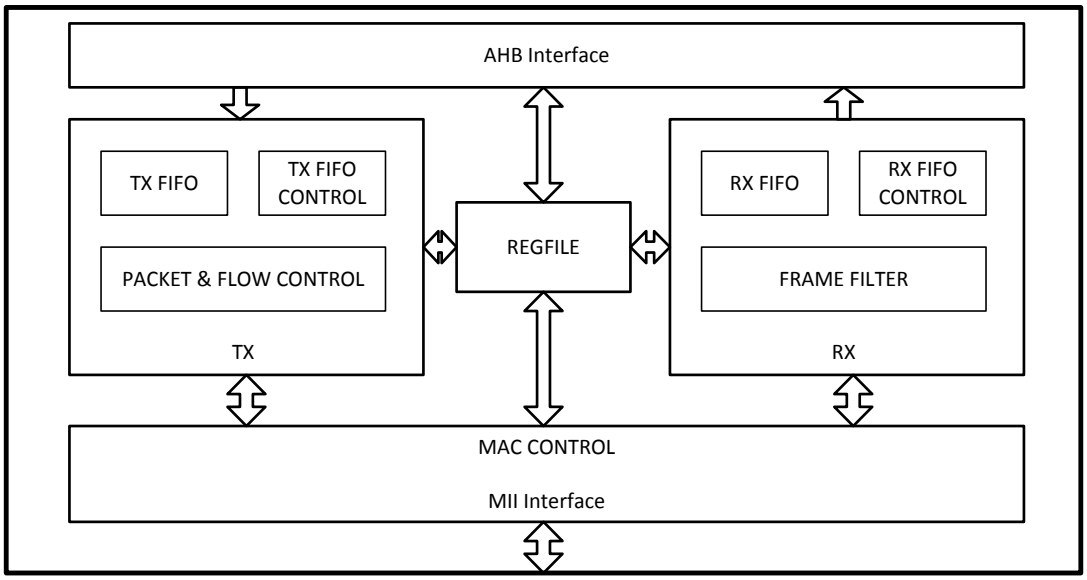


Figure 8-26. EMAC Block Diagram

8.10.3. Operations and Functional Descriptions

8.10.3.1. External Signals

Table 8-15 describes the pin list of EMAC.

Table 8-15. EMAC External Signals

Pin Name	Description	Type
ETXCK	MII Transmit Clock Input	I
ETXEN	MII Transmit Enable	O
ETXD[3:0]	MII Transmit Data	O
ETXERR	MII Transmit Error	O
ECRS	MII Carrier Sense	I
ECOL	MII Collision Detect	I
ERXCI	MII Receive Clock Input	I
ERXD[3:0]	MII Receive Data	I
ERXDV	MII Receive Data Valid	I
ERXERR	MII Receive Error	I
EMDC	MII Management Data Clock	O
EMDIO	MII Management Data Input/Output	I/O

8.10.3.2. Clock Requirement

EMAC module uses AHB bus clock, required AHB bus clock set between 25MHz and 220MHz.

8.10.3.3. EMAC Packet Header

Each received packet has 8-bytes header followed with data of the reception packet which CRC field isn't included. The format of the 8-byte header is 0x4d, 0x41, 0x43, 0x01, PKT_SIZE low and PKT_SIZE high status low, status high,. The received packet must be WORD(32-bit) aligned. If there is not enough data for WORD(32-bit) aligning. The zero byte is padded at the end of packet. The PKT_SIZE would count the size of useful data, not including padding bytes and 8-byte packet header.

Table 8-16 describes the 8-byte packet header.

Table 8-16. 8-Byte Packet Header

Index	Value	Description
BYTE0	PKT_VLD	Packet Valid Flag 0x01: packet valid 0x00: packet not valid
BYTE1	0x43	ASCII code 'C'
BYTE2	0x41	ASCII code 'A'
BYTE3	0x4d	ASCII code 'M'
BYTE4	PKT_STATUS	High byte of received packet's status
BYTE5	PKT_STATUS	Low byte of received packet's status
BYTE6	PKT_SIZE	High byte of packet size
BYTE7	PKT_SIZE	Low byte of packet size

Table 8-17 describes the 2-byte status.

Table 8-17. 2-Byte Status

Bit	Description
15	Reserved
14	Receive VLAN TYPE detected
13	Receive Unsupported Op-code
12	Receive Pause Control Frame
11	Receive Control Frame
10	Dribble Nibble
9	Broadcast Packet
8	Multicast Packet
7	Receive OK
6	Length Out of Range
5	Length Check Error
4	CRC Error
3	Receive Code Violation
2	Carrier Event Previously Seen
1	RXDV Event Previously Seen
0	Packet Previously Ignored

8.10.3.4. EMAC TX Operation

Figure 8-27 shows a block diagram of the TX Operation.

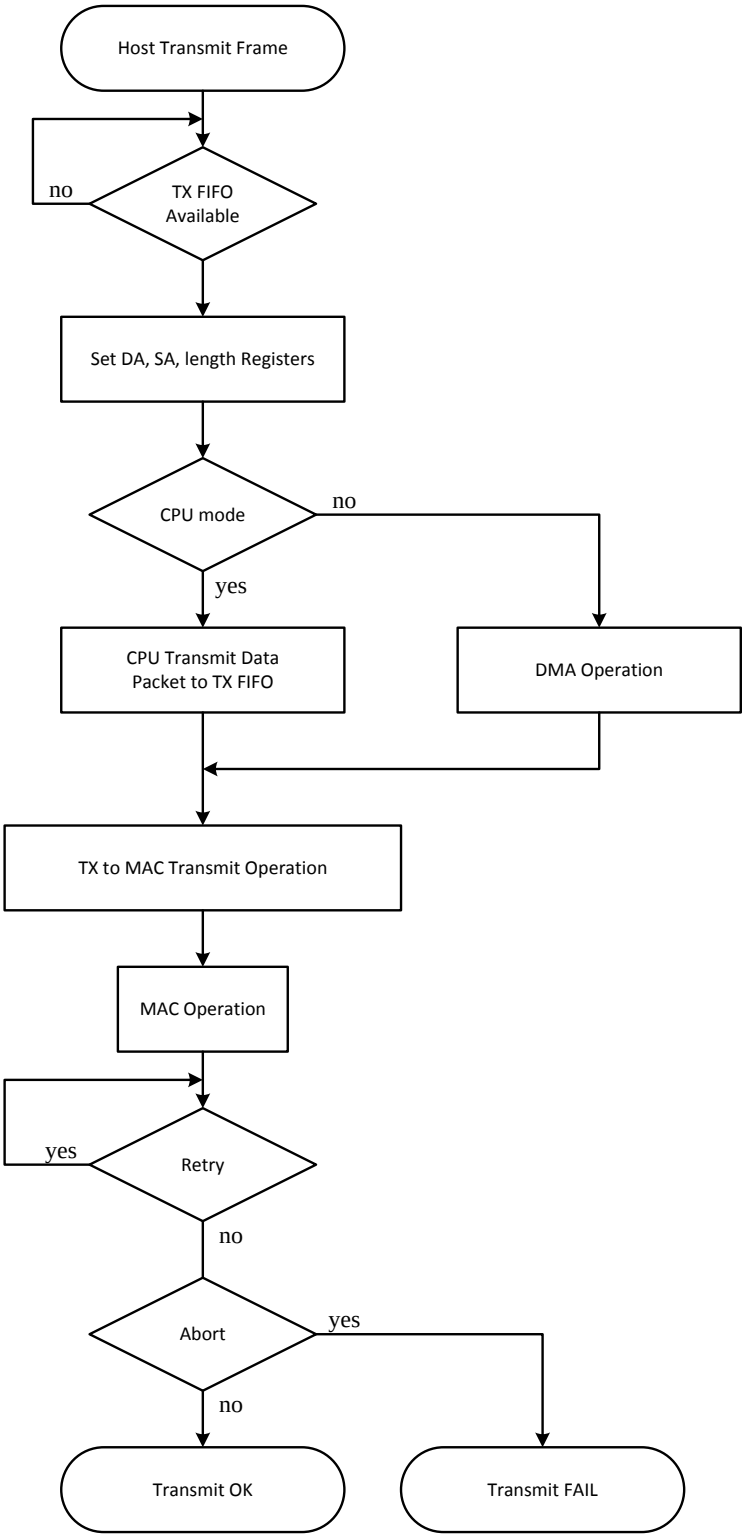


Figure 8-27. TX Operation Diagram

8.10.3.5. EMAC RX Operation

Figure 8-28 shows a block diagram of the RX Operation.

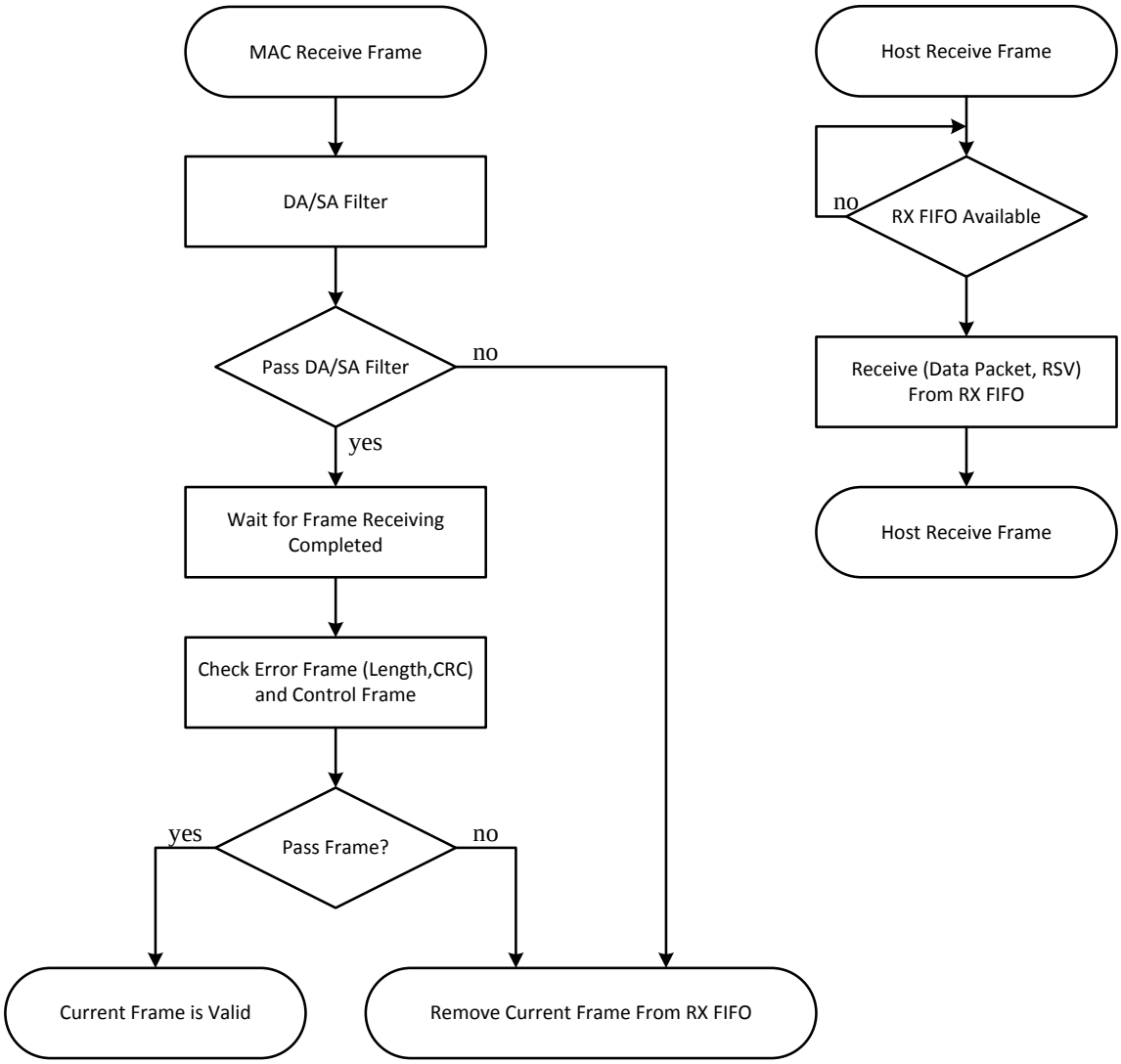


Figure 8-28. RX Operation Diagram

8.10.4. Register List

Module Name	Base Address
EMAC	0x01C0B000

Register Name	Offset	Description
EMAC_CTL	0x0000	EMAC Control Register
EMAC_TX_MODE	0x0004	EMAC TX Mode Register
EMAC_TX_FLOW	0x0008	EMAC TX Flow Control Register
EMAC_TX_CTL0	0x000C	EMAC TX Control Register0
EMAC_TX_CTL1	0x0010	EMAC TX Control Register1
EMAC_TX_INS	0x0014	EMAC TX Index Select Register
EMAC_TX_PL0	0x0018	EMAC TX Packet Length Register
EMAC_TX_PL1	0x001C	EMAC TX Packet Length Register
EMAC_TX_STA	0x0020	EMAC TX Status Register
EMAC_TX_IO_DATA0	0x0024	EMAC TX IO Data Register0
EMAC_TX_IO_DATA1	0x0028	EMAC TX IO Data Register1
EMAC_TX_TSVL0	0x002C	EMAC TX TSV Low Word Register0

Register Name	Offset	Description
EMAC_TX_TSVH0	0x0030	EMAC TX TSV High Word Register0
EMAC_TX_TSVL1	0x0034	EMAC TX TSV Low Word Register1
EMAC_TX_TSVH1	0x0038	EMAC TX TSV High Word Register1
EMAC_RX_CTL	0x003C	EMAC RX Control Register
EMAC_RX_HASH0	0x0040	EMAC RX Hash Table Register0
EMAC_RX_HASH1	0x0044	EMAC RX Hash Table Register1
EMAC_RX_STA	0x0048	EMAC RX Status Register
EMAC_RX_IO_DATA	0x004C	EMAC RX IO Data Register
EMAC_RX_FBC	0x0050	EMAC RX FIFO Byte Counter
EMAC_INT_CTL	0x0054	EMAC Interrupt Control Register
EMAC_INT_STA	0x0058	EMAC Interrupt Status Register
EMAC_MAC_CTL0	0x005C	EMAC MAC Control Register0
EMAC_MAC_CTL1	0x0060	EMAC MAC Control Register1
EMAC_MAC_IPGT	0x0064	EMAC MAC BTB Inter-Packet-Gap Register
EMAC_MAC_IPGR	0x0068	EMAC MAC NBTB Inter-Packet-Gap Register
EMAC_MAC_CLRT	0x006C	EMAC MAC Collision/ Retry Limit Register
EMAC_MAC_MAXF	0x0070	EMAC MAC Maximum Frame Register
EMAC_MAC_SUPP	0x0074	EMAC MAC PHY Support Register
EMAC_MAC_TEST	0x0078	EMAC MAC Test Register
EMAC_MAC_MCFG	0x007C	EMAC MAC MII Mgmt Configuration Register
EMAC_MAC_MCMD	0x0080	EMAC MAC MII Mgmt Command Register
EMAC_MAC_MADR	0x0084	EMAC MAC MII Mgmt Address Register
EMAC_MAC_MWTD	0x0088	EMAC MAC MII Mgmt Write Data Register
EMAC_MAC_MRDD	0x008C	EMAC MAC MII Mgmt Read Data Register
EMAC_MAC_MIND	0x0090	EMAC MAC MII Mgmt Indicators Register
EMAC_MAC_SSRR	0x0094	EMAC MAC SMII Status Register
EMAC_MAC_A0	0x0098	EMAC MAC Address Register0
EMAC_MAC_A1	0x009C	EMAC MAC Address Register1
EMAC_SAFX_A0	0x00A0+N*0x08(N=0~3)	EMAC SAFX Register0
EMAC_SAFX_A1	0x00A4+N*0x08(N=0~3)	EMAC SAFX Register1
EMAC_MDAF_A0	0x00C0+N*0x04(N=0~7)	EMAC MDAF Front Bytes Register
EMAC_MDAF_A1	0x00E0	EMAC MDAF Last Bytes Register

8.10.5. Register Description

8.10.5.1. EMAC Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: EMAC_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	EMAC_CRS EMAC Carrier Sense 0: Idle 1: Carrier lost
2	R/W	0x0	EMAC_RX_EN EMAC RX Enable 0: Disable 1: Enable
1	R/W	0x0	EMAC_TX_EN EMAC TX Enable

Offset: 0x0000			Register Name: EMAC_CTL
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable
0	R/W	0x0	EMAC_EN EMAC Enable Control 0: Disable 1: Enable

8.10.5.2. EMAC TX Mode Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: EMAC_TX_MODE
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	EMAC_TX_TM Transmit Mode Select 0: CPU mode 1: DMA mode
0	R/W	0x0	EMAC_TX_AB_M EMAC TX Aborted Packet Mode 0: Aborted frame auto clear 1: Aborted frame wait

8.10.5.3. EMAC TX Flow Control Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: EMAC_TX_FLOW
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:8	R/W	0x0	EMAC_TX_TPTV EMAC TX Transmit PAUSE Timer Value
7:2	/	/	/
1	R/W	0x0	EMAC_TX_THDF EMAC TX Transmit Half-Duplex Flow Control 0: Disable 1: Enable
0	R/W	0x0	EMAC_TX_TPCF EMAC TX Transmit PAUSE Control Frame **NOTE** **Write '1' to active pause control operation, auto clears after pause transmission completion.**

8.10.5.4. EMAC TX Control Register0(Default Value: 0x0000_0000)

Offset: 0x000C	Register Name: EMAC_TX_CTL0

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	EMAC_TX_PHUEN_0 EMAC TX Per-Packet Huge Enable 0: Disable 1: Enable Setting the bit to '1' will allow the transmission of a Huge Frame (over 1518 bytes) without truncating the current transmit frame.
6	R/W	0x0	EMAC_TX_CRC_EN_0 EMAC TX Per-Packet CRC Enable 0: Disable 1: Enable Setting the bit to '1' will append a correct CRC Value to the frame
5	R/W	0x0	EMAC_TX_PPADEN_0 EMAC TX Per-Packet Pad Enable 0: Disable 1: Enable Setting the bit to '1' will pad the current transmit frame to the IEEE minimum of 64 bytes and append a correct CRC Value to the frame
4	R/W	0x0	EMAC_TX_OVERR_0 EMAC TX Per-Packet Over Ride Enable 0: Disable 1: Enable When this bit is set to '1', the per-packet settings in this Register will override the current configuration settings In EMAC MAC Registers.
3:2	/	/	/
1	R/W	0x0	EMAC_TX_IN0_FTX EMAC TX Flush TX FIFO Index0 0: Disable 1: Enable Write '1' to Flush TX FIFO index0
0	R/W	0x0	EMAC_TX_IN0_REQ EMAC TX Index0 Transmit Request 0: Idle 1: Active **NOTE** **Auto clears after sending completely.**

8.10.5.5. EMAC TX Control Register1(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	EMAC_TX_PHUEN_1 EMAC TX Per-Packet Huge Enable 0: Disable

Offset: 0x0010			Register Name: EMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
			1: Enable Setting the bit to '1' will allow the transmission of a Huge Frame (over 1518 bytes) without truncating the current transmit frame.
6	R/W	0x0	EMAC_TX_CRC_EN_1 EMAC TX Per-Packet CRC Enable 0: Disable 1: Enable Setting the bit to '1' will append a correct CRC Value to the frame
5	R/W	0x0	EMAC_TX_PPADEN_1 EMAC TX Per-Packet Pad Enable 0: Disable 1: Enable Setting the bit to '1' will pad the current transmit frame to the IEEE minimum of 64 bytes and append a correct CRC Value to the frame
4	R/W	0x0	EMAC_TX_OVERR_1 EMAC TX Per-Packet Over Ride Enable 0: Disable 1: Enable When this bit is set to '1', the per-packet settings in this Register will override the current configuration settings In EMAC MAC Registers.
3:2	/	/	/
1	R/W	0x0	EMAC_TX_IN1_FTX EMAC TX Flush TX FIFO Index1 0: Disable 1: Enable Write '1' to Flush TX FIFO index1
0	R/W	0x0	EMAC_TX_IN1_REQ EMAC TX Index1 Transmit Request 0: Idle 1: Active **NOTE** **Auto clears after sending completely.**

8.10.5.6. EMAC TX Index Select Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: EMAC_TX_INS
Bit	**Read/Write**	**Default/Hex**	**Description**
31:1	/	/	/
0	R/W	0x0	EMAC_TX_INS EMAC TX Index Select 0: TX RAM0 1: TX RAM1

8.10.5.7. EMAC TX Package Length Register0(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: EMAC_TX_PL0
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	EMAC_TX_PA_LENTH_0 EMAC TX Packet Length for Index0

8.10.5.8. EMAC TX Package Length Register1(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: EMAC_TX_PL1
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	EMAC_TX_PA_LENTH_1 EMAC TX Packet Length for Index1

8.10.5.9. EMAC TX Status Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: EMAC_TX_STA
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	EMAC_TX_WAIT EMAC TX Waiting 0: Normal 1: TX is Waiting **NOTE** **Only active Aborted Frame Waiting Mode, Write '1' to clear this bit and wake up TX.**
7	R	0x0	EMAC_TX_INF EMAC TX Index Flag 0: Index0 is active 1: Index1 is active
6:0	/	/	/

8.10.5.10. EMAC TX IO Data Register0(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: EMAC_TX_IO_DATA0
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	EMAC_TX_IO_DATA Write data into internal RAM

8.10.5.11. EMAC TX IO Data Register1(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: EMAC_TX_IO_DATA1
Bit	Read/Write	Default/Hex	Description

Offset: 0x0028			Register Name: EMAC_TX_IO_DATA1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.10.5.12. EMAC TX TSVL Register0(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: EMAC_TX_TSVL0
Bit	Read/Write	Default/Hex	Description
31	R	0x0	EMAC_TX_UR Transmit under-run
30	R	0x0	EMAC_TX_GIANT Transmit Giant
29	R	0x0	EMAC_TX_LC Transmit Late Collisions
28	R	0x0	EMAC_TX_MC Transmit Maximum Collisions
27	R	0x0	EMAC_TX_ED Transmit Excessive Defer
26	R	0x0	EMAC_TX_PD Transmit Packet Defer
25	R	0x0	EMAC_TX_BC Transmit Broadcast
24	R	0x0	EMAC_TX_MC Transmit Multicast
23	R	0x0	EMAC_TX_DONE Transmit Done
22	R	0x0	EMAC_TX_LO Transmit Length Out of Range
21	R	0x0	EMAC_TX_LE Transmit Length Check Error
20	R	0x0	EMAC_TX_CRCE Transmit CRC Error
19:16	R	0x0	EMAC_TX_CCNT Transmit Collision Count
15:0	R	0x0	EMAC_TX_BCNT Transmit Byte Count

8.10.5.13. EMAC TX TSVH Register0(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: EMAC_TX_TSVH0
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R	0x0	EMAC_TX_VLAN Transmit VLAN Tagged frame
18	R	0x0	EMAC_TX_BA Backpressure Applied
17	R	0x0	EMAC_TX_PAUSE Transmit Pause Control Frame
16	R	0x0	EMAC_TX_CONTROL Transmit Control Frame
15:0	R	0x0	EMAC_TX_BOW

Offset: 0x0030			Register Name: EMAC_TX_TSVH0
Bit	Read/Write	Default/Hex	Description
			Total Bytes Transmitted on Wire

8.10.5.14. EMAC TX TSVL Register1(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: EMAC_TX_TSVL1
Bit	Read/Write	Default/Hex	Description
31	R	0x0	EMAC_TX_UR Transmit under-run
30	R	0x0	EMAC_TX_GIANT Transmit Giant
29	R	0x0	EMAC_TX_LC Transmit Late Collisions
28	R	0x0	EMAC_TX_MC Transmit Maximum Collisions
27	R	0x0	EMAC_TX_ED Transmit Excessive Defer
26	R	0x0	EMAC_TX_PD Transmit Packet Defer
25	R	0x0	EMAC_TX_BC Transmit Broadcast
24	R	0x0	EMAC_TX_MC Transmit Multicast
23	R	0x0	EMAC_TX_ED Transmit Done
22	R	0x0	EMAC_TX_LO Transmit Length Out of Range
21	R	0x0	EMAC_TX_LE Transmit Length Check Error
20	R	0x0	EMAC_TX_CRCE Transmit CRC Error
19:16	R	0x0	EMAC_TX_CCNT Transmit Collision Count
15:0	R	0x0	EMAC_TX_BCNT Transmit Byte Count

8.10.5.15. EMAC TX TSVH Register1(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: EMAC_TX_TSVH1
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R	0x0	EMAC_TX_VLAN Transmit VLAN Tagged Frame
18	R	0x0	EMAC_TX_BA Backpressure Applied
17	R	0x0	EMAC_TX_PAUSE Transmit Pause Control Frame
16	R	0x0	EMAC_TX_CONTROL Transmit Control Frame
15:0	R	0x0	EMAC_TX_BOW

Offset: 0x0038			Register Name: EMAC_TX_TSVH1
Bit	Read/Write	Default/Hex	Description
			Total Bytes Transmitted on Wire

8.10.5.16. EMAC RX Control Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: EMAC_RX_CTL
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25	R/W	0x0	EMAC_RX_SAIF EMC RX SA Inverse Filtering 0: Disable 1: Enable Active when EMAC_RX_SAF enable
24	R/W	0x0	EMAC_RX_SAF EMAC RX SA Filtering Enable 0: Disable 1: Enable
23	R/W	0x0	EMAC_RX_MDAF EMAC RX Multicast DA Filtering Enable 0: Disable 1: Eanble
22	R/W	0x0	EMAC_RX_BCO EMAC RX Broadcast Packet Accept 0: not accept 1: Accept Active when EMAC_RX_DAF enable
21	R/W	0x0	EMAC_RX_MHF EMAC RX Multicast Hash Filtering Enable 0: Disable 1: Enable Active when EMAC_RX_MCO enable
20	R/W	0x0	EMAC_RX_MCO EMAC RX Multicast Packet Accept 0: not accept 1: Accept
19:18	/	/	/
17	R/W	0x0	EMAC_RX_DAF EMC RX DA Filtering Enable 0: Disable 1: Enable Active when EMAC_RX_UCAD is set
16	R/W	0x0	EMAC_RX_UCAD EMAC RX Unicast Packet Accept 0: not accept 1: Accept

Offset: 0x003C			Register Name: EMAC_RX_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
15:11	/	/	/
10	R/W	0x0	EMAC_RX_PDB EMAC RX Pass packet with Dribble Nibble 0: Disable 1: Enable
9	R/W	0x0	EMAC_RX_PRCV EMAC RX Pass Packet with Receive Code Violation 0: Disable 1: Enable
8	R/W	0x0	EMAC_RX_PLO EMAC RX Pass Packet with Length Out of Range 0: Disable 1: Enable
7	R/W	0x0	EMAC_RX_PLE EMAC RX Pass Packet with Length Errors 0: Disable 1: Enable
6	R/W	0x0	EMAC_RX_PCRCE EMAC RX Pass Packet with CRC Errors 0: Disable 1: Enable
5	R/W	0x0	EMAC_RX_PCF EMAC RX Pass Control Frame 0: Disable 1: Enable
4	R/W	0x0	EMAC_RX_PA EMAC RX Pass All Enable 0: Disable 1: Enable **NOTE** **If this bit is set, all packets will be transmitted to the upper layer regardless of other settings.**
3	R/W	0x0	EMAC_RX_FRX EMAC RX FIFO Flush Write '1' to Flush RX FIFO
2	R/W	0x0	EMAC_RX_TM EMAC_RX Transmit Mode 0: CPU 1: DMA This bit is only valid in single frame mode.
1	R/W	0x0	EMAC_RX_DRQ_MODE EMAC RX DRQ Mode 0: DRQ always asserted 1: DRQ asserted automatically

Offset: 0x003C			Register Name: EMAC_RX_CTL
Bit	Read/Write	Default/Hex	Description
			Only valid in DMA Mode.
0	R/W	0x0	/

8.10.5.17. EMAC RX Hash Table Register0(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: EMAC_RX_HASH0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMAC_RX_HASH_L EMAC RX HASH Table Low 32bit The 64-bit Hash table is used for group address filtering. For hash filtering, the contents of the destination address in the incoming frame is passed through the CRC logic, and the upper 6 bits of the CRC register are used to index the contents of the Hash table. The most significant bit determines the register to be used (Hash Table 0/Hash Table 1), and the other 5 bits determine which bit within the register. A hash value of 5b'00000 selects bit 0 of the selected register, and a value of 5b'11111 selects bit 31 of the selected register.

8.10.5.18. EMAC RX Hash Table Register1(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: EMAC_RX_HASH1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	EMAC_RX_HASH_H EMAC RX HASH Table High 32bit The 64-bit Hash table is used for group address filtering. For hash filtering, the contents of the destination address in the incoming frame is passed through the CRC logic, and the upper 6 bits of the CRC register are used to index the contents of the Hash table. The most significant bit determines the register to be used (Hash Table 0/Hash Table 1), and the other 5 bits determine which bit within the register. A hash value of 5b'00000 selects bit 0 of the selected register, and a value of 5b'11111 selects bit 31 of the selected register.

8.10.5.19. EMAC RX Status Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: EMAC_RX_STA
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R	0x0	EMAC_RX_VLAN Receive VLAN TYPE Detected
29	R	0x0	EMAC_RX_UNSUP Receive Unsupported Op-code
28	R	0x0	EMAC_RX_PAUSE Receive Pause Control Frame
27	R	0x0	EMAC_RX_CONTROL Receive Control Frame

26	R	0x0	EMAC_RX_DN Dribble Nibble
25	R	0x0	EMAC_RX_BC Broadcast Packet
24	R	0x0	EMAC_RX_MC Multicast Packet
23	R	0x0	EMAC_RX_OK Receive OK
22	R	0x0	EMAC_RX_LO Length Out of Range
21	R	0x0	EMAC_RX_LE Length Check Error
20	R	0x0	EMAC_RX_CRCE CRC Error
19	R	0x0	EMAC_RX_CV Receive Code Violation
18	R	0x0	EMAC_RX_CE_PS Carrier Event Previously Seen
17	R	0x0	EMAC_RX_RXDVE_PS RXDV Event Previously Seen
16	R	0x0	EMAC_RX_PPI Packet Previously Ignored
15:0	R	0x0	EMAC_RX_BCNT Received Byte Count

8.10.5.20. EMAC RX IO Data Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: EMAC_RX_IO_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	EMAC_RX_IO_DATA Read data from internal ram

8.10.5.21. EMAC RX FIFO Byte Counter Register(Default Value: 0x0000_0000)

Offset: 0x0050			Register Name: EMAC_RX_FBC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:0	R	0x0	EMAC_RX_FIFO_BC EMAC RX FIFO Byte Counter

8.10.5.22. EMAC Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x0054			Register Name: EMAC_INT_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18	R/W	0x0	EMAC_CRL_INT EMAC Carrier Loss Interrupt 0: Disable 1: Enable

17	R/W	0x0	EMAC_RX_FCH_INT EMAC RX Flow Control High Level Interrupt 0: Disable 1: Enable If Enable, when free space less than 3K, the Interrupt will active.
16	R/W	0x0	EMAC_RX_FCL_INT EMAC RX Flow Control Low Level Interrupt 0: Disable 1: Enable If Enable, when free space less than 8K, the Interrupt will active.
15:10	/	/	/
9	R/W	0x0	EMAC_RX _OR_INT EMAC RX Overrun Interrupt Enable 0: Disable 1: Enable
8	R/W	0x0	EMAC_RX_RCE_INT EMAC RX Received Interrupt Enable 0: Disable 1: Enable
7:4	/	/	/
3	R/W	0x0	EMAC_TX_IN1_AB_INT EMAC TX FIFO Index1 Aborted Interrupt Enable 0: Disable 1: Enable
2	R/W	0x0	EMAC_TX_IN0_AB_INT EMAC TX FIFO Index0 Aborted Interrupt Enable 0: Disable 1: Enable
1	R/W	0x0	EMAC_TX_IN1_TC_INT EMAC TX FIFO Index1 Transmit Completed Interrupt Enable 0: Disable 1: Enable
0	R/W	0x0	EMAC_TX_IN0_TC_INT EMAC TX FIFO Index0 Transmit Completed Interrupt Enable 0: Disable 1: Enable

8.10.5.23. EMAC Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0058			**Register Name: EMAC_INT_STA**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/

18	R/W1C	0x0	EMAC_CRL_P EMAC Carrier Loss Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
17	R/W1C	0x0	EMAC_RX_FCH_P EMAC RX Flow Control High Level Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
16	R/W1C	0x0	EMAC_RX_FCL_P EMAC RX Flow Control Low Level Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
15:10	/	/	/
9	R/W1C	0x0	EMAC_RX _OR_P EMAC RX Overrun Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
8	R/W1C	0x0	EMAC_RX_RCE_P EMAC RX Received Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
7:4	/	/	/
3	R/W1C	0x0	EMAC_TX_IN1_AB_P EMAC TX FIFO Index1 Aborted Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
2	R/W1C	0x0	EMAC_TX_IN0_AB_P EMAC TX FIFO Index0 Aborted Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
1	R/W1C	0x0	EMAC_TX_IN1_TC_P EMAC TX FIFO Index1 Transmit Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
0	R/W1C	0x0	EMAC_TX_IN0_TC_P EMAC TX FIFO Index0 Transmit Completed Interrupt Pending 0: No Pending 1: Pending Write '1' to clear

8.10.5.24. EMAC MAC Control Register0(Default Value: 0x0000_8000)

Offset: 0x005C			Register Name: EMAC_MAC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x1	EMAC_MAC_SF EMAC MAC Soft Reset 0: Disable 1: Enable
14	R/W	0x0	EMAC_MAC_SIR EMAC MAC Simulation Reset 0: Disable 1: Enable
13:12	/	/	/
11	R/W	0x0	EMAC_MAC_RRX EMAC MAC Reset RX Logic 0: Disable 1: Enable
10	R/W	0x0	EMAC_MAC_RPT EMAC MAC Reset PERFUN 0: Disable 1: Enable
9	R/W	0x0	EMAC_MAC_RTX EMA MAC Reset TX logic 0: Disable 1: Enable
8	R/W	0x0	EMAC_MAC_RPT EMAC MAC Reset PETFUN 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	EMAC_MAC_LP EMAC MAC LOOPBACK 0: Disable 1: Enable
3	R/W	0x0	EMAC_MAC_TFC EMAC MAC Transmit Flow Control 0: Disable 1: Enable When enabled, PAUSE Flow Control frames are allowed to be transmitted

2	R/W	0x0	EMAC_MAC_RFC EMAC MAC Receive Flow Control 0: Disable 1: Enable When enabled, the MAC acts upon received PAUSE Flow Control frames
1	R/W	0x0	EMAC_MAC_PC EMA MAC Pass Control frames 0: Disable 1: Enable
0	R/W	0x0	EMAC_MAC_REN EMAC MAC Receive Enable 0: Disable 1: Enable

8.10.5.25. EMAC MAC Control Register1(Default Value: 0x0000_8000)

Offset: 0x0060			Register Name: EMAC_MAC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R/W	0x0	EMAC_MAC_ED EMAC MAC Excess Defer 0: Disable 1: Enable
13	R/W	0x0	EMAC_MAC_BP EMAC MAC Backpressure/no back off 0: Disable 1: Enable
12	R/W	0x0	EMAC_MAC_NB EMAC MAC No Back off 0: Disable 1: Enable
11:10	/	/	/
9	R/W	0x0	EMAC_MAC_LP EMAC MAC Long Preamble Enforcement Enable 0: Disable 1: Enable
8	R/W	0x0	EMAC_MAC_PP EMAC MAC Pure Preamble Enforcement Enable 0: Disable 1: Enable
7	R/W	0x0	EMAC_MAC_ADP EMAC MAC Auto Detect Pad Enable 0: Disable 1: Enable

6	R/W	0x0	EMAC_MAC_VLAN_PAD EMAC MAC VLAN PAD Enable 0: Disable 1: Enable
5	R/W	0x0	EMAC_MAC_PC EMAC MAC PAD/CRC Enable 0: Disable 1: Enable
4	R/W	0x0	EMAC_MAC_CRC EMAC MAC CRC Enable 0: Disable 1: Enable
3	R/W	0x0	EMAC_MAC_DCRC EMAC MAC Delayed CRC 0: Disable 1: Enable
2	R/W	0x0	EMAC_MAC_HF EMAC MAC Huge Frame Enable 0: Disable 1: Enable
1	R/W	0x0	EMAC_MAC_FLC EMAC MAC Frame Length Checking 0: Disable 1: Enable
0	R/W	0x0	EMAC_MAC_FULL EMAC MAC Full duplex 0: Half duplex 1: Full duplex

8.10.5.26. EMAC MAC BTB Inter-Packet-Gap Register(Default Value: 0x0000_0000)

Offset: 0x0064			Register Name: EMAC_MAC_IPGT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:7	/	/	/
6:0	R/W	0x0	EMAC_MAC_IPGT EMAC MAC Back to Back Inter Packet Gap

8.10.5.27. EMAC MAC NBTB Inter-Packet-Gap Register(Default Value: 0x0000_0000)

Offset: 0x0068			Register Name: EMAC_MAC_IPGR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14:8	R/W	0x0	EMAC_MAC_IPGR1 EMAC MAC Non Back to Back Inter Packet Gap Part1
7	/	/	/

6:0	R/W	0x0	EMAC_MAC_IPGR2 EMAC MAC Non Back to Back Inter Packet Gap Part2

8.10.5.28. EMAC MAC Collision/ Retry Limit Register(Default Value: 0x0000_370F)

Offset: 0x006C			Register Name: EMAC_MAC_CLRT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13:8	R/W	0x37	EMAC_MAC_CW EMAC MAC Collision Window
7:4	/	/	/
3:0	R/W	0xF	EMAC_MAC_REMX EMAC MAC Retransmission Maximum

8.10.5.29. EMAC MAC Maximum Frame Register(Default Value: 0x0000_0600)

Offset: 0x0070			Register Name: EMAC_MAC_MAXF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0600	EMAC_MAC_MAXF EMAC MAC Maximum Frame Length

8.10.5.30. EMAC MAC PHY Support Register(Default Value: 0x0000_1000)

Offset: 0x0074			Register Name: EMAC_MAC_SUPP
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15	R/W	0x0	EMAC_MAC_RIM EMAC MAC Reset Interface Module 0: Disable 1: Enable
14:13	/	/	/
12	R/W	0x1	EMAC_MAC_PHYM EMAC MAC PHY Mode 0: SMII MAC 1: SMII PHY
11	R/W	0x0	EMAC_MAC_RRMII EMAC MAC Reset RMII 0: Disable 1: Enable
10:9	/	/	/
8	R/W	0x0	EMAC_MAC_SPEED EMAC MAC Speed 0: 10M 1: 100M

7	R/W	0x0	EMAC_MAC_RPET100X EMAC MAC Reset PET100X 0: Disable 1: Enable
6	R/W	0x0	EMAC_MAC_FQ EMAC MAC Force Quiet 0: Disable 1: Enable
5	R/W	0x0	EMAC_MAC_NC EMAC MAC No Cipher 0: Disable 1: Enable
4	R/W	0x0	EMAC_MAC_DLF EMAC MAC Disable Link Fail 0: Disable 1: Enable
3	R/W	0x0	EMAC_MAC_RPET10 EMAC MAC Reset PET10 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	EMAC_MAC_JP EMAC MAC Jabber Protection Enable 0: Disable 1: Enable
0	R/W	0x0	EMAC_MAC_BM EMAC MAC Bit Mode 0: nibble clock 1: bit clock

8.10.5.31. EMAC MAC Test Register(Default Value: 0x0000_0000)

Offset: 0x0078			Register Name: EMAC_MAC_TEST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	EMAC_MAC_TB EMAC MAC Test backpressure
1	R/W	0x0	EMAC_MAC_TP EMAC MAC Test Pause
0	R/W	0x0	EMAC_MAC_SPQ EMAC MAC Shortcut Pause Quanta

8.10.5.32. EMAC MAC MII Mgmt Configuration Register(Default Value: 0x0000_0000)

Offset: 0x007C	Register Name: EMAC_MAC_MCFG

Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	R/W	0x0	EMAC_MAC_MII_RST EMAC MAC MII Reset 0: Disable 1: Enable
14:6	/	/	/
5:2	R/W	0x0	EMAC_MAC_MII_CLKD EMAC MAC MII Clock Divider 0000: 4 0001: 4 0010: 6 0011: 8 0100: 10 0101: 14 0110: 20 0111: 28 1000: 32 1001: 40 1010: 48 1011: 56 1100: 64 1101: 72 1110: 80 1111: 88
1	R/W	0x0	EMAC_MAC_MII_SP EMAC MAC MII Suppress Preamble
0	R/W	0x0	EMAC_MAC_MII_SI EMAC MAC MII Scan Increment

8.10.5.33. EMAC MAC MII Mgmt Command Register(Default Value: 0x0000_0000)

Offset: 0x0080			Register Name: EMAC_MAC_MCMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	EMAC_MAC_MII_SCAN EMAC MAC MII Scan
0	R/W	0x0	EMAC_MAC_MII_READ EMAC MAC MII Read This bit causes the MII interface to perform a single read cycle. The read data is returned in register EMAC_MAC_MRDD.

8.10.5.34. EMAC MAC MII Mgmt Address Register(Default Value: 0x0000_0000)

Offset: 0x0084			Register Name: EMAC_MAC_MADR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:13	/	/	/
12:8	R/W	0x0	EMAC_MAC_MII_PA EMAC MAC MII PHY Address

7:5	/	/	/
4:0	R/W	0x0	EMAC_MAC_MII_RA EMAC MAC MII Register Address

8.10.5.35. EMAC MAC MII Mgmt Write Data Register(Default Value: 0x0000_0000)

Offset: 0x0088			Register Name: EMAC_MAC_MWTD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	W	0x0	EMAC_MAC_MII_WD EMAC MAC MII Write Data When written, a MII interface write cycle is performed using 16-bit data and the pre-configured PHY and Register address in EMAC_MAC_MADR.

8.10.5.36. EMAC MAC MII Mgmt Read Data Register(Default Value: 0x0000_0000)

Offset: 0x008C			Register Name: EMAC_MAC_MRDD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R	0x0	EMAC_MAC_MII_RD EMAC MAC MII Read Data

8.10.5.37. EMAC MAC MII Mgmt Indicators Register(Default Value: 0x0000_0000)

Offset: 0x0090			Register Name: EMAC_MAC_MIND
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	EMAC_MAC_MII_LF EMAC MAC MII Link Fail
2	R	0x0	EMAC_MAC_MII_N EMAC MAC MII Not Valid
1	R	0x0	EMAC_MAC_MII_S EMAC MAC MII Scanning
0	R	0x0	EMAC_MAC_MII_B EMAC MAC MII Busy

8.10.5.38. EMAC MAC SMII Status Register(Default Value: 0x0000_0000)

Offset: 0x0094			Register Name: EMAC_MAC_SSRR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:5	/	/	/
4	R	0x0	EMAC_MAC_SMII_C EMAC MAC SMII Clash
3	R	0x0	EMAC_MAC_SMII_J EMAC MAC SMII Jabber

2	R	0x0	EMAC_MAC_SMII_L EMAC MAC SMII Link 0: fail 1: ok
1	R	0x0	EMAC_MAC_SMII_D EMAC MAC SMII Duplex 0: Half Duplex 1: Full Duplex
0	R	0x0	EMAC_MAC_SMII_S EMAC MAC SMII Speed 0: 10M 1: 100M

8.10.5.39. EMAC MAC Address Register0(Default Value: 0x0000_0000)

Offset: 0x0098			Register Name: EMAC_MAC_A0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	W	0x0	EMAC_MAC_ADR_B2 EMAC MAC Address Byte2
15:8	W	0x0	EMAC_MAC_ADR_B1 EMAC MAC Address Byte1
7:0	W	0x0	EMAC_MAC_ADR_B0 EMAC MAC Address Byte0

8.10.5.40. EMAC MAC Address Register1(Default Value: 0x0000_0000)

Offset: 0x009C			Register Name: EMAC_MAC_A1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	W	0x0	EMAC_MAC_ADR_B5 EMAC MAC Address Byte5
15:8	W	0x0	EMAC_MAC_ADR_B4 EMAC MAC Address Byte4
7:0	W	0x0	EMAC_MAC_ADR_B3 EMAC MAC Address Byte3

NOTE

B5 is the first Address Byte in Erthnet Packet, and B0 is the last.

8.10.5.41. EMAC SAFX Register0(Default Value: 0x0000_0000)

Offset: 0x00A0+N*0x08(N=0~3)			Register Name: EMAC_SAX_A0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	W	0x0	EMAC_SAX_ADR_B2 EMAC SA Filtering Address Byte2

15:8	W	0x0	EMAC_SAX_ADR_B1 EMAC SA Filtering Address Byte1
7:0	W	0x0	EMAC_SAX_ADR_B0 EMAC SA Filtering Address Byte0

8.10.5.42. EMAC SAFX Register1(Default Value: 0x0000_0000)

Offset: 0x00A4+N*0x08(N=0~3)			Register Name: EMAC_SAX_A1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	W	0x0	EMAC_SAX_ADR_B5 EMAC SA Filtering Address Byte5
15:8	W	0x0	EMAC_SAX_ADR_B4 EMAC SA Filtering Address Byte4
7:0	W	0x0	EMAC_SAX_ADR_B3 EMAC SA Filtering Address Byte3

8.10.5.43. EMAC MDAFX Register0(Default Value: 0x0000_0000)

Offset: 0x00C0+N*0x04(N=0~7)			Register Name: EMAC_MDAFX_A0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	EMAC_MDA_B2 EMAC Multicast DA filtering Address Byte2
16:8	R/W	0x0	EMAC_MDA_B1 EMAC Multicast DA filtering Address Byte1
7:0	R/W	0x0	EMAC_MDA_B0 EMAC Multicast DA filtering Address Byte0

8.10.5.44. EMAC MDAFX Register1(Default Value: 0x0000_0000)

Offset: 0x00E0			Register Name: EMAC_MDAFX_A1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	EMAC_MDA_B5 EMAC Multicast DA filtering Address Byte5
16:8	R/W	0x0	EMAC_MDA_B4 EMAC Multicast DA filtering Address Byte4
7:0	R/W	0x0	EMAC_MDA_B3 EMAC Multicast DA filtering Address Byte3

NOTE

8 EMAC_MDAFX_Register0 and 1 EMAC_MDAFX_Register1 for Multicast DA Filtering.

8.11. GMAC

8.11.1. Overview

The GMAC controller enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M/1000M external PHY with RGMII interface in both full and half duplex mode.

The internal DMA is designed for packet-oriented data transfer based on a linked list of descriptors. 4KB TXFIFO and 16KB RXFIFO are provided to keep continuous transmission and reception. Flow Control, CRC Pad & Stripping, and address filtering are supported in this module as well.

Features:

- Supports 10/100/1000Mbps data transfer rate
- Supports MII/RGMII PHY interface
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4KB data
- Comprehensive status report for normal operation and transfers with errors
- 4KB TXFIFO for transmission packets and 16KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

8.11.2. Block Diagram

Figure 8-29 shows a block diagram of the GMAC.

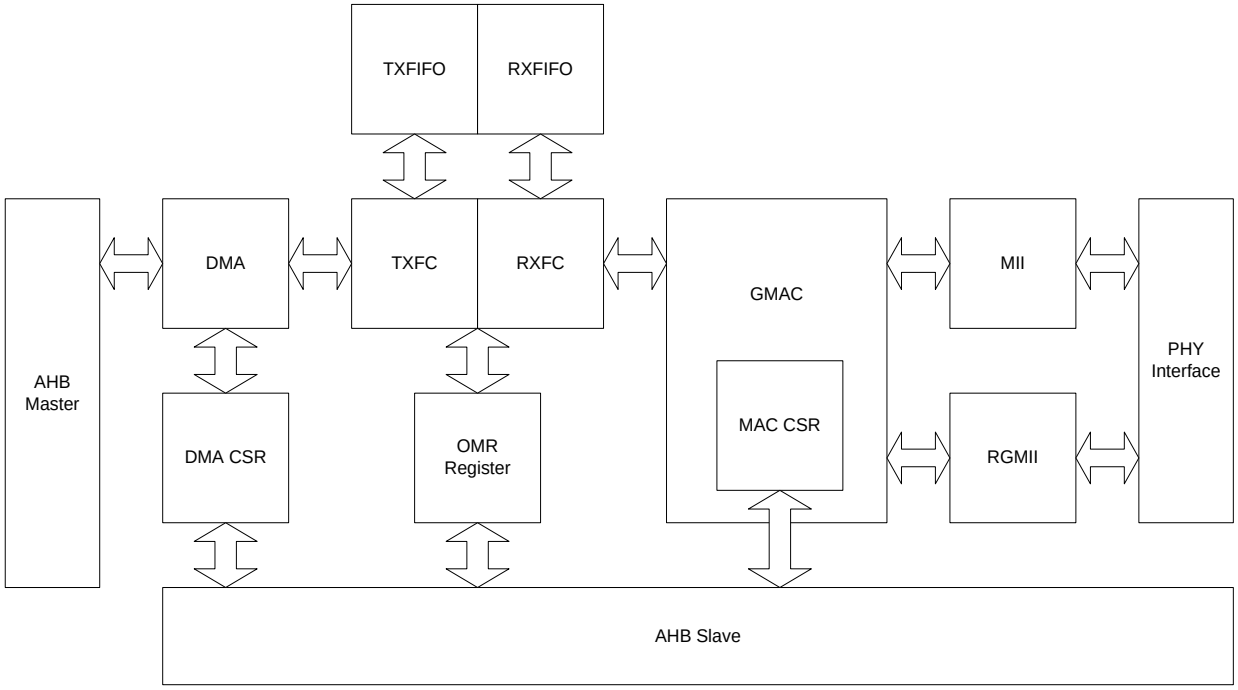


Figure 8-29. GMAC Block Diagram

8.11.3. Operations and Functional Descriptions

8.11.3.1. External Signals

Table 8-18 describes the external signals of GMAC.

Table 8-18. GMAC External Signals

Pin Name	Description	Type
GTXD[3:0]	RGMII/MII Transmit Data	O
GTXCTL/ETXEN	RGMII Transmit Control/MII Transmit Enable	O,O
GNULL/ETXCK	RGMII Null/MII Transmit Clock	I
GTXCK/ECRS	RGMII Transmit Clock/MII Carrier Sense	O,I
GNULL/ETXERR	RGMII Null/ MII Transmit Error	O
GRXD[3:0]	RGMII/MII Receive Data	I
GRXCTL/RXDV	RGMII Receive Control/MII Receive Data Valid	I,I
GRXCK	RGMII/MII Receive Error	I
GNULL/ERXERR	RGMII Null/ MII Receive Error	I
GMDC	RGMII/MII Management Data Clock	I
GMDIO	RGMII/MII Management Data Input Output	I/O
GCKIN/ECOL	RGMII 125M Reference Clock Input/MII Collision Detect	I,I

8.11.3.2. Clock Requirement

Table 8-19 describes the clock of GMAC.

Table 8-19. GMAC Clock Requirement

Clock Name	Description
GTXCK/ETXCK	In RGMII mode, output 2.5MHz/25MHz/125MHz. In MII mode, input 2.5MHz/25MHz

GRXCK	In RGMII mode, input 2.5MHz/25MHz/125MHz. In MII mode, input 2.5MHz/25MHz.
GCKIN	Input 125M Reference Clock

8.11.3.3. GMAC RX/TX Descriptor

The internal DMA of GMAC transfers data between host memory and internal RX/TX FIFO with a linked list of descriptors. Each descriptor is consisted of four words, and contains some necessary information to transfer TX and RX frames. The descriptor list structure is shown in Figure 8-30. The address of each descriptor must be 32-bit aligned.

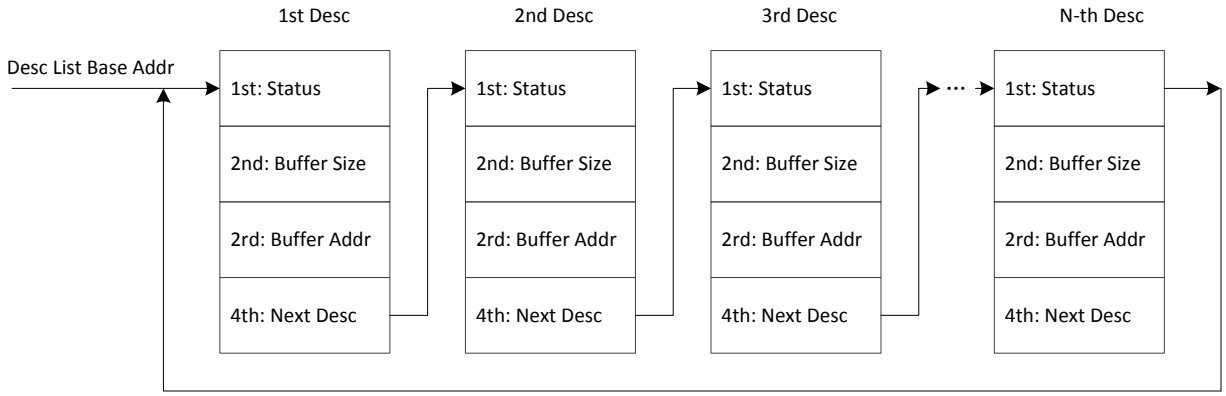


Figure 8-30. RX/TX Descriptor List

8.11.3.4. GMAC Transmit Descriptor

(1) 1st Word of Transmit Descriptor

Bits	Description
31	TX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when the whole frame is transmitted or all data in current descriptor's buffer are transmitted.
30:17	Reserved
16	TX_HEADER_ERR When set, the checksum of transmitted frame's header is wrong.
15	Reserved
14	TX_LENGHT_ERR When set, the length of transmitted frame is wrong.
13	Reserved
12	TX_PAYLOAD_ERR When set, the checksum of transmitted frame's payload is wrong.
11	Reserved
10	TX_CRS_ERR When set, carrier is lost during transmission.
9	TX_COL_ERR_0 When set, the frame is aborted because of collision after contention period.
8	TX_COL_ERR_1 When set, the frame is aborted because of too many collisions.
7	Reserved.
6:3	TX_COL_CNT The number of collisions before transmission.
2	TX_DEFER_ERR When set, the frame is aborted because of too much deferral.

1	TX_UNDERFLOW_ERR When set, the frame is aborted because of TX FIFO underflow error.
0	TX_DEFER When set in Half-Duplex mode, the GMAC defers the frame transmission.

(2) 2nd Word of Transmit Descriptor

Bits	Description
31	TX_INT_CTL When set and the current frame have been transmitted, the TX_INT in Interrupt Status Register will be set.
30	LAST_DESC When set, current descriptor is the last one for current frame.
29	FIR_DESC When set, current descriptor is the first one for current frame.
28:27	CHECKSUM_CTL These bits control to insert checksums in transmit frame.
26	CRC_CTL When set, CRC field is not transmitted.
25:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

(3) 3rd Word of Transmit Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

(4) 4th Word of Transmit Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. It must be 32-bit aligned.

8.11.3.5. GMAC Receive Descriptor

(1) 1st Word of Receive Descriptor

Bits	Description
31	RX_DESC_CTL When set, current descriptor can be used by DMA. This bit is cleared by DMA when complete frame is received or current descriptor's buffer is full.
30	RX_DAF_FAIL When set, current frame don't pass DA filter.
29:16	RX_FRM_LEN When LAST_DESC is not set and no error bit is set, this field is the length of received data for current frame. When LAST_DESC is set, RX_OVERFLOW_ERR and RX_NO_ENOUGH_BUF_ERR are not set, this field is the length of receive frame.
15	Reserved

14	RX_NO_ENOUGH_BUF_ERR When set, current frame is clipped because of no enough buffer.
13	RX_SAF_FAIL When set, current fame don't pass SA filter.
12	Reserved.
11	RX_OVERFLOW_ERR When set, a buffer overflow error occurred and current frame is wrong.
10	Reserved
9	FIR_DESC When set, current descriptor is the first descriptor for current frame.
8	LAST_DESC When set, current descriptor is the last descriptor for current frame.
7	RX_HEADER_ERR When set, the checksum of frame's header is wrong.
6	RX_COL_ERR When set, there is a late collision during reception in half-duplex mode.
5	Reserved.
4	RX_LENGTH_ERR When set, the length of current frame is wrong.
3	RX_PHY_ERR When set, the receive error signal from PHY is asserted during reception.
2	Reserved.
1	RX_CRC_ERR When set, the CRC filed of received frame is wrong.
0	RX_PAYLOAD_ERR When set, the checksum or length of received frame's payload is wrong.

(2) 2nd Word of Receive Descriptor

Bits	Description
31	RX_INT_CTL When set and a frame have been received, the RX_INT will not be set.
30:11	Reserved
10:0	BUF_SIZE The size of buffer specified by current descriptor.

(3) 3rd Word of Receive Descriptor

Bits	Description
31:0	BUF_ADDR The address of buffer specified by current descriptor.

(4) 4th Word of Receive Descriptor

Bits	Description
31:0	NEXT_DESC_ADDR The address of next descriptor. This field must be 32-bit aligned.

8.11.4. Register List

Module Name	Base Address
GMAC	0x01C50000

Register Name	Offset	Description
GMAC_BASIC_CTL0	0x0000	GMAC Basic Control Register0
GMAC_BASIC_CTL1	0x0004	GMAC Basic Control Register1
GMAC_INT_STA	0x0008	GMAC Interrupt Status Register
GMAC_INT_EN	0x000C	GMAC Interrupt Enable Register
GMAC_TX_CTL0	0x0010	GMAC Transmit Control Register0
GMAC_TX_CTL1	0x0014	GMAC Transmit Control Register1
GMAC_TX_FLOW_CTL	0x001C	GMAC Transmit Flow Control Register
GMAC_TX_DMA_DESC_LIST	0x0020	GMAC Transmit Descriptor List Address Register
GMAC_RX_CTL0	0x0024	GMAC Receive Control Register0
GMAC_RX_CTL1	0x0028	GMAC Receive Control Register1
GMAC_RX_DMA_DESC_LIST	0x0034	GMAC Receive Descriptor List Address Register
GMAC_RX_FRM_FLT	0x0038	GMAC Receive Frame Filter Register
GMAC_RX_HASH0	0x0040	GMAC Hash Table Register0
GMAC_RX_HASH1	0x0044	GMAC Hash Table Register1
GMAC_MII_CMD	0x0048	GMAC Management Interface Command Register
GMAC_MII_DATA	0x004C	GMAC Management Interface Data Register
GMAC_ADDR_HIGH0	0x0050	GMAC MAC Address High Register0
GMAC_ADDR_LOW0	0x0054	GMAC MAC Address High Register0
GMAC_ADDR_HIGHx	0x0050+N*0x08(N=1~7)	GMAC MAC Address High RegisterN(N:1~7)
GMAC_ADDR_LOWx	0x0054+N*0x08(N=1~7)	GMAC MAC Address Low RegisterN(N:1~7)
GMAC_TX_DMA_STA	0x00B0	GMAC Transmit DMA Status Register
GMAC_TX_CUR_DESC	0x00B4	GMAC Current Transmit Descriptor Register
GMAC_TX_CUR_BUF	0x00B8	GMAC Current Transmit Buffer Address Register
GMAC_RX_DMA_STA	0x00C0	GMAC Receive DMA Status Register
GMAC_RX_CUR_DESC	0x00C4	GMAC Current Receive Descriptor Register
GMAC_RX_CUR_BUF	0x00C8	GMAC Current Receive Buffer Address Register
GMAC_RGMII_STA	0x00D0	GMAC RGMII Status Register

8.11.5. Register Description

8.11.5.1. GMAC Basic Control Register0(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: GMAC_BASIC_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3:2	R/W	0x0	SPEED 00: 1000Mbps 01: Reserved 10: 10Mbps 11: 100Mbps
1	R/W	0x0	LOOPBACK 0: Disable 1: Enable

0	R/W	0x0	DUPLEX 0: Half-duplex 1: Full-duplex

8.11.5.2. GMAC Basic Control Register1(Default Value: 0x0800_0000)

Offset: 0x0004			Register Name: GMAC_BASIC_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:30	/	/	/
29:24	R/W	0x8	BURST_LEN The burst length of RX and TX DMA transfer.
23:2	/	/	/
1	R/W	0x0	RX_TX_PRI RX TX DMA priority 0: same priority 1: RX priority over TX
0	R/W	0x0	SOFT_RST Soft Reset all Registers and Logic 0: No valid 1: Reset **NOTE** **All clock inputs must be valid before soft rest. This bit is cleared internally when the reset operation is completed fully. Before write any register, this bit should read a 0.**

8.11.5.3. GMAC Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: GMAC_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W1C	0x0	RGMII_LINK_STA_P RMII Link Status Changed Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
15:14	/	/	/
13	R/W1C	0x0	RX_EARLY_P RX DMA Filled First data Buffer of the Receive Frame Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear

12	R/W1C	0x0	RX_OVERFLOW_P RX FIFO Overflow Error Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
11	R/W1C	0x0	RX_TIMEOUT_P RX Timeout Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear .When this bit asserted, the length of receive frame is greater than 2048 bytes(10240 when JUMBO_FRM_EN is set)
10	R/W1C	0x0	RX_DMA_STOPPED_P When this bit asserted, the RX DMA FSM is stopped.
9	R/W1C	0x0	RX_BUF_UA _P RX Buffer UA Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear .When this asserted, the RX DMA can’t acquire next RX descriptor and RX DMA FSM is suspended. The ownership of next RX descriptor should be changed to RX DMA. The RX DMA FSM will resume when write to DMA_RX_START bit or next receive frame is coming.
8	R/W1C	0x0	RX_P Frame RX Completed Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear. When this bit is asserted, a frame reception is completed. The RX DMA FSM remains in the running state.
7:6	/	/	/
5	R/W1C	0x0	TX_EARLY_P Frame is transmitted to FIFO totally Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear.
4	R/W1C	0x0	TX_UNDERFLOW_P TX FIFO Underflow Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear
3	R/W1C	0x0	TX_TIMEOUT_P Transmitter Timeout Interrupt Pending 0: No Pending 1: Pending Write ‘1’ to clear

2	R/W1C	0x0	TX_BUF_UA_P TX Buffer UA Interrupt Pending 0: No Pending 1: Pending When this asserted, the TX DMA can not acquire next TX descriptor and TX DMA FSM is suspended. The ownership of next TX descriptor should be changed to TX DMA. The TX DMA FSM will resume when write to DMA_TX_START bit.
1	R/W1C	0x0	TX_DMA_STOPPED_P Transmission DMA Stopped Interrupt Pending 0: No Pending 1: Pending Write '1' to clear
0	R/W1C	0x0	TX_P Frame Transmission Interrupt Pending 0: No Pending 1: Pending Write '1' to clear

8.11.5.4. GMAC Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x000C			**Register Name: GMAC_INT_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
31:14	/	/	/
13	R/W	0x0	RX_EARLY_INT_EN Early Receive Interrupt 0: Disable 1: Enable
12	R/W	0x0	RX_OVERFLOW_INT_EN Receive Overflow Interrupt 0: Disable 1: Enable
11	R/W	0x0	RX_TIMEOUT_INT_EN Receive Timeout Interrupt 0: Disable 1: Enable
10	R/W	0x0	RX_DMA_STOPPED_INT_EN Receive DMA FSM Stopped Interrupt 0: Disable 1: Enable
9	R/W	0x0	RX_BUF_UA_INT_EN Receive Buffer Unavailable Interrupt 0: Disable 1: Enable

8	R/W	0x0	RX_INT_EN Receive interrupt 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	TX_EARLY_INT_EN Early Transmit Interrupt 0: Disable 1: Enable
4	R/W	0x0	TX_UNDERFLOW_INT_EN Transmit Underflow Interrupt 0: Disable 1: Enable
3	R/W	0x0	TX_TIMEOUT_INT_EN Transmit Timeout Interrupt 0: Disable 1: Enable
2	R/W	0x0	TX_BUF_UA_INT_EN Transmit Buffer Available Interrupt 0: Disable 1: Enable
1	R/W	0x0	TX_DMA_STOPPED_INT_EN Transmit DMA FSM Stopped Interrupt 0: Disable 1: Enable
0	R/W	0x0	TX_INT_EN Transmit interrupt 0: Disable 1: Enable

8.11.5.5. GMAC Transmit Control Register0(Default Value: 0x0000_0000)

Offset: 0x0010			**Register Name: GMAC_TX_CTL0**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_EN Enable transmitter. 0: Disable 1: Enable When disable, transmit will continue until current transmit finish.
30	R/W	0x0	TX_FRM_LEN_CTL Frame Transmit Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off

29:0	/	/	/

8.11.5.6. GMAC Transmit Control Register1(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: GMAC_TX_CTL1
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_DMA_START Transmit DMA FSM Start 0: No valid 1: Start This cleared internally and always read a 0
30	R/W	0x0	TX_DMA_EN 0: Stop TX DMA after the completion of current frame transmission. 1: Start and run TX DMA.
29:11	/	/	/
10:8	R/W	0x0	TX_TH The threshold value of TX DMA FIFO. When TX_MD is 0, transmission starts when the size of frame in TX DMA FIFO is greater than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. 000: 64 001: 128 010: 192 011: 256 Others: Reserved
7:2	/	/	/
1	R/W	0x0	TX_MD Transmission Mode 0: TX start after TX DMA FIFO bytes is greater than TX_TH 1: TX start after TX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_TX_FIFO Flush the data in the TX FIFO. 0: Enable 1: Disable

8.11.5.7. GMAC Transmit Flow Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: GMAC_TX_FLOW_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_FLOW_CTL_STA This bit indicates a pause frame transmission is in progress. When the configuration of flow control is ready, set this bit to transmit a pause frame in full-duplex mode or activate the backpressure function. After completion of transmission, this bit will be cleared automatically. Before write register TX_FLOW_CTRL, this bit must be read as 0.
30:22	/	/	/

21:20	R/W	0x0	TX_PAUSE_FRM_SLOT The threshold of the pause timer at which the input flow control signal is checked for automatic retransmission of pause frame. The threshold values should be always less than the PAUSE_TIME
19:4	R/W	0x0	PAUSE_TIME The pause time field in the transmitted control frame.
3:2	/	/	/
1	R/W	0x0	ZQP_FRM_EN 0: Disable 1: Enable When set, enable the functionality to generate Zero-Quanta Pause control frame.
0	R/W	0x0	TX_FLOW_CTL_EN TX Flow Control Enable 0: Disable 1: Enable When set, enable flow control operation to transmit pause frames in full-duplex mode, or enable the back-pressure operation in half-duplex mode.

8.11.5.8. GMAC Transmit DMA Descriptor List Address Register (Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: GMAC_TX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_DESC_LIST The base address of transmit descriptor list. It must be 32-bit aligned.

8.11.5.9. GMAC Receive Control Register0(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: GMAC_RX_CTL0
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_EN Enable receiver 0: Disable receiver after current reception 1: Enable
30	R/W	0x0	RX_FRM_LEN_CTL Frame Receive Length Control 0: Up to 2,048 bytes (JUMBO_FRM_EN==0) Up to 10,240 bytes (JUMBO_FRM_EN==1) 1: Up to 16,384 bytes Any bytes after that is cut off
29	R/W	0x0	JUMBO_FRM_EN Jumbo Frame Enable 0: Disable 1: Enable Jumbo frames of 9,018 bytes without reporting a giant

28	R/W	0x0	STRIP_FCS When set, strip the Pad/FCS field on received frames only when the length's field value is less than or equal to 1,500 bytes.
27	R/W	0x0	CHECK_CRC Check CRC anable 0: Disable 1: Calculate CRC and check the IPv4 Header Checksum.
26:18	/	/	/
17	R/W	0x0	RX_PAUSE_FRM_MD 0: Only detect multicast pause frame specified in the 802.3x standard. 1: In addition to detect multicast pause frame specified in the 802.3x standard, also detect unicast pause frame with address specified in MAC Address 0 High Register and MAC address 0 Low Register.
16	R/W	0x0	RX_FLOW_CTL_EN When set, enable the functionality that decode the received pause frame and disable its transmitter for a specified time by pause frame.
15:0	/	/	/

8.11.5.10. GMAC Receive Control Register1(Default Value: 0x0000_0000)

Offset: 0x0028			**Register Name: GMAC_RX_CTL1**
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	RX_DMA_START When set, the RX DMA will go no to work. It is cleared internally and always read a 0.
30	R/W	0x0	RX_DMA_EN Receive DMA Enable 0: Stop RX DMA after finish receiving current frame 1: Start and run RX DMA
29:25	/	/	/
24	R/W	0x0	RX_FIFO_FLOW_CTL Receive FIFO Flow Control Enable 0: Disable 1: Enable,base on RX_FLOW_CTL_TH_DEACT and RX_FLOW_CTL_TH_ACT
23:22	R/W	0x0	RX_FLOW_CTL_TH_DEACT Threshold for Deactivating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.

21:20	R/W	0x0	RX_FLOW_CTL_TH_ACT Threshold for Activating Flow Control 00: Full minus 1 KB 01: Full minus 2 KB 10: Full minus 3 KB 11: Full minus 4 KB Valid in both half-duplex mode and full-duplex mode.
19:6	/	/	/
5:4	R/W	0x0	RX_TH Threshold for RX DMA FIFO Start 00: 64 01: 32 10: 96 11: 128 Only valid when RX_MD == 0, full frames with a length less than the threshold are transferred automatically.
3	R/W	0x0	RX_ERR_FRM 0: RX DMA drops frames with error 1: RX DMA forwards frames with error
2	R/W	0x0	RX_RUNT_FRM When set, forward undersized frames with no error and length less than 64bytes
1	R/W	0x0	RX_MD Receive Mode 0: RX start read after RX DMA FIFO bytes is greater than RX_TH 1: RX start read after RX DMA FIFO located a full frame
0	R/W	0x0	FLUSH_RX_FRM Flush Receive Frames 0: Enable when receive descriptors/buffers is unavailable 1: Disable

8.11.5.11. GMAC Receive DMA Descriptor List Address Register(Default Value: 0x0000_0000)

Offset: 0x0034			Register Name: GMAC_RX_DMA_LIST
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	RX_DESC_LIST The base address of receive descriptor list. It must be 32-bit aligned.

8.11.5.12. GMAC Receive Frame Filter Register(Default Value: 0x0000_0000)

Offset: 0x0038			Register Name: GMAC_RX_FRM_FLT
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	DIS_ADDR_FILTER Disable Address Filter 0: Enable 1: Disable

30:18	/	/	/
17	R/W	0x0	DIS_BROADCAST Disable Receive Broadcast frames 0: Receive 1: Drop
16	R/W	0x0	RX_ALL_MULTICAST Receive All Multicast frames Filter 0: Filter according to HASH_MULTICAST 1: Receive All
15:14	/	/	/
13:12	R/W	0x0	CTL_FRM_FILTER Receive Control Frames Filter 00: Drop all control frames 01: Drop all control frames 10: Receive all control frames 11: Receive all control frames when pass the address filter
11:10	/	/	/
9	R/W	0x0	HASH_MULTICAST Filter multicast frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
8	R/W	0x0	HASH_UNICAST Filter Unicast Frames Set 0: by comparing the DA field in DA MAC address registers 1: according to the hash table
7	/	/	/
6	R/W	0x0	SA_FILTER_EN Receive SA Filter Enable 0: Receive frames and update the result of SA filter 1: Update the result of SA filter. In addition, if the SA field of received frame does not match the values in SA MAC address registers, drop this frame.
5	R/W	0x0	SA_INV_FILTER Receive SA Invert Filter Set 0: Pass Frames whose SA field matches SA MAC address registers 1: Pass Frames whose SA field not matches SA MAC address registers
4	R/W	0x0	DA_INV_FILTER 0: Normal filtering of frames is performed 1: Filter both unicast and multicast frames by comparing DA field in inverse filtering mode
3:2	/	/	/
1	R/W	0x0	FLT_MD 0: If the HASH_MULTICAST or HASH_UNICAST is set, the frame is passed only when it matches the Hash filter 1: Receive the frame when it pass the address register filter or the hash filter(set by HASH_MULTICAST or HASH_UNICAST)

0	R/W	0x0	RX_ALL Receive All Frame Enable 0: Receive the frames that pass the SA/DA address filter 1: Receive all frames and update the result of address filter(pass or fail) in the receive status word

8.11.5.13. GMAC Receive Hash Table Register0(Default Value: 0x0000_0000)

Offset: 0x0040			Register Name: GMAC_RX_HASH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB0 The upper 32 bits of Hash table for receive frame filter.

8.11.5.14. GMAC Receive Hash Table Register1(Default Value: 0x0000_0000)

Offset: 0x0044			Register Name: GMAC_RX_HASH1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	HASH_TAB1 The lower 32 bits of Hash table for receive frame filter.

8.11.5.15. GMAC MII Command Register(Default Value: 0x0000_0000)

Offset: 0x0048			Register Name: GMAC_MII_CMD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:23	/	/	/
22:20	R/W	0x0	MDC_DIV_RATIO_M MDC Clock Divide Ratio 000: 16 001: 32 010: 64 011: 128 Others: Reserved MDC Clock is divided from AHB clock
19:17	/	/	/
16:12	R/W	0x0	PHY_ADDR PHY Address
11:9	/	/	/
8:4	R/W	0x0	PHY_REG_ADDR PHY Register Address
3:2	/	/	/
1	R/W	0x0	MII_WR MII Write and Read 0: Read 1: Write

0	R/W	0x0	MII_BUSY 0: Write no valid, read 0 indicate finish in read or write operation 1: Write start read or write operation, read 1 indicate busy.

8.11.5.16. GMAC MII Data Register(Default Value: 0x0000_0000)

Offset: 0x004C			Register Name: GMAC_MII_DATA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0x0	MII_DATA Written to or read from the register in the selected PHY.

8.11.5.17. GMAC MAC Address High Register0(Default Value: 0x0000_FFFF)

Offset: 0x0050			Register Name: GMAC_ADDR_HIGH0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	/	/	/
15:0	R/W	0xFFFF	MAC_ADDR_HIGH0 The upper 16bits of the 1st MAC address.

8.11.5.18. GMAC MAC Address Low Register0(Default Value: 0xFFFF_FFFF)

Offset: 0x0054			Register Name: GMAC_ADDR_LOW0
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0xFFFFFFFF	MAC_ADDR_LOW0 The lower 32bits of 1st MAC address.

8.11.5.19. GMAC MAC Address High RegisterN(Default Value: 0x0000_FFFF)

Offset: 0x0050+N*0x08(N=1~7)			Register Name: GMAC_ADDR_HIGHN
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	MAC_ADDR_CTL MAC Address is valid 0: Not valid 1: Valid
30	R/W	0x0	MAC_ADDR_TYPE MAC Address Type 0: Used to compare with the destination address of the received frame 1: Used to compare with the source address of the received frame
29:24	R/W	0x0	MAC_ADDR_BYTE_CTL MAC address byte control mask. The lower bit of mask controls the lower byte in MAC address. When the bit of mask is 1, do not compare the corresponding byte.
23:16	/	/	/

15:0	R/W	0x0	MAC_ADDR_HIGH The upper 16bits of the MAC address.

8.11.5.20. GMAC MAC Address Low RegisterN(Default Value: 0xFFFF_FFFF)

Offset: 0x0054+N*0x08(N=1~7)			Register Name: GMAC_ADDR_LOWN
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	MAC_ADDR_LOWN The lower 32bits of MAC address N (N: 1~7).

8.11.5.21. GMAC Transmit DMA Status Register(Default Value: 0x0000_0000)

Offset: 0x00B0			Register Name: GMAC_TX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2:0	R	0x0	TX_DMA_STA The state of Transmit DMA FSM. 000: STOP, When reset or disable TX DMA 001: RUN_FETCH_DESC, Fetching TX DMA descriptor 010: RUN_WAIT_STA, Waiting for the status of TX frame 011: RUN_TRANS_DATA, Passing frame from host memory to TX DMA FIFO 100: Reserved 101: Reserved 110: SUSPEND, TX descriptor unavailable or TX DMA FIFO underflow 111: RUN_CLOSE_DESC, Closing TX descriptor.

8.11.5.22. GMAC Transmit DMA Current Descriptor Register(Default Value: 0x0000_0000)

Offset: 0x00B4			Register Name: GMAC_TX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit descriptor.

8.11.5.23. GMAC Transmit DMA Current Buff Address Register(Default Value: 0x0000_0000)

Offset: 0x00B8			Register Name: GMAC_TX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current transmit DMA buffer

8.11.5.24. GMAC Receive DMA Status Register(Default Value: 0x0000_0000)

Offset: 0x00C0			Register Name: GMAC_RX_DMA_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/

2:0	R	0x0	RX_DMA_STA The state of RX DMA FSM. 000: STOP, When reset or disable RX DMA 001: RUN_FETCH_DESC, Fetching RX DMA descriptor 010: Reserved 011: RUN_WAIT_FRM, Waiting for frame 100: SUSPEND, RX descriptor unavailable 101: RUN_CLOSE_DESC, Closing RX descriptor 110: Reserved 111: RUN_TRANS_DATA, Passing frame from host memory to RX DMA FIFO

8.11.5.25. GMAC Receive DMA Current Descriptor Register(Default Value: 0x0000_0000)

Offset: 0x00C4			Register Name: GMAC_RX_DMA_CUR_DESC
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive descriptor

8.11.5.26. GMAC Receive DMA Current Buffer Address Register(Default Value: 0x0000_0000)

Offset: 0x00C8			Register Name: GMAC_RX_DMA_CUR_BUF
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	The address of current receive DMA buffer

8.11.5.27. GMAC RGMII Status Register(Default Value: 0x0000_0000)

Offset: 0x00D0			Register Name: GMAC_RGMII_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:4	/	/	/
3	R	0x0	RGMII_LINK The link status of RGMII interface 0: Down 1: Up
2:1	R	0x0	RGMII_LINK_SPD The link speed of RGMII interface 00: 2.5 MHz 01: 25 MHz 10: 125 MHz 11: Reserved
0	R	0x0	RGMII_LINK_MD The link Mode of RGMII interface 0: Half-Duplex 1: Full-Duplex

8.12. Transport Stream Controller

8.12.1. Overview

The transport stream controller (TSC) is responsible for de-multiplexing and pre-processing the inputting multimedia data defined in ISO/IEC 13818-1.

The transport stream controller receives multimedia data stream from SSI (Synchronous Serial Port)/SPI (Synchronous Parallel Port) inputs and de-multiplexing the data into Packets by PID (Packet Identify). Before the Packet is stored to memory by DMA, it can be pre-processed by the Transport Stream Descrambler.The transport stream controller can be used for almost all multimedia application cases, for example: DVB Set top Box, IPTV, Streaming-media Box, multi-media players and so on.

Features:

- Supports industry-standard AMBA Host Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus.
- Supports AHB 32-bit bus width
- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter
- Supports multiple transport stream packet (188, 192, 204) formats
- Configurable SPI and SSI timing parameters
- Hardware packet synchronous byte error detection
- Hardware PCR packet detection
- 64x16-bit FIFO for TSG, 64x32-bit FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DMA for data transfer
- Supports interrupt

8.12.2. Block Diagram

Figure 8-31 shows a block diagram of the TSC.

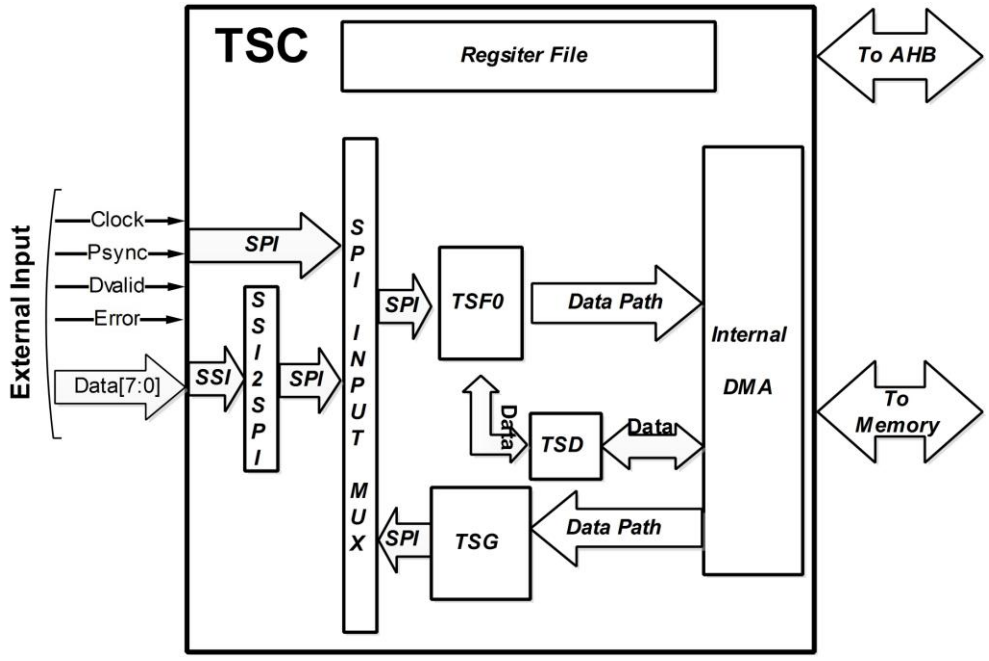


Figure 8-31. TSC Block Diagram1

TSC – TS Controller
TSF – TS Filter
TSD – TS Descrambler
TSG – TS Generator

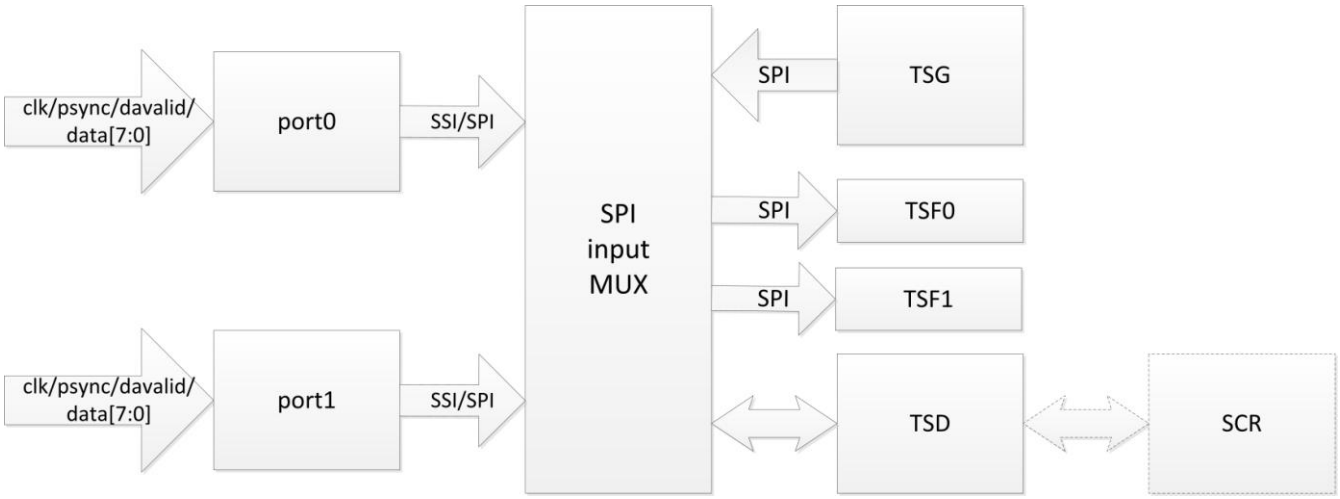


Figure 8-32. TSC Block Diagram2

8.12.3. Operations and Functional Descriptions

8.12.3.1. External Signals

Table 8-20 describes the external signals of TSC.

Table 8-20. TSC External Signals

Pin Name	Description	Type
TS0_CLK	Clock of SPI/SSI data input	I

TS0_SYNC	Packet sync (or Start flag) for TS packet	I
TS0_DVLD	Data valid flag for TS data input	I
TS0_ERR	Error flag for TS data, but do not used by TSC	I
TS0_D[7:0]	TS data input. Data[7:0] are used in SPI mode; Only Data[0] is used in SSI mode.	I
TS1_CLK	Clock of SPI/SSI data input	I
TS1_SYNC	Packet sync (or Start flag) for TS packet	I
TS1_DVLD	Data valid flag for TS data input	I
TS1_ERR	Error flag for TS data, but do not used by TSC	I
TS1_D[7:0]	TS data input. Data[7:0] are used in SPI mode; Only Data[0] is used in SSI mode.	I

8.12.3.2. Clock Sources

Table 8-21 describes the clock sources of TSC.

Table 8-21. TSC Clock Sources

Clock Sources	Description
OSC24M	24MHz Crystal
PLL_PERIPH0	Peripheral Clock, default value is 600MHz

8.12.4. Register List

Module Name	Base Address
TSC	0x01C04000
TSG OFFSET	0x00000040
TSF0 OFFSET	0x00000080
TSF1 OFFSET	0x00000100
TSD0 OFFSET	0x00000180
TSD1 OFFSET	0x00000200

Register Name	Offset	Description
TSC		
TSC_CTLR	TSC + 0x0000	TSC Control Register
TSC_STAR	TSC + 0x0004	TSC Status Register
TSC_PCTLR	TSC + 0x0010	TSC Port Control Register
TSC_PPARR	TSC + 0x0014	TSC Port Parameter Register
TSC_TSFMUXR	TSC + 0x0020	TSC TSF Input Multiplex Control Register
TSC_OUTMUXR	TSC + 0x0028	TSC Port Output Multiplex Control Register
TSG		
TSG_CTLR	TSG + 0x0000	TSG Control Register
TSG_PPR	TSG + 0x0004	TSG Packet Parameter Register
TSG_STAR	TSG + 0x0008	TSG Status Register
TSG_CCR	TSG + 0x000C	TSG Clock Control Register
TSG_BBAR	TSG + 0x0010	TSG Buffer Base Address Register
TSG_BSZR	TSG + 0x0014	TSG Buffer Size Register
TSG_BPR	TSG + 0x0018	TSG Buffer Pointer Register
TSF		

TSF_CTLR	TSF + 0x0000	TSF Control Register
TSF_PPR	TSF + 0x0004	TSF Packet Parameter Register
TSF_STAR	TSF + 0x0008	TSF Status Register
TSF_DIER	TSF + 0x0010	TSF DMA Interrupt Enable Register
TSF_OIER	TSF + 0x0014	TSF Overlap Interrupt Enable Register
TSF_DISR	TSF + 0x0018	TSF DMA Interrupt Status Register
TSF_OISR	TSF + 0x001C	TSF Overlap Interrupt Status Register
TSF_PCRCR	TSF + 0x0020	TSF PCR Control Register
TSF_PCRDR	TSF + 0x0024	TSF PCR Data Register
TSF_CENR	TSF + 0x0030	TSF Channel Enable Register
TSF_CPER	TSF + 0x0034	TSF Channel PES Enable Register
TSF_CDER	TSF + 0x0038	TSF Channel Descramble Enable Register
TSF_CINDR	TSF + 0x003C	TSF Channel Index Register
TSF_CCTLR	TSF + 0x0040	TSF Channel Control Register
TSF_CSTAR	TSF + 0x0044	TSF Channel Status Register
TSF_CCWIR	TSF + 0x0048	TSF Channel CW Index Register
TSF_CPIDR	TSF + 0x004C	TSF Channel PID Register
TSF_CBBAR	TSF + 0x0050	TSF Channel Buffer Base Address Register
TSF_CBSZR	TSF + 0x0054	TSF Channel Buffer Size Register
TSF_CBWPR	TSF + 0x0058	TSF Channel Buffer Write Pointer Register
TSF_CBRPR	TSF + 0x005C	TSF Channel Buffer Read Pointer Register
TSD		
TSD_CTLR	TSD + 0x0000	TSD Control Register
TSD_STAR	TSD + 0x0004	TSD Status Register
TSD_CWIR	TSD + 0x001C	TSD Control Word Index Register
TSD_CWR	TSD + 0x0020	TSD Control Word Register

8.12.5. Register Description

8.12.5.1. TSC Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: TSC_CTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

8.12.5.2. TSC Status Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: TSC_STAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

8.12.5.3. TSC Port Control Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: TSC_PCTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	TSOUTPORT0CTRL TS Output Port0 Control

Offset: 0x0010			Register Name: TSC_PCTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
			0 : SPI 1 : SSI
15:2	/	/	/
1	R/W	0x0	TSINPORT1CTRL TS Input Port1 Control 0 : SPI 1 : SSI
0	R/W	0x0	TSINPORT0CTRL TS Input Port0 Control 0 : SPI 1 : SSI

8.12.5.4. TSC Port Parameter Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: TSC_PPARR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	/	/	/
15:8	R/W	0x0	TSINPORT1PAR TS Input Port1 Parameters **Bit** / **Definition** 7:5 – Reserved 4 – SSI data order 0: MSB first for one byte data 1: LSB first for one byte data 3 – CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing 2 – ERROR signal polarity 0: High level active 1: Low level active 1 – DVALID signal polarity 0: High level active 1: Low level active 0 – PSYNC signal polarity 0: High level active 1: Low level active
7:0	R/W	0x0	TSINPORT0PAR TS Input Port0 Parameters **Bit** / **Definition** 7:5 – Reserved 4 – SSI data order 0: MSB first for one byte data

Offset: 0x0014			Register Name: TSC_PPARR
Bit	Read/Write	Default/Hex	Description
			1: LSB first for one byte data 3 CLOCK signal polarity 0 : Rise edge capturing 1: Fall edge capturing 2 ERROR signal polarity 0: High level active 1: Low level active 1 DVALID signal polarity 0: High level active 1: Low level active 0 PSYNC signal polarity 0: High level active 1: Low level active

8.12.5.5. TSC TSF Input Multiplex Control Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: TSC_TSFMUXR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0x0	TSF1INPUTMUXCTRL TSF1 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port0 0010: Data from TS IN Port1 Others: Reserved
3:0	R/W	0x0	TSF0INPUTMUXCTRL TSF0 Input Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port0 0010: Data from TS IN Port1 Others: Reserved

8.12.5.6. TSC Port Output Multiplex Control Register(Default Value: 0x0000_0000)

Offset: 0x0028			Register Name: TSC_TSFMUXR
Bit	Read/Write	Default/Hex	Description
31:4	/	/	/
3:0	R/W	0x0	TSPORTOUTPUTMUXCTRL TS Port Output Multiplex Control 0000: Data from TSG 0001: Data from TS IN Port0 0010: Data from TS IN Port1

Offset: 0x0028			Register Name: TSC_TSFMUXR
Bit	Read/Write	Default/Hex	Description
			Others : Reserved

8.12.5.7. TSG Control and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x0000			Register Name: TSG_CSR
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R	0x0	TSGSTS Status for TS Generator 00: IDLE state 01: Running state 10: PAUSE state Others: Reserved
23:10	/	/	/
9	R/W	0x0	TSGLBUFMODE Loop Buffer Mode When set to '1', the TSG external buffer is in loop mode.
8	R/W	0x0	TSGSYNCBYTECHKEN Sync Byte Check Enable Enable/ Disable check SYNC byte fro receiving new packet 0: Disable 1: Enable If enable check SYNC byte and an error SYNC byte is received, TS Generator would come into PAUSE state. If the correspond interrupt is enabled, the interrupt would happen.
7:3	/	/	/
2	R/W	0x0	TSGPAUSEBIT Pause Bit for TS Generator Write '1' to pause TS Generator. TS Generator would stop fetch new data from DRAM. After finishing this operation, this bit will clear to zero by hardware. In PAUSE state, write '1' to resume this state.
1	R/W	0x0	TSGSTOPBIT Stop Bit for TS Generator Write '1' to stop TS Generator. TS Generator would stop fetch new data from DRAM. The data already in its FIFO should be sent to TS filter. After finishing this operation, this bit will clear to zero by hardware.
0	R/W	0x0	TSGSTARTBIT Start Bit for TS Generator Write '1' to start TS Generator. TS Generator would fetch data from DRAM and generate SPI stream to TS filter. This bit will clear to zero by hardware after TS Generator is running.

8.12.5.8. TSG Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSG+0x0004			Register Name: TSG_PPR
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

Offset: TSG+0x0004			Register Name: TSG_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
23:16	R/W	0x47	SYNCBYTEVAL Sync Byte Value This is the value of sync byte used in the TS Packet.
15:8	/	/	/
7	R/W	0x0	SYNCBYTEPOS Sync Byte Position 0: The 1st byte position 1: The 5th byte position This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PKTSIZE Packet Size Byte Size for one TS packet 0: 188 bytes Others: Reserved

8.12.5.9. TSG Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSG+0x0008			Register Name: TSG_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSGENDIE TS Generator (TSG) End Interrupt Enable 0: Disable 1: Enable If set this bit, the interrupt would assert to CPU when all data in external DRAM are sent to TS PID filter.
18	R/W	0x0	TSGFFIE TS Generator (TSG) Full Finish Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSGHFIE TS Generator (TSG) Half Finish Interrupt Enable 0: Disable 1: Enable
16	R/W	0x0	TSGERRSYNCBYTEIE TS Generator (TSG) Error Sync Byte Interrupt Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0x0	TSGENDSTS TS Generator (TSG) End Status Write ‘1’ to clear it.
2	R/W	0x0	TSGFFSTS TS Generator (TSG) Full Finish Status

Offset: TSG+0x0008			Register Name: TSG_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
			Write '1' to clear it.
1	R/W	0x0	TSGHFSTS TS Generator (TSG) Half Finish Status Write '1' to clear it.
0	R/W	0x0	TSGERRSYNCBYTESTS TS Generator (TSG) Error Sync Byte Status Write '1' to clear it.

8.12.5.10. TSG Clock Control Register(Default Value: 0x0000_0000)

Offset: TSG+0x000C			Register Name: TSG_CCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	TSGCDF_N TSG Clock Divide Factor (N) The Numerator part of TSG Clock Divisor Factor.
15:0	R/W	0x0	TSGCDF_D TSG Clock Divide Factor (D) The Denominator part of TSG Clock Divisor Factor. Frequency of output clock: Fo = (Fi*(N+1))/(8*(D+1)). Fi is the input special clock of TSC, and D must not less than N.

8.12.5.11. TSG Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSG+0x0010			Register Name: TSG_BBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	RW	0x0	TSGBUFBASE Buffer Base Address This value is a start address of TSG buffer. This value should be 4 words (16-byte) aligned, and the lowest 4 bits of this value should be zero.

8.12.5.12. TSG Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSG+0x0014			Register Name: TSG_BSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:0	R/W	0x0	TSGBUFSIZE Data Buffer Size for TS Generator It is in byte unit. The size should be 4 words (16-byte) aligned, and the lowest 4 bits should be zero.

8.12.5.13. TSG Buffer Pointer Register(Default Value: 0x0000_0000)

Offset: TSG+0x0018	Register Name: TSG_BPR

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	0x0	TSGBUFPTR Data Buffer Pointer for TS Generator Current TS generator data buffer read pointer (in byte unit)

8.12.5.14. TSF Control and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x0000			Register Name: TSF_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
2	R/W	0x0	TSF ENABLE 0: Disable TSF Input 1: Enable TSF Input
1	/	/	/
0	R/W	0x0	TSFGSR TSF Global Soft Reset Writing '1' will reset all status and state machine of TSF. And it is cleared by hardware after finish reset. Writing '0' has no effect.

8.12.5.15. TSF Packet Parameter Register(Default Value: 0x0047_0000)

Offset: TSF+0x0004			Register Name: TSF_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:28	R/W	0x0	LOSTSYNCTHD Lost Sync Packet Threshold It is used for packet sync lost by checking the value of sync byte.
27:24	R/W	0x0	SYNCTHD Sync Packet Threshold It is used for packet sync by checking the value of sync byte.
23:16	R/W	0x47	SYNCBYTEVAL Sync Byte Value This is the value of sync byte used in the TS Packet.
15:10	/	/	/
9:8	R/W	0x0	SYNCMTHD Packet Sync Method 00: By PSYNC signal 01: By sync byte 10: By both PSYNC and Sync Byte 11: Reserved
7	R/W	0x0	SYNCBYTEPOS Sync Byte Position 0: The 1st byte position 1: The 5th byte position This bit is only used for 192 bytes packet size.
6:2	/	/	/
1:0	R/W	0x0	PKTSIZE

Offset: TSF+0x0004			Register Name: TSF_PPR
Bit	**Read/Write**	**Default/Hex**	**Description**
			Packet Size Byte Size for one TS packet 00: 188 bytes 01: 192 bytes 10: 204 bytes 11: Reserved

8.12.5.16. TSF Interrupt Enable and Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x0008			Register Name: TSF_IESR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:20	/	/	/
19	R/W	0x0	TSFFOIE TS PID Filter (TSF) Internal FIFO Overrun Interrupt Enable 0: Disable 1: Enable
18	R/W	0x0	TSFPPDIE TS PCR Packet Detect Interrupt Enable 0: Disable 1: Enable
17	R/W	0x0	TSFCOIE TS PID Filter (TSF) Channel Overlap Interrupt Global Enable 0: Disable 1: Enable
16	R/W	0x0	TSFCDIE TS PID Filter (TSF) Channel DMA Interrupt Global Enable 0: Disable 1: Enable
15:4	/	/	/
3	R/W	0x0	TSFFOIS TS PID Filter (TSF) Internal FIFO Overrun Status Write ‘1’ to clear it.
2	R/W	0x0	TSFPPDIS TS PCR Packet Found Status When it is ‘1’, one TS PCR Packet is found. Write ‘1’ to clear it.
1	R	0x0	TSFCOIS TS PID Filter (TSF) Channel Overlap Status It is global status for 32 channels. It would clear to zero after all channels status bits are cleared.
0	R	0x0	TSFCDIS TS PID Filter (TSF) Channel DMA status It is global status for 32 channels. It would clear to zero after all channels status bits are cleared.

8.12.5.17. TSF DMA Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x0010			Register Name: TSF_DIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMAIE DMA Interrupt Enable DMA interrupt enable bits for channel 0~31.

8.12.5.18. TSF Overlap Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x0014			Register Name: TSF_OIER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	OLPIE Overlap Interrupt Enable Overlap interrupt enable bits for channel 0~31.

8.12.5.19. TSF DMA Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x0018			Register Name: TSF_DISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DMAIS DMA Interrupt Status DMA interrupt Status bits for channel 0~31. Set by hardware, and writing '1'can be cleared by software. When both these bits and the corresponding DMA Interrupt Enable bits set, the TSF interrupt will generate.

8.12.5.20. TSF Overlap Interrupt Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x001C			Register Name: TSF_OISR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	OLPIS Overlap Interrupt Status Overlap interrupt Status bits for channel 0~31. Setting by hardware, and writing '1'can be cleared by software. When both these bits and the corresponding Overlap Interrupt Enable bits set, the TSF interrupt will generate.

8.12.5.21. TSF PCR Control Register(Default Value: 0x0000_0000)

Offset: TSF+0x0020			Register Name: TSF_PCRCR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:17	/	/	/
16	R/W	0x0	PCRDE PCR Detecting Enable 0: Disable 1: Enable

Offset: TSF+0x0020			Register Name: TSF_PCRCR
Bit	**Read/Write**	**Default/Hex**	**Description**
15:13	/	/	/
12:8	R/W	0x0	PCRCIND Channel Index m for Detecting PCR packet (m from 0 to 31)
7:1	/	/	/
0	R	0x0	PCRLSB PCR Contest LSB 1 bit PCR[0]

8.12.5.22. TSF PCR Data Register(Default Value: 0x0000_0000)

Offset: TSF+0x0024			Register Name: TSF_PCRDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R	0x0	PCRMSB PCR Data High 32 bits PCR[33:1]

8.12.5.23. TSF Channel Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x0030			Register Name: TSF_CENR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	FILTEREN Filter Enable for Channel 0~31 0: Disable 1: Enable From Disable to Enable, the internal status of the corresponding filter channel will be reset.

8.12.5.24. TSF Channel PES Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x0034			Register Name: TSF_CPER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	PESEN PES Packet Enable for Channel 0~31 0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

8.12.5.25. TSF Channel Descramble Enable Register(Default Value: 0x0000_0000)

Offset: TSF+0x0038			Register Name: TSF_CDER
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	DESCEN Descramble Enable for Channel 0~31

Offset: TSF+0x0038			Register Name: TSF_CDER
Bit	Read/Write	Default/Hex	Description
			0: Disable 1: Enable These bits should not be changed during the corresponding channel enable.

8.12.5.26. TSF Channel Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x003C			Register Name: TSF_CINDR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4:0	R/W	0x0	CHIND Channel Index This value is the channel index for channel private registers access. Range is from 0x00 to 0x1f. Address range of channel private registers is from 0x40 to 0x7f.

8.12.5.27. TSF Channel Control Register(Default Value: 0x0000_0000)

Offset: TSF+0x0040			Register Name: TSF_CCTLR
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.12.5.28. TSF Channel Status Register(Default Value: 0x0000_0000)

Offset: TSF+0x0044			Register Name: TSF_CSTAR
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

8.12.5.29. TSF Channel CW Index Register(Default Value: 0x0000_0000)

Offset: TSF+0x0048			Register Name: TSF_CCWIR
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2:0	R/W	0x0	CWIND Related Control Word Index Index to the control word used by this channel when Descramble Enable of this channel enable. This value is useless when the corresponding Descramble Enable is ‘0’.

8.12.5.30. TSF Channel PID Register(Default Value: 0x1FFF_0000)

Offset: TSF+0x004C			Register Name: TSF_CPIDR
Bit	Read/Write	Default/Hex	Description

Offset: TSF+0x004C			Register Name: TSF_CPIDR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x1fff	PIDMSK Filter PID Mask for Channel
15:0	R/W	0x0	PIDVAL Filter PID value for Channel

8.12.5.31. TSF Channel Buffer Base Address Register(Default Value: 0x0000_0000)

Offset: TSF+0x0050			Register Name: TSF_CBBAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TSFBUFBADDR Data Buffer Base Address for Channel It is 4-word (16Byte) aligned address. The LSB four bits should be zero.

8.12.5.32. TSF Channel Buffer Size Register(Default Value: 0x0000_0000)

Offset: TSF+0x0054			Register Name: TSF_CBSZR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:26	/	/	/
25:24	R/W	0x0	CHDMAINTTHD DMA Interrupt Threshold for Channel The unit is TS packet size. When received packet (has also stored in DRAM) size is beyond (>=) threshold value, the corresponding channel interrupt is generated to CPU. TSC should count the new received packet again, when exceed the specified threshold value, one new interrupt is generated again. 00: 1/2 data buffer packet size 01: 1/4 data buffer packet size 10: 1/8 data buffer packet size 11: 1/16 data buffer packet size
23:21	/	/	/
20:0	R/W	0x0	CHBUFPKTSZ Data Buffer Packet Size for Channel The exact buffer size of buffer is N+1 byte. The maximum buffer size is 2MB. This size should be 4word (16 Byte) aligned. The LSB four bit should be zero.

8.12.5.33. TSF Channel Buffer Write Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x0058			Register Name: TSF_CBWPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BUFWRPTR Data Buffer Write Pointer (in Bytes) This value is changed by hardware, when data is filled into buffer, this pointer is increased. And this pointer can be set by software, but it should not be changed by

Offset: TSF+0x0058			Register Name: TSF_CBWPR
Bit	**Read/Write**	**Default/Hex**	**Description**
			software during the corresponding channel is enabled.

8.12.5.34. TSF Channel Buffer Read Pointer Register(Default Value: 0x0000_0000)

Offset: TSF+0x005C			Register Name: TSF_CBRPR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
20:0	R/W	0x0	BUFRDPTR Data Buffer Read Pointer (in Bytes) This pointer should be changed by software after the data of buffer is read.

8.12.5.35. TSD Control Register(Default Value: 0x0000_0000)

Offset: TSD+0x0000			Register Name: TSD_CTLR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	
1:0	R/W	0x0	DESCARITH Descramble Arithmetic Reserved

8.12.5.36. TSD Status Register(Default Value: 0x0000_0000)

Offset: TSD+0x0004			Register Name: TSD_STAR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	/	/	/

8.12.5.37. TSD Control Word Index Register(Default Value: 0x0000_0000)

Offset: TSD+0x001C			Register Name: TSD_CWIR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:3	/	/	/
6:4	R/W	0x0	CWI Control Word Index This value is the Control index for Control word access. Range is from 0x0 to 0x7.
3:2	/	/	/
1:0	R/W	0x0	CWII Control Word Internal Index 00 : Odd Control Word Low 32-bit, OCW[31:0] 01 : Odd Control Word High 32-bit, OCW[63:32] 10 : Even Control Word Low 32-bit, ECW[31:0] 11 : Even Control Word High 32-bit, ECW[63:0]

8.12.5.38. TSD Control Word Register(Default Value: 0x0000_0000)

Offset: TSD+0x0020			Register Name: TSD_CWR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	CWD Content of Control Word corresponding to the TSD_CWIR value

8.13. Smart Card Reader

8.13.1. Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and smart card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, and data transfer, etc.

Features:

- Supports APB slave interface for easy integration with AMBA-based host systems
- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Perform functions needed for complete smart card sessions
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Supports commonly used communication protocols:
  - T=0: for asynchronous half-duplex character transmission
  - T=1: for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and other non-ISO 7816 and non-EMV cards
- 128x8-bit FIFO for data transmit & receive

8.13.2. Block Diagram

Figure 8-33 shows a block diagram of the SCR.

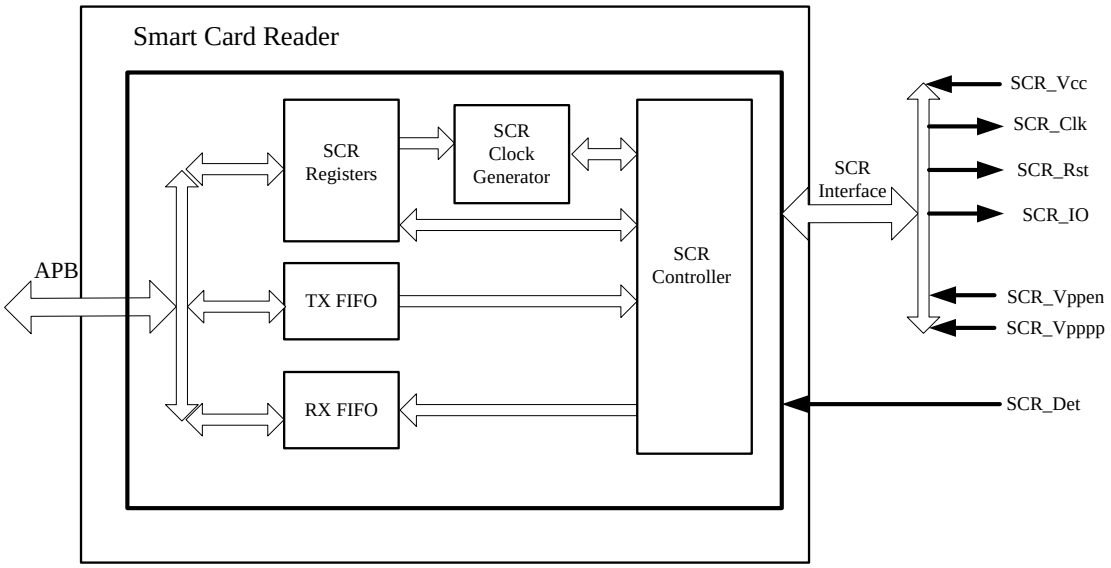


Figure 8-33. SCR Block Diagram

8.13.3. Operations and Functional Descriptions

8.13.3.1. External Signals

The following table describes the external signals of SCR.

Table 8-22. SCR External Signals

Pin Name	Description	Type
SMC_SLK	Clock of SCR	O
SMC_RST	Reset Signal	O
SMC_SDA	Data Signal	I/O
SMC_DET	Card Detect	I
SMC_VPPEN	Program Voltage Enable	O
SMC_VPPPP	Program Control	O
SMC_VCCEN	Power Enable	O

8.13.3.2. Clock Sources

The following table describes the clock source of SCR.

Table 8-23. SCR Clock Sources

Clock Sources	Description
APB2_CLK	APB2 Clock, default value is 24MHz Crystal

8.13.3.3. Timing Diagram

Please refer ISO/IEC 7816 and EMV2000 Specification.

8.13.3.4. Clock Generator

The Clock Generator generates the Smart Card Clock signal and the Baud Clock Impulse signal, used in timing the Smart Card Reader.

The Smart Card Clock signal is used as the main clock for the smart card. Its frequency can be adjusted using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock. The SCCLK frequency is given by the following equation:

$$f_{scclk} = \frac{f_{sysclk}}{2 * (SCCDIV + 1)}$$, f_{scclk} -- Smart Card Clock Frequency, f_{sysclk} -- System Clock (PCLK) Frequency

The Baud Clock Impulse signal is used to transmit and receive serial between the Smart Card Reader and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV). The value is used to divide the system clock. The BUAD rate is given by the following equation:

$$BAUD = \frac{f_{sysclk}}{2 * (BAUDDIV + 1)}$$, $BAUD$ -- Baud rate of the data stream between Smart Card and Reader

$$\frac{1}{BAUD} = ETU = \frac{372}{f_{scclk}}$$

In this case, the BAUDDIV should be

$$BAUDDIV = \frac{372 * f_{sysclk}}{2 * f_{scclk}} - 1 = 372 * (SCCDIV + 1) - 1$$

After the ATR is completed, the ETU can be changed according to Smart Card abilities.

$$\frac{1}{BAUD} = ETU = \frac{F}{D} * \frac{1}{f_{scclk}}$$

Parameters F and D are defined in the ISO/IEC 7816-3 Specification.

8.13.3.5. SCR IO Pad Configuration

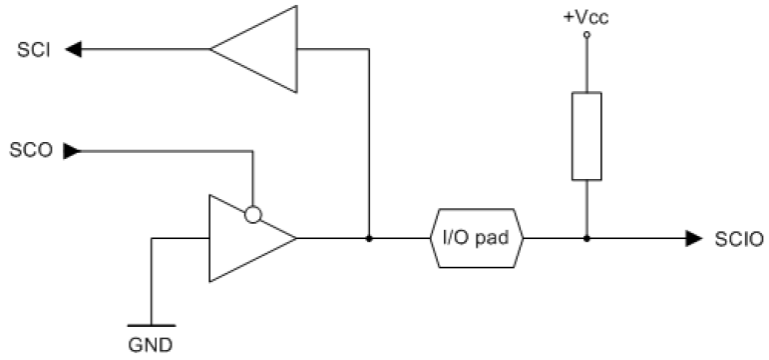


Figure 8-34. SCR IO Pad Diagram

8.13.4. Register List

Module Name	Base Address
SCR	0x01C2C400

Register Name	Offset	Description
SCR_CSR	0x0000	Smart Card Reader Control and Status Register
SCR_INTEN	0x0004	Smart Card Reader Interrupt Enable Register 1
SCR_INTST	0x0008	Smart Card Reader Interrupt Status Register 1
SCR_FCSR	0x000C	Smart Card Reader FIFO Control and Status Register
SCR_FCNT	0x0010	Smart Card Reader RX and TX FIFO Counter Register
SCR_RPT	0x0014	Smart Card Reader RX and TX Repeat Register
SCR_DIV	0x0018	Smart Card Reader Clock and Baud Divisor Register
SCR_LTIM	0x001c	Smart Card Reader Line Time Register
SCR_CTIM	0x0020	Smart Card Reader Character Time Register
SCR_LCTLR	0x0030	Smart Card Reader Line Control Register
SCR_FIFO	0x0100	Smart Card Reader RX and TX FIFO Access Point

8.13.5. Register Description

8.13.5.1. Smart Card Reader Control and Status Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: SCR_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R	0x0	SCDET Smart Card Detected This bit is set to '1' when the *scdetect* input is active at least for a debounce time.
30	/	/	/
24	R/W	0x0	SCDETPOL Smart Card Detect Polarity This bit set polarity of *scdetect* signal. 0: Low Active 1: High Active

Offset: 0x0000			Register Name: SCR_CSR
Bit	**Read/Write**	**Default/Hex**	**Description**
23:22	R/W	0x0	Protocol Selection (PTLSEL) 00: T=0. 01: T=1, no character repeating and no guard time is used when T=1 protocol is selected. 10: Reserved 11: Reserved
21	R/W	0x0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
20	R/W	0x0	TSRXE TS Receive Enable When set to '1', the TS character (the first ATR character) will be stored in RXFIFO during card session.
19	R/W	0x0	CLKSTPPOL Clock Stop Polarity The value of the *scclk* output during the clock stop state.
18	R/W	0x0	PECRXE Parity Error Character Receive Enable Enables storage of the characters received with wrong parity in RX FIFO.
17	R/W	0x0	MSBF MSB First When high, inverse bit ordering convention (msb to lsb) is used.
16	R/W	0x0	DATAPOL Data Polarity When high, inverse level convention is used (A='1', Z='0').
15:12	/	/	/
11	R/W	0x0	DEACTDeactivation. Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
10	R/W	0x0	ACT Activation. Setting of this bit initializes the activation sequence. When the activation is finished, the ACT bit is automatically cleared.
9	R/W	0x0	WARMRST Warm Reset Command. Writing '1' to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
8	R/W	0x0	CLKSTOP Clock Stop. When this bit is asserted and the smart card I/O line is in 'Z' state, the SCR core stops driving of the smart card clock signal after the CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is deasserted. New character transmission can be started after CLKSTARTDELAY time. The expiration of both times is signaled by the CLKSTOPRUN bit in the interrupt registers.
7:3	/	/	/
2	R/W	0x0	GINTEN Global Interrupt Enable. When high, IRQ output assertion is enabled.
1	R/W	0x0	RXEN Receiving Enable. When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
0	R/W	0x0	TXEN

Offset: 0x0000			Register Name: SCR_CSR
Bit	Read/Write	Default/Hex	Description
			Transmission Enable. When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card.

8.13.5.2. Smart Card Reader Interrupt Enable Register(Default Value: 0x0000_0000)

Offset: 0x0004			Register Name: SCR_INTEN
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt Enable.
22	R/W	0x0	SCACT Smart Card Activation Interrupt Enable.
21	R/W	0x0	SCINS Smart Card Inserted Interrupt Enable.
20	R/W	0x0	SCREM Smart Card Removed Interrupt Enable.
19	R/W	0x0	ATRDONE ATR Done Interrupt Enable.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt Enable.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt Enable.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt Enable.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt Enable.
11	R/W	0x0	RXDONE RX Done Interrupt Enable.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt Enable.
9	R/W	0x0	RXFIFOFULL RX FIFO Full Interrupt Enable.
8	/	/	/
7:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt Enable.
3	R/W	0x0	TXDONE TX Done Interrupt Enable.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt Enable.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt Enable.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt Enable.

8.13.5.3. Smart Card Reader Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x0008	Register Name: SCR_INTST

Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0x0	SCDEA Smart Card Deactivation Interrupt. When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete.
22	R/W	0x0	SCACT Smart Card Activation Interrupt. When enabled, this interrupt is asserted after the Smart Card activation sequence is complete.
21	R/W	0x0	SCINS Smart Card Inserted Interrupt. When enabled, this interrupt is asserted after the smart card insertion.
20	R/W	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal.
19	R/W	0x0	ATRDONE ATR Done Interrupt. When enabled, this interrupt is asserted after the ATR sequence is successfully completed.
18	R/W	0x0	ATRFAIL ATR Fail Interrupt. When enabled, this interrupt is asserted if the ATR sequence fails.
17	R/W	0x0	C2CFULL Two Consecutive Characters Limit Interrupt. When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.
16	R/W	0x0	CLKSTOPRUN Smart Card Clock Stop/Run Interrupt. When enabled, this interrupt is asserted in two cases: When the smart card clock is stopped. When the new character can be started after the clock restart. To distinguish between the two interrupt cases, we recommend reading the **CLKSTOP** bit in **SCR_CSR** register.
15:13	/	/	/
12	R/W	0x0	RXPERR RX Parity Error Interrupt. When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used.
11	R/W	0x0	RXDONE RX Done Interrupt. When enabled, this interrupt is asserted after a character was received from the Smart Card.
10	R/W	0x0	RXFIFOTHD RX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
9	R/W	0x0	RXFIFOFULL RX FIFO Full Interrupt.

Offset: 0x0008			Register Name: SCR_INTST
Bit	**Read/Write**	**Default/Hex**	**Description**
			When enabled, this interrupt is asserted if the RX FIFO is filled up.
8:5	/	/	/
4	R/W	0x0	TXPERR TX Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guard time after the character transmission was repeated TXREPEAT times or T=1 protocol is used.
3	R/W	0x0	TXDONE TX Done Interrupt. When enabled, this interrupt is asserted after one character was transmitted to the smart card.
2	R/W	0x0	TXFIFOTHD TX FIFO Threshold Interrupt. When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.
1	R/W	0x0	TXFIFOEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out.
0	R/W	0x0	TXFIFODONE TX FIFO Done Interrupt. When enabled, this interrupt is asserted after all bytes from TX FIFO transferred to the Smart Card.

8.13.5.4. Smart Card Reader FIFO Control and Status Register(Default Value: 0x0000_0101)

Offset: 0x000C			Register Name: SCR_FCSR
Bit	**Read/Write**	**Default/Hex**	**Description**
31:11	/	/	/
10	R/W	0x0	RXFIFOFLUSH Flush RX FIFO. RX FIFO is flushed when '1' is written to this bit.
9	R	0x0	RXFIFOFULL RX FIFO Full.
8	R	0x1	RXFIFOEMPTY RX FIFO Empty.
7:3	/	/	/
2	R/W	0x0	TXFIFOFLUSH Flush TX FIFO. TX FIFO is flushed when '1' is written to this bit.
1	R	0x0	TXFIFOFULL TX FIFO Full.
0	R	0x1	TXFIFOEMPTY TX FIFO Empty.

8.13.5.5. Smart Card Reader FIFO Count Register(Default Value: 0x0000_0000)

Offset: 0x0010			Register Name: SCR_FIFOCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R/W	0x0	RXFTH

Offset: 0x0010			Register Name: SCR_FIFOCNT
Bit	**Read/Write**	**Default/Hex**	**Description**
			RX FIFO Threshold These bits set the interrupt threshold of RX FIFO. The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold.
23:16	R/W	0x0	TXFTH TX FIFO Threshold These bits set the interrupt threshold of TX FIFO. The interrupt is asserted when the number of bytes in TX FIFO is equal to or less than the threshold.
15:8	R	0x0	RXFCNT RX FIFO Counter These bits provide the number of bytes stored in the RXFIFO.
7:0	R	0x0	TXFCNT TX FIFO Counter These bits provide the number of bytes stored in the TXFIFO.

8.13.5.6. Smart Card Reader Repeat Control Register(Default Value: 0x0000_0000)

Offset: 0x0014			Register Name: SCR_REPEAT
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:4	R/W	0x0	RXRPT RX Repeat This is a 4-bit register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the error signal during the guard time.
3:0	R/W	0x0	TXRPT TX Repeat This is a 4-bit register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guard time.

8.13.5.7. Smart Card Reader Clock Divisor Register(Default Value: 0x0000_0000)

Offset: 0x0018			Register Name: SCR_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	BAUDDIV Baud Clock Divisor. This 16-bit register defines the divisor value used to generate the Baud Clock impulses from the system clock. $BAUD = \frac{f_{sysclk}}{2 * (BAUDDIV + 1)}$

Offset: 0x0018			Register Name: SCR_CLKDIV
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	SCCDIV Smart Card Clock Divisor. This 16-bit register defines the divisor value used to generate the Smart Card Clock from the system clock. $f_{sccIk} = \frac{f_{sysclk}}{2 * (SCCDIV + 1)}$ f_{sccIk} is the frequency of Smart Card Clock Signal. f_{sysclk} is the frequency of APB Clock.

8.13.5.8. Smart Card Reader Line Time Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: SCR_LTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	ATR ATR Start Limit. This field defines the maximum time between the rising edge of the *scrstn* signal and the start of ATR response. ATR Start Limit = 128* ATR* T_{sccIk} .
15:8	R/W	0x0	RST Reset Duration. This field sets the duration of the Smart Card reset sequence. This value is same for the cold and warm reset. Cold/Warm Reset Duration = 128* RST* T_{sccIk} .
7:0	R/W	0x0	ACT Activation/Deactivation Time. This field sets the duration of each part of the activation and deactivation sequence. Activation/Deactivation Duration = 128* ACT * T_{sccIk} . $T_{sccIk} = \frac{1}{f_{sccIk}}$ is the Smart Card Clock Cycle.

8.13.5.9. Smart Card Reader Character Time Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: SCR_CTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x0	CHARLIMIT Character Limit. This field sets the maximum time between the leading edges of two consecutive characters. The value is ETUs.

Offset: 0x0020			Register Name: SCR_CTIM
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	/	/	/
7:0	R/W	0x0	GUARDTIME Character Guard time. This field sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in ETUs. The parity error is besides signaled during the guard time.

8.13.5.10. Smart Card Reader Line Control Register(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: SCR_PAD
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7	R/W	0x0	DSCVPPPP Direct Smart Card Vpp Pause/Prog. It provides direct access to SCVPPPP output.
6	R/W	0x0	DSCVPPEN Direct Smart Card Vpp Enable. It provides direct access to SCVPPEN output.
5	R/W	0x0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSVPPEN and DSVPPPP signals during activation and deactivation sequence.
4	R/W	0x0	DSCVCC Direct Smart Card VCC. When DIRACCPADS='1', the DSCVCC bit provides direct access to SCVCC pad.
3	R/W	0x0	DSCRST Direct Smart Card Clock. When DIRACCPADS='1', the DSCRST bit provides direct access to SCRST pad.
2	R/W	0x0	DSCCLK Direct Smart Card Clock. When DIRACCPADS='1', the DSCCLK bit provides direct access to SCCLK pad.
1	R/W	0x0	DSCIO Direct Smart Card Input/Output. When DIRACCPADS='1', the DSCIO bit provides direct access to SCIO pad.
0	R/W	0x0	DIRACCPADS Direct Access to Smart Card Pads. When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

8.13.5.11. Smart Card Reader FSM Register(Default Value: 0x0000_0000)

Offset: 0x003C			Register Name: SCR_FSM
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	R	0x0	ATR_Structure_FSM
23:16	R	0x0	ATR_FSM

Offset: 0x003C			Register Name: SCR_FSM
Bit	**Read/Write**	**Default/Hex**	**Description**
15:8	R	0x0	ACT_FSM
7:0	R	0x0	SCR_FSM

8.13.5.12. Smart Card Reader FIFO Data Register(Default Value: 0x0000_0000)

Offset: 0x0100			Register Name: SCR_FIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:8	/	/	/
7:0	R/W	0x0	FIFO_DATA This field provides access to the RX and TX FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer.

8.14. SATA Host

8.14.1. Overview

The SATA/AHCI interface implements the Serial Advanced Technology Attachment (SATA) storage interface for physical storage devices.

Features:

- Supports SATA 1.5Gb/s and SATA 3.0Gb/s
- Compliant with SATA Spec. 2.6, and AHCI Revision 1.3 specifications
- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian
- OOB signaling detection and generation
- SATA 1.5Gb/s and SATA 3.0Gb/s speed negotiation when Tx OON signal is selected
- Supports device hot-plugging
- Supports power management features including automatic Partial to Slumber transition
- Internal DMA engine for command and data transaction
- Supports hardware-assisted Native Command Queuing (NCQ) up to 32 entries
- Supports external SATA (eSATA)

8.14.2. Operations and Functional Descriptions

8.14.2.1. External Signals

Table 8-24 describes the external signals of SATA.

Table 8-24. SATA External Signals

Pin Name	Description	Type
SATA-TXP	TX Differential Output(Positive)	O
SATA-TXM	TX Differential Output(Negative)	O
SATA-RXP	RX Differential Input(Positive)	I
SATA-RXM	RX Differential Input(Negative)	I
SATA-CLKP	External Reference Clock Input(Positive)	I
SATA-CLKM	External Reference Clock Input(Negative)	I

8.14.2.2. Clock Sources

Table 8-25 describes the clock sources of SATA.Users can see **CCU** for clock setting, configuration and gating information.

Table 8-25. SATA Clock Sources

Clock Sources	Description
PLL_SATA	PLL_SATA divided into 100MHz
External Clock Source	Differential clock input from ESCLKP and ESCLKM

8.14.2.3. SATA_AHCI Timing Diagram

Please refer to Serial ATA Specification Rev. 2.6 and Serial ATA Advanced Host Controller Interface (AHCI) Specification Rev. 1.1.

8.15. Keypad

8.15.1. Overview

The keypad interface is used to connect external keypad devices. It can provide up to 8 rows and 8 columns. Key press or key release can be detected to the CPU by an interrupt. To prevent the switching noises, internal debouncing filter is provided.

Features:

- Supports industry-standard AMBA Peripheral Bus (APB) and is fully compliant with the AMBA Specification, Revision 2.0.
- Interrupt for key press or key release
- Internal debouncing filter to prevent the switching noises

8.15.2. Operations and Functional Descriptions

8.15.2.1. External Signals

Table 8-26 describes the external signals of Keypad. For information about General Purpose I/O ports,see **Port Controller** in chapter3.

Table 8-26. Keypad External Signals

Pin Name	Description	Type
KP_IN[7:0]	KEYPAD input	I
KP_OUT[7:0]	KEYPAD output	O

8.15.2.2. Clock Sources

Keypad controller gets two clocks,users can select one of them to make the clock source of Keypad.Table 8-27 describes the clock sources for Keypad.Users can see **CCU** in chapter3 for clock setting,configuration and gating information.

Table 8-27. Keypad Clock Sources

Clock Sources	Description
LOSC	32KHz Crystal
OSC24M	24MHz Crystal

8.15.3. Register List

Module Name	Base Address
KeyPad	0x01C23000

Register Name	Offset	Description
KP_CTL	0x0000	Keypad Control Register

Register Name	Offset	Description
KP_TIMING	0x0004	Keypad Timing Parameter Register
KP_INT_CFG	0x0008	Keypad Interrupt Configure Register
KP_INT_STA	0x000C	Keypad Interrupt Status Register
KP_IN0	0x0010	Keypad Row Input Data Register 0
KP_IN1	0x0014	Keypad Row Input Data Register 1

8.15.4. Register Description

8.15.4.1. Keypad Control Register(Default Value: 0x0000_0000)

Offset: 0x0000			Register Name: KP_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:24	/	/	/
23:16	R/W	0x0	ROW_INPUT_MSK Keypad Row Input Mask When set to '1', the corresponding input is masked.
15:8	R/W	0x0	Keypad Column Output Mask When set to '1', the corresponding output is masked.
7:1	/	/	/
0	R/W	0x0	IF_ENB Keypad Interface Enable 0: Disable 1: Enable

8.15.4.2. Keypad Timing Register(Default Value: 0x0200_0100)

Offset: 0x0004			Register Name: KP_TIMING
Bit	**Read/Write**	**Default/Hex**	**Description**
31:16	R/W	0x200	DBC_CYCLE Keypad Debounce Clock Cycle n It is used for filter switching noises. When row input is low level, the Keypad Interface would delay (n+1) clock to check whether it is still keeping on low level. If it is true, the Keypad Interface would scan the state of the external keypad and get the state into internal registers. After scan, the interrupt is generated if enabled. The value below 0x10 can not be used.
15:0	R/W	0x100	SCAN_CYCLE Keypad Scan Period Clock Cycle n When the Keypad Interface is enabled, it would scan the external keypad in period. The period time is 8*(n+1)/kp_clk. The kp_clk is input clock for Keypad Interface from CCU. The value below 0x10 can't be used.

8.15.4.3. Keypad Interrupt Configure Register(Default Value: 0x0000_0000)

Offset: 0x0008			Register Name: KP_INT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**

Offset: 0x0008			Register Name: KP_INT_CFG
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W	0x0	REDGE_INT_EN Keypad input rising edge (key release) interrupt enable 0: Disable 1: Enable
0	R/W	0x0	FEDGE_INT_EN Keypad input falling edge (key press) interrupt enable 0: Disable 1: Enable

8.15.4.4. Keypad Interrupt Status Register(Default Value: 0x0000_0000)

Offset: 0x000C			Register Name: KP_INT_STA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:2	/	/	/
1	R/W1C	0x0	REDGE_FLAG Keypad input rising edge (key release) interrupt status When it is '1', the key released interrupt occurred. The interrupt is cleared by writing '1'.
0	R/W1C	0x0	FEDGE_FLAG Keypad input falling edge (key press) interrupt status When it is '1', the corresponding pressed interrupt occurred. The interrupt is cleared by writing '1'.

8.15.4.5. Keypad Input Data Register 0(Default Value: 0xFFFF_FFFF)

Offset: 0x0010			Register Name: KP_IN0
Bit	**Read/Write**	**Default/Hex**	**Description**
[8i+7:8i] (i=0~3)	R/W	0xFF	COL_STA0 Keypad row input byte for column n scan (n from 0 to 3)

8.15.4.6. Keypad Input Data Register 1(Default Value: 0xFFFF_FFFF)

Offset: 0x14			Register Name: KP_IN1
Bit	**Read/Write**	**Default/Hex**	**Description**
[8i+7:8i] (i=0~3)	R/W	0xFF	COL_STA1 Keypad row input byte for column n scan (n from 4 to 7)

8.16. OWA

8.16.1. Overview

The OWA interface is one wire audio interface.

Features:

- IEC-60958 transmitter functionality
- Supports S/PDIF Interface
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 32×24 bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

8.16.2. Block Diagram

The OWA provides a serial bus interface for audio data between system. This interface is widely used for consumer audio connect.

Figure 8-35 shows a block diagram of the OWA.

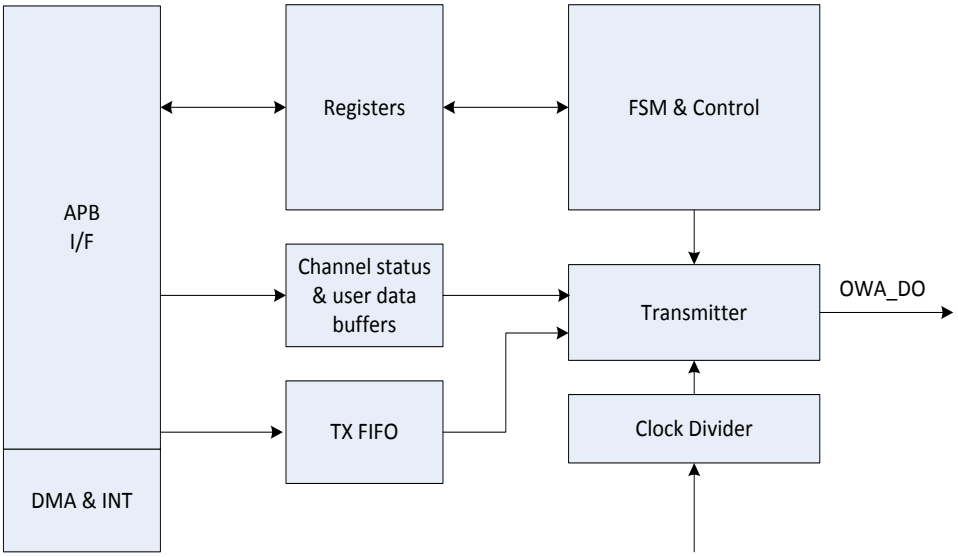


Figure 8-35. OWA Block Diagram

8.16.3. Operations and Functional Descriptions

8.16.3.1. External Signals

OWA is a biphase-mark encoding digital audio transfer protocol. In this protocol, the CLK signal and data signal transfer in the same line. Table 8-28 describes the external signals of OWA. OWA_DO is output pin for output CLK and DATA.

Table 8-28. OWA External Signals

Pin Name	Description	Type
OWA_DO	OWA Output	O
OWA_MCLK	OWA Master Clock	O

8.16.3.2. Clock Sources

Table 8-29 describes the clock sources for OWA. Users can see **CCU** for clock setting, configuration and gating information.

Table 8-29. OWA Clock Sources

Clock Name	Description
PLL_Audio	OWA serial access clock 4x24.576MHz or 4x22.5792MHz from CCU

8.16.3.3. OWA Transmit Format

The OWA supports digital audio data transfer out and receive in. And it supports full-duplex synchronous work mode. Software can set the work mode by the OWA Control Register.

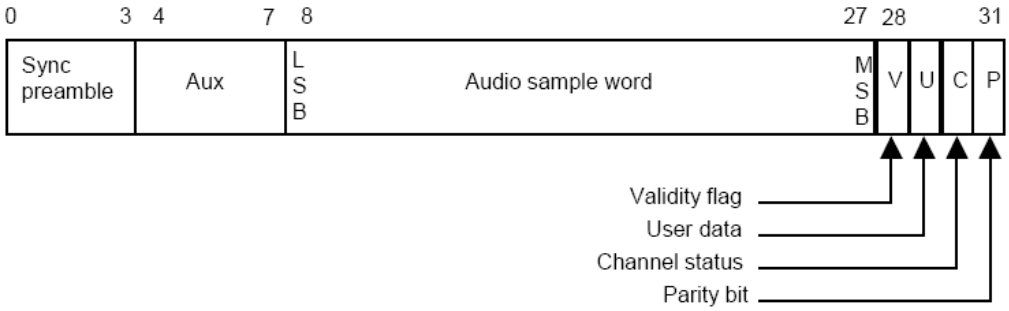


Figure 8-36. OWA Sub-Frame Format

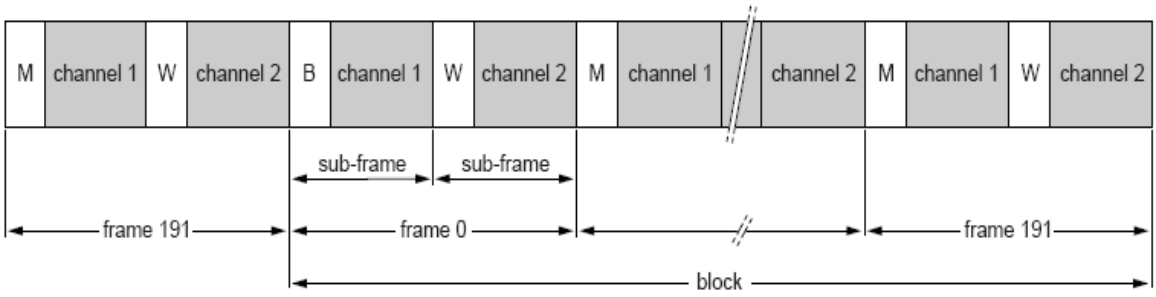


Figure 8-37. OWA Frame/Block Format

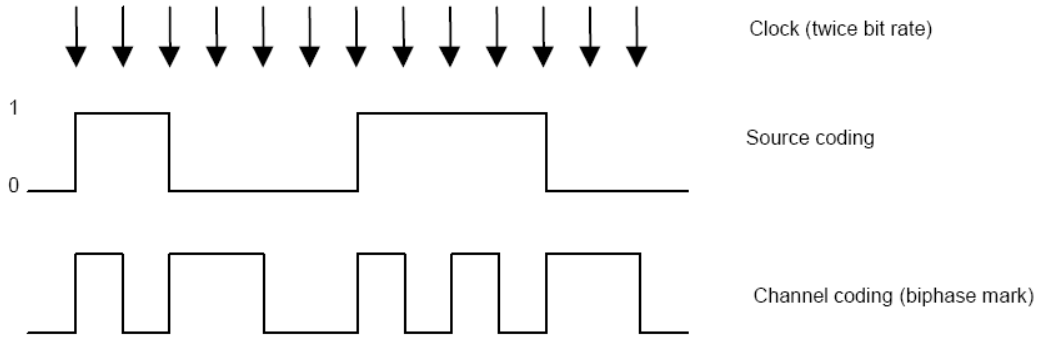


Figure 8-38. OWA Biphase-Mark Encoding

8.16.3.4. Operation Modes

The software operation of the OWA is divided into five steps: system setup, OWA initialization, the channel setup, DMA setup and Enable/Disable module. These five steps are described in detail in the following sections.

(1) System setup and OWA initialization

The first step in the OWA initialization is properly programming the GPIO. Because the OWA port is a multiplex pin. You can find the function in the **Port Controller**. The clock source for the OWA should be followed. At first you must reset the audio PLL in the **CCU**. The second step, you must setup the frequency of the Audio PLL. After that, you must open the OWA gating. At last, you must open the OWA bus gating.

After the system setup, the register of OWA can be setup. At first, you should reset the OWA by writing 1 to the **RST** bit and clear the TX FIFO by writing 1 to **FTX**. After that you should enable the globe enable bit by writing 1 to **GEN** and clear the interrupt and TX counter by the **OWA_ISTA** and **OWA_TX_CNT**.

(2) Channel setup and DMA setup

The OWA supports three methods to transfer the data. The most common way is DMA, the configuration of DMA can be found in the **DMA**. In this module, you just enable the DRQ.

(3) Enable and disable the OWA

To enable the function, you can enable TX by writing the **TX_SINGLE_MODE** . After that, you must enable OWA by writing the **GEN** bit to 1. Writing the **GEN** bit to 0 disable process.

8.16.4. Register List

Module Name	Base Address
OWA	0x01C21000

Register Name	Offset	Description
OWA_CTL	0x0000	OWA General Control
OWA_TX_CFIG	0x0004	OWA TX Configuration Register
OWA_ISTA	0x000C	OWA Interrupt Status Register
OWA_FCTL	0x0014	OWA FIFO Control Register
OWA_FSTA	0x0018	OWA FIFO Status Register

Register Name	Offset	Description
OWA_INT	0x001C	OWA Interrupt Control Register
OWA_TX_FIFO	0x0020	OWA TX FIFO Register
OWA_TX_CNT	0x0024	OWA TX Counter Register
OWA_TX_CHSTA0	0x002C	OWA TX Channel Status Register0
OWA_TX_CHSTA1	0x0030	OWA TX Channel Status Register1

8.16.5. Register Description

8.16.5.1. OWA General Control Register(Default Value: 0x0000_0080)

Offset: 0x0000			Register Name: OWA_CTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:4	R/W	0x08	MCLK_DIV_RATIO mclk divide Ratio Only support 2n divide ratio(n=1~31)
3:2	/	/	/
1	R/W	0x0	GEN Globe Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable
0	R/W1C	0x0	RST Reset 0: Normal 1: Reset *Self clear to 0*

8.16.5.2. OWA TX Configure Register(Default Value: 0x0000_00F0)

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	TX_SINGLE_MODE Tx single channel mode 0: Disable 1: Enable
30:18	/	/	/
17	R/W	0x0	ASS Audio sample select with TX FIFO under run When 0: Sending 0 1: Sending the last audio This bit is only valid in PCM mode.
16	R/W	0x0	TX_AUDIO TX data type

Offset: 0x0004			Register Name: OWA_TX_CFIG
Bit	**Read/Write**	**Default/Hex**	**Description**
			0: Linear PCM (Valid bit of both sub-frame set to 0) 1: Non-audio(Valid bit of both sub-frame set to 1)
15:9	/	/	/
8:4	R/W	0xF	TX_RATIO TX clock divide Ratio Clock divide ratio = TX TATIO +1
3:2	R/W	0x0	TX_SF TX Sample format 00: 16bit 01: 20bit 10: 24bit 11: Reserved
1	R/W	0x0	TX_CHM CHSTMODE 0: Channel status A&B set to 0 1: Channel status A&B generated from TX_CHSTA
0	R/W	0x0	TXEN 0: Disabled 1: Enabled

8.16.5.3. OWA Interrupt Status Register(Default Value: 0x0000_0010)

Offset: 0x000C			Register Name: OWA_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:16	R/W1C	0x0	Reserved
15:7	/	/	/
6	R/W1C	0x0	TXU_INT TX FIFO Under run Pending Interrupt 0: No pending IRQ 1: FIFO under run pending interrupt Write ‘1’ to clear this interrupt.
5	R/W1C	0x0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No pending IRQ 1: FIFO overrun pending interrupt Write ‘1’ to clear this interrupt.
4	R/W1C	0x1	TXE_INT TX FIFO Empty Pending Interrupt 0: No pending IRQ 1: FIFO empty pending interrupt Write ‘1’ to clear this interrupt or automatically clear if interrupt condition fails.
3:2	/	/	/

Offset: 0x000C			Register Name: OWA_ISTA
Bit	**Read/Write**	**Default/Hex**	**Description**
1:0	R/W1C	0x0	Reserved

8.16.5.4. OWA FIFO Control Register(Default Value: 0x0000_1078)

Offset: 0x0014			Register Name: OWA_FCTL
Bit	**Read/Write**	**Default/Hex**	**Description**
31	R/W	0x0	HUB_EN Audio hub enable 0: Disable 1: Enable
30:18	/	/	/
17	R/W1C	0x0	FTX Write '1' to flush TX FIFO, self clear to '0'
16	R/W1C	0x0	Reserved
15:13	/	/	/
12:8	R/W	0x10	TXTL TX FIFO empty Trigger Level Interrupt and DMA request trigger level for TX FIFO normal condition Trigger Level = TXTL
7:3	R/W	0x0F	Reserved
2	R/W	0x0	TXIM TX FIFO Input Mode(Mode0, 1) 0: Valid data at the MSB of OWA_TXFIFO register 1: Valid data at the LSB of OWA_TXFIFO register Example for 20-bits transmitted audio sample: Mode 0: FIFO_I[23:0] = {TXFIFO[31:12], 4'h0} Mode 1: FIFO_I[23:0] = {TXFIFO[19:0], 4'h0}
1:0	R/W	0x0	Reserved

8.16.5.5. OWA FIFO Status Register(Default Value: 0x0000_6000)

Offset: 0x0018			Register Name: OWA_FSTA
Bit	**Read/Write**	**Default/Hex**	**Description**
31:15	/	/	/
14	R	0x1	TXE TX FIFO Empty (indicate FIFO is not full) 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>=1 word)
13:8	R	0x20	TXE_CNT TX FIFO Empty Space Word counter
7	/	/	/
6:0	R	0x0	Reserved

8.16.5.6. OWA Interrupt Control Register(Default Value: 0x0000_0000)

Offset: 0x001C			Register Name: OWA_INT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:19	/	/	/
18:16	R/W	0x0	Reserved
15:8	/	/	/
7	R/W	0x0	TX_DRQ TX FIFO Empty DRQ Enable 0: Disable 1: Enable
6	R/W	0x0	TXUI_EN TX FIFO Underrun Interrupt Enable 0: Disable 1: Enable
5	R/W	0x0	TXOI_EN TX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
4	R/W	0x0	TXEI_EN TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
3	/	/	/
2:0	R/W	0x0	Reserved

8.16.5.7. OWA TX FIFO Register(Default Value: 0x0000_0000)

Offset: 0x0020			Register Name: OWA_TXFIFO
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	W	0x0	TX_DATA Transmitting A, B channel data should be written this register one by one. The A channel data is first and then the B channel data.

8.16.5.8. OWA TX Counter Register(Default Value: 0x0000_0000)

Offset: 0x0024			Register Name: OWA_TX_CNT
Bit	**Read/Write**	**Default/Hex**	**Description**
31:0	R/W	0x0	TX_CNT TX Sample counter The audio sample number of writing into TX FIFO. When one sample is written by DMA or by host IO, the TX sample counter register increases by one. The TX Counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this value.

8.16.5.9. OWA TX Channel Status Register0(Default Value: 0x0000_0000)

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
31: 30	/	/	/
29:28	R/W	0x0	CA Clock Accuracy 00: Level 2 01: Level 1 10: Level 3 11: Not matched
27:24	R/W	0x0	FREQ Sampling frequency 0000: 44.1kHz 0001: not indicated 0010: 48kHz 0011: 32kHz 0100: 22.05kHz 0101: Reserved 0110: 24kHz 0111: Reserved 1000: Reserved 1001: 768kHz 1010: 96kHz 1011: Reserved 1100:176.4kHz 1101: Reserved 1110: 192kHz 1111: Reserved
23:20	R/W	0x0	CN Channel Number
19:16	R/W	0x0	SN Source Number
15:8	R/W	0x0	CC Category code Indicates the kind of equipment that generates the digital audio interface signal.
7:6	R/W	0x0	MODE Mode 00: Default Mode 01~11: Reserved
5:3	R/W	0x0	EMP Emphasis Additional format information For bit 1 = ‘0’, Linear PCM audio mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 µs / 15 µs pre-emphasis 010: Reserved (for 2 audio channels with pre-emphasis) 011: Reserved (for 2 audio channels with pre-emphasis) 100~111: Reserved For bit 1 = ‘1’, other than Linear PCM applications:

Offset: 0x002C			Register Name: OWA_TX_CHSTA0
Bit	**Read/Write**	**Default/Hex**	**Description**
			000: Default state 001~111: Reserved
2	R/W	0x0	CP Copyright 0: copyright is asserted 1: no copyright is asserted
1	R/W	0x0	TYPE Audio Data Type 0: Linear PCM Samples 1: For none-linear PCM audio such as AC3, DTS, MPEG audio
0	R/W	0x0	PRO Application Type 0: Consumer Application 1: Professional Application This bit must be fixed to '0'

8.16.5.10. OWA TX Channel Status Register1(Default Value: 0x0000_0000)

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:10	/	/	/
9:8	R/W	0x0	CGMS_A 00: Copying is permitted without restriction 01: One generation of copies may be made 10: Condition not be used 11: No copying is permitted
7:4	R/W	0x0	ORIG_FREQ Original sampling frequency 0000: Not indicated 0001: 192kHz 0010: 12kHz 0011: 176.4kHz 0100: Reserved 0101: 96kHz 0110: 8kHz 0111: 88.2kHz 1000: 16kHz 1001: 24kHz 1010: 11.025kHz 1011: 22.05kHz 1100: 32kHz 1101: 48kHz 1110: Reserved 1111: 44.1kHz
3:1	R/W	0x0	WL Sample word length

Offset: 0x0030			Register Name: OWA_TX_CHSTA1
Bit	**Read/Write**	**Default/Hex**	**Description**
			For bit 0 = “0”: 000: not indicated 001: 16 bits 010: 18 bits 100: 19 bits 101: 20 bits 110: 17 bits 111: Reserved For bit 0 = “1”: 000: not indicated 001: 20 bits 010: 22 bits 100: 23 bits 101: 24 bits 110: 21 bits 111: Reserved
0	R/W	0x0	MWL Max Word length 0: Maximum audio sample word length is 20 bits 1: Maximum audio sample word length is 24 bits

