AC200 Datasheet

Revision 1.1

Jun.19,2017

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About This Documentation

This documentation is be used by ASIC designers and product software developers. The datasheet assumes that the reader has a background in computer engineering and/or software engineering and understands concepts of digital system design, Audio Video and Ethernet, Input / Output (I/O) devices, industry standard communication and device interface protocols.

Organization

This document aims to describe the AC200 from following aspects: Feature, Block diagram, Pin Assignment, Package Dimension, Electrical Characteristics, Pin Description, Function Description, Register description and Reference.

Revision History

Version	Date	Description
V1.0	Mar.23,2015	Initial Release Version
V1.1	Jun.19,2017	

Table of Contents

Chapter 1 Description

The AC200 is a digital analog mix IC, which use in TV-BOX. It is composed of Audio,Video and EPHY modules.

Audio, communicate with SOC in I2S interface， transform I2S to 2 MIC and 1 Line out

Video, communicate with SOC in CCIR656 interface， transform CCIR656 to Composite Video Broadcast Signal.

EPHY, communicate with SOC in MII/RMII interface, transform to 100M Ethernet.

Chapter 2 Feature

2.1. Audio

- Support One I2S/PCM interface
- Two audio digital-to-analog(DAC) channels
  — 100dB SNR@A-weight
  — Supports DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Two differential microphone inputs
- One lineout output with voltage ramp
- Two audio analog-to-digital(ADC) channels
  — 92dB SNR@A-weight
  — Supports ADC Sample Rates from 8KHz to 48KHz
- Support Automatic Gain Control(AGC) adjusting the ADC recording output

2.2. Video

- Support CCIR656 and Serial YUV interface
- 1 CVBS out, Support NTSC and PAL
- Plug status auto detecting

2.3. EPHY

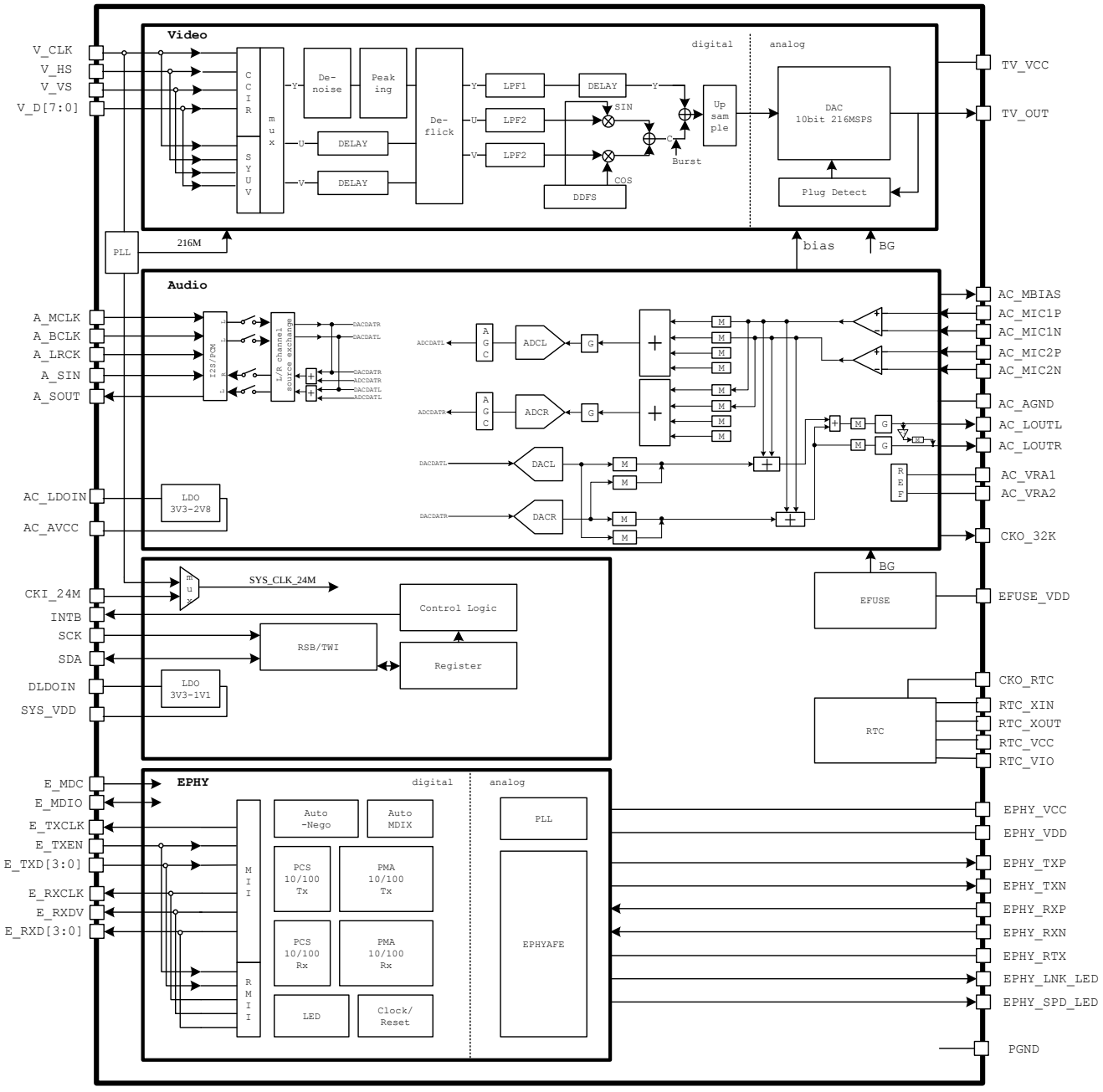
- Support MII and RMII interface
- Fully IEEE 802.3 10/100 Base-TX compliant and supports EEE
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Programmable loopback mode for diagnostic
- Supports WOL (Wake-On-Lan) functionality
- Design for Testability with extensive testability feature and 95% fault coverage
- Power consumption (100Base-TX) less than 140mW

2.4. OTHERS

- TWI/RSB control interface, TWI up to 400Kbps, RSB up to10Mbps
- Integrate Codec LDO, Core LDO, single 3.3V supply for chip
- Internal OSC, 32K clock output
- Internal RTC function
- QFN 68-pin package, 8mm x 8mm

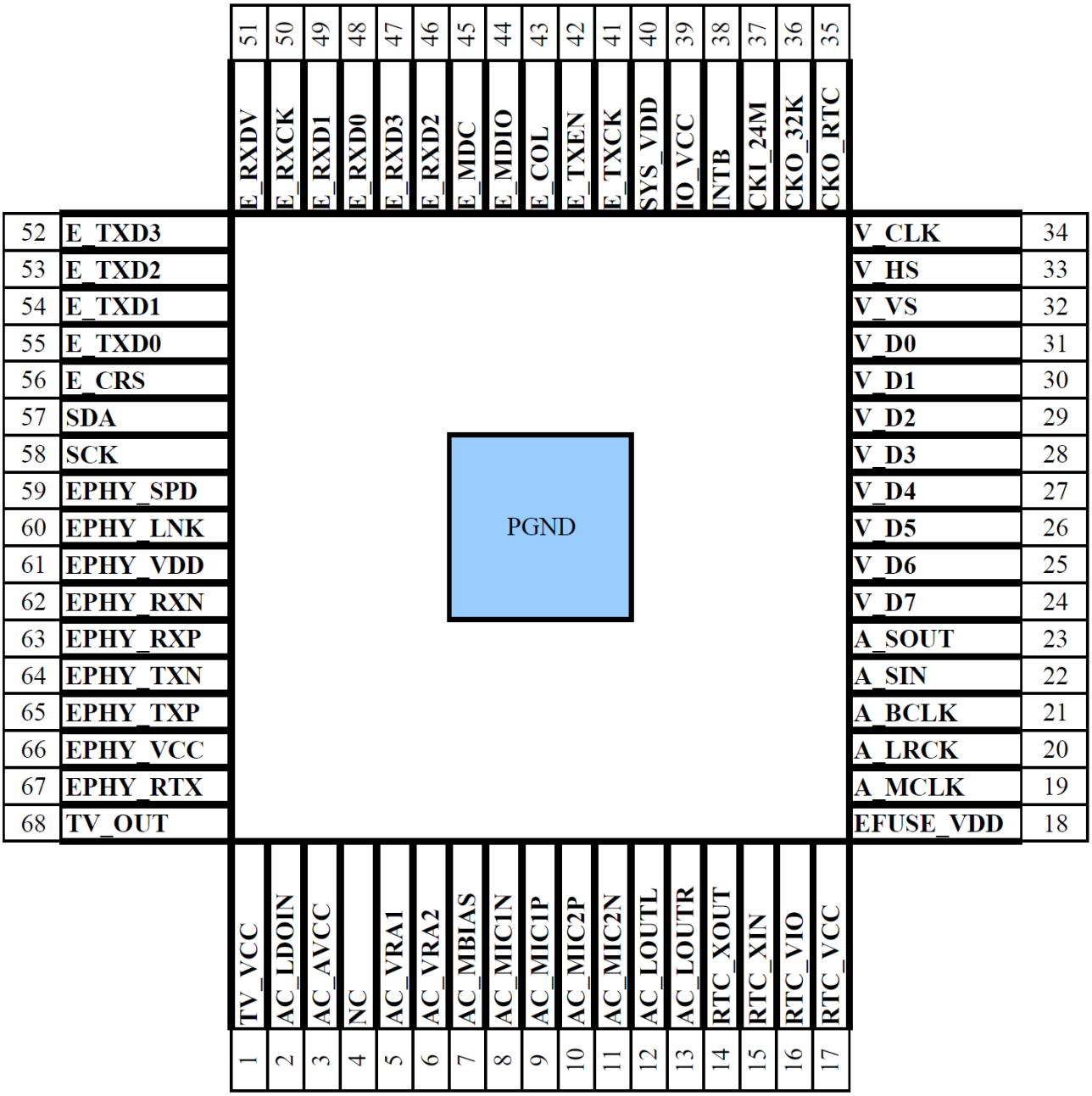
Chapter 3 Block Diagram

AC200 block diagram is as follow:



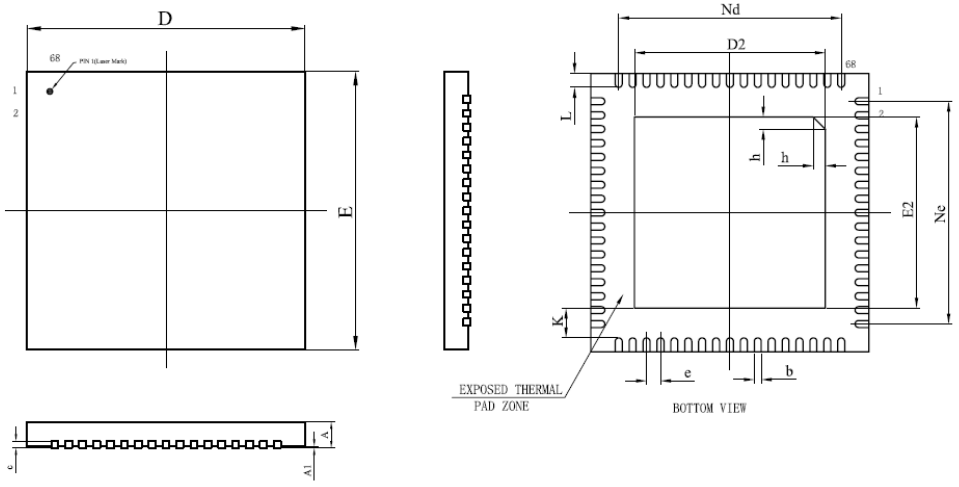
Chapter 4 Pin Assignment

The following figure shows the top views of the 68-pin QFN package.



Chapter 5 Package Dimension

The following diagram shows the package dimension of AC200.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	5.39	5.49	5.59
e	0.40BSC		
Nd	6.40BSC		
E	7.90	8.00	8.10
E2	5.39	5.49	5.59
Ne	6.40BSC		
L	0.35	0.40	0.45
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	240*240		

Chapter 6 Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

Symbol	Parameter	MIN	MAX	Unit
IO_VCC	power for IO	-0.3	3.6	V
SYS_VDD	power for CORE	-0.3	1.2	V
EPHY_VDD	power for EPHY core	-0.3	1.2	V
EPHY_VCC	power for EPHYAFE	-0.3	3.6	V
TV_VCC	power for TVDAC	-0.3	3.6	V
AC_LDOIN	power for CODEC_LDO	-0.3	3.6	V
RTC_VCC	power for RTC	-0.3	3.6	V
T_A	Operating Ambient Temperature	-20	70	℃

6.2. Recommended Operating Conditions

Parameter	Description	MIN	TPY	MAX	Unit
IO_VCC	power for IO	1.7	1.8/3.3	3.4	V
SYS_VDD	power for core	1.0	1.1	1.2	V
EPHY_VDD	power for EPHY core	1.0	1.1	1.2	V
EPHY_VCC	power for EPHYAFE	3.2	3.3	3.4	V
TV_VCC	power for TVDAC	3.2	3.3	3.4	V
AC_LDOIN	power for CODEC_LDO	3.2	3.3	3.4	V
RTC_VCC	power for RTC	3.2	3.3	3.4	V

Chapter 7 Pin Description

Name	Type	QFN68 Pin Number	Description
TV_VCC	P	1	TV analog power
AC_LDOIN	P	2	PLL power input for LDO
AC_AVCC	P	3	ADDA analog VCC power,2.8V
NC	/	4	NC
AU_VRA1	AO	5	ADDA Internal reference voltage
AU_VRA2	AO	6	ADDA Internal reference voltage
AC_MBIAS	AO	7	Master Analog Microphone Bias Voltage Output
AC_MICIN1N	AI	8	Negative differential input for MIC1
AC_MICIN1P	AI	9	Positive differential input for MIC1
AC_MICIN2P	AI	10	Positive differential input for MIC2
AC_MICIN2N	AI	11	Negative differential input for MIC2
AC_LOUTL	AO	12	Left single-end output for LINE-OUT
AC_LOUTR	AO	13	Right single-end output for LINE-OUT
RTC_XOUT	AO	14	RTC XTAL output
RTC_XIN	AI	15	RTC XTAL input
RTC_VIO	P	16	RTC LDO output, 1.2V
RTC_VCC	P	17	RTC power,3.3V
EFUSE_VDD	P	18	SID analog power, 2.5V
A_MCLK	I	19	Audio I2S interface master input clock
A_LRCK	I/O	20	Audio I2S interface synchronous clock
A_BCLK	I/O	21	Audio I2S interface serial bit clock
A_SIN	I	22	Audio I2S interface serial data input
A_SOUT	O	23	Audio I2S interface serial data output
V_D7	I	24	Video CCIR656 interface data7 input
V_D6	I	25	Video CCIR656 interface data6 input
V_D5	I	26	Video CCIR656 interface data5 input
V_D4	I	27	Video CCIR656 interface data4 input
V_D3	I	28	Video CCIR656 interface data3 input
V_D2	I	29	Video CCIR656 interface data2 input
V_D1	I	30	Video CCIR656 interface data1 input
V_D0	I	31	Video CCIR656 interface data0 input
V_VS	I	32	Video CCIR656 interface horizontal sync input
V_HS	I	33	Video CCIR656 interface vertical sync input
V_CLK	I	34	Video CCIR656 interface clock input
CKO_RTC	O	35	RTC 32K clock output
CKO_32K	O	36	OSC 32K clock output
CKI_24M	I	37	System 24M clock input
INTB	O	38	System interrupt output
IO_VCC	P	39	Digital IO power, 3.3V or 1.8V

SYS_VDD	P	40	Digital Core power
E_TXCK	O	41	Ethernet MII interface transmit clock output
E_TXEN	O	42	Ethernet MII interface transmit enable
E_COL	O	43	Ethernet MII interface collision test output
E_MDIO	I/O	44	Ethernet Management data input and output
E_MDC	I	45	Ethernet Management data reference clock input
E_RXD2	O	46	Ethernet MII interface receive data output bit2
E_RXD3	O	47	Ethernet MII interface receive data output bit3
E_RXD0	O	48	Ethernet MII interface receive data output bit0
E_RXD1	O	49	Ethernet MII interface receive data output bit1
E_RXCK	O	50	Ethernet MII interface receive clock output
E_RX_DV	O	51	Ethernet MII interface receive data valid output
E_TXD3	I	52	Ethernet MII interface transmit data input bit3
E_TXD2	I	53	Ethernet MII interface transmit data input bit2
E_TXD1	I	54	Ethernet MII interface transmit data input bit1
E_TXD0	I	55	Ethernet MII interface transmit data input bit0
E_CRS	O	56	Ethernet MII interface carrier sense output
SDA	I/O	57	System TWI interface serial data
SCK	I/O	58	System TWI interface serial clock
EPHY_SPD	I	59	EPHY Speed LED
EPHY_LNK	I	60	EPHY Link/Activity LED
EPHY_VDD	P	61	EPHY Analog 1.1V power for TX/RX
EPHY_RXN	AI/O	62	EPHY Receiver negative output/input
EPHY_RXP	AI/O	63	EPHY Receiver positive output/input
EPHY_TXN	AI/O	64	EPHY Transceiver negative output/input
EPHY_TXP	AI/O	65	EPHY Transceiver positive output/input
EPHY_VCC	P	66	EPHY Analog 3.3V power for TX/RX
EPHY_RTX	AO	67	EPHY External 6K-Ohm resistance to ground
TV_OUT	AO	68	TV output

Chapter 8 Function Description

8.1. Power Sequence

Power on sequence is as follows:

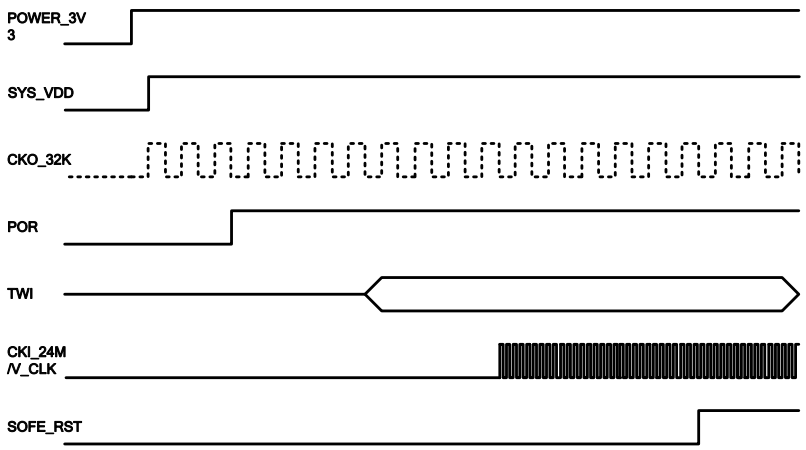


Figure 8-1. AC200 Power On Tree

Power off sequence is as follows:

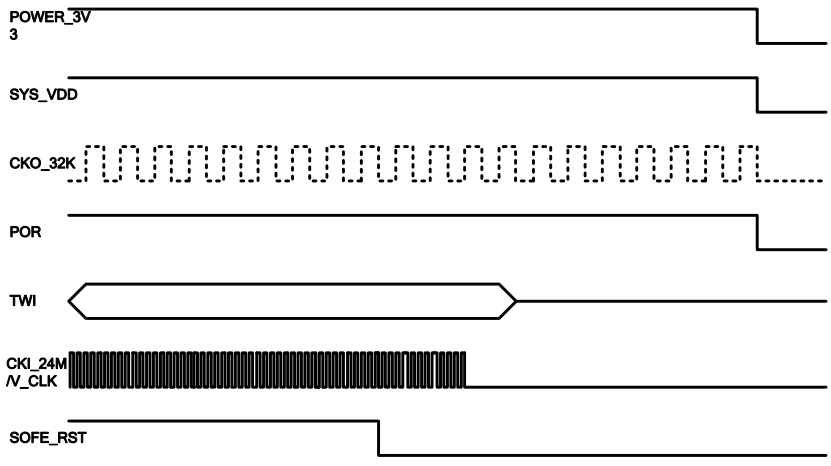


Figure 8-2. AC200 Power Off Tree

8.2. Digital IO

- All digital IO is share one power domain, which is from pin VCC_IO.
- All digital IO support 1.8V and 3.3V
- INTB, CKO_32K, CKO_RTC, TWI_SCK, TWI_SDA is open drain.

8.3. TWI/RSB Interface

AC200 can support two series control interface protocol for writing to or readback from registers on SCK and SDA pins . One is TWI interface, the other is RSB interface. RSB is top-priority for higher efficiency and lower power consumption.

8.3.1. TWI Interface

TWI is a 2-wire (SCK/SDA) half-duplex serial communication interface, supporting only slave mode. SCK is used for clock and SDA is for data. SCK clock supports up to 400 KHz rate and SDA data is a open drain structure.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave address. It is a 7-bit chip address followed by a R/W bit. The chip address must be 0010000x. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCK is high.

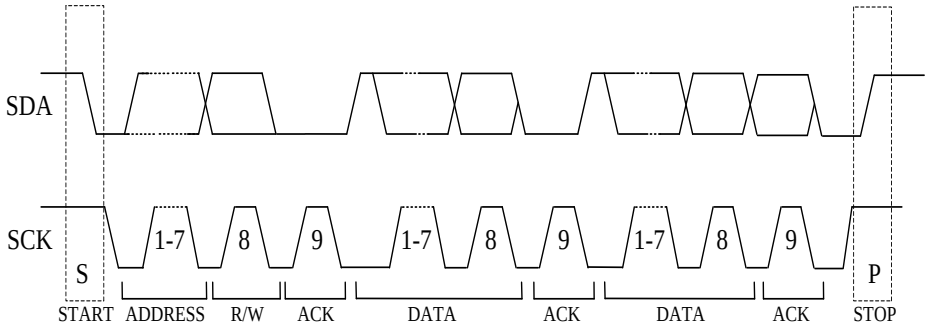


Figure 8-3. TWI Interface

The formats of “write” and “read” instructions are shown in below.

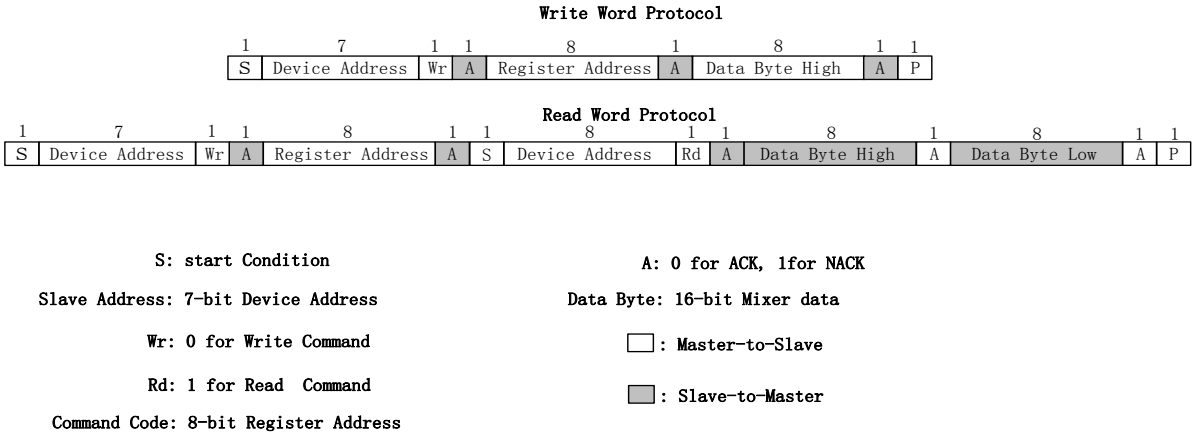


Figure 8-4. TWI Read and Write

8.3.2. RSB Interface

RSB interface supports a special protocol with a simplified two wire protocol on a push-pull bus. So the transfer speed can be up to 10MHz and the performance will be improved much. AC200 works only in slave mode.

RSB support multi-slaves. It uses CK as clock and uses CD to transmit command and data. The Bus Topology is showed as follows:

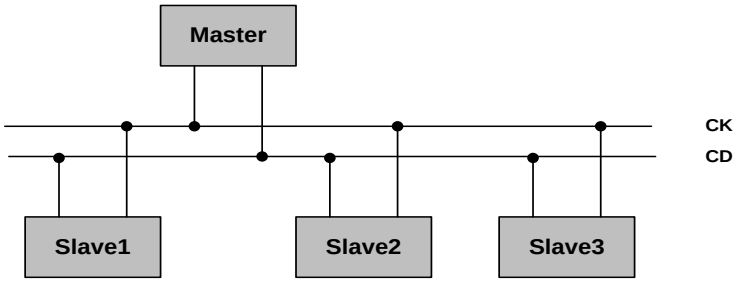


Figure 8-5. RSB Bus Topology

The start bit marks the beginning of a transaction with the slave device. When CK is high, a change from high to low on CD is defined as a start condition. This start condition notifies the selected device to start a transfer.

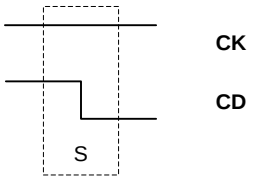


Figure 8-6. Start signal

RSB protocol uses parity bit to check the correction of every byte. The checked object is the 7, 8 or 15 bit in front of the parity bit.

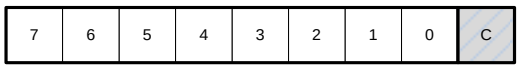


Figure 8-7. Parity bit

ACK bit is the acknowledgement from device to host, The ACK is active low. When device finds the parity bit is error, it will not send ACK to host, so host can know that an error happens in the transaction.

Set run-time slave address(RTSADDR) command. It is used to set run time slave address(RTSADDR) for different devices in the same system. There are 15 devices in a system at most. The RTSADDR can be selected from the command code set and a device 's RTSADDR can be modified many times by using set run-time slave address command.

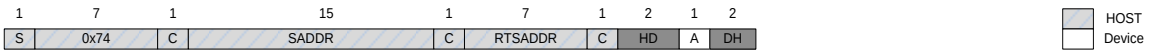


Figure 8-8. RTSADDR command

Read command is used to read data from device. It has byte, half word and word operation. When devices receive the command, they shall check if the command's RTSADDR matches their own RTSADDR. The device's RTSADDR is set by set run-time slave address(RTSADDR) command.

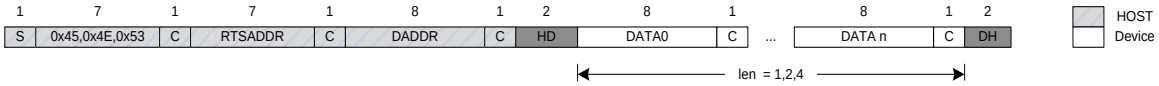


Figure 8-9. Read command

Write command is used to write data to the devices. It has byte, half word and word operation. When devices receive the command, they shall check if the command's RTSADDR matches their own RTSADDR. The device's RTSADDR is set by set run-time slave address(RTSADDR) command.

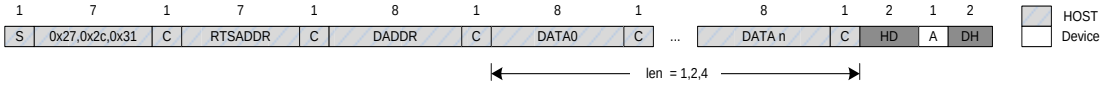


Figure 8-10. Write command

8.4. Audio CODEC

8.4.1. Typical Performance

Test Conditions:

SYS-VDD=1.1V, IO-VCC= 3.3V, AVCC=2.8V, TA=25℃, 1KHz sinusoid signal, fs = 48KHz, Input PGA gain = 0dB, 20-bit audio data unless otherwise stated.

Items	PARAMETER	Test Conditions	MIN	TYP	MAX	UNIT
DAC Path	DAC to LINEOUTL or LINEOUTR(R=10kΩ)					
	Fullscale	0dBFS 1KHz		0.9		Vrms
	SNR@A	0dB 1KHz		100		dB
	THD+N	0dB 1KHz		-80		dB
	Crosstalk	0dB 1KHz		75		dB
	Noise Floor	0data A-weighted		7		uVrms
ADC Path	MIC1 to ADC via ADC mixer					
	SNR@A	2.4Vpp 1KHz 0dB		92		dB
	THD+N	2.4Vpp 1KHz 0dB		-80		dB

	SNR@A	30mV 1KHz 24dB		81		dB
	THD+N	30mV 1KHz 24dB		-76		dB
	SNR@A	30mV 1KHz 30dB		81		dB
	THD+N	30mV 1KHz 30dB		-76		dB
	SNR@A	10mV 1KHz 42dB		73		dB
	THD+N	10mV 1KHz 42dB		-72		dB
	Crosstalk			80		dB
	Noise Floor			7		uVrms
	MIC2 to ADC via ADC mixer					
	SNR@A	2.4Vpp 1KHz 0dB		92		dB
	THD+N	2.4Vpp 1KHz 0dB		-65		dB
	SNR@A	30mV 1KHz 24dB		81		
	THD+N	30mV 1KHz 24dB		-77		dB
	SNR@A	30mV 1KHz 30dB		83		dB
	THD+N	30mV 1KHz 30dB		-77		dB
	SNR@A	30mV 1KHz 42dB		73		dB
	THD+N	30mV 1KHz 42dB		-71		dB
	Crosstalk			80		dB
	Noise Floor			7		uVrms
	LINEINL or LINEINR to ADC via ADC mixer					
	FullScale	2.4Vpp 1KHz 0dB		0.8		Vrms
	SNR@A	2.4Vpp 1KHz 0dB		92		dB
	THD+N	2.4Vpp 1KHz 0dB		81		dB
	Crosstalk			80		dB
	Noise Floor			7		uVrms
AA path	LINEIN to LINEOUT via output mixer					
	Fullscale	2.4Vpp 1KHz 0dB		0.8		Vrms
	SNR@A	2.4Vpp 1KHz 0dB		95		dB
	THD+N	2.4Vpp 1KHz 0dB		91		dB
	CrossTalk			80		dB

8.4.2. Power Domain

The AVCC is provided to ADC/DAC analog part. SYS_VDD is provided to ADC/DAC digital part and all the register.

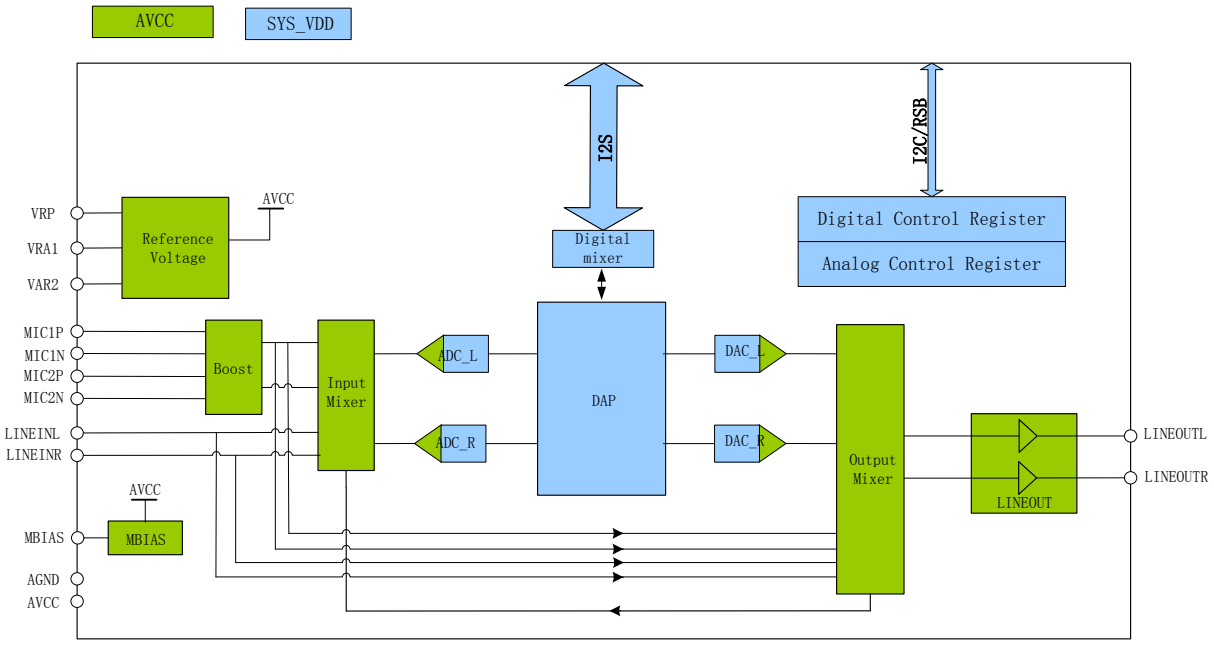


Figure 8-11. Power Domain

8.4.3. Clock System

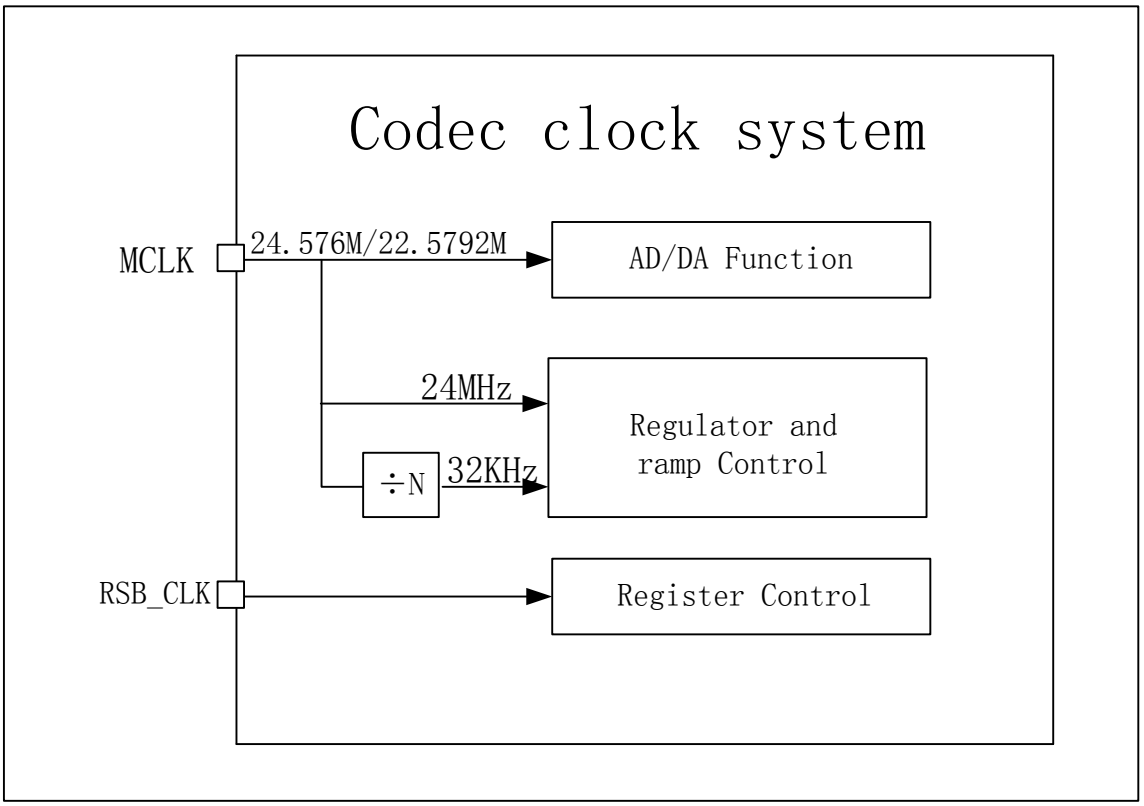


Figure 8-12. Audio clock tree

8.4.4. Audio Codec Reset

When AVCC power on , the reset circuit will send a rising edge signal named AVCC_POR, which goes through the level shift and RC filter, then it will be sent to ADDA Logic Core to reset the audio analog part.

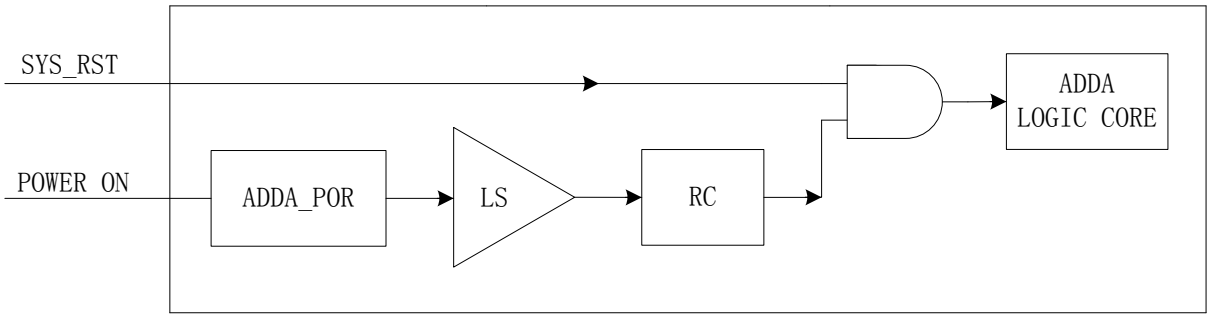


Figure 8-13. Audio CODEC Analog Reset

8.4.5. Data Path Diagram

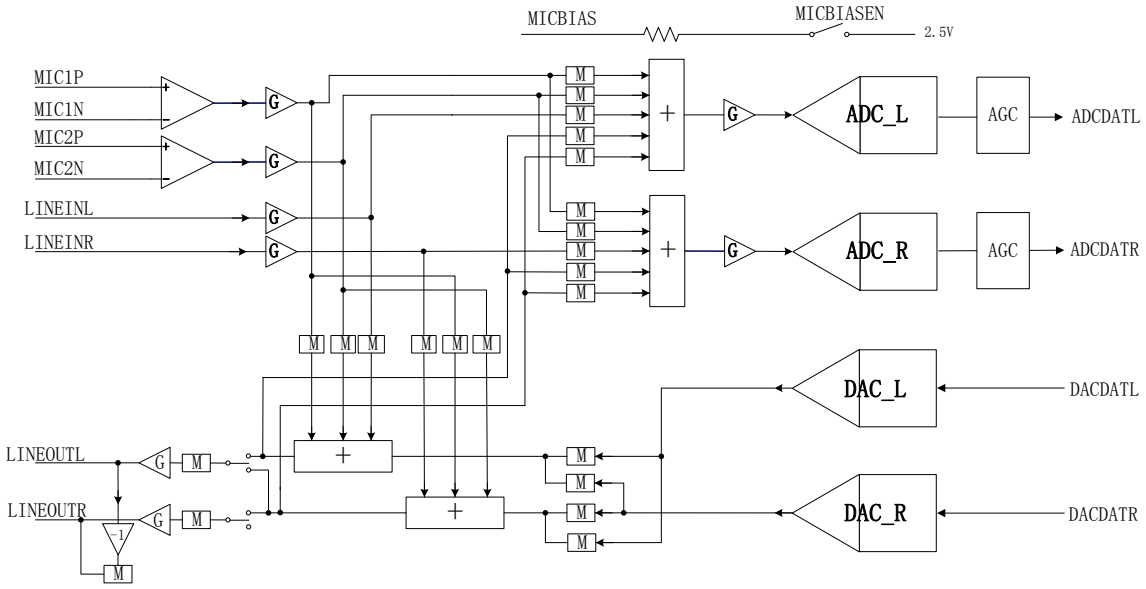


Figure 8-14. Analog Data Path Diagram

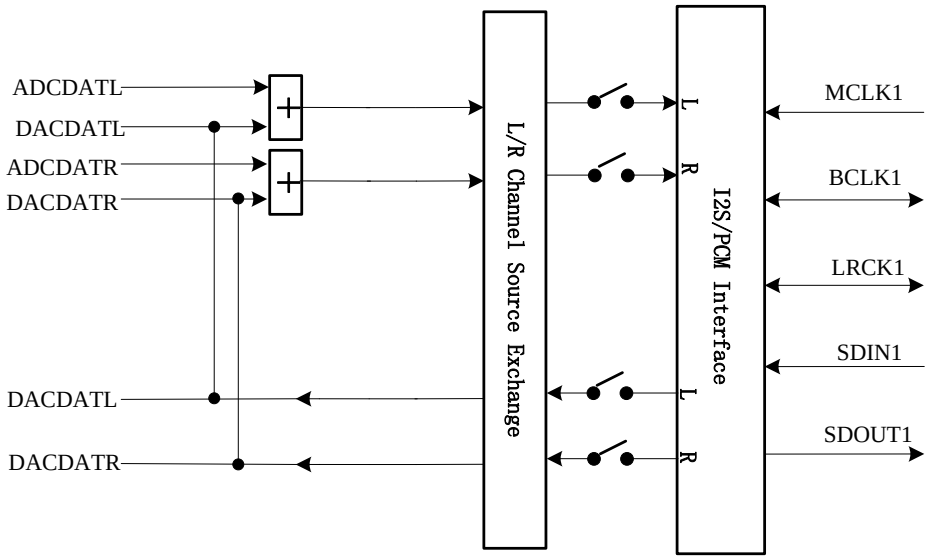


Figure 8-15. Digital Data Path Diagram

8.4.6. Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC is independent of DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting register AC_ADC_ACTRL.

The volume control of the stereo ADC is set via register AC_ADC_ACTRL.

8.4.7. Stereo DAC

The stereo DAC can be configured to different sample rate by setting the register. In order to save power, the left and right DAC can be powered down separately by setting register AC_DAC_ACTRL.

8.4.8. Analogue Mixer

The Codec supports two mixers for all function requirements: LINEOUT mixer and ADC record mixer

8.4.9. Analogue inputs and outputs

The Codec has two types analog input ports: microphone input and line input.

The Codec has one type analog output ports: LINEOUT output.

8.4.10. Microphone BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external

components.

8.4.11. Interrupt

The Codec has one interrupt. it has two interrupt source, such as DAC FIFO IRQ and ADC FIFO IRQ.

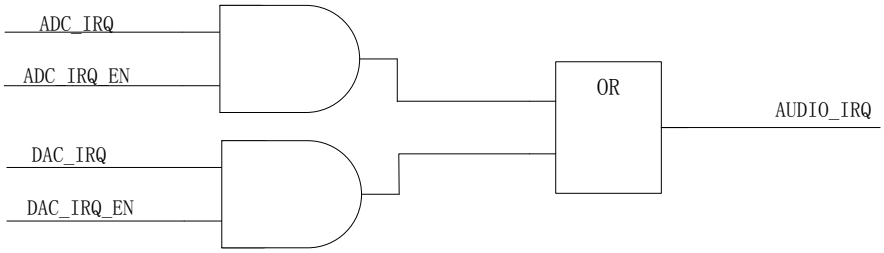


Figure 8-16. Interrupt System

8.5. TV Encoder

8.5.1. Typical Performance

No.	Test Item	Test Signal	Test Condition	Index Requirement	Unit	Typ
1	Video output level	Cbar75（75％ color bar）or CCITT033.ts L35 Matrx625.mpg，L28	Peak-to-peak (p-p)	1000±10%	mV	1000
			Luminance level	700±20	mV	700
			Horizontal synchronization level	300±10	mV	300
			Color synchronization level	300±10	mV	300
2	Luminance non-linear	CCIR 17 or CCITT033.TS，L35 or Matrx625.Trp，L36 Matrx625.mpg，L28	1st order	100≤±4	%	100
			2nd order	100≤±4	%	97.6
			3rd order	100≤±4	%	99.8
			4th order	100≤±4	%	99.0
			5th order	100≤±4	%	98.7
3	Luminance gain		Δ τ	100≤±5	%	102.0
4	Bright delay		Δ t	≤30	nS	3.0
5	K coefficient		K-2T	≤3	%	0.5
			K-PB	≤3	%	0.2
6	Short time distortion		The proportion of Upper/Lower punches	20	%	8.0

			Up/Down time	300	nS	197.5
7	Chroma noise ratio AM/PM	CCITT033.TS，L25 or Matrx625.Trp，L178	AM	≥50	dB	70
			PM	≥50	dB	60
8	Differential Gain(DG)	Modulated five-step wave or CCITT033 L612 Matrx625.mpg，L58	dG	≤±3	%	0.80
9	Differential Phase(DP)		dP	≤±3°	0	0.80
10	SNR(S/N)	CCITT033，L44 Matrx625.mpg，L 229	Non-weighting	≥52	dB	56
			Weighting	≥56	dB	60
11	Chroma non-linear	CCIR 331 or Matrx625.Trp，L84	Color gain error	≤±3	%	2.0
			Color phase error	≤±3°	0	0.0
			Color and Luminance intermodulation	≤±5	%	0.0
12	Amplitude-frequency characteristics	CCIR 18 or Matrx625.Trp，L105 Matrx625.mpg，L105	0.5MHz	≤±0.5	dB	0.10
			1.0MHz	≤±0.5	dB	0.10
			2.0MHz	≤±0.5	dB	0.15
			4.0MHz	≤±0.5	dB	0.15
			4.8MHz	≤±1	dB	0.20
			5.8MHz	-3～0.5	dB	0.20
13	Line synchronizationfront-end dither	Arbitrarily video signal	Jitter	≤20nSp-p	nS	3
14	Line Phase of subcarrier		SCH Phase	≤±10	0	0.5

8.5.2. Block Diagram

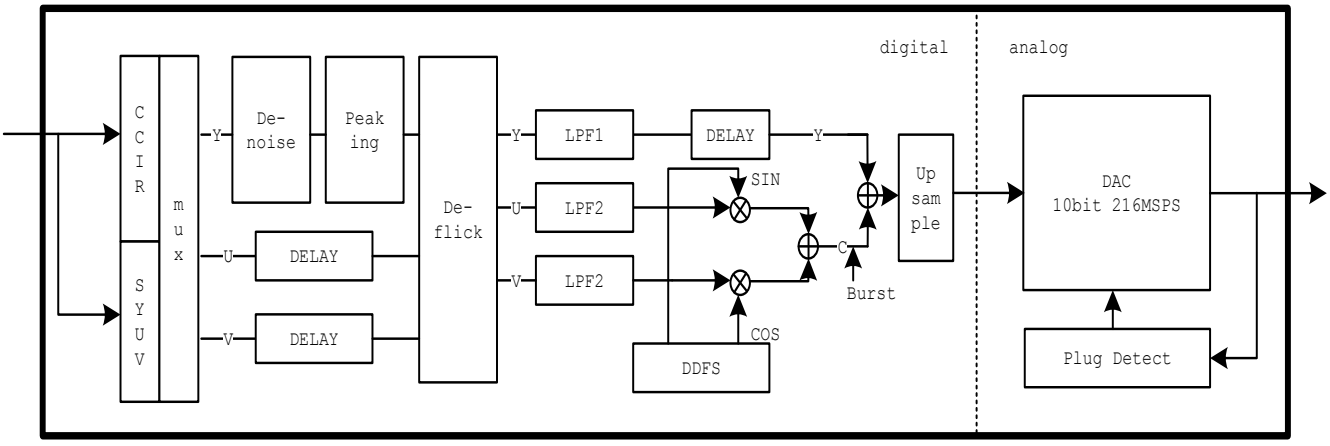


Figure 8-17. TV Encoder Block Diagram

8.5.3. CCIR656 Interface

In AC200, CCIR656 supports 8 bits format. The video timing reference codes are as follows:

Data bit number	First word (FF)	Second word (00)	Third word (00)	Forth word (XY)
7(MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0(LSB)	1	0	0	P0

F = 0 during filed 1

= 1 during filed 2

V = 0 elsewhere

= 1 during filed blanking

H = 0 in SAV

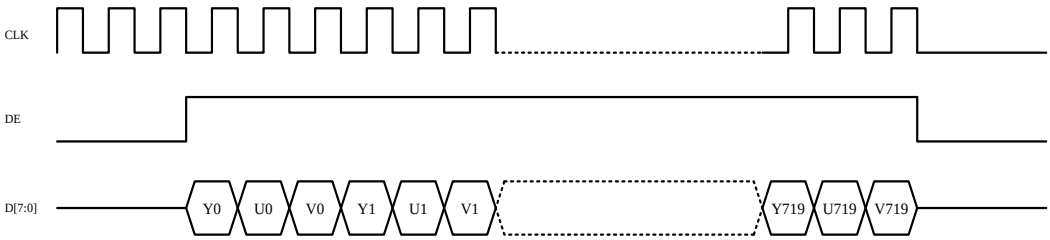
= 1 in EAV

P0, P1, P2, P3: protection bits

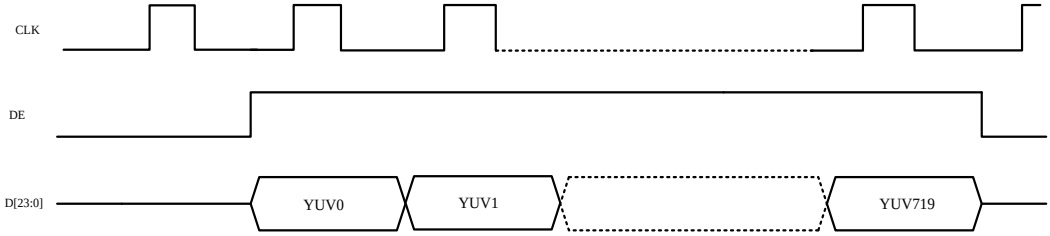
In AC200, TV Encoder required Parallel YUV data with DE signal and RESYNC signal. There is 2 modes to generate DE signal and RESYNC signal.

8.5.4. Serial YUV Interface

- Internal H and V are generated the same as CCIR656 SYNC mode
- YUV serial data format is as follows.



Serial YUV Horizontal Timing

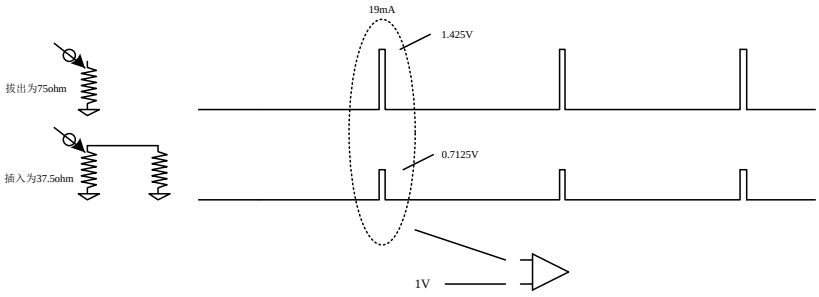


Parallel YUV Horizontal Timing

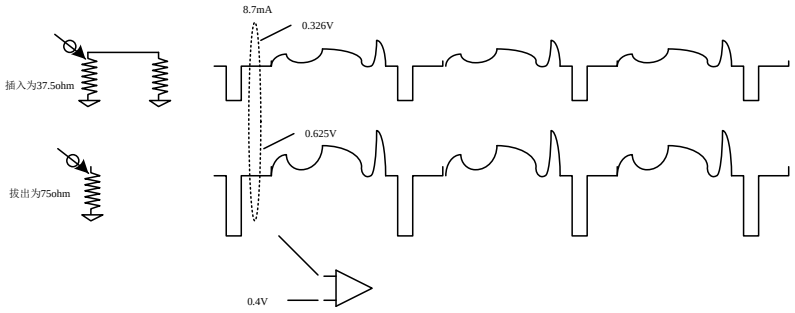
Figure 8-18. Serial YUV Interface Timing

8.5.5. Plug detect

DAC plug status detect block diagram is as follows.



Plug detect at no CVBS output



Plug detect at CVBS output

Figure 8-19. DAC Plug Detect Block Diagram

8.6. Fast Ethernet PHY

8.6.1. Features

- SMIC 40nm logic Low Leakage Process
- Power Supply: 1.1V and 3.3V
- Minimum metal requirement: 7 metal layers
- Operating Temperature: -40_C_125_C
- Power consumption (100Base-TX) less than 140mW
- Fully IEEE 802.3 10/100 Base-TX compliant and supports EEE
- Capable to support length up to 120m in 100Base-TX for UTP CAT 5 cables
- Integrated MDI termination resistors
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Supports MII and RMII interfaces
- Auto polarity correction in 10Base-T
- Design for Testability with extensive testability feature and 95% fault coverage
- Supports Auto-MDIX function for Plug-n-Play
- Programmable loopback mode for diagnostic
- Supports programmable LED output for different applications and power on LED Self-Test
- Supports 24M/25M/27M REFCLK clock sources
- Supports WOL (Wake-On-Lan) functionality

8.7. RTC

8.7.1. Power

RTC power is independent from other power. RTC analog circuit use RTC-VCC power. RTC digital circuit use RTC-VIO power, which is from RTC internal LDO. The LDO input is also RTC-VCC.

8.7.2. Reset and clock

RTC reset and clock is independent from core. RTC clock can from internal OSC 16M or external XTAL.

Chapter 9 Register Description

9.1. Memory Mapping

TWI Slave Address	0x10
RSB Slave Address	0x09cc

Module	Address	Size
SYSTEM	0000H - 1FFFH	8K
AUDIO	2000H - 3FFFH	8K
TVE	4000H - 5FFFH	8K
EPHY	6000H - 7FFFH	8K
EFUSE	8000H - 9FFFH	8K
RTC	A000H - BFFFH	8K

9.2. TWI Register List

Register Name	Address	Description
TWI_CHANGE_RSB	XX3EH	TWI change to RSB address Register
TWI_PAD_DELAY	XXC4H	TWI/RSB pad delay Register
TWI_REG_ADDR_H	XXFEH	TWI/RSB register address high Register

9.3. TWI Register Description

9.3.1. XX3Eh TWI change to RSB address Register

Default: 0x0000			Register Name: TWI_CHANGE_RSB
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0	Write this register ‘7c’to change TWI into RSB Write this register others to change RSB into TWI

9.3.2. XXC4h TWI/RSB pad delay Register

Default: 0x0000			Register Name: TWI_PAD_DELAY
Bit	**Read/Write**	**Default**	**Description**
15:3	R/W	0	
2:0	R/W	0	PAD delay set

9.3.3. XXFEh TWI/RSB register address high Register

Default: 0x0000			Register Name: TWI_REG_ADDR_H
Bit	**Read/Write**	**Default**	**Description**
15:8	/	/	/
7:0	R/W	0	ADDR_H

9.4. System Register List

Register Name	Address	Description
SYS_VERSION	0000h	System Version Register
SYS_CONTROL	0002h	System Control Register
SYS_IRQ_ENABLE	0004h	System IRQ Enable Register
SYS_IRQ_STATUS	0006h	System IRQ Status Register
SYS_CLK_CTL	0008h	System Clock Control Register
SYS_DLDO_OSC_CTL	000Ah	System DLDO and OSC Control Register
SYS_PLL_CTL0	000Ch	System PLL Control 0 Register
SYS_PLL_CTL1	000Eh	System PLL Control 1 Register
SYS_AUDIO_CTL0	0010h	System AUDIO Control 0 Register
SYS_AUDIO_CTL1	0012h	System AUDIO Control 1 Register
SYS_EPHY_CTL0	0014h	System EPHY Control 0 Register
SYS_EPHY_CTL1	0016h	System EPHY Control 1 Register
SYS_TVE_CTL0	0018h	System TVE Control 0 Register
SYS_TVE_CTL1	001Ah	System TVE Control 1 Register

9.5. System Register Description

9.5.1. 0000h System Version Register

Default: 0x0101			Register Name: SYS_VERSION
Bit	**Read/Write**	**Default**	**Description**
15:14	R	0x0	CHIP_PACKAGE 0 : QFN68 Others : Reserved
13:12	/	/	/
11:0	R	0x101	CHIP_VERSION

9.5.2. 0002h System Control Register

Default: 0x0000			Register Name: SYS_CONTROL
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/

0	R/W	0	CHIP_RESET 0：reset all register to their default state. 1：reset invalid

9.5.3. 0004h System IRQ Enable Register

Default: 0x0000			**Register Name: SYS_IRQ_ENABLE**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	INTB_OUTPUT_ENABLE 0：INTB pin disable 1：INTB pin output
14	R/W	0	INTB_OUTPUT_CFG 0 : Default high level, any irq status with irq enable is '1', set INBT output low level 1 : Default low level, any irq status with irq enable is '1' , set INBT output high level
13	/	/	/
12	R/W	0	RTC_IRQ_ENABLE 0：IRQ is disable 1：IRQ is enable
11:9	/	/	/
8	R/W	0	EPHY_IRQ_ENABLE 0：IRQ is disable 1：IRQ is enable
7:5	/	/	/
4	R/W	0	TVE_IRQ_ENABLE 0：IRQ is disable 1：IRQ is enable
3:1	/	/	/
0	/	/	/

9.5.4. 0006h System IRQ Status Register

Default: 0x0000			**Register Name: SYS_IRQ_STATUS**
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12	R	0	RTC_IRQ_ STATUS 0：IRQ is waiting 1：IRQ is pending
11:9	/	/	/
8	R	0	EPHY_IRQ_ STATUS 0：IRQ is waiting 1：IRQ is pending
7:5	/	/	/

4	R	0	TVE_IRQ_STATUS 0：IRQ is waiting 1：IRQ is pending
3:1	/	/	/
0	/	/	/

9.5.5. 0008h System Clock Control Register

Default: 0x0000			**Register Name: SYS_CLK_CTL**
Bit	**Read/Write**	**Default**	**Description**
15:6	/	/	/
5	R/W	0	Reserved
4	R/W	0	SYS_CLK_SEL 0：SYS_CLK from CKI_24M_PIN 1：SYS_CLK from PLL_CKO_DIV
3	/	/	/
2	R/W	1	CKI_24M_ENABLE 0：CKI_24M PIN disable 1：CKI_24M PIN input
1	R/W	1	CKO_RTC_ENABLE 0：CKO_RTC PIN disable 1：CKO_RTC PIN output CKO_RTC is from RTC 32.768K
0	R/W	1	CKO_32K_ENABLE 0：CKO_32K PIN disable 1：CKO_32K PIN output CKO_32K is from ADDA_OSC 32K

9.5.6. 000Ah System DLDO OSC Control Register

Default: 0xC80C			**Register Name: SYS_ DLDO_OSC_CTL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x1	DLDOEN Digital LDO enable 0: disable; 1: enable
14:12	R/W	0x4	DLDOVOL DLDO Voltage select 000: 0.825V 001: 0.880V, 010: 0.943V 011: 1.015V 100: 1.1V 101: 1.2V

			110: 1.32V 111: 1.467V
11	R/W	0x1	Reserved
10	R/W	0x0	Reserved
9:4	R/W	0x0	/
3	R/W	0x1	OSCEN 32K oscillator enable 0: disable; 1: enable
2:0	R/W	0x4	OSCSEL Oscillator frequency select

9.5.7. 000Ch System PLL Control 0 Register

Default: 0x0200			**Register Name: SYS_PLL_CTL0**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	PLL_ENABLE 0: disable 1: enable The PLL Output cko = (ccir_clk/M)*N The PLL Output cko_div = The PLL Output / PLL_POST_DIV
14	R/W	0	PLL_BIAS_EN Mbias enable 0: disable 1: enable
13:12	/	/	/
11	R/W	0	PLL_LDO1_EN On-chip LDO1 enable 0: disable 1: enable
10	R/W	0	PLL_LDO_EN On-chip LDO enable 0: disable 1: enable
9	R/W	1	PLL_POST_DIV PLL post div factor 0: div 8 1: div 9
8:4	/	/	/
3:0	R/W	0	PLL_PRE_DIV_M PLL pre-divider control bit

9.5.8. 000Eh System PLL Control 1 Register

Default: 0x014A	**Register Name: SYS_PLL_CTL1**

Bit	Read/Write	Default	Description
15:0	/	/	Reserved

9.5.9. 0010h System AUDIO Control 0 Register

Default: 0x0000			Register Name: SYS_AUDIO_CTL0
Bit	**Read/Write**	**Default**	**Description**
15:2	/	/	/
1	R/W	0	AC_MCLK_GATING 0：Clock is gating 1：Clock is enable
0	R/W	0	AC_RESET_INVALID 0：Reset 1：Reset Invalid

9.5.10. 0012h System AUDIO Control 1 Register

Default: 0x0000			Register Name: SYS_AUDIO_CTL1
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/
0	R/W	0	AC_I2S_IO_EN 0：all I2S io is disable 1：I2S

9.5.11. 0014h System EPHY Control 0 Register

Default: 0x0000			Register Name: SYS_EPHY_CTL0
Bit	**Read/Write**	**Default**	**Description**
15:4	/	/	/
3:2	/	/	/
1	R/W	0	EPHY_SYSCLK_GATING 0：Clock is OFF 1：Clock is ON
0	R/W	0	EPHY_RESET_INVALID 0：Reset 1：Reset Invalid

9.5.12. 0016h System EPHY Control 1 Register

Default: 0x0000			Register Name: SYS_EPHY_CTL1
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	Reserved

14	R/W	0	Reserved
13:1	/	/	/
3	R/W	0	E_DPX_LED_IO_EN 0 : E_DPX_LED io is disable 1 : E_DPX_LED io is enable
2	R/W	0	E_SPD_LED_IO_EN 0 : E_SPD_LED io is disable 1 : E_SPD_LED io is enable
1	R/W	0	E_LNK_LED_IO_EN 0 : E_LNK_LED io is disable 1 : E_LNK_LED io is enable
0	R/W	0	EPHY_MII_IO_EN 0：all MII io is disable,include FE_TEST_MDI and FE_TEST_MDO 1：MII

9.5.13. 0018h System TVE Control 0 Register

Default: 0x0000			**Register Name: SYS_TVE_CTL0**
Bit	**Read/Write**	**Default**	**Description**
15:4	/	/	/
3	R/W	0	TVE_SYSCLK_GATING 0：Clock is gating 1：Clock is enable
2	R/W	0	TVE_SCLK_GATING(PLL_216M) 0：Clock is gating 1：Clock is enable
1	R/W	0	TVE_DCLK_GATING(CCIR_CLK) 0：Clock is gating 1：Clock is enable
0	R/W	0	TVE_RESET_INVALID 0：Reset 1：Reset Invalid

9.5.14. 001Ah System TVE Control 1 Register

Default: 0x0000			**Register Name: SYS_TVE_CTL1**
Bit	**Read/Write**	**Default**	**Description**
15:2	/	/	/
1	R/W	0	TVE_CCIR_CLK_IO_EN 0：IO ccir_clk is disable 1：IO ccir_clk is enable
0	R/W	0	TVE_CCIR_SYNC_DATA_IO_EN 0：IO ccir_hs,ccir_vs,ccir_data is disable 1：IO ccir_hs,ccir_vs,ccir_data is enable

9.5.15. 0040h System PLL Debug Register

Default: 0x0702			Register Name: SYS_PLL_DEBUG
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	PLL_BANDWIDTH_SEL
14:8	R/W	7	PLL_FACTOR_N
7	/	/	/
6:4	R/W	0	PLL_VSET On-chip LDO output voltage control hv_is_33 1 0 0 : 1.1 1.325 1 : 1.13 1.355 2 : 1.16 1.39 3 : 1.19 1.425 4 : 1.22 1.46 5 : 1.255 1.5 6 : 1.29 1.545 7 : 1.325 1.585
3:2	/	/	/
1	R/W	1	PLL_HV_IS_33 pll input power select 0 : 2.5V power 1 : 3.3V power
0	/	/	/

9.5.16. 0050h System Bandgap Control Register

Default: 0x0400			Register Name: SYS_BG_CTL
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0	Reserved

9.6. AC Register List

Register Name	Offset	Description
SYS_CLK_CTL	0x0000	System Clock Control Register
SYS_MOD_RST	0x0002	System Module Reset Control Register
SYS_SAMP_CTL	0x0004	System Sample Rate Control Register
I2S_CTL	0x0100	I2S Control Register
I2S_CLK	0x0102	I2S Clock Register
I2S_FMT0	0x0104	I2S Format 0 Register
I2S_FMT1	0x0108	I2S Format 1 Register
I2S_MIX_SRC	0x0114	I2S Digital Mixer Source Select Register
I2S_MIX_GAIN	0x0116	I2S Digital Mixer Gain Select Register

I2S_DACDAT_DVC	0x0118	I2S DACDAT Volume Control Register
I2S_ADCDAT_DVC	0x011A	I2S ADCDAT Volume Control Register
AC_DAC_DPC	0x0200	DAC Digital Part Control Register
AC_DAC_MIX_SRC	0x0202	DAC Digital Input Mixer Source Select Register
AC_DAC_MIX_GAIN	0x0204	DAC Digital Input Mixer Gain Select Register
DACA_OMIXER_CTRL	0x0220	DAC & Output Mixer Analog Control Register
OMIXER_SR	0x0222	Output Mixer Source Select Register
LINEOUT_CTRL	0x0224	Lineout Control Register
AC_ADC_DPC	0x0300	ADC Digital Part Control Register
MBIAS_CTRL	0x0310	MICBIAS Control Register
ADC_MIC_CTRL	0x0320	ADC & MIC Control Register
ADCMIXER_SR	0x0322	ADC Mixer Source Control Register
ANALOG_TUNING0	0x032A	Bias Control Register
ANALOG_TUNING	0x032C	Analog performance tuning Control Register
AC_AGC_SEL	0x0480	ADC DAP Function Selected Register
AC_ADC_DAPLCTRL	0x0500	ADC DAP Left Channel Control Register
AC_ADC_DAPRCTRL	0x0502	ADC DAP Right Channel Control Register
AC_ADC_DAPLSTA	0x0504	ADC DAP Left Status Register
AC_ADC_DAPRSTA	0x0506	ADC DAP Right Status Register
AC_ADC_DAPLTL	0x0508	ADC DAP Left Target Level Register
AC_ADC_DAPRTL	0x050A	ADC DAP Right Target Level Register
AC_ADC_DAPLHAC	0x050C	ADC DAP Left High Average Coef Register
AC_ADC_DAPLLAC	0x050E	ADC DAP Left Low Average Coef Register
AC_ADC_DAPRHAC	0x0510	ADC DAP Right High Average Coef Register
AC_ADC_DAPRLAC	0x0512	ADC DAP Right Low Average Coef Register
AC_ADC_DAPLDT	0x0514	ADC DAP Left Decay Time Register
AC_ADC_DAPLAT	0x0516	ADC DAP Left Attack Time Register
AC_ADC_DAPRDT	0x0518	ADC DAP Right Decay Time Register
AC_ADC_DAPRAT	0x051A	ADC DAP Right Attack Time Register
AC_ADC_DAPNTH	0x051C	ADC DAP Noise Threshold Register
AC_ADC_DAPLHNAC	0x051E	ADC DAP Left Input Signal High Average Coef Register
AC_ADC_DAPLLNAC	0x0520	ADC DAP Left Input Signal Low Average Coef Register
AC_ADC_DAPRHNAC	0x0522	ADC DAP Right Input Signal High Average Coef Register
AC_ADC_DAPRLNAC	0x0524	ADC DAP Right Input Signal Low Average Coef Register
AC_DAPHHPFC	0x0526	ADC DAP High HPF Coef Register
AC_DAPLHPFC	0x0528	ADC DAP Low HPF Coef Register
AC_DAPOPT	0x052A	ADC DAP Optimum Register
AC_DAC_DAPCTRL	0x1000	DAC DAP Channel Control Register
AC_DRC_HHPFC	0x1002	DRC High HPF Coef Register
AC_DRC_LHPFC	0x1004	DRC Low HPF Coef Register
AC_DRC_CTRL	0x1006	DRC Control Register
AC_DRC_LPFHAT	0x1008	DRC Left Peak Filter High Attack Time Coef Register
AC_DRC_LPFLAT	0x100A	DRC Left Peak Filter Low Attack Time Coef Register
AC_DRC_RPFHAT	0x100C	DRC Right Peak Filter High Attack Time Coef Register

AC_DRC_RPFLAT	0x100E	DRC Peak Filter Low Attack Time Coef Register
AC_DRC_LPFHRT	0x1010	DRC Left Peak Filter High Release Time Coef Register
AC_DRC_LPFLRT	0x1012	DRC Left Peak Filter Low Release Time Coef Register
AC_DRC_RPFHRT	0x1014	DRC Right Peak filter High Release Time Coef Register
AC_DRC_RPFLRT	0x1016	DRC Right Peak filter Low Release Time Coef Register
AC_DRC_LRMSHAT	0x1018	DRC Left RMS Filter High Coef Register
AC_DRC_LRMSLAT	0x101A	DRC Left RMS Filter Low Coef Register
AC_DRC_RRMSHAT	0x101C	DRC Right RMS Filter High Coef Register
AC_DRC_RRMSLAT	0x101E	DRC Right RMS Filter Low Coef Register
AC_DRC_HCT	0x1020	DRC Compressor Threshold High Setting Register
AC_DRC_LCT	0x1022	DRC Compressor Threshold High Setting Register
AC_DRC_HKC	0x1024	DRC Compressor Slope High Setting Register
AC_DRC_LKC	0x1026	DRC Compressor Slope Low Setting Register
AC_DRC_HOPC	0x1028	DRC Compressor High Output at Compressor Threshold Register
AC_DRC_LOPC	0x102A	DRC Compressor Low Output at Compressor Threshold Register
AC_DRC_HLT	0x102C	DRC Limiter Theshold High Setting Register
AC_DRC_LLT	0x102E	DRC Limiter Theshold Low Setting Register
AC_DRC_HKl	0x1030	DRC Limiter Slope High Setting Register
AC_DRC_LKl	0x1032	DRC Limiter Slope Low Setting Register
AC_DRC_HOPL	0x1034	DRC Limiter High Output at Limiter Threshold
AC_DRC_LOPL	0x1036	DRC Limiter Low Output at Limiter Threshold
AC_DRC_HET	0x1038	DRC Expander Threshold High Setting Register
AC_DRC_LET	0x103A	DRC Expander Threshold Low Setting Register
AC_DRC_HKE	0x103C	DRC Expander Slope High Setting Register
AC_DRC_LKE	0x103E	DRC Expander Slope Low Setting Register
AC_DRC_HOPE	0x1040	DRC Expander High Output at Expander Threshold
AC_DRC_LOPE	0x1042	DRC Expander Low Output at Expander Threshold
AC_DRC_HKN	0x1044	DRC Linear Slope High Setting Register
AC_DRC_LKN	0x1046	DRC Linear Slope Low Setting Register
AC_DRC_SFHAT	0x1048	DRC Smooth Filter Gain High Attack Time Coef Register
AC_DRC_SFLAT	0x104A	DRC Smooth Filter Gain Low Attack Time Coef Register
AC_DRC_SFHRT	0x104C	DRC Smooth Filter Gain High Release Time Coef Register
AC_DRC_SFLRT	0x104E	DRC Smooth Filter Gain Low Release Time Coef Register
AC_DRC_MXGHS	0x1050	DRC MAX Gain High Setting Register
AC_DRC_MXGLS	0x1052	DRC MAX Gain Low Setting Register
AC_DRC_MNGHS	0x1054	DRC MIN Gain High Setting Register
AC_DRC_MNGLS	0x1056	DRC MIN Gain Low Setting Register
AC_DRC_EPSHC	0x1058	DRC Expander Smooth Time High Coef Register
AC_DRC_EPSLC	0x105A	DRC Expander Smooth Time Low Coef Register
AC_DRC_HPFHGAIN	0x105E	DRC HPF Gain High Coef Register
AC_DRC_HPFLGAIN	0x1060	DRC HPF Gain Low Coef Register
AC_DRC_BISTCR	0x1100	DRC Bist Control Register
AC_DRC_BISTST	0x1102	DRC Bist Status Register

9.7. AC Register Description

9.7.1. 2000h System Clock Control Register

Default: 0x0000			Register Name: SYS_CLK_CTL
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	Module clock enable control 0-Clock disable 1-Clock enable BIT15-I2S BIT14-Reserved BIT13-Reserved BIT12-Reserved BIT11-Reserved BIT10-Reserved BIT9-Reserved BIT8-Reserved BIT7-HPF & AGC BIT6-HPF & DRC BIT5-Reserved BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

9.7.2. 2002h System Module Reset Control Register

Default: 0x0000			Register Name: SYS_MOD_RST
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0	Module Reset control 0-Reset asserted 1-Reset de-asserted BIT15-I2S BIT14-Reserved BIT13-Reserved BIT12-Reserved BIT11-Reserved BIT10-Reserved BIT9-Reserved BIT8-Reserved BIT7-HPF & AGC BIT6-HPF & DRC

			BIT5-Reserved BIT4-Reserved BIT3-ADC Digital BIT2-DAC Digital BIT1-Reserved BIT0-Reserved

9.7.3. 2004h System Sample Rate Control Register

Default: 0x0000			**Register Name: SYS_SAMP_CTL**
Bit	**Read/Write**	**Default**	**Description**
3:0	R/W	0x0	SYS_FS System Sample Rate Control 0000: 8KHz 0001: 11.025KHz 0010: 12KHz 0011: 16KHz 0100: 22.05KHz 0101: 24KHz 0110: 32KHz 0111: 44.1KHz 1000: 48KHz 1001: 96KHz 1010: 192KHz Other: Reserved

9.7.4. 2100h I2S Control Register

Default: 0x0000			**Register Name: I2S_CTL**
Bit	**Read/Write**	**Default**	**Description**
15:4	/	/	/
3	R/W	0	SDO0_EN 0: Disable, Hi-Z state 1: Enable
2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Globe Enable

			A disable on this bit overrides any other block or channel enables. 0: Disable 1: Enable

9.7.5. 2102h I2S Clock Register

Default: 0x0000			**Register Name: I2S_CLK**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	BCLK_OUT 0: input 1: output
14	R/W	0	LRCK_OUT 0: input 1: output
13:10	R/W	0	BCLKDIV BCLK Divide Ratio from PLL2 0: reserved 1: Divide by 1 2: Divide by 2 3: Divide by 4 4: Divide by 6 5: Divide by 8 6: Divide by 12 7: Divide by 16 8: Divide by 24 9: Divide by 32 10: Divide by 48 11: Divide by 64 12: Divide by 96 13: Divide by 128 14: Divide by 176 15: Divide by 192
9:0	R/W	0	LRCK_PERIOD It is used to program the number of BCLKs per channel of sample frame. This value is interpreted as follow: PCM mode: Number of BCLKs within (Left + Right) channel width I2S / Left-Justified / Right-Justified mode: Number of BCLKs within each individual channel width (Left or Right) N+1 For example: n = 7: 8 BCLK width … n = 1023: 1024 BCLKs width

9.7.6. 2104h I2S Format 0 Register

Default: 0x0000			Register Name: I2S_FMT0
Bit	**Read/Write**	**Default**	**Description**
15:14	R/W	0	MODE_SEL Mode Selection 0: PCM mode (offset 0: DSP_B; offset 1: DSP_A) 1: Left mode (offset 0: LJ mode; offset 1: I2S mode) 2: Right-Justified mode 3: Reserved
13:12	/	/	/
11:10	R/W	0	TXn_OFFSET TXn offset tune, TXn data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
9:8	R/W	0	RX_OFFSET RX offset tune, RX data offset to LRCK 0: no offset n: data is offset by n BCLKs to LRCK
7	/	/	/
6:4	R/W	0	SR Sample Resolution 0: Reserved 1: 8-bit 2: 12-bit 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit
3:1	R/W	0	SW Slot Width Select 0: Reserved 1: 8-bit 2: 12-bit 3: 16-bit 4: 20-bit 5: 24-bit 6: 28-bit 7: 32-bit
0	R/W	0	LOOP Loop back test 0: Normal mode 1: Loop back test

			When set '1', connecting the SDO0 with the SDI

9.7.7. 2108h I2S Format 1 Register

Default: 0x0300			**Register Name: I2S_FMT1**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	BCLK_POLARITY 0: normal mode, negative edge drive and positive edge sample 1: invert mode, positive edge drive and negative edge sample
14	R/W	0	LRCK_POLARITY When apply in I2S / Left-Justified / Right-Justified mode: 0: Left channel when LRCK is low 1: Left channel when LRCK is high When apply in PCM mode: 0: PCM LRCK asserted at the negative edge 1: PCM LRCK asserted at the positive edge
13	R/W	0	EDGE_TRANSFER 0: SDO drive data and SDI sample data at the different BCLK edge 1: SDO drive data and SDI sample data at the same BCLK edge BCLK_POLARITY = 0, use negative edge BCLK_POLARITY = 1, use positive edge
12	/	/	/
11	R/W	0	RX MLS MSB / LSB First Select 0: MSB First 1: LSB First
10	R/W	0	TX MLS MSB / LSB First Select 0: MSB First 1: LSB First
9:8	R/W	3	SEXT Sign Extend in slot [sample resolution < slot width] 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position 2: Reserved 3: Transfer 0 after each sample in each slot
7:5			
4	R/W	0	LRCK_WIDTH (only apply in PCM mode) LRCK width 0: LRCK = 1 BCLK width (short frame) 1: LRCK = 2 BCLK width (long frame)
3:2	R/W	0	RX_PDM PCM Data Mode 0: Linear PCM

			1: reserved 2: 8-bits u-law 3: 8-bits A-law
1:0	R/W	0	TX_PDM PCM Data Mode 0: Linear PCM 1: reserved 2: 8-bits u-law 3: 8-bits A-law

9.7.8. 2114h I2S Digital Mixer Source Select Register

Default: 0x0000			**Register Name: I2S_MIX_SRC**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:12	R/W	0x0	I2S_MIXL_SRC I2S ADCDAT left channel mixer source select 0: Disable 1:Enable Bit13: I2S_ DACDATL Bit12: ADCDATL
11:10	/	/	/
9:8	R/W	0x0	I2S_MIXR_SRC I2S ADCDAT Right channel mixer source select 0: Disable 1:Enable Bit9: I2S_ DACDATR Bit8: ADCR
7:0	/	/	/

9.7.9. 2116h I2S Digital Mixer Gain Select Register

Default: 0x0000			**Register Name: I2S_MIX_GAIN**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:12	R/W	0x0	I2S_MIXL_SRC I2S ADCDAT left channel mixer gain control 0: 0dB 1: -6dB Bit13: I2S_ DACDATL Bit12: ADCDATL
11:10	/	/	/
9:8	R/W	0x0	I2S_MIXR_SRC I2S ADCDAT Right channel mixer gain control 0: 0dB 1: -6dB Bit9: I2S_ DACDATR

			Bit8: ADCR
7:0	/	/	/

9.7.10. 2118h I2S DACDAT Volume Control Register

Default: 0xA0A0			**Register Name: I2S_DACDAT_DVC**
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	I2S_DACDAT_VOL_L I2S DACDAT left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …… 0xFF = 71.25dB
7:0	R/W	0xA0	I2S_DACDAT_VOL_R I2S DACDAT Right channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …… 0xFF = 71.25dB

9.7.11. 211Ah I2S ADCDAT Volume Control Register

Default: 0xA0A0			**Register Name: I2S_ADCDAT_DVC**
Bit	**Read/Write**	**Default**	**Description**
15:8	R/W	0xA0	I2S_ADCDAT_VOL_L I2S ADCDAT left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB

			0xA1 = 0.75dB …… 0xFF = 71.25dB
7:0	R/W	0xA0	I2S_ADCDAT_VOL_L I2S ADCDAT left channel volume (-119.25dB To 71.25dB, 0.75dB/Step) 0x00: Mute 0x01: -119.25dB …… 0x9F = -0.75dB 0xA0 = 0dB 0xA1 = 0.75dB …… 0xFF = 71.25dB

9.7.12. 2200h DAC Digital Part Control Register

Default: 0x0000			**Register Name: AC_DAC_DPC**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ENDA. DAC Digital Part Enable 0: Disabe 1: Enable
14	R/W	0x0	ENHPF HPF Function Enable 0: Enable 1: Disable
13	R/W	0x0	DAFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12	R/W	0x0	Reserved
11:8	R/W	0x0	MODQU Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
7:0	R/W	0x0	Reserved

9.7.13. 2202h DAC Digital Input Mixer Source Select Register

Default: 0x0000			**Register Name: AC_DAC_MIX_SRC**
Bit	**Read/Write**	**Default**	**Description**

15:14	/	/	/
13:12	R/W	0x0	DACL_MXR_SRC DAC left channel mixer source select 0: Disable 1:Enable Bit13: I2S_ DACDATL Bit12: ADCDATL
11:10	/	/	/
9:8	R/W	0x0	DACR_MXR_SRC DAC right channel mixer source select 0: Disable 1:Enable Bit9: I2S_ DACDATR Bit8: ADCR
7:0	/	/	/

9.7.14. 2204h DAC Digital Input Mixer Gain Select Register

Default: 0x0000			**Register Name: AC_DAC_MIX_GAIN**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:12	R/W	0x0	DACL_MXR_SRC DAC left channel mixer source select 0: 0dB 1: -6dB Bit13: I2S_ DACDATL Bit12: ADCDATL
11:10	/	/	/
9:8	R/W	0x0	DACR_MXR_SRC DAC right channel mixer source select 0: 0dB 1: -6dB Bit9: I2S_ DACDATR Bit8: ADCR
7:0	/	/	/

9.7.15. 2220h DAC & Output Mixer Analog Control Register

Default: 0x0333			**Register Name: DACA_OMIXER_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	DACAREN Internal DAC Analog Right channel Enable 0: Disable; 1: Enable
14	R/W	0x0	DACALEN Internal DAC Analog Left channel Enable 0: Disable; 1: Enable

13	R/W	0x0	RMIXEN Right analog output MIXer Enable 0: Disable; 1: Enable
12	R/W	0x0	LMIXEN Left analog output MIXer Enable 0: Disable; 1: Enable
11	R/W	0x0	/
10:8	R/W	0x3	LINEING, (volln) LINEINL/R to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
7	R/W	0x0	/
6:4	R/W	0x3	MIC1G, (volm1) MIC1 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	/
2:0	R/W	0x3	MIC2G, (volm2) MIC2 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

9.7.16. 2222h Output Mixer Source Select Register

Default: 0x0000			**Register Name: OMIXER_SR**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	/
14:8	R/W	0x0	RMIXMUTE Right output MIXer MUTE control 0: Mute; 1: On Bit14: MIC1 boost stage Bit13: MIC2 boost stage Bit12: PHONEN-PHONEP Bit11: PHONEP Bit10: LINEINR Bit9: DACR Bit8: DACL
7	R/W	0x0	/
6:0	R/W	0x0	LMIXMUTE Left output MIXer MUTE control 0: Mute; 1: On Bit6: MIC1 boost stage Bit5: MIC2 boost stage Bit4: PHONEN-PHONEP Bit3: PHONEN Bit2: LINEINL

			Bit1: DACL Bit0: DACR

9.7.17. 2224h Lineout Control Register

Default: 0x0120			Register Name: LINEOUT_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	LINEOUTEN Right & Left LINEOUT Enable 0-disable 1-enable
14	R/W	0x0	Line-out Left Select 0-not select 1-selected
13	R/W	0x0	Line-out Right Select 0-not select 1-selected
12	R/W	0x0	Left line-out source select 0-left output mixer 1-left output mixer + right output mixer
11	R/W	0x0	Right line-out source select 0-right output mixer 1-left line-out, for differential output
10	R/W	0x0	LINEOUT_SLOPE_SELECT LINEOUT slope select cosine or ramp 0: select cosine 1: select ramp
9:8	R/W	0x1	LINEOUT_SLOPE_LENGTH_CTRL, (slopelengthsel) LINEOUT Anti-pop slope time Control 00:131ms; 01: 262ms; 10: 393ms; 11:524ms
7:5	R/W	0x1	ANTI_POP_CTRL, (antipoplengthsel) LINEOUT Anti-pop time Control 000:131ms; 001: 262ms; 010: 393ms; 011:524ms 100:655ms; 101: 786ms; 110: 917ms; 111:1048ms
4:0	R/W	0x0	LINEOUTVOL Line-out Volume Control, Total 31 level, from 0dB to -48dB, 1.5dB/step, mute when 00000 & 00001

9.7.18. 2300h ADC Digital Part Control Register

Default: 0x0000			Register Name: AC_ADC_DPC
Bit	**Read/Write**	**Default**	**Description**

15	R/W	0x0	ENAD ADC Digital part enable 0: Disable 1: Enable
14	R/W	0x0	ENDM Digital microphone enable 0: Analog ADC mode 1: Digital microphone mode
13	R/W	0x0	ADFIR32 Enable 32-tap FIR filter 0: 64-tap 1: 32-tap
12:4	R/W	0x0	Reserved
3:2	R/W	0x0	ADOUT_DTS ADC Delay Time For transmitting data after ENAD 00:5ms 01:10ms 10:20ms 11:30ms
1	R/W	0x0	ADOUT_DLY ADC Delay Function enable for transmitting data after ENAD 0: Disable 1: Enable
0	R/W	0x0	Reserved

9.7.19. 2310h MICBIAS Control Register

Default: 0x6100			**Register Name: MBIAS_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	MMICBIASEN Master Microphone Bias enable 0: disable, 1: enable
14	R/W	0x1	MMIC BIAS chopper enable 0: disable; 1:enable
13:12	R/W	0x2	MMIC BIAS chopper clock select 00: 250KHz; 01: 500KHz; 10: 1MHz; 11: 2MHz
11:10	R/W	0x0	/
9:8	R/W	0x1	MBIASSEL MMICBIAS voltage level select 00: 1.88V 01: 2.09V 10: 2.33V 11: 2.50V

7:0	R/W	0x0	/

9.7.20. 2320h ADC & MIC Control Register

Default: 0x0344			Register Name: ADC_MIC_CTRL
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	ADCREN ADC Right Channel Enable 0-Disable; 1-Enable
14	R/W	0x0	ADCLEN ADC Left Channel Enable 0-Disable; 1-Enable
13:11	R/W	0x0	/
10:8	R/W	0x3	ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB
7	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0-Disable; 1-Enable
5:4	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB
3	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0-Disable; 1-Enable
2:0	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

9.7.21. 2322h ADC Mixer Source Control Register

Default: 0x0000			Register Name: ADCMIXER_SR
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x0	/
14:8	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control: 0: Mute; 1:On Bit 14: MIC1 Boost stage Bit 13: MIC2 Boost stage Bit 12: PHONEP-PHONEN Bit 11: PHONEP

			Bit 10: LINEINR Bit 9: Right output mixer Bit 8: Left output mixer
7	R/W	0x0	/
6:0	R/W	0x0	LADCMIXMUTE Left ADC Mixer Mute Control: 0-Mute, 1-Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEN Bit 2: LINEINL Bit 1: Left output mixer Bit 0: Right output mixer

9.7.22. 232Ah Bias Control Register

Default: 0x8900			**Register Name: ANALOG_TUNING0**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0x1	ALDOEN Analog LDO enable 0: disable; 1: enable
14:12	R/W	0x0	/
11	R/W	0x1	DITHER ADC dither on/off control 0: dither off; 1: dither on
10	R/W	0x0	/
9:8	R/W	0x1	DITHER_CLK_SELECT ADC dither clock select 00: ADC FS * (8/9), about 43KHz when FS=48KHz 01: ADC FS * (16/15), about 51KHz when FS=48KHz 10: ADC FS * (4/3), about 64KHz when FS=48KHz 11: ADC FS * (16/9), about 85KHz when FS=48KHz
7	R/W	0x0	LINEOUT_SPEED_SELECT LINEOUT setup speed control (for testing) 0: slow; 1: fast
6	R/W	0x0	CURRENT_TEST_SELECT Internal current sink test enable (from MICIN1N pin) 0:Normal; 1: For Debug
5:0	R/W	0x0	/

9.7.23. 232Ch Analog performance tuning Control Register

Default: x5555			Register Name: ANALOG_TUNING
Bit	**Read/Write**	**Default**	**Description**
15:14	R/W	0x1	OPDRV_OPCOM_CUR. OPDRV/OPCOM output stage current setting
13:12	R/W	0x1	OPADC1_BIAS_CUR. OPADC1 Bias Current Select
11:10	R/W	0x1	OPADC2_BIAS_CUR. OPADC2 Bias Current Select
9:8	R/W	0x1	OPAAF_BIAS_CUR. OPAAF in ADC Bias Current Select
7:6	R/W	0x1	OPMIC_BIAS_CUR OPMIC Bias Current Control
5:4	R/W	0x1	OPVR_BIAS_CUR. OPVR Bias Current Control
3:2	R/W	0x1	OPDAC_BIAS_CUR. OPDAC Bias Current Control
1:0	R/W	0x1	OPMIX_BIAS_CUR. OPMIX/OPLPF/OPDRV/OPCOM Bias Current Control

9.7.24. 2480h ADC DAP Function Selected Register

Default: 0x0000			Register Name: AC_AGC_SEL
Bit	**Read/Write**	**Default**	**Description**
15:2	/	/	/
1	R/W	0x0	/
0	R/W	0x0	AGC_SEL AGC Function selected Control 0: disable 1: enable

9.7.25. 2500h ADC DAP Left Channel Control Register

Default : 0x0000			Register Name: AC_ADC_DAPLCTRL
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14	R/W	0x0	Left AGC enable 0: disable 1: enable
13	R/W	0x0	Left HPF enable 0: disable 1: enable
12	R/W	0x0	Left Noise detect enable 0: disable 1: enable

11:10	R/W	0x0	Reserved
9:8	R/W	0x0	Left Hysteresis setting 00: 1dB 01: 2dB 10: 4dB 11: disable;
7:4	R/W	0x0	Left Noise debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs $T=2^{(N+1)}/fs$, except N=0
3:0	R/W	0x0	Left Signal debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs $T=2^{(N+1)}/fs$, except N=0

9.7.26. 2502h ADC DAP Right Channel Control Register

Default : 0x0000			**Register Name: AC_ADC_DAPRCTRL**
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14	R/W	0x0	Right AGC enable 0: disable 1: enable
13	R/W	0x0	Right HPF enable 0: disable 1: enable
12	R/W	0x0	Right Noise detect enable 0: disable 1: enable
11:10	R/W	0x0	Reserved
9: 8	R/W	0x0	Right Hysteresis setting 00: 1dB 01: 2dB 10: 4dB 11: disable
7: 4	R/W	0x0	Right Noise debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs

			T=$2^{(N+1)}$/fs ,except N=0
3: 0	R/W	0x0	Right Signal debounce time 0000: disable 0001: 4/fs 0010: 8/fs ---------- 1111: 16*4096/fs T=$2^{(N+1)}$/fs, except N=0

9.7.27. 2504h ADC DAP Left Status Register

Default : 0x0000			**Register Name: AC_ADC_DAPLSTA**
Bit	**Read/Write**	**Default**	**Description**
15:10	R	0x0	Reserved
9	R	0x0	Left AGC saturation flag
8	R	0x0	Left AGC noise-threshold flag
7:0	R	0x0	Left Gain applied by AGC (7.1 format 2s complement(-20dB – 40dB), 0.5B/ step) 0x50: 40dB 0x4F: 39.5dB ---------- 0x00: 00dB 0xFF: -0.5dB

9.7.28. 2506h ADC DAP Right Status Register

Default : 0x0000			**Register Name: AC_ADC_DAPRSTA**
Bit	**Read/Write**	**Default**	**Description**
11:10	R	0x0	Reserved
9	R	0x0	Right AGC saturation flag
8	R	0x0	Right AGC noise-threshold flag
7:0	R	0x0	Right Gain applied by AGC (7.1 format 2s complement(-20dB – 40dB), 0.5dB /step) 0x50: 40dB 0x4F: 39.5dB ---------- 0x00: 00dB 0xFF: -0.5dB

9.7.29. 2508h ADC DAP Left Target Level Register

Default : 0x2C28			**Register Name: AC_ADC_DAPLTL**
Bit	**Read/Write**	**Default**	**Description**

15:14	/	/	/
13:8	R/W	0x2C (-20dB)	Left channel target level setting(-1dB -- -30dB).(6.0format 2s complement)
7:0	R/W	0x28 (20dB)	Left channel max gain setting(0-40dB).(7.1format 2s complement)

9.7.30. 250Ah ADC DAP Right Target Level Register

Default : 0x2C28			**Register Name: AC_ADC_DAPRTL**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:8	R/W	0x2C (-20dB)	Right channel target level setting(-1dB -- -30dB).(6.0format 2s complement)
7:0	R/W	0x28 (20dB)	Right channel max gain setting (0-40dB). (7.1format 2s complement)

9.7.31. 250Ch ADC DAP Left High Average Coef Register

Default : 0x0005			**Register Name: AC_ADC_DAPLHAC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Left channel output signal average level coefficient setting(the coefficient [reg06[10:0],reg07] is 3.24 format 2s complement)

9.7.32. 250Eh ADC DAP Left Low Average Coef Register

Default : 0x1EB8			**Register Name: AC_ADC_DAPLLAC**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	Left channel output signal average level coefficient setting(the coefficient [reg07[10:0],reg08] is 3.24 format 2s complement)

9.7.33. 2510h ADC DAP Right High Average Coef Register

Default : 0x0005			**Register Name: AC_ADC_DAPRHAC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Right channel output signal average level coefficient setting(the coefficient [reg08[10:0],reg09] is 3.24 format 2s complement)

9.7.34. 2512h ADC DAP Right Low Average Coef Register

Default : 0x1EB8	**Register Name: AC_ADC_DAPRLAC**

Bit	Read/Write	Default	Description
15:0	R/W	0x1EB8	Right channel output signal average level coefficient setting(the coefficient [reg08[10:0],reg09] is 3.24 format 2s complement)

9.7.35. 2514h ADC DAP Left Decay Time Register

Default : 0x001F			Register Name: AC_ADC_DAPLDT
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x001F (32x32fs)	Left decay time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain increases, the actual gain will increase 0.5dB at every decay time.

9.7.36. 2516h ADC DAP Left Attack Time Register

Default Value: 0x0000			Register Name: AC_ADC_DAPLAT
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x0000	Left attack time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.

9.7.37. 2518h ADC DAP Right Decay Time Register

Default : 0x0000_001F			Register Name: AC_ADC_DAPRDT
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x001F (32x32fs)	Right decay time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs

			When the gain increases, the actual gain will increase 0.5dB at every decay time.

9.7.38. 251Ah ADC DAP Right Attack Time Register

Default : 0x0000			**Register Name: AC_ADC_DAPRAT**
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0x0000	Right attack time coefficient setting 0000: 1x32/fs 0001: 2x32/fs ---------- 7FFF: 2^{15} x32/fs T=(n+1)*32/fs When the gain decreases, the actual gain will decrease 0.5dB at every attack time.

9.7.39. 251Ch ADC DAP Noise Threshold Register

Default : 0x1E1E			**Register Name:AC_ADC_DAPNTH**
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12:8	R/W	0x1E (-90dB)	Left channel noise threshold setting. 0x00: -30dB 0x01: -32dB 0x02: -34dB ---------- 0x1D: -88dB 0x1E: -90dB 0x1F: -90dB(the same as 0x1E)
7:5	/	/	/
4:0	R/W	0x1E (-90dB)	Right channel noise threshold setting(-90 -- -30dB). 0x00: -30dB 0x01: -32dB 0x02: -34dB ---------- 0x1D: -88dB 0x1E: -90dB 0x1F: -90dB(the same as 0x1E)

9.7.40. 251Eh ADC DAP Left Input Signal High Average Coef Register

Default : 0x0005	**Register Name: AC_ADC_DAPLHNAC**

Bit	Read/Write	Default	Description
15:11	/	/	/
10:0	R/W	0x0005	Left input signal average filter coefficient to check noise or not(the coefficient [reg0f[10:0],reg10] is 3.24 format 2s complement), always the same as the left output signal average filter's.

9.7.41. 2520h ADC DAP Left Input Signal Low Average Coef Register

Default : 0x1EB8			Register Name: AC_ADC_DAPLLNAC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	Left input signal average filter coefficient to check noise or not(the coefficient [reg0f[10:0],reg10] is 3.24 format 2s complement) always the same as the left output signal average filter's

9.7.42. 2522h ADC DAP Right Input Signal High Average Coef Register

Default : 0x0005			Register Name: AC_ADC_DAPRHNAC
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0005	Right input signal average filter coefficient to check noise or not(the coefficient [reg11[10:0],reg12] is 3.24 format 2s complement), always the same as the right output signal average filter's

9.7.43. 2524h ADC DAP Right Input Signal Low Average Coef Register

Default : 0x1EB8			Register Name: AC_ADC_DAPRLNAC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	Right input signal average filter coefficient to check noise or not(the coefficient [reg11[10:0],reg12] is 3.24 format 2s complement), always the same as the right output signal average filter's

9.7.44. 2526h ADC DAP High HPF Coef Register

Default : 0x00FF			Register Name: AC_DAPHHPFC
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x00FF	HPF coefficient setting(the coefficient [reg13[10:0],reg14] is 3.24 format 2s complement)

9.7.45. 2528h ADC DAP Low HPF Coef Register

Default : 0xFAC1	Register Name: AC_DAPLHPFC

Bit	Read/Write	Default	Description
15:0	R/W	0xFAC1	HPF coefficient setting(the coefficient [reg13[10:0],reg14] is 3.24 format 2s complement)

9.7.46. 252Ah ADC DAP Optimum Register

Default : 0x0000			Register Name: AC_DAPOPT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10	R/W	0	Left energy default value setting(include the input and output) 0: min 1: max
9:8	R/W	00	Left channel gain hystersis setting. The different between target level and the signal level must larger than the hystersis when the gain change. 00: 0.4375db 01: 0.9375db 10: 1.9375db 11: 3db
7:6	/	/	/
5	R/W	0	The input signal average filter coefficient setting 0: is the [reg0f[10:0], reg10] and [reg11[1:0], reg12]; 1: is the [reg06[10:0], reg07] and [reg08[1:0], reg09];
4	R/W	0	AGC output when the channel in noise state 0: output is zero 1: output is the input data
3	/	/	/
2	R/W	0	Right energy default value setting(include the input and output) 0: min 1: max
1:0	R/W	00	Right channel gain hystersis setting. The different between target level and the signal level must larger than the hystersis when the gain change. 00: 0.4375db 01: 0.9375db 10: 1.9375db 11: 3db

9.7.47. 3000h DAC DAP Channel Control Register

Default : 0x0000			Register Name: AC_DAC_DAPCTRL
Bit	**Read/Write**	**Default**	**Description**
15:3	/	/	/
2	R/W	0	DRC enable control

			0: disable 1: enable
1	R/W	0	DRC Left channel HPF enable control 0: disable 1: enable
0	R/W	0	DRC Right channel HPF enable control 0: disable 1: enable

9.7.48. 3002h DRC High HPF Coef Register

Default : 0x00FF			**Register Name: AC_DRC_HHPFC**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0xFF	HPF coefficient setting and the data is 3.24 format.

9.7.49. 3004h DRC Low HPF Coef Register

Default : 0xFAC1			**Register Name: AC_DRC_LHPFC**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xFAC1	HPF coefficient setting and the data is 3.24 format.

9.7.50. 3006h DRC Control Register

Default : 0x0080			**Register Name: AC_DRC_CTRL**
Bit	**Read/Write**	**Default**	**Description**
15	R	0	DRC delay buffer data output state when drc delay function is enble and the drc funciton disable. After disable drc function and this bit go to 0, the user should write the drc delay function bit to 0; 0 : not complete 1 : is complete
14	/	/	/
13:8	R/W	0	Signal delay time setting 6'h00 : (8x1)fs 6'h01 : (8x2)fs 6'h02 : (8x3)fs ---------- 6'h2e : (8*47)fs 6'h2f : (8*48)fs 6'h30 -- 6'h3f : (8*48)fs Delay time = 8*(n+1)fs, n<6'h30; When the delay function is disable, the signal delay time is unused.
7	R/W	0x1	The delay buffer use or not when the drc disable and the drc buffer data output completely 0 : don't use the buffer 1 : use the buffer

6	R/W	0x0	DRC gain max limit enable 0 : disable 1 : enable
5	R/W	0x0	DRC gain min limit enable. when this fuction enable, it will overwrite the noise detect funciton. 0 : disable 1 : enable
4	R/W	0x0	Control the drc to detect noise when ET enable 0 : disable 1 : enable
3	R/W	0x0	Signal function Select 0 : RMS filter 1 : Peak filter When Signal function Select Peak filter, the RMS parameter is unused.(AC_DRC_LRMSHAT / AC_DRC_LRMSLAT / AC_DRC_LRMSHAT / AC_DRC_LRMSLAT) When Signal function Select RMS filter, the Peak filter parameter is unused.(AC_DRC_LPFHAT / AC_DRC_LPFLAT / AC_DRC_RPFHAT / AC_DRC_RPFLAT / AC_DRC_LPFHRT / AC_DRC_LPFLRT / AC_DRC_RPFHRT / AC_DRC_RPFLRT)
2	R/W	0x0	Delay function enable 0 : disable 1 : enable When the Delay function enable is disable, the Signal delay time is unused.
1	R/W	0x0	DRC LT enable 0 : disable 1 : enable When the DRC LT is disable the LT, Kl and OPL parameter is unused.
0	R/W	0x0	DRC ET enable 0 : disable 1 : enable When the DRC ET is disable the ET, Ke and OPE parameter is unused.

9.7.51. 3008h DRC Left Peak Filter High Attack Time Coef Register

Default : 0x000B			**Register Name: AC_DRC_LPFHAT**
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.7.52. 300Ah DRC Left Peak Filter Low Attack Time Coef Register

Default : 0x77BF			Register Name: AC_DRC_LPFLAT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.7.53. 300Ch DRC Right Peak Filter High Attack Time Coef Register

Default : 0x000B			Register Name: AC_DRC_RPFHAT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x000B	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.7.54. 300Eh DRC Peak Filter Low Attack Time Coef Register

Default : 0x77BF			Register Name: AC_DRC_RPFLAT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x77BF	The left peak filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/ta). The format is 3.24. (1ms)

9.7.55. 3010h DRC Left Peak Filter High Release Time Coef Register

Default : 0x00FF			Register Name: AC_DRC_LPFHRT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.7.56. 3012h DRC Left Peak Filter Low Release Time Coef Register

Default : 0xE1F8			Register Name: AC_DRC_LPFLRT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.7.57. 3014h DRC Right Peak filter High Release Time Coef Register

Default : 0x00FF	Register Name: AC_DRC_RPFHRT

Bit	Read/Write	Default	Description
15:11	/	/	/
10:0	R/W	0x00FF	The left peak filter attack time parameter setting, which determine by the equation that RT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.7.58. 3016h DRC Right Peak filter Low Release Time Coef Register

Default : 0xE1F8			Register Name: AC_DRC_RPFLRT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xE1F8	The left peak filter release time parameter setting, which determine by the equation that AT = exp(-2.2Ts/tr). The format is 3.24. (100ms)

9.7.59. 3018h DRC Left RMS Filter High Coef Register

Default : 0x0001			Register Name: AC_DRC_LRMSHAT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0001	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.7.60. 301Ah DRC Left RMS Filter Low Coef Register

Default : 0x2BAF			Register Name: AC_DRC_LRMSLAT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x2BAF	The left RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.7.61. 301Ch DRC Right RMS Filter High Coef Register

Default : 0x0001			Register Name: AC_DRC_RRMSHAT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0001	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.7.62. 301Eh DRC Right RMS Filter Low Coef Register

Default : 0x2BAF	Register Name: AC_DRC_RRMSLAT

Bit	Read/Write	Default	Description
15:0	R/W	0x2BAF	The right RMS filter average time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tav). The format is 3.24. (10ms)

9.7.63. 3020h DRC Compressor Theshold High Setting Register

Default : 0x06A4			Register Name: AC_DRC_HCT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x06A4	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

9.7.64. 3022h DRC Compressor Theshold High Setting Register

Default : 0xD3C0			Register Name: AC_DRC_LCT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xD3C0	The compressor threshold setting, which set by the equation that CTin = -CT/6.0206. The format is 8.24 (-40dB)

9.7.65. 3024h DRC Compressor Slope High Setting Register

Default : 0x0800			Register Name: AC_DRC_HKC
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
13:0	R/W	0x0800	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

9.7.66. 3026h DRC Compressor Slope Low Setting Register

Default : 0x0000			Register Name: AC_DRC_LKC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	The slope of the compressor which determine by the equation that Kc = 1/R, there, R is the ratio of the compressor, which always is interger. The format is 8.24. (2 : 1)

9.7.67. 3028h DRC Compressor High Output at Compressor Threshold Register

Default : 0xF95B			Register Name: AC_DRC_HOPC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xF95B	The output of the compressor which determine by the equation -OPC/6.0206 The format is 8.24 (-40dB)

9.7.68. 302Ah DRC Compressor Low Output at Compressor Threshold Register

Default : 0x2C3F			Register Name: AC_DRC_LOPC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x2C3F	The output of the compressor which determine by the equation OPC/6.0206 The format is 8.24 (-40dB)

9.7.69. 302Ch DRC Limiter Theshold High Setting Register

Default : 0x01A9			Register Name: AC_DRC_HLT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x01A9	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

9.7.70. 302Eh DRC Limiter Theshold Low Setting Register

Default : 0x34F0			Register Name: AC_DRC_LLT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x34F0	The limiter threshold setting, which set by the equation that LTin = -LT/6.0206, The format is 8.24. (-10dB)

9.7.71. 3030h DRC Limiter Slope High Setting Register

Default : 0x0005			Register Name: AC_DRC_HKl
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
13:0	R/W	0x0005	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

9.7.72. 3032h DRC Limiter Slope Low Setting Register

Default : 0x1EB8			Register Name: AC_DRC_LKl
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x1EB8	The slope of the limiter which determine by the equation that Kl = 1/R, there, R is the ratio of the limiter, which always is interger. The format is 8.24. (50 :1)

9.7.73. 3034h DRC Limiter High Output at Limiter Threshold

Default : 0xFBD8			Register Name: AC_DRC_HOPL
Bit	**Read/Write**	**Default**	**Description**

15:0	R/W	0xFBD8	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

9.7.74. 3036h DRC Limiter Low Output at Limiter Threshold

Default : 0xFBA7			**Register Name: AC_DRC_LOPL**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xFBA7	The output of the limiter which determine by equation OPT/6.0206. The format is 8.24 (-25dB)

9.7.75. 3038h DRC Expander Theshold High Setting Register

Default : 0x0BA0			**Register Name: AC_DRC_HET**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0BA0	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

9.7.76. 303Ah DRC Expander Theshold Low Setting Register

Default : 0x7291			**Register Name: AC_DRC_LET**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x7291	The expander threshold setting, which set by the equation that ETin = -ET/6.0206, The format is 8.24. (-70dB)

9.7.77. 303Ch DRC Expander Slope High Setting Register

Default : 0x0050			**Register Name: AC_DRC_HKE**
Bit	**Read/Write**	**Default**	**Description**
15:14			
13:0	R/W	0x0050	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

9.7.78. 303Eh DRC Expander Slope Low Setting Register

Default : 0x0000			**Register Name: AC_DRC_LKE**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	The slope of the expander which determine by the equation that Ke = 1/R, there, R is the ratio of the expander, which always is interger and the ke must larger than 50. The format is 8.24. (1:5)

9.7.79. 3040h DRC Expander High Output at Expander Threshold

Default : 0xF45F			Register Name: AC_DRC_HOPE
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xF45F	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

9.7.80. 3042h DRC Expander Low Output at Expander Threshold

Default : 0x8D6E			Register Name: AC_DRC_LOPE
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x8D6E	The output of the expander which determine by equation OPE/6.0206. The format is 8.24 (-70dB)

9.7.81. 3044h DRC Linear Slope High Setting Register

Default : 0x0100			Register Name: AC_DRC_HKN
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:0	R/W	0x0100	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

9.7.82. 3046h DRC Linear Slope Low Setting Register

Default : 0x0000			Register Name: AC_DRC_LKN
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	The slope of the linear which determine by the equation that Kn = 1/R, there, R is the ratio of the linear, which always is interger . The format is 8.24. (1:1)

9.7.83. 3048h DRC Smooth filter Gain High Attack Time Coef Register

Default : 0x0002			Register Name: AC_DRC_SFHAT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0002	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

9.7.84. 304Ah DRC Smooth filter Gain Low Attack Time Coef Register

Default : 0x5600	Register Name: AC_DRC_SFLAT

Bit	Read/Write	Default	Description
15:0	R/W	0x5600	The smooth filter attack time parameter setting, which determine by the equation that AT = 1-exp(-2.2Ts/tr). The format is 3.24. (5ms)

9.7.85. 304Ch DRC Smooth filter Gain High Release Time Coef Register

Default : 0x0000			Register Name: AC_DRC_SFHRT
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0000	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

9.7.86. 304Eh DRC Smooth filter Gain Low Release Time Coef Register

Default : 0x0F04			Register Name: AC_DRC_SFLRT
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0F04	The gain smooth filter release time parameter setting, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (200ms)

9.7.87. 3050h DRC MAX Gain High Setting Register

Default : 0xFE56			Register Name: AC_DRC_MXGHS
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xFE56	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG< 30dB (-10dB)

9.7.88. 3052h DRC MAX Gain Low Setting Register

Default : 0xCB0F			Register Name: AC_DRC_MXGLS
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xCB0F	The max gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -20dB <MXG < 30dB (-10dB)

9.7.89. 3054h DRC MIN Gain High Setting Register

Default : 0xF95B			Register Name: AC_DRC_MNGHS
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0xF95B	The min gain setting which determine by equation MXG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -30dB (-30dB)

9.7.90. 3056h DRC MIN Gain Low Setting Register

Default : 0x2C3F			Register Name: AC_DRC_MNGLS
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x2C3F	The min gain setting which determine by equation MNG/6.0206. The format is 8.24 and must -60dB ≤MNG ≤ -30dB (-30dB)

9.7.91. 3058h DRC Expander Smooth Time High Coef Register

Default : 0x0000			Register Name: AC_DRC_EPSHC
Bit	**Read/Write**	**Default**	**Description**
11:0	R/W	0x0000	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

9.7.92. 305Ah DRC Expander Smooth Time Low Coef Register

Default : 0x640C			Register Name: AC_DRC_EPSLC
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x640C	The gain smooth filter release and attack time parameter setting in expander region, which determine by the equation that RT = 1-exp(-2.2Ts/tr). The format is 3.24. (30ms)

9.7.93. 305Eh DRC HPF Gain High Coef Register

Default : 0x0100			Register Name: AC_DRC_HPFHGAIN
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x0100	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.7.94. 3060h DRC HPF Gain Low Coef Register

Default : 0x0000			Register Name: AC_DRC_HPFLGAIN
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x0000	The gain of the hpf coefficient setting which format is 3.24.(gain = 1)

9.7.95. 3100h DRC Bist control Register

Default : 0x0000			Register Name: AC_DRC_BISTCR
Bit	**Read/Write**	**Default**	**Description**
15:13	R/W	0	DRC SRAM BIST Register Select

12	R/W	0	DRC SRAM BIST Address MODE Select
11:9	R/W	0	DRC SRAM BIST Write Data Pattern 0: 0x0000_0000 1: 0x5555_5555 2: 0x3333_3333 3: 0x0f0f_0f0f 4: 0x00ff_00ff 5: 0x0000_ffff Others, reserved.
8	R/W	0	DRC SRAM BIST Enable A positive edge will trigger the SRAM BIST to start
7:0	/	/	/

9.7.96. 3102h DRC Bist Status Register

Default : 0x0020			**Register Name: AC_DRC_BISTST**
Bit	**Read/Write**	**Default**	**Description**
15:8	/	/	/
7	R	0	DRC SRAM BIST Error Status 0: No Error 1: Error
6:4	R	0	DRC SRAM BIST Error Pattern
3:2	R	0	DRC SRAM BIST Error Cycles
1	R	1	DRC SRAM BIST Stop 0: Running 1: Stop
0	R	0	DRC SRAM BIST Busy 0: Idle 1: Busy

9.8. TVE Register List

Register Name	**Address**	**Description**
TVE_CTL0	4000h	TV Encoder Control 0 Register
TVE_CTL1	4002h	TV Encoder Control 1 Register
TVE_MOD0	4004h	TV Encoder Mode 0 Register
TVE_MOD1	4006h	TV Encoder Mode 1 Register
TVE_DAC_CFG0	4008h	TV Encoder DAC Configuration 0 Register
TVE_DAC_CFG1	400Ah	TV Encoder DAC Configuration 1 Register
TVE_YC_DELAY	400Ch	TV Encoder YC Delay Register
TVE_YC_FILTER	400Eh	TV Encoder YC Filter Register
TVE_BURST_FRQ0	4010h	TV Encoder Burst Frequency 0 Register
TVE_BURST_FRQ1	4012h	TV Encoder Burst Frequency 1 Register
TVE_FRONT_PORCH	4014h	TV Encoder Front Porch Register
TVE_BACK_PORCH	4016h	TV Encoder Back Porch Register
TVE_TOTAL_LINE	401Ch	TV Encoder Total Line Number Register

TVE_FIRST_ACTIVE	401Eh	TV Encoder First Active Line Register
TVE_BLACK_LEVEL	4020h	TV Encoder Black Level Register
TVE_BLANK_LEVEL	4022h	TV Encoder Blank Level Register
TVE_PLUG_EN	4030h	TV Encoder Plug Detect Enable Register
TVE_PLUG_IRQ_EN	4032h	TV Encoder Plug Detect Interrupt Enable Register
TVE_PLUG_IRQ_STA	4034h	TV Encoder Plug Detect Interrupt Status Register
TVE_PLUG_STA	4038h	TV Encoder Plug Detect Status Register
TVE_PLUG_DEBOUNCE	4040h	TV Encoder Plug Detect De-Bounce Register
TVE_DAC_TEST	4042h	TV Encoder DAC TEST Register
TVE_PLUG_PULSE_LEVEL	40F4h	TV Encoder Plug Detect Pulse Level Register
TVE_PLUG_PULSE_START	40F8h	TV Encoder Plug Detect Pulse Start Register
TVE_PLUG_PULSE_PERIOD	40FAh	TV Encoder Auto Detect Pulse Period Register
TVE_IF_CTL	5000h	TV Encoder Interface Control Register
TVE_IF_TIM0	5008h	TV Encoder Interface Timing 0 Register
TVE_IF_TIM1	500ah	TV Encoder Interface Timing 1 Register
TVE_IF_TIM2	500ch	TV Encoder Interface Timing 2 Register
TVE_IF_TIM3	500eh	TV Encoder Interface Timing 3 Register
TVE_IF_SYNC0	5010h	TV Encoder Interface SYNC 0 Register
TVE_IF_SYNC1	5012h	TV Encoder Interface SYNC 1 Register
TVE_IF_SYNC2	5014h	TV Encoder Interface SYNC 2 Register
TVE_IF_TIM4	5016h	TV Encoder Interface Timing 4 Register
TVE_IF_STATUS	5018h	TV Encoder Interface Status Register

9.9. TVE Register Description

9.9.1. 4000h TV Encoder Control 0 Register

Default: 0x0000			**Register Name: TVE_CTL0**
Bit	**Read/Write**	**Default**	**Description**
15:14	/	/	/
13:10	R/W	0	Reserved
9	R/W	0	Reserved
8	R/W	0	Reserved
7:1	/	/	/
0	R/W	0	EN TV Encoder enable, default disable, write 1 to take it out of the reset state

9.9.2. 4002h TV Encoder Control 1 Register

Default: 0x0000			**Register Name: TVE_CTL1**
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	CLK_DISABLE

			TV Encoder clock gate disable 1: disable 0: enable
14:0	/	/	/

9.9.3. 4004h TV Encoder Mode 0 Register

Default: 0x0000			**Register Name: TVE_MOD0**
Bit	**Read/Write**	**Default**	**Description**
15:10	/	/	/
9	R/W	0	COLOR_BAR_TYPE Color Bar Type 0: NTSC: 75/7.5/75/7.5 PAL: 100/0/75/0 1: NTSC: 100/7.5/100/7.5 PAL: 100/0/100/0
8	R/W	0	COLOR_BAR_MOD Color Bar Mode Standard Color bar input selection This bit selects whether the Video Encoder video data input is replaced by an internal standard color bar generator or not. 0: The Video Encoder input is coming from the Display Engineer 1: The Video Encoder input is coming from an internal standard color bar generator.
7:1	/	/	/
0	R/W	0	TV_MOD TV Mode Select 0: NTSC 1: PAL note: changing this register value will cause some relative register setting to relative value.

9.9.4. 4006h TV Encoder Mode 1 Register

Default: 0x0000			**Register Name: TVE_MOD1**
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12	R/W	0	DAC_TEST_MOD 0: TV mode, DAC using tvclk 1: DAC test mode，DAC using AHB clock
11:5	/	/	/
4	R/W	0	C_SEQ

			Cb/Cr sequence for 422 mode 0: Cb first 1: Cr first
3	R/W	0	C_MODE Chroma Mode 0: 444 1: 422
2:0	/	/	/

9.9.5. 4008h TV Encoder DAC Configuration 0 Register

Default: 0x12A0			Register Name: TVE_DAC_CFG0
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	Reserved
0	R/W	0	DAC_EN DAC Enable 0:disable 1:enable

9.9.6. 400Ah TV Encoder DAC Configuration 1 Register

Default: 0x4300			Register Name: TVE_DAC_CFG1
Bit	**Read/Write**	**Default**	**Description**
15:12	/	/	Reserved

9.9.7. 400Ch TV Encoder YC Delay Register

Default: 0x0004			Register Name: TVE_YC_DELAY
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:12	R/W	0	Y_DELAY
11	/	/	/
10:8	R/W	0	C_DELAY
7:3	/	/	/
2:0	R/W	/	Reserved

9.9.8. 400Eh TV Encoder YC Filter Register

Default: 0x0003			Register Name: TVE_YC_FILTER
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	Luma filter lti enable 0:disable Luma filter lti

			1:enable Luma filter lti
14	/	/	/
13:12	R/W	0	upsample for dac Out up sample 0:27M 1:54M 2:108M 3:216M
11	/	/	/
10	R/W	0	Filters_Select 0: enable new peaking filter 1: enable new reduction filter
9:8	R/W	0	New luminance peaking filter selection
7:5	/	/	/
4	R/W	0	C_FIELD1_BP Chroma filter Stage 1 0 : Chroma Filter stage 1 Enable 1: Chroma Filter stage 1 bypass
3	R/W	0	C_FIELD2_BP Chroma filter Stage 2 Bypass 0 : Chroma Filter stage 2 Enable 1: Chroma Filter stage 2 bypass
2	R/W	0	C_FILTER3_BP Chroma Filter Stage 3 Bypass 0 : Chroma Filter stage 3 Enable 1: Chroma Filter stage 3 bypass
1	R/W	1	Y_FIELD_BP Luma Filter Bypass 0: Luma Filter enable 1: Luma Filter bypass
0	R/W	1	NOTCH_EN Notch Enable Luma notch filter on/off selection This bit selects if the luma notch filter is operating or bypassed. 0: The luma notch filter is bypassed 1: The luma notch filter is operating

9.9.9. 4010h TV Encoder Burst Frequency 0 Register

Default: 0x7C1F			**Register Name: TVE_BURST_FRQ0**
Bit	**Read/Write**	**Default**	**Description**
15:0	R/W	0x7c1f	BURST_FRQ_15_0 Specify the ratio between the color burst frequency. 32 bit unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC

			specs. 3.5795455MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'):PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

9.9.10. 4012h TV Encoder Burst Frequency 1 Register

Default: 0x21F0			**Register Name: TVE_BURST_FRQ1**
Bit	**Read/Write**	**Default**	**Description**
31:0	R/W	0x21f0	BURST_FRQ_31_16 Specify the ratio between the color burst frequency. 32 bit unsigned fraction. Default value is h21f07c1f, which is compatible with NTSC specs. 3.5795455MHz (X'21F07C1F'): NTSC-M, NTSC-J 4.43361875 MHz(X'2A098ACB'): PAL-B, D, G, H,I, N 3.582056 MHz (X'21F69446'):PAL-N(Argentina) 3.579611 MHz (X'21E6EFE3'): PAL-M

9.9.11. 4014h TV Encoder Front Porch Register

Default: 0x0020			**Register Name: TVE_FRONT_PORCH**
Bit	**Read/Write**	**Default**	**Description**
15:12	/	/	/
11:0	R/W	0x20	FRONT_PORCH Front Porch must be even specify the width of the front porch in encoder clock cycles. 6 bit unsigned even integer. Allowed range is 10 to 62. Default value is 32.

9.9.12. 4016h TV Encoder Back Porch Register

Default: 0x0076			**Register Name: TVE_BACK_PORCH**
Bit	**Read/Write**	**Default**	**Description**
31:9	/	/	/
8:0	R/W	0x76	BACK_PORCH Back Porch Specify the width of the back porch in encoder clock cycles. Min value is (burst_width+breeze_way+17). 8 bit unsigned integer. Default value is 118

9.9.13. 401Ch TV Encoder Total Line Number Register

Default: 0x020D			Register Name: TVE_TOTAL_LINE
Bit	**Read/Write**	**Default**	**Description**
15:11	/	/	/
10:0	R/W	0x20D	NUM_LINES Number Lines Specify the total number of lines in a video frame. 11 bit unsigned integer. Allowed range is 0 to 2048. Default value is 525. For interlaced video: When NTSC, and FirstVideoLine is greater than 20, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When NTSC, and FirstVideoLine is not greater than 20, then NumLines is restricted to be greater than 77. When PAL, and FirstVideoLine is greater than 22, then NumLines is restricted to be greater than 2*(FirstVideoLine+18). When PAL, and FirstVideoLine is not greater than 22, then NumLines is restricted to be greater than 81. If NumLines is even, then it is restricted to be divisible by 4. If NumLines is odd, then it is restricted to be divisible by 4 with a remainder of 1.

9.9.14. 401Eh TV Encoder First Active Line Register

Default: 0x0016			Register Name: TVE_FIRST_ACTIVE
Bit	**Read/Write**	**Default**	**Description**
15:8	/	/	/
7:0	R/W	0x16	FIRST_VIDEO_LINE First Video Line Specify the index of the first line in a field/frame to have active video. 8 bit unsigned integer. For interlaced video: When VSync5=B'0', FirstVideoLine is restricted to be greater than 7. When VSync5=B'1', FirstVideoLine is restricted to be greater than 9. Default value is 21.

9.9.15. 4020h TV Encoder Black Level Register

Default: 0x011A			Register Name: TVE_BLACK_LEVEL
Bit	**Read/Write**	**Default**	**Description**
15:10	/	/	/
9:0	R/W	11a	BLACK_LEVEL Black Level Specify the black level setting. 10 bit unsigned integer. Allowed range is 240 to 1023. Default value is 282

9.9.16. 4022h TV Encoder Blank Level Register

Default: 0x00F0			Register Name: TVE_BLANK_LEVEL
Bit	**Read/Write**	**Default**	**Description**
15:10	/	/	/
9:0	R/W	0f0	BLANK_LEVEL Blank Level Specify the blank level setting for active lines. 10 bit unsigned integer. Allowed range 0 to 1023. Default value is hexF0(dec240).

9.9.17. 4030h TV Encoder Plug Detect Enable Register

Default: 0x0000			Register Name: TVE _PLUG_ EN
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/
0	R/W	0	AUTO_DET_EN Auto Detection Enable

9.9.18. 4032h TV Encoder Plug Detect Interrupt Enable Register

Default: 0x0000			Name: TVE _PLUG_IRQ_EN
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/
0	R/W	0	AUTO_DET_IRQ_EN Auto Detection Interrupt Enable

9.9.19. 4034h TV Encoder Plug Detect Interrupt Status Register

Default: 0x0000			Register Name: TVE_ PLUG_IRQ_STA
Bit	**Read/Write**	**Default**	**Description**
15:1	/	/	/
0	R/W	0	AUTO_DET_IRQ_STA Auto detection interrupt active flag, write 1 to inactive DAC0 auto detection interrupt

9.9.20. 4038h TV Encoder Plug Detect Status Register

Default: 0x0000			Register Name: TVE_ PLUG_STA
Bit	**Read/Write**	**Default**	**Description**
15:2	/	/	/
1:0	R/W	0	AUTO_DET_STA DAC Status

			00: Unconnected 01: Connected 11: Short to ground 10: Reserved

9.9.21. 4040h TV Encoder Plug Detect De-Bounce Register

Default: 0x0000			Register Name: TVE_ PLUG_DEBOUNCE
Bit	**Read/Write**	**Default**	**Description**
15:4	/	/	/
3:0	R/W	0	DAC_DE_BNC DAC De-bounce times

9.9.22. 4042h TV Encoder DAC TEST Register

Default: 0x0000			Register Name: TVE_DAC_TEST
Bit	**Read/Write**	**Default**	**Description**
15:10	/	/	Reserved

9.9.23. 40F4h TV Encoder Plug Detect Pulse Level Register

Default: 0x0000			Register Name: TVE_PLUG_PULSE_LEVEL
Bit	**Read/Write**	**Default**	**Description**
15:10	/	/	/
9:0	R/W	0	DETECT_PULSE_LEVEL Use for DAC data input at auto detect pluse

9.9.24. 40F8h TV Encoder Plug Detect Pulse Start Register

Default: 0x0000			Register Name: TVE_PLUG_ PULSE_START
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0	DETECT_PULSE_START

9.9.25. 40FAh TV Encoder Auto Detect Pulse Period Register

Default: 0x0000			Register Name: TVE_PLUG_PULSE_PERIOD
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:0	R/W	0	DETECT_PULSE_PERIOD Use 32K clock

9.9.26. 5000h TV Encoder Interface Control Register

Default: 0x0000			Register Name: TVE_IF_CTL0
Bit	**Read/Write**	**Default**	**Description**
15:13	/	/	/
12	R/W	0	PROGRESSIVE_MODE 0: interlaced 1: progressive
11:10	/	/	/
9:8	R/W	0	SYUV_INPUT_FORMAT 000: YUV 001: YVU 010: UYV 011: UVY 100: VYU 101: VUY Others: reserved
6	/	/	/
5:4	R/W	0	CCIR656_INPUT_FORMAT 00: YUYV 01: YVYU 10: UYVY 11: VYUY
3:2	/	/	/
1:0	R/W	0	INTERFACE_SEL 0：CCIR656 input interface 1：Serial YUV input interface

9.9.27. 5008h TV Encoder Interface Timing 0 Register

Default: 0x0000			Register Name: TVE_IF_TIM0
Bit	**Read/Write**	**Default**	**Description**
15:9	/	/	/
8:0	R/W	0	HBP horizontal back porch T_{hbp} = HBP×T_{clk}

9.9.28. 500ah TV Encoder Interface Timing 1 Register

Default: 0x0000			Register Name: TVE_IF_TIM1
Bit	**Read/Write**	**Default**	**Description**
15:12	/	/	/
11:0	R/W	0	HACT

			Horizontal active cycle T_{hact} = H_ HACT×T_{clk}

9.9.29. 500ch TV Encoder Interface Timing 2 Register

Default: 0x0000			Register Name: TVE_IF_TIM2
Bit	**Read/Write**	**Default**	**Description**
15:9	/	/	/
8:0	R/W	0	VBP_ODD Vertical back porch in line T_{hbp} = VBP×T_h

9.9.30. 500eh TV Encoder Interface Timing 3 Register

Default: 0x0000			Register Name: TVE_IF_TIM3
Bit	**Read/Write**	**Default**	**Description**
15:10	/	/	/
9:0	R/W	0	VACT Vertical active in line T_{hact} = VACT×T_h

9.9.31. 5010h TV Encoder Interface SYNC 0 Register

Default: 0x0000			Register Name: TVE_IF_SYNC0
Bit	**Read/Write**	**Default**	**Description**
15	R/W	0	INPUT_BYPASS_TO_DAC 0: normal 1: D[7:0] - DAC[7:0], HSYNC - DAC[8], VSYNC-DAC[9]
14:10	/	/	/
9	R/W	0	V_OUTPUT 0: VSYNC IO normal mode, as input 1: internal V signal output to VSYNC IO
8	R/W	0	H_OUTPUT 0: HSYNC IO normal mode, as input 1: internal H signal output to HSYNC IO
7	/	/	/
6	R/W	0	/
5	R/W	0	V_SEL 0 : internal V signal from sync CCIR reference codes 1 : internal V signal from sync IO generator Node that internal DE signal is generate from internal V and H signal
4	R/W	0	H_SEL 0 : internal H signal from sync CCIR reference codes

			1 : internal H signal from sync IO generator Node that internal DE signal is generate from internal V and H signal
3	/	/	/
2	R/W	0	CLOCK_POLARITY 0: latch data from clock falling edge 1: latch data from clock rising edge
1	R/W	0	VSYNC_ POLARITY 0: active 0 1: active 1
0	R/W	0	HSYNC_ POLARITY 0: active 0 1: active 1

9.9.32. 5012h TV Encoder Interface SYNC 1 Register

Default: 0x0000			**Register Name: TVE_IF_SYNC1**
Bit	**Read/Write**	**Default**	**Description**
15:3	/	/	/
2:0	R/W	0	RESYNC_INTERVAL_TIME 000： Disable 001： once at start 010： every 4 vsync 011： every 8 vsync 100： every 16 vsync Others： Disable

9.9.33. 5014h TV Encoder Interface SYNC 2 Register

Default: 0x0000			**Register Name: TVE_IF_SYNC2**
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0	RESYNC_DELAY_LINE
11:0	R/W	0	RESYNC_DELAY_PIXLE Count by dclk

9.9.34. 5016h TV Encoder Interface Timing 4 Register

Default: 0x0000			**Register Name: TVE_IF_TIM4**
Bit	**Read/Write**	**Default**	**Description**
15:9	/	/	/
8:0	R/W	0	VBP_EVEN Vertical back porch in line $T_{hbp} = VBP \times T_h$

9.9.35. 5018h TV Encoder Interface Status Register

Default: 0x0000			Register Name: TVE_IF_STATUS
Bit	**Read/Write**	**Default**	**Description**
15	R	0	DE_STATUS Internal DE signal status
14	R	0	F_STATUS Internal F signal status
13	R	0	V_STATUS Internal V signal status
12	R	0	H_STATUS Internal H signal status
11	R	0	CCIR_P_ERROR If CCIR code P3-P0 is not equal to H V F XOR result, this bit is set'1', write '1' to clear this bit.
10	/	/	/
9:0	R	0	H_LINE_NUM Indecate total H signal cycle number in a Frame time.

9.10. EPHY Register List

Register Name	Address	Description
EPHY_CTL	6000H	Ethernet PHY Control 0 Register

9.11. EPHY Register Description

9.11.1. 6000h Ethernet PHY Control Register

Default: 0x0005			Register Name: EPHY_CTL
Bit	**Read/Write**	**Default**	**Description**
15:12	R/W	0x0	BPS_EFFUSE
11	R/W	0x0	XMII_SEL 0: MII 1: RMII
10:9	R/W	0x0	EPHY_MODE Operation Mode Selection 00 : Normal Mode 01 : Sim Mode 10 : AFE Test Mode 11 : /
8:4	R/W	0x0	PHY_ADDR PHY Address

3	R/W	0x0	BIST_CLK_EN 0 : BIST clk disable 1 : BIST clk enable
2	R/W	0x1	CLK_SEL 0 : 27MHz 1 : 24MHz
1	R/W	0x0	LED_POL 0 : High active 1 : Low active
0	R/W	0x1	SHUTDOWN 0 : Power up 1 : Shutdown

9.11.2. 6002h Ethernet PHY BIST Register

Default: 0x0000			**Register Name: EPHY_BIST**
Bit	**Read/Write**	**Default**	**Description**
15	/	/	/
14:12	R/W	0x0	BIST_STATUS bist_status[5]:BIST_FAIL_RMII2MII bist_status[4]:BIST_FAIL_MII2RMII bist_status[3]:BIST_FAIL_PLPIC
11	/	/	/
10:8	R/W	0x0	BIST_FINISH bist_status[2]:BIST_FINISH_RMII2MII bist_status[1]:BIST_FINISH_MII2RMII bist_status[0]:BIST_FINISH_PLPIC
7:1	/	/	/
0	R/W	0x0	BIST_START 0 : disable 1 : Start

9.12. RTC Register List

Module Name	**Base Address**
RTC	A000H

Register Name	**Address**	**Description**
LOSC_CTRL_REG0	A000h	Low Oscillator Control Register 0
LOSC_CTRL_REG1	A002h	Low Oscillator Control Register 1
LOSC_AUTO_SWT_STA_REG	A004h	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	A008h	Internal OSC Clock Prescalar Register
RTC_YY_MM_DD_REG0	A010h	RTC Year-Month-Day Register 0

RTC_YY_MM_DD_REG1	A012h	RTC Year-Month-Day Register 1
RTC_HH_MM_SS_REG0	A014h	RTC Hour-Minute-Second Register 0
RTC_HH_MM_SS_REG1	A016h	RTC Hour-Minute-Second Register 1
ALARM0_CUR_VLU_REG0	A024h	Alarm 0 Counter Current Value Register 0
ALARM0_CUR_VLU_REG1	A026h	Alarm 0 Counter Current Value Register 1
ALARM0_ENABLE_REG	A028h	Alarm 0 Enable Register
ALARM0_IRQ_EN	A02Ch	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	A030h	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM-SS_REG0	A040h	Alarm 1 Week HMS Register 0
ALARM1_WK_HH_MM-SS_REG1	A042h	Alarm 1 Week HMS Register 1
ALARM1_ENABLE_REG	A044h	Alarm 1 Enable Register
ALARM1_IRQ_EN	A048h	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	A04Ch	Alarm 1 IRQ Status Register
ALARM_CONFIG_REG	A050h	Alarm Config Register
LOSC_OUT_GATING_REG	A060h	LOSC output gating register
GP_DATA_REG	A100h~A11C	General Purpose Register (N=0~15)
RTC_DEB_REG	A170h	RTC Debug Register
GPL_HOLD_OUTPUT_REG	A180h	GPL Hold Output Register
VDD_RTC_REG	A190h	VDD RTC Regulate Register
IC_CHARA_REG0	A1F0h	IC Characteristic Register 0
IC_CHARA_REG1	A1F2h	IC Characteristic Register 1

9.13. RTC Register Description

9.13.1. A000h LOSC Control 0

Default: 0x4000			**Register Name: LOSC_CTRL_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN. LOSC auto switch enable. 0: Disable, 1: Enable.
13	R/W	0x0	RTC_HHMMSS_LOCK. 0: RTC HHMMSS is update auto 1: RTC HHMMSS is lock
12	R/W	0x0	RTC_HHMMSS_WRITE. Write '1' to update RTC HHMMSS by RTC register, this bit is clear auto.
11	/	/	/
10	R/W	0x0	RTC_HHMMSS1_ACCE. RTC HH-MM-SS access. After writing the RTC HH-MM-SS1 register, this bit is set and it will be cleared until the real writing operation is finished.

			After writing the RTC HH-MM-SS1 register, the HH-MM-SS1 register will be refreshed for at most one second.
9	R/W	0x0	RTC_HHMMSS0_ACCE. RTC HH-MM-SS0 access. After writing the RTC HH-MM-SS0 register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC HH-MM-SS0 register, the HH-MM-SS0 register will be refreshed for at most one second.
8	R/W	0x0	RTC_YYMMDD1_ACCE. RTC YY-MM-DD1 access. After writing the RTC YY-MM-DD1 register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD1 register, the YY-MM-DD1 register will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD0_ACCE. RTC YY-MM-DD0 access. After writing the RTC YY-MM-DD0 register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD0 register, the YY-MM-DD0 register will be refreshed for at most one second.
6:4	/	/	/
5	R/W	0x0	RTC_ YYMMDD_LOCK. 0: RTC YYMMDD is update auto 1: RTC YYMMDD is lock
4	R/W	0x0	RTC_ YYMMDD_WRITE. Write ‘1’ to update RTC YYMMDD by register, this bit is clear auto.
3:2	R/W	0x0	EXT_LOSC_GSM. External 32768Hz Crystal GSM. 00 low 01 10 11 high
1	/	/	/
0	R/W	0x0	LOSC_SRC_SEL. LOSC Clock source Select. ‘N’ is the value of Internal OSC Clock Prescalar register. 0: InternalOSC / N, 1: External 32.768KHz OSC.

Note1: Any bit of [9:7] is set, the RTC HH-MM-SS, YY-MM-DD and ALARM DD-HH-MM-SS register can’t be written.

Note2: Internal OSC is about 16MHz.

9.13.2. A002h LOSC Control 1

Default: 0x0000	**Register Name: LOSC_CTRL_REG**

Bit	Read/Write	Default/Hex	Description
15:0	W	0x0	KEY_FIELD. Key Field. This field should be filled with 0x16AB, and then the bit 0 can be written with the new value.

9.13.3. A004h LOSC Auto Switch Status Register

Default: 0x0000			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:2	/	/	/
1	R/W	0x0	LOSC_AUTO_SWT_PEND. LOSC auto switch pending. 0: No effect 1: Auto switches pending Set 1 to this bit will clear it.
0	RO	0x0	LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. 'N' is the value of Internal OSC Clock Prescalar register. 0: InternalOSC / N 1: External 32.768KHz OSC

9.13.4. A008h Internal OSC Clock Prescalar Register

Default: 0x000F			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0xF	INTOSC_CLK_PRESCAL. Internal OSC Clock Prescalar value N. 0x000: 1 0x001: 2 0x002: 3 ..... 0x1FF: 512

9.13.5. A010h RTC YY-MM-DD Register 0

Default: 0x0000			Register Name: RTC_YY_MM_DD_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:12	/	/	/
11:8	R/W	x	MONTH. Month. Range from 1~12.
7:5	/	/	/
4:0	R/W	x	DAY.

			Day. Range from 1~31.

Note1: If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area. If the **RTC_YY_MM_DD_REG0** and **RTC_YY_MM_DD_REG1** need to be written simultaneously, write the **RTC_YY_MM_DD_REG1** firstly**.**

Note2: The number of days in different month may be different.

9.13.6. A012h RTC YY-MM-DD Register 1

Default: 0x0000			**Register Name: RTC_YY_MM_DD_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:7	/	/	/
6	R/W	0x0	LEAP. Leap Year. 0: not, 1: Leap year. This bit can not set by hardware. It should be set or clear by software.
5:0	R/W	x	YEAR. Year. Range from 0~63.

Note1: If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area. If the **RTC_YY_MM_DD_REG0** and **RTC_YY_MM_DD_REG1** need to be written simultaneously, write the **RTC_YY_MM_DD_REG1** firstly**.**

Note2: The number of days in different month may be different.

9.13.7. A014h RTC HH-MM-SS Register 0

Default: 0x0000			**Register Name: RTC_HH_MM_SS_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND. Range from 0~59

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area. If the **RTC_HH_MM_SS_REG0** and **RTC_HH_MM_SS_REG1** need to be written simultaneously, write the **RTC_HH_MM_SS_REG1** firstly**.**

9.13.8. A016h RTC HH-MM-SS Register 1

Default: 0x0000	**Register Name: RTC_HH_MM_SS_REG1**

Bit	Read/Write	Default/Hex	Description
15:13	R/W	x	WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday 111: /
12:5	/	/	/
4:0	R/W	x	HOUR. Range from 0~23

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area. If the **RTC_HH_MM_SS_REG0** and **RTC_HH_MM_SS_REG1** need to be written simultaneously, write the **RTC_HH_MM_SS_REG1** firstly**.**

9.13.9. A020h Alarm 0 Counter Register 0

Default: 0x0000			Register Name: ALARM0_COUNTER_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	ALARM0_COUNTER_LOW. Alarm 0 Counter is Based on Second.

Note: If the second is set to 0, it will be 1 second in fact.

9.13.10. A022h Alarm 0 Counter Register 1

Default: 0x0000			Register Name: ALARM0_COUNTER_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	ALARM0_COUNTER_HIGH. Alarm 0 Counter is Based on Second.

Note: If the second is set to 0, it will be 1 second in fact.

9.13.11. A024h Alarm 0 Current Value Register 0

Default:			Register Name: ALARM0_CUR_VLU_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	RO	x	ALARM0_CUR_VLU_LOW. Check Alarm 0 Counter Current Values.

Note: If the second is set to 0, it will be 1 second in fact.

9.13.12. A026h Alarm 0 Current Value Register 1

Default:			**Register Name: ALARM0_CUR_VLU_REG1**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	RO	x	ALARM0_CUR_VLU_HIGH. Check Alarm 0 Counter Current Values.

Note: If the second is set to 0, it will be 1 second in fact.

9.13.13. A028h Alarm 0 Enable Register

Default: 0x0000			**Register Name: ALARM0_ENABLE_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	ALM_0_EN Alarm 0 Enable. If this bit is set to "1", the Alarm 0 Counter register's valid bits will down count to zero, and the alarm pending bit will be set to "1". 0: Disable 1: Enable

9.13.14. A02Ch Alarm 0 IRQ Enable Register

Default: 0x0000			**Register Name: ALARM0_IRQ_EN**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_EN. Alarm 0 IRQ Enable. 0: Disable 1: Enable

9.13.15. A030h Alarm 0 IRQ Status Register

Default: 0x0000			**Register Name: ALARM0_IRQ_STA_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	ALARM0_IRQ_PEND. Alarm 0 IRQ Pending bit. 0: No effect 1: Pending, alarm 0 counter value is reached If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.

9.13.16. A040h Alarm 1 Week HH-MM-SS Register 0

Default: 0x0000			Register Name: ALARM1_WK_HH_MM-SS_REG0
Bit	**Read/Write**	**Default/Hex**	**Description**
15:14	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59.
7:6	/	/	/
5:0	R/W	x	SECOND. Range from 0~59.

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

9.13.17. A042h Alarm 1 Week HH-MM-SS Register 1

Default: 0x0000			Register Name: ALARM1_WK_HH_MM-SS_REG1
Bit	**Read/Write**	**Default/Hex**	**Description**
31:21	/	/	/
4:0	R/W	x	HOUR. Range from 0~23.

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

9.13.18. A044h Alarm 1 Enable Register

Default: 0x0000			Register Name: ALARM1_EN_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:7	/	/	/
6	R/W	0x0	WK6_ALM1_EN. Week 6 (Sunday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 6, the week 6 alarm irq pending bit will be set to “1”.
5	R/W	0x0	WK5_ALM1_EN. Week 5 (Saturday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 5, the week 5 alarm irq pending bit will be set

			to “1”.
4	R/W	0x0	WK4_ALM1_EN. Week 4 (Friday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 4, the week 4 alarm irq pending bit will be set to “1”.
3	R/W	0x0	WK3_ALM1_EN. Week 3 (Thursday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 3, the week 3 alarm irq pending bit will be set to “1”.
2	R/W	0x0	WK2_ALM1_EN. Week 2 (Wednesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 2, the week 2 alarm irq pending bit will be set to “1”.
1	R/W	0x0	WK1_ALM1_EN. Week 1 (Tuesday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 1, the week 1 alarm irq pending bit will be set to “1”.
0	R/W	0x0	WK0_ALM1_EN. Week 0 (Monday) Alarm 1 Enable. 0: Disable 1: Enable If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 0, the week 0 alarm irq pending bit will be set to “1”.

9.13.19. A048h Alarm 1 IRQ Enable Register

Default: 0x0000	**Register Name: ALARM1_IRQ_EN**

Bit	Read/Write	Default/Hex	Description
15:1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN. Alarm 1 IRQ Enable. 0: Disable 1: Enable

9.13.20. A04Ch Alarm 1 IRQ Status Register

Default: 0x0000			Register Name: ALARM1_IRQ_STA_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect 1: Pending, week counter value is reached If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

9.13.21. A050h Alarm Config Register

Default: 0x0000			Register Name: ALARM_CONFIG_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: Disable alarm wake up output 1: Enable alarm wake up output

9.13.22. A060h LOSC Output Gating Register

Default: 0x0000			Register Name: LOSC_OUT_GATING_REG
Bit	**Read/Write**	**Default/Hex**	**Description**
15:1	/	/	/
0	R/W	0x0	LOSC_OUT_GATING. Configuration of LOSC output, and no LOSC output by default. 0: Enable LOSC output gating 1: Disable LOSC output gating

9.13.23. A100h ~ A13eh General Purpose Register

Default: 0x0000			Register Name: GP_DATA_REGn
Bit	**Read/Write**	**Default/Hex**	**Description**

15:0	R/W	0x0	GP_DATA. Data [15:0].

Note: general purpose register 0~31 value can be stored if the VDD_RTC is larger than 1.0v.

9.13.24. A170h RTC Debug Register

Default: 0x0000			**Register Name: RTC_DEB_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:2	/	/	/
1	R/W	0x0	RTC_TEST_MODE_CTRL. RTC TEST Mode Control bit.
0	R/W	0x0	RTC_DEBUG. RTC Simulation Control bit 0: No effect. 1: simulation mode

9.13.25. A190h VDD RTC Regulation Register

Default: 0x0004			**Register Name: VDD_RTC_REG**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:3	/	/	/
2:0	R/W	0x100	VDD_RTC_REGU. These bits are useful for regulating the RTC_VIO from 0.7v to 1.4v, and the regulation step is 0.1v. (Voltage =VDD_RTC_REGU*3.3/3) 000: 0.7v 001: 0.8v 010: 0.9v 011: 1.0v 100: 1.1v 101: 1.2v 110: 1.3v 111: 1.4v

9.13.26. A1F0h IC Characteristic Register 0

Default: 0x0000			**Register Name: IC_CHARA_REG0**
Bit	**Read/Write**	**Default/Hex**	**Description**
15:0	R/W	0x0	ID_DATA. Return 0x16ab only if the KEY_FIELD is set as 0x16ab when read those bits, otherwise return 0x0.

9.13.27. A1F2h IC Characteristic Register 1

Default: 0x0000	**Register Name: IC_CHARA_REG1**

Bit	Read/Write	Default/Hex	Description
15:0	R/W	0x0	IC_CHARA. Key Field. Should be written at value 0x16ab. Writing any other value in this field aborts the write operation.

Chapter 10 Reference

Figure 10-1 shows the reference schematic of QFN68 Package.

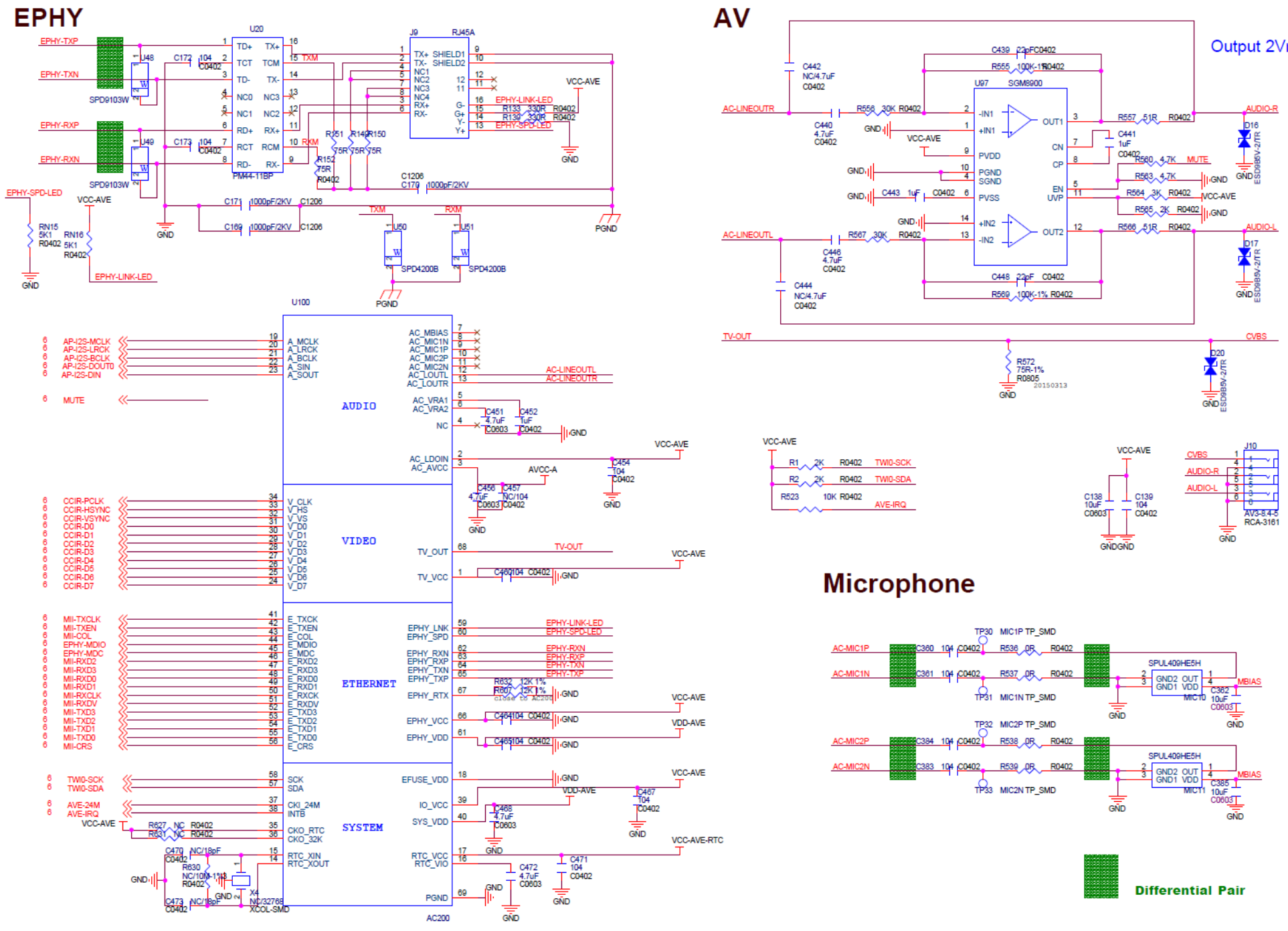


Figure 10-1. QFN68 Package reference schematic

