Boxchip F20 Datasheet

V1.01

2010-12-12

Boxchip

Revision History

Version	Date	Section/ Page	Changes compared to previous issue
V1.00	2010-11-21		Initial version
V1.01	2010-12-12	TBD	TBD

Table of Contents

1. Introduce

The F20 is a 16/32-bit RISC microprocessor, which is designed to provide a cost-effective, low-power capabilities, high performance processor for video application and general application. The F20 is developed with ARM926-EJS core with separated 16KB instruction and 16KB data caches. To reduce total system cost, the F20 includes the following components.

2. Feature List

The system includes the following feature:

- Around 400MHz@1.3V, 533MHz@1.4V ARM926-EJS Core with 16KB I-Cache/16KB D-Cache
- 16/32-bits SDRAM controller support SDR SDRAM, DDR SDRAM, DDR2 SDRAM and LPDDR SDRAM
- 8-ch normal DMA controllers and 8-ch dedicated DMA controllers
- 8 UARTs with 64 Bytes TX FIFO and 64 Bytes RX FIFO, 1 UART with full modem function, 2 UARTs with RTS/CTS hardware flow control, others are two wire UARTs
- 3 SPI controller, 1 dedicated SPI controller for serial NOR Flash boot application, others are for general applications
- 2 PS2 controller for connecting external PS2 mouse and PS2 keypad
- CAN bus controller for automotive and general industrial environments
- 3 Two Wire Interface, its speed can up to 400K
- Key Matrix (8x8) with internal debounce filter
- IR controller support SIR, MIR, FIR and IR remoter
- Smart Card Read controller for security application
- 8-bits NAND Flash Controller with 8 chip select and 2 r/b signals
- 1 high-speed Memory controller supports SD version 3.0 and MMC version 4.2
- 3 normal Memory controller supports SD version 2.0 and MMC version 4.0
- Memory Stick Host Controller supports memory stick version 1.0 and memory stick PRO
- ATA controller used for IDE hard disc or CF card
- 3 USB 2.0 OTG controller for general application
- 10/100M Ethernet MAC compatible with IEEE802.3 standard
- Transport stream controller for DTV application
- I2S/PCM controller for 8-channel output and 2-channel input
- AC97 controller compatible with AC97 version 2.3 standard
- Internal 24-bits Audio Codec for 2 channel headphone, 2 channel microphone and 2 channel FM/Linen input
- Internal 6-bits LRADC for line control
- Internal 4-wire touch panel controller for touch application

- Multi format video codec
- Multi path video output
- TFBGA400 package

3. Functional Block Diagram

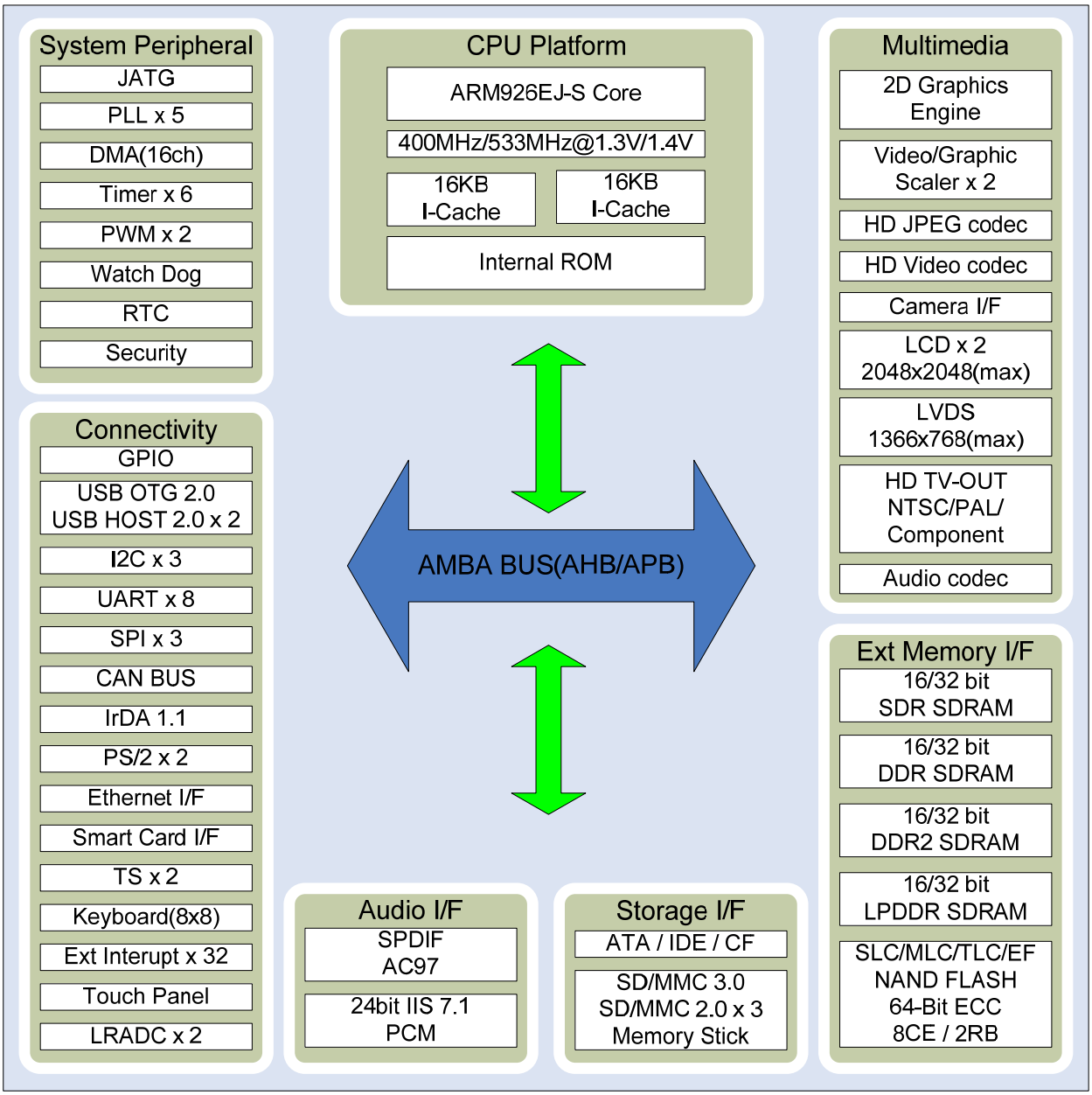


Figure 3-1 F20 Functional Block Diagram

4. Pin Assignments

4.1. Dimension

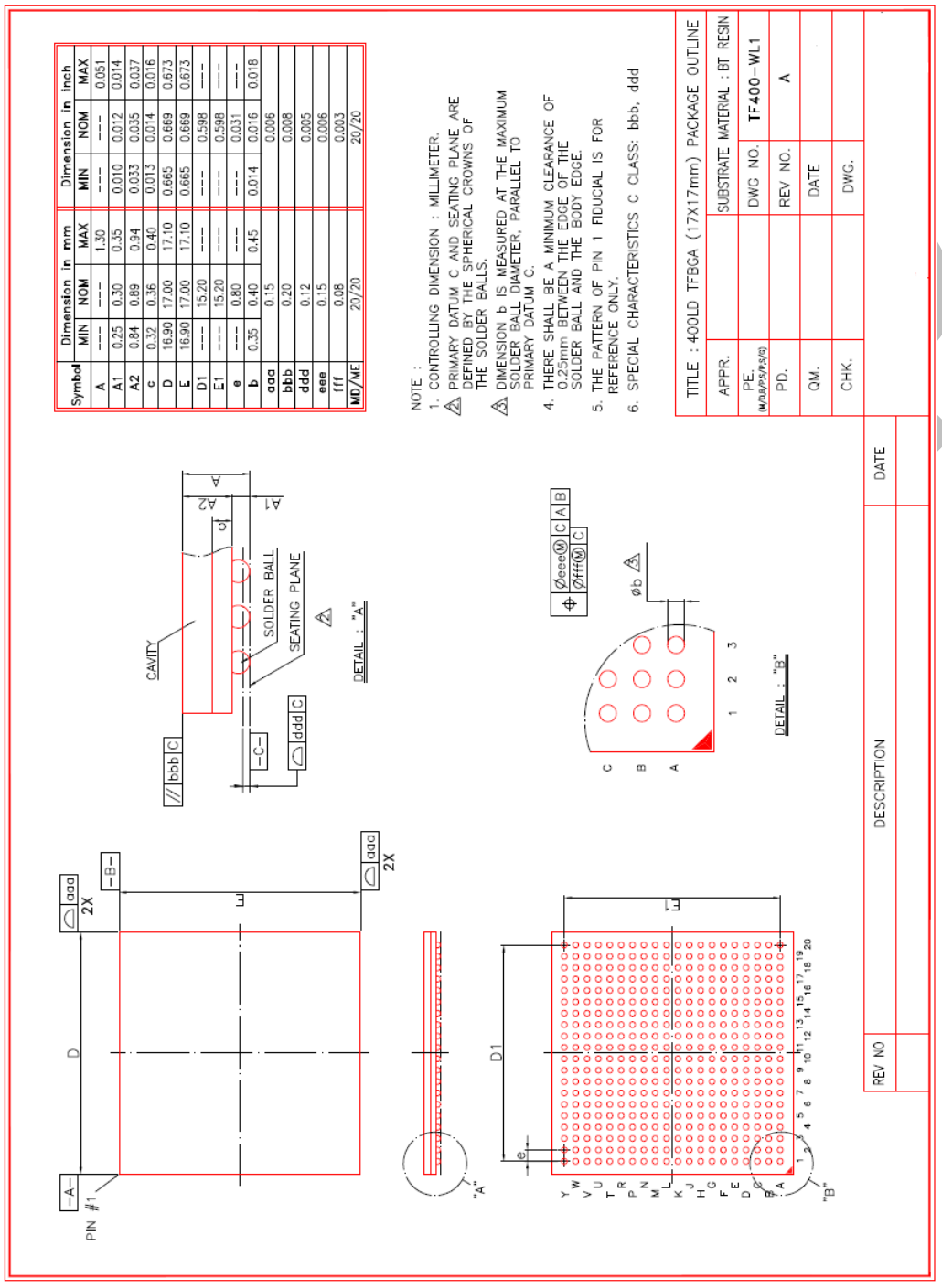
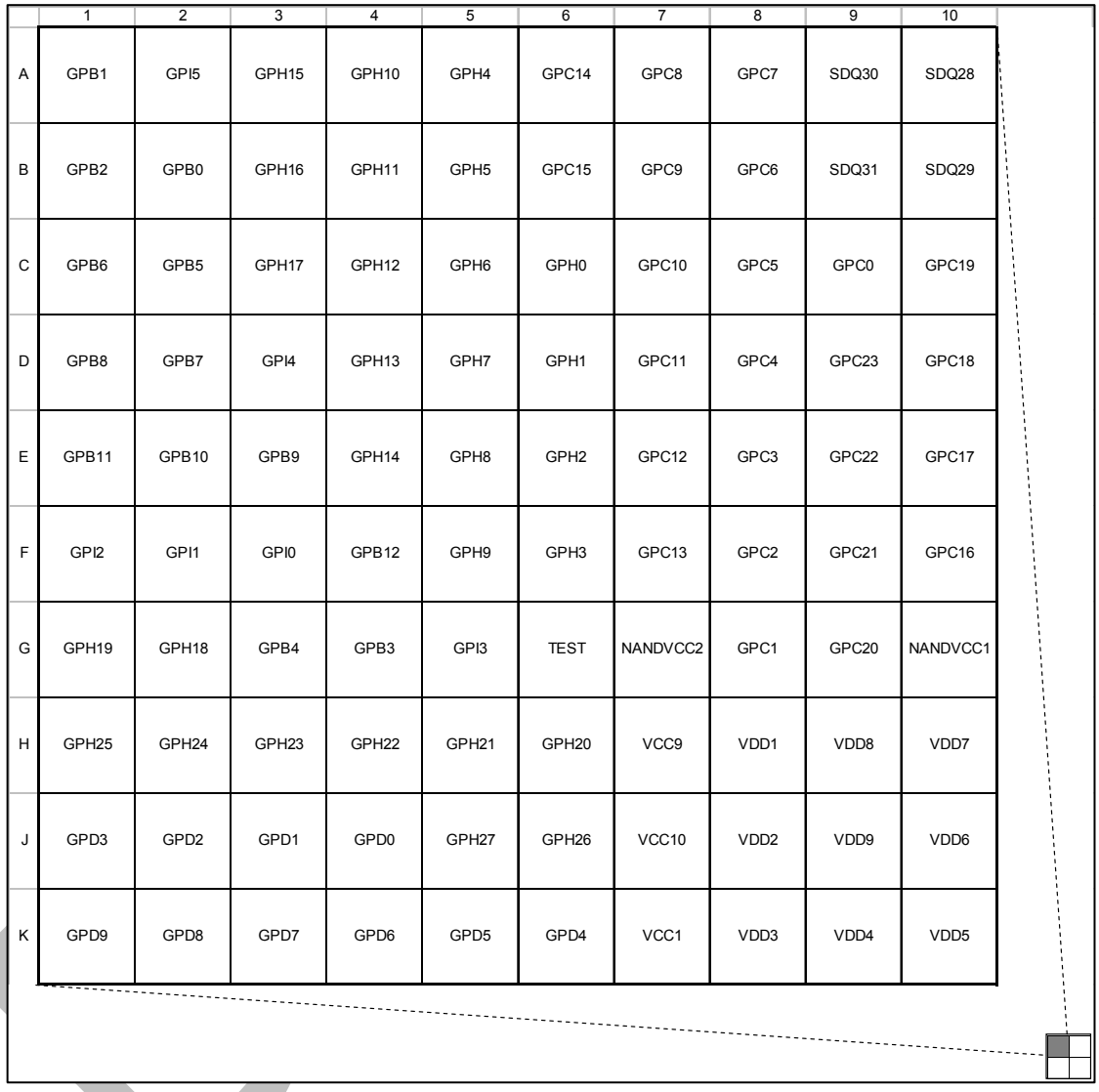


Figure 4-1 F20 FBGA400 Package Dimension

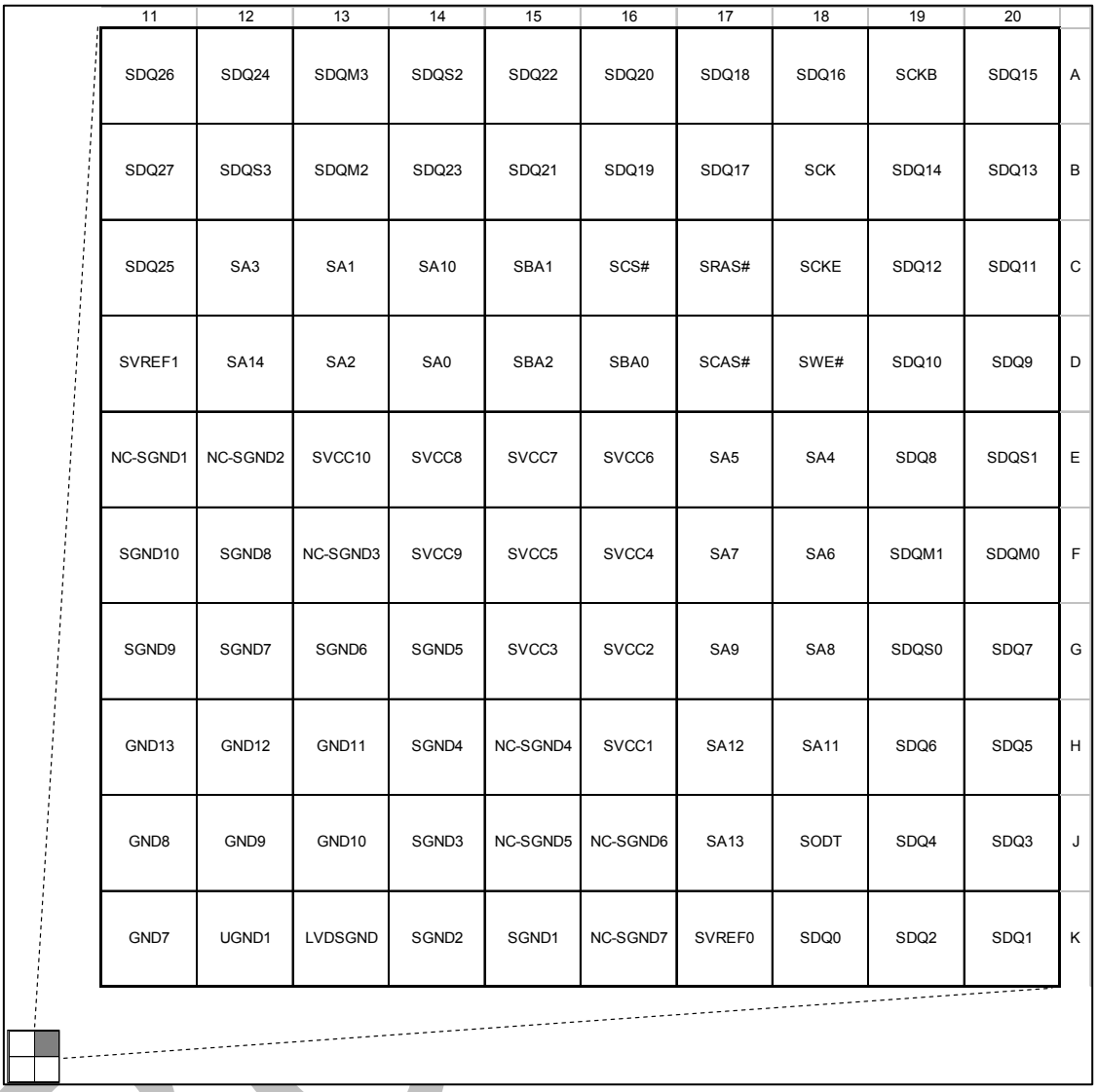
4.2. Pin Map

The following pin maps show the top view of the 400-pin FBGA package pin assignments in four quadrants (A, B, C, D).



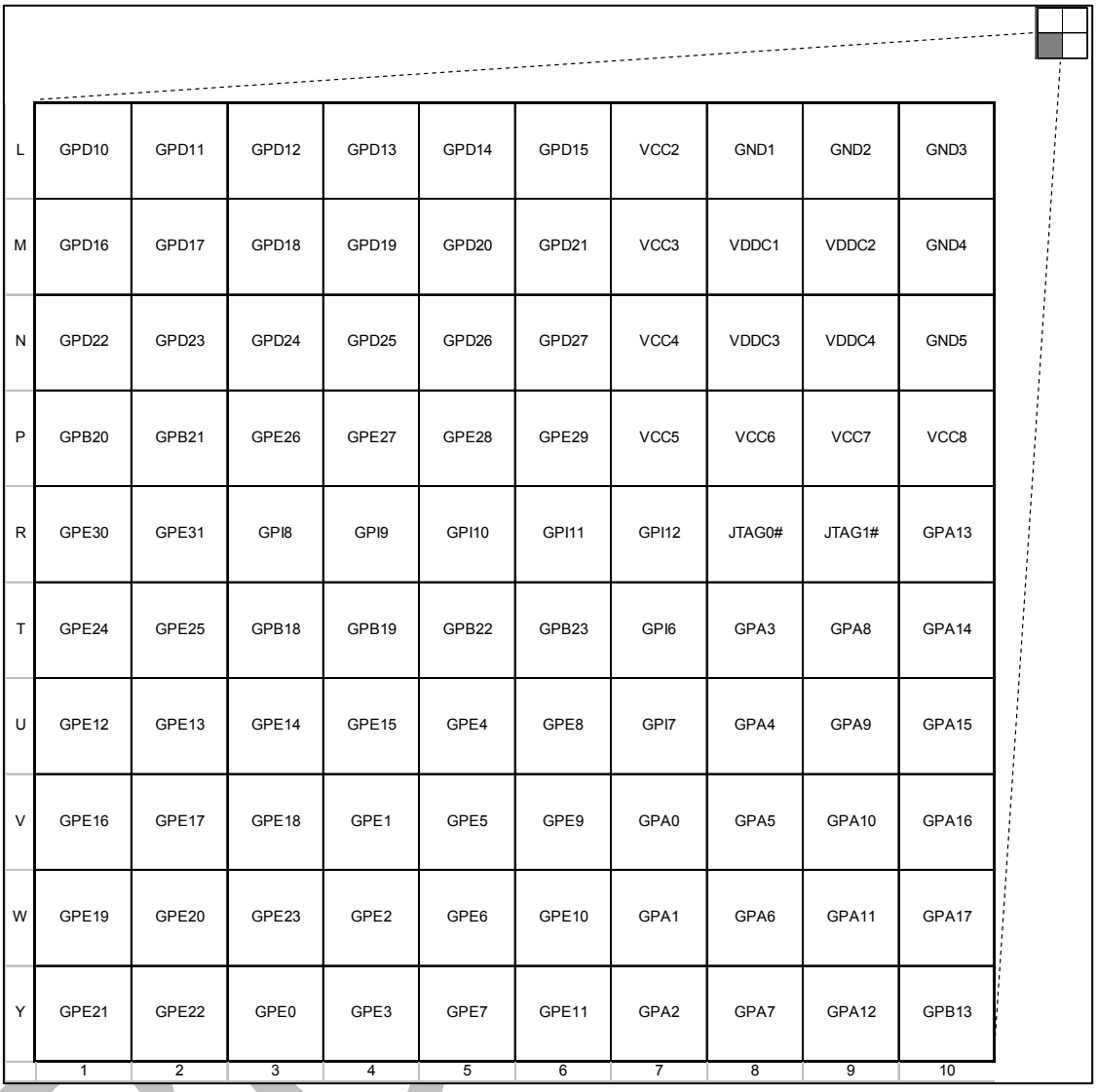
	1	2	3	4	5	6	7	8	9	10
A	GPB1	GPI5	GPH15	GPH10	GPH4	GPC14	GPC8	GPC7	SDQ30	SDQ28
B	GPB2	GPB0	GPH16	GPH11	GPH5	GPC15	GPC9	GPC6	SDQ31	SDQ29
C	GPB6	GPB5	GPH17	GPH12	GPH6	GPH0	GPC10	GPC5	GPC0	GPC19
D	GPB8	GPB7	GPI4	GPH13	GPH7	GPH1	GPC11	GPC4	GPC23	GPC18
E	GPB11	GPB10	GPB9	GPH14	GPH8	GPH2	GPC12	GPC3	GPC22	GPC17
F	GPI2	GPI1	GPI0	GPB12	GPH9	GPH3	GPC13	GPC2	GPC21	GPC16
G	GPH19	GPH18	GPB4	GPB3	GPI3	TEST	NANDVCC2	GPC1	GPC20	NANDVCC1
H	GPH25	GPH24	GPH23	GPH22	GPH21	GPH20	VCC9	VDD1	VDD8	VDD7
J	GPD3	GPD2	GPD1	GPD0	GPH27	GPH26	VCC10	VDD2	VDD9	VDD6
K	GPD9	GPD8	GPD7	GPD6	GPD5	GPD4	VCC1	VDD3	VDD4	VDD5

Figure 4-2 FBGA400 Pin Map-Top View [Quadrant A]



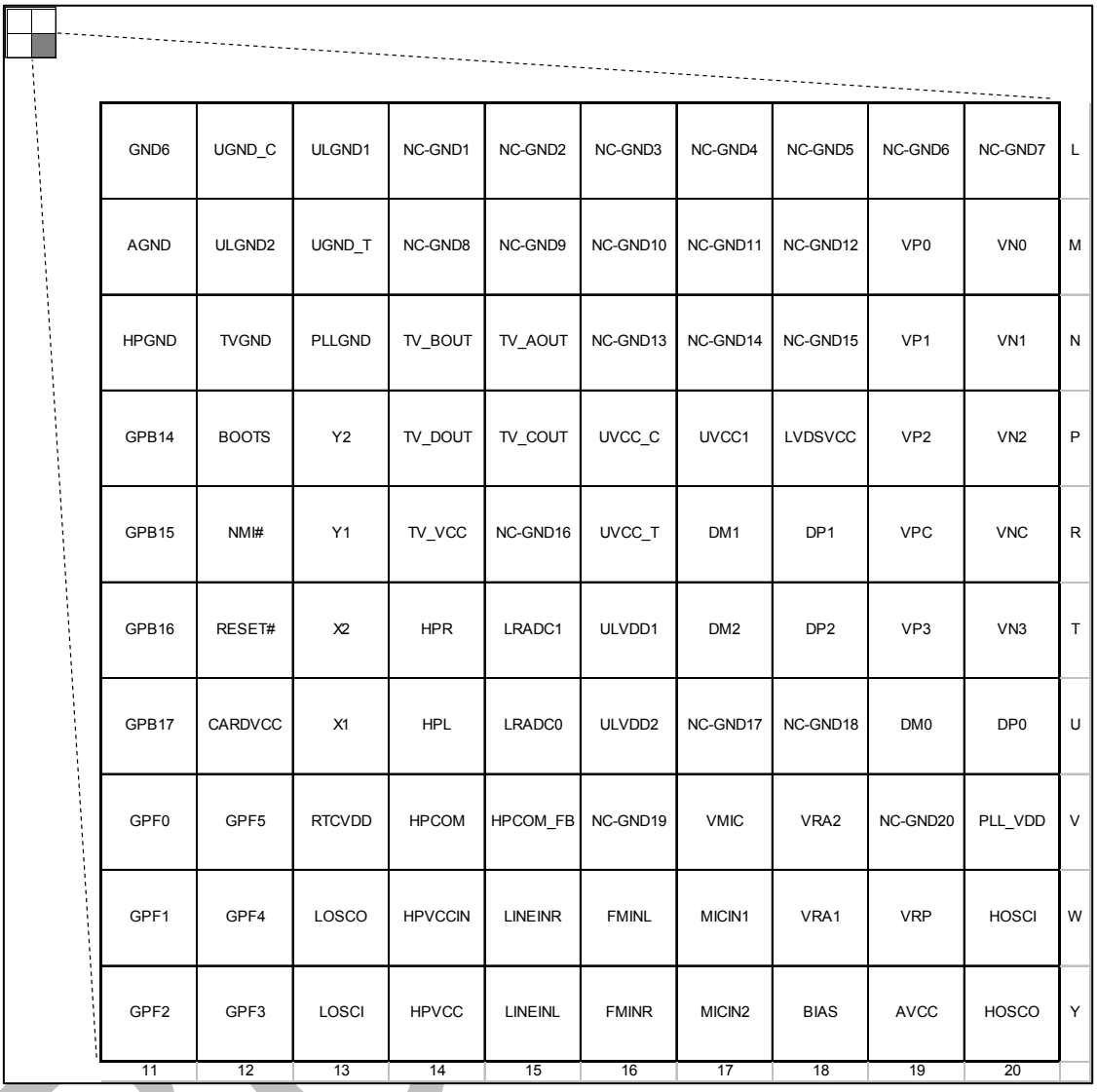
11	12	13	14	15	16	17	18	19	20	
SDQ26	SDQ24	SDQM3	SDQS2	SDQ22	SDQ20	SDQ18	SDQ16	SCKB	SDQ15	A
SDQ27	SDQS3	SDQM2	SDQ23	SDQ21	SDQ19	SDQ17	SCK	SDQ14	SDQ13	B
SDQ25	SA3	SA1	SA10	SBA1	SCS#	SRAS#	SCKE	SDQ12	SDQ11	C
SVREF1	SA14	SA2	SA0	SBA2	SBA0	SCAS#	SWE#	SDQ10	SDQ9	D
NC-SGND1	NC-SGND2	SVCC10	SVCC8	SVCC7	SVCC6	SA5	SA4	SDQ8	SDQS1	E
SGND10	SGND8	NC-SGND3	SVCC9	SVCC5	SVCC4	SA7	SA6	SDQM1	SDQM0	F
SGND9	SGND7	SGND6	SGND5	SVCC3	SVCC2	SA9	SA8	SDQS0	SDQ7	G
GND13	GND12	GND11	SGND4	NC-SGND4	SVCC1	SA12	SA11	SDQ6	SDQ5	H
GND8	GND9	GND10	SGND3	NC-SGND5	NC-SGND6	SA13	SODT	SDQ4	SDQ3	J
GND7	UGND1	LVDSGND	SGND2	SGND1	NC-SGND7	SVREF0	SDQ0	SDQ2	SDQ1	K

Figure 4-3 FBGA400 Pin Map-Top View [Quadrant B]



	1	2	3	4	5	6	7	8	9	10
L	GPD10	GPD11	GPD12	GPD13	GPD14	GPD15	VCC2	GND1	GND2	GND3
M	GPD16	GPD17	GPD18	GPD19	GPD20	GPD21	VCC3	VDDC1	VDDC2	GND4
N	GPD22	GPD23	GPD24	GPD25	GPD26	GPD27	VCC4	VDDC3	VDDC4	GND5
P	GPB20	GPB21	GPE26	GPE27	GPE28	GPE29	VCC5	VCC6	VCC7	VCC8
R	GPE30	GPE31	GPI8	GPI9	GPI10	GPI11	GPI12	JTAG0#	JTAG1#	GPA13
T	GPE24	GPE25	GPB18	GPB19	GPB22	GPB23	GPI6	GPA3	GPA8	GPA14
U	GPE12	GPE13	GPE14	GPE15	GPE4	GPE8	GPI7	GPA4	GPA9	GPA15
V	GPE16	GPE17	GPE18	GPE1	GPE5	GPE9	GPA0	GPA5	GPA10	GPA16
W	GPE19	GPE20	GPE23	GPE2	GPE6	GPE10	GPA1	GPA6	GPA11	GPA17
Y	GPE21	GPE22	GPE0	GPE3	GPE7	GPE11	GPA2	GPA7	GPA12	GPB13

Figure 4-4 FBGA400 Pin Map-Top View [Quadrant C]



GND6	UGND_C	ULGND1	NC-GND1	NC-GND2	NC-GND3	NC-GND4	NC-GND5	NC-GND6	NC-GND7	L
AGND	ULGND2	UGND_T	NC-GND8	NC-GND9	NC-GND10	NC-GND11	NC-GND12	VP0	VN0	M
HPGND	TVGND	PLLGND	TV_BOUT	TV_AOUT	NC-GND13	NC-GND14	NC-GND15	VP1	VN1	N
GPB14	BOOTS	Y2	TV_DOUT	TV_COUT	UVCC_C	UVCC1	LVDSVCC	VP2	VN2	P
GPB15	NMI#	Y1	TV_VCC	NC-GND16	UVCC_T	DM1	DP1	VPC	VNC	R
GPB16	RESET#	X2	HPR	LRADC1	ULVDD1	DM2	DP2	VP3	VN3	T
GPB17	CARDVCC	X1	HPL	LRADC0	ULVDD2	NC-GND17	NC-GND18	DM0	DP0	U
GPF0	GPF5	RTCVDD	HPCOM	HPCOM_FB	NC-GND19	VMIC	VRA2	NC-GND20	PLL_VDD	V
GPF1	GPF4	LOSCO	HPVCCIN	LINEINR	FMINL	MICIN1	VRA1	VRP	HOSCI	W
GPF2	GPF3	LOSCI	HPVCC	LINEINL	FMINR	MICIN2	BIAS	AVCC	HOSCO	Y
11	12	13	14	15	16	17	18	19	20	

Figure 4-5 FBGA400 Pin Map-Top View [Quadrant D]

5. Pin Description

5.1. Pin Characteristics

Through describe the terminal characteristics and the signals multiplexed on each pin for the FBGA package. The following list describes the table column headers.

1. **BALL#:** Ball numbers on the bottom side associated with each signals on the bottom.
2. **Pin Name:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in function 0).
3. **Function:** Multiplexing function number.
   Function 0 is the the default function, but is not necessarily the primary mode.
   Functions 1 to 5 are possible modes for alternate functions.
4. **Type:** signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - A = Analog
   - PWR = Power
   - GND = Ground
5. **Pin Reset State:** The state of the terminal at reset (power up).
   - 0: The buffer drives VOL(pull down/pull up resistor not activated)
   - 0 (PD): The buffer drives V_{OL} with an active pull down resistor.
   - 1: The buffer drives VOH (pull down/pull up resistor not activated).
   - 1 (PU): The buffer drives V_{OH} with an active pull up resistor.
   - Z: High-impedance
   - L: High-impedance with an active pull down resistor.
   - H: High-impedance with an active pull up resistor.
6. **Pull Up/Down:** Denotes the presence of an internal pull up or pull down resister. Pull up and pull down resistor can be enabled or disabled via software.
7. **Buffer Strength:** Drive strength of the associated output buffer.

Table 5-1 Pin Characteristics (FBGA400)

Table 5-1

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
K18	SDQ0	0	I/O			
K20	SDQ1	0	I/O			
K19	SDQ2	0	I/O			
J20	SDQ3	0	I/O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
J19	SDQ4	0	I/O			
H20	SDQ5	0	I/O			
H19	SDQ6	0	I/O			
G20	SDQ7	0	I/O			
E19	SDQ8	0	I/O			
D20	SDQ9	0	I/O			
D19	SDQ10	0	I/O			
C20	SDQ11	0	I/O			
C19	SDQ12	0	I/O			
B20	SDQ13	0	I/O			
B19	SDQ14	0	I/O			
A20	SDQ15	0	I/O			
A18	SDQ16	0	I/O			
B17	SDQ17	0	I/O			
A17	SDQ18	0	I/O			
B16	SDQ19	0	I/O			
A16	SDQ20	0	I/O			
B15	SDQ21	0	I/O			
A15	SDQ22	0	I/O			
B14	SDQ23	0	I/O			
A12	SDQ24	0	I/O			
C11	SDQ25	0	I/O			
A11	SDQ26	0	I/O			
B11	SDQ27	0	I/O			
A10	SDQ28	0	I/O			
B10	SDQ29	0	I/O			
A9	SDQ30	0	I/O			
B9	SDQ31	0	I/O			
K17	SVREF0	0				
D11	SVREF1	0				
G19	SDQS0	0	I/O			
F20	SDQM0	0	O			
E20	SDQS1	0	I/O			
F19	SDQM1	0	O			
A14	SDQS2	0	I/O			
B13	SDQM2	0	O			
B12	SDQS3	0	I/O			
A13	SDQM3	0	O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
A19	SCK#	0	O			
B18	SCK	0	O			
C18	SCKE	0	O			
D14	SA0	0	O			
C13	SA1	0	O			
D13	SA2	0	O			
C12	SA3	0	O			
E18	SA4	0	O			
E17	SA5	0	O			
F18	SA6	0	O			
F17	SA7	0	O			
G18	SA8	0	O			
G17	SA9	0	O			
C14	SA10	0	O			
H18	SA11	0	O			
H17	SA12	0	O			
J17	SA13	0	O			
D12	SA14	0	O			
D16	SBA0	0	O			
C15	SBA1	0	O			
D15	SBA2	0	O			
D18	SWE#	0	O			
D17	SCAS#	0	O			
C17	SRAS#	0	O			
C16	SCS#	0	O			
J18	SDOT	0	O			
V7	PA0	0	I/O			
	ERXD3	1				
	SPI1_CS0	2				
	UART2_RTS	3				
W7	PA1	0	I/O			
	ERXD2	1				
	SPI1_CLK	2				
	UART2_CTS	3				
Y7	PA2	0	I/O			
	ERXD1	1				
	SPI1_MOSI	2				
	UART2_TX	3				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
T8	PA3	0	I/O			
	ERXD0	1				
	SPI1_MISO	2				
	UART2_RX	3				
U8	PA4	0	I/O			
	ETXD3	1				
	SDC3_D3	2				
V8	PA5	0	I/O			
	ETXD2	1				
	SDC3_D2	2				
W8	PA6	0	I/O			
	ETXD1	1				
	SDC3_D1	2				
Y8	PA7	0	I/O			
	ETXD0	1				
	SDC3_D0	2				
T9	PA8	0	I/O			
	ERXCK	1				
	SDC3_CLK	2				
U9	PA9	0	I/O			
	ERXERR	1				
	SDC3_CMD	2				
V9	PA10	0	I/O			
	ERXDV	1				
	UART1_TX	3				
W9	PA11	0	I/O			
	EMDC	1				
	UART1_RX	3				
Y9	PA12	0	I/O			
	EMDIO	1				
	UART6_TX	2				
	UART1_RST	3				
R10	PA13	0	I/O			
	ETXEN	1				
	UART6_RX	2				
	UART1_CTS	3				
T10	PA14	0	I/O			
	ETXCK	1				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	UART7_TX	2				
	UART1_DTR	3				
U10	PA15	0	I/O			
	ECRS	1				
	UART7_RX	2				
	UART1_DSR	3				
V10	PA16	0	I/O			
	ECOL	1				
	CAN_TX	2				
	UART1_DCD	3				
W10	PA17	0	I/O			
	ETXERR	1				
	CAN_RX	2				
	UART1_RING	3				
B2	PB0	0	I/O			
	TWI0_SCK	1				
A1	PB1	0	I/O			
	TWI0_SDA	1				
B1	PB2	0	I/O			
	PWM0	1				
G4	PB3	0	I/O			
	IR_TX	1				
	SPDIF_MCLK	3				
	EINT16	5				
G3	PB4	0	I/O			
	IR_RX	1				
C2	PB5	0	I/O			
	I2S_MCLK	1				
	AC97_MCLK	2				
C1	PB6	0	I/O			
	I2S_BCLK	1				
	AC97_BCLK	2				
D2	PB7	0	I/O			
	I2S_LRCK	1				
	AC97_SYNC	2				
D1	PB8	0	I/O			
	I2S_DO0	1				
	AC97_DO	2				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
E3	PB9	0	I/O			
	I2S_DO1	1				
	GPS_CLK	2				
	EINT17	5				
E2	PB10	0	I/O			
	I2S_DO2	1				
	GPS_SIGN	2				
	EINT18	5				
E1	PB11	0	I/O			
	I2S_DO3	1				
	GPS_MAG	2				
	EINT19	5				
F4	PB12	0	I/O			
	I2S_DI	1				
	AC97_DI	2				
	SPDIF_DI	3				
Y10	PB13	0	I/O			
	SPI2_CS1	1				
	SPDIF_DO	3				
P11	PB14	0	I/O			
	SPI2_CS0	1				
	JTAG_MS0	2				
R11	PB15	0	I/O			
	SPI2_CLK	1				
	JTAG_CK0	2				
T11	PB16	0	I/O			
	SPI2_MOSI	1				
	JTAG_DO0	2				
U11	PB17	0	I/O			
	SPI2_MOSO	1				
	JTAG_DI0	2				
T3	PB18	0	I/O			
	TWI1_SCK	1				
	PS2_SCK0	2				
	ENT20	5				
T4	PB19	0	I/O			
	TWI1_SDA	1				
	PS2_SDA0	2				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	EINT21	5				
P1	PB20	0	I/O			
	TWI2_SCK	1				
	EINT22	5				
P2	PB21	0	I/O			
	TWI2_SDA	1				
	EINT23	5				
T5	PB22	0	I/O			
	UART0_TX	1				
T6	PB23	0	I/O			
	UART0_RX	1				
C9	PC0	0	I/O			
	NWE	1				
	SPI0_MOSI	2				
G8	PC1	0	I/O			
	NALE	1				
	SPI0_MISO	2				
F8	PC2	0	I/O			
	NCLE	1				
	SPI0_CLK	2				
E8	PC3	0	I/O		Pull Up (default)	
	NCE1	1				
	SDC1_CMD	2				
D8	PC4	0	I/O		Pull Up (default)	
	NCE0	1				
C8	PC5	0	I/O			
	NRD	1				
	SDC1_CLK	2				
B8	PC6	0	I/O		Pull Up (default)	
	NRB0	1				
	SDC2_CMD	2				
A8	PC7	0	I/O		Pull Up (default)	
	NRB1	1				
	SDC2_CLK	2				
A7	PC8	0	I/O			
	ND0	1				
	SDC2_D0	2				
B7	PC9	0	I/O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	ND1	1				
	SDC2_D1	2				
C7	PC10	0	I/O			
	ND2	1				
	SDC2_D2	2				
D7	PC11	0	I/O			
	ND3	1				
	SDC2_D3	2				
E7	PC12	0	I/O			
	ND4	1				
	SDC1_D0	2				
F7	PC13	0	I/O			
	ND5	1				
	SDC1_D1	2				
A6	PC14	0	I/O			
	ND6	1				
	SDC1_D2	2				
B6	PC15	0	I/O			
	ND7	1				
	SDC1_D3	2				
F10	PC16	0	I/O		Pull Down (default)	
	NWP	1				
E10	PC17	0	I/O		Pull Up (default)	
	NCE2	1				
D10	PC18	0	I/O		Pull Up (default)	
	NCE3	1				
C10	PC19	0	I/O			
	NCE4	1				
	SPI2_CS0	2				
	EINT12	5				
G9	PC20	0	I/O			
	NCE5	1				
	SPI2_CLK	2				
	EINT13	5				
F9	PC21	0	I/O			
	NCE6	1				
	SPI2_MOSI	2				
	EINT14	5				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
E9	PC22	0	I/O			
	NCE7	1				
	SPI2_MISO	2				
	EINT15	5				
D9	PC23	0	I/O		Pull Up (default)	
	SPI0_CS0	2				
J4	PD0	0	I/O			
	LCD0_CLK	1				
	TS0_CLK	2				
	LCD1_CLK	3				
J3	PD1	0	I/O			
	LCD0_DE	1				
	TS0_ERR	2				
	LCD1_DE	3				
J2	PD2	0	I/O			
	LCD0_HSYNC	1				
	TS0_SYNC	2				
	LCD1_HSYNC	3				
J1	PD3	0	I/O			
	LCD0_VSYNC	1				
	TS0_DVLD	2				
	LCD1_VSYNC	3				
K6	PD4	0	I/O			
	LCD0_D0	1				
	KP_IN0	2				
	LCD1_D0	3				
K5	PD5	0	I/O			
	LCD0_D1	1				
	KP_IN1	2				
	LCD1_D1	3				
K4	PD6	0	I/O			
	LCD0_D2	1				
	KP_IN2	2				
	LCD1_D2	3				
K3	PD7	0	I/O			
	LCD0_D3	1				
	KP_IN3	2				
	LCD1_D3	3				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
K2	PD8	0	I/O			
	LCD0_D4	1				
	KP_IN4	2				
	LCD1_D4	3				
K1	PD9	0	I/O			
	LCD0_D5	1				
	KP_IN5	2				
	LCD1_D5	3				
L1	PD10	0	I/O			
	LCD0_D6	1				
	KP_IN6	2				
	LCD1_D6	3				
L2	PD11	0	I/O			
	LCD0_D7	1				
	KP_IN7	2				
	LCD1_D7	3				
L3	PD12	0	I/O			
	LCD0_D8	1				
	KP_IN8	2				
	LCD1_D8	3				
L4	PD13	0	I/O			
	LCD0_D9	1				
	KP_IN9	2				
	LCD1_D9	3				
L5	PD14	0	I/O			
	LCD0_D10	1				
	KP_IN10	2				
	LCD1_D10	3				
L6	PD15	0	I/O			
	LCD0_D11	1				
	KP_IN11	2				
	LCD1_D11	3				
M1	PD16	0	I/O			
	LCD0_D12	1				
	KP_IN12	2				
	LCD1_D12	3				
M2	PD17	0	I/O			
	LCD0_D13	1				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	KP_IN13	2				
	LCD1_D13	3				
M3	PD18	0	I/O			
	LCD0_D14	1				
	KP_IN14	2				
	LCD1_D14	3				
M4	PD19	0	I/O			
	LCD0_D15	1				
	KP_IN15	2				
	LCD1_D15	3				
M5	PD20	0	I/O			
	LCD0_D16	1				
	TS0_D0	2				
	LCD1_D16	3				
M6	PD21	0	I/O			
	LCD0_D17	1				
	TS0_D1	2				
	LCD1_D17	3				
N1	PD22	0	I/O			
	LCD0_D18	1				
	TS0_D2	2				
	LCD1_D18	3				
N2	PD23	0	I/O			
	LCD0_D19	1				
	TS0_D3	2				
	LCD1_D19	3				
N3	PD24	0	I/O			
	LCD0_D20	1				
	TS0_D4	2				
	LCD1_D20	3				
N4	PD25	0	I/O			
	LCD0_D21	1				
	TS0_D5	2				
	LCD1_D21	3				
N5	PD26	0	I/O			
	LCD0_D22	1				
	TS0_D6	2				
	LCD1_D22	3				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
N6	PD27	0	I/O			
	LCD0_D23	1				
	TS0_D7	2				
	LCD1_D23	3				
Y3	PE0	0	I/O			
	TS0_CLK	1				
	CSI0_PCK	2				
V4	PE1	0	I/O			
	TS0_ERR	1				
	CSI0_CK	2				
W4	PE2	0	I/O			
	TS0_SYNC	1				
	CSI0_HSYNC	2				
Y4	PE3	0	I/O			
	TS0_DVLD	1				
	CSI0_VSYNC	2				
U5	PE4	0	I/O			
	TS0_D0	1				
	CSI0_D0	2				
V5	PE5	0	I/O			
	TS0_D1	1				
	CSI0_D1	2				
	SMC_VPPEN	3				
W5	PE6	0	I/O			
	TS0_D2	1				
	CSI0_D2	2				
	SMC_VPPPP	3				
Y5	PE7	0	I/O			
	TS0_D3	1				
	CSI0_D3	2				
	SMC_DET	3				
U6	PE8	0	I/O			
	TS0_D4	1				
	CSI0_D4	2				
	SMC_VCCEN	3				
V6	PE9	0	I/O			
	TS0_D5	1				
	CSI0_D5	2				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	SMC_RST	3				
W6	PE10	0	I/O			
	TS0_D6	1				
	CSI0_D6	2				
	SMC_SLK	3				
Y6	PE11	0	I/O			
	TS0_D7	1				
	CSI0_D7	2				
	SMC_SDA	3				
U1	PE12	0	I/O			
	TS1_CLK	1				
	CSI1_PCK	2				
	SDC1_CMD	3				
U2	PE13	0	I/O			
	TS1_ERR	1				
	CSI1_CK	2				
	SDC1_CLK	3				
U3	PE14	0	I/O			
	TS1_SYNC	1				
	CSI1_HSYNC	2				
	SDC1_D0	3				
U4	PE15	0	I/O			
	TS1_DVLD	1				
	CSI1_VSYNC	2				
	SDC1_D1	3				
V1	PE16	0	I/O			
	TS1_D0	1				
	CSI1_D0	2				
	SDC1_D2	3				
V2	PE17	0	I/O			
	TS1_D1	1				
	CSI1_D1	2				
	SDC1_D3	3				
V3	PE18	0	I/O			
	TS1_D2	1				
	CSI1_D2	2				
	UART3_TX	3				
W1	PE19	0	I/O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	TS1_D3	1				
	CSI1_D3	2				
	UART3_RX	3				
W2	PE20	0	I/O			
	TS1_D4	1				
	CSI1_D4	2				
	UART3_RTS	3				
Y1	PE21	0	I/O			
	TS1_D5	1				
	CSI1_D5	2				
	UART3_CTS	3				
Y2	PE22	0	I/O			
	TS1_D6	1				
	CSI1_D6	2				
	UART3_TX	3				
W3	PE23	0	I/O			
	TS1_D7	1				
	CSI1_D7	2				
	UART3_RX	3				
T1	PE24	0	I/O			
	PS2_SCK0	1				
	EINT10	5				
T2	PE25	0	I/O			
	PS2_SDA0	1				
	EINT11	5				
P3	PE26	0	I/O			
	SDC3_CMD	1				
P4	PE27	0	I/O			
	SDC3_CLK	1				
P5	PE28	0	I/O			
	SDC3_D0	1				
P6	PE29	0	I/O			
	SDC3_D1	1				
R1	PE30	0	I/O			
	SDC3_D2	1				
R2	PE31	0	I/O			
	SDC3_D3	1				
V11	PF0	0	I/O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	SDC0_D1	1				
	MS_D1	2				
	JTAG_MS1	3				
	SDC2_D1	4				
W11	PF1	0	I/O			
	SDC0_D0	1				
	MS_D0	2				
	JTAG_DI1	3				
	SDC2_D0	4				
Y11	PF2	0	I/O			
	SDC0_CLK	1				
	MS_CLK	2				
	UART0_TX	3				
	SDC2_CLK	4				
Y12	PF3	0	I/O			
	SDC0_CMD	1				
	MS_BS	2				
	JTAG_DO1	3				
	SDC2_CMD	4				
W12	PF4	0	I/O			
	SDC0_D3	1				
	MS_D3	2				
	UART0_RX	3				
	SDC2_D3	4				
V12	PF5	0	I/O			
	SDC0_D2	1				
	MS_D2	2				
	JTAG_CK1	3				
	SDC2_D2	4				
T19	PG0	0	I/O			
	LVDS_VP3	1				
	EINT0	5				
T20	PG1	0	I/O			
	LVDS_VN3	1				
	EINT1	5				
R19	PG2	0	I/O			
	LVDS_VPC	1				
	EINT2	5				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
R20	PG3	0	I/O			
	LVDS_VNC	1				
	EINT3	5				
P19	PG4	0	I/O			
	LVDS_VP2	1				
	EINT4	5				
P20	PG5	0	I/O			
	LVDS_VN2	1				
	EINT5	5				
N19	PG6	0	I/O			
	LVDS_VP1	1				
	EINT6	5				
N20	PG7	0	I/O			
	LVDS_VN1	1				
	EINT7	5				
M19	PG8	0	I/O			
	LVDS_VP0	1				
	EINT8	5				
M20	PG9	0	I/O			
	LVDS_VN0	1				
	EINT9	5				
C6	PH0	0	I/O			
	LCD1_CLK	1				
	ATAA0	2				
	UART3_TX	3				
	EINT24	5				
D6	PH1	0	I/O			
	LCD1_DE	1				
	ATAA1	2				
	UART3_RX	3				
	EINT25	5				
E6	PH2	0	I/O			
	LCD1_HSYNC	1				
	ATAA2	2				
	UART3_RTS	3				
	EINT26	5				
F6	PH3	0	I/O			
	LCD1_VSYNC	1				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	ATAIRQ	2				
	UART3_CTS	3				
	EINT27	5				
A5	PH4	0	I/O			
	LCD1_D0	1				
	ATAD0	2				
	UART4_TX	3				
B5	PH5	0	I/O			
	LCD1_D1	1				
	ATAD1	2				
	UART4_RX	3				
C5	PH6	0	I/O			
	LCD1_D2	1				
	ATAD2	2				
	UART5_TX	3				
D5	PH7	0	I/O			
	LCD1_D3	1				
	ATAD3	2				
	UART5_RX	3				
E5	PH8	0	I/O			
	LCD1_D4	1				
	ATAD4	2				
	KP_IN0	3				
F5	PH9	0	I/O			
	LCD1_D5	1				
	ATAD5	2				
	KP_IN1	3				
A4	PH10	0	I/O			
	LCD1_D6	1				
	ATAD6	2				
	KP_IN2	3				
B4	PH11	0	I/O			
	LCD1_D7	1				
	ATAD7	2				
	KP_IN3	3				
C4	PH12	0	I/O			
	LCD1_D8	1				
	ATAD8	2				

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	PS2_SCK1	3				
D4	PH13	0	I/O			
	LCD1_D9	1				
	ATAD9	2				
	PS2_SDA1	3				
E4	PH14	0	I/O			
	LCD1_D10	1				
	ATAD10	2				
	PS2_KP_IN4	3				
A3	PH15	0	I/O			
	LCD1_D11	1				
	ATAD11	2				
	KP_IN5	3				
B3	PH16	0	I/O			
	LCD1_D12	1				
	ATAD12	2				
	KP_IN6	3				
C3	PH17	0	I/O			
	LCD1_D13	1				
	ATAD13	2				
	KP_IN7	3				
G2	PH18	0	I/O			
	LCD1_D14	1				
	ATAD14	2				
	KP_OUT0	3				
G1	PH19	0	I/O			
	LCD1_D15	1				
	ATAD15	2				
	KP_OUT1	3				
H6	PH20	0	I/O			
	LCD1_D16	1				
	ATAOE	2				
	CAN_TX	3				
H5	PH21	0	I/O			
	LCD1_D17	1				
	ATADREQ	2				
	CAN_RX	3				
H4	PH22	0	I/O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	LCD1_D18	1				
	ATADACK	2				
	KP_OUT2	3				
H3	PH23	0	I/O			
	LCD1_D19	1				
	ATACS0	2				
	KP_OUT3	3				
H2	PH24	0	I/O			
	LCD1_D20	1				
	ATACS1	2				
	KP_OUT4	3				
H1	PH25	0	I/O			
	LCD1_D21	1				
	ATAIORDY	2				
	KP_OUT5	3				
J6	PH26	0	I/O			
	LCD1_D22	1				
	ATAIORDY	2				
	KP_OUT6	3				
J5	PH27	0	I/O			
	LCD1_D23	1				
	ATAIOW	2				
	KP_OUT7	3				
F3	PI0	0	I/O			
	GPS_CLK	1				
F2	PI1	0	I/O			
	GPS_SIGN	1				
F1	PI2	0	I/O			
	GPS_MAG	1				
G5	PI3	0	I/O			
	PWM1	1				
D3	PI4	0	I/O			
	EINT28	5				
A2	PI5	0	I/O			
	EINT29	5				
T7	PI6	0	I/O			
	EINT30	5				
U7	PI7	0	I/O			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
	EINT31	5				
R3	PI8	0	I/O			
	SPI1_CS0	1				
R4	PI9	0	I/O			
	SPI1_CS1	1				
R5	PI10	0	I/O			
	SPI1_CLK	1				
R6	PI11	0	I/O			
	SPI1_MOSI	1				
R7	PI12	0	I/O			
	SPI1_MISO	1				
R8	JTAG0#	0	I/O		pull-up (default)	
R9	JTAG1#	0	I/O		pull-up (default)	
P12	BOOTS	0	I/O		pull-up (default)	
G6	TEST	0	I/O		pull-down (default)	
R12	NMI#	0	A		no-pull (default)	
T12	RESET#	0	A			
U19	DM0	0	IO			
U20	DP0	0	IO			
P17	UVCC0	0	PWR	-	-	-
K12	UGND0	0	GND	-	-	-
T16	ULVDD0	0	PWR	-	-	-
L13	ULGND0	0	GND	-	-	-
R17	DM1	0	IO			
R18	DP1	0	IO			
P16	UVCC_C	0	PWR	-	-	-
L12	UGND_C	0	GND	-	-	-
R16	UVCC_T	0	PWR	-	-	-
M13	UGND_T	0	GND	-	-	-
U16	ULVDD1	0	PWR	-	-	-
M12	ULGND1	0	GND	-	-	-
T17	DM2	0	IO			
T18	DP2	0	IO			

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
U13	X1	0	AI			
T13	X2	0	AI			
R13	Y1	0	AI			
P13	Y2	0	AI			
U14	HPL	0	AO			
T14	HPR	0	AO			
V14	HPCOM	0	A			
V15	HPCOM_FB	0	A			
Y14	HPVCC	0	PWR	-	-	-
W14	HPVCC_IN	0	PWR	-	-	-
N11	HPGND	0	GND	-	-	-
W16	FMINL	0	AI			
Y16	FMINR	0	AI			
Y15	LINEINL	0	AI			
W15	LINEINR	0	AI			
V17	VMIC	0	PWR	-	-	-
W17	MICINL	0	AI			
Y17	MICINR	0	AI			
Y18	BIAS	0	A			
W19	VRP	0	A			
W18	VRA1	0	A			
V18	VRA2	0	A			
U15	LRADC0	0	AI			
T15	LRADC1	0	AI			
N15	TV_DAC0	0	AO			
N14	TV_DAC1	0	AO			
P15	TV_DAC2	0	AO			
P14	TV_DAC3	0	AO			
R14	TV_VCC	0	PWR	-	-	-
N12	TV_GND	0	GND	-	-	-
Y13	LOSCI	0	A			
W13	LOSCO	0	A			
V13	RTC_VDD	0	PWR	-	-	-
W20	HOSCI	0	A			
Y20	HOSCO	0	A			
V20	PLL_VDD	0	PWR	-	-	-
N13	PLL_GND	0	GND	-	-	-

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
K7\L7\ M7\N7\ P7\P8\ P9\P10\ H7\J7	VCC(10)	0	PWR	-	-	-
U12	CARD_VCC(1)	0	PWR	-	-	-
G10\G7	NAND_VCC(2)	0	PWR	-	-	-
H16\G16\G15\F16\ F15\E16\ E15\E14\ F14\E13	DRAM_VCC(10)	0	PWR	-	-	-
K15\K14\ J14\H14\ G14\G13\ G12\G11\ F12\F11	DRAM_GND(10)	0	GND	-	-	-
H8\J8\K8\K9\K10 J10\H10\H9\J9	VDD(9)	0	PWR	-	-	-
M8\M9\ N8\N9	VCDDC(4)	0	PWR	-	-	-
L8\L9\ L10\M10\ N10\L11\ K11\J11\ H11\J12\ J13\H13\ H12	GND(13)	0	GND	-	-	-
P18	LVDS_VCC(1)	0	PWR	-	-	-
K13	LVDS_GND(1)	0	GND	-	-	-
Y19	AVCC(1)	0	PWR	-	-	-
M11	AGND(1)	0	GND	-	-	-

BALL#	Pin Name	Function	Type	Ball Reset State	Pull Up/Down	Buffer Strength (mA)
E11\E12\ F13\H15\ J15\J16\ K16\L14\ L15\L16\ L17\L18\ L19\L20\ M14\M15\ M16\M17\ M18\N16\ N17\N18\ R15\U17\ U18\V16\ V19	Not Connect(27)	-	-	-	-	-

5.2. Multiplexing Characteristics

Table 5-2. provides a description of the F20 multiplexing on the FBGA400 package.

Table 5-2 Multiplexing Characteristics

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
K18	SDQ0					
K20	SDQ1					
K19	SDQ2					
J20	SDQ3					
J19	SDQ4					
H20	SDQ5					
H19	SDQ6					
G20	SDQ7					
E19	SDQ8					
D20	SDQ9					
D19	SDQ10					
C20	SDQ11					
C19	SDQ12					
B20	SDQ13					
B19	SDQ14					

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
A20	SDQ15					
A18	SDQ16					
B17	SDQ17					
A17	SDQ18					
B16	SDQ19					
A16	SDQ20					
B15	SDQ21					
A15	SDQ22					
B14	SDQ23					
A12	SDQ24					
C11	SDQ25					
A11	SDQ26					
B11	SDQ27					
A10	SDQ28					
B10	SDQ29					
A9	SDQ30					
B9	SDQ31					
G19	SDQS0	SDQS0				
F20	SDQM0	SDQM0				
K17	SVREF0	SVREF0				
F19	SDQM1	SDQM1				
E20	SDQS1	SDQS1				
A14	SDQS2	SDQS2				
B13	SDQM2	SDQM2				
D11	SVREF1	SVREF1				
A13	SDQM3	SDQM2				
B12	SDQS3	SDQS2				
A19	SCK#	SCK#				
B18	SCK	SCK				
C18	SCKE	SCKE				
D14	SA0	SA0				
C13	SA1	SA1				
D13	SA2	SA2				
C12	SA3	SA3				
E18	SA4	SA14				
E17	SA5	SA13				
F18	SA6	SA12				
F17	SA7	SA11				
G18	SA8	SA10				

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
G17	SA9	SA9				
C14	SA10	SA8				
H18	SA11	SA7				
H17	SA12	SA6				
J17	SA13	SA5				
D12	SA14	SA4				
D18	SWE#	SWE				
D17	SCAS	SCAS				
C17	SRAS	SRAS				
C16	SCS	SCS				
D16	SBA0	SBA0				
C15	SBA1	SBA1				
D15	SBA2	SBA2				
J18	SODT	ODT				
V7	PA0	ERXD3	SPI1_CS0	UART2_RTS		
W7	PA1	ERXD2	SPI1_CLK	UART2_CTS		
Y7	PA2	ERXD1	SPI1_MOSI	UART2_TX		
T8	PA3	ERXD0	SPI1_MISO	UART2_RX		
U8	PA4	ETXD3	SDC3_D3			
V8	PA5	ETXD2	SDC3_D2			
W8	PA6	ETXD1	SDC3_D1			
Y8	PA7	ETXD0	SDC3 D0			
T9	PA8	ERXCK	SDC3_CLK			
U9	PA9	ERXERR	SDC3_CMD			
V9	PA10	ERXDV		UART1_TX		
W9	PA11	EMDC		UART1_RX		
Y9	PA12	EMDIO	UART6_TX	UART1_RTS		
R10	PA13	ETXEN	UART6_RX	UART1_CTS		
T10	PA14	ETXCK	UART7_TX	UART1_DTR		
U10	PA15	ECRS	UART7_RX	UART1_DSR		
V10	PA16	ECOL	CAN_TX	UART1_DCD		
W10	PA17	ETXERR	CAN_RX	UART1_RING		
B2	PB0	TWI0_SCK				
A1	PB1	TWI0_SDA				
B1	PB2	PWM0				
G4	PB3	IR_TX		SPDIF_MCLK		EINT16
G3	PB4	IR_RX				
C2	PB5	I2S_MCLK	AC97_MCLK			
C1	PB6	I2S_BCLK	AC97_BCLK			

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
D2	PB7	I2S_LRCK	AC97_SYNC			
D1	PB8	I2S_DO0	AC97_DO			
E3	PB9	I2S_DO1	GPS_CLK			EINT17
E2	PB10	I2S_DO2	GPS_SIGN			EINT18
E1	PB11	I2S_DO3	GPS_MAG			EINT19
F4	PB12	I2S_DI	AC97_DI	SPDIF_DI		
Y10	PB13	SPI2_CS1		SPDIF_DO		
P11	PB14	SPI2_CS0	JTAG_MS0			
R11	PB15	SPI2_CLK	JTAG_CK0			
T11	PB16	SPI2_MOSI	JTAG_DO0			
U11	PB17	SPI2_MISO	JTAG_DI0			
T3	PB18	TWI1_SCK	PS2_SCK0			EINT20
T4	PB19	TWI1_SDA	PS2_SDA0			EINT21
P1	PB20	TWI2_SCK				EINT22
P2	PB21	TWI2_SDA				EINT23
T5	PB22	UART0_TX				
T6	PB23	UART0_RX				
C9	PC0	NWE	SPI0_MOSI			
G8	PC1	NALE	SPI0_MISO			
F8	PC2	NCLE	SPI0_CLK			
E8	PC3	NCE1	SDC1_CMD			
D8	PC4	NCE0				
C8	PC5	NRD	SDC1_CLK			
B8	PC6	NRB0	SDC2_CMD			
A8	PC7	NRB1	SDC2_CLK			
A7	PC8	ND0	SDC2_D0			
B7	PC9	ND1	SDC2_D1			
C7	PC10	ND2	SDC2_D2			
D7	PC11	ND3	SDC2_D3			
E7	PC12	ND4	SDC1_D0			
F7	PC13	ND5	SDC1_D1			
A6	PC14	ND6	SDC1_D2			
B6	PC15	ND7	SDC1_D3			
F10	PC16	NWP				
E10	PC17	NCE2				
D10	PC18	NCE3				
C10	PC19	NCE4	SPI2_CS0			EINT12
G9	PC20	NCE5	SPI2_CLK			EINT13
F9	PC21	NCE6	SPI2_MOSI			EINT14

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
E9	PC22	NCE7	SPI2_MISO			EINT15
D9	PC23		SPI0_CS0			
J4	PD0	LCD0_CLK	TS0_CLK	LCD1_CLK		
J3	PD1	LCD0_DE	TS0_ERR	LCD1_DE		
J2	PD2	LCD0_HSYNC	TS0_SYNC	LCD1_HSYNC		
J1	PD3	LCD0_VSYNC	TS0_DVLD	LCD1_VSYNC		
K6	PD4	LCD0_D0	KP_IN0	LCD1_D0		
K5	PD5	LCD0_D1	KP_IN1	LCD1_D1		
K4	PD6	LCD0_D2	KP_IN2	LCD1_D2		
K3	PD7	LCD0_D3	KP_IN3	LCD1_D3		
K2	PD8	LCD0_D4	KP_IN4	LCD1_D4		
K1	PD9	LCD0_D5	KP_IN5	LCD1_D5		
L1	PD10	LCD0_D6	KP_IN6	LCD1_D6		
L2	PD11	LCD0_D7	KP_IN7	LCD1_D7		
L3	PD12	LCD0_D8	KP_OUT0	LCD1_D8		
L4	PD13	LCD0_D9	KP_OUT1	LCD1_D9		
L5	PD14	LCD0_D10	KP_OUT2	LCD1_D10		
L6	PD15	LCD0_D11	KP_OUT3	LCD1_D11		
M1	PD16	LCD0_D12	KP_OUT4	LCD1_D12		
M2	PD17	LCD0_D13	KP_OUT5	LCD1_D13		
M3	PD18	LCD0_D14	KP_OUT6	LCD1_D14		
M4	PD19	LCD0_D15	KP_OUT7	LCD1_D15		
M5	PD20	LCD0_D16	TS0_D0	LCD1_D16		
M6	PD21	LCD0_D17	TS0_D1	LCD1_D17		
N1	PD22	LCD0_D18	TS0_D2	LCD1_D18		
N2	PD23	LCD0_D19	TS0_D3	LCD1_D19		
N3	PD24	LCD0_D20	TS0_D4	LCD1_D20		
N4	PD25	LCD0_D21	TS0_D5	LCD1_D21		
N5	PD26	LCD0_D22	TS0_D6	LCD1_D22		
N6	PD27	LCD0_D23	TS0_D7	LCD1_D23		
Y3	PE0	TS0_CLK	CSI0_PCK			
V4	PE1	TS0_ERR	CSI0_CK			
W4	PE2	TS0_SYNC	CSI0_HSYNC			
Y4	PE3	TS0_DVLD	CSI0_VSYNC			
U5	PE4	TS0_D0	CSI0_D0			
V5	PE5	TS0_D1	CSI0_D1	SMC_VPPEN		
W5	PE6	TS0_D2	CSI0_D2	SMC_VPPPP		
Y5	PE7	TS0_D3	CSI0_D3	SMC_DET		
U6	PE8	TS0_D4	CSI0_D4	SMC_VCCEN		

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
V6	PE9	TS0_D5	CSI0_D5	SMC_RST		
W6	PE10	TS0_D6	CSI0_D6	SMC_SLK		
Y6	PE11	TS0_D7	CSI0_D7	SMC_SDA		
U1	PE12	TS1_CLK	CSI1_PCK	SDC1_CMD		
U2	PE13	TS1_ERR	CSI1_CK	SDC1_CLK		
U3	PE14	TS1_SYNC	CSI1_HSYNC	SDC1_D0		
U4	PE15	TS1_DVLD	CSI1_VSYNC	SDC1_D1		
V1	PE16	TS1_D0	CSI1_D0	SDC1_D2		
V2	PE17	TS1_D1	CSI1_D1	SDC1_D3		
V3	PE18	TS1_D2	CSI1_D2	UART3_TX		
W1	PE19	TS1_D3	CSI1_D3	UART3_RX		
W2	PE20	TS1_D4	CSI1_D4	UART3_RTS		
Y1	PE21	TS1_D5	CSI1_D5	UART3_CTS		
Y2	PE22	TS1_D6	CSI1_D6	UART4_TX		
W3	PE23	TS1_D7	CSI1_D7	UART4_RX		
T1	PE24	PS2_SCK0				EINT10
T2	PE25	PS2_SDA0				EINT11
P3	PE26	SDC3_CMD				
P4	PE27	SDC3_CLK				
P5	PE28	SDC3_D0				
P6	PE29	SDC3_D1				
R1	PE30	SDC3_D2				
R2	PE31	SDC3_D3				
V11	PF0	SDC0_D1	MS_D1	JTAG_MS1	SDC2_D1	
W11	PF1	SDC0_D0	MS_D0	JTAG_DI1	SDC2_D0	
Y11	PF2	SDC0_CLK	MS_CLK	UART0_TX	SDC2_CLK	
Y12	PF3	SDC0_CMD	MS_BS	JTAG_DO1	SDC2_CMD	
W12	PF4	SDC0_D3	MS_D3	UART0_RX	SDC2_D3	
V12	PF5	SDC0_D2	MS_D2	JTAG_CK1	SDC2_D2	
T19	PG0	LVDS_VP3				EINT0
T20	PG1	LVDS_VN3				EINT1
R19	PG2	LVDS_VPC				EINT2
R20	PG3	LVDS_VNC				EINT3
P19	PG4	LVDS_VP2				EINT4
P20	PG5	LVDS_VN2				EINT5
N19	PG6	LVDS_VP1				EINT6
N20	PG7	LVDS_VN1				EINT7
M19	PG8	LVDS_VP0				EINT8
M20	PG9	LVDS_VN0				EINT9

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
C6	PH0	LCD1_CLK	ATAA0	UART3_TX		EINT24
D6	PH1	LCD1_DE	ATAA1	UART3_RX		EINT25
E6	PH2	LCD1_HSYNC	ATAA2	UART3_RTS		EINT26
F6	PH3	LCD1_VSYNC	ATAIRQ	UART3_CTS		EINT27
A5	PH4	LCD1_D0	ATAD0	UART4_TX		
B5	PH5	LCD1_D1	ATAD1	UART4_RX		
C5	PH6	LCD1_D2	ATAD2	UART5_TX		
D5	PH7	LCD1_D3	ATAD3	UART5_RX		
E5	PH8	LCD1_D4	ATAD4	KP_IN0		
F5	PH9	LCD1_D5	ATAD5	KP_IN1		
A4	PH10	LCD1_D6	ATAD6	KP_IN2		
B4	PH11	LCD1_D7	ATAD7	KP_IN3		
C4	PH12	LCD1_D8	ATAD8	PS2_SCK1		
D4	PH13	LCD1_D9	ATAD9	PS2_SDA1		
E4	PH14	LCD1_D10	ATAD10	KP_IN4		
A3	PH15	LCD1_D11	ATAD11	KP_IN5		
B3	PH16	LCD1_D12	ATAD12	KP_IN6		
C3	PH17	LCD1_D13	ATAD13	KP_IN7		
G2	PH18	LCD1_D14	ATAD14	KP_OUT0		
G1	PH19	LCD1_D15	ATAD15	KP_OUT1		
H6	PH20	LCD1_D16	ATAOE	CAN_TX		
H5	PH21	LCD1_D17	ATADREQ	CAN_RX		
H4	PH22	LCD1_D18	ATADACK	KP_OUT2		
H3	PH23	LCD1_D19	ATACS0	KP_OUT3		
H2	PH24	LCD1_D20	ATACS1	KP_OUT4		
H1	PH25	LCD1_D21	ATAIORDY	KP_OUT5		
J6	PH26	LCD1_D22	ATAIOR	KP_OUT6		
J5	PH27	LCD1_D23	ATAIOW	KP_OUT7		
F3	PI0	GPS_CLK				
F2	PI1	GPS_SIGN				
F1	PI2	GPS_MAG				
G5	PI3	PWM1				
D3	PI4					EINT28
A2	PI5					EINT29
T7	PI6					EINT30
U7	PI7					EINT31
R3	PI8	SPI1_CS0				
R4	PI9	SPI1_CS1				
R5	PI10	SPI1_CLK				

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
R6	PI11	SPI1_MOSI				
R7	PI12	SPI1_MISO				
R8	JTAG0#	JTAG_SEL				
R9	JTAG1#	JTAG_SEL				
P12	BOOTS	BOOT_SEL				
G6	TEST					
R12	NMI#					
T12	RESET#					
U19	DM0					
U20	DP0					
P17	UVCC0					
K12	UGND0					
T16	ULVDD0					
L13	ULGND0					
R17	DM1					
R18	DP1					
P16	UVCC_C					
L12	UGND_C					
R16	UVCC_T					
M13	UGND_T					
U16	ULVDD1					
M12	ULGND1					
T17	DM2					
T18	DP2					
U13	X1					
T13	X2					
R13	Y1					
P13	Y2					
U14	HPL					
T14	HPR					
V14	HPCOM					
V15	HPCOM_FB					
Y14	HPVCC					
W14	HPVCC_IN					
N11	HPGND					
W16	FMINL					
Y16	FMINR					
Y15	LINEINL					
W15	LINEINR					

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
V17	VMIC					
W17	MICINL					
Y17	MICINR					
Y18	BIAS					
W19	VRP					
W18	VRA1					
V18	VRA2					
U15	LRADC0					
T15	LRADC1					
N15	TV_DAC0					
N14	TV_DAC1					
P15	TV_DAC2					
P14	TV_DAC3					
R14	TV_VCC					
N12	TV_GND					
Y13	LOSCI					
W13	LOSCO					
V13	RTC_VDD					
W20	HOSCI					
Y20	HOSCO					
V20	PLL_VDD					
N13	PLL_GND					
K7\L7\ M7\N7\ P7\P8\ P9\P10\ H7\J7	VCC (10)					
U12	CARD_VCC (1)					
G10\G7	NAND_VCC (2)					
H16\G16\ G15\F16\ F15\E16\ E15E14\ F14\E13	DRAM_VCC (10)					

Ball #	Multi0 (default)	Multi1	Multi2	Multi3	Multi4	Multi5
K15\K14\ J14\H14\ G14\G13\ G12\G11\ F12\F11	DRAM_GND (10)					
H8\J8\ K8\K9\ K10\J10\ H10\H9\ J9	VDD (9)					
M8\M9\ N8\N9	VCDDC (4)					
L8\L9\ L10\M10\ N10\L11\ K11\J11\ H11\J12\ J13\H13\ H12	GND (13)					
P18	LVDS_VCC(1)					
K13	LVDS_GND(1)					
Y19	AVCC(1)					
M11	AGND(1)					
E11\E12\ F13\H15\ J15\J16\ K16\L14\ L15\L16\ L17\L18\ L19\L20\ M14\M15\ M16\M17\ M18\N16\ N17\N18\ R15\U17\ U18\V16\ V19	NC(27)					

5.3. Power and Miscellaneous Signals

Many signals are available on multiple pins according to the software configuration of the multiplexing options.

1. Signal Name: The signal name
2. Description: Description of the signal
3. Type: type = Pin type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance
   - A = Analog
   - PWR = Power
   - GND = Ground
4. Pin #: Associated ball(s) number

5.3.1. Power Domain Signal Description

Table 5-3 Power Domain Signal Description

Signal Name	Description	Pin Name	Ball#
TV-OUT DAC Power			
TV-VCC	TV-OUT Power Supply	TV-VCC	R14
TV-GND	TV-OUT Ground	TV-GND	N12
Audio DAC Power			
HPVCC	Audio output DAC Power Supply	HPVCC	Y14
HPVCC_IN	Audio output DAC Power Supply	HPVCC_IN	W14
HPGND	Audio output DAC Ground	HPGND	N11
Audio ADC Power			
VMIC	Microphone ADC Power Supply	VMIC	V17
USB Power			
UVCC0	USB0 PHY Analog Power Supply	UVCC0	P17
ULVDD0	USB0 Digital Power Supply	ULVDD0	T16
UVCC_C	USB1 PHY Analog Power Supply	UVCC_C	P16
UVCC_T	USB2 PHY Analog Power Supply	UVCC_T	R16
ULVDD1	USB1/2 Digital Power Supply	ULVDD1	U16
UGND0	USB0 PHY Analog Ground	UGND0	K12
ULGND0	USB0 Digital Ground	ULGND0	L13
UGND_C	USB1 PHY Analog Ground	UGND_C	L12
UGND_T	USB2 PHY Analog Ground	UGND_T	M13
ULGND1	USB1/2 Digital Ground	ULGND1	M12

Signal Name	Description	Pin Name	Ball#
RTC Power			
RTC_VDD	RTC Power Supply	RTC_VDD	V13
PLL Power			
PLL_VDD	PLL Power Supply	PLL_VDD	V20
PLL_GND	PLL Ground	PLL_GND	N13
Core Power			
VDD	Core Chip Power Supply	VDD(13)	H8\J8\ K8\K9\ K10\J10\ H10\H9\ J9\M8\ M9\N8\ N9
GND	Core Chip Ground	GND(13)	L8\L9\ L10\M10\ N10\L11\ K11\J11\ H11\J12\ J13\H13\ H12
IO Power			
VCC	IO Power Supply	VCC(10)	K7\L7\ M7\N7\ P7\P8\ P9\P10\ H7\J7
Card Power			
Card VCC	Card Power Supply	Card VCC	U12
NAND Power			
NAND_VCC	NAND Flash Power Supply	NAND_VCC(2)	G10\G7
DRAM Power			
DRAM_VCC	DRAM Power Supply	DRAM_VCC(10)	H16\G16\ G15\F16\ F15\E16\ E15\E14\ F14\E13

Signal Name	Description	Pin Name	Ball#
DRAM_GND	DRAM Ground	DRAM_GND(10)	K15\K14\ J14\H14\ G14\G13\ G12\G11\ F12\F11
LVDS Power			
LVDS_VCC	LVDS Power Supply	LVDS_VCC(1)	P18
LVDS_GND	LVDS Ground	LVDS_GND(1)	K13
Analog Power			
AVCC	Analog Power Supply	AVCC(1)	Y19
AGND	Analog Ground	AGND(1)	M11

5.3.2. Miscellaneous Signal Description

Table 5-4 Miscellaneous Signal Description

Signal Name	Description	Type	Pin Name	Ball#
JTAG Interface				
JTAG_SEL0	JTAG port Select bit0	I	JTAG0#	R8
JTAG_SEL1	JTAG port Select bit1	I	JTAG1#	R9
JTAG Port 0				
JTAG_MS0	JTAG Mode Select	I	PB14	P11
JTAG_CK0	JTAG Clock	I	PB15	R11
JTAG_DO0	JTAG test DataOutput	O	PB16	T11
JTAG_DI0	JTAG test Data Input	I	PB17	U11
JTAG Port 1				
JTAG_MS1	JTAG Mode Select	I	PF0	V11
JTAG_CK1	JTAG Clock	I	PF5	V12
JTAG_DO1	JTAG test DataOutput	O	PF11	W11
JTAG_DI1	JTAG test Data Input	I	PF3	Y12
Clock				
HOSCI	Main 24MHz crystal Input for internal OSC	AI	HOSCI	W20
HOSCO	Main 24MHz crystal Output for internal OSC	AO	HOSCO	Y20
LOSCI	32K768Hz crystal Input for RTC	AI	LOSCI	Y13
LOSCO	32K768Hz crystal Output for RTC	AO	LOSCO	W13
Reset				
RESET#	System Reset	AI	RESET#	T12
FIQ				

Signal Name	Description	Type	Pin Name	Ball#
NMI#	External Fast Interrupt Request	I	NMI#	R12
Boot				
BOOT_SEL	Boot Mode Select	I	BOOTS	P12
Test				
TEST	Test Pin(Pull down Internal default)	I	TEST	G6
Others				
BIAS	Bias of the CPU connect a 200Kohm Resistor to ground	A	BIAS	Y18
VRP	=AVCC=3.0V	A	VRP	W19
VRA1	=1.5V	A	VRA1	W18
VRA2	=0V	A	VRA2	V18
NC	Not Connect	NC(27)	NC	E11\E12\ F13\H15\ J15\J16\ K16\L14\ L15\L16\ L17\L18\ L19\L20\ M14\M15\ M16\M17\ M18\N16\ N17\N18\ R15\U17\ U18\V16\ V19

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 6-1) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the F20.

Note: Absolute maximum ratings are not operating ranges. Operation at absolute maximum ratings is not guaranteed.

Table 6-1 Multiplexing Characteristics

Symbol	Parameter		Min	Max	Unit
TS	Storage Temperature		TBD	TBD	°C
II/O	In/Out current for input and output		TBD	TBD	mA
VESD	ESD stress voltage	HBM(human body model)	TBD	TBD	V
		CDM(charged device model)	TBD	TBD	V
VCC	DC Supply Voltage for I/O		TBD	TBD	V
VDD	DC Supply Voltage for Internal Digital Logic		TBD	TBD	V
VCC_ANALOG	DC Supply Voltage for Analog Part		TBD	TBD	V
VCC_DRAM	DC Supply Voltage for DRAM Part		TBD	TBD	V
VCC_USB	DC Supply Voltage for USB PHY		TBD	TBD	V
VCC_TV	DC Supply Voltage for TV-OUT DAC		TBD	TBD	V
VCC_LRADC	DC Supply Voltage for LRADC		TBD	TBD	V
VCC_HP	DC Supply Voltage for Audio DAC		TBD	TBD	V
VDD_PLL	DC Supply Voltage for PLL		TBD	TBD	V
VDD_RTC	DC Supply Voltage for RTC		TBD	TBD	V

6.2. Recommended Operating Conditions

All F20 modules are used under the operating Conditions contained in Table 6-2.

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Operating Temperature[Commercial]	-25	–	+85	°C
	Operating Temperature[Extended]	-40	–	+85	°C
GND	Ground	0	0	0	V
VCC	DC Supply Voltage for I/O	TBD	3.3	TBD	V
VDD	DC Supply Voltage for Internal Digital Logic	TBD	1.32	TBD	V
VCC_ANALOG	DC Supply Voltage for Analog Part	TBD	3.0	TBD	V
VCC_DRAM	DC Supply Voltage for DRAM Part	TBD	1.8	TBD	V
VCC_USB	DC Supply Voltage for USB PHY	TBD	3.3	TBD	V
VCC_TV	DC Supply Voltage for TV-OUT DAC	TBD	3.3	TBD	V
VCC_HP	DC Supply Voltage for Audio DAC	TBD	TBD	TBD	V
VDD_PLL	DC Supply Voltage for PLL	TBD	TBD	TBD	V
VDD_RTC	DC Supply Voltage for RTC	TBD	1.25	TBD	V

6.3. DC Electrical Characteristics

Table 6-3 summarized the DC electrical characteristics of F20.

Table 6-3 DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIH	**High-level input voltage**	**TBD**	**TBD**	**TBD**	**V**
VIL	Low-level input voltage	TBD	TBD	TBD	V
VHYS	Hysteresis voltage	TBD	TBD	TBD	mV
IIH	High-level input current	TBD	TBD	TBD	uA
IIL	Low-level input current	TBD	TBD	TBD	uA
VOH	High-level output voltage	TBD	TBD	TBD	V
VOL	Low-level output voltage	TBD	TBD	TBD	V
IOZ	Tri-State Output Leakage Current	TBD	TBD	TBD	uA
CIN	Input capacitance	TBD	TBD	TBD	pF
COUT	Output capacitance	TBD	TBD	TBD	pF

6.4. Oscillator Electrical Characteristics

The F20 contains two oscillators: a 24.000 MHz oscillator and a 32.768kHz oscillator. Each oscillator requires a specific crystal.

The F20 device operation requires the following two input clocks:

- The 32.768kHz frequency is used for low frequency operation.
- The 24.000MHz frequency is used to generate the main source clock of the F20 device.

6.4.1. 24MHz Oscillator Characteristics

The 24.0MHz crystal is connected between the HOSCI (amplifier input) and HOSCO (amplifier output). Table 6-4 lists the 24.MHz crystal specifications.

Table 6-4 24MHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(tCPMAIN)	Crystal Oscillator Frequency Range		24.000		MHz
tST	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
PON	Drive level	–	–	50	uW
CL	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
RS	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
CM	Motional capacitance	–	–		pF
CSHUT	Shunt capacitance	–	–		pF
RBIAS	Internal bias resistor				MΩ

6.4.2. 32.768kHz Oscillator Characteristics

The 32.768kHz crystal is connected between the LOSCI (amplifier input) and LOSCO (amplifier output). Table 6-5 lists the 32.768kHz crystal specifications.

Table 6-5 32.768kHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(tCPMAIN)	Crystal Oscillator Frequency Range		24.000		MHz
tST	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm

Symbol	Parameter	Min	Typ	Max	Unit
PON	Drive level	–	–	50	uW
CL	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
RS	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
CM	Motional capacitance	–	–		pF
CSHUT	Shunt capacitance	–	–		pF
RBIAS	Internal bias resistor				MΩ

6.5. Power up/down and Reset Specifications

This section includes specification for the following:

- Power-up sequence
- Power-down sequence

6.5.1. Power-up Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation. Figure 6-x shows this sequence and is detailed in Table 6-x

TBD

6.5.2. Power-down Sequence

The sequence indicated in Figure 6-x and detailed in Table 6-x is the required timing parameters for power-down.

TBD

7. Clock Control Module

TBD

7.1. Clock Tree Diagram

TBD

7.2. PLL Diagram

7.3. PWM

7.3.1. PWM Timing Diagram

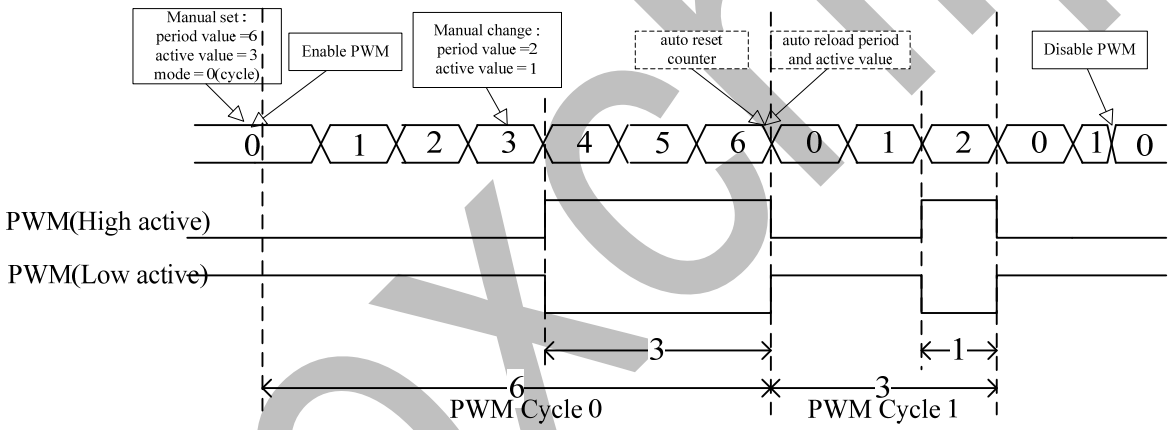


Figure 7-x PWM Timing Diagram

7.3.2. PWM Signal Description

Table 7-1 PWM Signal Description

Signal Name	Description	Type	Pin Name	Ball#
PWM0	PWM output for port 0	O	PB2	B1
PWM1	PWM output for port 1	O	PI3	G5

8. Timer Controller

8.1. Timer Controller Overview

TBD

8.2. Timer Block Diagram

TBD

9. Interrupt Controller

9.1. Interrupt Controller Overview

The interrupt controller has the following feature:

- Controls the nIRQ and FIQ of an AC320 Processor
- Thirty-one individually maskable interrupt sources
- One external NMI interrupt source
- 4-Level Priority Controller
- Six External Sources of Edge-sensitive or Level-sensitive
- Fast Forcing

It provides handling of up to thirty-two interrupt sources. The 4-level Priority Controller allows the user to define the priority for each interrupt source, thus permitting higher priority interrupts to be serviced even if a lower priority interrupt is being treated. The fast forcing feature redirects any internal or external source to provide a fast interrupt rather than a normal interrupt.

9.2. Interrupt Block Diagram

TBD

9.3. External Interrupt Signal Description

Table 9-1 External Interrupt Signal Description

Signal Name	Description	Type	Pin Name	Ball#
EINT0	External Interrupt source 0	I	PG0	T19
EINT1	External Interrupt source 1	I	PG1	T20
EINT2	External Interrupt source 2	I	PG2	R19
EINT3	External Interrupt source 3	I	PG3	R20
EINT4	External Interrupt source 4	I	PG4	P19
EINT5	External Interrupt source 5	I	PG5	P20
EINT6	External Interrupt source 6	I	PG6	N19
EINT7	External Interrupt source 7	I	PG7	N20
EINT8	External Interrupt source 8	I	PG8	M19
EINT9	External Interrupt source 9	I	PG9	M20
EINT10	External Interrupt source 10	I	PE24	T1
EINT11	External Interrupt source 11	I	PE25	T2
EINT12	External Interrupt source 12	I	PC19	C10

Signal Name	Description	Type	Pin Name	Ball#
EINT13	External Interrupt source 13	I	PC20	G9
EINT14	External Interrupt source 14	I	PC21	F9
EINT15	External Interrupt source 15	I	PC22	E9
EINT16	External Interrupt source 16	I	PB3	G4
EINT17	External Interrupt source 17	I	PB9	E3
EINT18	External Interrupt source 18	I	PB10	E2
EINT19	External Interrupt source 19	I	PB11	E1
EINT20	External Interrupt source 20	I	PB18	T3
EINT21	External Interrupt source 21	I	PB19	T4
EINT22	External Interrupt source 22	I	PB20	P1
EINT23	External Interrupt source 23	I	PB21	P2
EINT24	External Interrupt source 24	I	PH0	C6
EINT25	External Interrupt source 25	I	PH1	D6
EINT26	External Interrupt source 26	I	PH2	E6
EINT27	External Interrupt source 27	I	PH3	F6
EINT28	External Interrupt source 28	I	PI4	D3
EINT29	External Interrupt source 29	I	PI5	A2
EINT30	External Interrupt source 30	I	PI6	T7
EINT31	External Interrupt source 31	I	PI7	U7

10. DMA Controller

10.1. DMA Controller Overview

There are three kinds of DMA in the F20. One is Normal DMA (NDMA) with 8 channels, the second is Dedicated DMA (DDMA) with 8 channels and the third one is the Special function DMA for special engine, such as video engine and display engine etc.

11. SDRAM Controller

11.1. SDRAM Controller Description

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all in-dusty-standard double data rate (DDR) ordinary SDRAM and double data rate (DDR) Mobile SDRAM. It supports up to a 1G Bytes memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Mode-Register settings.

The DRAMC includes the following features:

- Support DDR SDRAM, DDR Mobile SDRAM and DDR2 SDRAM
- Support Different Memory Device's Power Voltage of 1.8V and 2.5V
- Support DDR SDRAM, DDR Mobile SDRAM and DDR2 SDRAM of clock frequency up to DDR333
- Support Memory Capacity up to 1G bytes
- Support one chip select signals
- 18 address lines including 3 bank address lines
- Data IO size can up to 16/32-bit for DDR
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different application
- Random read or write operation is supported

11.2. SDRAM Controller Signal Description

Table 11-1. SDRAM Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
SDQ0	SDRAM Data Bus bit0	I/O	SDQ0	K18
SDQ1	SDRAM Data Bus bit1	I/O	SDQ1	K20
SDQ2	SDRAM Data Bus bit2	I/O	SDQ2	K19
SDQ3	SDRAM Data Bus bit3	I/O	SDQ3	J20
SDQ4	SDRAM Data Bus bit4	I/O	SDQ4	J19
SDQ5	SDRAM Data Bus bit5	I/O	SDQ5	H20
SDQ6	SDRAM Data Bus bit6	I/O	SDQ6	H19
SDQ7	SDRAM Data Bus bit7	I/O	SDQ7	G20

Signal Name	Description	Type	Pin Name	Ball#
SDQ8	SDRAM Data Bus bit8	I/O	SDQ8	E19
SDQ9	SDRAM Data Bus bit9	I/O	SDQ9	D20
SDQ10	SDRAM Data Bus bit10	I/O	SDQ10	D19
SDQ11	SDRAM Data Bus bit11	I/O	SDQ11	C20
SDQ12	SDRAM Data Bus bit12	I/O	SDQ12	C19
SDQ13	SDRAM Data Bus bit13	I/O	SDQ13	B20
SDQ14	SDRAM Data Bus bit14	I/O	SDQ14	B19
SDQ15	SDRAM Data Bus bit15	I/O	SDQ15	A20
SDQ16	SDRAM Data Bus bit16	I/O	SDQ16	A18
SDQ17	SDRAM Data Bus bit17	I/O	SDQ17	B17
SDQ18	SDRAM Data Bus bit18	I/O	SDQ18	A17
SDQ19	SDRAM Data Bus bit19	I/O	SDQ19	B16
SDQ20	SDRAM Data Bus bit20	I/O	SDQ20	A16
SDQ21	SDRAM Data Bus bit21	I/O	SDQ21	B15
SDQ22	SDRAM Data Bus bit22	I/O	SDQ22	A15
SDQ23	SDRAM Data Bus bit23	I/O	SDQ23	B14
SDQ24	SDRAM Data Bus bit24	I/O	SDQ24	A12
SDQ25	SDRAM Data Bus bit25	I/O	SDQ25	C11
SDQ26	SDRAM Data Bus bit26	I/O	SDQ26	A11
SDQ27	SDRAM Data Bus bit27	I/O	SDQ27	B11
SDQ28	SDRAM Data Bus bit28	I/O	SDQ28	A10
SDQ29	SDRAM Data Bus bit29	I/O	SDQ29	B10
SDQ30	SDRAM Data Bus bit30	I/O	SDQ30	A9
SDQ31	SDRAM Data Bus bit31	I/O	SDQ31	B9
SDQS0	SDRAM Data Strobe 0	I/O	SDQS0	G19
SDQM0	SDRAM Data Mask 0	O	SDQM0	F20
SVREF0	SDRAM Reference Input 0	AI	SVREF0	K17
SDQM1	SDRAM Data Mask 1	O	SDQM1	F19
SDQS1	SDRAM Data Strobe 1	I/O	SDQS1	E20
SDQS2	SDRAM Data Strobe 2	I/O	SDQS2	A14
SDQM2	SDRAM Data Mask 2	O	SDQM2	B13
SVREF1	SDRAM Reference Input 1	AI	SVREF1	D11
SDQM3	SDRAM Data Mask 3	O	SDQM3	A13
SDQS3	SDRAM Data Strobe 3	I/O	SDQS3	B12
SCK#	SDRAM Clock Invert	O	SCK#	A19
SCK	SDRAM Clock	O	SCK	B18
SCKE	SDRAM Clock Enable	O	SCKE	C18
SA0	SDRAM Data Address bit0	O	SA0	D14
SA1	SDRAM Data Address bit1	O	SA1	C13

Signal Name	Description	Type	Pin Name	Ball#
SA2	SDRAM Data Address bit2	O	SA2	D13
SA3	SDRAM Data Address bit3	O	SA3	C12
SA4	SDRAM Data Address bit4	O	SA4	E18
SA5	SDRAM Data Address bit5	O	SA5	E17
SA6	SDRAM Data Address bit6	O	SA6	F18
SA7	SDRAM Data Address bit7	O	SA7	F17
SA8	SDRAM Data Address bit8	O	SA8	G18
SA9	SDRAM Data Address bit9	O	SA9	G17
SA10	SDRAM Data Address bit10	O	SA10	C14
SA11	SDRAM Data Address bit11	O	SA11	H18
SA12	SDRAM Data Address bit12	O	SA12	H17
SA13	SDRAM Data Address bit13	O	SA13	J17
SA14	SDRAM Data Address bit14	O	SA14	D12
SWE#	SDRAM Write Enable	O	SWE#	D18
SCAS	SDRAM Column address strobe	O	SCAS	D17
SRAS	SDRAM Raw address strobe	O	SRAS	C17
SCS	SDRAM Chip Select	O	SCS	C16
SBA0	SDRAM Bank Select 0	O	SBA0	D16
SBA1	SDRAM Bank Select 1	O	SBA1	C15
SBA2	SDRAM Bank Select 2	O	SBA2	D15
SODT	SDRAM ODT Control Signal	O	SODT	J18

12. NAND Flash Controller

12.1. NFC Overview

The NFC is one NAND Flash Controller which supports all NAND/MLC flash memory available in the market. New type flash can be supported by software re-configuration. The NFC can support 8 NAND flash with 1.8/3.3 V voltage supply. There are 8 separate chip select lines (CE#) for connecting up to 8 flash chips with2 R/B signals.

The On-the-fly error correction code (ECC) is built-in NFC for enhancing reliability. BCH-16/-24/-28/-32 is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control for reading or writing external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kinds of modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NAND Flash Controller (NFC) includes the following features:

- Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
- Software configure seed for randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Supports 8-bit Data Bus Width
- Supports 1024, 2048, 4096, 8192, 16384 bytes size per page
- Supports 1.8/3.3 V voltage supply Flash
- Up to 8 flash chips which are controlled by NFC_CEx#
- Supports Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NFC status information is reported by its' registers and interrupt is supported
- One Command FIFO
- External DMA is supported for transferring data
- Two 256x32-bit RAM for Pipeline Procession
- Support self –debug for NFC debug

12.2. NAND Flash Controller Signal Description

Table 12-1. NAND Flash Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
NCE0	NAND FLASH Chip Select bit0	O	PC4	D8
NCE1	NAND FLASH Chip Select bit1	O	PC3	E8
NCE2	NAND FLASH Chip Select bit2	O	PC17	E10
NCE3	NAND FLASH Chip Select bit3	O	PC18	D10
NCE4	NAND FLASH Chip Select bit4	O	PC19	C10
NCE5	NAND FLASH Chip Select bit5	O	PC20	G9
NCE6	NAND FLASH Chip Select bit6	O	PC21	F9
NCE7	NAND FLASH Chip Select bit7	O	PC22	E9
NRB0	NAND FLASH Chip Ready/Busy bit0	I	PC6	B8
NRB1	NAND FLASH Chip Ready/Busy bit1	I	PC7	A8
NWE	NAND FLASH Chip Write Enable	O	PC0	C9
NRD	NAND FLASH Chip Read Enable	O	PC5	C8
NALE	NAND FLASH Chip Address Latch Enable	O	PC1	G8
NCLE	NAND FLASH Chip Cammand Latch Enable	O	PC2	F8
NWP	NAND FLASH Chip Write Protect	O	PC16	F10
ND0	NAND FLASH Data bit0	I/O	PC8	A7
ND1	NAND FLASH Data bit1	I/O	PC9	B7
ND2	NAND FLASH Data bit2	I/O	PC10	C7
ND3	NAND FLASH Data bit3	I/O	PC11	D7
ND4	NAND FLASH Data bit4	I/O	PC12	E7
ND5	NAND FLASH Data bit5	I/O	PC13	F7
ND6	NAND FLASH Data bit6	I/O	PC14	A6
ND7	NAND FLASH Data bit7	I/O	PC15	B6

13. SD2.0 Controller

13.1. SD/MMC Overview

The SD/MMC can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Mem), Secure Digital I/O (SDIO), Multimedia Cards (MMC), and Consumer Electronics Advanced Transport Architecture (CE-ATA).

The SD/MMC controller includes the following features:

- Supports Secure Digital memory protocol commands
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands
- Supports CE-ATA digital protocol commands
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD or MMC (3.3 or 4.0) or CE-ATA device
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports SDIO read wait
- Supports block size of 1 to 65535 bytes
- Internal 16x32-bit (64 bytes total) FIFO for data transfer
- DMA interface for dedicated DMA transfer
- Only support 3.3 V IO pad

13.2. SD2.0 Controller Signal Description

Table 13-1. NAND Flash Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
SD1/SDIO1/MMC1(2.0)				
SDC1_CLK	SD1/SDIO1/MMC1 Output Clock	O	PE13 PC5	U2 C8
SDC1_CMD	SD1/SDIO1/MMC1 Cmmand Line	I/O	PE12 PC3	U1 E8
SDC1_D0	SD1/SDIO1/MMC1 Data bit0	I/O	PE14 PC12	U3 E7
SDC1_D1	SD1/SDIO1/MMC1 Data bit1	I/O	PE15	U4

Signal Name	Description	Type	Pin Name	Ball#
			PC13	F7
SDC1_D2	SD1/SDIO1/MMC1 Data bit2	I/O	PE16 PC14	V1 A6
SDC1_D3	SD1/SDIO1/MMC1 Data bit3	I/O	PE17 PC15	V2 B6
SD2/SDIO2/MMC2(2.0)				
SDC2_CLK	SD2/SDIO2/MMC2 Output Clock	O	PC7 PF2	A8 Y11
SDC2_CMD	SD2/SDIO2/MMC2 Cmmand Line	I/O	PC6 PF3	B8 Y12
SDC2_D0	SD2/SDIO2/MMC2 Data bit0	I/O	PC8 PF1	A7 W11
SDC2_D1	SD2/SDIO2/MMC2 Data bit1	I/O	PC9 PF0	B7 V11
SDC2_D2	SD2/SDIO2/MMC2 Data bit2	I/O	PC10 PF4	C7 W12
SDC2_D3	SD2/SDIO2/MMC2 Data bit3	I/O	PC11 PF5	D7 V12
SD3/SDIO3/MMC3(2.0)				
SDC3_CLK	SD3/SDIO3/MMC3 Output Clock	O	PA8 PE27	T9 P4
SDC3_CMD	SD3/SDIO3/MMC3 Cmmand Line	I/O	PA9 PE26	U9 P3
SDC3_D0	SD3/SDIO3/MMC3 Data bit0	I/O	PA7 PE28	Y8 P5
SDC3_D1	SD3/SDIO3/MMC3 Data bit1	I/O	PA6 PE29	W8 P6
SDC3_D2	SD3/SDIO3/MMC3 Data bit2	I/O	PA5 PE30	V8 R1
SDC3_D3	SD3/SDIO3/MMC3 Data bit3	I/O	PA4 PE31	U8 R2

14. SD3.0 Controller

14.1. SD3.0 Controller Overview

The SD3.0 controller can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

- The SD3.0 controller includes the following features:
- Supports Secure Digital memory protocol commands (up to SD3.0)
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands (up to MMC4.3)
- Supports CE-ATA digital protocol commands
- Supports eMMC boot operation and alternative boot operation
- Supports UHS-1card voltage switching and DDR R/W operation
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.3) or CE-ATA device
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports SDIO read wait
- Supports block size of 1 to 65535 bytes
- Supports descriptor-based internal DMA controller
- Internal 16x32-bit (64 bytes total) FIFO for data transfer
- Support 3.3 V and 1.8V IO pad

14.2. SD3.0 Controller Signal Description

Table 14-1. NAND Flash Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
SD0/SDIO0/MMC0(3.0)				
SDC0_CLK	SD0/SDIO0/MMC0 Output Clock	O	PF2	Y11
SDC0_CMD	SD0/SDIO0/MMC0 Cmmand Line	I/O	PF3	Y12
SDC0_D0	SD0/SDIO0/MMC0 Data bit0	I/O	PF1	W11
SDC0_D1	SD0/SDIO0/MMC0 Data bit1	I/O	PF0	V11
SDC0_D2	SD0/SDIO0/MMC0 Data bit2	I/O	PF5	V12
SDC0_D3	SD0/SDIO0/MMC0 Data bit3	I/O	PF4	W12

15. Memory Stick Card Controller

15.1. Memory Stick Overview

The Memory Stick Host Controller (MSHC) is one interface for transfer data between Host and external memory stick device. It includes the following features:

- Supports Memory Stick Version 1.x and Memory Stick PRO
- Memory Stick serial clock (Version 1.x : 20MHz (max), PRO: 40MHz (max))
- 32 Bytes Data FIFO for transfer
- Hardware CRC circuit
- Interrupt for Memory Stick Host Controller (MSHC)
- Dedicated DMA support
- Support 3.3 V IO pad

15.2. Memory Stick Card Controller Signal Description

Table 15-1. Memory Stick Card Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
MS(memory stick)				
MS_CLK	Memory Stick Serial Clock	O	PF2	Y11
MS_BS	Memory Stick Bus State	O	PF3	Y12
MS_D0	Memory Stick Data bit0	I/O	PF1	W11
MS_D1	Memory Stick Data bit1	I/O	PF0	V11
MS_D2	Memory Stick Data bit2	I/O	PF5	V12
MS_D3	Memory Stick Data bit3	I/O	PF4	W12

16. Two Wire Interface

16.1. TWI Controller Description

This 2-Wire Controller is designed to be used as an interface between CPU host and the serial 2-Wire bus. It can supports all the standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This 2-Wire Controller can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

The 2-Wire Controller includes the following features:

- Software-programmable for Slave or Master
- Supports Repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with 2-Wire bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s (‘fast mode’)
- Allows operation from a wide range of input clock frequencies

16.2. TWI Controller Signal Description

Table 16-1. TWI Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
I2C port0				
TWI0_SCK	I2C-BUS Clock for Channel0	I/O	PB0	B2
TWI0_SDA	I2C-BUS Data for Channel0	I/O	PB1	A1
I2C port1				
TWI1_SCK	I2C-BUS Clock for Channel1	I/O	PB18	T3
TWI1_SDA	I2C-BUS Data for Channel1	I/O	PB19	T4
I2C port2				
TWI2_SCK	I2C-BUS Clock for Channel2	I/O	PB20	P1
TWI2_SDA	I2C-BUS Data for Channel2	I/O	PB21	P2

17. SPI Interface

17.1. SPI Description

The SPI is the Serial Peripheral Interface which allows rapid data communication with less software interrupts. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode. It includes the following features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals for SPI0 and SPI1 has one chip select
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- DMA support

17.2. SPI Controller Signal Description

Table 17-1. SPI Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
Serial Port Interface(SPI0)				
SPI0_CS0	SPI0 Chip Select	I/O	PC23	D9
SPI0_MOSI	SPI0 Master data Out, Slave data In	I/O	PC0	C9
SPI0_MISO	SPI0 Master data In, Slave data Out	I/O	PC1	G8
SPI0_CLK	SPI0 Clock	I/O	PC2	F8
Serial Port Interface(SPI1)				
SPI1_CS0	SPI1 Chip Select 0	I/O	PI8 PA0	R3 V7
SPI1_CS1	SPI1 Chip Select 1	O	PI9	R4
SPI1_CLK	SPI1 Master data Out, Slave data In	I/O	PI10 PA1	R5 W7
SPI1_MOSI	SPI1 Master data In, Slave data Out	I/O	PI11 PA2	R6 Y7
SPI1_MISO	SPI1 Clock	I/O	PI12 PA3	R7 T8
Serial Port Interface(SPI2)				
SPI2_CS0	SPI2 Chip Select 0	I/O	PB14 PC19	P11 C10
SPI2_CS1	SPI2 Chip Select 1	O	PB13	Y10

Signal Name	Description	Type	Pin Name	Ball#
SPI2_CLK	SPI2 Master data Out, Slave data In	I/O	PB15 PC20	R11 G9
SPI2_MOSI	SPI2 Master data In, Slave data Out	I/O	PB16 PC21	T11 F9
SPI2_MISO	SPI2 Clock	I/O	PB17 PC22	U11 E9

18. UART Interface

18.1. UART Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Support IrDA 1.0 SIR
- Interrupt support for FIFOs, Status Change

18.2. UART Controller Signal Description

Table 18-1. UART Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
UART0				
UART0_TX	UART0 Transmit Data	O	PB22 PF2	T5 Y11
UART0_RX	UART0 Receive Data	I	PB23 PF4	T6 W12
UART1				
UART1_TX	UART1 Transmit Data	O	PA10	V9
UART1_RX	UART1 Receive Data	I	PA11	W9
UART1_RTS	UART1 Request To Send	O	PA12	Y9
UART1_CTS	UART1 Clear To Send	I	PA13	R10
UART1_DTR	UART1 Data Terminal Ready	O	PA14	T10
UART1_DSR	UART1 Data Set Ready	I	PA15	U10
UART1_DCD	UART1 Data Carrier Detect	I	PA16	V10
UART1_RING	UART1 Ring Indicator	I	PA17	W10
UART2				
UART2_RTS	UART2 Request To Send	O	PA0	V7
UART2_CTS	UART2 Clear To Send	I	PA1	W7
UART2_TX	UART2 Transmit Data	O	PA2	Y7
UART2_RX	UART2 Receive Data	I	PA3	T8
UART3				
UART3_TX	UART3 Transmit Data	O	PE18 PH0	V3 C6
UART3_RX	UART3 Receive Data	I	PE19 PH1	W1 D6
UART3_RTS	UART3 Request To Send	O	PE20 PH2	W2 E6
UART3_CTS	UART3 Clear To Send	I	PE21 PH3	Y1 F6
UART4				
UART4_TX	UART4 Transmit Data	O	PE22 PH4	Y2 A5
UART4_RX	UART4 Receive Data	I	PE23 PH5	W3 B5
UART5				
UART5_TX	UART5 Transmit Data	O	PH6	C5
UART5_RX	UART5 Receive Data	I	PH7	D5
UART6				
UART6_TX	UART6 Transmit Data	O	PA12	Y9
UART6_RX	UART6 Receive Data	I	PA13	R10

Signal Name	Description	Type	Pin Name	Ball#
UART7				
UART7_TX	UART7 Transmit Data	O	PA14	T10
UART7_RX	UART7 Receive Data	I	PA15	U10

19. PS/2 Interface

19.1. PS/2 Interface Overview

The PS/2 is a Dual-Role controller, which supports both device and host functions and is full compliant with IBM PS/2 in Personal Computer. It can be configured as a Host to connect PS/2 Keyboard or PS/2 Mouse; it can also be configured as Device to connect Computer. The PS/2 module can be integrated with industry-standard AMBA Peripheral Bus (APB) for communication with other system modules, such as ARM CPU, System Memory.

The PS/2 Module includes the following features:

- Compliance to IBM PS/2 and AT-Compatible Keyboard and Mouse Interface
- Dual Role Controller, it can be either a PS/2 Host or a PS/2 Device
- 4-byte TXFIFO and 4-byte RXFIFO for data buffering
- Odd parity generation and checking
- Register bits for override of keyboard clock and data lines
- Internal Clock Divider for Simple Clock Interface

19.2. PS/2 Controller Signal Description

Table 19-1. PS/2 Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
PS/2 port 0				
PS2_SCK0	PS/2 Clock	I/O	PB18 PE24	T3 T1
PS2_SDA0	PS/2 Data	I/O	PB19 PE25	T4 T2
PS/2 port 1				
PS2_SCK1	PS/2 Clock	I/O	PH12	C4
PS2_SDA1	PS/2 Data	I/O	PH13	D4

20. IR Interface

20.1. IR Overview

Fast Infrared Interface (FIR) signals are multiplexed with UART2 signals using a system configuration for a complete infrared interface that supports SIR, CIR, MIR, and FIR modes. The Serial Infrared (SIR) protocol, which supports data rate which supports data rates up to 1.875 Mbit/s, is implemented in each UART module. The IR includes the following features:

- Compliant with IrDA 1.1 for MIR and FIR
- Full physical layer implementation
- Supports 0.576 Mbit/s and 1.152 Mbit/s Medium Infrared (MIR) physical layer protocol
- Support 4 Mbit/s FIR physical layer protocol defined by IrDA version 1.4
- Support CIR for remote control or wireless keyboard
- Hardware CRC16 for MIR and CRC32 for FIR
- Dual 16x8-bits FIFO for data transfer
- Programmable FIFO thresholds
- Interrupt and DMA Support

20.2. IR Controller Signal Description

Table 20-1. IR Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
IR_TX	IR Transmit Data	O	PB3	G4
IR_RX	IR Receive Data	I	PB4	G3

21. USB OTG Controller

21.1. USB OTG Overview

The USB/OTG is a Dual-Role Device (DRD) controller, which supports both device and host functions and is full compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. The USB/OTG connects to the industry-standard AMBA High-Performance Bus (AHB) for communication with other system modules, such as AC320 CPU, System Memory. It is fully compliant with the AMBA Specification, Revision 2.0. As an AHB slave device, microcontroller can access its Control and Status Registers (CSRs), the Data FIFO (DFIFO), and queues. Industry standard Single Port RAM (SPRAM) is supported for saving area and power. The Single Port RAM is used as Data FIFO. Standard USB transceiver can be used through its UTMI+PHY Level2 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. In AHB slave mode, the data transfer between the USB/OTG and the system memory is handled by the application. For saving CPU bandwidth, USB/OTG DMA interface can support one external DMA controller to take care of the data transfer between the memory and USB/OTG core. The driver sets up the transfer and the USB/OTG interrupts the CPU only on transfer completion or and error condition. One central DMA engine is designed for the data transfer in system role. The DMA function can be disabled by software. The Host Negotiation Protocol (HNP), Session Request Protocol (SRP), and other critical functions are implemented in hardware for processing efficiency. The USB/OTG core also supports USB power saving functions.

The USB2.0 OTG controller System-Level block diagram is showed below:

The USB2.0 OTG controller (SIE) includes the following features:

- Complies with USB 2.0 Specification and its On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode and support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP)
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Supports up to 4 User-Configurable Endpoints for Bulk , Isochronous**,** Control and Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)

- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Dedicated Central DMA controller; data is transferred through Special bus for saving ABH bus bandwidth
- Supports industry-standard Single Port SRAM for USB Configurable Data FIFO; The size is 2112 byte with 32-bit word width; The RAM can be used by other modules when USB/OTG disable

21.2. USB Controller Signal Description

Table 21-1. USB Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
USB0 OTG 2.0				
DM0	USB0 OTG Data(-)	I/O	DM0	U19
DP0	USB0 OTG Data(+)	I/O	DP0	U20
USB1 HOST 2.0				
DM1	USB1 HOST Data(-)	I/O	DM1	R17
DP1	USB1 HOST Data(+)	I/O	DP1	R18
USB2 HOST 2.0				
DM2	USB2 HOST Data(-)	I/O	DM2	T17
DP2	USB2 HOST Data(+)	I/O	DP2	T18

22. Digital Audio Interface

22.1. Digital Audio Interface Overview

The Digital Audio Interface can be configured as I2S interface or PCM interface by software. When configured as I2S interface, it can support the industry standard format for I2S, left-justified, or right-justified. PCM is a standard method used to digital audio for transmission over digital communication channels. It supports linear 13 or 16-bits linear or 8-bit u-law or A-law companded sample formats at 8K samples/s and can receive and transmit on any selection of four of the first four slots following PCM_SYNC. It includes the following features:

- I2S or PCM configured by software
- Full-duplex synchronous serial interface
- Master / Slave Mode operation configured by software
- Audio data resolutions of 16, 20, 24
- I2S Audio data sample rate from 8Khz to 192Khz
- I2S Data format for standard I2S, Left Justified and Right Justified
- I2S support 8 channel output and 2 channel input
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law companded sample
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA Support
- Two 32-bits Counters for AV sync application
- Loopback mode for test

22.2. Digital Audio Signal Description

Table 22-1. Digital Audio Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
I2S_MCLK	I2S Main Clock(system clock)	O	PB5	C2
I2S_BCLK	I2S serial Bit Clock	I/O	PB6	C1
I2S_LRCK	I2S Left or Right channel select clock(frame clock)	I/O	PB7	D2
I2S_DO0	I2S serial Data Output bit0	O	PB8	D1
I2S_DO1	I2S serial Data Output bit1	O	PB9	E3
I2S_DO2	I2S serial Data Output bit2	O	PB10	E2
I2S_DO3	I2S serial Data Output bit3	O	PB11	E1
I2S_DI	I2S serial Data Input	I	PB12	F4

23. AC97 Interface

23.1. AC97 Interface Overview

The AC97 interface supports AC97 revision 2.3 features. AC97 controller communicates with AC97 Codec using an audio controller link (AC-link). Controller sends the stereo PCM data to Codec. The external digital-to-analog converter (DAC) in the Codec converts the audio sample to an analog audio waveform. Controller receives the stereo PCM data and the mono Microphone data from Codec then stores in memories.

AC97 Interface includes below features:

- Compliant with AC97 2.3 component Specification
- Full-duplex synchronous serial interface
- Support 2 channels, TX (stereo),RX (PCM stereo, MIC mono optional)
- Variable Sampling Rate AC97 Codec Interface support, up to 48KHz
- Support 2 channel and 6 channel audio data output
- DRA mode support
- Only one primary Codec support
- Channels support mono or stereo samples of 16(standard), 18(optional) and 20(optional) bit wide.
- One 96×20bits FIFO and one 32×20-bits FIFO for data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

23.2. AC97 Signal Description

Table 23-1. AC97 Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
AC97_MCLK	AC97 Codec Input Mclk	O	PB5	C2
AC97_BCLK	Digital Audio Serial Clock Provided by AC97 Codec	I	PB6	C1
AC97_SYNC	Digital Audio Sample rate/sync	O	PB7	D2
AC97_DO	Digital Audio Serial Data Input	I	PB8	D1
AC97_DI	Digital Audio Serial Data Onput	O	PB12	E3

24. SPDIF Interface

24.1. SPDIF interface Overview

24.1.1. Features

- IEC-60958 transmitter and receiver functionality
- Support channel status capture on the receiver
- Support channel status insertion for the transmitter
- Hardware Parity checking on the receiver
- Hardware Parity generation on the transmitter
- One 32×24bits FIFO (TX) and one32×24bits FIFO (RX) for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

24.2. SPDIF Signal Description

Table 24-1. SPDIF Controller Signal Description

Signal Name	Description	Type	Pin Name	Ball#
SPDIF_MCLK	SPDIF Main Clock	O	PB3	G4
SPDIF_DI	SPDIF Data Input	I	PB12	F4
SPDIF_DO	SPDIF Data Onput	O	PB13	Y10

25. Ethernet MAC

25.1. EMAC Overview

The Ethernet MAC Controller enables the host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard. It supports 10M/100M external PHY with MII interface in both full and half duplex mode. A 16K Byte SRAM is provided to keeping continuous data transmission, and Flow control, DA/SA filtering is also supported in the module.

The Ethernet MAC Controller (EMAC) includes the following features:

- Compatible with IEEE802.3standards
- Support 10/100Mbps data rate
- Support full and half duplex operations
- Support IEEE 802.3x flow control for full-duplex operation
- Support back-pressure flow control for half-duplex operation
- Support DA/SA Filtering
- Support Loop back operations
- Provide MII Interface for external Ethernet PHY
- 3K Bytes FIFO for TX
- 13K Bytes FIFO for RX

25.2. Ethernet Signal Description

Table 25-1. Ethernet Signal Description

Signal Name	Description	Type	Pin Name	Ball#
ERXD3	EMAC MII Receive Data Nibble Data Bit3	I	PA0	V7
ERXD2	EMAC MII Receive Data Nibble Data Bit2	I	PA1	W7
ERXD1	EMAC MII Receive Data Nibble Data Bit1	I	PA2	Y7
ERXD0	EMAC MII Receive Data Nibble Data Bit0	I	PA3	T8
ETXD3	EMAC MII Transmit Data Nibble Data Bit3	O	PA4	U8
ETXD2	EMAC MII Transmit Data Nibble Data Bit2	O	PA5	V8
ETXD1	EMAC MII Transmit Data Nibble Data Bit1	O	PA6	W8
ETXD0	EMAC MII Transmit Data Nibble Data Bit0	O	PA7	Y8
ERXCK	EMAC MII Receive Clock Input	I	PA8	T9
ERXERR	EMAC MII Receive Error	I	PA9	U9
ERXDV	EMAC MII Receive Data Valid	I	PA10	V9
EMDC	EMAC MII Management Data Clock	O	PA11	W9
EMDIO	EMAC MII Management Data Input/Output	I/O	PA12	Y9
ETXEN	EMAC MII Transmit Enable	O	PA13	R10

Signal Name	Description	Type	Pin Name	Ball#
ETXCK	EMAC MII Transmit Clock Input	I	PA14	T10
ECRS	EMAC MII Carrier Sense	I	PA15	U10
ECOL	MII Collision Detect	I	PA16	V10
ETXERR	EMAC MII Transmit Error	O	PA17	W10

26. Transport Stream Controller

26.1. Transport Stream Controller (TSC) Overview

The ITU-T Rec. H.222.0 | ISO/IEC Transport Stream coding layer all owns one or more programs to be combined into a single stream. The DVB demodulator can output transport stream by SPI (Synchronous Parallel Interface) or SSI (Synchronous Serial Interface). The TSC can receive one SPI or one SSI transport stream with software configurable packet format. Since there are one or more programs and there are more elementary streams within a program. By their PID, the TSC can filter out the unused streams and put the streams into the specified memory space. The 16-channel filter can be support by the TSC.

Since there are some Transport Stream files stored in solid storage media, such as NAND Flash, HDD, SD/MMC card, Memory Stick Card, UDISK. The MPEG Transport Stream can be received from network, such as WLAN, Ethernet LAN. The TSC can read these transport streams from DRAM and generate internal SPI transport stream. The TSC can select the internal SPI transport stream by TS switch. The selected streams are feed into PID filter. The filtered streams are stored into external DRAM memory.

TSC – TS Controller

TSF – TS Filter

TSD – TS Descrambler

TSG – TS Generator

The Transport Stream Controller (TSC) includes the following features:

- One external Synchronous Parallel Interface (SPI) or one external Synchronous Serial Interface (SSI)
- 32 channels PID filter
- Multiple transport stream packet (188, 192, 204) format support
- SPI and SSI timing parameters are configurable
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- Configurable SPI transport stream generator for streams in DRAM memory
- DMA is supported for transferring data
- Interrupt is supported
- Support DVB-CSA V1.1 Descrambler

26.2. Transport Stream Signal Description

Table 26-1. Transport Stream Signal Description

Signal Name	Description	Type	Pin Name	Ball#
TS0				
TS0_CLK	TS System Clock	I	PE0 PD0	Y3 J4
TS0_ERR	TS Error indicate Signal	I	PE1 PD1	V4 J3
TS0_SYNC	TS Synchronization control signal	I	PE2 PD2	W4 J2
TS0_DVLD	TS valid signal	I	PE3 PD3	Y4 J1
TS0_D0	TS input Data bit0	I	PE4 PD20	U5 M5
TS0_D1	TS input Data bit1	I	PE5 PD21	V5 M6
TS0_D2	TS input Data bit2	I	PE6 PD22	W5 N1
TS0_D3	TS input Data bit3	I	PE7 PD23	Y5 N2
TS0_D4	TS input Data bit4	I	PE8 PD24	U6 N3
TS0_D5	TS input Data bit5	I	PE9 PD25	V6 N4
TS0_D6	TS input Data bit6	I	PE10 PD26	W6 N5
TS0_D7	TS input Data bit7	I	PE11 PD27	Y6 N6
TS1				
TS0_CLK	TS System Clock	I	PE12	U1
TS0_ERR	TS Error indicate Signal	I	PE13	U2
TS0_SYNC	TS Synchronization control signal	I	PE14	U3
TS0_DVLD	TS valid signal	I	PE15	U4
TS0_D0	TS input Data bit0	I	PE16	V1
TS0_D1	TS input Data bit1	I	PE17	V2
TS0_D2	TS input Data bit2	I	PE18	V3
TS0_D3	TS input Data bit3	I	PE19	W1
TS0_D4	TS input Data bit4	I	PE20	W2
TS0_D5	TS input Data bit5	I	PE21	Y1
TS0_D6	TS input Data bit6	I	PE22	Y2
TS0_D7	TS input Data bit7	I	PE23	W3

27. Smart Card Reader

27.1. SCR Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the system and Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation. Cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

The SCR includes the following features:

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Support adjustable clock rate and bit rate
- Configurable automatic byte repetition
- Support commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission, and
  - T=1 for asynchronous half-duplex block transmission
- Support FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Support configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

27.2. Smart Card Signal Description

Table 27-1. Smart Card Signal Description

Signal Name	Description	Type	Pin Name	Ball#
SMC_VPPEN	SMC Programming Voltage Enable	O	PE5	V5
SMC_VPPPP	SMC Programming Voltage	I/O	PE6	W5
SMC_DET	SMC Insert Detect	I	PE7	Y5
SMC_VCCEN	SMC power supply Enable	O	PE8	U6
SMC_RST	SMC Reset signal Output	O	PE9	V6
SMC_SLK	SMC Clock signal Output	O	PE10	W6
SMC_SDA	SMC Serial Data for Input/Output	I/O	PE11	Y6

28. ATA Interface

28.1. ATA Overview

The ATA Interface module is an IDE (Integrated Drive Electronics) controller, which can be configured either as a HD (Hard Disk) Controller or as a CF (Compact Flash) Card Controller.

The ATA Interface includes the following features:

- Support for two IDE devices in one channel
- Independently programmable timing for each device
- Programmable posted writes and read-prefetch for each channel
- Supports:
  - PIO Modes 0, 2, 3, 4
  - Programmable DMA
  - Ultra DMA 0, 1, 2 (33), 3, 4 (66)
- Support for external bi-directional buffers if required

28.2. ATA Signal Description

Table 28-1. ATA Signal Description

Signal Name	Description	Type	Pin Name	Ball#
ATAA0	ATA Address bit0	O	PH0	C6
ATAA1	ATA Address bit1	O	PH1	D6
ATAA2	ATA Address bit2	O	PH2	E6
ATAIRQ	ATA Interrupt Request from IDE Device	I	PH3	F6
ATAD0	ATA Data input and output bit0	I/O	PH4	A5
ATAD1	ATA Data input and output bit1	I/O	PH5	B5
ATAD2	ATA Data input and output bit2	I/O	PH6	C5
ATAD3	ATA Data input and output bit3	I/O	PH7	D5
ATAD4	ATA Data input and output bit4	I/O	PH8	E5
ATAD5	ATA Data input and output bit5	I/O	PH9	F5
ATAD6	ATA Data input and output bit6	I/O	PH10	A4
ATAD7	ATA Data input and output bit7	I/O	PH11	B4
ATAD8	ATA Data input and output bit8	I/O	PH12	C4
ATAD9	ATA Data input and output bit9	I/O	PH13	D4
ATAD10	ATA Data input and output bit10	I/O	PH14	E4
ATAD11	ATA Data input and output bit11	I/O	PH15	A3
ATAD12	ATA Data input and output bit12	I/O	PH16	B3
ATAD13	ATA Data input and output bit13	I/O	PH17	C3
ATAD14	ATA Data input and output bit14	I/O	PH18	G2

Signal Name	Description	Type	Pin Name	Ball#
ATAD15	ATA Data input and output bit15	I/O	PH19	G1
ATAOE	ATA Output Enable for external bus buffer direction control. '1'—Host to Device; '0' – Device to Host.	O	PH20	H6
ATADREQ	ATA DMA Request from IDE Device	I	PH21	H5
ATADACK	ATA DMA Acknowledge for ATA_DREQ	O	PH22	H4
ATACS0	ATA Chip Select 0, Active Low	O	PH23	H3
ATACS1	ATA Chip Select 1, Active Low	O	PH24	H2
ATAIORDY	ATA IO Ready	I	PH25	H1
ATAIOR	ATA IO Read Enable, Active Low	O	PH26	J6
ATAIOW	ATA IO Write Enable, Active Low	O	PH27	J5

29. CAN Bus

29.1. CAN Overview

The CAN module is a controller for the Controller Area Network (CAN) used in automotive and general industrial environments. It implements the CAN 2.0A/B protocol as defined in the BOSCH CAN bus specification 2.0.

The CAN controller includes the following features:

- Supports the CAN 2.0A and 2.0B protocol specification
- Programmable data rate up to 1Mbps
- 64 byte receive buffers
- Support one-shot transmission option
- Supports two configurable filter modes
- Supports listen only mode
- Supports self-test mode

29.2. CAN Bus Signal Description

Table 29-1. CAN Bus Signal Description

Signal Name	Description	Type	Pin Name	Ball#
CAN_TX	CAN Transmit Data	O	PH20 PA16	H6 V10
CAN_RX	Can Receive Data	I	PH21 PA17	H5 W10

30. Audio Codec

30.1. Audio Codec Overview

Embedded Audio Codec Includes below features:

- On-chip 24-bits DAC for play-back
- On-chip 24-birs ADC fro recorder
- On-chip Class-D Power Amplifier for speaker
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- Support FM/ Line-in/ Microphone recorder

30.2. Audio Codec Signal Description

Table 30-1. Audio Codec Signal Description

Signal Name	Description	Type	Pin Name	Ball#
HPL	Audio DAC(24bit) output for Left channel ofHeadphone	AO	HPL	U14
HPR	Audio DAC(24bit) output for Right channel of Headphone	AO	HPR	T14
HPCOM	Audio DAC(24bit) amplifier output	A	HPCOM	V14
HPCOM_FB	Audio DAC(24bit) amplifier Feedback	A	HPCOM_FB	V15
FMINL	Audio ADC(24bit) Input for Left channel of FM radio	AI	FMINL	W16
FMINR	Audio ADC(24bit) Input for Right channel of FM radio	AI	FMINR	Y16
LINEINL	Audio ADC(24bit) Input for Left channel of Line In	AI	LINEINL	Y15
LINEINR	Audio ADC(24bit) Input for Right channel of Line In	AI	LINEINR	W15
MICINL	Audio ADC(24bit) Input for Left channel of Microphone	AI	MICINL	W17
MICINR	Audio ADC(24bit) Input for Right channel of Microphone	AI	MICINR	Y17

31. LRADC

31.1. LRADC Description

LRADC is 6-bit resolution for key matrix application. The LRADC can work up to maximum conversion rate of 250Hz. Besides using for ordinary key application, the LRADC can also use for special hold key application.

System features listed below:

- Interrupt support
- 6-bit Resolution
- Voltage input range between 0 to 0.67*AVCC (AVCC is LRADC reference voltage)
- Sample rate up to 250Hz

31.2. LRADC Signal Description

Table 31-1. LRADC Signal Description

Signal Name	Description	Type	Pin Name	Ball#
LRADC0	Low Resolution ADC0 input(6bit)	AI	LRADC0	U15
LRADC1	Low Resolution ADC1 input(6bit)	AI	LRADC1	T15

32. Keypad Interface

32.1. Keypad Interface Description

The Keypad Interface is used for connecting external keypad devices. It can provide up to 8 rows and 8 columns. The events of key press or key release can be detected to the CPU by an interrupt. To prevent the switching noises, internal debouncing filter is provided.

The Keypad Interface includes the following features:

- Interrupt for key press or key release
- Internal debouncing filter to prevent the switching noises

32.2. Keypad Signal Description

Table 32-1. Keypad Signal Description

Signal Name	Description	Type	Pin Name	Ball#
KP_IN0	Keypad Interface Row0 data	I	PD4 PH8	K6 E5
KP_IN1	Keypad Interface Row1 data	I	PD5 PH9	K5 F5
KP_IN2	Keypad Interface Row2 data	I	PD6 PH10	K4 A4
KP_IN3	Keypad Interface Row3 data	I	PD7 PH11	K3 B4
KP_IN4	Keypad Interface Row4 data	I	PD8 PH14	K2 E4
KP_IN5	Keypad Interface Row5 data	I	PD9 PH15	K1 A3
KP_IN6	Keypad Interface Row6 data	I	PD10 PH16	L1 B3
KP_IN7	Keypad Interface Row7 data	I	PD11 PH17	L2 C3
KP_OUT0	Keypad Interface Column0 data	O	PD12 PH18	L3 G2
KP_OUT1	Keypad Interface Column1 data	O	PD13 PH19	L4 G1
KP_OUT2	Keypad Interface Column2 data	O	PD14 PH22	L5 H4
KP_OUT3	Keypad Interface Column3 data	O	PD15 PH23	L6 H3

Signal Name	Description	Type	Pin Name	Ball#
KP_OUT4	Keypad Interface Column4 data	O	PD16 PH24	M1 H2
KP_OUT5	Keypad Interface Column5 data	O	PD17 PH25	M2 H1
KP_OUT6	Keypad Interface Column6 data	O	PD18 PH26	M3 J6
KP_OUT7	Keypad Interface Column7 data	O	PD19 PH27	M4 J5

33. Security System

33.1. Security System Description

The Security System (SS) is one encrypt/ decrypt function accelerator. It is suitable for a variety of applications. It supports both encryption and decryption. Several modes are support by the SS module. Both of CPU mode and DMA method are supported for different application.

It includes the following features:

- AES, DES, 3DES, SHA-1, MD5 are supported by this system
- ECB, CBC, CNT modes for AES/DES/3DES
- 128-bits, 192-bits and 256-bits key size for AES
- 32-words RX FIFO and 32-words TX FIFO for high speed application
- CPU mode and DMA mode are supported
- Interrupt supported

34. Touch Panel

34.1. TP Description

TPADC is 11-bit for touch screen application or for normal ADC application. The TPADC can work up to maximum conversion rate of 8 KHz. The TPADC can also used for 4-channels normal ADC application.

Touch Panel Controller's features are listed below:

- Interrupt support
- 11-bit Resolution
- Voltage input range between 0V to 2/3AVCC(2.0V)
- Sample rate up to 128K
- 32-level FIFO for touch Panel data
- Software configured sample FIFO trigger level
- Software configured sample period for Touch Screen application
- 4 channels auxiliary analog input for normal ADC application
- Normal DMA support

34.2. Touch Panel Signal Description

Table 34-1. Touch Panel Signal Description

Signal Name	Description	Type	Pin Name	Ball#
X1	Touch Pane ADC input(11bit)	AI	X1	U13
X2	Touch Pane ADC input(11bit)	AI	X2	T13
Y1	Touch Pane ADC input(11bit)	AI	Y1	R13
Y2	Touch Pane ADC input(11bit)	AI	Y2	P13

35. Port Controller

35.1. Port Description

The chip has 8 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 18 input/output port
- Port B(PB): 24 input/output port
- Port C(PC): 24 input/output port
- Port D(PD): 28 input/output port
- Port E(PE) : 32 input/output port
- Port F(PF) : 6 input/output port
- Port G(PG) : 10 input/output port
- Port H(PH) : 28 input/output port
- Port I(PI) : 13 input/output port
- Port S(PS) : 68 input/output port for DRAM controller

For various system configurations, these ports can be easily configured by software. All these ports (except PS) can be configured as GPIO if multiplexed functions not used. 32 external PIO interrupt sources are supported and interrupt mode can be configured by software.

35.2. Port Configuration Table

Refer to Section 5.2.

36. Display Engine Sub-System

36.1. Display Engine Sub-system Description

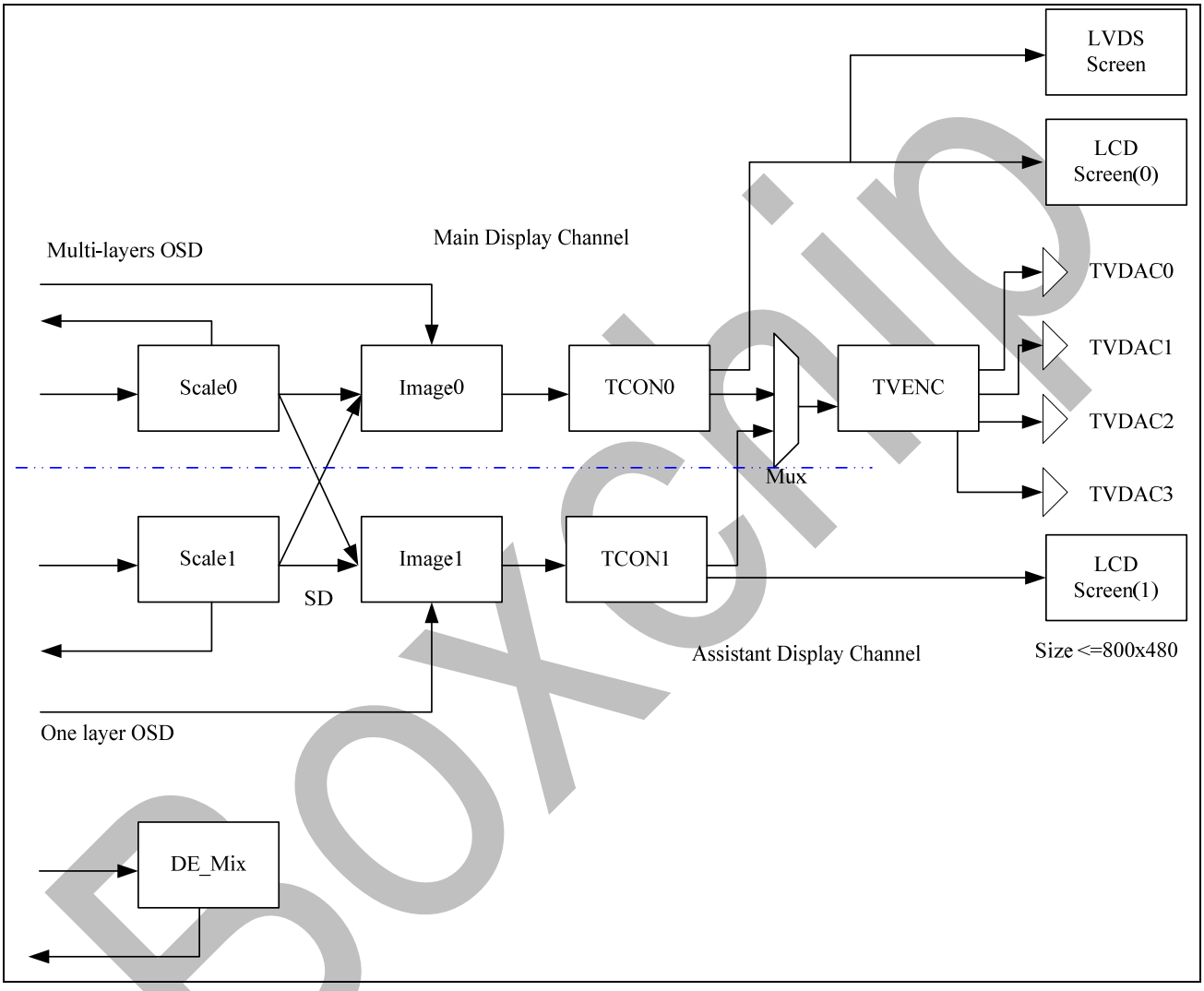


Figure 33-1 F20 Display Engine Sub-system Block Diagram

37. Display Scalar 0/1

37.1. Overview

The scalar performs video/graphic scale, format conversion and color space conversion. It is composed of DMA controller, scalar, color space conversion and output controller as show in figure 34-1.

37.2. Block Diagram

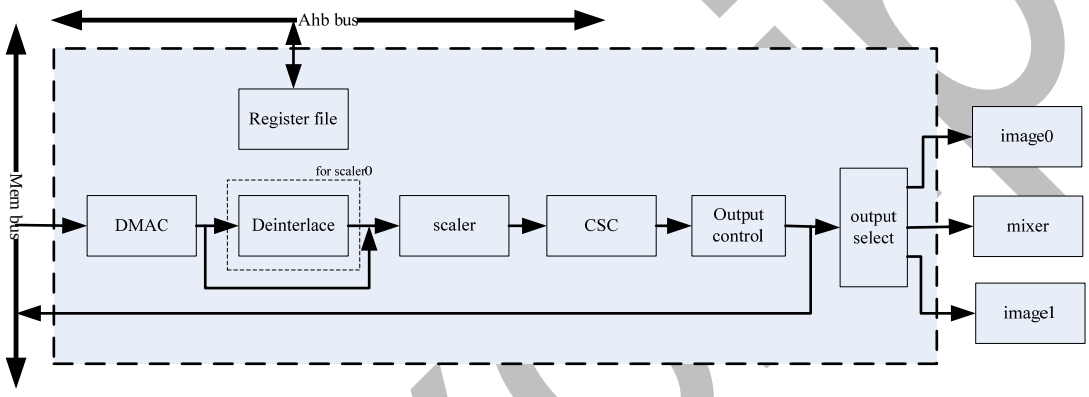


Figure 34-1 F20 Scalar Block Diagram

37.3. Features

Scalar 0:

- Output scan type: interlace/progressive
- De-interlace method: weave/bob/maf/maf-bob
- Input format: YUV444/YUV422/YUV420/YUV411/RGB
- Direct display output format: RGB
- Write back output format: RGB/YUV444/YUV420/YUV422/YUV411
- 3 channel scaling pipelines for scaling up/down
- Programmable source image size from 8x4 to 8192x8192 resolution
- Programmable destination image size from 8x4 to 8192x8192 resolution
- tap scale filter in horizontal and in vertical direction
- 32 Programmable coefficients for each tap
- Color space conversion between YUV and RGB
- Output support directly display and write back to memory

Scalar 1:

- Output scan type: interlace/progressive

- Input format: YUV444/YUV422/YUV420/YUV411/RGB
- Direct display output format: RGB
- Write back output format: RGB/YUV444/YUV420/YUV422/YUV411
- 3 channel scaling pipelines for scaling up/down
- Programmable source image size from 8x4 to 8192x8192 resolution
- Programmable destination image size from 8x4 to 2048x2048 resolution
- tap scale filter in horizontal and in vertical direction
- 32 Programmable coefficients for each tap
- Color space conversion between YUV and RGB
- Output support directly display and write back to memory

38. Display Engine (BE0)

38.1. Display engine back-end

- 4 moveable & size-adjustable layers
- Layer size up to 2048*2048 pixels
- Alpha blending support
- Color key support
- Write back function support
- 1/2/4/8 bpp mono / palette support
- 16/24/32 bpp color support (external frame buffer)
  - ----5/6/5
  - ----1/5/5/5
  - ----0/8/8/8
  - ----8/8/8/8
- On chip SRAM support
  - ----256 entry 32-bpp palette
  - ----1/2/4/8 bpp internal frame buffer
  - ----Gamma correction support
- Hardware cursor support
  - ----32*32 @8-bpp
  - ----64*64 @2-bpp
  - ----64*32 @4-bpp
  - ----32*64 @4-bpp
- Sprite function support
  - ----32bpp true color or 8bpp palette mode
  - ----up to 32 independent sprite blocks
  - ----each block can be set arbitrary coordinate
  - ----the block size can be adjust (8/16/32/64)
- YUV input channel support
- Vertical keystone correction
- Output color correction

39. Display Engine (BE1)

39.1. Feature

39.1.1. Display engine back-end 1

- 2 moveable & size-adjustable layers
- Layer size up to 2048*2048 pixels
- Alpha blending support
- 16/32 bpp & palette mode support (external frame buffer)

40. Camera sensor interface

40.1. Feature

- 8 bits input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Received data double buffer support
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or MB Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software

40.2. Camera sensor Signal Description

Table 40-1. Camera sensor Signal Description

Signal Name	Description	Type	Pin Name	Ball#
COMS Sensor0				
CSI0_PCK	CMOS Sensor Pixel Clock	I	PE0	Y3
CSI0_MCK	CMOS Sensor Clock Output	O	PE1	V4 U2
CSI0_HSYNC	CMOS Sensor Horizontal Synchronization	I	PE2	W4
CSI0_VSYNC	CMOS Sensor Verizontal Synchronization	I	PE3	Y4
CSI0_D0	Digital Image Data bit 0	I	PE4	U5
CSI0_D1	Digital Image Data bit 1	I	PE5	V5
CSI0_D2	Digital Image Data bit 2	I	PE6	W5
CSI0_D3	Digital Image Data bit 3	I	PE7	Y5
CSI0_D4	Digital Image Data bit 4	I	PE8	U6
CSI0_D5	Digital Image Data bit 5	I	PE9	V6
CSI0_D6	Digital Image Data bit 6	I	PE10	W6
CSI0_D7	Digital Image Data bit 7	I	PE11	Y6
COMS Sensor1				
CSI0_PCK	CMOS Sensor Pixel Clock	I	PE12	U1
CSI1_MCK	CMOS Sensor Clock Output	O	PE13	U2
CSI1_HSYNC	CMOS Sensor Horizontal Synchronization	I	PE14	U3
CSI1_VSYNC	CMOS Sensor Verizontal Synchronization	I	PE15	U4
CSI1_D0	Digital Image Data bit 0	I	PE16	V1
CSI1_D1	Digital Image Data bit 1	I	PE17	V2
CSI1_D2	Digital Image Data bit 2	I	PE18	V3
CSI1_D3	Digital Image Data bit 3	I	PE19	W1

Signal Name	Description	Type	Pin Name	Ball#
CSI1_D4	Digital Image Data bit 4	I	PE20	W2
CSI1_D5	Digital Image Data bit 5	I	PE21	Y1
CSI1_D6	Digital Image Data bit 6	I	PE22	Y2
CSI1_D7	Digital Image Data bit 7	I	PE23	W3

41. Universal LCD/TV Timing Controller

This IP is expected to drive a wide range of LCD panels; it also can generate 4-4-4 YUV signals for TV encoder. Its main function is to convert the pixel stream from the graphic engine or DMA, to the wide range digital/analog LCD display panels.

41.1. Feature

- System clock SCLK: 270－297MHz
- Programmable IO standard by VCCIO(3.3v/2.5v/1.8v)
- 3 input source: 2 DE sources and one DMA source
- Support simultaneous display (different picture/video) for both LCD and TV
- Support HV-DE-Sync(digital parallel RGB) input LCD panels(Max 1024*1024 resolution, 24-bit color)
- Support HV-DE-Sync(digital serial RGB, both delta and stripe panel) input LCD panels(Max 680*1024 resolution, up to true color)
- Support TTL(digital RGB) input LCD panels(Max 1024*1024 resolution, 18-bit color)
- Support Analog RGB input LCD panels(Max 1024*1024 resolution, 3 channel 6bit DAC output)
- Support 18/16/9/8bit 8080 CPU I/F panels(Max 1024*1024 resolution)
- CCIR656 output interface for LCD panel or TV encoder
- Up to full HDTV timing for TV encoder and HDMI transmitter
- Internal line scaling and Gamma correction
- 4 interrupts for programmer

41.2. LCD Signal Description

Table 41-1. LCD Signal Description

Signal Name	Description	Type	Pin Name	Ball#
LCD Controller0 for RGB Interface				
LCD0_CLK	LCD RGB Pixel Clock	O	PD0	J4
LCD0_DE	LCD RGB Data Enable	O	PD1	J3
LCD0_HSYNC	LCD RGB Horizontal Synchronization	O	PD2	J2
LCD0_VSYNC	LCD RGB Verizontal Synchronization	O	PD3	J1
LCD0_D0	LCD Pixel Data bit 0	O	PD4	K6
LCD0_D1	LCD Pixel Data bit 1	O	PD5	K5
LCD0_D2	LCD Pixel Data bit 2	O	PD6	K4
LCD0_D3	LCD Pixel Data bit 3	O	PD7	K3
LCD0_D4	LCD Pixel Data bit 4	O	PD8	K2
LCD0_D5	LCD Pixel Data bit 5	O	PD9	K1
LCD0_D6	LCD Pixel Data bit 6	O	PD10	L1

Signal Name	Description	Type	Pin Name	Ball#
LCD0_D7	LCD Pixel Data bit 7	O	PD11	L2
LCD0_D8	LCD Pixel Data bit 8	O	PD12	L3
LCD0_D9	LCD Pixel Data bit 9	O	PD13	L4
LCD0_D10	LCD Pixel Data bit 10	O	PD14	L5
LCD0_D11	LCD Pixel Data bit 11	O	PD15	L6
LCD0_D12	LCD Pixel Data bit 12	O	PD16	M1
LCD0_D13	LCD Pixel Data bit 13	O	PD17	M2
LCD0_D14	LCD Pixel Data bit 14	O	PD18	M3
LCD0_D15	LCD Pixel Data bit 15	O	PD19	M4
LCD0_D16	LCD Pixel Data bit 16	O	PD20	M5
LCD0_D17	LCD Pixel Data bit 17	O	PD21	M6
LCD0_D18	LCD Pixel Data bit 18	O	PD22	N1
LCD0_D19	LCD Pixel Data bit 19	O	PD23	N2
LCD0_D20	LCD Pixel Data bit 20	O	PD24	N3
LCD0_D21	LCD Pixel Data bit 21	O	PD25	N4
LCD0_D22	LCD Pixel Data bit 22	O	PD26	N5
LCD0_D23	LCD Pixel Data bit 23	O	PD27	N6
LCD Controller1 for RGB Interface				
LCD1_CLK	LCD RGB Pixel Clock	O	PD0 PH0	J4 C6
LCD1_DE	LCD RGB Data Enable	O	PD1 PH1	J3 D6
LCD1_HSYNC	LCD RGB Horizontal Synchronization	O	PD2 PH2	J2 E6
LCD1_VSYNC	LCD RGB Verizontal Synchronization	O	PD3 PH3	J1 F6
LCD1_D0	LCD Pixel Data bit 0	O	PD4 PH4	K6 A5
LCD1_D1	LCD Pixel Data bit 1	O	PD5 PH5	K5 B5
LCD1_D2	LCD Pixel Data bit 2	O	PD6 PH6	K4 C5
LCD1_D3	LCD Pixel Data bit 3	O	PD7 PH7	K3 D5
LCD1_D4	LCD Pixel Data bit 4	O	PD8 PH8	K2 E5
LCD1_D5	LCD Pixel Data bit 5	O	PD9 PH9	K1 F5
LCD1_D6	LCD Pixel Data bit 6	O	PD10	L1

Signal Name	Description	Type	Pin Name	Ball#
			PH10	A4
LCD1_D7	LCD Pixel Data bit 7	O	PD11 PH11	L2 B4
LCD1_D8	LCD Pixel Data bit 8	O	PD12 PH12	L3 C4
LCD1_D9	LCD Pixel Data bit 9	O	PD13 PH13	L4 D4
LCD1_D10	LCD Pixel Data bit 10	O	PD14 PH14	L5 E4
LCD1_D11	LCD Pixel Data bit 11	O	PD15 PH15	L6 A3
LCD1_D12	LCD Pixel Data bit 12	O	PD16 PH16	M1 B3
LCD1_D13	LCD Pixel Data bit 13	O	PD17 PH17	M2 C3
LCD1_D14	LCD Pixel Data bit 14	O	PD18 PH18	M3 G2
LCD1_D15	LCD Pixel Data bit 15	O	PD19 PH19	M4 G1
LCD1_D16	LCD Pixel Data bit 16	O	PD20 PH20	M5 H6
LCD1_D17	LCD Pixel Data bit 17	O	PD21 PH21	M6 H5
LCD1_D18	LCD Pixel Data bit 18	O	PD22 PH22	N1 H4
LCD1_D19	LCD Pixel Data bit 19	O	PD23 PH23	N2 H3
LCD1_D20	LCD Pixel Data bit 20	O	PD24 PH24	N3 H2
LCD1_D21	LCD Pixel Data bit 21	O	PD25 PH25	N4 H1
LCD1_D22	LCD Pixel Data bit 22	O	PD26 PH26	N5 J6
LCD1_D23	LCD Pixel Data bit 23	O	PD27 PH27	N6 J5
LCD Controller for LVDS Interface				
LVDS_VP3	LVDS Output Data+ for Channel 3	O	PG0	T19
LVDS_VN3	LVDS Output Data- for Channel 3	O	PG1	T20
LVDS_VP2	LVDS Output Data+ for Channel 2	O	PG4	P19

Signal Name	Description	Type	Pin Name	Ball#
LVDS_VN2	LVDS Output Data- for Channel 2	O	PG5	P20
LVDS_VP1	LVDS Output Data+ for Channel 1	O	PG6	N19
LVDS_VN1	LVDS Output Data- for Channel 1	O	PG7	N20
LVDS_VP0	LVDS Output Data+ for Channel 0	O	PG8	M19
LVDS_VN0	LVDS Output Data- for Channel 0	O	PG9	M20
LVDS_VPC	LVDS Output Clock+ for Channel 0	O	PG2	R19
LVDS_VNC	LVDS Output Clock- for Channel 0	O	PG3	R20

42. Mixer Engine

42.1. Feature

42.2. Mixer

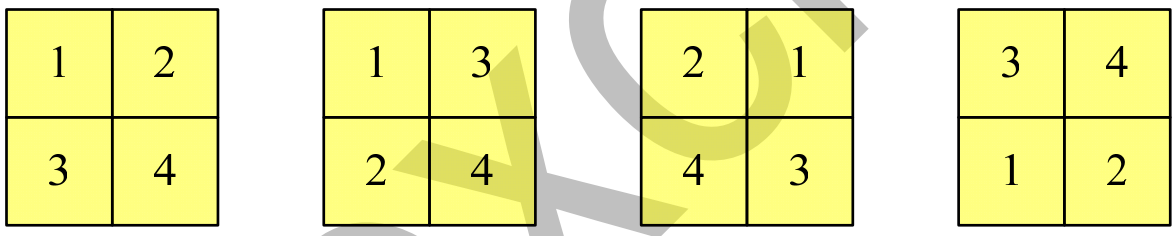
42.3. Block diagram

42.4. Mixer

42.4.1. Mixer description

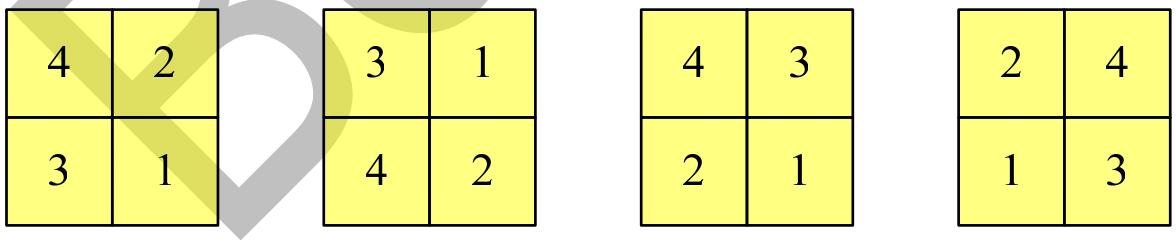
42.4.2. Layer rotation and mirroring control

Each layer data can be realized rotation and mirror operation function, total 8 operation according 8 control code, reference the following diagram.



Control code:

Normal A X Y



Control code:

AXY AY XY AX

43. TV Encoder

43.1. Feature

- Multi-standard support for NTSC-M, NTSCJAPAN,PAL (B, D, G, H, I, M, N,Combination N)@27M clock
- Support 480P, 576P@54M clock
- Support 720P,1080i@74.25M clock
- Support 1080P@148.5M clock
- Video input data port supports: CCIR-656 4:2:2 8-bit parallel input format
- Video output data port supports: 3 X10-bit DAC data output, Composite(CVBS) and Component S-video(Y/C) or Component YUV or RGB
- Support Wide-Screen Signaling (WSS)
- Analog signal output copyright protection
- Programmable 3 X DAC data path
- Plug status auto detecting

43.2. TV-OUT Signal Description

Table 43-1. TV-OUT Signal Description

Signal Name	Description	Type	Pin Name	Ball#
TV_DAC0	TV Analog Output(12bit DAC0)	AO	TV_DAC0	N15
TV_DAC1	TV Analog Output(12bit DAC1)	AO	TV_DAC1	N14
TV_DAC2	TV Analog Output(12bit DAC2)	AO	TV_DAC2	P15
TV_DAC3	TV Analog Output(12bit DAC3)	AO	TV_DAC3	P14