Allwinner A13 User Manual

V1.5

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Revision History

Version	Date	Description
V1.0	2012.04.16	Initial version
V1.1	2012.10.25	Modify SDRAM/NAND module descriptions
V1.2	2013.01.08	Modify NAND, USB DRD, SD/MMC
V1.3	2013.03.26	Modify Audio Codec register description
V1.4	2015.01.10	Modify Declaration description, Change document format
V1.5	2015.04.20	Add the programming guide of crypto engine

Declaration

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Technical Items

NO.	Abbreviation	Full Name	Description
1	ARM Cortex™-A8	ARM Cortex™-A8	A processor core designed by ARM Holdings implementing the ARM v7 instruction set architecture
2	Mali-400	Mali-400	A 2D/3D graphic processor unit designed by ARM Holdings
3	SDRAM	Synchronous Dynamic Random Access Memory	Dynamic random access memory (DRAM) that is synchronized with the system bus
4	PWM	Pulse Width Modulator	A commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches
5	SPI	Serial Peripheral Interface	A synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame
6	UART	Universal Asynchronous Receiver / Transmitter	Used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set
7	DMA	Direct Memory Access	A feature of modern computers that allow certain hardware subsystems within the computer to access system memory independently of the CPU
8	PWM	Pulse Width Modulation	A commonly used technique for controlling power to inertial electrical devices, made practical by modern electronic power switches
9	Audio Codec	Audio Codec	A computer program implementing an algorithm that compresses and decompresses digital audio data according to a given audio file format or streaming media audio format.
10	SD 3.0	Security Digital 3.0	A non-volatile memory card format developed by the SD Card Association for use in portable devices.
11	USB OTG	USB On-The-Go	It is Dual-role controller which supports both Host and device functions and is full compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a
12	EHCI	Enhanced Host Controller Interface	A high-speed controller standard that is publicly specified
13	OHCI	Open Host Controller Interface	A register-level interface that enables a host controller for USB or FireWire hardware to communicate with a host controller driver in software
14	TP	Touch Panel	A Human-Machine Interactive Interface
15	LRADC	Low Resolution Analog to Digital Converter	A module which can transfer analog signal to digital signal

16	CSI	CMOS Sensor Interface	The hardware block that interfaces with different image sensor interfaces and provides a standard output that can be used for subsequent image processing.

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Chapter 1 Overview

The A13 processor is an ARM Cortex-A8-based tablet processor that is even more competitive for Android tablets with higher performance (ManyCore Lite), lower power consumption, and lower total system cost. As the brains of Android 4.0.3, A13 makes multitasking smoother, apps loading more quickly, and anything you touch responds instantly. What's more important, A13 is available in eLQFP176 package with Audio Codec, and 2 Points R-TP integrated.

1.1. Features

CPU

- ARM Cortex™-A8 Core
- ARMv7 Instruction set plus Thumb-2 Instruction Set
- 32KB Instruction Cache and 32KB Data Cache
- 256KB L2 Cache
- NEON™ SIMD Coprocessor
- Jazelle RCT Acceleration

GPU

3D Graphic Engine

- Support Open GL ES 1.1/ 2.0 and Open VG 1.1

Video Engine

- Video Decoding (FULL HD)
  - Support multi-format video decoding, including VP6/8, AVS, H.264, H.263, MPEG-1/2/4, etc
  - Up to 1080p@30fps resolution in all formats
- Video Encoding
  - Support encoding in H.264 MP format
  - Up to 720p@30fps resolution

Display Processing Ability

- Four moveable and size-adjustable layers
- Support multi-format image input
- Support image enhancement processor
- Support Alpha blending /anti-flicker
- Support Hardware cursor
- Support output color correction (luminance / hue / saturation etc)

Display Output Ability

- LCD interface (CPU / Sync RGB)

Image Input Ability

- Support 8bit CMOS sensor parallel interface
- Support CCIR656 protocol for NTSC and PAL

Memory

- 16-bit SDRAM controller
  - Support DDR2 SDRAM and DDR3 SDRAM
  - Memory Capacity up to 512MB
- 8-bit NAND Flash Controller with 2 CE and 2 RB signals
  - Support SLC/MLC/TLC NAND
  - 64-bit ECC

External Peripherals

- One USB 2.0 OTG controller for general application and one USB EHCI/OHCI controller for host application
- Two High-speed memory controllers supporting SD version 2.0 and eMMC version 4.3
- Four UARTs(all with Infrared data Association[IrDA])
- Three SPI controllers(master/slave mode)
- Three Two-Wire Interfaces(TWI)
- IR controller supporting CIR remoter
- 6-bit LRADC for line control
- Internal 4-wire touch panel controller with pressure sensor and 2-point touch
- Internal 24-bit Audio Codec for 2-Ch headphone and 1-Ch microphone

- PWM controller

System Peripherals

- 8 channels normal DMA and 8 channels dedicated DMA
- Internal 48K SRAM on chip
- 6 asynchronic timers, 2 synchronic timers, 1 watchdog, and 2 AVS counters

Security System

- Crypto Engine
  - Support DES/3DES/AES encryption and decryption.
  - Support SHA-1, MD5 message digest
  - 160-bit hardware PRNG with 192-bit seed
- 128-bit EFUSE chip ID

Package

- eLQFP176 package

Chapter 2 Architecture

2.1. Functional Block Diagram

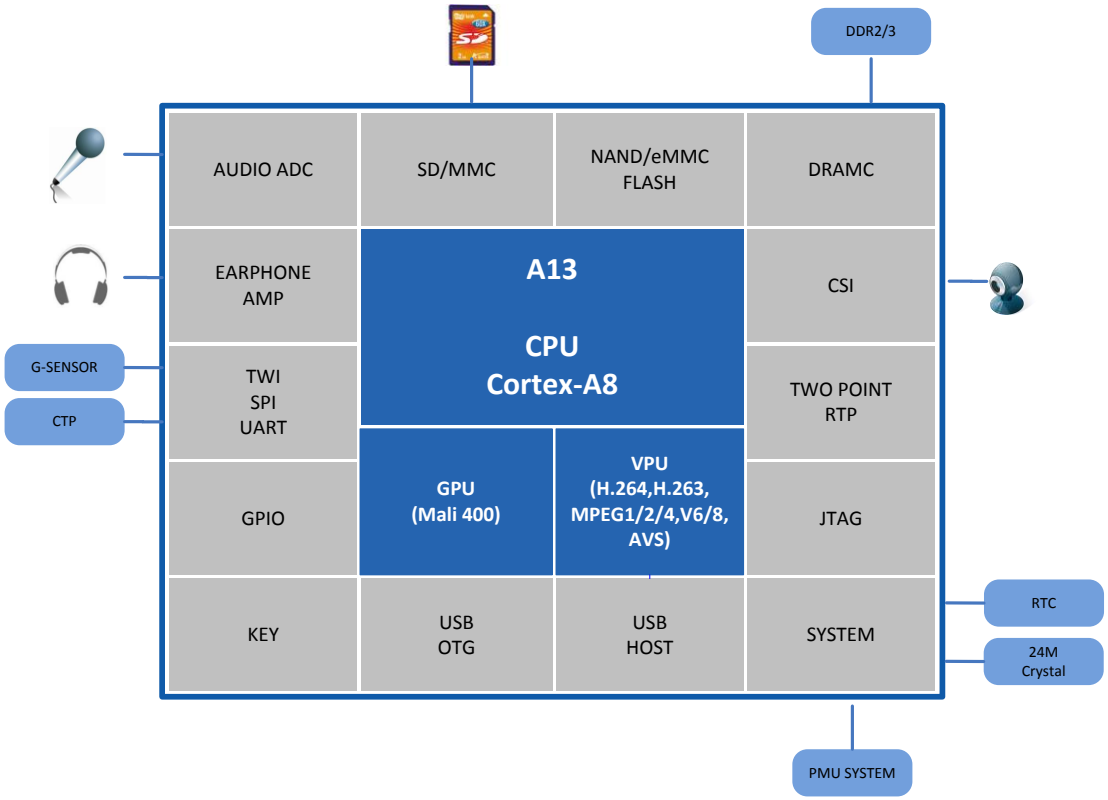


Figure2-1. A13 Block Diagram

2.2. Memory Mapping

Module	Address	Size(Bytes)
SRAM A1	0x0000 0000---0x0000 3FFF	16K
SRAM A2	0x0000 4000---0x0000 7FFF	16K
SRAM A3	0x0000 8000---0x0000 B3FF	13K
SRAM A4	0x0000 B400---0x0000 BFFF	3K
SRAM NAND	/	2K
SRAM D	0x0001 0000---0x0001 0FFF	4K
SRAM Controller	0x01C0 0000---0x01C0 0FFF	4K
DRAM Controller	0x01C0 1000---0x01C0 1FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
NFC	0x01C0 3000---0x01C0 3FFF	4K
/	0x01C0 4000---0x01C0 4FFF	4K
SPI 0	0x01C0 5000---0x01C0 5FFF	4K
SPI 1	0x01C0 6000---0x01C0 6FFF	4K
/	0x01C0 7000---0x01C0 7FFF	4K
/	0x01C0 8000---0x01C0 8FFF	4K
CSI	0x01C0 9000---0x01C0 9FFF	4K
/	0x01C0 A000---0x01C0 AFFF	/

EMAC	0x01C0 B000---0x01C0 BFFF	/
LCD	0x01C0 C000---0x01C0 CFFF	4K
/	0x01C0 D000---0x01C0 DFFF	4K
VE	0x01C0 E000---0x01C0 EFFF	4K
SD/MMC 0	0x01C0 F000---0x01C0 FFFF	4K
SD/MMC 1	0x01C1 0000---0x01C1 0FFF	4K
SD/MMC 2	0x01C1 1000---0x01C1 1FFF	4K
/	0x01C1 2000---0x01C1 2FFF	4K
USB OTG	0x01C1 3000---0x01C1 3FFF	4K
USB HCI	0x01C1 4000---0x01C1 4FFF	4K
CE	0x01C1 5000---0x01C1 5FFF	4K
/	0x01C1 6000---0x01C1 6FFF	/
SPI 2	0x01C1 7000---0x01C1 7FFF	4K
/	0x01C1 8000---0x01C1 8FFF	4K
/	0x01C1 9000---0x01C1 9FFF	4K
/	0x01C1 A000---0x01C1 AFFF	4K
/	0x01C1 B000---0x01C1 BFFF	4K
/	0x01C1 C000---0x01C1 CFFF	4K
/	0x01C1 D000---0x01C1 DFFF	4K
/	0x01C1 E000---0x01C1 EFFF	4K
/	0x01C1 F000---0x01C1 FFFF	4K
CCM	0x01C2 0000---0x01C2 03FF	1K
INTC	0x01C2 0400---0x01C2 07FF	1K
PIO	0x01C2 0800---0x01C2 0BFF	1K
Timer	0x01C2 0C00---0x01C2 0FFF	1K
/	0x01C2 1000---0x01C2 13FF	1K
/	0x01C2 1400---0x01C2 17FF	1K
IR	0x01C2 1800---0x01C2 1BFF	1K
/	0x01C2 1C00---0x01C2 1FFF	1K
/	0x01C2 2000---0x01C2 23FF	1K
IIS	0x01C2 2400---0x01C2 27FF	1K
LRADC	0x01C2 2800---0x01C2 2BFF	1K
Audio Codec	0x01C2 2C00---0x01C2 2FFF	1K
KEYPAD	0x01C2 3000---0x01C2 33FF	/
CPU Control	0x01C2 3400---0x01C2 37FF	1K
SID	0x01C2 3800---0x01C2 3BFF	1K
/	0x01C2 3C00---0x01C2 3FFF	1K
/	0x01C2 4000---0x01C2 43FF	1K
/	0x01C2 4400---0x01C2 47FF	1K
/	0x01C2 4800---0x01C2 4BFF	1K
/	0x01C2 4C00---0x01C2 4FFF	1K
TP	0x01C2 5000---0x01C2 53FF	1K
PMU	0x01C2 5400---0x01C2 57FF	1K
/	0x01C2 5800---0x01C2 5BFF	1K
/	0x01C2 5C00---0x01C2 5FFF	1K
/	0x01C2 6000---0x01C2 63FF	1K
/	0x01C2 6400---0x01C2 67FF	1K
/	0x01C2 6800---0x01C2 6BFF	1K
/	0x01C2 6C00---0x01C2 6FFF	1K
/	0x01C2 7000---0x01C2 73FF	1K
/	0x01C2 7400---0x01C2 77FF	1K
/	0x01C2 7800---0x01C2 7BFF	1K
/	0x01C2 7C00---0x01C2 7FFF	1K
UART 0	0x01C2 8000---0x01C2 83FF	1K
UART 1	0x01C2 8400---0x01C2 87FF	1K

UART 2	0x01C2 8800---0x01C2 8BFF	1K
UART 3	0x01C2 8C00---0x01C2 8FFF	1K
/	0x01C2 9000---0x01C2 93FF	1K
/	0x01C2 9400---0x01C2 97FF	1K
/	0x01C2 9800---0x01C2 9BFF	1K
/	0x01C2 9C00---0x01C2 9FFF	1K
/	0x01C2 A000---0x01C2 A3FF	1K
/	0x01C2 A300---0x01C2 A7FF	1K
/	0x01C2 A800---0x01C2 ABFF	1K
TWI 0	0x01C2 AC00---0x01C2 AFFF	1K
TWI 1	0x01C2 B000---0x01C2 B3FF	1K
/	0x01C2 B400---0x01C2 B7FF	1K
/	0x01C2 B800---0x01C2 BBFF	1K
/	0x01C2 BC00---0x01C2 BFFF	1K
/	0x01C2 C000---0x01C2 C3FF	1K
/	0x01C2 C400---0x01C2 C7FF	1K
/	0x01C2 C800---0x01C2 CBFF	1K
/	0x01C2 CC00---0x01C2 CFFF	1K
/	0x01C3 0000---0x01C3 FFFF	64K
Mali-400	0x01C4 0000---0x01C4 FFFF	64K
Sync Timer	0x01C6 0000—0x01C6 0FFF	4K
SRAM C	0x01D0 0000---0x01DF FFFF	Module SRAM
DE_FE	0x01E0 0000---0x01E1 FFFF	128K
/	0x01E2 0000---0x01E3 FFFF	128K
DE_BE	0x01E6 0000---0x01E6 FFFF	64K
IEP	0x01E7 0000---0x01E7 FFFF	64K
/	0x01E4 0000---0x01E5 FFFF	128K
/	0x01E8 0000---0x01E9 FFFF	128K
/	0x01EA 0000---0x01EB FFFF	128K
/	0x3F50 0000---0x3F50 FFFF	64K
DDR-II/DDR-III	0x4000 0000---0xBFFF FFFF	2G
BROM	0xFFFF 0000—0xFFFF 7FFF	32K

Chapter 3 Boot System

3.1. Overview

With one 32KB ROM, the A13 supports five boot methods. The system can boot sequencially from NAND Flash, SPI NOR Flash, SD Card and USB. However, if the external boot select pin(BSP), which is pulled up by an internal 50K resistor in normal state, is checked by boot code to be on low-level state after system power-on, the system will directly jump to boot from USB.

3.2. Boot Diagram

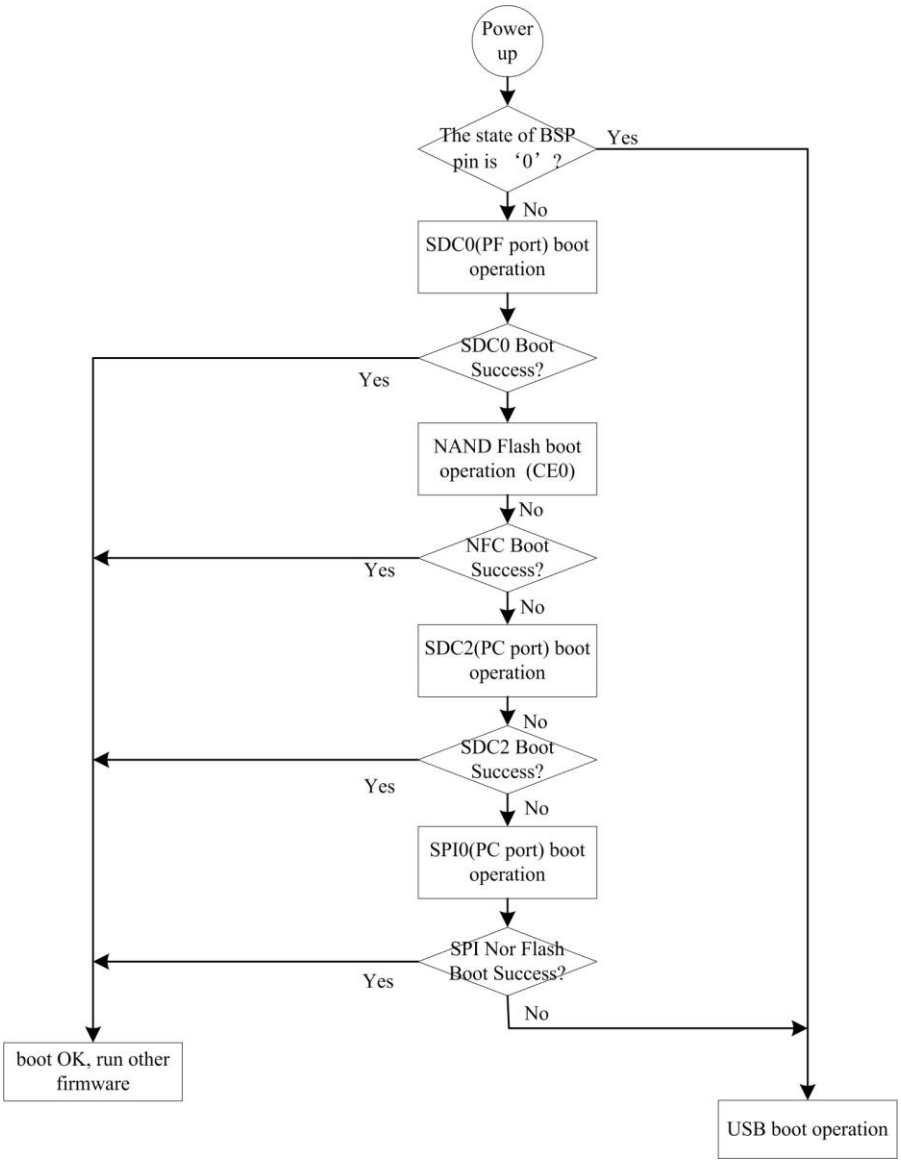


Figure 3-1. Boot Diagram

Chapter 4 PMU

4.1. Overview

The Power Management Unit (PMU) aims to reduce dynamic power consumption and static leakage current to extend the life of batteries in end products. This module is the central control module for CPU clock and power management signals in the device.

4.2. PMU Register List

Module Name	Base Address
PMU	0x01C25400

Register Name	Offset	Description
PMU_DVFS_CTRL_REG0	0x0000	PMU Control Register 0
PMU_DVFS_CTRL_REG1	0x0004	PMU Control Register 1
/	0x0008	/
PMU_DVFS_CTRL_REG2	0x000C	PMU Control Register 2
/	0x0010	/
/	0x0014	/
PMU_DVFS_CTRL_REG3	0x0018	PMU Control Register 3
PMU_DVFS_TIMEOUT_CTRL_REG	0x001C	PMU Timeout Control Register
PMU_AXI_AUTO_SWT_REG0	0x0020	PMU AXI Auto Switch CLK Register0
PMU_AXI_AUTO_SWT_REG1	0x0024	PMU AXI Auto Switch CLK Register1
PMU_IRQ_EN_REG	0x0040	PMU IRQ Enable Register
PMU_IRQ_STATUS_REG	0x0044	PMU IRQ Status Register
PMU_STATUS_REG	0x0048	PMU Status Register
PMU_CPUVDD_CTRL_REG_ADDR	0x004C	PMU CPUVDD Register Address
PMU_TWI_ADDR_REG	0x0050	PMU TWI Address
PMU_CPUVDD_VALUE_REG	0x0054	PMU Cpuvdd Value
PMU_CPUVDD_RAMP_CTRL_REG	0x0058	PMU CPUVDD Voltage Ramp Control
PMU_32KHZ_CPUVDD_MIN_REG	0x005C	PMU 32khz CPUVDD Minimum Value
PMU_VF_TABLE_REG0	0x0080	CPU speed max if the vddcpu=0.70v
PMU_VF_TABLE_REG1	0x0084	CPU speed max if the vddcpu=0.75v
PMU_VF_TABLE_REG2	0x0088	CPU speed max if the vddcpu=0.80v
PMU_VF_TABLE_REG3	0x008C	CPU speed max if the vddcpu=0.85v
PMU_VF_TABLE_REG4	0x0090	CPU speed max if the vddcpu=0.90v
PMU_VF_TABLE_REG5	0x0094	CPU speed max if the vddcpu=0.95v
PMU_VF_TABLE_REG6	0x0098	CPU speed max if the vddcpu=1.00v
PMU_VF_TABLE_REG7	0x009C	CPU speed max if the vddcpu=1.05v
PMU_VF_TABLE_REG8	0x00A0	CPU speed max if the vddcpu=1.10v
PMU_VF_TABLE_REG9	0x00A4	CPU speed max if the vddcpu=1.15v
PMU_VF_TABLE_REG10	0x00A8	CPU speed max if the vddcpu=1.20v
PMU_VF_TABLE_REG11	0x00AC	CPU speed max if the vddcpu=1.25v
PMU_VF_TABLE_REG12	0x00B0	CPU speed max if the vddcpu=1.30v
PMU_VF_TABLE_REG13	0x00B4	CPU speed max if the vddcpu=1.35v

PMU_VF_TABLE_REG14	0x00B8	CPU speed max if the vddcpu=1.40v
PMU_VF_TABLE_REG15	0x00BC	CPU speed max if the vddcpu=1.45v
PMU_VF_TABLE_REG16	0x00C0	CPU speed max if the vddcpu=1.50v
PMU_VF_TABLE_REG17	0x00C4	CPU speed max if the vddcpu=1.55v
PMU_VF_TABLE_REG18	0x00C8	CPU speed max if the vddcpu=1.60v
PMU_VF_TABLE_VALID_REG	0x00CC	PMU Vf Table Valid Control
PMU_VF_TABLE_INDEX_REG	0x00D0	PMU Vf Table Index
PMU_VF_TABLE_RANGE_REG	0x00D4	PMU Vf Table Range
PMU_SPEED_FACTOR_REG0	0x00E0	PMU Speed Factor Register 0
PMU_SPEED_FACTOR_REG1	0x00E4	PMU Speed Factor Register 1
PMU_SPEED_FACTOR_REG2	0x00E8	PMU Speed Factor Register 2
CPU_IDLE_CNT_LOW_REG	0x00F0	CPU Idle Counter Low
CPU_IDLE_CNT_HIGH_REG	0x00F4	CPU Idle Counter High
CPU_IDLE_COUNTER_CTRL_REG	0x00F8	CPU Idle Counter Control
CPU_IDLE_STATUS_REG	0x00FC	CPU Idle Status Register

4.3. PMU Register Description

4.3.1. PMU DVFS Control Register 0 (Default: 0x00000000)

Offset: 0x00			Register Name: PMU_DVFS_CTRL_REG0
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x0	DVFS_MODE_SEL. DVFS Mode Select. 00: mode 0 01: mode 1 10: mode 2 11: /.
15	R/W	0x0	AXI_DIV_AUTO_SWITCH. AXICLK auto switch enable. 0: Disable, 1: Enable.
14:13	/	/	/
12	R/W	0x0	VOLT_CHANGE_MODE. Voltage Change Mode 0: normal mode 1: maximum mode
11:9	/	/	/
8	R/W	0x0	CLK_CHANGE_SM_MODE. Clock Change Smooth Mode 0: Divide mode 1: Gating mode.
7	R/W	0x0	SM_EN. Smooth enable. 0: Disable, 1: Enable.
6	R/W	0x0	CLK_SWTH_EN. Clock switch enable. 0: Disable, 1: Enable.
5	R/W	0x0	VOLT_CHANGE_EN. Voltage change enable. 0: Disable, 1: Enable.
4	R/W	0x0	SPD_DET_EN. Speed detect enable. 0: Disable, 1: Enable.

3:1	/	/	/
0	R/W	0x0	DVFS_EN. PMU DVFS Enable. 0: Disable 1: Enable.

4.3.2. PMU DVFS Control Register 1(Default: 0x00001010)

Offset: 0x04			Register Name: PMU_DVFS_CTRL_REG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:8	R/W	0x10	PLL_STAB_TIME PLL stable time.
7:0	R/W	0x10	SM_INTV_VALUE Smooth interval value

4.3.3. PMU DVFS Control Register 2 (Default: 0x00000000)

Offset: 0x0C			Register Name: PMU_DVFS_CTRL_REG2
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	VOLT_SET_EN. Voltage Set Enable. It will be auto cleared after the voltage setting command is sent successfully. Set this bit to 1 will start the voltage setting (set the CPUVDD register value to the external PMU IC through the TWI interface).

Note: This bit can not be set to one if the VoltageChangeEnable bit in the DVFS Ctrl register 0 is set to 1.

4.3.4. PMU AXI Clock Range Register0 (Default: 0x00000000)

Offset: 0x20			Register Name: PMU_AXI_AUTO_SWT_REG0
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0x0	AXI_CLK_LEVEL1 AXICLK level 1
15:11	/	/	/
10:0	R/W	0x0	AXI_CLK_LEVEL0 AXICLK level 0

4.3.5. PMU AXI Clock Range Register1 (Default: 0x00000000)

Offset: 0x24			Register Name: PMU_AXI_AUTO_SWT_REG1
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0x0	AXI_CLK_LEVE3 AXICLK level 3
15:11	/	/	/
10:0	R/W	0x0	AXI_CLK_LEVEL2 AXICLK level 2

4.3.6. PMU DVFS Control Register 3

Offset: 0x18			Register Name: PMU_DVFS_CTRL_REG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

4.3.7. PMU DVFS TimeOut Control Register(Default: 0x00000027)

Offset: 0x1C			Register Name: PMU_DVFS_TIMEOUT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0x27	DVFS_TIMEOUT. DVFS operate on TWI timeout cycles in TWI peripheral clock. 0: 1 cycle …… 0x27: 40 cycles …… 0x3F: 64 cycles

4.3.8. PMU IRQ En Register (Default: 0x00000000)

Offset: 0x40			Register Name: PMU_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VOLT_DET_ERR_IRQ_EN. Voltage Detect Error IRQ Enable. 0: Disable 1: Enable.
11	R/W	0x0	DVFS_CLK_SWTH_ERR_IRQ_EN. DVFS Clock Switch Operation Error IRQ Enable. 0: Disable 1: Enable.
10	R/W	0x0	DVFS_VOLT_CHANGE_ERR_EN. DVFS Voltage Change Error Enable. 0: Disable, 1: Enable.
9	R/W	0x0	DVFS_SPD_DET_ERR_IRQ_EN. DVFS Speed Detect Error IRQ Enable. 0: Disable 1: Enable.
8:5	/	/	/
4	R/W	0x0	VOLT_DET_FIN_IRQ_EN. Voltage Detect Finished IRQ Enable. 0: Disable 1: Enable.
3	R/W	0x0	DVFS_CLK_SWT_FIN_IRQ_EN. DVFS Clock Switch Operation Finished IRQ Enable. 0: Disable 1: Enable.
2	R/W	0x0	DVFS_VOLT_CHANGE_FIN_EN. DVFS Voltage Change Finished Enable. 0: Disable, 1: Enable.
1	R/W	0x0	DVFS_SPD_DET_FIN_IRQ_EN. DVFS Speed Detect Finished IRQ Enable. 0: Disable,

			1: Enable.
0	R/W	0x0	DVFS_FIN_IRQ_EN. DVFS Finished IRQ Enable. 0: Disable 1: Enable.

4.3.9. PMU IRQ Status Register (Default: 0x00000000)

Offset: 0x44			Register Name: PMU_IRQ_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	VOLT_DET_ERR_IRQ_PEND. Voltage Detect Error IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it...
11	R/W	0x0	DVFS_CLK_SWT_ERR_IRQ_PEND. DVFS Clock Switch Operation Error IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
10	R/W	0x0	DVFS_VOLT_CHANGE_ERR_PEND. DVFS Voltage Change Error Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
9	R/W	0x0	DVFS_SPD_DET_ERR_IRQ_PEND. DVFS Speed Detect Error IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
8:5	/	/	/
4	R/W	0x0	VOLT_DET_FIN_IRQ_PEND. Voltage Detect Finished IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
3	R/W	0x0	DVFS_CLK_SWT_FIN_IRQ_PEND. DVFS Clock Switch Operation Finished IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
2	R/W	0x0	DVFS_VOLT_CHANGE_FIN_PEND. DVFS Voltage Change Finished Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
1	R/W	0x0	DVFS_SPD_DET_FIN_IRQ_PEND. DVFS Speed Detect Finished IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.
0	R/W	0x0	DVFS_FIN_IRQ_PEND. DVFS Finished IRQ Pending. 0: No effect, 1: Pending. Set one to this bit will clear it.

4.3.10. PMU Status Register (Default: 0x00000000)

Offset: 0x48			Register Name: PMU_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DVFS_BUSY.

			DVFS Busy. 0: no effect 1: DVFS is busy.

4.3.11. PMU CPUVDD DCDC Control Register Address(Default: 0x00000023)

Offset: 0x4C			Register Name: PMU_CPUVDD_CTRL_REG_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.
7:0	R/W	0x23	CPUVDD_CTRL_REG_ADDR. PMU CPUVDD DCDC Control Register address.

4.3.12. PMU TWI Address(Default: 0x00000068)

Offset: 0x50			Register Name: PMU_TWI_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.
7:0	R/W	0x68	PMU_TWI_ADDR. PMU TWI address set.

4.3.13. PMU CPUVDD Value(Default: 0x00000016)

Offset: 0x54			Register Name: PMU_CPUVDD_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.
7:0	R/W	0x16	CPUVDD_DEFAULT. PMU CPUVDD Default Value 0x00 = 0.70v 0x02 = 0.75v 0x04 = 0.80v 0x06 = 0.85v 0x08 = 0.90v 0x0A = 0.95v 0x0C = 1.00v 0x0E = 1.05v 0x10 = 1.10v 0x12 = 1.15v 0x14 = 1.20v 0x16 = 1.25v 0x18 = 1.30v 0x1A = 1.35v 0x1C = 1.40v 0x1E = 1.45v 0x20 = 1.50v 0x22 = 1.55v 0x24 = 1.60v

Note: This register can be modified by PMU DVFS.

4.3.14. PMU CPUVDD Voltage Ramp Control in DVM (Default: 0x00000000)

Offset: 0x58			Register Name: PMU_CPUVDD_RAMP_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/.
0	R/W	0x0	CPUVDD_VOLT_RAMP_CTRL.

			CPUvdd voltage ramp control in DVM 0 = 15.625us 1 = 31.25us

Note: If the cpuvdd voltage ramp control in the external PMU is changed by the CPU, the CPU should also modify this to be the same in the PMU.

4.3.15. PMU 32KHz CPUVDD Minimum Value(Default: 0x0000000C)

Offset: 0x5C			Register Name: PMU_32KHZ_CPUVDD_MIN_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/.
7:0	R/W	0xc	CPUVDD_32KHZ_MIN_VALUE. PMU CPUVDD Default Value 0x00 = 0.70v 0x02 = 0.75v 0x04 = 0.80v 0x06 = 0.85v 0x08 = 0.90v 0x0A = 0.95v 0x0C = 1.00v 0x0E = 1.05v 0x10 = 1.10v 0x12 = 1.15v 0x14 = 1.20v 0x16 = 1.25v 0x18 = 1.30v 0x1A = 1.35v 0x1C = 1.40v 0x1E = 1.45v 0x20 = 1.50v 0x22 = 1.55v 0x24 = 1.60v

4.3.16. PMU VF Table Register 0

Offset: 0x80			Register Name: PMU_VF_TABLE_REG0
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_070. CPU max frequency if cpuvdd=0.7v (unit: MHz) This register can only be written if the DVFS function is disabled.

4.3.17. PMU VF Table Register 1

Offset: 0x84			Register Name: PMU_VF_TABLE_REG1
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_075. CPU max frequency if cpuvdd=0.75v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.18. PMU VF Table Register 2

Offset: 0x88			Register Name: PMU_VF_TABLE_REG2
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

10:0	R/W	x	CPU_MAX_FREQ_080. CPU max frequency if cpuvdd=0.8v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.19. PMU VF Table Register 3

Offset: 0x8C			Register Name: PMU_VF_TABLE_REG3
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_085. CPU max frequency if cpuvdd=0.85v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.20. PMU VF Table Register 4

Offset: 0x90			Register Name: PMU_VF_TABLE_REG4
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_090. CPU max frequency if vddcpu=0.9v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.21. PMU VF Table Register 5

Offset: 0x94			Register Name: PMU_VF_TABLE_REG5
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_095. CPU max frequency if cpuvdd=0.95v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.22. PMU VF Table Register 6

Offset: 0x98			Register Name: PMU_VF_TABLE_REG6
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_100. CPU max frequency if cpuvdd=1.0v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.23. PMU VF Table Register 7

Offset: 0x9C			Register Name: PMU_VF_TABLE_REG7
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_105. CPU max frequency if cpuvdd=1.05v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.24. PMU VF Table Register 8

Offset: 0xA0			Register Name: PMU_VF_TABLE_REG8
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/

10:0	R/W	x	CPU_MAX_FREQ_110. CPU max frequency if cpuvdd=1.1v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.25. PMU VF Table Register 9

Offset: 0xA4			Register Name: PMU_VF_TABLE_REG9
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_115. CPU max frequency if cpuvdd=1.15v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.26. PMU VF Table Register 10

Offset: 0xA8			Register Name: PMU_VF_TABLE_REG10
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_120. CPU max frequency if cpuvdd=1.2v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.27. PMU VF Table Register 11

Offset: 0xAC			Register Name: PMU_VF_TABLE_REG11
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_125. CPU max frequency if cpuvdd=1.25v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.28. PMU VF Table Register 12

Offset: 0xB0			Register Name: PMU_VF_TABLE_REG12
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_130. CPU max frequency if cpuvdd=1.3v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.29. PMU VF Table Register 13

Offset: 0xB4			Register Name: PMU_VF_TABLE_REG13
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/.
10:0	R/W	x	CPU_MAX_FREQ_135. CPU max frequency if cpuvdd=1.35v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.30. PMU VF Table Register 14

Offset: 0xB8			Register Name: PMU_VF_TABLE_REG14
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/.

10:0	R/W	x	CPU_MAX_FREQ_140. CPU max frequency if cpuvdd=1.4v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.31. PMU VF Table Register 15

Offset: 0xBC			Register Name: PMU_VF_TABLE_REG15
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/.
10:0	R/W	x	CPU_MAX_FREQ_145. CPU max frequency if cpuvdd=1.45v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.32. PMU VF Table Register 16

Offset: 0xC0			Register Name: PMU_VF_TABLE_REG16
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_150. CPU max frequency if cpuvdd=1.5v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.33. PMU VF Table Register 17

Offset: 0xC4			Register Name: PMU_VF_TABLE_REG17
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_155. CPU max frequency if cpuvdd=1.55v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.34. PMU VF Table Register 18

Offset: 0xC8			Register Name: PMU_VF_TABLE_REG18
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10:0	R/W	x	CPU_MAX_FREQ_160. CPU max frequency if cpuvdd=1.6v (unit: MHz). This register can only be written if the DVFS function is disabled.

4.3.35. PMU VF Table Valid Register (Default: 0x0000003C)

Offset: 0xCC			Register Name: PMU_VF_TABLE_VALID_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0x0	/
15:6	/	/	/
5	R/W	0x1	VF_TABLE_18_VALID. PMU V-F Table Register 18 valid. 0: valid, 1: invalid.
4	R/W	0x1	VF_TABLE_17_VALID. PMU V-F Table Register 17 valid. 0: valid 1: invalid

3	R/W	0x1	VF_TABLE_16_VALID. PMU V-F Table Register 16 valid. 0: valid 1: invalid
2	R/W	0x1	VF_TABLE_15_VALID. PMU V-F Table Register 15 valid. 0: valid 1: invalid
1	R/W	0x0	VF_TABLE_14_VALID. PMU V-F Table Register 14 valid. 0: valid 1: invalid
0	R/W	0x0	VF_TABLE_13_VALID. PMU V-F Table Register 13 valid. 0: valid 1: invalid

4.3.36. PMU VF Table Index Register (Default: 0x00000000)

Offset: 0xD0			Register Name: PMU_VF_TABLE_INDEX_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	VF_TABLE_IDX. PMU V-F Table Index. 00: 01 10 11

4.3.37. PMU VF Table Range Register (Default: 0x00000000)

Offset: 0xD4			Register Name: PMU_VF_TABLE_RANGE_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	VF_TABLE_RNG2. PMU V-F Table Range 2.
15:8	R/W	0x0	VF_TABLE_RNG1. PMU V-F Table Range 1.
7:0	R/W	0x0	VF_TABLE_RNG0. PMU V-F Table Range 0.

4.3.38. PMU Speed Factor Register 0 (Default: 0x00000000)

Offset: 0xE0			Register Name: PMU_SPEED_FACTOR_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPD_DET_EN. Speed Detect Enable. 0: Disable, 1: Enable
30	R/W	0x0	SPD_DET_MODE. Speed Detect Mode. 0: single mode 1: continuous mode
29:28	R/W	0x0	SPD_DET_SPDUP_FACTOR. Speed Detect Speed Up Factor

			Set these bits to non-zero value can speed up the scan operation 00: lowest … 11: fastest
27:17	/	/	/
16	R	0x0	SPD_DET_SCN_FIN. Speed Detect Scan Finished 0: no effect, 1: scan finished.
15:8	R	0x0	SPD_DET_FACTOR1 Speed Detect Factor 1 This number indicates the delay length equivalent to input clock period x2
7:0	R	0x0	SPD_DET_FACTOR0. Speed Detect Factor 0 This number indicates the delay length equivalent to input clock period x1

4.3.39. PMU Speed Factor Register 1 (Default: 0x00000000)

Offset: 0xE4			Register Name: PMU_SPEED_FACTOR_REG1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPD_DET_EN. Speed Detect Enable. 0: Disable, 1: Enable
30	R/W	0x0	SPD_DET_MODE. Speed Detect Mode. 0: single mode 1: continuous mode
29:28	R/W	0x0	SPD_DET_SPDUP_FACTOR Speed Detect Speed Up Factor Set these bits to non-zero value can speed up the scan operation 00: lowest … 11: fastest
27:17	/	/	/
16	R	0x0	SPD_DET_SCN_FIN Speed Detect Scan Finished 0: no effect, 1: scan finished.
15:8	R	0x0	SPD_DET_FACTOR1. Speed Detect Factor 1 This number indicates the delay length equivalent to input clock period x2
7:0	R	0x0	SPD_DET_FACTOR0. Speed Detect Factor 0 This number indicates the delay length equivalent to input clock period x1

4.3.40. PMU Speed Factor Register 2 (Default: 0x00000000)

Offset: 0xE8			Register Name: PMU_SPEED_FACTOR_REG2
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SPD_DET_EN.

			Speed Detect Enable. 0: Disable, 1: Enable
30	R/W	0x0	SPD_DET_MODE. Speed Detect Mode. 0: single mode 1: continuous mode
29:28	R/W	0x0	SPD_DET_SPDUP_FACTOR Speed Detect Speed Up Factor Set these bits to non-zero value can speed up the scan operation 00: lowest … 11: fastest
27:17	/	/	/
16	R	0x0	SPD_DET_SCN_FIN Speed Detect Scan Finished 0: no effect, 1: scan finished.
15:8	R	0x0	SPD_DET_FACTOR1. Speed Detect Factor 1 This number indicates the delay length equivalent to input clock period x2
7:0	R	0x0	SPD_DET_FACTOR0 Speed Detect Factor 0 This number indicates the delay length equivalent to input clock period x1

4.3.41. CPU Idle Counter Low Register (Default: 0x00000000)

Offset: 0XF0			Register Name: CPU_IDLE_CNT_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CPU_IDLE_CNT_LO CPU Idle Counter [31:0]. This counter clock source is 24MHz. If CPU is in idle state, the counter will count up in the clock of 24MHz. Any write to this register will clear this register and the CPU idle counter high register.

4.3.42. CPU Idle Counter High Register (Default: 0x00000000)

Offset: 0xF4			Register Name: CPU_IDLE_CNT_HIGH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CPU_IDLE_CNT_HI. CPU Idle Counter [63:32]. Any write to this register will clear this register and the CPU idle counter low register.

4.3.43. CPU Idle Control Register (Default: 0x00000000)

Offset: 0xF8			Register Name: CPU_IDLE_COUNTER_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	CPU_IDLE_AUTO_SWTH_EN. CPU idle enter/exit, clk auto switch enable. 0: disable, 1: enable.

			If the CPU enter the idle mode and this bit is set, the ccu will auto switch the CPU clock divide ratio to /8. If the CPU exit the idle mode and this bit is set, the ccu will auto switch the CPU clock divide ratio from /8 to /1 with 4 steps.
6:3	/	/	/
2	R/W	0x0	CPU_IDLE_CNT_EN. CPU idle counter enable. 0: disable 1: enable.
1	R/W	0x0	CPU_IDLE_RL_EN. CPU idle Counter Read Latch Enable. 0: no effect, 1: to latch the idle Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	CPU_IDLE_CNT_CLR_EN. CPU idle Counter Clear Enable. 0: no effect, 1: to clear the idle Counter Low/Hi registers and it will change to zero after the registers are cleared.

4.3.44. CPU Idle Status Register (Default: 0x00000000)

Offset: 0xFC			Register Name: CPU_IDLE_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	CPU_IDLE_STA. CPU idle exit finished pending. 0: no effect, 1: idle exit finished. Set 1 to this bit will clear it.

Chapter 5 Clock Control Module (CCM)

5.1. Overview

The Clock Control Module (CCM) is made up of 7 PLLs, a Main Oscillator and an on-chip RC Oscillator. The 24-MHz crystal is mandatory and to generate input clock source for PLLs and main digital blocks.

In order to provide high performance, low-power consumption and user-friendly interfaces, the chip includes several clock domains: CPU clock, AHB clock, APB clock and special clock. See details in the following table.

CLK Domain	Module	Speed Range	Description
OSC24M	Most Clock Generator	24MHz	Root clock for most of the chip
RC_OSC	Timer,key	32KHz	Source for the timer
CPU32_clk	CPU32	2K~1200M	Divided from CPU32_clk or OSC24M
AHB_clk	AHB Devices	8K~276M	Divided from CPU32_clk
APB_clk	Peripheral	0.5K~138M	Divided from AHB_clk
SDRAM_clk	SDRAM	0~400MHz	Sourced from the PLL
USB_clk	USB	480MHz	Sourced from the PLL
Audio_clk	A/D,D/A	24.576MHz /22.5792MHz	Sourced from the PLL

5.2. Clock Tree Diagram

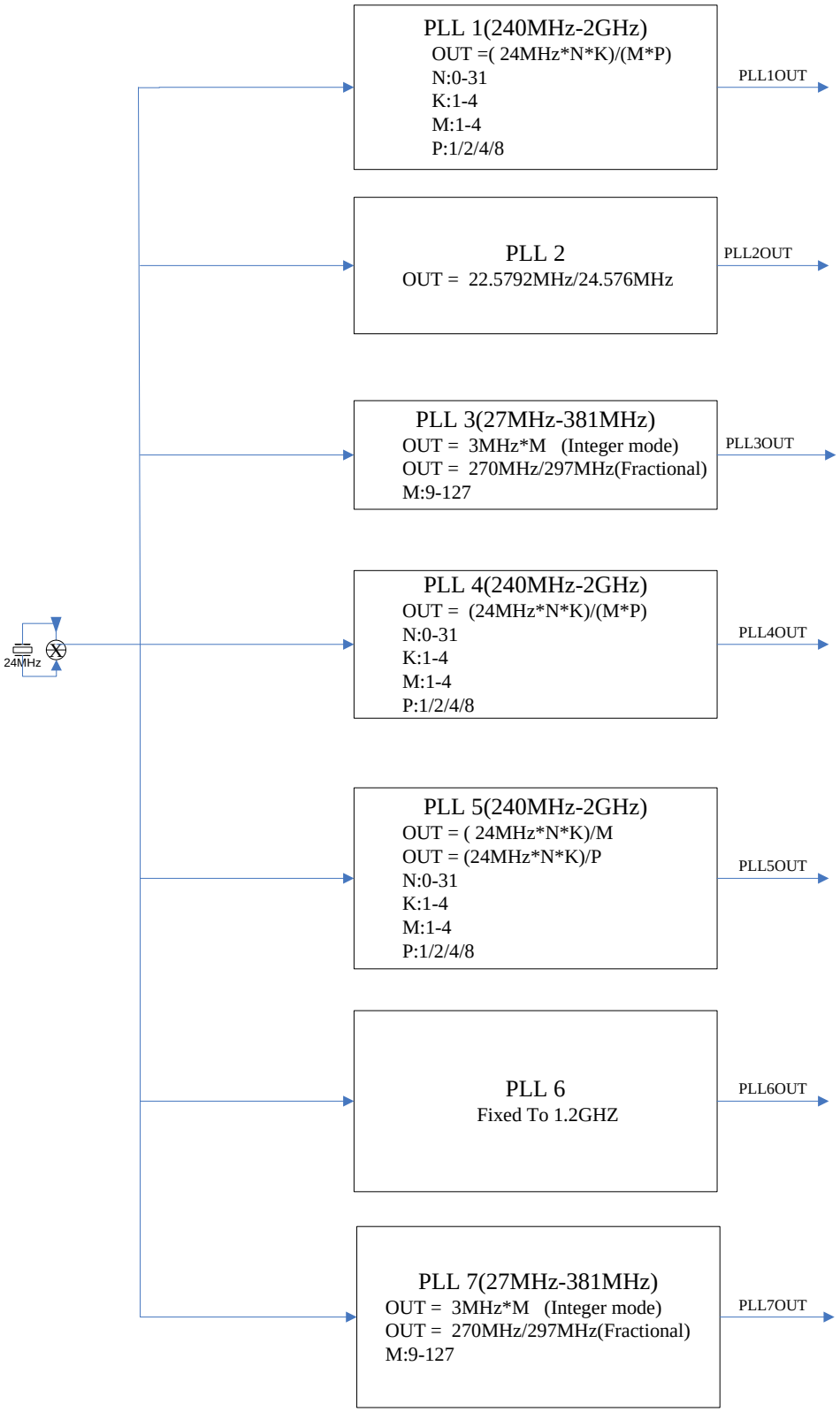


Figure 5-1. Clock Generation from PLL Outputs

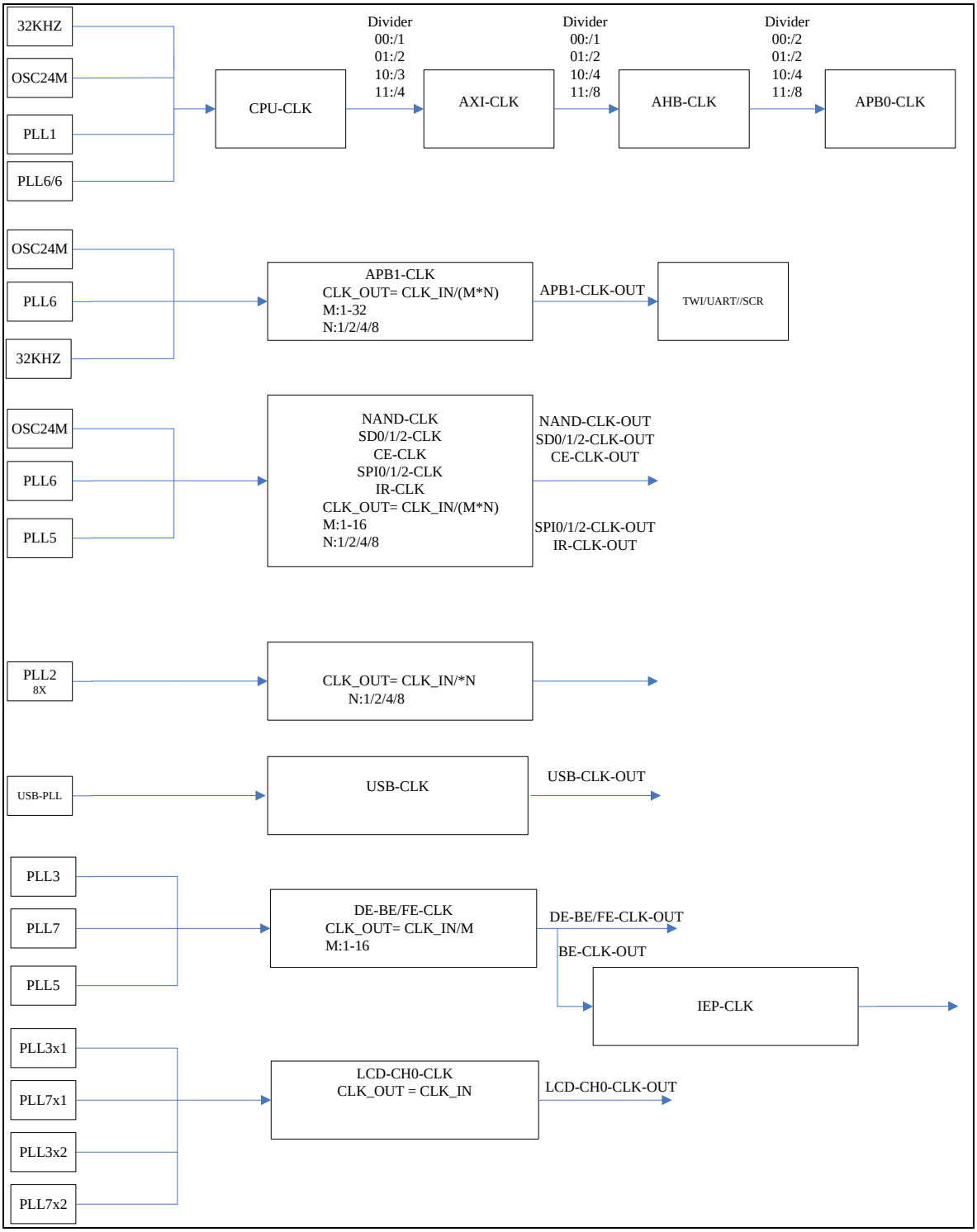


Figure 5-2. Bus Clock Generation Part 1

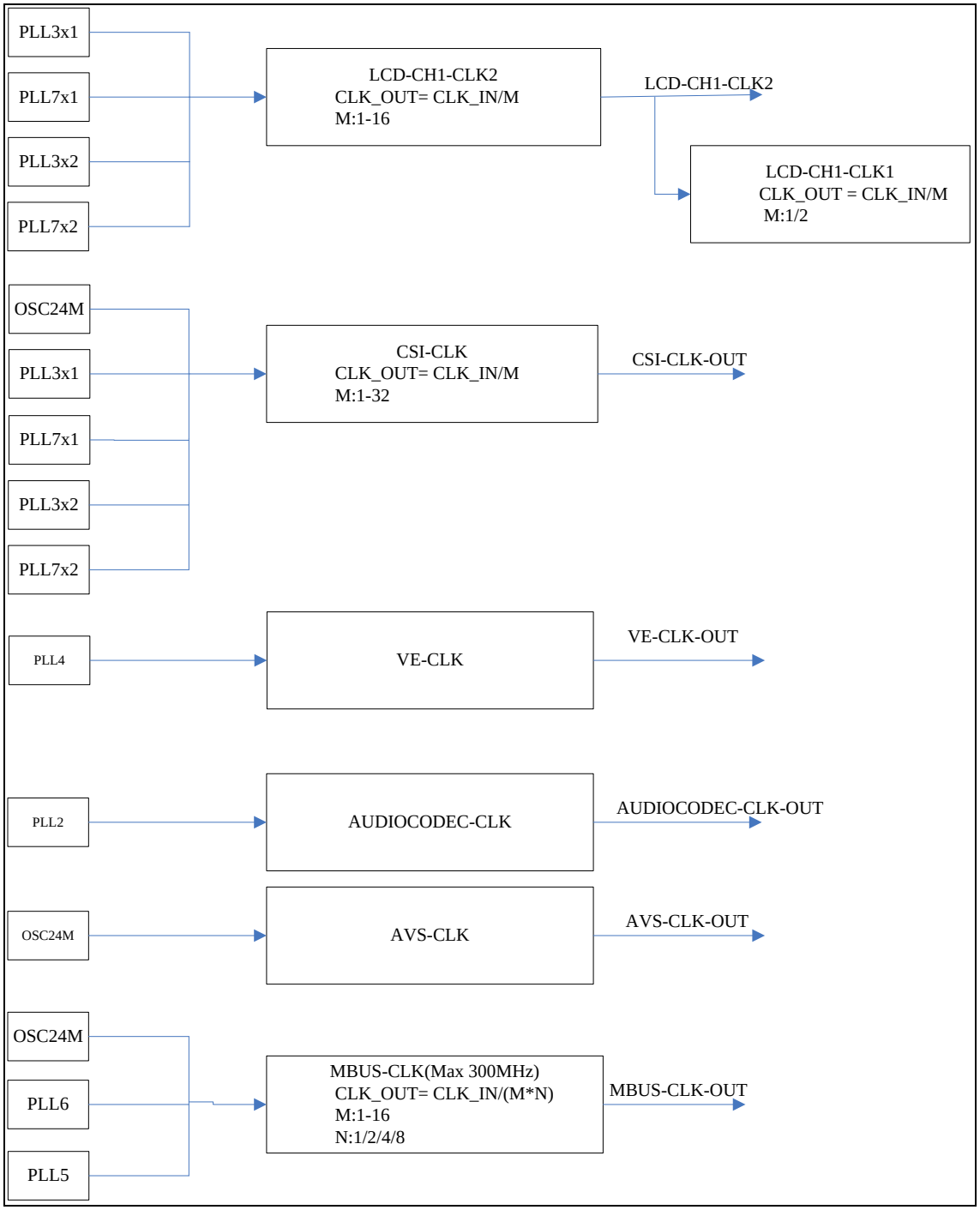


Figure 5-3. Bus Clock Generation Part 2

5.3. CCM Register List

Module Name	Base Address
CCM	0x01C20000

Register Name	Offset	Description
PLL1_CFG_REG	0x0000	PLL1 Control
PLL1_TUN_REG	0x0004	PLL1 Tuning
PLL2_CFG_REG	0x0008	PLL2 Control

PLL2_TUN_REG	0x000C	PLL2 Tuning
PLL3_CFG_REG	0x0010	PLL3 Control
/	0x0014	/
PLL4_CFG_REG	0x0018	PLL4 Control
/	0x001C	/
PLL5_CFG_REG	0x0020	PLL5 Control
PLL5_TUN_REG	0x0024	PLL5 Tuning
PLL6_CFG_REG	0x0028	PLL6 Control
/	0x002C	PLL6 Tuning
PLL7_CFG_REG	0x0030	/
/	0x0034	/
PLL1_TUN2_REG	0x0038	PLL1 Tuning2
PLL5_TUN2_REG	0x003C	PLL5 Tuning2
/	0x004C	/
OSC24M_CFG_REG	0x0050	OSC24M control
CPU_AHB_APB0_CFG_REG	0x0054	CPU, AHB And APB0 Divide Ratio
APB1_CLK_DIV_REG	0x0058	APB1 Clock Divider
AXI_GATING_REG	0x005C	AXI Module Clock Gating
AHB_GATING_REG0	0x0060	AHB Module Clock Gating 0
AHB_GATING_REG1	0x0064	AHB Module Clock Gating 1
APB0_GATING_REG	0x0068	APB0 Module Clock Gating
APB1_GATING_REG	0x006C	APB1 Module Clock Gating
NAND_SCLK_CFG_REG	0x0080	Nand Flash Clock
/	0x0084	/
SD0_SCLK_CFG_REG	0x0088	SD0 Clock
SD1_SCLK_CFG_REG	0x008C	SD1 Clock
SD2_SCLK_CFG_REG	0x0090	SD2 Clock
/	0x0094	/
/	0x0098	/
CE_SCLK_CFG_REG	0x009C	Crypto Engine Clock
SPI 0_SCLK_CFG_REG	0x00A0	SPI0 Clock
SPI 1_SCLK_CFG_REG	0x00A4	SPI1 Clock
SPI 2_SCLK_CFG_REG	0x00A8	SPI2 Clock
/	0x00AC	/
IR_SCLK_CFG_REG	0x00B0	IR Clock
/	0x00B4	/
/	0x00B8	/
/	0x00BC	/
/	0x00C0	/
/	0x00C4	/
/	0x00C8	/
/	0x00CC	/
/	0x00D0	/
/	0x00D4	/
DRAM_SCLK_CFG_REG	0x0100	DRAM Clock
BE_CFG_REG	0x0104	Display Engine Backend Clock
/	0x0108	
FE_CFG_REG	0x010C	Display Engine Front End Clock

/	0x0110	/
/	0x0114	/
/	0x0118	/
/	0x011C	/
/	0x0120	/
/	0x0124	/
/	0x0128	/
LCD_CH1_CFG_REG	0x012C	LCD Channel1 Clock
/	0x0130	/
CSI_CFG_REG	0x0134	CSI Clock
/	0x0138	/
VE_CFG_REG	0x013C	Video Engine Clock
AUDIO_CODEC_SCLK_CFG_REG	0x0140	Audio Codec Gating Special Clock
AVS_SCLK_CFG_REG	0x0144	AVS Gating Special Clock
/	0x0148	/
/	0x014C	/
/	0x0150	/
MALI_CLOCK_CFG_REG	0x0154	Mali400 Gating Special Clock
/	0x0158	/
MBUS_SCLK_CFG_REG	0x015C	MBUS Gating Clock
IEP_SCLK_CFG_REG	0x0160	IEP Gating Clock

5.4. CCM Register Description

5.4.1. PLL1-Core (Default: 0x21005000)

Offset: 0x00			Register Name: PLL1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL1_Enable. 0: Disable, 1: Enable. The PLL1 output= (24MHz*N*K)/ (M*P). The PLL1 output is for the CORECLK. Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled. Its default is 384MHz.
30:18	/	/	/
17:16	R/W	0x0	PLL1_OUT_EXT_DIVP. PLL1 Output external divider P. The range is 1/2/4/8.
15:13	/	/	/.
12:8	R/W	0x10	PLL1_FACTOR_N PLL1 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2 …… Factor=31,N=31
7:6	/	/	/
5:4	R/W	0x0	PLL1_FACTOR_K. PLL1 Factor K.(K=Factor + 1) The range is from 1 to 4.
3	R/W	0x0	/
2	R/W	0x0	/

1:0	R/W	0x0	PLL1_FACTOR_M. PLL1 Factor M. (M=Factor + 1) The range is from 1 to 4.

5.4.2. PLL1-Tuning (Default: 0x0A101000)

Offset: 0x04			Register Name: PLL1_TUN_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0x1	/
26	R/W	0x0	/
25:23	R/W	0x4	/
22:16	R/W	0x10	/
15	R/W	0x0	/
14:8	R/W	0x10	/
7	R/W	0x0	/
6:0	R	0x0	/

5.4.3. PLL2-Audio (Default: 0x08100010)

Offset: 0x08			Register Name: PLL2_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL2_Enable. 0: Disable, 1: Enable. The PLL2 is for Audio. PLL2 Output = 24MHz*N/PLL2_PRE_DIV/PLL2_POST_DIV. 1X = 48*N/PreDiv/PostDiv/2(not 50% duty) 2X = 48*N/PreDiv/4(8X/4 50% duty) 4X = 48*N/PreDiv/2(8X/2 50% duty) 8X = 48*N/PreDiv(not 50% duty)
30	/	/	/
29:26	R/W	0x2	PLL2_POST_DIV. PLL2 post-divider [3:0]. 0000: 0x1 …… 1111: 0x10
25:21	R/W	0x0	/
20:16	R/W	0x10	/
15	/	/	/
14:8	R/W	0x0	PLL2_Factor_N. PLL2 Factor N. Factor=0, N=1; Factor=1, N=1; …… Factor=0x7F, N=0x7F;
7:5	/	/	/
4:0	R/W	0x10	PLL2_PRE_DIV. PLL2 pre-divider [4:0]. 00000: 0x1 …… 11111: 0x20

5.4.4. PLL2-Tuning (Default: 0x00000000)

Offset: 0x0C	Register Name: PLL2_TUN_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	/
30:29	R/W	0x0	/
28:20	R/W	0x0	/
19	/	/	/
18:17	R/W	0x0	/
16:0	R/W	0x0	/

5.4.5. PLL3-Video (Default: 0x0010D063)

Offset: 0x10			Register Name: PLL3_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL3_Enable. 0: Disable, 1: Enable. In the integer mode, The PLL3 output=3MHz*M. In the fractional mode, the PLL3 output is select by bit 14. The PLL3 output range is 27MHz~381MHz.
30:27	/	/	/
26:24	R/W	0x0	/
23:21	/	/	/
20:16	R/W	0x10	/
15	R/W	0x1	PLL3_MODE_SEL. PLL3 mode select. 0: fractional mode, 1: integer mode.
14	R/W	0x1	PLL3_FUNC_SET. PLL3 fractional setting. 0: 270MHz, 1: 297MHz.
13	/	/	/
12:8	R/W	0x10	/
7	/	/	/
6:0	R/W	0x63	PLL3_FACTOR_M. PLL3 Factor M. The range is from 9 to 127.

5.4.6. PLL4-VE (Default: 0x21081000)

Offset: 0x18			Register Name: PLL4_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL4_Enable. 0: Disable, 1: Enable. The PLL4 output= (24MHz*N*K)/ (M*P). The PLL4 output is for the VE. Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled.
30	R/W	0x0	PLL4_OUT_BYPASS_EN. PLL4 Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL4 output is 24MHz.
29:25	R/W	0x10	/
24:20	R/W	0x10	/
19	R/W	0x1	/
18	/	/	/.
17:16	R/W	0x0	PLL4_OUT_EXT_DIV_P. PLL4 Output external divider P. The range is 1/2/4/8.

15:13	/	/	/
12:8	R/W	0x10	PLL4_FACTOR_N. PLL4 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2 …… Factor=31,N=31
7:6	/	/	/.
5:4	R/W	0x0	PLL4_FACTOR_K. PLL4 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/.
1:0	R/W	0x0	PLL4_FACTOR_M. PLL4 Factor M.(M = Factor + 1) The range is from 1 to 4.

5.4.7. PLL5-DDR (Default: 0x11049280)

Offset: 0x20			Register Name: PLL5_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL5_Enable. 0: Disable, 1: Enable. The PLL5 output for DDR = (24MHz*N*K)/M. The PLL5 output for other module = (24MHz*N*K)/P. The PLL5 output is for the DDR. Note: the output 24MHz*N*K clock must be in the range of 240MHz~2GHz if the bypass is disabled.
30	R/W	0x0	PLL5_OUT_BYPASS_EN. PLL5 Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL6 output is 24MHz.
29	R/W	0x0	DDR_CLK_OUT_EN. DDR clock output en.
28:25	R/W	0x8	/
24:20	R/W	0x10	/
19	R/W	0x0	/
18	R/W	0x1	/
17:16	R/W	0x0	PLL5_OUT_EXT_DIV_P. PLL5 Output External Divider P. The range is 1/2/4/8.
15:13	R/W	0x4	/
12:8	R/W	0x12	PLL5_FACTOR_N. PLL5 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2 …… Factor=31,N=31
7	R/W	0x1	LDO_EN. LDO Enable.
6	/	/	/
5:4	R/W	0x0	PLL5_FACTOR_K. PLL5 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	R/W	0x0	PLL5_FACTOR_M1.

			PLL5 Factor M1.
1:0	R/W	0x0	PLL5_FACTOR_M. PLL5 Factor M.(M = Factor + 1) The range is from 1 to 4.

5.4.8. PLL5-Tuning (Default: 0x14880000)

Offset: 0x24			Register Name: PLL5_TUN_REG
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

5.4.9. PLL6 (Default: 0x21009931)

Offset: 0x28			Register Name: PLL6_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL6_Enable. 0: Disable, 1: Enable. Output =(24MHz*N*K)/M/2 Note: the output 24MHz*N*K clock must be in the range of 240MHz~3GHz if the bypass is disabled. Its default is 1200MHz.
30	R/W	0x0	PLL6_BYPASS_EN. PLL6 Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL6 output is 24MHz.
29:13	/	/	/
12:8	R/W	0x19	PLL6_FACTOR_N. PLL6 Factor N. Factor=0, N=0; Factor=1, N=1; Factor=2, N=2; …… Factor=31,N=31
7:6	/	/	PLL6 damping factor control [1:0].
5:4	/	/	PLL6_FACTOR_K. PLL6 Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	PLL6_FACTOR_M. PLL6 Factor M.(M = Factor + 1) The range is from 1 to 4.

5.4.10. PLL7 (Default: 0x0010D063)

Offset: 0x30			Register Name: PLL7_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	PLL7_Enable. 0: Disable, 1: Enable. In the integer mode, The PLL7 output=3MHz*M. In the fractional mode, the PLL7 output is select by bit 14. The PLL7 output range is 27MHz~381MHz.
30:16	/	/	/
15	R/W	0x1	PLL7_MODE_SEL. PLL7 mode select. 0: fractional mode, 1: integer mode.

14	R/W	0x1	PLL7_FRAC_SET. PLL7 fractional setting. 0: 270MHz, 1: 297MHz.
13:7	/	/	/
6:0	R/W	0x63	PLL7_FACTOR_M. PLL7 Factor M. The range is from 9 to 127.

5.4.11. PLL1-Tuning2 (Default: 0x00000000)

Offset: 0x38			Register Name: PLL1_TUN2_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

5.4.12. PLL5-Tuning2 (Default: 0x00000000)

Offset: 0x3C			Register Name: PLL5_TUN2_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

5.4.13. OSC24M (Default: 0x00138013)

Offset: 0x50			Register Name: OSC24M_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	/
23:18	/	/	/
17	R/W	0x1	PLL_IN_PWR_SEL. PLL Input Power Select. 0: 2.5v, 1: 3.3v
16	R/W	0x1	LDO_EN. LDO Enable. 0: Disable, 1: Enable.
15	R/W	0x1	PLL_BIAS_EN. PLL Bias Enable. 0: disable, 1: enable.
14:2	/	/	/
1	R/W	0x1	OSC24M_GSM. OSC24M GSM.
0	R/W	0x1	OSC24M_EN. OSC24M Enable. 0: Disable, 1: Enable.

5.4.14. CPU/AHB/APB0 Clock Ratio (Default: 0x00010010)

Offset: 0x54			Register Name: CPU_AHB_APB0_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17:16	R/W	0x1	CPU_CLK_SRC_SEL. CPU Clock Source Select. 00: 32KHz OSC(Internal) 01: OSC24M 10: PLL1 11: 200MHz (source from the PLL6). If the clock source is changed, at most to wait for 8 present running clock cycles.
15:10	/	/	/
9:8	R/W	0x0	APB0_CLK_RATIO. APB0 Clock divide ratio. APB0 clock source is AHB2 clock. 00: /2 01: /2 10: /4 11: /8
7:6	R/W	0x0	AHB_CLK_SRC_SEL. 00: AXI 01: CPUCLK 10: PLL6/2 11:
5:4	R/W	0x1	AHB_CLK_DIV_RATIO. AHB Clock divide ratio. AHB clock source is AXI Clock. 00: /1 01: /2 10: /4

			11: /8
3:2	/	/	/
1:0	R/W	0x0	AXI_CLK_DIV_RATIO. AXI Clock divide ratio. AXI Clock source is CPU clock. 00: /1 01: /2 10: /3 11: /4

5.4.15. APB1 Clock Divide Ratio (Default: 0x00000000)

Offset: 0x58			Register Name: APB1_CLK_DIV_REG
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:24	R/W	0x0	APB1_CLK_SRC_SEL. APB1 Clock Source Select 00: OSC24M 01: PLL6 (set to 1.2GHz) 10: 32KHz 11: / This clock is used for some special module apbclk (TWI, UART, and SCR). Because these modules need special clock rate even if the apbclk changes.
23:18	/	/	/
17:16	R/W	0x0	CLK_RAT_N Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:5	/	/	/
4:0	R/W	0x0	CLK_RAT_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

5.4.16. AXI Module Clock Gating (Default: 0x00000000)

Offset: 0x5C			Register Name: AXI_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	DRAM_AXI_GATING. Gating AXI Clock for SDRAM (0: mask, 1: pass).

5.4.17. AHB Module Clock Gating Register 0(Default: 0x00000000)

Offset: 0x60			Register Name: AHB_GATING_REG0
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28	R/W	0x0	STIMER_AHB_GATING. Gating AHB Clock for Sync timer (0: mask, 1: pass).
27	/	/	/
26	R/W	0x0	/
25:23	/	/	/
22	R/W	0x0	SPI2_AHB_GATING. Gating AHB Clock for SPI2 (0: mask, 1: pass).
21	R/W	0x0	SPI1_AHB_GATING.

			Gating AHB Clock for SPI1 (0: mask, 1: pass).
20	R/W	0x0	SPI0_AHB_GATING. Gating AHB Clock for SPI0 (0: mask, 1: pass).
19	/	/	/
18	R/W	0x0	/
17	R/W	0x0	/
16:15	/	/	/
14	R/W	0x0	SDRAM_AHB_GATING. Gating AHB Clock for SDRAM (0: mask, 1: pass).
13	R/W	0x0	NAND_AHB_GATING. Gating AHB Clock for NAND (0: mask, 1: pass).
12	R/W	0x0	/
11	/	/	/
10	R/W	0x0	SD2_AHB_GATING. Gating AHB Clock for SD/MMC2 (0: mask, 1: pass).
9	R/W	0x0	SD1_AHB_GATING. Gating AHB Clock for SD/MMC1 (0: mask, 1: pass).
8	R/W	0x0	SD0_AHB_GATING. Gating AHB Clock for SD/MMC0 (0: mask, 1: pass).
7	R/W	0x0	BIST_AHB_GATING. Gating AHB Clock for BIST (0: mask, 1: pass).
6	R/W	0x0	DMA_AHB_GATING. Gating AHB Clock for DMA (0: mask, 1: pass).
5	R/W	0x0	CE_AHB_GATING. Gating AHB Clock for CE (0: mask, 1: pass).
4:3	/	/	/
2	R/W	0x0	OHCI_AHB_GATING. Gating AHB Clock for USB OHCI (0: mask, 1: pass).
1	R/W	0x0	EHCI_AHB_GATING. Gating AHB Clock for USB EHCI (0: mask, 1: pass).
0	R/W	0x0	USBOTG_AHB_GATING. Gating AHB Clock for USB OTG (0: mask, 1: pass).

5.4.18. AHB Module Clock Gating Register 1(Default: 0x00000000)

Offset: 0x64			Register Name: AHB_GATING_REG1
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20	R/W	0x0	Gating AHB Clock for Mali-400(0: mask, 1: pass).
19	R/W	0x0	IEP_AHB_GATING. Gating AHB Clock for IEP (0: mask, 1: pass).
18:15	/	/	/
14	R/W	0x0	FE_AHB_GATING. Gating AHB Clock for DE-FE (0: mask, 1: pass).
13	/	/	/
12	R/W	0x0	BE_AHB_GATING. Gating AHB Clock for DE-BE (0: mask, 1: pass).
11	R/W	0x0	/
10:9	/	/	/
8	R/W	0x0	CSI_AHB_GATING. Gating AHB Clock for CSI (0: mask, 1: pass).
7:5	/	/	/
4	R/W	0x0	LCD_AHB_GATING. Gating AHB Clock for LCD (0: mask, 1: pass).
3	/	/	/

2	R/W	0x0	/
1	/	/	/
0	R/W	0x0	VE_AHB_GATING. Gating AHB Clock for VE (0: mask, 1: pass).

5.4.19. APB0 Module Clock Gating (Default: 0x00000000)

Offset: 0x68			Register Name: APB0_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	/
9:7	/	/	/
6	R/W	0x0	IR_APB_GATING. Gating APB Clock for IR (0: mask, 1: pass).
5	R/W	0x0	PIO_APB_GATING. Gating APB Clock for PIO (0: mask, 1: pass).
4	/	/	/
3	R/W	0x0	/
2	/	/	/
1	R/W	0x0	/
0	R/W	0x0	CODEC_APB_GATING. Gating APB Clock for Audio CODEC (0: mask, 1: pass).

5.4.20. APB1 Module Clock Gating (Default: 0x00000000)

Offset: 0x6C			Register Name: APB1_GATING_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	/	/	/
22	/	/	/
21	/	/	/
20	/	/	/
19	R/W	0x0	UART3_APB_GATING. Gating APB Clock for UART3 (0: mask, 1: pass).
18	R/W	0x0	/
17	R/W	0x0	UART1_APB_GATING. Gating APB Clock for UART1 (0: mask, 1: pass).
16	R/W	0x0	/
15:8	/	/	/
7	/	/	/
6	/	/	/
5	/	/	/
4	/	/	/
3	/	/	/
2	R/W	0x0	TWI2_APB_GATING. Gating APB Clock for TWI2 (0: mask, 1: pass).
1	R/W	0x0	TWI1_APB_GATING. Gating APB Clock for TWI1 (0: mask, 1: pass).
0	R/W	0x0	TWI0_APB_GATING. Gating APB Clock for TWI0 (0: mask, 1: pass).

5.4.21. NAND Clock (Default: 0x00000000)

Offset: 0x80	Register Name: NAND_SCLK_CFG_REG

Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

Note: In application, the module clock frequency always switches off.

5.4.22. SD0 Clock (Default: 0x00000000)

Offset: 0x88			Register Name: SD0_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.23. SD1 Clock (Default: 0x00000000)

Offset: 0x8C			Register Name: SD1_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz)

			0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.24. SD2 Clock (Default: 0x00000000)

Offset: 0x90			Register Name: SD2_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.25. CE Clock (Default: 0x00000000)

Offset: 0x9C			Register Name: CE_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL.

			Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.26. SPI0 Clock (Default: 0x00000000)

Offset: 0xA0			Register Name: SPI 0_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.27. SPI1 Clock (Default: 0x00000000)

Offset: 0xA4			Register Name: SPI1_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /

23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.28. SPI2 Clock (Default: 0x00000000)

Offset: 0xA8			Register Name: SPI2_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_M. Clock pre-divide ratio (n) The select clock source is pre-divided by 2n. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.29. IR Clock (Default: 0x00000000)

Offset: 0xB0			Register Name: IR_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 100MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: /
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO. Clock pre-divide ratio (n) The select clock source is pre-divided by 2n. The divider is 1/2/4/8.
15:4	/	/	/

3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.30. USB Clock (Default: 0x00000000)

Offset: 0xCC			Register Name: USBPHY_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R/W	0x0	USBPHY1_CLK_GATING. Gating Special Clock for USB PHY1 0: Clock is OFF 1: Clock is ON
8	R/W	0x0	USBPHY0_CLK_GATING. Gating Special Clock for USB PHY0 0: Clock is OFF 1: Clock is ON
7	/	/	/
6	R/W	0x0	OHCI_SCLK_GATING. Gating Special Clock for OHCI 0: Clock is OFF 1: Clock is ON
5	/	/	/
4	/	/	/
3	/	/	/
2	/	/	/
1	R/W	0x0	USBPHY1_RST_CTRL. USB PHY1 Reset Control 0: Reset valid 1: Reset invalid
0	R/W	0x0	USBPHY0_RST_CTRL. USB PHY0 Reset Control 0: Reset valid 1: Reset invalid

5.4.31. DRAM CLK (Default: 0x00000000)

Offset: 0x100			Register Name: DRAM_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	IEP_DCLK_GATING. Gating DRAM Clock for IEP (0: mask, 1: pass).
30	/	/	/
29	R/W	0x0	ACE_DCLK_GATING. Gating DRAM Clock for ACE (0: mask, 1: pass).
28	/	/	/
27	/	/	/
26	R/W	0x0	BE_DCLK_GATING. Gating DRAM Clock for DE_BE (0: mask, 1: pass).
25	R/W	0x0	FE_DCLK_GATING. Gating DRAM Clock for DE_FE (0: mask, 1: pass).
24	/	/	/
23:16	/	/	/
15	/	/	/
14:7	/	/	/
6	/	/	/

5	R/W	0x0	/
4	/	/	/
3	R/W	0x0	/
2	/	/	/
1	R/W	0x0	CSI_DCLK_GATING. Gating DRAM Clock for CSI (0: mask, 1: pass).
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM Clock for VE (0: mask, 1: pass).

5.4.32. DE-BE Clock (Default: 0x00000000)

Offset: 0x104			Register Name: BE_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	BE_RST. DE-BE Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL5 11: /.
23:18	/	/	/
17:16	/	/	/
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.33. DE-FE Clock(Default: 0x00000000)

Offset: 0x10C			Register Name: FE_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	FE_RST. DE-FE Reset. 0: reset valid, 1: reset invalid.
29:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: PLL3 01: PLL7 10: PLL5 11: /.
23:18	/	/	/

17:16	/	/	/
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.34. LCD CH1 Clock (Default: 0x00000000)

Offset: 0x12C			Register Name: LCD_CH1_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK2_GATING. Gating Special Clock 2 0: Clock is OFF 1: Clock is ON This special clock 2= Special Clock 2 Source/Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK2_SRC_SEL. Special Clock 2 Source Select 00: PLL3(1X) 01:PLL7(1X) 10: PLL3(2X) 11: PLL7(2X)
23:18	/	/	/
17:16	R/W	0x0	/
15	/	/	SCLK1_GATING. Gating Special Clock 1 0: Clock is OFF 1: Clock is ON This special clock 1= Special Clock 1 Source.
14:12	/	/	/
11	R/W	0x0	SCLK1_SRC_SEL. Special Clock 1 Source Select. 0: Special Clock 2 1: Special Clock 2 divide by 2
10:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.35. CSI Clock (Default: 0x00000000)

Offset: 0x134			Register Name: CSI_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	CSI_RST. CSI Reset. 0: reset valid, 1: reset invalid.
29:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: OSC24M

			001: PLL3(1X) 010: PLL7(1X) 011: / 100: / 101: PLL3(2X) 110: PLL7(2X) 111: /
23:18	/	/	/
17:16	/	/	/
15:5	/	/	/
4:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

5.4.36. VE Clock (Default: 0x00000000)

Offset: 0x13C			Register Name: VE_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating the Special clock for VE (0: mask, 1: pass). 0: Clock is OFF 1: Clock is ON This special clock is PLL4.
25:24	/	/	/
30:20	/	/	/
19:16	/	/	/
15:1	/	/	/
0	R/W	0x0	VE_RST. VE Reset. 0: reset valid, 1: reset invalid.

5.4.37. Audio Codec Clock (Default: 0x00000000)

Offset: 0x140			Register Name: AUDIO_CODEC_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = PLL2 output.
30:0	/	/	/

5.4.38. AVS Clock (Default: 0x00000000)

Offset: 0x144			Register Name: AVS_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = OSC24M.
30:0	/	/	/

5.4.39. Mali-400 Clock Register(Default: 0x00000000)

Offset: 0x154			Register Name: MALI_CLOCK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 381MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30	R/W	0x0	MALI400_RST. Mali400 Reset. 0: reset valid, 1: reset invalid
29:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL3(1X) 001: PLL4 010: PLL5 011: PLL7 (1X). 100: PLL7(2X)
23:18	/	/	/
17:16	/	/	/
15:4	/	/	/.
3:0	R/W	0x0	CLK_DIV_RATIO_M Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

5.4.40. MBUS Clock Control (Default: 0x00000000)

Offset: 0x15C			Register Name: MBUS_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS (Max Clock = 300MHz) 0: Clock is OFF, 1: Clock is ON; MBUS_CLOCK = Clock Source/Divider N/Divider M
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select 00: OSC24M 01: PLL6 10: PLL5 11: Reserved
23:18	/	/	/
17:16	R/W	0x0	MBUS_SCLK_RATIO_N Clock Pre-divide Ratio (N) The select clock source is pre-divided by 2^N. The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (M) The divided clock is divided by (M+1). The divider is from 1 to 16.

5.4.41. IEP Clock Control (Default: 0x00000000)

Offset: 0x160			Register Name: IEP_SCLK_CFG_REG
Bit	Read/Write	Default/Hex	Description

31	R/W	0x0	IEP_SCLK_GATING. Gating Clock for IEP (Max Clock = 300MHz) 0: Clock is OFF, 1: Clock is ON; IEP_CLOCK = BE Clock
30	R/W	0x0	IEP_RST. IEP Reset. 0: reset valid, 1: reset invalid.
29:0	/	/	/

Chapter 6 System Control

6.1. Overview

The chip embeds a high-speed SRAM, which is split into five areas. Its Memory Mapping is detailed in the following table:

Area	Address	Size(Bytes)
A1	0x00000000--0x00003FFF	16K
A2	0x00004000--0x00007FFF	16K
A3	0x00008000--0x0000B3FF	13K
A4	0x0000B400--0x0000BFFF	3K
C1	0x01D00000-0x01D7FFFF	VE
C3	0x01DC0000-0x01DCFFFF	ISP
NAND		2K
D(USB)	0x00010000—0x00010FFF	4K
CPU I-Cache		32K
CPU D-Cache		32K
CPU L2 Cache		128K

6.2. System Control Register List

Module Name	Base Address
SRAM	0x01C00000

Register Name	Offset	Description
SRAM_CFG_REG0	0x0000	SRAM Configuration
SRAM_CFG_REG1	0x0004	SRAM Control

6.3. System Control Register Description

6.3.1. SRAM Configuration Register 0(Default: 0x7FFFFFFF)

Offset: 0x00			Register Name: SRAM_CFG_REG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:0	R/W	0x7fffffff	SRAM_C1_MAP. SRAM Area C1 50K Bytes Configuration by AHB. 0: map to CPU/DMA 1: map to VE

6.3.2. SRAM Configuration Register 1(Default: 0x00001000)

Offset: 0x04			Register Name: SRAM_CFG_REG1
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	/
30:18	/	/	/
17	R/W	0x0	/
16	R/W	0x0	/
15:14	R/W	0x0	/

13	/	/	/
12	R/W	0x1	SRAM_C3_MAP. SRAM C3 map config. 0: map to CPU/BIST 1: map to ISP
11:6	/	/	/
5:4	R/W	0x0	SRAM_A3_A4_MAP. SRAM Area A3/A4 Configuration by AHB. 00: map to CPU/DMA 01: / 10/11: /
3:1	/	/	/
0	R/W	0x0	SRAM_D_MAP. SRAM D Area Config. 0: map to CPU/DMA 1: map to USB-OTG

Chapter 7 CPU Control

7.1. CPU Register List

Module Name	Base Address
CPU CTL	0x01C23400

Register Name	Offset	Description
CPU_CTRL_REG	0x0020	CPU Control Register

7.2. CPU Control Register Description

7.2.1. CPU Control Register(Default:0x00000002)

Offset: 0x20			Register Name: CPU_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/.
8	R/W	0x0	CPU_ID. CPU ID Option.
7:2	/	/	/
1	R/W	0x1	/
0	R/W	0x0	CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

Chapter 8 SDRAM Controller

8.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industy-standard double data rate II (DDR2) ordinary SDRAM and Double data rate III (DDR3) ordinary SDRAM. It supports up to a 512MB memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The DRAMC includes following features:

- Support DDR2 SDRAM and DDR3 SDRAM
- Support different memory device power voltage of 1.5V and 1.8V
- Support memory capacity up to 512MB
- 15 address lines and 3 bank address lines
- Data IO size can up to 16-bit for DDR2 and DDR3
- Automatically generate initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different applications
- Priority of transferring through multiple ports is programmable
- Support random read or write operation

Chapter 9 PWM

9.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to activate state and count from 0x0000.

The PWM divider divides the clock (24MHz) by 1-4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

9.2. PWM Register List

Module Name	Base Address
PWM	0x01C20C00

Register Name	Offset	Description
PWM_CTRL_REG	0x0200	PWM Control Register
PWM_CH0_PERIOD_REG	0x0204	PWM Channel 0 Period Register

9.3. PWM Register Description

9.3.1. PWM Control Register (Default: 0x00000000)

Offset: 0x200			Register Name: PWM_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0x0	/
28	R/W	0x0	PWM0_RDY. PWM0 period register ready. 0: PWM0 period register is ready to write, 1: PWM0 period register is busy.
27:25	/	/	/
24:15	R/W	0x0	/
14:10	/	/	/
9	R/W	0x0	PWM0_BYPASS. PWM CH0 bypass enable. If the bit is set to 1, PWM0's output is OSC24MHz. 0: disable, 1: enable.
8	R/W	0x0	PWM_CH0_PUL_START. PWM Channel 0 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 0 register [15:0], and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.

7	R/W	0x0	PWM_CHANNEL0_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH0_GATING. Gating the Special Clock for PWM0 (0: mask, 1: pass).
5	R/W	0x0	PWM_CH0_ACT_STA. PWM Channel 0 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH0_PRESCAL. PWM Channel 0 Prescalar. These bits should be setting before the PWM Channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1

9.3.2. PWM Channel 0 Period Register

Offset: 0x204			Register Name: PWM_CH0_PERIOD_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	x	PWM_ENT_CYC. Number of the entire cycles in the PWM clock. 0 = 1 cycle 1 = 2 cycles …… N = N+1 cycles.
15:0	R/W	x	PWM_ACT_CYC. Number of the active cycles in the PWM clock. 0 = 0 cycle 1 = 1 cycles …… N = N cycles

Note: the active cycles should be no larger than the period cycles.

Chapter 10 Asynchronic Timer

10.1. Overview

The chip implements 6 async timers.

Timer 0/1/2 can take their inputs from the PLL6/6 or OSC24M. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 32-bit programmable overflow counter and work in auto-reload mode or no-reload mode.

The watch-dog is used to resume controller operation by generating a general reset or an interrupt request when it is disturbed by malfunctions such as noise sand system errors. It features a down counter that allows a watchdog period of up to 16 seconds.

Timer 3 is used for OS to generate a periodic interrupt.

10.2. ASYNC Timer Register List

Module Name	Base Address
ASYNC Timer	0x01C20C00

Register Name	Offset	Description
ASYNC_TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable
ASYNC_TMR_IRQ_STAS_REG	0x0004	Timer Status
ASYNC_TMR0_CTRL_REG	0x0010	Timer 0 Control
ASYNC_TMR0_INTV_VALUE_REG	0x0014	Timer 0 Interval Value
ASYNC_TMR0_CURNT_VALUE_REG	0x0018	Timer 0 Current Value
ASYNC_TMR1_CTRL_REG	0x0020	Timer 1 Control
ASYNC_TMR1_INTV_VALUE_REG	0x0024	Timer 1 Interval Value
ASYNC_TMR1_CURNT_VALUE_REG	0x0028	Timer 1 Current Value
ASYNC_TMR2_CTRL_REG	0x0030	Timer 2 Control
ASYNC_TMR2_INTV_VALUE_REG	0x0034	Timer 2 Interval Value
ASYNC_TMR2_CURNT_VALUE_REG	0x0038	Timer 2 Current Value
ASYNC_TMR3_CTRL_REG	0x0040	Timer 3 Control
ASYNC_TMR3_INTV_VALUE_REG	0x0044	Timer 3 Interval Value
ASYNC_TMR4_CTRL_REG	0x0050	Timer 4 Control
ASYNC_TMR4_INTV_VALUE_REG	0x0054	Timer 4 Interval Value
ASYNC_TMR4_CURNT_VALUE_REG	0x0058	Timer 4 Current Value
ASYNC_TMR5_CTRL_REG	0x0060	Timer 5 Control
ASYNC_TMR5_INTV_VALUE_REG	0x0064	Timer 5 Interval Value
ASYNC_TMR5_CURNT_VALUE_REG	0x0068	Timer 5 Current Value
AVS_CNT_CTL_REG	0x0080	AVS Control Register
AVS_CNT0_REG	0x0084	AVS Counter 0 Register
AVS_CNT1_REG	0x0088	AVS Counter 1 Register
AVS_CNT_DIVISOR_REG	0x008C	AVS Divisor
WDOG_CTRL_REG	0x0090	Watchdog Control

WDOG_MODE_REG	0x0094	Watchdog Mode
COUNTER64_CTRL_REG	0x00A0	64-bit Counter control
COUNTER64_LOW_REG	0x00A4	64-bit Counter low
COUNTER64_HI_REG	0x00A8	64-bit Counter high
CPU_CFG_REG	0x0140	CPU configuration register

10.3. ASYNC Timer Register Description

10.3.1. ASYNC Timer IRQ Enable Register (Default: 0x00000000)

Offset: 0x00			Register Name: ASYNC_TMR_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	WDOG_INT_EN. Watchdog Interrupt Enable. 0: No effect, 1: watchdog Interval Value reached interrupt enable.
7:6	/	/	/
5	R/W	0x0	TMR5_INT_EN. Timer 5 Interrupt Enable. 0: No effect, 1: Timer 5 Interval Value reached interrupt enable.
4	R/W	0x0	TMR4_INT_EN. Timer 4 Interrupt Enable. 0: No effect, 1: Timer 4 Interval Value reached interrupt enable.
3	R/W	0x0	TMR3_INT_EN. Timer 3 Interrupt Enable. 0: No effect, 1: Timer 3 Interval Value reached interrupt enable.
2	R/W	0x0	TMR2_INT_EN. Timer 2 Interrupt Enable. 0: No effect, 1: Timer 2 Interval Value reached interrupt enable.
1	R/W	0x0	TMR1_INT_EN. Timer 1 Interrupt Enable. 0: No effect, 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	TMR0_INT_EN. Timer 0 Interrupt Enable. 0: No effect, 1: Timer 0 Interval Value reached interrupt enable.

10.3.2. ASYNC Timer IRQ Status Register(Default: 0x00000000)

Offset: 0x04			Register Name: ASYNC_TMR_IRQ_STAS_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	WDOG_IRQ_PEND. Watchdog IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, Watchdog counter value is reached.
7:6	/	/	/
5	R/W	0x0	TMR5_IRQ_PEND. Timer 5 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 5 counter value is reached.
4	R/W	0x0	TMR4_IRQ_PEND. Timer 4 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 4 counter value is reached.
3	R/W	0x0	TMR3_IRQ_PEND. Timer 3 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 3 counter value is reached.
2	R/W	0x0	TMR2_IRQ_PEND.

			Timer 2 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 2 counter value is reached.
1	R/W	0x0	TMR1_IRQ_PEND. Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 1 interval value is reached.
0	R/W	0x0	TMR0_IRQ_PEND. Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending, timer 0 interval value is reached.

10.3.3. ASYNC Timer 0 Control Register (Default: 0x00000004)

Offset: 0x10			Register Name: ASYNC_TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR0_MODE. Timer0 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically.
6:4	R/W	0x0	TMR0_CLK_PRES Select the pre-scale of timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR0_CLK_SRC. Timer 0 Clock Source. 00:/ 01: OSC24M. 10: PLL6/6 11: /
1	R/W	0x0	TMR0_RELOAD. Timer 0 Reload. 0: No effect, 1: Reload timer 0 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR0_EN. Timer 0 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0"; the current value counter will pause. At least wait for 2 Tcycles, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note: Time between the timer disabled and enabled should be larger than 2*Tcycles (Tcycles= Timer clock source/pre-scale).

10.3.4. ASYNC Timer 0 Interval Value Register

Offset: 0x14			Register Name: ASYNC_TMR0_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR0_INTV_VALUE. Timer 0 Interval Value.

Note: The value setting should consider the system clock and the timer clock source.

10.3.5. ASYNC Timer 0 Current Value Register

Offset: 0x18			Register Name: ASYNC_TMR0_CURNT_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TMR0_CUR_VALUE. Timer 0 Current Value.

Note: Timer 0 current value is a 32-bit down-counter (from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq (TimerFreq = TimerClkSource/pre-scale).

10.3.6. ASYNC Timer 1 Control Register (Default: 0x00000004)

Offset: 0x20			Register Name: ASYNC_TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR1_MODE. Timer1 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically.
6:4	R/W	0x0	TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR1_CLK_SRC. Timer 1 Clock Source. 00:/ 01: OSC24M. 10: PLL6/6 11: /
1	R/W	0x0	TMR1_RELOAD. Timer 1 Reload. 0: No effect, 1: Reload timer 1 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR1_EN. Timer 1 Enable. 0: Stop/Pause, 1: Start.

			If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0"; the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note: Time between the timer disabled and enabled should be larger than 2*Tcycles (Tcycles= Timer clock source/pre-scale).

10.3.7. ASYNC Timer 1 Interval Value Register

Offset: 0x24			Register Name: ASYNC_TMR1_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR1_INTV_VALUE. Timer 1 Interval Value.

Note: The value setting should consider the system clock and the timer clock source.

10.3.8. ASYNC Timer 1 Current Value Register

Offset: 0x28			Register Name: ASYNC_TMR1_CURNT_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR1_CUR_VALUE. Timer 1 Current Value.

Note: Timer 1 current value is a 32-bit down-counter (from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq (TimerFreq = TimerClkSource/pre-scale).

10.3.9. ASYNC Timer 2 Control Register (Default: 0x00000004)

Offset: 0x30			Register Name: ASYNC_TMR2_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR2_EN. Timer2 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically.
6:4	R/W	0x0	TMR2_CLK_PRESCALE. Select the pre-scale of timer 2 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR2_CLK_SRC. Timer 2 Clock Source.

			00:/ 01: OSC24M. 1x: /.
1	R/W	0x0	TMR2_RELOAD. Timer 2 Reload. 0: No effect, 1: Reload timer 2 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR2_EN. Timer 2 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0"; the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note: Time between the timer disabled and enabled should be larger than 2*Tcycles (Tcycles= Timer clock source/pre-scale).

10.3.10. ASYNC Timer 2 Interval Value Register

Offset: 0x34			Register Name: ASYNC_TMR2_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR2_INTV_VALUE. Timer 2 Interval Value.

Note: The value setting should consider the system clock and the timer clock source.

10.3.11. ASYNC Timer 2 Current Value Register

Offset: 0x38			Register Name: ASYNC_TMR2_CURNT_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR2_CUR_VALUE. Timer 2 Current Value.

Note: Timer current value is a 32-bit down-counter (from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq (TimerFreq = TimerClkSource/pre-scale).

10.3.12. ASYNC Timer 3 Control Register (Default: 0x00000000)

Offset: 0x40			Register Name: ASYNC_TMR3_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR3_CLK_SRC. Timer 3 Clock Source. 0:internal 32k 1: OSC24M.
6:5	/	/	/
4	R/W	0x0	TMR3_MODE. Timer 3 mode.

			0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically.
3:2	R/W	0x0	TMR3_CLK_PRESCALE. Select the pre-scale of timer 3 clock source. 00: /16 01: /32 10: /64 11: /1
1	/	/	/
0	R/W	0x0	TMR3_EN. Timer 3 Enable. 0: Disable, 1: Enable.

Note: the time between the timer disabled and enabled should be larger than 2*Tcycles (Tcycles= Timer clock source/pre-scale).

10.3.13. ASYNC Timer 3 Interval Value

Offset: 0x44			Register Name: ASYNC_TMR3_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR3_INTV_VALUE. Timer 3 Interval Value.

10.3.14. ASYNC Timer 4 Control Register (Default: 0x00000004)

Offset: 0x50			Register Name: ASYNC_TMR4_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR4_MODE. Timer4 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically.
6:4	R/W	0x0	TMR4_CLK_PRESCALE. Select the pre-scale of timer 4 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR4_CLK_SRC. Timer 4 Clock Source. 00: / 01: OSC24M. 10: External CLKIN0 11: /.
1	R/W	0x0	TMR4_RELOAD. Timer 4 Reload. 0: No effect, 1: Reload timer 0 Interval value.

			After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR4_EN. Timer 4 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0"; the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note:
1.If the clock source is External CLKIN, the interval value register is not used, the current value register is an up counter that counting from 0.
2.The time between the timer disabled and enabled should be larger than 2*Tcycles (Tcycles= Timer clock source/pre-scale).

10.3.15. ASYNC Timer 4 Interval Value Register

Offset: 0x54			Register Name: ASYNC_TMR4_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR4_INTV_VALUE. Timer 4 Interval Value.

Note: the value setting should consider the system clock and the timer clock source.

10.3.16. ASYNC Timer 4 Current Value Register

Offset: 0x58			Register Name: ASYNC_TMR4_CURNT_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR4_CUR_VALUE. Timer 4 Current Value.

Note:
1.Timer current value is a 32-bit down-counter (from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq (TimerFreq = TimerClkSource/pre-scale).
2.Before the timer 4 is enabled, its current value register needs to be written with zero.

10.3.17. ASYNC Timer 5 Control Register (Default: 0x00000004)

Offset: 0x60			Register Name: ASYNC_TMR5_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0x0	TMR5_MODE. Timer5 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically.
6:4	R/W	0x0	TMR5_CLK_PRESCALE. Select the pre-scale of timer 5 clock source. 000: /1 001: /2

			010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
3:2	R/W	0x1	TMR5_CLK_SRC. Timer 5 Clock Source. 00: / 01: OSC24M. 10: External CLKIN1 11: /.
1	R/W	0x0	TMR5_RELOAD. Timer 5 Reload. 0: No effect, 1: Reload timer 0 Interval value. After the bit is set, it can not be written again before it's cleared automatically.
0	R/W	0x0	TMR5_EN. Timer 5 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0"; the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

Note：

1.If the clock source is External CLKIN, the interval value register is not used, the current value register is an up counter that counting from 0.

2.The time between the timer disabled and enabled should be larger than 2*Tcycles (Tcycles= Timer clock source/pre-scale).

10.3.18. ASYNC Timer 5 Interval Value Register

Offset: 0x64			Register Name: ASYNC_TMR5_INTV_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR5_INTV_VALUE. Timer 5 Interval Value.

Note: The value setting should consider the system clock and the timer clock source.

10.3.19. ASYNC Timer 5 Current Value Register

Offset: 0x68			Register Name: ASYNC_TMR5_CURNT_VALUE_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	TMR5_CUR_VALUE. Timer 5 Current Value.

Note:

1.Timer 1 current value is a 32-bit down-counter (from interval value to 0). This register can be read correctly if the PCLK is faster than 2*TimerFreq (TimerFreq = TimerClkSource/pre-scale).

2.Before timer 5 is enabled, its current value register needs to be written with zero.

10.3.20. AVS Counter Control Register (Default: 0x00000000)

Offset: 0x80			Register Name: AVS_CNT_CTL_REG
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
9	R	0x0	AVS_CNT1_PS Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable

10.3.21. AVS Counter 0 Register (Default: 0x00000000)

Offset: 0x84			Register Name: AVS_CNT0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	AVS_CNT0 Counter 0 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits 90KHz counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter won't increase.

10.3.22. AVS Counter 1 Register (Default: 0x00000000)

Offset: 0x88			Register Name: AVS_CNT1_REG
Bit	Read	Default/Hex	Description
31:0	R/W	0x0	AVS_CNT1 Counter 1 for Audio/ Video Sync Application The high 32 bits of the internal 33-bits 90KHz counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter won't increase.

10.3.23. AVS Counter Divisor Register (Default: 0x05DB05DB)

Offset: 0x8C			Register Name: AVS_CNT_DIVISOR_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0x5DB	AVS_CNT1_D Divisor N for AVS Counter1 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. Notes: It can be configured by software at any time.
15:12	/	/	/
11:0	R/W	0x5DB	AVS_CNT0_D Divisor N for AVS Counter0 The number N is from 1 to 0x7ff. The zero value is reserved. The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (>= N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again. Notes: It can be configured by software at any time.

10.3.24. Watchdog Control Register

Offset: 0x90			Register Name: WDOG_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:1	R/W	0x333	KEY_FIELD. /
0	R/W	x	WDOG_RESTART. Watchdog Restart. 0: No effect, 1: Restart the Watchdog.

10.3.25. Watchdog Mode Register (Default: 0x00000000)

Offset: 0x94			Register Name: WDOG_MODE_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	WDOG_TEST_MODE. 0: normal mode, 1: test mode.
30:7	/	/	/
6:3	R/W	0x0	WDOG_INTV_VALUE. Watchdog Interval Value Watchdog clock source is OSC24M. If the OSC24M is turned off, the watchdog will not work. 0000: 0.5sec 0001: 1sec 0010: 2sec 0011: 3sec 0100: 4sec 0101: 5sec 0110: 6sec 0111: 8sec

			1000: 10sec 1001: 12sec 1010: 14sec 1011: 16sec 1100: / 1101: / 1110: / 1111: /
2	/	/	/
1	R/W	0x0	WDOG_RST_EN. Watchdog Reset Enable. 0: No effect on the resets, 1: Enables the Watchdog to activate the system reset.
0	R/W	0x0	WDOG_EN. Watchdog Enable. 0: No effect, 1: Enable the Watchdog.

10.3.26. 64-bit Counter Low Register (Default: 0x00000000)

Offset: 0xA4			Register Name: COUNTER64_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CONT64_LO. 64-bit Counter [31:0].

10.3.27. 64-bit Counter High Register (Default: 0x00000000)

Offset: 0xA8			Register Name: COUNTER64_HI_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	CONT64_HI. 64-bit Counter [63:32].

10.3.28. 64-bit Counter Control Register (Default: 0x00000000)

Offset: 0xA0			Register Name: COUNTER64_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	CONT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: PLL6/6
1	R/W	0x0	CONT64_RLATCH_EN. 64-bit Counter Read Latch Enable. 0: no effect, 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	CONT64_CLR_EN. 64-bit Counter Clear Enable. 0: no effect, 1: to clear the 64-bit Counter Low/Hi registers and it will change to zero after the registers are cleared.

10.3.29. CPU Config Register (Default: 0x00000000)

Offset: 0x13C			Register Name: CPU_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	L1_INVALID_RST_EN.

			Enable L1 data cache invalidation at reset. For L1 data cache, the cycles are up to 512 CPU clock cycles 0: enable 1: disable
0	R/W	0x0	L2_INVALID_RST_EN. Enable L2 data cache invalidation at reset. For L1 data cache, the cycles are up to 1024 CPU clock cycles 0: enable 1: disable

Note: The bit [1:0] can be set to 0 by software.

Chapter 11 Synchronic Timer

11.1. Overview

The chip implements 2 sync timers for high-speed counter.

11.2. Sync Timer Register List

Module Name	Base Address
Sync Timer	0x01C60000

Register Name	Offset	Description
SYNC_TMR_IRQ_EN_REG	0x0000	Timer IRQ Enable
SYNC_TMR_IRQ_STAS_REG	0x0004	Timer Status
SYNC_TMR0_CTRL_REG	0x0010	Timer 0 Control
SYNC_TMR0_INTV_LO_REG	0x0014	Timer 0 Interval Value Low
SYNC_TMR0_INTV_HI_REG	0x0018	Timer 0 Interval Value High
SYNC_TMR0_CURNT_LO_REG	0x001C	Timer 0 Current Value Low
SYNC_TMR0_CURNT_HI_REG	0x0020	Timer 0 Current Value High
SYNC_TMR1_CTRL_REG	0x0030	Timer 1 Control
SYNC_TMR1_INTV_LO_REG	0x0034	Timer 1 Interval Value Low
SYNC_TMR1_INTV_HI_REG	0x0038	Timer 1 Interval Value High
SYNC_TMR1_CURNT_LO_REG	0x003C	Timer 1 Current Value Low
SYNC_TMR1_CURNT_HI_REG	0x0040	Timer 1 Current Value High

11.3. Sync Timer Register Description

11.3.1. Sync Timer IRQ Enable Register (Default: 0x00000000)

Offset: 0x00			Register Name: SYNC_TMR_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	STMR1_INT_EN. Sync Timer 1 Interrupt Enable. 0: No effect 1: Timer 1 Interval Value reached interrupt enable.
0	R/W	0x0	STMR0_INT_EN. Sync Timer 0 Interrupt Enable. 0: No effect 1: Timer 0 Interval Value reached interrupt enable.

11.3.2. Sync Timer IRQ Status Register(Default: 0x00000000)

Offset: 0x04			Register Name: SYNC_TMR_IRQ_STAS_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	STMR1_IRQ_PEND.

			Sync Timer 1 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, timer 1 interval value is reached.
0	R/W	0x0	STMR0_IRQ_PEND. Sync Timer 0 IRQ Pending. Set 1 to the bit will clear it. 0: No effect 1: Pending, timer 0 interval value is reached.

11.3.3. Sync Timer 0 Control Register (Default: 0x00000004)

Offset: 0x10			Register Name: SYNC_TMR0_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SYNC_TMR0_TEST. Sync timer0 test mode. In test mode, the low register should be set to 0x1, the high register will down count. The counter needs to be reloaded. 0: normal mode 1: test mode.
30:8	/	/	/
7	R/W	0x0	STMR0_MODE. Sync Timer0 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically. Timer 0 Clock Source is fixed to AHBCLK.
6:4	R/W	0x0	STMR0_CLK_ Select the pre-scale of the sync timer 0 clock source. 000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	STMR0_RELOAD. Sync Timer 0 Reload. 0: No effect, 1: Reload timer 0 Interval value.
0	R/W	0x0	STMR0_EN. Sync Timer 0 Enable. 0: Stop/Pause 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to “0”; the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

11.3.4. Sync Timer 0 Interval Value Low Register

Offset: 0x14			Register Name: SYNC_TMR0_INTV_LO_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	STMR0_INTV_VALUE_LO. Sync Timer 0 Interval Value [31:0].

11.3.5. Sync Timer 0 Interval Value High Register

Offset: 0x18			Register Name: SYNC_TMR0_INTV_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	STMR0_INTV_VALUE_HI. Sync Timer 0 Interval Value [55:32].

Note: The interval value register is a 56-bit register. When read or write the interval value, the Low register should be read or write first. And the High register should be written after the Low register.

11.3.6. Sync Timer 0 Current Value Lo Register

Offset: 0x1C			Register Name: SYNC_TMR0_CURNT_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	STMR0_CUR_VALUE_LOW. Sync Timer 0 Current Value [31:0].

11.3.7. Sync Timer 0 Current Value Hi Register

Offset: 0x20			Register Name: SYNC_TMR0_CURNT_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	STMR0_CUR_VALUE_HI. Sync Timer 0 Current Value [55:32].

Note:
1. Timer 0 current value is a 56-bit down-counter (from interval value to 0).
2. The current value register is a 56-bit register. When read or write the current value, the Low register should be read or write first.

11.3.8. Sync Timer 1 Control Register (Default: 0x00000004)

Offset: 0x30			Register Name: SYNC_TMR1_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	SYNC_TMR1_TEST. Sync timer1 test mode. In test mode, the low register should be set to 0x1, the high register will down count. The counter needs to be reloaded. 0: normal mode, 1: test mode.
30:8	/	/	/
7	R/W	0x0	STMR1_MODE. Sync Timer1 mode. 0: Continuous mode. When reaches the internal value, the timer will not be disabled automatically. 1: Single mode. When reaches the internal value, the timer will be disabled automatically. Sync Timer 1 Clock Source is fixed to AHBCLK.
6:4	R/W	0x0	STMR1_CLK_SRC. Select the pre-scale of the sync timer 1 clock source.

			000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /
3:2	/	/	/
1	R/W	0x0	STMR1_RELOAD. Sync Timer 1 Reload. 0: No effect, 1: Reload timer 1 Interval value.
0	R/W	0x0	STMR1_EN. Sync Timer 1 Enable. 0: Stop/Pause, 1: Start. If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0. If the current counter does not reach the zero, the timer enable bit is set to "0"; the current value counter will pause. At least wait for 2 Tcylces, the start bit can be set to 1. In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.

11.3.9. Sync Timer 1 Interval Value Low Register

Offset: 0x34			Register Name: SYNC_TMR1_INTV_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	STMR1_INTV_VALUE_LOW. Sync Timer 1 Interval Value [31:0].

11.3.10. Sync Timer 1 Interval Value High Register

Offset: 0x38			Register Name: SYNC_TMR1_INTV_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	STMR1_INTV_VALUE_HI. Sync Timer 1 Interval Value [55:32].

Note: The interval value register is a 56-bit register. When read or write the interval value, the Low register should be read or write first. And the High register should be written after the Low register.

11.3.11. Sync Timer 1 Current Value Low Register

Offset: 0x3C			Register Name: SYNC_TMR1_CURNT_LOW_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	STMR1_CUR_VALUE_LOW. Sync Timer 1 Current Value [31:0].

11.3.12. Sync Timer 1 Current Value High Register

Offset: 0x40			Register Name: SYNC_TMR1_CURNT_HI_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/

23:0	R/W	x	STMR1_CUR_VALUE_HI. Sync Timer 1 Current Value [55:32].

Note: Timer 0 current value is a 56-bit down-counter (from interval value to 0). The current value register is a 56-bit register. When read or write the current value, the Low register should be read or written first.

Chapter 12 Interrupt Controller

12.1. Overview

The interrupt controller features:

- Control the nIRQ and FIQ of a RISC Processor
- Support 96 interrupt sources
- 4-Level Priority Controller
- External Sources of Edge-sensitive or Level-sensitive

The 4-level Priority Controller allows users to define the priority of each interrupt source, so higher priority interrupts can be serviced even if a lower priority interrupt is being treated.

12.2. Interrupt Source

The interrupt source 0 is always located at FIQ. The interrupt sources 1 to 63 are located at System Interrupt and user peripheral.

Interrupt Source	SRC	Vector	FIQ	Description
External NMI	0	0x0000	YES	External Non-Mask Interrupt. Power module battery/VDD/VDDIO/VDD18/VDD25 brownout detect
/	1	0x0004		/
UART 1	2	0x0008		UART 1 interrupt
/	3	0x000C		/
UART 3	4	0x0010		UART 3 interrupt
IR	5	0x0014		IR 0 interrupt
/	6	0x0018		/
TWI 0	7	0x001C		TWI 0 interrupt
TWI 1	8	0x0020		TWI 1 interrupt
TWI 2	9	0x0024		TWI 2 interrupt
SPI 0	10	0x0028		SPI 0 interrupt
SPI 1	11	0x002C		SPI 1 interrupt
SPI 2	12	0x0030		SPI 2 interrupt
/	13	0x0034		/
/	14	0x0038		/
/	15	0x003C		/
/	16	0x0040		/
/	17	0x0044		/
/	18	0x0048		/
/	19	0x004C		/
/	20	0x0050		/
/	21	0x0054		/
Timer 0	22	0x0058		Timer port 0
Timer 1	23	0x005C		Timer port 1
Timer 2/Alarm/WD	24	0x0060		Timer 2 , Alarm, Watchdog
Timer 3	25	0x0064		Timer 3 interrupt
/	26	0x0068		/

Interrupt Source	SRC	Vector	FIQ	Description
DMA	27	0x006C		DMA channel interrupt
PIO	28	0x0070		PIO interrupt
Touch Panel	29	0x0074		Touch Panel interrupt.
Audio Codec	30	0x0078		Analog Audio Codec interrupt
LRADC	31	0x007C		LRADC interrupt
SD/MMC 0	32	0x0080		SD/MMC Host Controller 0 interrupt
SD/MMC 1	33	0x0084		SD/MMC Host Controller 1 interrupt
SD/MMC 2	34	0x0088		SD/MMC Host Controller 2 interrupt
/	35	0x008C		/
/	36	0x0090		/
NAND	37	0x0094		NAND Flash Controller (NFC) interrupt
USB-OTG	38	0x0098		USB OTG wakeup, connect, disconnect interrupt
USB-EHCI	39	0x009C		USB EHCI wakeup, connect, disconnect interrupt
USB-OHCI	40	0x00A0		USB OHCI wakeup, connect, disconnect interrupt
/	41	0x00A4		/
CSI	42	0x00A8		CSI interrupt
/	43	0x00AC		/
LCD Controller	44	0x00B0		LCD Controller interrupt
/	45	0x00B4		/
/	46	0x00B8		/
DE-FE/DE-BE	47	0x00BC		DE-FE/DE-BE interrupt
/	48	0x00C0		/
PMU	49	0x00C4		PMU interrupt
/	50	0x00C8		/
/	51	0x00CC		/
/	52	0x00D0		/
VE	53	0x00D4		VE interrupt
CE	54	0x00D8		Crypto Engine interrupt
/	55	0x00DC		/
/	56	0x00E0		/
/	57	0x00E4		/
/	58	0x00E8		/
/	59	0x00EC		/
/	60	0x00F0		/
/	61	0x00F4		/
/	62	0x00F8		/
/	63	0x00FC		/
/	64	0x100		/
/	65	0x104		/
PLE/PERFMU	66	0x108		PLE on non-secure transfers interrupt PLE on secure transfer interrupt PLE error interrupt Performance monitor interrupt
Timer 4	67	0x010C		Timer 4 interrupt
Timer 5	68	0x0110		Timer 5 interrupt
GPU-GP	69	0x0114		
GPU-GPMMU	70	0x0118		
GPU-PP0	71	0x011C		
GPU-PPMMU0	72	0x0120		
GPU-PMU	73	0x0124		
GPU-RSV0	74	0x0128		
GPU-RSV1	75	0x012C		

Interrupt Source	SRC	Vector	FIQ	Description
GPU-RSV2	76	0x0130		
GPU-RSV3	77	0x0134		
GPU-RSV4	78	0x0138		
GPU-RSV5	79	0x013C		
GPU-RSV6	80	0x0140		
/	81	0x0144		
Sync timer 0	82	0x0148		
Sync timer 1	83	0x014C		

12.3. Interrupt Register List

Module Name	Base Address
INTC	0x01C20400

Register Name	Offset	Description
INTC_VECTOR_REG	0x0000	Interrupt Vector
INTC_BASE_ADDR_REG	0x0004	Interrupt Base Address
INC_PROTEC_REG	0x0008	Interrupt Protection
INTC_NMII_CTRL_REG	0x000C	Interrupt Control
INTC_IRQ_PEND_REG0	0x0010	Interrupt IRQ Pending 0 Status
INTC_IRQ_PEND_REG1	0x0014	Interrupt IRQ Pending 1 Status
INTC_IRQ_PEND_REG2	0x0018	Interrupt IRQ Pending 2 Status
/	0x001C	/
INTC_FIQ_PEND_REG0	0x0020	Interrupt FIQ Pending 0 Status
INTC_FIQ_PEND_REG1	0x0024	Interrupt FIQ Pending 1 Status
INTC_FIQ_PEND_REG2	0x0028	Interrupt FIQ Pending 2 Status
/	0x002C	/
INTC_SEL_REG0	0x0030	Interrupt Select 0
INTC_SEL_REG1	0x0034	Interrupt Select 1
INTC_SEL_REG2	0x0038	Interrupt Select 2
/	0x003C	/
INTC_EN_REG0	0x0040	Interrupt Enable 0
INTC_EN_REG1	0x0044	Interrupt Enable 1
INTC_EN_REG2	0x0048	Interrupt Enable 2
/	0x004C	/
INTC_MASK_REG0	0x0050	Interrupt Mask 0
INTC_MASK_REG1	0x0054	Interrupt Mask 1
INTC_MASK_REG2	0x0058	Interrupt Mask 2
/	0x005C	/
INTC_RESP_REG0	0x0060	Interrupt Response 0
INTC_RESP_REG1	0x0064	Interrupt Response 1
INTC_RESP_REG2	0x0068	Interrupt Response 2
/	0x006C	/
INTC_FORCE_REG0	0x0070	Interrupt Fast Forcing 0
INTC_FORCE_REG1	0x0074	Interrupt Fast Forcing 1
INTC_FORCE_REG2	0x0078	Interrupt Fast Forcing 2
/	0x007C	/

INTC_SRC_PRIO_REG0	0x0080	Interrupt Source Priority 0
INTC_SRC_PRIO_REG1	0x0084	Interrupt Source Priority 1
INTC_SRC_PRIO_REG2	0x0088	Interrupt Source Priority 2
INTC_SRC_PRIO_REG3	0x008C	Interrupt Source Priority 3
INTC_SRC_PRIO_REG4	0x0090	Interrupt Source Priority 4
INTC_SRC_PRIO_REG5	0x0094	Interrupt Source Priority 5

12.4. Interrupt Register Description

12.4.1. Interrupt Vector Register (Default: 0x00000000)

Offset:0x00			Register Name: INTC_VECTOR_REG
Bit	Read/Write	Default/Hex	Description
31:2	R	0x0	VECTOR_ADDR. This register present the vector address for the interrupt currently active on the CPU IRQ input.
1:0	R	0x0	ZERO. Always return zero to this field.

12.4.2. Interrupt Base Address Register (Default: 0x00000000)

Offset:0x04			Register Name: INTC_BASE_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:2	R/W	0x0	BASE_ADDR. This bit-field holds the upper 30 bits of the base address of the vector table.
1:0	R	0x0	ZERO. Always write zero to this bit-field.

12.4.3. Interrupt Protection Register (Default: 0x00000000)

Offset:0x08			Register Name: INC_PROTEC_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	PROTECT_EN. Enables or disables protected register access: 0: disable protection mode 1: enable protection mode If enabled, only privileged mode access can access the interrupt controller registers. If disabled, both user mode and privileged mode can access the registers. This register can only be accessed in privileged mode.

12.4.4. NMI Interrupt Control Register (Default: 0x00000000)

Offset:0x0C			Register Name: INTC_NMIl_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1:0	R/W	0x0	NMI_SRC_TYPE. External NMI Interrupt Source Type. 00 : Low level sensitive 01 : Negative edge trigged 10 : High level sensitive 11 : Positive edge sensitive

12.4.5. Interrupt IRQ Pending Register 0(Default: 0x00000000)

Offset:0x10			Register Name: INTC_IRQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_IRQ_SRC_PEND0. Interrupt IRQ Source [31:0] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

12.4.6. Interrupt IRQ Pending Register 1(Default: 0x00000000)

Offset:0x14			Register Name: INTC_PEND_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_IRQ_SRC_PEND1. Interrupt IRQ Source [63:32] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

12.4.7. Interrupt IRQ Pending Register 2(Default: 0x00000000)

Offset:0x18			Register Name: INTC_PEND_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_IRQ_SRC_PEND2. Interrupt IRQ Source [95:64] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

12.4.8. Interrupt FIQ Pending/Clear Register 0 (Default: 0x00000000)

Offset:0x20			Register Name: INTC_FIQ_PEND_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_FIQ_SRC_PEND0. Interrupt FIQ Source [31:0] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

12.4.9. Interrupt FIQ Pending/Clear Register 1(Default: 0x00000000)

Offset:0x24			Register Name: INTC_FIQ_PEND_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_FIQ_SRC_PEND1. Interrupt Source [63:32] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

12.4.10. Interrupt FIQ Pending/Clear Register 2(Default: 0x00000000)

Offset:0x28			Register Name: INTC_FIQ_PEND_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	INT_FIQ_SRC_PEND2. Interrupt Source [95:64] Pending/Clear Bit. 0: Corresponding interrupt is not pending. 1: Corresponding interrupt is pending

12.4.11. Interrupt Select Register 0(Default: 0x00000000)

Offset:0x30			Register Name: INTC_SEL_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_SRC_TYPE0 Interrupt Source [31:0] irq type select. 0: IRQ. 1: FIQ

12.4.12. Interrupt Select Register 1(Default: 0x00000000)

Offset:0x34			Register Name: INTC_SEL_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_SRC_TYPE1. Interrupt Source [63:32] irq type select. 0: IRQ. 1: FIQ

12.4.13. Interrupt Select Register 2(Default: 0x00000000)

Offset:0x38			Register Name: INTC_SEL_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_SRC_TYPE2. Interrupt Source [95:64] irq type select. 0: IRQ. 1: FIQ

12.4.14. Interrupt Enable Register 0(Default: 0x00000000)

Offset:0x40			Register Name: INTC_EN_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_SRC_EN0. Interrupt Source [31:0] Enable Bits. 0: Corresponding interrupt is disabled. 1: Corresponding interrupt is enabled.

12.4.15. Interrupt Enable Register 1(Default: 0x00000000)

Offset:0x44			Register Name: INTC_EN_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_SRC_EN1. Interrupt Source [63:32] Enable Bits. 0: Corresponding interrupt is disabled. 1: Corresponding interrupt is enabled.

12.4.16. Interrupt Enable Register 2(Default: 0x00000000)

Offset:0x48			Register Name: INTC_EN_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_SRC_EN2. Interrupt Source [95:64] Enable Bits. 0: Corresponding interrupt is disabled. 1: Corresponding interrupt is enabled.

12.4.17. Interrupt Mask Register 0(Default: 0x00000000)

Offset:0x50			Register Name: INTC_MASK_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_MASK0. Interrupt Source [31:0] Mask Bits. 0: No effect. 1: interrupt is masked. If interrupt is enabled and the interrupt occurred, the interrupt pending bit will be set whether the corresponding interrupt mask bit is set.

12.4.18. Interrupt Mask Register 1(Default: 0x00000000)

Offset:0x54			Register Name: INTC_MASK_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_MASK1. Interrupt Source [63:32] Mask Bits. 0: No effect. 1: interrupt is masked. If interrupt is enabled and the interrupt occurred, the interrupt pending bit will be set whether the corresponding interrupt mask bit is set.

12.4.19. Interrupt Mask Register 2(Default: 0x00000000)

Offset:0x58			Register Name: INTC_MASK_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_MASK2. Interrupt Source [95:64] Mask Bits. 0: No effect. 1: interrupt is masked. If interrupt is enabled and the interrupt occurred, the interrupt pending bit will be set whether the corresponding interrupt mask bit is set.

12.4.20. Interrupt Response Register 0(Default: 0x00000000)

Offset:0x60			Register Name: INTC_RESP_REG0
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_RESP0. Interrupt Source [31:0] response bit. If the corresponding bit is set, the interrupt with the lower or the same priority level is masked.

12.4.21. Interrupt Response Register 1(Default: 0x00000000)

Offset:0x64			Register Name: INTC_RESP_REG1
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_RESP1. Interrupt Source [63:32] response bit. If the corresponding bit is set, the interrupt with the lower or the same priority level is masked.

12.4.22. Interrupt Response Register 2(Default: 0x00000000)

Offset:0x68			Register Name: INTC_RESP_REG2
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	INT_RESP2. Interrupt Source [95:64] response bit. If the corresponding bit is set, the interrupt with the lower or the same priority level is masked.

12.4.23. Interrupt Fast Forcing Register 0(Default: 0x00000000)

Offset:0x70			Register Name: INTC_FORCE_REG0
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	INT_FF0 Enables the fast forcing feature on the corresponding interrupt source [31:0]. 0: No effect. 1: Forcing the corresponding interrupt. Setting this bit can be valid only when the corresponding interrupt enable bit is set.

12.4.24. Interrupt Fast Forcing Register 1(Default: 0x00000000)

Offset:0x74			Register Name: INTC_FORCE_REG1
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	INT_FF1. Enables the fast forcing feature on the corresponding interrupt source [63:32]. 0: No effect. 1: Forcing the corresponding interrupt. Setting this bit can be valid only when the corresponding interrupt enable bit is set.

12.4.25. Interrupt Fast Forcing Register 2(Default: 0x00000000)

Offset:0x78			Register Name: INTC_FORCE_REG2
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	INT_FF2. Enables the fast forcing feature on the corresponding interrupt source [95:64]. 0: No effect. 1: Forcing the corresponding interrupt. Setting this bit can be valid only when the corresponding interrupt enable bit is set.

12.4.26. Interrupt Source Priority 0 Register (Default: 0x00000000)

Offset:0x80			Register Name: INTC_SRC_PRIO_REG0
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	IRQ15_PRIO. IRQ 15 Priority. Set priority level for IRQ bit 15 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority

Offset:0x80			Register Name: INTC_SRC_PRIO_REG0
29:28	R/W	0x0	IRQ14_PRIO. IRQ 14 Priority. Set priority level for IRQ bit 14 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
27:26	R/W	0x0	IRQ13_PRIO. IRQ 13 Priority. Set priority level for IRQ bit 13 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
25:24	R/W	0x0	IRQ12_PRIO. IRQ 12 Priority. Set priority level for IRQ bit 12 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
23:22	R/W	0x0	IRQ11_PRIO. IRQ 11 Priority. Set priority level for IRQ bit 11 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
21:20	R/W	0x0	IRQ10_PRIO. IRQ 10 Priority. Set priority level for IRQ bit 10 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
19:18	R/W	0x0	IRQ9_PRIO. IRQ 9 Priority. Set priority level for IRQ bit 9 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
17:16	R/W	0x0	IRQ8_PRIO. IRQ 8 Priority. Set priority level for IRQ bit 8 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
15:14	R/W	0x0	IRQ7_PRIO. IRQ 7 Priority. Set priority level for IRQ bit 7 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2

Offset:0x80			Register Name: INTC_SRC_PRIO_REG0
			Level3 = 0x3 level 3, highest priority
13:12	R/W	0x0	IRQ6_PRIO. IRQ 6 Priority. Set priority level for IRQ bit 6 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
11:10	R/W	0x0	IRQ5_PRIO. IRQ 5 Priority. Set priority level for IRQ bit 5 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
9:8	R/W	0x0	IRQ4_PRIO. IRQ 4 Priority. Set priority level for IRQ 4 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x2 level 2 Level3 = 0x3 level 3, highest priority
7:6	R/W	0x0	IRQ3_PRIO. IRQ 3 Priority. Set priority level for IRQ bit 3 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
5:4	R/W	0x0	IRQ2_PRIO. IRQ 2 Priority. Set priority level for IRQ bit 2 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
3:2	R/W	0x0	IRQ1_PRIO. IRQ 1 Priority. Set priority level for IRQ bit 1 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
1:0	/	/	/

Note:Programs the priority level for all sources except FIQ source (source 0).The priority level ranges from 0(lowest) to 7(highest).

12.4.27. Interrupt Source Priority 1 Register (Default: 0x00000000)

Offset:0x84			Register Name: INTC_SRC_PRIO_REG1
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	IRQ31_PRIO. IRQ 31 Priority. Set priority level for IRQ bit 31

Offset:0x84			Register Name: INTC_SRC_PRIO_REG1
			Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
29:28	R/W	0x0	IRQ30_PRIO. IRQ 30 Priority. Set priority level for IRQ bit 30 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
27:26	R/W	0x0	IRQ29_PRIO. IRQ 29 Priority. Set priority level for IRQ bit 29 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
25:24	R/W	0x0	IRQ28_PRIO. IRQ 28 Priority. Set priority level for IRQ bit 28 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
23:22	R/W	0x0	IRQ27_PRIO. IRQ 27 Priority. Set priority level for IRQ bit 27 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
21:20	R/W	0x0	IRQ26_PRIO. IRQ 26 Priority. Set priority level for IRQ bit 26 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
19:18	R/W	0x0	IRQ25_PRIO. IRQ 25 Priority. Set priority level for IRQ bit 25 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
17:16	R/W	0x0	IRQ24_PRIO. IRQ 24 Priority. Set priority level for IRQ bit 24 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
15:14	R/W	0x0	IRQ23_PRIO. IRQ 23 Priority.

Offset:0x84			Register Name: INTC_SRC_PRIO_REG1
			Set priority level for IRQ bit 23 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
13:12	R/W	0x0	IRQ22_PRIO. IRQ 22 Priority. Set priority level for IRQ bit 22 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
11:10	R/W	0x0	IRQ21_PRIO. IRQ 21 Priority. Set priority level for IRQ bit 21 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
9:8	R/W	0x0	IRQ20_PRIO. IRQ 20 Priority. Set priority level for IRQ bit 20 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
7:6	R/W	0x0	IRQ19_PRIO. IRQ 19 Priority. Set priority level for IRQ bit 19 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
5:4	R/W	0x0	IRQ18_PRIO. IRQ 18 Priority. Set priority level for IRQ bit 18 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
3:2	R/W	0x0	IRQ17_PRIO. IRQ 17 Priority. Set priority level for IRQ bit 17 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
1:0	R/W	0x0	IRQ16_PRIO. IRQ 16 Priority. Set priority level for IRQ bit 16 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority

12.4.28. Interrupt Source Priority 2 Register (Default: 0x00000000)

Offset:0x88			Register Name: INTC_SRC_PRIO_REG2
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	IRQ47_PRIO. IRQ 47 Priority. Set priority level for IRQ bit 47 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
29:28	R/W	0x0	IRQ46_PRIO. IRQ 46 Priority. Set priority level for IRQ bit 46 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
27:26	R/W	0x0	IRQ45_PRIO. IRQ 45 Priority. Set priority level for IRQ bit 45 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
25:24	R/W	0x0	IRQ44_PRIO. IRQ 44 Priority. Set priority level for IRQ bit 44 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
23:22	R/W	0x0	IRQ43_PRIO. IRQ 43 Priority. Set priority level for IRQ bit 43 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
21:20	R/W	0x0	IRQ42_PRIO. IRQ 42 Priority. Set priority level for IRQ bit 42 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
19:18	R/W	0x0	IRQ41_PRIO. IRQ 41 Priority. Set priority level for IRQ bit 41 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
17:16	R/W	0x0	IRQ40_PRIO. IRQ 40 Priority. Set priority level for IRQ bit 40 Level0 = 0x0 level 0, lowest priority

Offset:0x88			Register Name: INTC_SRC_PRIO_REG2
			Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
15:14	R/W	0x0	IRQ39_PRIO. IRQ 39 Priority. Set priority level for IRQ bit 39 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
13:12	R/W	0x0	IRQ38_PRIO. IRQ 38 Priority. Set priority level for IRQ bit 38 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
11:10	R/W	0x0	IRQ37_PRIO. IRQ 37 Priority. Set priority level for IRQ bit 37 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
9:8	R/W	0x0	IRQ36_PRIO. IRQ 36 Priority. Set priority level for IRQ bit 36 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
7:6	R/W	0x0	IRQ35_PRIO. IRQ 35 Priority. Set priority level for IRQ bit 35 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
5:4	R/W	0x0	IRQ34_PRIO. IRQ 34 Priority. Set priority level for IRQ bit 34 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
3:2	R/W	0x0	IRQ33_PRIO. IRQ 33 Priority. Set priority level for IRQ bit 33 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
1:0	R/W	0x0	IRQ32_PRIO. IRQ 32 Priority. Set priority level for IRQ bit 32

Offset:0x88			Register Name: INTC_SRC_PRIO_REG2
			Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority

12.4.29. Interrupt Source Priority 3 Register (Default: 0x00000000)

Offset:0x8C			Register Name: INTC_SRC_PRIO_REG3
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	IRQ63_PRIO. IRQ 63 Priority. Set priority level for IRQ bit 63 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
29:28	R/W	0x0	IRQ62_PRIO. IRQ 62 Priority. Set priority level for IRQ bit 62 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
27:26	R/W	0x0	IRQ61_PRIO. IRQ 61 Priority. Set priority level for IRQ bit 61 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
25:24	R/W	0x0	IRQ60_PRIO. IRQ 60 Priority. Set priority level for IRQ bit 60 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
23:22	R/W	0x0	IRQ59_PRIO. IRQ 59 Priority. Set priority level for IRQ bit 59 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
21:20	R/W	0x0	IRQ58_PRIO. IRQ 58 Priority. Set priority level for IRQ bit 58 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
19:18	R/W	0x0	IRQ57_PRIO. IRQ 57 Priority. Set priority level for IRQ bit 57 Level0 = 0x0 level 0, lowest priority

Offset:0x8C			Register Name: INTC_SRC_PRIO_REG3
			Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
17:16	R/W	0x0	IRQ56_PRIO. IRQ 56 Priority. Set priority level for IRQ bit 56 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
15:14	R/W	0x0	IRQ55_PRIO. IRQ 55 Priority. Set priority level for IRQ bit 55 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
13:12	R/W	0x0	IRQ54_PRIO. IRQ 54 Priority. Set priority level for IRQ bit 54 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
11:10	R/W	0x0	IRQ53_PRIO. IRQ 53 Priority. Set priority level for IRQ bit 53 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
9:8	R/W	0x0	IRQ52_PRIO. IRQ 52 Priority. Set priority level for IRQ bit 52 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
7:6	R/W	0x0	IRQ51_PRIO. IRQ 51 Priority. Set priority level for IRQ bit 51 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
5:4	R/W	0x0	IRQ50_PRIO. IRQ 50 Priority. Set priority level for IRQ bit 50 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
3:2	R/W	0x0	IRQ49_PRIO. IRQ 49 Priority. Set priority level for IRQ bit 49

Offset:0x8C			Register Name: INTC_SRC_PRIO_REG3
			Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
1:0	R/W	0x0	IRQ48_PRIO. IRQ 48 Priority. Set priority level for IRQ bit 48 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority

12.4.30. Interrupt Source Priority 4 Register (Default: 0x00000000)

Offset:0x90			Register Name: INTC_SRC_PRIO_REG4
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	IRQ79_PRIO. IRQ 79 Priority. Set priority level for IRQ bit 79 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
29:28	R/W	0x0	IRQ78_PRIO. IRQ 78 Priority. Set priority level for IRQ bit 78 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
27:26	R/W	0x0	IRQ77_PRIO. IRQ 77 Priority. Set priority level for IRQ bit 77 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
25:24	R/W	0x0	IRQ76_PRIO. IRQ 76 Priority. Set priority level for IRQ bit 76 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
23:22	R/W	0x0	IRQ75_PRIO. IRQ 75 Priority. Set priority level for IRQ bit 75 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
21:20	R/W	0x0	IRQ74_PRIO. IRQ 74 Priority. Set priority level for IRQ bit 74 Level0 = 0x0 level 0, lowest priority

Offset:0x90			Register Name: INTC_SRC_PRIO_REG4
			Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
19:18	R/W	0x0	IRQ73_PRIO. IRQ 73 Priority. Set priority level for IRQ bit 73 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
17:16	R/W	0x0	IRQ72_PRIO. IRQ 72 Priority. Set priority level for IRQ bit 72 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
15:14	R/W	0x0	IRQ71_PRIO. IRQ 71 Priority. Set priority level for IRQ bit 71 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
13:12	R/W	0x0	IRQ70_PRIO. IRQ 70 Priority. Set priority level for IRQ bit 70 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
11:10	R/W	0x0	IRQ69_PRIO. IRQ 69 Priority. Set priority level for IRQ bit 69 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
9:8	R/W	0x0	IRQ68_PRIO. IRQ 68 Priority. Set priority level for IRQ bit 68 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
7:6	R/W	0x0	IRQ67_PRIO. IRQ 67 Priority. Set priority level for IRQ bit 67 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
5:4	R/W	0x0	IRQ66_PRIO. IRQ 66 Priority. Set priority level for IRQ bit 66

Offset:0x90			Register Name: INTC_SRC_PRIO_REG4
			Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
3:2	R/W	0x0	IRQ65_PRIO. IRQ 65 Priority. Set priority level for IRQ bit 65 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
1:0	R/W	0x0	IRQ64_PRIO. IRQ 64 Priority. Set priority level for IRQ bit 64 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority

12.4.31. Interrupt Source Priority 5 Register (Default: 0x00000000)

Offset:0x94			Register Name: INTC_SRC_PRIO_REG5
Bit	Read/Write	Default/Hex	Description
31:30	R/W	0x0	IRQ95_PRIO. IRQ 95 Priority. Set priority level for IRQ bit 95 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
29:28	R/W	0x0	IRQ94_PRIO. IRQ 94 Priority. Set priority level for IRQ bit 94 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
27:26	R/W	0x0	IRQ93_PRIO. IRQ 93 Priority. Set priority level for IRQ bit 93 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
25:24	R/W	0x0	IRQ92_PRIO. IRQ 92 Priority. Set priority level for IRQ bit 92 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
23:22	R/W	0x0	IRQ91_PRIO. IRQ 91 Priority. Set priority level for IRQ bit 91 Level0 = 0x0 level 0, lowest priority

Offset:0x94			Register Name: INTC_SRC_PRIO_REG5
			Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
21:20	R/W	0x0	IRQ90_PRIO. IRQ 90 Priority. Set priority level for IRQ bit 90 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
19:18	R/W	0x0	IRQ89_PRIO. IRQ 89 Priority. Set priority level for IRQ bit 89 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
17:16	R/W	0x0	IRQ88_PRIO. IRQ 88 Priority. Set priority level for IRQ bit 88 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
15:14	R/W	0x0	IRQ87_RPIO. IRQ 87 Priority. Set priority level for IRQ bit 87 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
13:12	R/W	0x0	IRQ86_RPIO. IRQ 86 Priority. Set priority level for IRQ bit 86 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
11:10	R/W	0x0	IRQ85_PRIO. IRQ 85 Priority. Set priority level for IRQ bit 85 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
9:8	R/W	0x0	IRQ84_PRIO. IRQ 84 Priority. Set priority level for IRQ bit 84 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
7:6	R/W	0x0	IRQ83_PRIO. IRQ 83 Priority. Set priority level for IRQ bit 83

Offset:0x94			Register Name: INTC_SRC_PRIO_REG5
			Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
5:4	R/W	0x0	IRQ82_PRIO. IRQ 82 Priority. Set priority level for IRQ bit 82 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
3:2	R/W	0x0	IRQ81_PRIO. IRQ 81 Priority. Set priority level for IRQ bit 81 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority
1:0	R/W	0x0	IRQ80_PRIO. IRQ 80 Priority. Set priority level for IRQ bit 80 Level0 = 0x0 level 0, lowest priority Level1 = 0x1 level 1 Level2 = 0x1 level 2 Level3 = 0x1 level 3, highest priority

Chapter 13 DMA

13.1. Overview

There are two kinds of DMA in the chip. One is Normal DMA (NDMA) with 8 channels, and the other is Dedicated DMA (DDMA) with 8 channels.

For NDMA, only one channel can be active and the sequence is in accordance with the priority level. For DDMA, at most 8 channels can be active at the same time if their source or destination does not conflict.

13.2. DMA Description

DMA can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned.

13.3. DMA Register List

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_IRQ_EN_REG	0x0000	DMA IRQ Enable
DMA_IRQ_PEND_STAS_REG	0x0004	DMA IRQ Pending Status
NDMA_CTRL_REG	0x100+N*0x20	Normal DMA Configuration (N=0,1,2,3,4,5,6,7)
NDMA_SRC_ADDR_REG	0x100+N*0x20+4	Normal DMA Source Address
NDMA_DEST_ADDR_REG	0x100+N*0x20+8	Normal DMA Destination Address
NDMA_BC_REG	0x100+N*0x20+C	Normal DMA Byte Counter
DDMA_CFG_REG	0x300+N*0x20	Dedicated DMA Configuration (N=0,1,2,3,4,5,6,7)
DDMA_SRC_ADDR_REG	0x300+N*0x20+4	Dedicated DMA Source Start Address
DDMA_DEST_ADDR_REG	0x300+N*0x20+8	Dedicated DMA Destination Start Address
DDMA_BC_REG	0x300+N*0x20+C	Dedicated DMA Byte Counter
DDMA_PARA_REG	0x300+N*0x20+0x18	Dedicated DMA Parameter

13.4. DMA Register Description

13.4.1. DMA IRQ Enable Register (Default: 0x00000000)

Offset: 0x00			Register Name: DMA_IRQ_EN_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DDMA7_END_IRQ_EN. Dedicated DMA 7 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
30	R/W	0x0	DDMA7_HF_IRQ_EN.

			Dedicated DMA 7 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
29	R/W	0x0	DDMA6_END_IRQ_EN. Dedicated DMA 6 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
28	R/W	0x0	DDMA6_HF_IRQ_EN. Dedicated DMA 6 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
27	R/W	0x0	DDMA5_END_IRQ_EN. Dedicated DMA 5 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
26	R/W	0x0	DDMA5_HF_IRQ_EN. Dedicated DMA 5 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
25	R/W	0x0	DDMA4_END_IRQ_EN. Dedicated DMA 4 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
24	R/W	0x0	DDMA4_HF_IRQ_EN. Dedicated DMA 4 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
23	R/W	0x0	DDMA3_END_IRQ_EN. Dedicated DMA 3 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
22	R/W	0x0	DDMA3_HF_IRQ_EN. Dedicated DMA 3 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
21	R/W	0x0	DDMA2_END_IRQ_EN. Dedicated DMA 2 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
20	R/W	0x0	DDMA2_HF_IRQ_EN. Dedicated DMA 2 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
19	R/W	0x0	DDMA1_END_IRQ_EN. Dedicated DMA 1 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
18	R/W	0x0	DDMA1_HF_IRQ_EN. Dedicated DMA 1 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
17	R/W	0x0	DDMA0_END_IRQ_EN. Dedicated DMA 0 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
16	R/W	0x0	DDMA0_HF_IRQ_EN. Dedicated DMA 0 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
15	R/W	0x0	NDMA7_END_IRQ_EN. Normal DMA 7 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
14	R/W	0x0	NDMA7_HF_IRQ_EN. Normal DMA 7 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
13	R/W	0x0	NDMA6_END_IRQ_EN. Normal DMA 6 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
12	R/W	0x0	NDMA6_HF_IRQ_EN. Normal DMA 6 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.

11	R/W	0x0	NDMA5_END_IRQ_EN. Normal DMA 5 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
10	R/W	0x0	NDMA5_HF_IRQ_EN. Normal DMA 5 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
9	R/W	0x0	NDMA4_END_IRQ_EN. Normal DMA 4 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
8	R/W	0x0	NDMA4_HF_IRQ_EN. Normal DMA 4 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
7	R/W	0x0	NDMA3_END_IRQ_EN. Normal DMA 3 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
6	R/W	0x0	NDMA3_HF_IRQ_EN. Normal DMA 3 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
5	R/W	0x0	NDMA2_END_IRQ_EN. Normal DMA 2 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
4	R/W	0x0	NDMA2_HF_IRQ_EN. Normal DMA 2 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
3	R/W	0x0	NDMA1_END_IRQ_EN. Normal DMA 1 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
2	R/W	0x0	NDMA1_HF_IRQ_EN. Normal DMA 1 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	NDMA0_END_IRQ_EN. Normal DMA 0 End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	NDMA0_HF_IRQ_EN. Normal DMA 0 Half Transfer Interrupt Enable. 0: Disable, 1: Enable.

13.4.2. DMA IRQ Pending Status Register (Default: 0x00000000)

Offset: 0x04			Register Name: DMA_IRQ_PEND_STAS_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DDMA7_END_IRQ_PEND. Dedicated DMA 7 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
30	R/W	0x0	DDMA7_HF_IRQ_PEND. Dedicated DMA 7 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
29	R/W	0x0	DDMA6_END_IRQ_PEND. Dedicated DMA 6 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
28	R/W	0x0	DDMA6_HF_IRQ_PEND. Dedicated DMA 6 Half Transfer Interrupt Pending. Set 1 to the bit will clear it.

			0: No effect, 1: Pending.
27	R/W	0x0	DDMA5_END_IRQ_PEND. Dedicated DMA 5 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
26	R/W	0x0	DDMA5_HF_IRQ_PEND. Dedicated DMA 5 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
25	R/W	0x0	DDMA4_END_IRQ_PEND. Dedicated DMA 4 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
24	R/W	0x0	DDMA4_HF_IRQ_PEND. Dedicated DMA 4 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
23	R/W	0x0	DDMA3_END_IRQ_PEND. Dedicated DMA 3 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
22	R/W	0x0	DDMA3_HF_IRQ_PEND. Dedicated DMA 3 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
21	R/W	0x0	DDMA2_END_IRQ_PEND. Dedicated DMA 2 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
20	R/W	0x0	DDMA2_HF_IRQ_PEND. Dedicated DMA 2 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
19	R/W	0x0	DDMA1_END_IRQ_PEND. Dedicated DMA 1 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
18	R/W	0x0	DDMA1_HF_IRQ_PEND. Dedicated DMA 1 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
17	R/W	0x0	DDMA0_END_IRQ_PEND. Dedicated DMA 0 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
16	R/W	0x0	DDMA0_HF_IRQ_PEND. Dedicated DMA 0 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
15	R/W	0x0	NDMA7_END_IRQ_PEND. Normal DMA 7 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
14	R/W	0x0	NDMA7_HF_IRQ_PEND. Normal DMA 7 Half Transfer Interrupt Pending. Set 1 to the bit will clear it.

			0: No effect, 1: Pending.
13	R/W	0x0	NDMA6_END_IRQ_PEND. Normal DMA 6 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
12	R/W	0x0	NDMA6_HF_IRQ_PEND. Normal DMA 6 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
11	R/W	0x0	NDMA5_END_IRQ_PEND. Normal DMA 5 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
10	R/W	0x0	NDMA5_HF_IRQ_PEND. Normal DMA 5 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
9	R/W	0x0	NDMA4_END_IRQ_PEND. Normal DMA 4 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
8	R/W	0x0	NDMA4_HF_IRQ_PEND. Normal DMA 4 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
7	R/W	0x0	NDMA3_END_IRQ_PEND. Normal DMA 3 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
6	R/W	0x0	NDMA3_HF_IRQ_PEND. Normal DMA 3 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
5	R/W	0x0	NDMA2_END_IRQ_PEND. Normal DMA 2 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
4	R/W	0x0	NDMA2_HF_IRQ_PEND. Normal DMA 2 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
3	R/W	0x0	NDMA1_END_IRQ_PEND. Normal DMA 1 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
2	R/W	0x0	NDMA1_HF_IRQ_PEND. Normal DMA 1 Half Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W	0x0	NDMA0_END_IRQ_PEND. Normal DMA 0 End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W	0x0	NDMA0_HF_IRQ_PEND. Normal DMA 0 Half Transfer Interrupt Pending. Set 1 to the bit will clear it.

			0: No effect, 1: Pending.

13.4.3. Normal DMA Configuration Register (Default: 0x00000000) (N=0:7)

Offset: 0x100+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	NDMA_LOAD. DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finishes. It will be cleared automatically. Set 0 to the bit will reset the corresponding DMA channel.
30	R/W	0x0	NDMA_CONTI_EN. DMA Continuous Mode Enable. 0: Disable, 1: Enable.
29:27	R/W	0x0	NDMA_WAIT_STATE. DMA Wait State. 0: wait for 0 DMA clock to request, … 7: wait for 2(n+1) DMA clock to request.
26:25	R/W	0x0	NDMA_DST_DATA_WIDTH. Normal DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
24:23	R/W	0x0	NDMA_DST_BST_LEN. DMA Destination Burst Length. 00: 1, 01: 4 10: 8 11: /
22	/	/	/
21	R/W	0x0	NDMA_DST_ADDR_TYPE. Normal DMA Destination Address Type. 0: Increment 1: No Change.
20:16	R/W	0x0	NDMA_DST_DRQ_TYPE. Normal DMA Destination DRQ Type. 00000 : IR-TX 00001 : / 00010 : / 00011 : / 00100 : / 00101 : / 00110 : / 00111 : / 01000 : / 01001 : UART1 TX 01010 : / 01011 : UART3 TX 01100 : / 01101 : / 01110 : / 01111 : /

			10000 : / 10001 : / 10010 : / 10011 : Audio Codec D/A 10100 : / 10101 : SRAM(range :) 10110 : SDRAM 10111 : / 11000 : SPI0 TX 11001 : SPI1 TX 11010 : SPI2 TX 11011 : USB EP1 11100 :USB EP2 11101 :USB EP3 11110 :USB EP4 11111 :USB EP5
15	R/W	0x0	BC_MODE_SEL. BC mode select. 0 : normal mode(the value read back equals to the value that is written) 1: remain mode (the value read back equals to the remain counter to be transferred).
14:10	/	/	/
10:9	R/W	0x0	NDMA_SRC_DATA_WIDTH. Normal DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
8:7	R/W	0x0	NDMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: 4 10: 8 11: /.
6	/	/	/
5	R/W	0x0	NDMA_SRC_ADDR_TYPE. Normal DMA Source Address Type. 0: Increment 1: No Change
4:0	R/W	0x0	NDMA_SRC_DRQ_TYPE. Normal DMA Source DRQ Type. 00000 : IR-RX 00001 : / 00010 : / 00011 : / 00100 : / 00101 : / 00110 : 00111 : / 01000 : / 01001 : UART1 RX 01010 : / 01011 : UART3 RX 01100 : / 01101 : /

			01110 : / 01111 : / 10000 : / 10001 : / 10010 : / 10011 : Audio Codec A/D 10100 : / 10101 : SRAM(range :) 10110 : SDRAM 10111 : TP A/D 11000 : SPI0 RX 11001 : SPI1 RX 11010 : SPI2 RX 11011 : USB EP1 11100 :USB EP2 11101 :USB EP3 11110 :USB EP4 11111 :USB EP5

13.4.4. Normal DMA Source Address Register (Default: 0x00000000)

Offset: 0x100+N*0x20+0x4 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_SRC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	NDMA_SRC_ADDR. Normal DMA Source Address.

13.4.5. Normal DMA Destination Address Register (Default: 0x00000000)

Offset: 0x100+N*0x20+0x8 (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_DEST_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	NDMA_DST_ADDR. Normal DMA Destination Address.

13.4.6. Normal DMA Byte Counter Register (Default: 0x00000000)

Offset: 0x100+N*0x20+0xC (N=0,1,2,3,4,5,6,7)			Register Name: NDMA_BC_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	x	NDMA_BC. Normal DMA Byte Counter.

Note: If ByteCounter=0, DMA will transfer no byte. The maximum value is 128k.

13.4.7. Dedicated DMA Configuration Register (Default: 0x00000000)

Offset: 0x300+N*0x20 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_CFG_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DDMA_LOAD. DMA Loading. If set to 1, DMA will start and load the DMA registers to the shadow registers. The bit will hold on until the DMA finishes. It will be cleared

			automatically. Set 0 to the bit will stop the corresponding DMA channel and reset its state machine.
30	R	0x0	DDMA_BSY_STA. DMA Busy Status. 0: DMA idle 1: DMA busy.
29	R/W	0x0	DDMA_CONTI_MODE_EN. DMA Continuous Mode Enable. 0: Disable, 1: Enable.
28	/	/	/
27	/	/	/
26:25	R/W	0x0	DDMA_DST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
24:23	R/W	0x0	DDMA_DST_BST_LEN. DMA Destination Burst Length. 00: 1, 01: 4. 10: 8 11: /
22:21	R/W	0x0	DDMA_ADDR_MODE. DMA Destination Address Mode DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: Horizontal Page Mode 0x3: Vertical Page Mode
20:16	R/W	0x0	DDMA_DST_DRQ_SEL. Dedicated DMA Destination DRQ Type 0x0: SRAM memory 0x1: SDRAM memory 0x2: / 0x3: NAND Flash Controller (NFC) 0x4: USB0 0x5: / 0x6: / 0x7: / 0x8: SPI1 TX 0x9: / 0xA: Crypto Engine TX 0xB: / 0xC: / 0xD: / 0xE: TCON0 0xF: / 0x10: / 0x11: / 0x12: / 0x13: / 0x14: / 0x15: / 0x16: /

			0x17: / 0x18: / 0x19: / 0x1A: SPI0 TX 0x1B: /. 0x1C: SPI2 TX 0x1D: / 0x1E: / 0x1F: /
15	R/W	0x0	BC_MODE_SEL. BC mode select. 0 : normal mode(the value read back equals to the value that is written) 1: remain mode (the value read back equals to the remain counter to be transferred).
14:11	/	/	/
10:9	R/W	0x0	DDMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
8:7	R/W	0x0	DDMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: 4 10: 8 11: /
6:5	R/W	0x0	DDMA_SRC_ADDR_MODE. DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: Horizontal Page Mode 0x3: Vertical Page Mode
4:0	R/W	0x0	DDMA_SRC_DRQ_TYPE. Dedicated DMA Source DRQ Type 0x0: SRAM memory 0x1: SDRAM memory 0x2: / 0x3: NAND Flash Controller (NFC) 0x4: USB0 0x5: / 0x6: / 0x7: / 0x8: / 0x9: SPI1 RX 0xA: / 0xB: Crypto Engine RX 0xC: / 0xD: / 0xE: / 0xF: / 0x10: / 0x11: / 0x12: / 0x13: /

			0x14: / 0x15: / 0x16: / 0x17: / 0x18: / 0x19: / 0x1A: / 0x1B: SPI0 RX. 0x1C: / 0x1D: SPI2 RX 0x1E: / 0x1F: /

13.4.8. Dedicated DMA Source Start Address Register (N=0:7)

Offset: 0x300+N*0x20+0x4 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_SRC_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	DDMA_SRC_START_ADDR. Dedicated DMA Source Start Address.

13.4.9. Dedicated DMA Destination Start Address Register (N=0:7)

Offset: 0x300+N*0x20+0x8 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_DEST_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	x	DDMA_DST_START_ADDR. Dedicated DMA Destination Start Address.

13.4.10. Dedicated DMA Byte Counter Register (N=0:7)

Offset: 0x300+N*0x20+0Xc (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_BC_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R/W	x	DDMA_BC. Dedicated DMA Byte Counter.

Note: If ByteCounter=0, DMA will transfer no byte. The maximum value is 0x1000000.

13.4.11. Dedicated DMA Parameter Register

Offset: 0x300+N*0x20+0x18 (N=0,1,2,3,4,5,6,7)			Register Name: DDMA_PARA_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	DEST_DATA_BLK_SIZE. Destination Data Block Size n.
23:16	R/W	0x0	DEST_WAIT_CLK_CYC. Destination Wait Clock Cycles n
15:8	R/W	0x0	SRC_DATA_BLK_SIZE. Source Data Block Size n.
7:0	R/W	x	SRC_WAIT_CLK_CYC. Source Wait Clock Cycles n.

Note: If the counter is N, the value is N+1.

Chapter 14 NAND Flash

14.1. Overview

The NFC supports all NAND/MLC flash memory available in the market and new types can be supported by software re-configuration as well. It can support 2 NAND flash. There are 2 separate chip select lines (CE#) to connect up to 2 flash chips with2 R/B signals.

The On-the-fly error correction code (ECC) is built in NFC to enhance reliability. BCH is implemented to detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control to read or write external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kinds of modes are supported for serial read access: Mode 0 is the conventional serial access, Mode 1 for EDO type, and Mode 2 is for extension EDO type. In addition, NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NFC features:

- Support SLC/MLC/TLC flash and EF-NAND memory
- Software configure seed to randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Support 8-bit Data Bus Width
- Support 1024, 2048, 4096, 8192, 16384 bytes size per page
- Up to 2 flash chips which are controlled by NFC_CEx#
- Support Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NFC status information is reported by its registers
- Support interrupt
- One Command FIFO
- Support external DMA for data transfer
- Two 256x32-bit RAM for Pipeline Procession
- Support SDR, DDR and Toggle 1.0 NAND

14.2. NFC Block Diagram

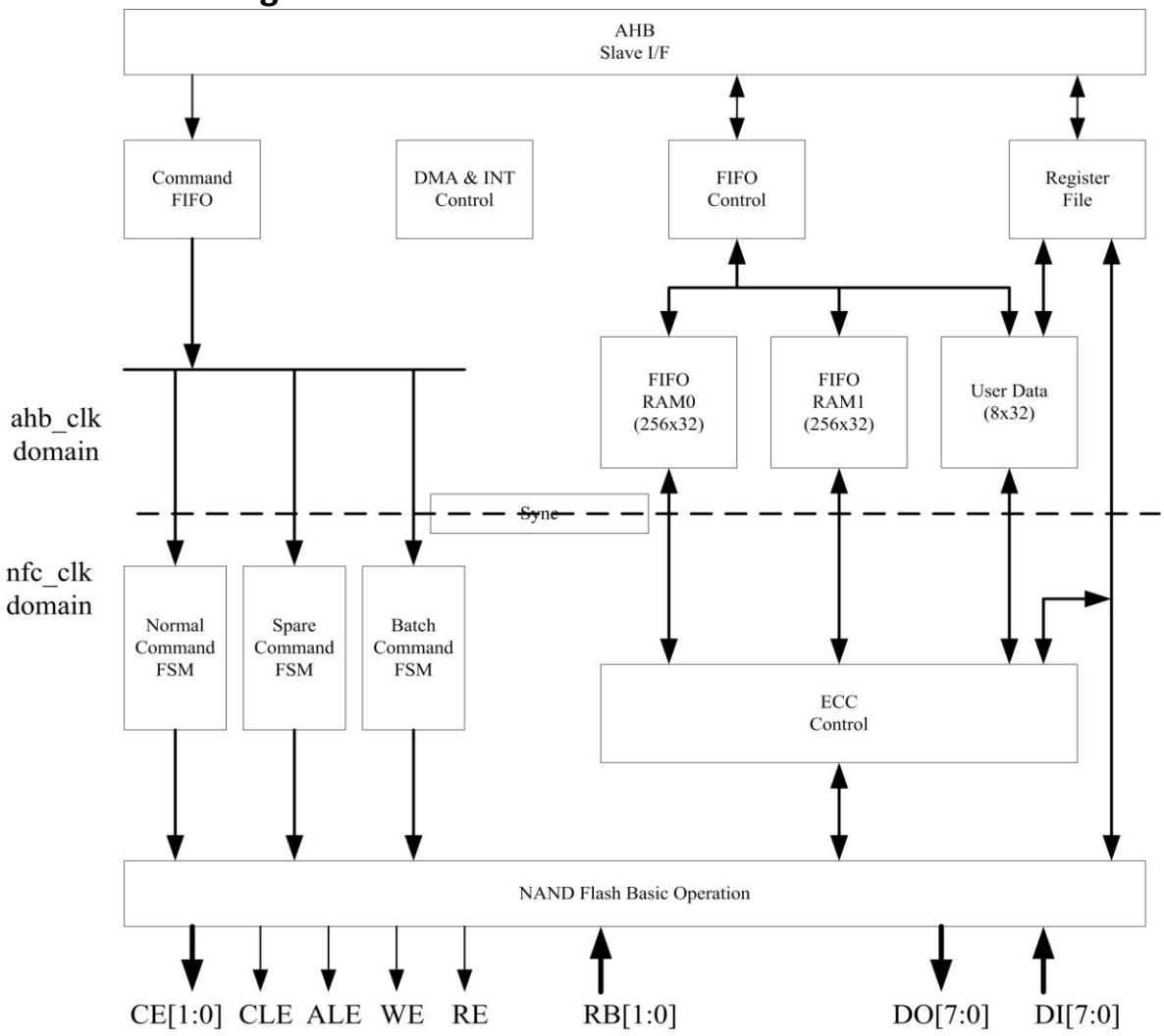


Figure 14-1. NFC Block Diagram

14.3. NFC Timing Diagram

Typically, there are two kinds of serial access method. One is the conventional method that fetches data at the rise edge of NFC_RE# signal line, and the other is EDO type that fetches data at the next fall edge of NFC_RE# signal line.

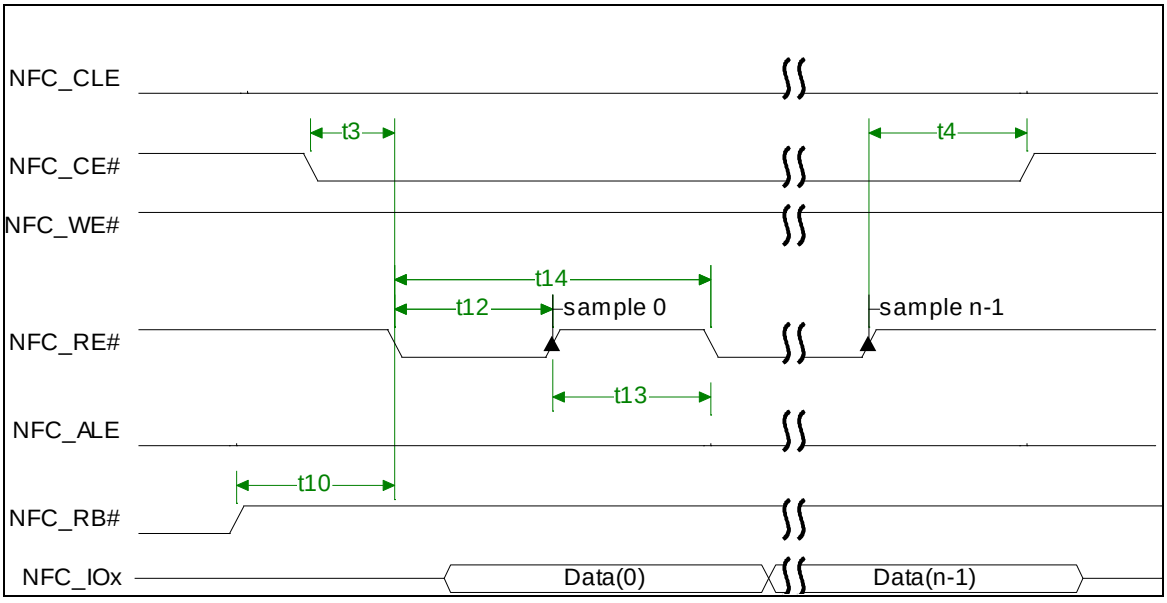


Figure 14-2. Conventional Serial Access Cycle Diagram (SAM0)

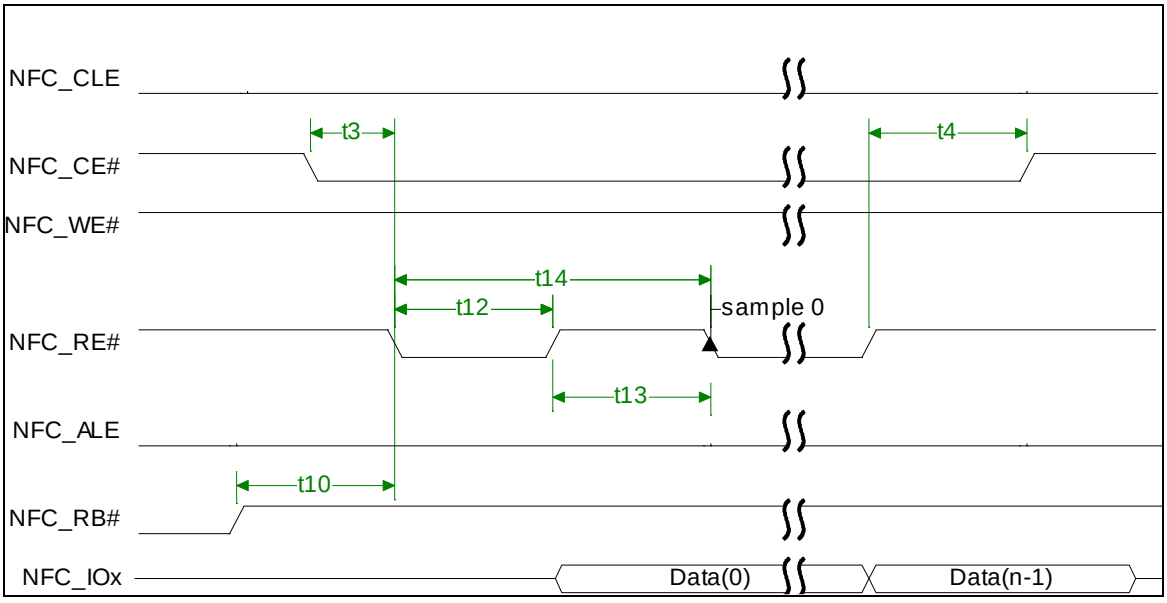


Figure 14-3. EDO Type Serial Access after Read Cycle (SAM1)

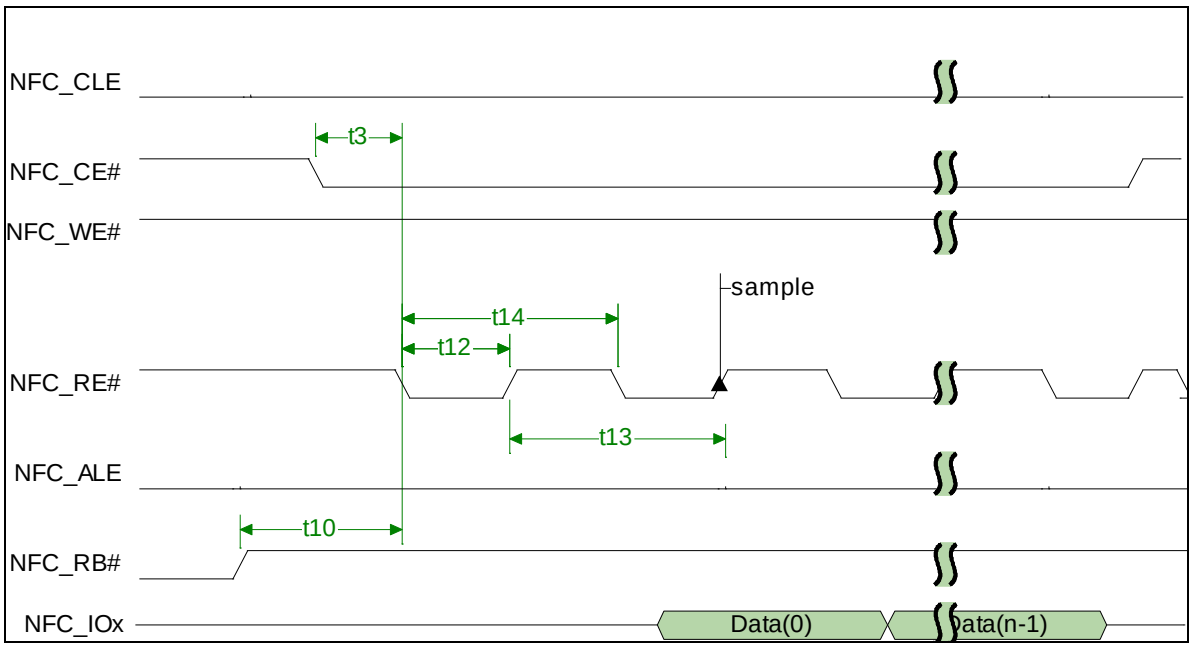


Figure 14-4. Extending EDO Type Serial Access Mode (SAM2)

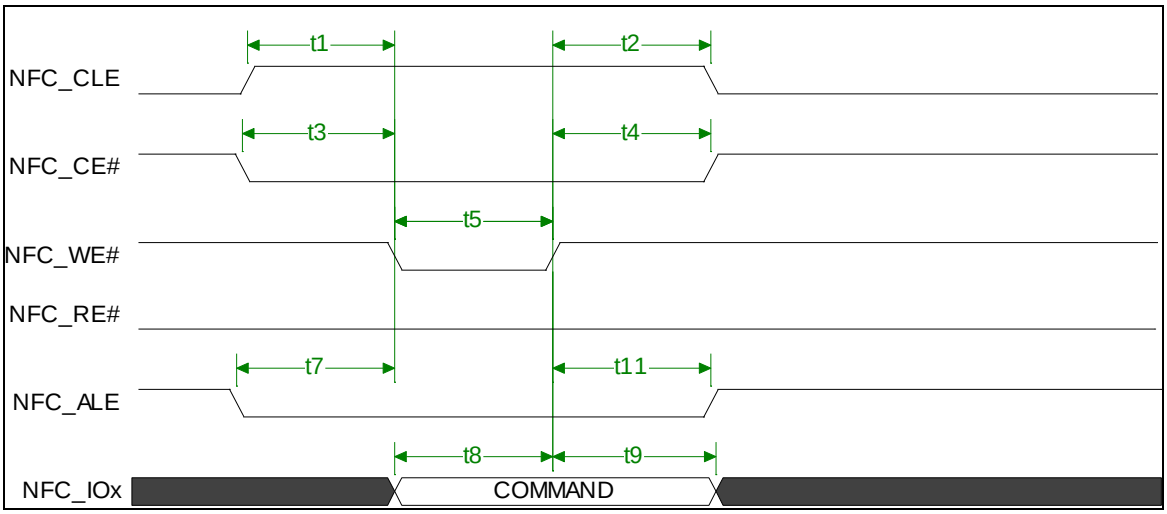


Figure 14-5. Command Latch Cycle

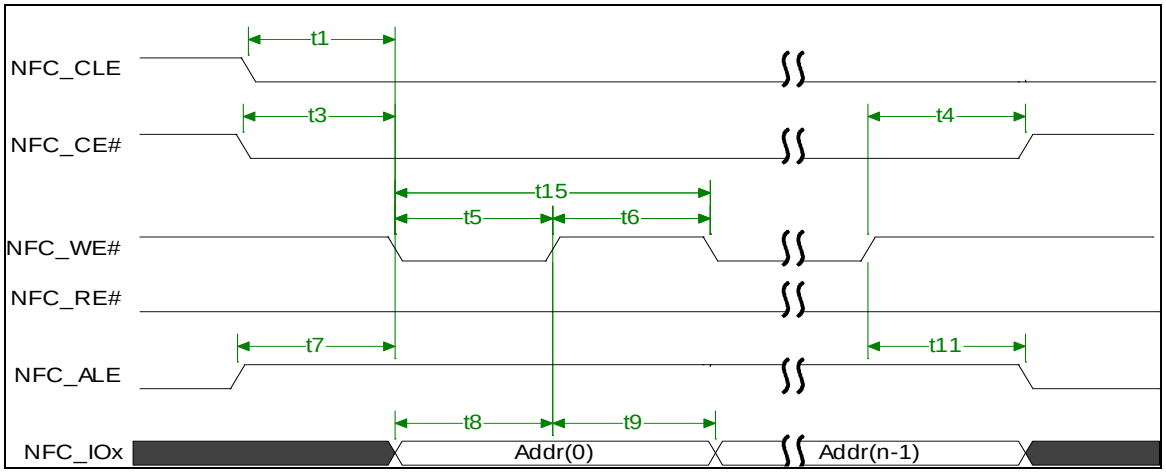


Figure 14-6. Address Latch Cycle

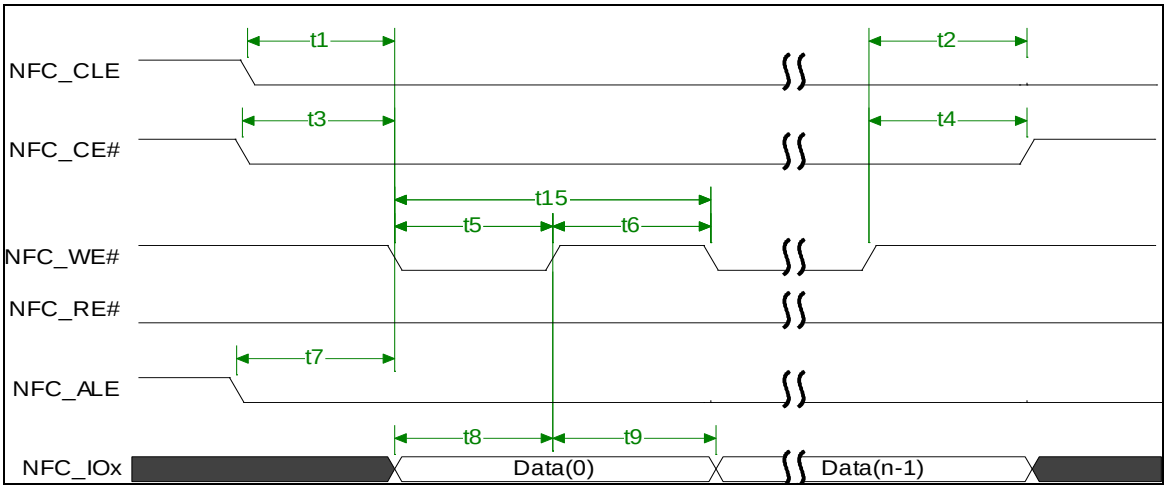


Figure 14-7. Write Data to Flash Cycle

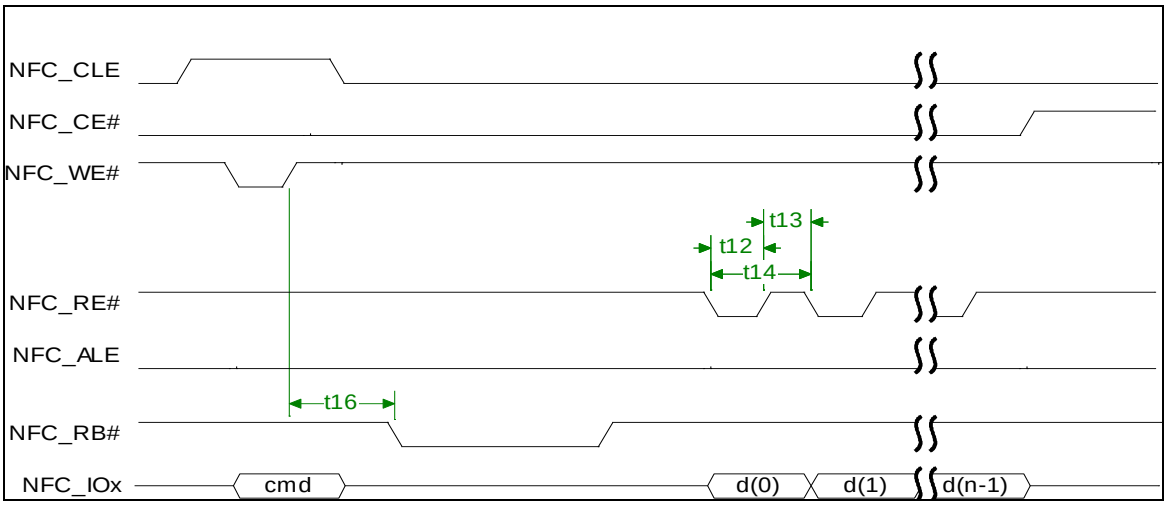


Figure14-8. Waiting R/B# Ready Diagram

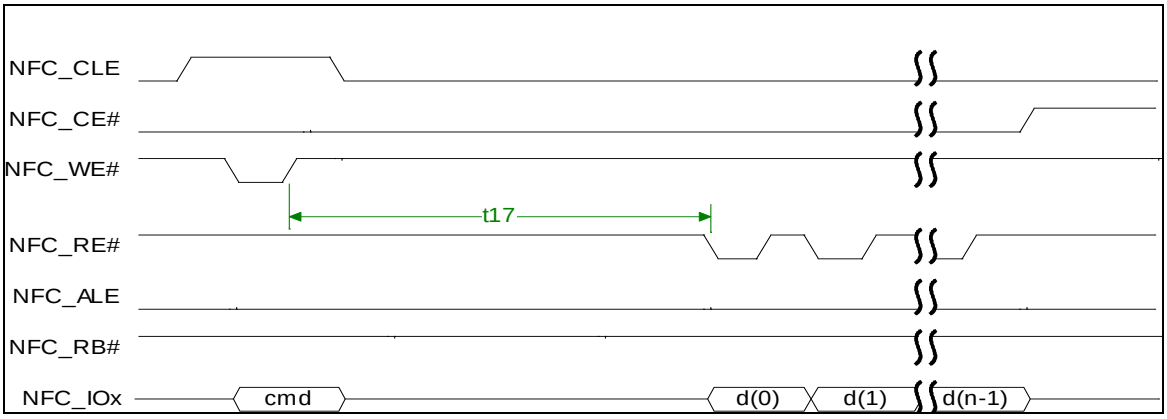


Figure14-9. WE # High to RE# Low Timing Diagram

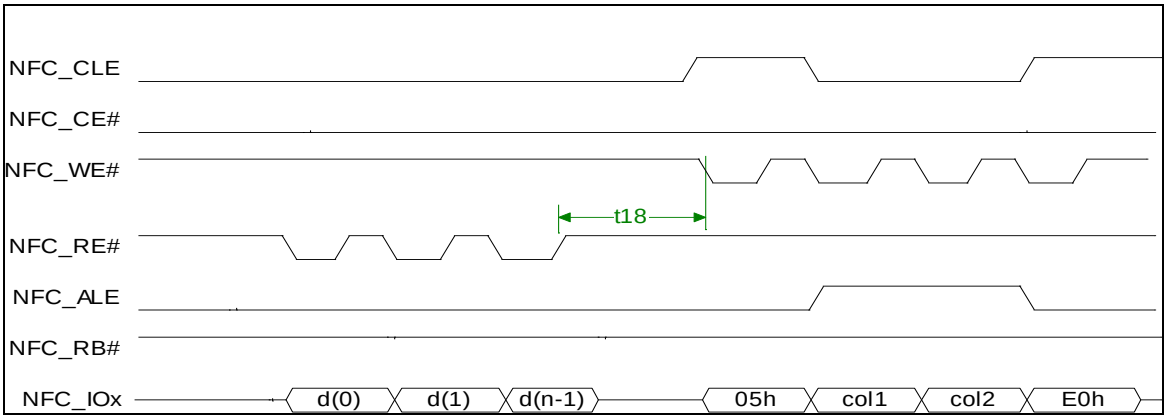


Figure14-10. RE # High to WE# Low Timing Diagram

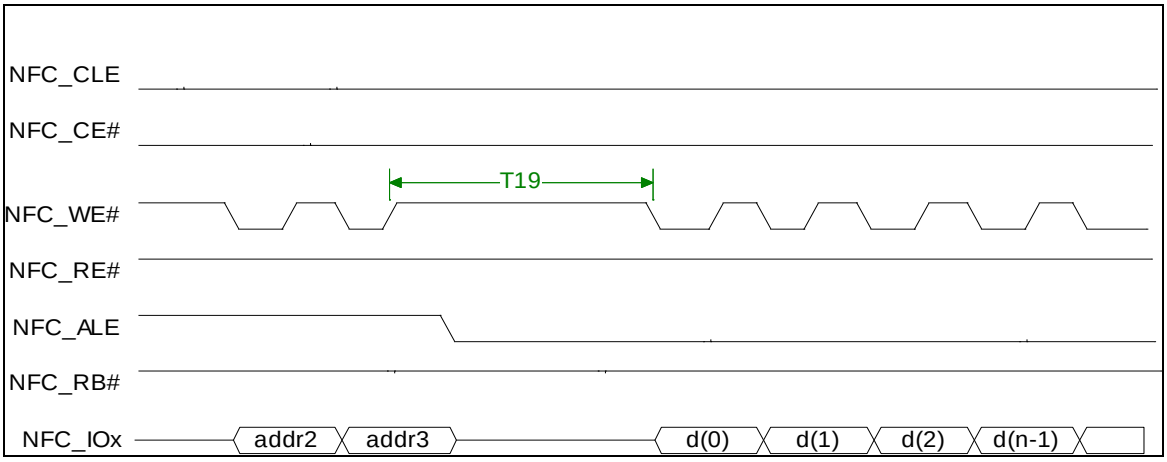


Figure14-11. Address to Data Loading Timing Diagram

Timing Cycle List:

ID	Parameter	Timing	Notes

T1	NFC_CLE setup time	T	
T2	NFC_CLE hold time	T	
T3	NFC_CE setup time	T	
T4	NFC_CE hold time	T	
T5	NFC_WE# pulse width	T	
T6	NFC_WE# hold time	T	
T7	NFC_ALE setup time	T	
T8	Data setup time	T	
T9	Data hold time	T	
T10	Ready to NFC_RE# low	3T	
T11	NFC_ALE hold time	T	
T12	NFC_RE# pulse width	T	
T13	NFC_RE# hold time	T	
T14	Read cycle time	2T	
T15	Write cycle time	2T	
T16	NFC_WE# high to R/B# busy	tWB	Specified by timing configure register(NFC_TIMING_CFG)
T17	NFC_WE# high to NFC_RE# low	tWHR	Specified by timing configure register(NFC_TIMING_CFG)
T18	NFC_RE# high to NFC_WE# low	tRHW	Specified by timing configure register(NFC_TIMING_CFG)
T19	Address to Data Loading time	tADL	Specified by timing configure register(NFC_TIMING_CFG)

Notes: T is the clock period duration of NFC_CLK (x2).

14.4. NFC Operation Guide

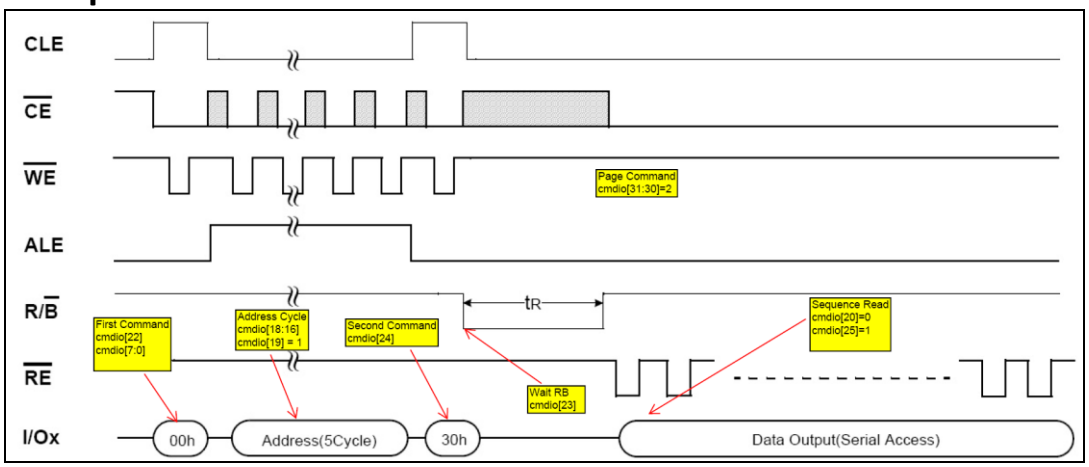


Figure14-12. Page Read Command Diagram

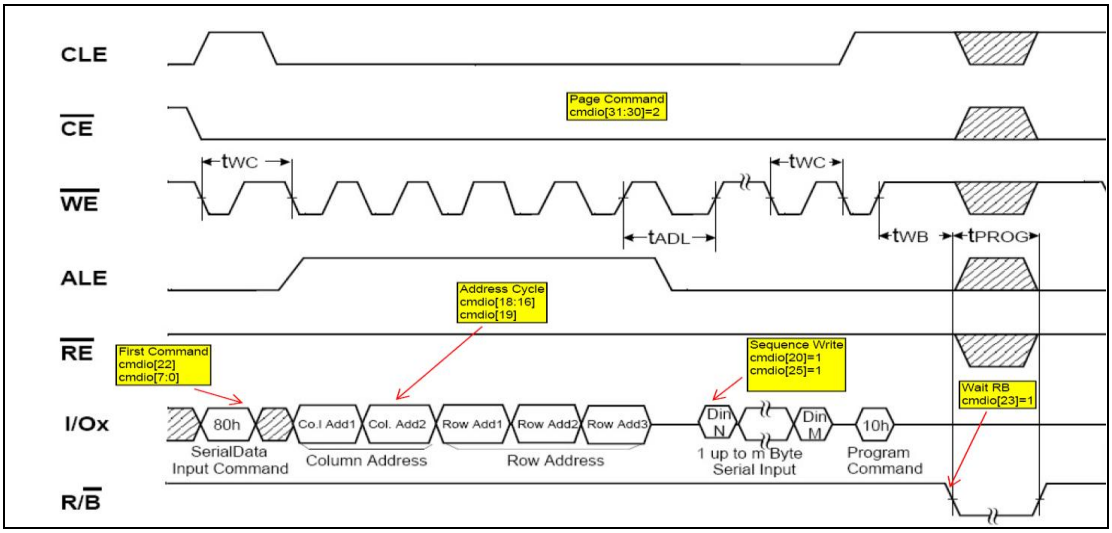


Figure14-13. Page Program Diagram

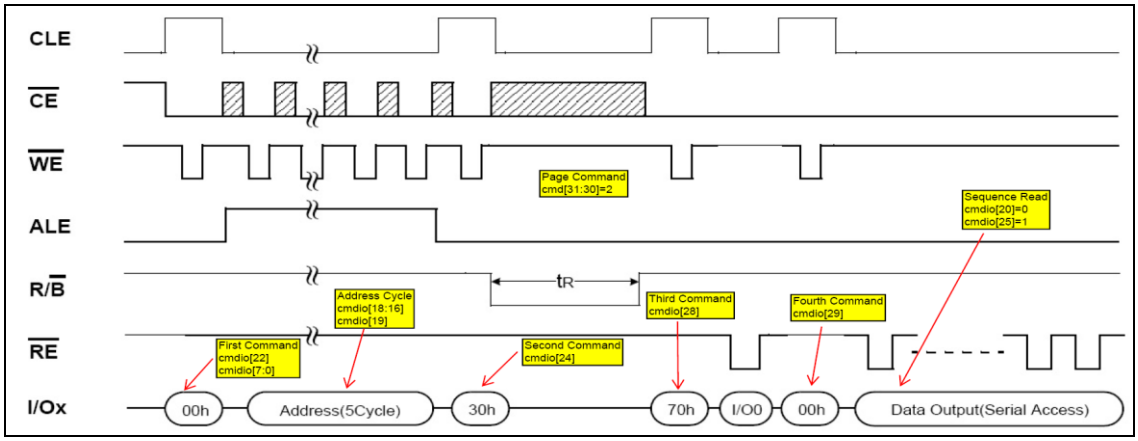


Figure14-14. EF-NAND Page Read Diagram

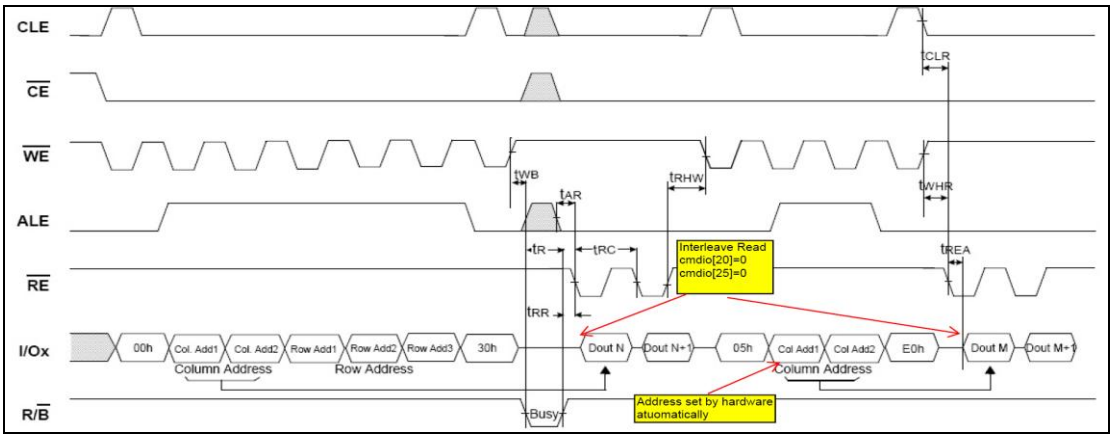


Figure14-15. Interleave Page Read Diagram

Chapter 15 SD/MMC Controller

15.1. Overview

The SD/MMC controller can be configured as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card.

The SD/MMC controller features:

- Support Secure Digital memory protocol commands (up to SD2.0)
- Support Secure Digital I/O protocol commands(up to SDIO2.0)
- Support Multimedia Card protocol commands (up to MMC4.3)
- Support hardware CRC generation and error detection
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 16x32-bit (64 bytes total) FIFO for data transfer

15.2. SD/MMC Timing Diagram

Please refer to relative Specifications listed below:

- Physical Layer Specification Ver2.00 Final
- SDIO Specification Ver2.00
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard

Chapter 16 Two Wire Interface

16.1. Overview

This Two Wire Interface (TWI) controller is an interface between CPU host and the serial 2-Wire bus, which supports all standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This 2-Wire Controller can be operated in standard mode (100K bps) or fast-mode (up to 400K bps). Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is supported in Slave mode.

The 2-Wire Controller features:

- Software-programmable for Slave or Master
- Support Repeated START signal
- Support Multi-master systems
- Support 10-bit addressing with 2-Wire bus
- Perform arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Support speed up to 400K bits/s (‘fast mode’)
- Support operation from a wide range of input clock frequencies

16.2. TWI Timing Diagram

Data are always transferred:

1) In unit of byte (8-bit);
2) Each byte followed by an acknowledge bit;
3) Unlimited number of byte in each data transfer;
4) Data are transferred in serial, with MSB first.
5) The receiver will hold SCL low to force the transmitter to enter a wait state while it is waiting for responses from the microprocessor after every byte transfer.

Acknowledge is indispensible in data transfer, and related acknowledge clock pulse is generated by the master. After sending a byte, the transmitter will release the SDA line, and one of the following two cases will occur:

a. The SDA is pulled down by the receiver and an acknowledge signal is sent back;
b. The SDA is left high, and a “not acknowledge” signal is sent back;

When the slave receiver doesn't acknowledge the slave address (because of resource deficiency), the SDA will be left high for master to generate a STOP condition to abort the transfer.

When the slave receiver acknowledges the slave address, but not ready to receive more during a data transfer, the SDA will be left high for the master to generate a STOP condition to abort the transfer.

The following diagram provides an illustration to the relation between SDA signal line and SCL signal line on the 2-Wire serial bus.

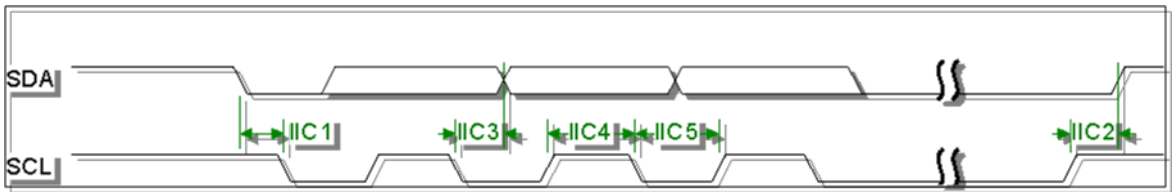


Figure 16-1. TWI Timing Diagram

16.3. TWI Controller Register List

Module Name	Base Address
TWI0	0x01C2AC00
TWI1	0x01C2B000
TWI2	0x01C2B400

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address
TWI_XADDR	0x0004	TWI Extended slave address
TWI_DATA	0x0008	TWI Data byte
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock control register
TWI_SRST	0x0018	TWI Software reset
TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register

16.4. TWI Controller Register Description

16.4.1. TWI Slave Address Register(Default: 0x00000000)

Offset: 0x00			Register Name: TWI_ADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:1	R/W	0	SLA Slave address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0	GCE General call address enable 0: Disable 1: Enable

Note:
For 7-bit addressing:
SLA6 – SLA0 is the 7-bit address of TWI in slave mode. When TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the two wire bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).
For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

16.4.2. TWI Extend Address Register(Default: 0x00000000)

Offset: 0x04			Register Name: TWI_XADDR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	SLAX Extend Slave Address SLAX[7:0]

16.4.3. TWI Data Register(Default: 0x00000000)

Offset: 0x08			Register Name: TWI_DATA
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	Data byte for transmitting or receiving

16.4.4. TWI Control Register(Default: 0x00000000)

Offset: 0x0C			Register Name: TWI_CNTR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R/W	0	INT_EN Interrupt Enable 1'b0: The interrupt line always low 1'b1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0	BUS_EN two-wire bus Enable 1'b0: The two-wire bus inputs ISDA/ISCL are ignored and the 2-Wire Controller will not respond to any address on the bus 1'b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set. Notes: In master operation mode, this bit should be set to '1'
5	R/W	0	M_STA Master Mode Start When M_STA is set to '1', TWI controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the 2-Wire Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released. The M_STA bit is cleared automatically after a START condition is sent: writing a '0' to this bit has no effect.
4	R/W	0	M_STP Master Mode Stop If M_STP is set to '1' in master mode, a STOP condition is transmitted

			on the two-wire bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the two-wire bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode), and then transmit the START condition. The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.
3	R/W	0	INT_FLAG Interrupt Flag INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the two-wire bus clock line (SCL) is stretched until '0' is written to INT_FLAG. The 2-wire clock line is then released and the interrupt line goes low.
2	R/W	0	A_ACK Assert Acknowledge When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the two-wire bus if: 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3. A data byte has been received in master or slave mode. When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode. If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte is transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared. The TWI will not respond as a slave unless A_ACK is set.
1:0	/	/	/

16.4.5. TWI Status Register(Default: 0x000000F8)

Offset: 0x10			Register Name: TWI_STAT
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0xF8	Status Information Byte Code Status 0x00: Bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte

			0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK transmitted 0x58: Data byte received in master mode, not ACK transmitted 0x60: Slave address + Write bit received, ACK transmitted 0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted 0x70: General Call address received, ACK transmitted 0x78: Arbitration lost in address as master, General Call address received, ACK transmitted 0x80: Data byte received after slave address received, ACK transmitted 0x88: Data byte received after slave address received, not ACK transmitted 0x90: Data byte received after General Call received, ACK transmitted 0x98: Data byte received after General Call received, not ACK transmitted 0xA0: STOP or repeated START condition received in slave mode 0xA8: Slave address + Read bit received, ACK transmitted 0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted 0xB8: Data byte transmitted in slave mode, ACK received 0xC0: Data byte transmitted in slave mode, ACK not received 0xC8: Last byte transmitted in slave mode, ACK received 0xD0: Second Address byte + Write bit transmitted, ACK received 0xD8: Second Address byte + Write bit transmitted, ACK not received 0xF8: No relevant status information, INT_FLAG=0 Others: Reserved

16.4.6. TWI Clock Register(Default: 0x00000000)

Offset: 0x14			Register Name: TWI_CCR
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:3	R/W	0	CLK_M
2:0	R/W	0	CLK_N The two-wire bus is sampled by the TWI at the frequency defined by F0: Fsamp = F 0 = Fin / 2^CLK_N The TWI OSCL output frequency, in master mode, is F1 / 10: F1 = F0 / (CLK_M + 1) Foscl = F1 / 10 = Fin / (2^CLK_N * (CLK_M + 1)*10) For Example： Fin = 48Mhz (APB clock input) For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 F0 = 48M/2^2=12Mhz, F1= F0/(10*(2+1)) = 0.4Mhz For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 F0=48M/2^2=12Mhz, F1=F0/(10*(11+1)) = 0.1Mhz

16.4.7. TWI Soft Reset Register(Default: 0x00000000)

Offset: 0x18	Register Name: TWI_SRST

Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0	Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when complete Soft Reset operation.

16.4.8. TWI Enhance Feature Register(Default: 0x00000000)

Offset: 0x1C			Register Name: TWI_EFR
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
0:1	R/W	0	Data Byte follow Read Command Control No Data Byte to be written after read command Only 1 byte data to be written after read command 2 bytes data can be written after read command 3 bytes data can be written after read command

16.4.9. TWI Line Control Register(Default: 0x0000003a)

Offset: 0x20			Register Name: TWI_LCR
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R	1	Current state of TWI_SCL 0 – low 1 - high
4	R	1	Current state of TWI_SDA 0 – low 1 - high
3	R/W	1	TWI_SCL line state control bit When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL 0 – output low level 1 – output high level
2	R/W	0	TWI_SCL line state control enable When this bit is set, the state of TWI_SCL is controlled by the value of bit[3]. 0-disable TWI_SCL line control mode 1-enable TWI_SCL line control mode
1	R/W	1	TWI_SDA line state control bit When line control mode is enabled (bit[0] set), value of this bit decides the output level of TWI_SDA 0 – output low level 1 – output high level
0	R/W	0	TWI_SDA line state control enable When this bit is set, the state of TWI_SDA is controlled by the value of bit[1]. 0-disable TWI_SDA line control mode 1-enable TWI_SDA line control mode

16.4.10. TWI DVFS Control Register(Default: 0x00000000)

Offset: 0x24			Register Name: TWI_DVFSCR
Bit	Read/Write	Default/Hex	Description

31:2	/	/	/
2	R/W	0	CPU and DVFS BUSY set priority select 0: CPU has higher priority 1: DVFS has higher priority
1	R/W	0	CPU Busy set
0	R/W	0	DVFS Busy set

Notes: This register is only implemented in TWI0.

16.5. TWI Controller Special Requirement

16.5.1. TWI Pin List

Port Name	Width	Direction	Description
TWI_SCL	1	IN/OUT	TWI Clock line
TWI_SDA	1	IN/OUT	TWI Serial Data line

16.5.2. TWI Controller Operation

There are four operation modes on the two-wire bus which dictates the communications method: Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP condition is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupts the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

Chapter 17 SPI

17.1. Overview

The Serial Peripheral Interface (SPI) allows rapid data communication with less software interrupts. The SPI module contains one 8x64 receiver buffer (RXFIFO) and one 8x64 transmit buffer (TXFIFO). It can work in two modes: Master mode and Slave mode.

It features:

- Full-duplex synchronous serial interface
- Configurable Master/Slave
- 8x64 FIFO for data transmit and receive
- Configurable Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK)
- Support Dedicated DMA

17.2. SPI Timing Diagram

The SPI master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used to setup or sample data. The leading edge is used to setup data when PHA is '1' and to sample data when PHA is '0'. The four modes are listed below:

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

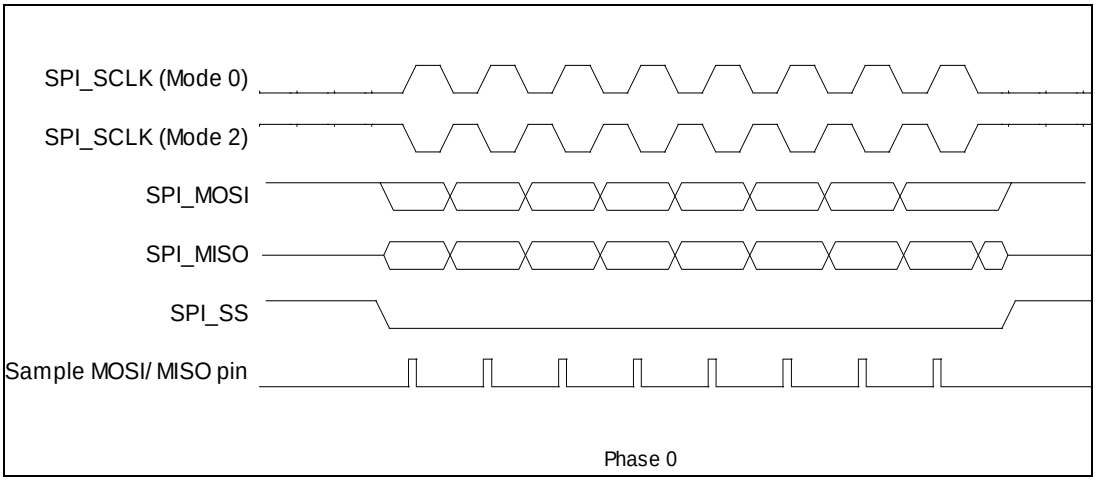


Figure17-1. SPI Phase 0 Timing Diagram

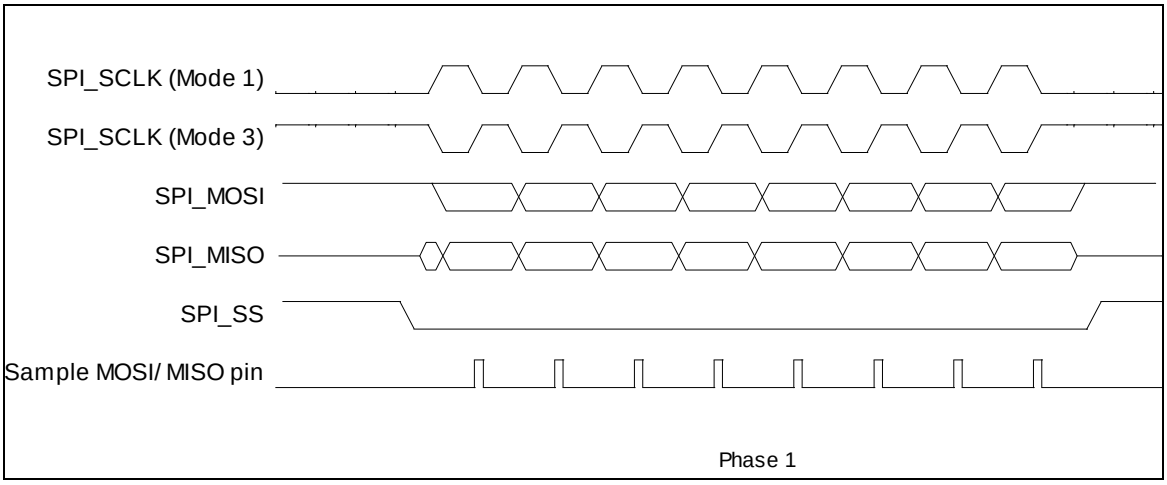


Figure 17-2. SPI Phase 1 Timing Diagram

17.3. SPI Register List

Module Name	Base Address
SPI0	0x01C05000
SPI1	0x01C06000
SPI2	0x01C17000

Register Name	Offset	Description
SPI_RXDATA	0x00	SPI RX Data Register
SPI_TXDATA	0x04	SPI TX Data Register
SPI_CTL	0x08	SPI Control Register
SPI_INTCTL	0x0C	SPI Interrupt Control Register
SPI_ST	0x10	SPI Status Register
SPI_DMACTL	0x14	SPI DMA Control Register
SPI_WAIT	0x18	SPI Wait Clock Counter Register
SPI_CCTL	0x1C	SPI Clock Rate Control Register
SPI_BC	0x20	SPI Burst Counter Register

SPI_TC	0x24	Spi Transmit Counter Register
SPI_FIFO_STA	0x28	SPI FIFO Status Register

17.4. SPI Register Description

17.4.1. SPI RX Data Register(Default: 0x00000000)

Offset: 0x00			Register Name: SPI_RXDATA
Bit	Read/Write	Default/hex	Description
31:0	R	0	Receive Data In 8-bits SPI bus width, this register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are words in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, the two SPI bursts are returned and the RXFIFO depth decreases by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth decreases by 4.

17.4.2. SPI TX Data Register(Default: 0x00000000)

Offset: 0x04			Register Name: SPI_TXDAT
Bit	Read/Write	Default/Hex	Description
31:0	W	0	Transmit Data

17.4.3. SPI Control Register(Default: 0x0002001C)

Offset: 0x08			Register Name: SPI_CTL
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19	R/W	0	Master Sample Data Control Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave. 1 – delay internal read sample point 0 – normal operation, do not delay internal read sample point
18	R/W	0	Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1 – stop transmit data when RXFIFO full 0 – normal operation, ignore RXFIFO status
17	R/W	1	SS_LEVEL When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal. 1 – set SS to high 0 – set SS to low
16	R/W	0	SS_CTRL - SS Output Mode Select Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTRL_REG.SS_LEVEL (bit [17]) to 1 or 0 to control the level of SS signal. 1 – manual output SS 0 – automatic output SS
15	R/W	0	Discard Hash Burst DHB

			In master mode it controls whether discarding unused SPI bursts. 0: Receiving all SPI bursts in BC period 1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by WTC.
14	R/W	0	DDB Dummy Burst Type 0: The bit value of dummy SPI burst is zero 1: The bit value of dummy SPI burst is one
13:12	R/W	0	SS SPI Chip Select Select one of four external SPI Master/Slave Devices 00: SPI_SS0 will be asserted 01: SPI_SS1 will be asserted 10: SPI_SS2 will be asserted 11: SPI_SS3 will be asserted Notes: These two bits can't be configured for SPI1 Engine.
11	R/W	0	RPSM Rapids Mode Select Select Rapids operation mode for high speed read. 0: Normal read mode 1: Rapids read mode
10	R/W	0	XCH Exchange Burst In master mode it is used to start to SPI burst. 0: Idle 1: Initiates exchange. After finishing the SPI bursts transfer specified by BC, this bit is cleared to zero by SPI Controller.
9	R/W	0	RXFIFO Reset Write '1' to reset the control portion of the receiver FIFO and treats the FIFO as empty. It is 'self-clearing'. It is not necessary to clear this bit.
8	R/W	0	TXFIFO Reset Write '1' to reset the control portion of the transmit FIFO and treats the FIFO as empty. It is 'self-clearing'. It is not necessary to clear this bit.
7	R/W	0	SSCTL In master mode, this bit selects the output wave form for the SPI_SSx signal. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts
6	R/W	0	LMTF LSB/ MSB Transfer First select 0: MSB first 1: LSB first
5	R/W	0	DMAM DMA mode control 0: normal dma 1: dedicate dma
4	R/W	1	SSPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)
3	R/W	1	POL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle)

2	R/W	1	PHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data)
1	R/W	0	MODE SPI Function Mode Select 0: Slave Mode 1: Master Mode
0	R/W	0	EN SPI Module Enable Control 0: Disable 1: Enable

17.4.4. SPI Interrupt Control Register(Default: 0x00000000)

Offset: 0x0C			Register Name: SPI_INTCTL
Bit	Read/Write	Default/Hex	Description
31:18	/	/	/
17	R/W	0	SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable 1: Enable
16	R/W	0	Transfer Completed Interrupt Enable 0: Disable 1: Enable
15	/	/	/
14	R/W	0	TXFIFO under run Interrupt Enable 0: Disable 1: Enable
13	R/W	0	TX FIFO Overflow Interrupt Enable 0: Disable 1: Enable
12	R/W	0	TX FIFO 3/4 Empty Interrrupt Enable 0: Disable 1: Enable
11	R/W	0	TX FIFO 1/4 Empty Interrrupt Enable 0: Disable 1: Enable
10	R/W	0	TX FIFO Full Interrupt Enable 0: Disable 1: Enable
9	R/W	0	TX FIFO Half Empty Interrupt Enable 0: Disable 1: Enable
8	R/W	0	TX FIFO Empty Interrupt Enable 0: Disable 1: Enable
7	/	/	/
6	R/W	0	RXFIFO under run Interrupt Enable 0: Disable 1: Enable
5	R/W	0	RX FIFO Overflow Interrupt Enable 0: Disable 1: Enable

4	R/W	0	RXFIFO 3/4 Full Interrupt Enable 0: Disable 1: Enable
3	R/W	0	RX FIFO 1/4 Full Interrupt Enable 0: Disable 1: Enable
2	R/W	0	RX FIFO Full Interrupt Enable 0: Disable 1: Enable
1	R/W	0	RX FIFO Half Full Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RX FIFO Ready Interrupt Enable 0: Disable 1: Enable

17.4.5. SPI Interrupt Status Register(Default: 0x00001B00)

Offset: 0x10			Register Name: SPI_INT_STA
Bit	Read/Write	Default/Hex	Description
31	R	0	Clear interrupt busy flag 0: clearing interrupt is done 1: clearing interrupt is busy
30:24	/	/	/
23:20	/	/	/
19:18	/	/	/
17	R/W	0	SSI SS Invalid Interrupt When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.
16	R/W	0	TC Transfer Completed In master mode, it indicates that all bursts specified by BC have been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it. 0: Busy 1: Transfer Completed
15	/	/	/
14	R/W	0	TU TXFIFO under run This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it. 0: TXFIFO is not underrun 1: TXFIFO is underrun
13	R/W	0	TO TXFIFO Overflow This bit is set when the TXFIFO overflows. Writing 1 to this bit clears it. 0: TXFIFO is not overflowed 1: TXFIFO is overflowed
12	R/W	1	TXFIFO 3/4 empty This bit is set if the TXFIFO is more than 3/4 empty. Writing 1 to this bit clears it.
11	R/W	1	TXFIFO 1/4 empty

			This bit is set if the TXFIFO is more than 1/4 empty. Writing 1 to this bit clears it.
10	R/W	0	TF TXFIFO Full This bit is set when the TXFIFO is full. Writing 1 to this bit clears it. 0: TXFIFO is not Full 1: TXFIFO is Full
9	R/W	1	THE TXFIFO Half empty This bit is set if the TXFIFO is more than half empty. Writing 1 to this bit clears it. 0: TXFIFO holds more than half words 1: TXFIFO holds half or fewer words
8	R/W	1	TE TXFIFO Empty This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it. 0: TXFIFO contains one or more words. 1: TXFIFO is empty
7	/	/	/
6	R/W	0	RU RXFIFO Underrun When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.
5	R/W	0	RO RXFIFO Overflow When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it. 0: RXFIFO is available. 1: RXFIFO has overflowed.
4	R/W	0	RXFIFO 3/4 Full This bit is set when the RXFIFO is 3/4 full. Writing 1 to this bit clears it. 0: Not 3/4 Full 1: 3/4 Full
3	R/W	0	RXFIFO 1/4 Full This bit is set when the RXFIFO is 1/4 full. Writing 1 to this bit clears it. 0: Not 1/4 Full 1: 1/4 Full
2	R/W	0	RF RXFIFO Full This bit is set when the RXFIFO is full. Writing 1 to this bit clears it. 0: Not Full 1: Full
1	R/W	0	RHF RXFIFO Half Full. This bit is set if the RXFIFO is half full (≥ 4 words in RXFIFO) . Writing 1 to this bit clears it. 0: Less than 4 words are stored in RXFIFO. 1: Four or more words are available in RXFIFO.
0	R/W	0	RR RXFIFO Ready This bit is set any time there is one or more words stored in RXFIFO (≥ 1 words). Writing 1 to this bit clears it. 0: No valid data in RXFIFO 1: More than 1 word in RXFIFO

17.4.6. SPI DMA Control Register(Default: 0x00000000)

Offset: 0x14			Register Name: SPI_DMACTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0	TXFIFO3/4 Empty DMA Request Enable 0: Disable 1: Enable
11	R/W	0	TXFIFO 1/4 Empty DMA Request Enable 0: Disable 1: Enable
10	R/W	0	TXFIFO Not Full DMA Request Enable When enabled, if more than one free room for burst, DMA request is asserted, otherwise, it's de-asserted. 0: Disable 1: Enable
9	R/W	0	TXFIFO Half Empty DMA Request Enable 0: Disable 1: Enable
8	R/W	0	TXFIFO Empty DMA Request Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0	RXFIFO 3/4 Full DMA Request Enable This bit enables/disables the RXFIFO 3/4 Full DMA Request. 0: Disable 1: Enable
3	R/W	0	RXFIFO 1/4 Full DMA Request Enable This bit enables/disables the RXFIFO 1/4 Full DMA Request. 0: Disable 1: Enable
2	R/W	0	RXFIFO Full DMA Request Enable This bit enables/disables the RXFIFO Half Full DMA Request. 0: Disable 1: Enable
1	R/W	0	RXFIFO Half Full DMA Request Enable This bit enables/disables the RXFIFO Half Full DMA Request. 0: Disable 1: Enable
0	R/W	0	RXFIFO Ready Request Enable This bit enables/disables the RXFIFO Ready DMA Request when one or more than one words in RXFIFO 0: Disable 1: Enable

17.4.7. SPI Wait Clock Register(Default: 0x00000000)

Offset: 0x18			Register Name: SPI_WAIT
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:0	R/W	0	WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer.

			0: No wait states inserted N: N SPI_SCLK wait states inserted

17.4.8. SPI Clock Control Register(Default: 0x00000002)

Offset: 0x1C			Register Name: SPI_CCTL
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0	DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1 1: Select Clock Divide Rate 2
11:8	R/W	0	CDR1 Clock Divide Rate 1 (Master Mode Only) This field selects the baud rate of the SPI_SCLK based on a division of the AHB_CLK. These bits allow SPI to synchronize with different external SPI devices. The max frequency is one quarter of AHB_CLK. The divide ratio is determined according to the following table using the equation: 2^(n+1). The SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / 2^(n+1).
7:0	R/W	0x2	CDR2 Clock Divide Rate 2 (Master Mode Only) The SPI_SCLK is determined according to the following equation: SPI_CLK = AHB_CLK / (2*(n + 1)).

17.4.9. SPI Burst Counter Register(Default: 0x00000000)

Offset: 0x20			Register Name: SPI_BC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	BC Burst Counter In master mode, this field specifies the total burst number. 0: 0 burst 1: 1 burst … N: N bursts

17.4.10. SPI Transmit Counter Register(Default: 0x00000000)

Offset: 0x24			Register Name: SPI_TC
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	WTC Write Transmit Counter In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically. 0: 0 burst 1: 1 burst … N: N bursts

17.4.11. SPI FIFO Status Register(Default: 0x00000000)

Offset: 0x28			Register Name: SPI_FIFO_STA
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
22:16	R	0x0	TXFIFO Counter These bits indicate the number of words in TXFIFO 0: 0 byte in TXFIFO 1: 1 byte in TXFIFO … … 63: 63 bytes in TXFIFO 64: 64 bytes in TXFIFO
15:7	/	/	/
6:0	R	0x0	RXFIFO Counter These bits indicate the number of words in RXFIFO 0: 0 byte in RXFIFO 1: 1 byte in RXFIFO … … 63: 63 bytes in RXFIFO 64: 64 bytes in RXFIFO

17.5. SPI Special Requirement

17.5.1. SPI Pin List

The direction of SPI pin is different in two work modes: Master Mode and Slave Mode.

Port Name	Width	Direction(M)	Direction(S)	Description
SPI_SCLK	1	OUT	IN	SPI Clock
SPI_MOSI	1	OUT	IN	SPI Master Output Slave Input Data Signal
SPI_MISO	1	IN	OUT	SPI Master Input Slave Output Data Signal
SPI_CS[1:0]	2	OUT	IN	SPI Chip Select Signal

17.5.2. SPI Module Clock Source and Frequency

The SPI module uses two clock sources: AHB_CLK and SPI_CLK. The SPI_SCLK can in the range from 3KHz to 100MHz and AHB_CLK>= 2x SPI_SCLK.

Clock Name	Description	Requirement
AHB_CLK	AHB Bus Clock, as the clock source of SPI module	AHB_CLK >= 2xSPI_SCLK
SPI_CLK	SPI Serial Input Clock	

Chapter 18 UART

18.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1.5 or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Interrupt support for FIFOs, Status Change

18.2. UART Timing Diagram

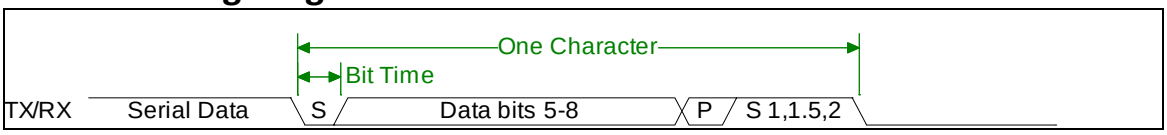


Figure 18-1. UART Serial Data Format

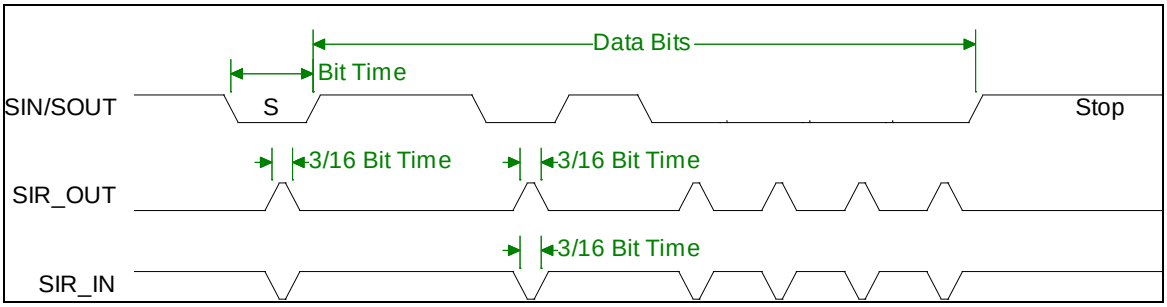


Figure 18-2. Serial IrDA Data Format

18.3. UART Register List

There are 4 UART controllers that can be configured as Serial IrDA.

Module Name	Base Address
UART0	0x01C28000
UART1	0x01C28400
UART2	0x01C28800
UART3	0x01C28C00

Register Name	Offset	Description
UART_RBR	0x00	UART Receive Buffer Register
UART_THR	0x00	UART Transmit Holding Register
UART_DLL	0x00	UART Divisor Latch Low Register
UART_DLH	0x04	UART Divisor Latch High Register
UART_IER	0x04	UART Interrupt Enable Register
UART_IIR	0x08	UART Interrupt Identity Register
UART_FCR	0x08	UART FIFO Control Register
UART_LCR	0x0C	UART Line Control Register
UART_MCR	0x10	UART Modem Control Register
UART_LSR	0x14	UART Line Status Register
UART_MSR	0x18	UART Modem Status Register
UART_SCH	0x1C	UART Scratch Register
UART_USR	0x7C	UART Status Register
UART_TFL	0x80	UART Transmit FIFO Level
UART_RFL	0x84	UART_RFL
UART_HALT	0xA4	UART Halt TX Register

18.4. UART Register Description

18.4.1. UART Receiver Buffer Register(Default: 0x00000000)

Offset: 0x00			Register Name: UART_RBR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/

7:0	R	0	RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, the data already in the FIFO is preserved, but all incoming data are lost and an overrun error occurs.

18.4.2. UART Transmit Holding Register(Default: 0x00000000)

Offset: 0x00			Register Name: UART_THR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	W	0	THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results the write data lost.

18.4.3. UART Divisor Latch Low Register(Default: 0x00000000)

Offset: 0x00			Register Name: UART_DLL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	DLL Divisor Latch Low Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate equals to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

18.4.4. UART Divisor Latch High Register(Default: 0x00000000)

Offset: 0x04			Register Name: UART_DLH
Bit	Read/Write	Default/Hex	Description

31:8	/	/	/
7:0	R/W	0	DLH Divisor Latch High Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate equals to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

18.4.5. UART Interrupt Enable Register(Default: 0x00000000)

Offset: 0x04			Register Name: UART_IER
Bit	Read/Write	Default/Hex	Description
31:8	/	/	
7	R/W		PTIME Programmable THRE Interrupt Mode Enable This is used to enable/disable the generation of THRE Interrupt. 0: Disable 1: Enable
6:4	/	/	/
3	R/W	0	EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
2	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
0	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable

18.4.6. UART Interrupt Identity Register(Default: 0x00000000)

Offset: 0x08			Register Name: UART_IIR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	R	0	FEFLAG FIFOs Enable Flag This is used to indicate whether the FIFOs are enabled or disabled. 00: Disable 11: Enable
5:4	/	/	/
3:0	R	0x1	IID Interrupt ID This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver Line Status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received Data Available	Receiver data available (non-FIFO mode or FIFOs disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	Reading the receiver buffer register (non-FIFO mode or FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Second	Character Timeout Indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during this time	Reading the receiver buffer register
0010	Third	Transmit Holding Register Empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem Status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Fifth	Busy Detect	UART_16550_COMPATIBLE =	Reading the UART status

		Indication	NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	register

18.4.7. UART FIFO Control Register(Default: 0x00000000)

Offset: 0x08			Register Name: UART_FCR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:6	W	0	RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
5:4	W	0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
3	W	0	DMAM DMA Mode 0: Mode 0 1: Mode 1
2	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request. It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR RCVR FIFO Reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request. It is 'self-clearing'. It is not necessary to clear this bit.
0	W	0	FIFOE Enable FIFOs This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

18.4.8. UART Line Control Register(Default: 0x00000000)

Offset: 0x0C			Register Name: UART_LCR
Bit	Read/Write	Default/Hex	Description

31:8	/	/	/
7	R/W	0	DLAB Divisor Latch Access Bit It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. 0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER) 1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)
6	R/W	0	BC Break Control Bit This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	/	/	/
4	R/W	0	EPS Even Parity Select It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). 0: Odd Parity 1: Even Parity
3	R/W	0	PEN Parity Enable It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0: parity disabled 1: parity enabled
2	R/W	0	STOP Number of stop bits It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	R/W	0	DLS Data Length Select It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits

			01: 6 bits 10: 7 bits 11: 8 bits

18.4.9. UART Modem Control Register(Default: 0x00000000)

Offset: 0x10			Register Name: UART_MCR
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6	R/W	0	SIRE SIR Mode Enable 0: IrDA SIR Mode disabled 1: IrDA SIR Mode enabled
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	/	/	/
2	/	/	/
1	R/W	0	RTS Request to Send This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. 0: rts_n de-asserted (logic 1) 1: rts_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	R/W	0	DTR Data Terminal Ready

			This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n。 0：dtr_n de-asserted (logic 1) 1：dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

18.4.10. UART Line Status Register(Default: 0x00000060)

Offset: 0x14			Register Name: UART_LSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	FIFOERR RX Data Error in FIFO When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.
6	R	1	TEMT Transmitter Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.
5	R	1	THRE TX Holding Register Empty If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register. If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written to the TX FIFO.
4	R	0	BI Break Interrupt This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	R	0	FE

			Framing Error This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error occurs due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no framing error 1:framing error Reading the LSR clears the FE bit.
2	R	0	PE Parity Error This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0: no parity error 1: parity error Reading the LSR clears the PE bit.
1	R	0	OE Overrun Error This occurs if a new data character is received before the previous data is read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character is read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0: no overrun error 1: overrun error Reading the LSR clears the OE bit.
0	R	0	DR Data Ready This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0: no data ready 1: data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty in FIFO mode.

18.4.11. UART Modem Status Register(Default: 0x00000000)

Offset: 0x18			Register Name: UART_MSR
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7	R	0	DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line

			dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)
6	R	0	RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)
5	R	0	DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	R	0	CTS Line State of Clear To Send This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted, it is an indication that the modem or data set is ready to exchange data with UART. 0: cts_n input is de-asserted (logic 1) 1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	R	0	DDCD Delta Data Carrier Detect This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0: no change on dcd_n since last read of MSR 1: change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. Note: If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	R	0	TERI Trailing Edge Ring Indicator This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR is read. 0: no change on ri_n since last read of MSR 1: change on ri_n since last read of MSR Reading the MSR clears the TERI bit.
1	R	0	DDSR Delta Data Set Ready This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 0: no change on dsr_n since last read of MSR 1: change on dsr_n since last read of MSR

			Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note: If the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	R	0	DCTS Delta Clear to Send This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0: no change on ctsdsr_n since last read of MSR 1: change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note: If the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

18.4.12. UART Scratch Register(Default: 0x00000000)

Offset: 0x1C			Register Name: UART_SCH
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R/W	0	Scratch Register This register is used by programmers as a temporary storage space. It has no defined purpose in the UART.

18.4.13. UART Status Register(Default: 0x00000006)

Offset: 0x7C			Register Name: UART_USR
Bit	Read/Write	Default/Hex	Description
31:5	/	/	/
4	R	0	RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	R	0	RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	R	1	TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	R	1	TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO is not full. 0: Transmit FIFO is full

			1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

18.4.14. UART Transmit FIFO Level Register(Default: 0x00000000)

Offset: 0x80			Register Name: UART_TFL
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0	Transmit FIFO Level This indicates the number of data entries in the transmit FIFO.

18.4.15. UART Receive FIFO Level Register(Default: 0x00000000)

Offset: 0x84			Register Name: UART_RFL
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:0	R	0	Receive FIFO Level This indicates the number of data entries in the receive FIFO.

18.4.16. UART Halt TX Register(Default: 0x00000000)

Offset: 0xA4			Register Name: UART_HALT
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5	R/W	0	SIR Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
4	R/W	0	SIR Transmit Pulse Polarity Invert 0: Not invert transmit pulse 1: Invert transmit pulse
3:1	/	/	/
0	R/W	0	Halt TX This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 : Halt TX disabled 1 : Halt TX enabled Note: If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

18.5. UART Special Requirement

18.5.1. IrDA Inverted Signals

When the UART is working in IrDA mode (MCR[6]='1'), if HALT[4] is set to '1', the signal is inverted before transferring to pin SOUT, and if HALT[5] is set to '1', the signal is inverted after receiving from pin SIN.

Chapter 19 CIR

19.1. Overview

The CIR features:

- Full physical layer implementation
- Support CIR for remote control or wireless keyboard
- 64x8-bits FIFO for data transfer
- Programmable FIFO thresholds
- Support Interrupt and DMA

CIR receiver is implemented in hardware to save CPU resource. It samples the input signals on the programble frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width, and the encoded data is buffered in a 64 levels and 8-bit width RX FIFO: the MSB bit is used to record the polarity of the receiving CIR signal (The high level is represented as 1 and the low level is represented as 0), and the rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low) is more than 128, another byte is used. Since there are always some noises in the air, a threshold can be set to filter the noises to reduce system loading and improve system stability.

19.2. CIR Register List

Module Name	Base Address
CIR	0x01C21800

Register Name	Offset	Description
CIR_CTL	0x00	CIR Control Register
CIR_RXCTL	0x10	CIR Receiver Configure Register
CIR_RXFIFO	0x20	CIR Receiver FIFO Register
CIR_RXINT	0x2C	CIR Receiver Interrupt Control Register
CIR_RXSTA	0x30	CIR Receiver Status Register
CIR_CONFIG	0x34	CIR Configure Register

19.3. CIR Regsiter Description

19.3.1. CIR Control Register(Default: 0x00000000)

Offset: 0x00			Register Name: CIR_CTL
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0	CGPO General Program Output (GPO) Control in CIR mode for TX Pin 0: Low level 1: High level
7:6	/	/	/
5:4	R/W	0	CIR ENABLE 00~10: / 11: CIR mode enable
3:2	/	/	/

1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Global Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

19.3.2. CIR Receiver Configure Register(Default: 0x00000000)

Offset: 0x10			Register Name: IR_RXCTL
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	1	RPPI Receiver Pulse Polarity Invert 0: Not invert receiver signal 1: Invert receiver signal
1:0	/	/	/

19.3.3. CIR Receiver FIFO Register(Default: 0x00000000)

Offset: 0x20			Register Name: IR_RXFIFO
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:0	R	0	Receiver Byte FIFO

19.3.4. CIR Receiver Interrupt Control Register(Default: 0x00000000)

Offset: 0x2C			Register Name: IR_RXINT
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:6	R/W	0	RAL RX FIFO Available Received Byte Level for interrupt and DMA request TRIGGER_LEVEL = RAL + 1
5	R/W	0	DRQ_EN RX FIFO DMA Enable 0: Disable 1: Enable When set to ‘1’, the Receiver FIFO DRQ is asserted if reaching RAL. The DRQ is de-asserted when condition fails.
4	R/W	0	RAI_EN RX FIFO Available Interrupt Enable 0: Disable 1: Enable When set to ‘1’, the Receiver FIFO IRQ is asserted if reaching RAL. The IRQ is de-asserted when condition fails.
3:2	/	/	/
1	R/W	0	RPEI_EN Receiver Packet End Interrupt Enable

			0: Disable 1: Enable
0	R/W	0	ROI_EN Receiver FIFO Overrun Interrupt Enable 0: Disable 1: Enable

19.3.5. CIR Receiver Status Register(Default: 0x00000000)

Offset: 0x30			Register Name: IR_RXSTA
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:6	R	0	RAC RX FIFO Available Counter 0: No available data in RX FIFO 1: 1 byte available data in RX FIFO 2: 2 byte available data in RX FIFO … 64: 64 byte available data in RX FIFO
5	/	/	/
4	R/W	0	RA RX FIFO Available 0: RX FIFO not available according its level 1: RX FIFO available according its level This bit is cleared by writing a ‘1’.
3:2	/	/	/
1	R/W	0	RPE Receiver Packet End Flag 0: STO was not detected. In CIR mode, one CIR symbol is receiving or not detected. 1: STO field or packet abort symbol (7’b0000,000 and 8’b0000,0000 for MIR and FIR) is detected. In CIR mode, one CIR symbol is received. This bit is cleared by writing a ‘1’.
0	R/W	0	ROI Receiver FIFO Overrun 0: Receiver FIFO not overrun 1: Receiver FIFO overrun This bit is cleared by writing a ‘1’.

19.3.6. CIR Configure Register(Default: 0x00001828)

Offset: 0x34			Register Name: IR_CIR
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:8	R/W	0x18	ITHR Idle Threshold for CIR The Receiver uses it to decide whether the CIR command has been received. If there is no CIR signal on the air, the receiver is staying in IDLE status. One active pulse will bring the receiver from IDLE status to Receiving status. After the CIR is end, the inputting signal will keep the specified level (high or low level) for a long time. The receiver can use this idle signal duration to decide that it has received the CIR command. The corresponding flag is asserted. If the corresponding interrupt is enabled, the interrupt line is asserted to CPU.

			When the duration of signal keeps one status (high or low level) for the specified duration ((ITHR + 1)*128 sample_clk), this means that the previous CIR command has been finished.
7:2	R/W	0xa	NTHR Noise Threshold for CIR When the duration of signal pulse (high or low level) is less than NTHR, the pulse is taken as noise and should be discarded by hardware. 0: all samples are recorded into RX FIFO 1: If the signal is only one sample duration, it is taken as noise and discarded. 2: If the signal is less than (<=) two sample duration, it is taken as noise and discarded. … 61: if the signal is less than (<=) sixty-one sample duration, it is taken as noise and discarded.
1:0	R/W	0	SCS Sample Clock Select for CIR 0: CIR sample_clk is ir_clk/64 1: CIR sample_clk is ir_clk/128 2: CIR sample_clk is ir_clk/256 3: CIR sample_clk is ir_clk/512

Chapter 20 USB OTG Controller

20.1. Overview

The USB OTG controller supports Host and device functions. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0 Specification. The USB2.0 OTG can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode, support high-speed (HS, 480-Mbps) and full-speed (FS, 12-Mbps) in Device mode.

The USB2.0 OTG controller (SIE) features:

- 64-Byte Endpoint 0 for Control Transfer
- Support up to 5 User-Configurable Endpoints for Bulk , Isochronous**,** Control and Interrupt bi-directional transfers
- Support High-Bandwidth Isochronous & Interrupt transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode

20.2. USB OTG Timing Diagram

Please refer USB2.0 Specification.

Chapter 21 USB Host

21.1. Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

It features:

- Include an internal DMA Controller for data transfer with memory.
- Comply with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Support only one USB Root Port shared between EHCI and OHCI

21.2. USB Host Block Diagram

The USB host controller System-Level block diagram is showed below:

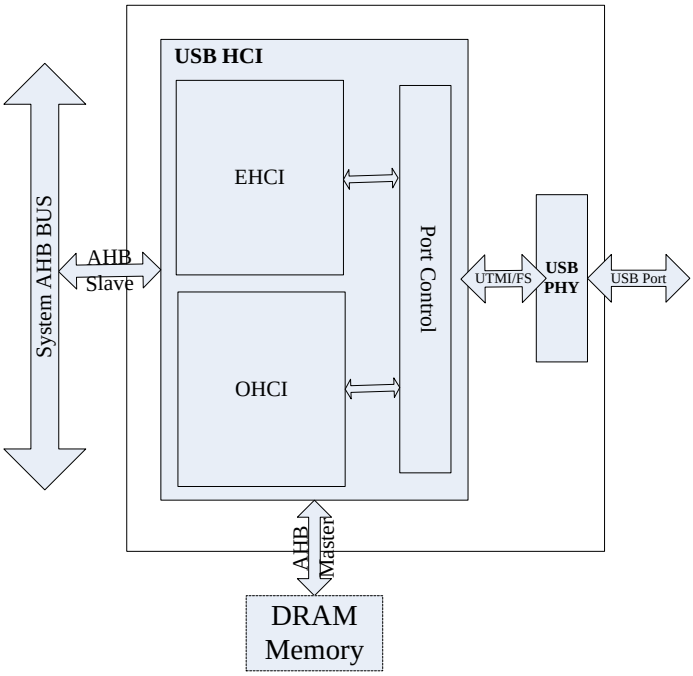


Figure21-1. USB Host Block Diagram

21.3. USB Host Timing Diagram

Please refer USB2.0 Specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

21.4. USB Host Register List

Module Name	Base Address
USB_HCI0	0x01C14000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x000	EHCI Capability register Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x00c	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01c	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x400	OHCI Revision Register
O_HcControl	0x404	OHCI Control Register
O_HcCommandStatus	0x408	OHCI Command Status Register
O_HcInterruptStatus	0x40c	OHCI Interrupt Status Register
O_HcInterruptEnable	0x410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x418	OHCI HCCA Base
O_HcPeriodCurrentED	0x41c	OHCI Period Current ED Base
O_HcControlHeadED	0x420	OHCI Control Head ED Base
O_HcControlCurrentED	0x424	OHCI Control Current ED Base
O_HcBulkHeadED	0x428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x42c	OHCI Bulk Current ED Base
O_HcDoneHead	0x430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x434	OHCI Frame Interval Register
O_HcFmRemaining	0x438	OHCI Frame Remaining Register
O_HcFmNumber	0x43c	OHCI Frame Number Register
O_HcPerioddicStart	0x440	OHCI Periodic Start Register
O_HcLSThreshold	0x444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x448	OHCI Root Hub Descriptor Register A
O_HcRhDesriptorB	0x44c	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x454	OHCI Root Hub Port Status Register

21.5. EHCI Register Description

21.5.1. EHCI Identification Register(Default: Implementation Dependent)

Offset:0x00	Register Name: CAPLENGTH

Bit	Read/Write	Default/Hex	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

21.5.2. EHCI Host Interface Version Number Register(Default:0x00000100)

Offset: 0x02			Register Name: HCIVERSION
Bit	Read/Write	Default/Hex	Description
15:0	R	0x0100	HCIVERSION This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

21.5.3. EHCI Host Control Structural Parameter Register(Default: Implementation Dependent)

Offset: 0x04			Register Name: HCSPARAMS
Bit	Read/Write	Default/Hex	Description
31:24	/	0	Reserved. These bits are reserved and should be set to zero.
23:20	R	0	Debug Port Number This register identifies which of the host controller ports is the debug port. The value is the port number (one based) of the debug port. This field will always be '0'.
19:16	/	0	Reserved. These bits are reserved and should be set to zero.
15:12	R	0	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s). This field will always be '0'.
11:8	R	0	Number of Port per Companion Controller(N_PCC) This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software. This field will always fix with '0'.
7	R	0	Port Routing Rules This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation: Value: 0 — The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. Value: 1 — The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array. This field will always be '0'.
6:4	/	0	Reserved. These bits are reserved and should be set to zero.
3:0	R	1	N_PORTS This field specifies the number of physical downstream ports

			implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f. This field is always 1.

21.5.4. EHCI Host Control Capability Parameter Register(Default: Implementation Dependent)

Offset: 0x08			Register Name: HCCPARAMS
Bit	Read/Write	Default/Hex	Description
31:16	/	0	Reserved These bits are reserved and should be set to zero.
15:18	R	0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capabiliby. The pointer value must be 40h or greater if implemented to maintain to consistency of the PCI header defined for this calss of device. The value of this field is always '00b'.
7:4	R		Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	R	0	Reserved These bits are reserved and should be set to zero.
2	R		Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.
1	R		Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller.The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1,then system software can specify and use the frame list in the USBCMD register Frame List Size field to cofigure the host controller. The frame list must always aligned on a 4K page boundary.This requirement ensures that the frame list is always physically contiguous.
0	R	0	Reserved These bits are reserved for future use and should return a value of zero when read.

21.5.5. EHCI Companion Port Route Description(Default: Undefined)

Offset: 0x0C			Register Name: HCSP-PORTROUTE
Bit	Read/Write	Default/Hex	Description
31:0	R	x	HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is

			mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.

21.5.6. EHCI USB Command Register(Default: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one))

<table>
<tr><td colspan="3">Offset: 0x10</td><td>Register Name: USBCMD</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:24</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>23:16</td><td>R/W</td><td>0x08</td><td>Interrupt Threshold Control
The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:
<table>
<tr><td>Value</td><td>Minimum Interrupt Interval</td></tr>
<tr><td>0x00</td><td>Reserved</td></tr>
<tr><td>0x01</td><td>1 micro-frame</td></tr>
<tr><td>0x02</td><td>2 micro-frame</td></tr>
<tr><td>0x04</td><td>4 micro-frame</td></tr>
<tr><td>0x08</td><td>8 micro-frame(default, equates to 1 ms)</td></tr>
<tr><td>0x10</td><td>16 micro-frame(2ms)</td></tr>
<tr><td>0x20</td><td>32 micro-frame(4ms)</td></tr>
<tr><td>0x40</td><td>64 micro-frame(8ms)</td></tr>
</table>
Any other value in this register yields undefined results.
The default value in this field is 0x08 .
Software modifications to this bit while HC Halted bit equals to zero results in undefined behavior.</td></tr>
<tr><td>15:12</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>11</td><td>R/W or R</td><td>0</td><td>Asynchronous Schedule Park Mode Enable(OPTIONAL)
If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</td></tr>
<tr><td>10</td><td>/</td><td>0</td><td>Reserved
These bits are reserved and should be set to zero.</td></tr>
<tr><td>9:8</td><td>R/W or R</td><td>0</td><td>Asynchronous Schedule Park Mode Count(OPTIONAL)
Asynchronous Park Capability bit in the HCCPARAMS register is a one,
Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.
Valid value are 0x1 to 0x3.Software must not write a zero to this bit</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>when Park Mode Enable is a one as it will result in undefined behavior.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>Light Host Controller Reset(OPTIONAL)
This control bit is not required.
If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships).
A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it si safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</td></tr>
<tr><td>6</td><td>R/W</td><td>0</td><td>Interrupt on Async Advance Doorbell
This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-
Ware must write a 1 to this bit to ring the doorbell.
When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.
The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.
Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</td></tr>
<tr><td>5</td><td>R/W</td><td>0</td><td>Asynchronous Schedule Enable
This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:
<table>
<tr><th>Bit Value</th><th>Meaning</th></tr>
<tr><td>0</td><td>Do not process the Asynchronous Schedule.</td></tr>
<tr><td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr>
</table>
The default value of this field is ‘0b’.</td></tr>
<tr><td>4</td><td>R/W</td><td>0</td><td>Periodic Schedule Enable
This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:
<table>
<tr><th>Bit Value</th><th>Meaning</th></tr>
<tr><td>0</td><td>Do not process the Periodic Schedule.</td></tr>
<tr><td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr>
</table>
The default value of this field is ‘0b’.</td></tr>
<tr><td>3:2</td><td>R/W or R</td><td>0</td><td>Frame List Size
This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the Frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index. Values mean:
<table>
<tr><th>Bits</th><th>Meaning</th></tr>
<tr><td>00b</td><td>1024 elements(4096bytes)Default value</td></tr>
<tr><td>01b</td><td>512 elements(2048byts)</td></tr>
<tr><td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr>
<tr><td>11b</td><td>reserved</td></tr>
</table>
The default value is ‘00b’.</td></tr>
</table>

1	R/W	0	Host Controller Reset This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.
0	R/W	0	Run/Stop When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16 micro-frames after software clears this bit. The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state. Software must not write a one to this field unless the Host Controller is in the Halt State. The default value is 0x0.

21.5.7. EHCI USB Status Register(Default: 0x00001000)

Offset: 0x14			Register Name: USBSTS
Bit	Read/Write	Default/Hex	Description
31:16	/	0	Reserved These bits are reserved and should be set to zero.
15	R	0	Asynchronous Schedule Status The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	R	0	Periodic Schedule Status The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to immediately disable or enable the Periodic Schedule when software transitions the Periodic Schedule Enable bit in the USBCMD register. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).

13	R	0	Reclamation This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	1	HC Halted This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error). The default value is '1'.
11:6	/	0	Reserved These bits are reserved and should be set to zero.
5	R/WC	0	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.
4	R/WC	0	Host System Error The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.
3	R/WC	0	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.
2	R/WC	0	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0	USB Error Interrupt(USBERRINT) The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both. This bit and USBINT bit are set.
0	R/WC	0	USB Interrupt(USBINT) The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes)

21.5.8. EHCI USB Interrupt Enable Register(Default: 0x00000000)

Offset: 0x18			Register Name: USBINTR
Bit	Read/Write	Default/Hex	Description

31:6	/	0	Reserved These bits are reserved and should be zero.
5	R/W	0	Interrupt on Async Advance Enable When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	R/W	0	Host System Error Enable When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	R/W	0	Frame List Rollover Enable When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	R/W	0	Port Change Interrupt Enable When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.
1	R/W	0	USB Error Interrupt Enable When this bit is 1, and the USBERRINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.
0	R/W	0	USB Interrupt Enable When this bit is 1, and the USBINT bit in the USBSTS register is 1,the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit

21.5.9. EHCI Frame Index Register(Default: 0x00000000)

Offset: 0x1c			Register Name: FRINDEX
Bit	Read/Write	Default/Hex	Description
31:14	/	0	Reserved These bits are reserved and should be zero.
13:0	R/W	0	Frame Index The value in this register increment at the end of each time frame (e.g. micro-frame).Bits[N:3] are used for the Frame List current index. It Means that each location of the frame list is accessed 8 times(frames or Micro-frames) before moving to the next index. The following illustrates Values of N based on the value of the Frame List Size field in the USBCMD register.

USBCMD[Frame List Size]	Number Elements	N
00b	1024	12
01b	512	11
10b	256	10
11b	Reserved	

Note: This register must be written as a DWord. Byte writes produce undefined results.

21.5.10. EHCI Periodic Frame List Base Address Register(Default: Undefined)

Offset: 0x24			Register Name: PERIODICLISTBASE
Bit	Read/Write	Default/Hex	Description

31:12	R/W	x	Base Address These bits correspond to memory address signals [31:12], respectively. This register contains the beginning address of the Periodic Frame List in the system memory. System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.
11:0	/	x	Reserved Must be written as 0x0 during runtime, the values of these bits are undefined.

Note: Writes must be Dword Writes.

21.5.11. EHCI Current Asynchronous List Address Register(Default: Undefined)

Offset: 0x28			Register Name: ASYNCLISTADDR
Bit	Read/Write	Default/Hex	Description
31:5	R/W	x	Link Pointer (LP) This field contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5], respectively.
4:0	/	/	Reserved These bits are reserved and their value has no effect on operation. Bits in this field cannot be modified by system software and will always return a zero when read.

Note: Write must be DWord Writes.

21.5.12. EHCI Configure Flag Register(Default: 0x00000000)

Offset: 0x50			Register Name: CONFIGFLAG
Bit	Read/Write	Default/Hex	Description
31:1	/	0	Reserved These bits are reserved and should be set to zero.
0	R/W	0	Configure Flag(CF) Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow: Value: 0 — Port routing control logic default-routs each port to an implementation dependent classic host controller. Value: 1 — Port routing control logic default-routs all ports to this host controller. The default value of this field is '0'.

Note: This register is not use in the normal implementation.

21.5.13. EHCI Port Status and Control Register(Default: 0x00002000(w/PPC set to one); 0x00003000(w/PPC set to a zero))

<table>
<tr><td colspan="3">Offset: 0x54</td><td>Register Name: PORTSC</td></tr>
<tr><td>Bit</td><td>Read/Write</td><td>Default/Hex</td><td>Description</td></tr>
<tr><td>31:22</td><td>/</td><td>0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>21</td><td>R/W</td><td>0</td><td>Wake on Disconnect Enable(WKDSCNNT_E)
Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>20</td><td>R/W</td><td>0</td><td>Wake on Connect Enable(WKCNNT_E)
Writing this bit to a one enable the port to be sensitive to device connects as wake-up events.
This field is zero if Port Power is zero.
The default value in this field is ‘0’.</td></tr>
<tr><td>19:16</td><td>R/W</td><td>0</td><td>Port Test Control
The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow:
<table>
<tr><td>Bits</td><td>Test Mode</td></tr>
<tr><td>0000b</td><td>The port is NOT operating in a test mode.</td></tr>
<tr><td>0001b</td><td>Test J_STATE</td></tr>
<tr><td>0010b</td><td>Test K_STATE</td></tr>
<tr><td>0011b</td><td>Test SE0_NAK</td></tr>
<tr><td>0100b</td><td>Test Packet</td></tr>
<tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr>
<tr><td>0110b-1111b</td><td>Reserved</td></tr>
</table>
The default value in this field is ‘0000b’.</td></tr>
<tr><td>15:14</td><td>R/W</td><td>0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>13</td><td>R/W</td><td>1</td><td>Port Owner
This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.
System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device).Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.
Default Value = 1b.</td></tr>
<tr><td>12</td><td>/</td><td>0</td><td>Reserved
These bits are reserved for future use and should return a value of zero when read.</td></tr>
<tr><td>11:10</td><td>R</td><td>0</td><td>Line Status
These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.
The encoding of the bits are:</td></tr>
</table>

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Bit[11:10]</th><th>USB State</th><th>Interpretation</th></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.
</td></tr>
<tr><td>9</td><td>/</td><td>0</td><td>Reserved
This bit is reserved for future use, and should return a value of zero when read.</td></tr>
<tr><td>8</td><td>R/W</td><td>0</td><td>Port Reset
1=Port is in Reset. 0=Port is not in Reset. Default value = 0.
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes.
Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit.
Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.
The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a one when the HC Halted bit is a one.
This field is zero if Port Power is zero.</td></tr>
<tr><td>7</td><td>R/W</td><td>0</td><td>Suspend
Port Enabled Bit and Suspend bit of this register define the port states as follows:
<table>
<tr><th>Bits[Port Enables, Suspend]</th><th>Port State</th></tr>
<tr><td>0x</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
<tr><td>11</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Not that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
① Software sets the Force Port Resume bit to a zero(from a one).
② Software sets the Port Reset bit to a one(from a zero).
If host software sets this bit to a one when the port is not enabled(i.e.</td></tr>
</table>

			Port enabled bit is a zero), the results are undefined. This field is zero if Port Power is zero. The default value in this field is '0'.
6	R/W	0	Force Port Resume 1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0. This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the effects on the bus are undefined. Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.
5	R/WC	0	Over-current Change Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.
4	R	0	Over-current Active 0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed. The default value of this bit is '0'.
3	R/WC	0	Port Enable/Disable Change Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change. For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.
2	R/W	0	Port Enabled/Disabled 1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port except for reset.

			The default value of this field is '0'. This field is zero if Port Power is zero.
1	R/WC	0	Connect Status Change 1=Change in Current Connect Status, 0=No change, Default=0. Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.
0	R	0	Current Connect Status Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set. This field is zero if Port Power zero.

Note: This register is only reset by hardware or in response to a host controller reset.

21.6. OHCI Register Description

21.6.1. HcRevision Register(Default: 0x00000010)

Offset: 0x400				Register Name: HcRevision
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:8	/	/	0x00	Reserved
7:0	R	R	0x10	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.

21.6.2. HcControl Register(Default: 0x00000000)

Offset: 0x404				Register Name: HcRevision
	Read/Write			Description
Bit	HCD	HC	Default/Hex	
31:11	/	/	0x00	Reserved
10	R/W	R	0x0	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	R/W	R/W	0x0	RemoteWakeupConnected This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.

8	R/W	R	0x0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	R/W	0x0	HostControllerFunctionalState for USB 00b USBReset 01b USBResume 10b USBOperational 11b USBSuspend A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartoFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
5	R/W	R	0x0	BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.
4	R/W	R	0x0	ControlListEnable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.
3	R/W	R	0x0	IsochronousEnable This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	R	0x0	PeriodicListEnable This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	R	0x0	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving

				another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. CBSR: No. of Control EDs Over Bulk EDs Served 0: 1:1 1: 2:1 2: 3:1 3: 4:1 The default value is 0x0.

21.6.3. HcCommandStatus Register(Default: 0x00000000)

Offset: 0x408				Register Name: HcCommandStatus
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problem.
15:4	/	/	0x0	Reserved
3	R/W	R/W	0x0	OwershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	R/W	0x0	BulklListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	R/W	R/E	0x0	HostControllerReset This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSuspend state in which most of the operational registers are reset except those stated otherwise; e.g,

				the InteruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

21.6.4. HcInterruptStatus Register(Default: 0x00000000)

Offset: 0x40c				Register Name: HcInterruptStatus
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:7	/	/	0x0	Reserved
6	R/W	R/W	0x0	RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	R/W	0x0	FrameNumberOverflow This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
4	R/W	R/W	0x0	UnrecoverableError This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	R/W	R/W	0x0	ResumeDetected This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRseume state.
2	R/W	R/W	0x0	StartofFrame This bit is set by HC at each start of frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	R/W	0x0	WritebackDoneHead This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	R/W	0x0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be Incremented.

21.6.5. HcInterruptEnable Register(Default: 0x00000000)

Offset: 0x410				Register Name: HcInterruptEnable Register
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31	R/W	R	0x0	MasterInterruptEnable A ‘0’ writtern to this field is ignored by HC. A ‘1’ written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.
30:7	/	/	0x0	Reserved
6	R/W	R	0x0	RootHubStatusChange Interrupt Enable

				0 Ignore; 1 Enable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable 0 Ignore; 1 Enable interrupt generation due to Scheduling Overrun;

21.6.6. HcInterruptDisable Register(Default: 0x00000000)

Offset: 0x414				Register Name: HcInterruptDisable Register
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.
30:7	/	/	0x00	Reserved
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Root Hub Status Change;
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Frame Number Over Flow;
4	R/W	R	0x0	UnrecoverableError Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Unrecoverable Error;
3	R/W	R	0x0	ResumeDetected Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Start of Flame;
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable

				0 Ignore; 1 Disable interrupt generation due to Write back Done Head;
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable 0 Ignore; 1 Disable interrupt generation due to Scheduling Overrun;

21.6.7. HcHCCA Register(Default: 0x00000000)

Offset: 0x418				Register Name: HcHCCA
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

21.6.8. HcPeriodCurrentED Register(Default: 0x00000000)

Offset: 0x41c				Register Name: HcPeriodCurrentED(PCED)
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:4	R	R/W	0x0	PCED[31:4] This is used by HC to point to the head of one of the Periodec list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	R	R	0x0	PCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

21.6.9. HcControlHeadED Register(Default: 0x00000000)

Offset: 0x420				Register Name: HcControlHeadED[CHED]
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:4	R/W	R	0x0	EHCD[31:4] The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	EHCD[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

21.6.10. HcControlCurrentED Register(Default: 0x00000000)

Offset: 0x424				Register Name: HcControlCurrentED[CCED]
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:4	R/W	R/W	0x0	CCED[31:4] The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0	R	R	0x0	CCED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, bit 0 to bit 3, must be zero in this field.

21.6.11. HcBulkHeadED Register(Default: 0x00000000)

Offset: 0x428				Register Name: HcBulkHeadED[BHED]
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:4	R/W	R	0x0	BHED[31:4] The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	R	R	0x0	BHED[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, bit 0 to bit 3, must be zero in this field.

21.6.12. HcBulkCurrentED Register(Default: 0x00000000)

Offset: 0x42c				Register Name: HcBulkCurrentED [BCED]
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:4	R/W	R/W	0x0	BulkCurrentED[31:4] This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0	R	R	0x0	BulkCurrentED [3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.

21.6.13. HcDoneHead Register(Default: 0x00000000)

Offset: 0x430				Register Name: HcDoneHead
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0	R	R	0x0	HcDoneHead[3:0] Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, bit 0 to bit 3, must be zero in this field.

21.6.14. HcFmInterval Register(Default: 0x00002EDF)

Offset: 0x434				Register Name: HcFmInterval Register
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31	R/W	R	0x0	FrameIntervalToggler HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	R	0x0	FSLargestDataPacket This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14	/	/	0x0	Reserved
13:0	R/W	R	0x2edf	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

21.6.15. HcFmRemaining Register(Default: 0x00000000)

Offset: 0x438				Register Name: HcFmRemaining
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31	R	R/W	0x0	FrameRemaining Toggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	/	/	0x0	Reserved
13:0	R	RW	0x0	FramRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC

				re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

21.6.16. HcFmNumber Register(Default: 0x00000000)

Offset: 0x43c				Register Name: HcFmNumber
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:16	/	/	/	Reserved
15:0	R	R/W	0x0	FrameNumber This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0x0 after 0x0ffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

21.6.17. HcPeriodicStart Register(Default: 0x00000000)

Offset: 0x440				Register Name: HcPeriodicStatus
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:14	/	/	/	Reserved
13:0	R/W	R	0x0	PeriodicStart After hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 0x2A3F. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

21.6.18. HcLSThreshold Register(Default: 0x00000628)

Offset: 0x444				Register Name: HcLSThreshold
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:12	/	/	/	Reserved
11:0	R/W	R	0x0628	LSThreshold This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

21.6.19. HcRhDescriptorA Register(Default: 0x02001201)

Offset: 0x448				Register Name: HcRhDescriptorA
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:24	R/W	R	0x2	PowerOnToPowerGoodTime[POTPGT]

				This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.
23:13				Reserved
12	R/W	R	1	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 Over-current status is reported collectively for all downstream ports. 1 No overcurrent protection supported.
11	R/W	R	0	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 Over-current status is reported collectively for all downstream ports. 1 Over-current status is reported on per-port basis.
10	R	R	0x0	Device Type This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	R	1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid when the NoPowerSwitching field is cleared. 0 All ports are powered at the same time. 1 Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switch. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
8	R/W	R	0	NoPowerSwithcing These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 Ports are power switched. 1 Ports are always powered on when the HC is powered on.
7:0	R	R	0x01	NumberDownstreamPorts These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1.

21.6.20. HcRhDescriptorB Register(Default: 0x00000000)

Offset: 0x44c				Register Name: HcRhDescriptorB Register
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:16	R/W	R	0x0	PortPowerControlMask Each bit indicates if a port is affected by a global power control

				command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode = 0), this field is not valid. Bit0 Reserved Bit1 Ganged-power mask on Port #1. Bit2 Ganged-power mask on Port #2. … Bit15 Ganged-power mask on Port #15.
15:0	R/W	R	0x0	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit0 Reserved Bit1 Device attached to Port #1. Bit2 Device attached to Port #2. … Bit15 Device attached to Port #15.

21.6.21. HcRhStatus Register(Default: 0x00000000)

Offset: 0x450				Register Name: HcRhStatus Register
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31	W	R	0	(write)ClearRemoteWakeupEnable Write a ‘1’ clears DeviceRemoteWakeupEnable. Write a ‘0’ has no effect.
30:18	/	/	0x0	Reserved
17	R/W	R	0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a ‘1’.Writing a ‘0’ has no effect.
16	R/W	R	0x0	(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as ‘0’. (write)SetGlobalPower In global power mode (PowerSwitchingMode=0), this bit is written to ‘1’ to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a ‘0’ has no effect.
15	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0 ConnectStatusChange is not a remote wakeup event. 1 ConnectStatusChange is a remote wakeup event. (write)SetRemoteWakeupEnable Writing a ‘1’ sets DeviceRemoveWakeupEnable. Writing a ‘0’ has no effect.
14:2				Reserved

1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

21.6.22. HcRhPortStatus Register(Default: 0x00000100)

Offset: 0x454				Register Name: HcRhPortStatus
	Read/Write			
Bit	HCD	HC	Default/Hex	Description
31:21	/	/	0x0	Reserved
20	R/W	R/W	0x0	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 port reset is not complete 1 port reset is complete
19	R/W	R/W	0x0	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortOverCurrentIndicator 1 PortOverCurrentIndicator has changed
18	R/W	R/W	0x0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 resume is not completed 1 resume completed
17	R/W	R/W	0x0	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 no change in PortEnableStatus 1 change in PortEnableStatus
16	R/W	R/W	0x0	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset,SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if

				the port is disconnected. 0 no change in PortEnableStatus 1 change in PortEnableStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10	/	/	0x0	Reserved
9	R/W	R/W	-	(read)LowSpeedDeviceAttached This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When cleared, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 full speed device attached 1 low speed device attached (write)ClearPortPower The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.
8	R/W	R/W	0x1	(read)PortPowerStatus This bit reflects the port's power status, irrelevant of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0 port power is off 1 port power is on (write)SetPortPower The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. Note: This bit is always read as '1b' if power switching is not supported.
7:5	/	/	0x0	Reserved
4	R/W	R/W	0x0	(read)PortResetStatus When this bit is set by writing to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 port reset signal is not active 1 port reset signal is active (write)SetPortReset The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

<table>
<tr><td>3</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortOverCurrentIndicator
This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.
<table><tr><td>0</td><td>no overcurrent condition.</td></tr><tr><td>1</td><td>overcurrent condition detected.</td></tr></table>
(write)ClearSuspendStatus
The HCD writes a ‘1’ to initiate a resume. Writing a ‘0’ has no effect. A resume is initiated only if PortSuspendStatus is set.</td></tr>
<tr><td>2</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortSuspendStatus
This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
<table><tr><td>0</td><td>port is not suspended</td></tr><tr><td>1</td><td>port is suspended</td></tr></table>
(write)SetPortSuspend
The HCD sets the PortSuspendStatus bit by writing a ‘1’ to this bit. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</td></tr>
<tr><td>1</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)PortEnableStatus
This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
<table><tr><td>0</td><td>port is disabled</td></tr><tr><td>1</td><td>port is enabled</td></tr></table>
(write)SetPortEnable
The HCD sets PortEnableStatus by writing a ‘1’. Writing a ‘0’ has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, and sets ConnectStatusChange instead. This informs the driver that it attempts to enable a disconnected Port.</td></tr>
<tr><td>0</td><td>R/W</td><td>R/W</td><td>0x0</td><td>(read)CurrentConnectStatus
This bit reflects the current state of the downstream port.
<table><tr><td>0</td><td>No device connected</td></tr><tr><td>1</td><td>Device connected</td></tr></table>
(write)ClearPortEnable
The HCD writes a ‘1’ to clear the PortEnableStatus bit. Writing ‘0’ has no effect. The CurrentConnectStatus is not affected by any write.</td></tr>
</table>

				Note: This bit is always read as '1' when the attached device is non-removable(DviceRemoveable[NumberDownstreamPort]).

21.7. USB Host Special Requirement

Name	Description
HCLK	System clock (provided by AHB bus clock). This clock needs to be >30MHz.
CLK60M	Clock from PHY for HS SIE, is constant to be 60MHz.
CLK48M	Clock from PLL for FS/LS SIE, is constant to be 48MHz.

Chapter 22 Audio Codec

22.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplifier.

It features:

- On-chip 24-bit DAC for play-back
- On-chip 24-bit ADC for recorder
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- Support 192K and 96K sample
- Support Microphone recorder
- Stereo headphone amplifier that can be operated in capless headphone mode
- Support Virtual Ground to automatically change to True Ground to protect headphone amplifier and make function work in normal mode

22.2. Audio Codec Block Diagram

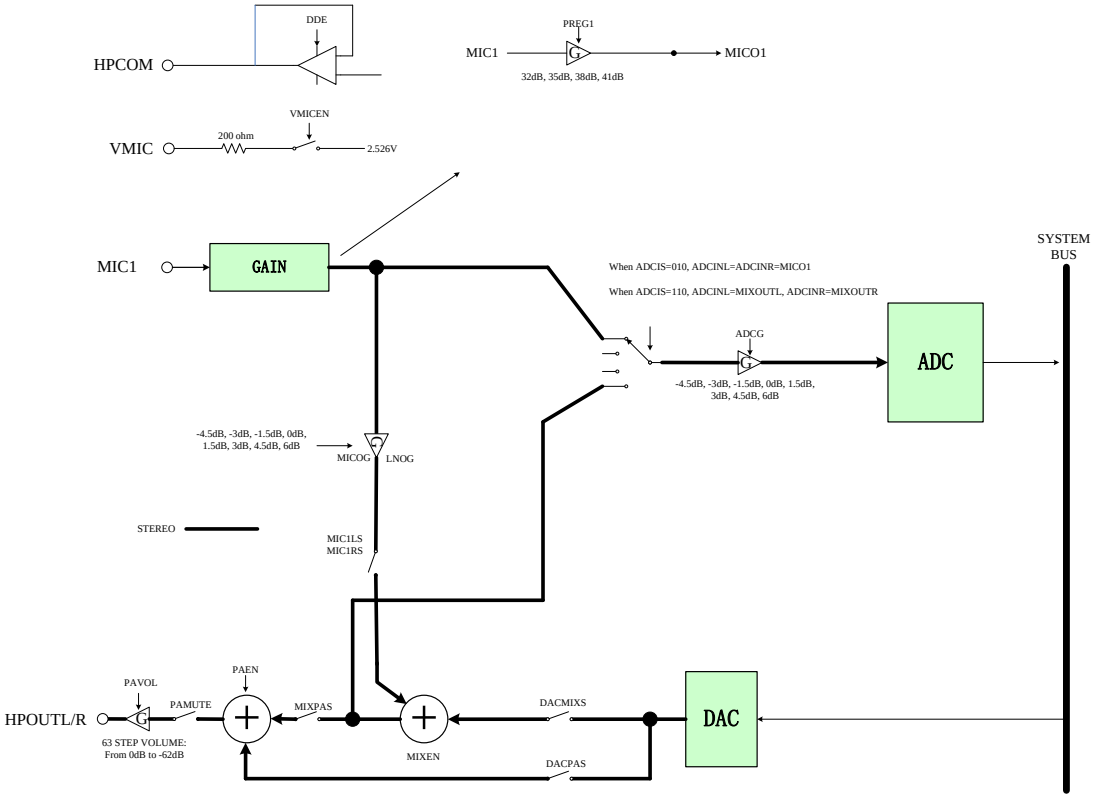


Figure22-1. Audio Codec Block Diagram

22.3. Audio Codec Register List

Module Name	Base Address
Audio Codec	0x01C22C00

Register Name	Offset	Description
AC_DAC_DPC	0x00	DAC Digital Part Control Register
AC_DAC_FIFOC	0x04	DAC FIFO Control Register
AC_DAC_FIFOS	0x08	DAC FIFO Status Register
AC_DAC_TXDATA	0x0C	DAC TX Data Register
AC_DAC_ACTL	0x10	DAC Analog Control Register
AC_ADC_FIFOC	0x1C	ADC FIFO Control Register
AC_ADC_FIFOS	0x20	ADC FIFO Status Register
AC_ADC_RXDATA	0x24	ADC RX Data Register
AC_ADC_ACTL	0x28	ADC Analog Control Register
AC_DAC_CNT	0x30	DAC TX FIFO Counter Register
AC_ADC_CNT	0x34	ADC RX FIFO Counter Register

22.4. Audio Codec Register Description

22.4.1. DAC Digital Part Control Register(Default: 0x00000000)

Offset: 0x00			Register Name: AC_DAC_DPC
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	EN_DA. DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU. Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA. DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN. High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL. Digital volume control: dvc, ATT=(DVC[5:0]-2)*(-1.16dB) 62 steps, -1.16dB/step
11:0	/	/	/

22.4.2. DAC FIFO Control Register(Default: 0x00000000)

Offset: 0x4			Register Name: AC_DAC_FIFOC
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	DAC_FS. Sample Rate of DAC 000: 48KHz 010: 24KHz 100: 12KHz 110: 192KHz

			001: 32KHz 011: 16KHz 101: 8KHz 111: 96KHz 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	R/W	FIR Version 0:64-Tap FIR 1:32-Tap FIR
27	/	/	/
26	R/W	0x0	SEND_LASAT. Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
25	/	/	/
24	R/W	0x0	For 24-bits transmitted audio sample: 0: FIFO_I[23:0] = {TXDATA[31:8]} 1: Reserved For 16-bits transmitted audio sample: 0: FIFO_I[23:0] = {TXDATA[31:16], 8'b0} 1: FIFO_I[23:0] = {TXDATA[15:0], 8'b0}
23	/	/	/
22:21	R/W	0x0	DAC_DRQ_CLR_CNT. When TX FIFO available room less than or equal N, DRQ Request will be de-asserted. N is defined here: 000: IRQ/DRQ Deasserted when WLEVEL > TXTL 01: 4 10: 8 11: 16
20:15	/	/	/
14:8	R/W	0x10	TX FIFO Empty Trigger Level (TXTL[6:0]) Interrupt and DMA request trigger level for TX FIFO normal condition. IRQ/DRQ Generated when WLEVEL ≤ TXTL
7	R/W	0x0	ADDA_LOOP_EN. ADDA loop Enable, adda 0: Disable 1: Enable
6	R/W	0x0	DAC_MONO_EN. DAC Mono Enable 0: Stereo, 64 levels FIFO 1: mono, 128 levels FIFO When enabled, L & R channel send same data
5	R/W	0x0	TX_SAMPLE_BITS. Transmitting Audio Sample Resolution 0: 16 bits 1: 24 bits
4	R/W	0x0	DAC_DRQ_EN. DAC FIFO Empty DRQ Enable 0: Disable 1: Enable
3	R/W	0x0	DAC_IRQ_EN. DAC FIFO Empty IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	FIFO_UNDERRUN_IRQ_EN. DAC FIFO Under Run IRQ Enable

			0: Disable 1: Enable
1	R/W	0x0	FIFO_OVERRUN_IRQ_EN. DAC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	FIFO_FLUSH. DAC FIFO Flush Write '1' to flush TX FIFO, self clear to '0'

22.4.3. DAC FIFO Status Register(Default: 0x00808008)

Offset: 0x8			Register Name: AC_DAC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R	0x1	TX_EMPTY. TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
22:8	R	0x80	TXE_CNT. TX FIFO Empty Space Word Counter
7:4	/	/	/
3	R/W	0x1	TXE_INT. TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	R/W	0x0	TXU_INT. TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt Write '1' to clear this interrupt
1	R/W	0x0	TXO_INT. TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
0	/	/	/

22.4.4. DAC TX DATA Register(Default: 0x00000000)

Offset: 0xC			Register Name: AC_DAC_TXDATA
Bit	Read/Write	Default/Hex	Description
31:0	W	0x0	TX_DATA. Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.

22.4.5. DAC Analog Control Register(Default: 0x05B00000)

Offset:0x10			Register Name: AC_DAC_ACTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	DACAREN.

			Internal DAC Analog Right channel Enable 0:Disable 1:Enable
30	R/W	0x0	DACALEN. Internal DAC Analog Left channel Enable 0:Disable 1:Enable
29	R/W	0x0	MIXEN. Analog Output Mixer Enable 0:Disable 1:Enable
28:27	/	/	/
26	R/W	0x1	LNG. Line-in gain stage to output mixer Gain Control 0: -1.5dB 1: 0dB
25:23	R/W	0x3	FMG. FM Input to output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
22:20	R/W	0x3	MICG. MIC gain stage to output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
19	R/W	0x0	LLNS. Left LINEIN gain stage to left output MP mute 0-mute; 1-Not mute When LNRDF is 0, left select LINEINL When LNRDF is 1, left select LINEINL-LINEINR
18	R/W	0x0	RLNS. Right LINEIN gain stage to right output MP mute 0-mute; 1-Not mute When LNRDF is 0, right select LINEINR When LNRDF is 1, right select LINEINL-LINEINR
17	R/W	0x0	LFMS. Left FM to left output MP mute 0:mute 1:Not mute
16	R/W	0x0	RFMS. right FM to right output MP mute 0:mute 1:Not mute
15	R/W	0x0	LDACLMIXS. Left DAC to left output mixer Mute 0:Mute 1:Not mute
14	R/W	0x0	RDACRMIXS. Right DAC to right output mixer Mute 0:Mute 1:Not mute
13	R/W	0x0	LDACRMIXS. Left DAC to right output mixer Mute, 0:Mute 1:Not mute
12	R/W	0x0	MIC LS. MIC to output mixer left channel mute 0: mute 1: Not mute

11	R/W	0x0	MIC RS. MIC to output mixer right channel mute 0: mute 1: Not mute
10	R/W	0x0	/
9	R/W	0x0	/
8	R/W	0x0	DACPAS. DAC to PA Mute 0-Mute 1-Not mute
7	R/W	0x0	MIXPAS. Output Mixer to PA mute 0: Mute 1: Not mute
6	R/W	0x0	PAMUTE. All input source to PA mute, including Output mixer and Internal DAC, (): 0:Mute 1: Not mute
5:0	R/W	0x0	PAVOL. PA Volume Control, (PAVOL): Total 64 level, from 0dB to -62dB, 1dB/step，mute when 000000

22.4.6. ADC FIFO Control Register(Default: 0x00000F00)

Offset: 0x1C			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0x0	ADFS. Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz 011: 16KHz 101: 8KHz 111: Reserved
28	R/W	0x0	EN_AD. ADC Digital Part Enable, en_ad 0: Disable 1: Enable
27:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE. RX FIFO Output Mode (Mode 0, 1) 0: Expanding ‘0’ at LSB of TX FIFO register 1: Expanding received sample sign bit at MSB of TX FIFO register For 24-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8’h0} Mode 1: Reserved For 16-bits received audio sample: Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16’h0} Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}
23:13	/	/	/
12:8	R/W	0xF	RX_FIFO_TRG_LEVEL. RX FIFO Trigger Level (RXTL[4:0]) Interrupt and DMA request trigger level for TX FIFO normal condition

			IRQ/DRQ Generated when WLEVEL ＞ RXTL[4:0] Note: WLEVEL represents the number of valid samples in the RX FIFO
7	R/W	0x0	ADC_MONO_EN. ADC Mono Enable. 0: Stereo, 16 levels FIFO 1: mono, 32 levels FIFO When set to '1', Only left channel samples are recorded
6	R/W	0x0	RX_SAMPLE_BITS. Receiving Audio Sample Resolution 0: 16 bits 1: 24 bits
5	/	/	/
4	R/W	0x0	ADC_DRQ_EN. ADC FIFO Data Available DRQ Enable. 0: Disable 1: Enable
3	R/W	0x0	ADC_IRQ_EN. ADC FIFO Data Available IRQ Enable. 0: Disable 1: Enable
2	/	/	/
1	R/W	0x0	ADC_OVERRUN_IRQ_EN. ADC FIFO Over Run IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	ADC_FIFO_FLUSH. ADC FIFO Flush. Write '1' to flush TX FIFO, self clear to '0'.

22.4.7. ADC FIFO Status Register(Default: 0x00000000)

Offset: 0x20			Register Name: AC_ADC_FIFOS
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R	0x0	RXA. RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:14	/	/	/
13:8	R	0x0	RXA_CNT. RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W	0x0	RXA_INT. RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/W	0x0	RXO_INT. RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ

			Write '1' to clear this interrupt
0	/	/	/

22.4.8. ADC RX DATA Register(Default: 0x00000000)

Offset: 0x24			Register Name: AC_ADC_RXDATA
Bit	Read/Write	Default/Hex	Description
31:0	R	0x0	RX_DATA. RX Sample Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.

22.4.9. ADC Analog Control Register(Default: 0x0534814C)

Offset:0x28			Register Name: AC_PA_ADC_ACTRL
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	ADCREN. ADC Right Channel Enable 0-Disable 1-Enable
30	R/W	0x0	ADCLEN. ADC Left Channel Enable 0-Disable 1-Enable
29	R/W	0x0	PREG1EN. MIC1 pre-amplifier Enable 0-Disable 1-Enable
28	R/W	0x0	PREG2EN. MIC2 pre-amplifier Enable 0-Disable 1-Enable
27	R/W	0x0	VMICEN. VMIC pin voltage enable 0: disable 1: enable
26:25	R/W	0x2	PREG1. MIC1 pre-amplifier Gain Control 00: 0dB 01: 35dB 10: 38dB 11: 41dB
24:23	R/W	0x2	PREG2. MIC2 pre-amplifier Gain Control 00: 0dB 01: 35dB 10: 38dB 11: 41dB
22:20	R/W	0x3	ADCG. ADC Input Gain Control 000: -4.5dB 001: -3dB 010: -1.5dB 011: 0dB 100: 1.5dB

			101: 3dB 110: 4.5dB 111: 6dB
19:17	R/W	0x2	ADCIS. ADC input source select 000: left select LINEINL, right select LINEINR; or, both select LINEINL-LINEINR, depending on LNRDF (bit 16) 001: left channel select FMINL & right channel select FMINR 010: left and right channel both select MIC1 gain stage output 011: left and right channel both select MIC2 gain stage output 100: left select MIC1 gain stage output & right select MIC2 gain stage output 101: left and right both select MIC1 gain stage plus MIC2 gain stage output 110: left select output mixer L & right select output Mixer right 111: left select LINEINL or LINEINL-LINEINR, depending on LNRDF (bit 16), right select MIC1 gain stage
16	R/W	0x0	LNRDF. Line-in-r function define 0: Line-in right channel which is independent of line-in left channel 1: negative input of line-in left channel for fully differential application
15:13	R/W	0x4	LNPREG. Line-in pre-amplifier Gain Control From -12dB to 9dB, 3dB/step, default is 0dB
12	R/W	0x0	MIC1NEN. Mic1outn enable 0: disable 1: enable
11:9	/	/	/
8	R/W	0x1	DITHER. ADC dither on/off control 0: dither off 1: dither on
7:6	R/W	0x1	/
5	/	/	/
4	R/W	0x0	PA_EN. PA Enable 0-disable 1-enable
3	R/W	0x1	DDE. Headphone direct-drive enable, (DDE): 0-disable 1-enable
2	R/W	0x1	COMPTEN. HPCOM output protection enable 0: protection disable 1: protection enable
1:0	R/W	0x0	PTDBS. HPCOM protect de-bounce time setting 00: 2-3ms 01: 4-6ms 10: 8-12ms 11: 16-24ms

22.4.10. DAC TX Counter Register(Default: 0x00000000)

Offset: 0x30			Register Name: AC_DAC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	TX_CNT. TX Sample Counter The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

22.4.11. ADC RX Counter Register(Default: 0x00000000)

Offset: 0x34			Register Name: AC_ADC_CNT
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	RX_CNT. RX Sample Counter The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial valve at any time. After been updated by the initial value, the counter register should count on base of this initial value. Notes: It is used for Audio/ Video Synchronization

Chapter 23 LRADC

23.1. Overview

LRADC is 6-bit resolution.

It features:

- Support APB 32-bit bus width
- Support interrupt
- Support hold key and general key
- Support single key and continue key mode
- 6-bit resolution
- Voltage input range between 0 to 2V
- Sample rate up to 250Hz

23.2. Principle of operation

23.2.1. Block Diagram

The LRADC converted data can by accessed by interrupt and polling method. If software can't access the last converted data instantly, the new converted data would update the old one at new sampling data.

23.2.2. Hold Key and General Key Function Introduction

When ADC_IN Signal change from ADC_REF to 2/3 ADC_REF (Level A), the comparator24 send first interrupt to control logic; When ADC_IN Signal changes from 2/3 ADC_REF to certain level (Program can set), the comparator25 give second interrupt. If the control Logic get the first interrupt, In a certain time range (program can set), doesn't get second interrupt, it will send hold key interrupt to the host; If the control Logic get the first interrupt, In a certain time range (program can set), get second interrupt, it will send key down interrupt to the host; If the control logic only get the second interrupt, doesn't get the first interrupt, it will send already hold interrupt to the host.

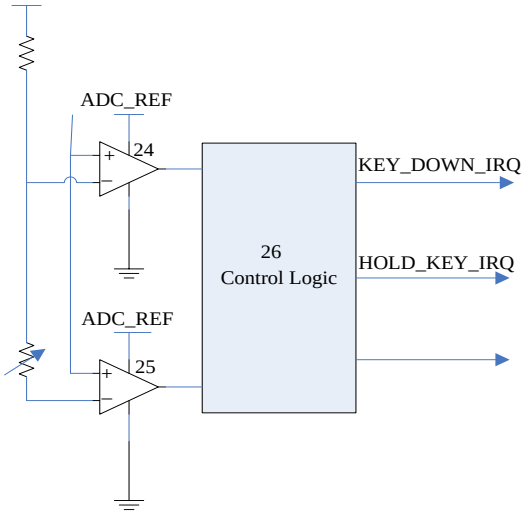


Figure 23-1. LRADC Control Logic Diagram

23.3. LRADC Register List

Module Name	Base Address
LRADC	0x01C22800

Register Name	Offset	Description
LRADC_CTRL	0x00	LRADC Control Register
LRADC_INTC	0x04	LRADC Interrupt Control Register
LRADC_INTS	0x08	LRADC Interrupt Status Register
LRADC_DATA0	0x0c	LRADC Data Register 0
LRADC_DATA1	0x10	LRADC Data Register 1

23.4. LRADC Register Description

23.4.1. LRADC Control Register(Default: 0x01000168)

Offset: 0x00			Register Name: LRADC_CTRL
Bit	Read/Write	Default/Hex	Description
31: 24	R/W	0x1	FIRST_CONCERT_DLY. ADC First Convert Delay setting, ADC conversion is delayed by n samples
23:22	R/W	0x0	ADC_CHAN_SELECT. ADC channel select 00: ADC0 channel 01: ADC1 channel 1x: ADC0&ADC1 channel
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode time select, one of 8*(N+1) sample as a valuable sample data
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select: 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples
7	/	/	/
6	R/W	0x1	LRADC_HOLD_EN. LRADC Sample hold Enable 0: Disable 1: Enable
5: 4	R/W	0x2	LEVELB_VOL. Level B Corresponding Data Value setting (the real voltage value) 00: 0x3C (~1.9v) 01: 0x39 (~1.8v) 10: 0x36 (~1.7v) 11: 0x33 (~1.6v)
3: 2	R/W	0x2	LRADC_SAMPLE_RATE. LRADC Sample Rate 00: 250 Hz 01: 125 Hz 10: 62.5 Hz 11: 32.25 Hz

1	/	/	/
0	R/W	0x0	LRADC_EN. LRADC enable 0: Disable 1: Enable

23.4.2. LRADC Interrupt Control Register(Default: 0x00000000)

Offset: 0x04			Register Name: LRADC_INTC
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
12	R/W	0x0	ADC1_KEYUP_IRQ_EN. ADC 1 Key Up IRQ Enable 0: Disable 1: Enable
11	R/W	0x0	ADC1_ALRDY_HOLD_IRQ_EN. ADC 1 Already Hold Key IRQ Enable 0: Disable 1: Enable
10	R/W	0x0	ADC 1 Hold Key IRQ Enable 0: Disable 1: Enable
9	R/W	0x0	ADC1_KEYIRQ_EN. ADC 1 Key IRQ Enable 0: Disable 1: Enable
8	R/W	0x0	ADC1_DATA_IRQ_EN. ADC 1 DATA IRQ Enable 0: Disable 1: Enable
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN. ADC 0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN. ADC 0 Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN. ADC 0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC 0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN. ADC 0 Data IRQ Enable 0: Disable 1: Enable

23.4.3. LRADC Interrupt Status Register(Default: 0x00000000)

Offset: 0x08	Register Name: LRADC_INT

Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
12	R/W	0x0	ADC1_KEYUP_PENDING. ADC 1 Key up pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable
11	R/W	0x0	ADC1_ALRDY_HOLD_PENDING. ADC 1 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled
10	R/W	0x0	ADC1_HOLDKEY_PENDING. ADC 1 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
9	R/W	0x0	ADC1_KEYDOWN_IRQ_PENDING. ADC 1 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
8	R/W	0x0	ADC1_DATA_IRQ_PENDING. ADC 1 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled
7:5	/	/	/
4	R/W	0x0	ADC0_KEYUP_PENDING. ADC 0 Key up pending Bit When general key pull up, it the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
3	R/W	0x0	ADC0_ALRDY_HOLD_PENDING. ADC 0 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
2	R/W	0x0	ADC0_HOLDKEY_PENDING.

			ADC 0 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
1	R/W	0x0	ADC0_KEYDOWN_PENDING. ADC 0 Key Down IRQ Pending Bit When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.
0	R/W	0x0	ADC0_DATA_PENDING. ADC 0 Data IRQ Pending Bit 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enabled.

23.4.4. LRADC Data 0 Register(Default: 0x00000000)

Offset: 0x0c			Register Name: LRADC_DATA
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x0	LRADC0_DATA. LRADC 0 Data

23.4.5. LRADC Data 1 Register(Default: 0x00000000)

Offset: 0x10			Register Name: LRADC_DATA
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R	0x0	LRADC1_DATA. LRADC 1 Data

Chapter 24 Touch Panel

24.1. Overview

The controller is a 4-wire resistive touch screen controller, includes 12-bit resolution A/D converter. Especially, it provides the ability of dual touch detection. The controller through the implementation of the two A/D conversion has been identified by the location of the screen of single touch, in addition to measurable increase in pressure on the touch screen.

It features:

- 12-bit SAR type A/D converter
- 4-wire I/F
- Dual touch detect
- Touch-pressure measurement (Support program set threshold)
- Sampling frequency: 2MHz (max)
- Single-ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change

24.2. Typical Application Circuit

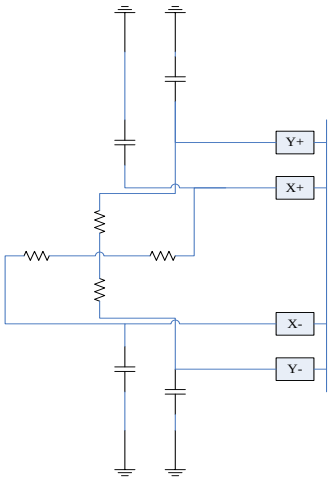


Figure 24-1. TP Typical Application Circuit

24.3. Clock Tree and ADC Time

24.3.1. Clock Tree

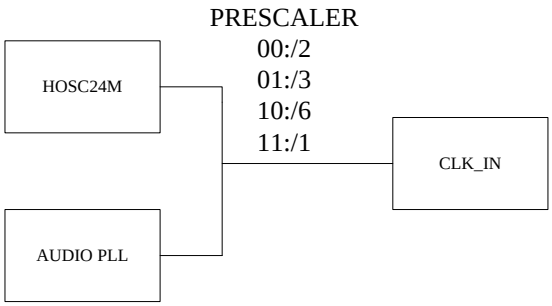


Figure 24-2. TP Clock Tree

24.3.2. A/D Convertion Time

When the clock source is 24MHz and the prescaler value is 6, total 12-bit conversion time is:

CLK_IN = 24MHz/6 = 4MHz

Conversion Time = 1/(4MHz/13Cycles) = 3.25us

Touch acquire time divider is 16

TACQ = 16*16*1/4us = 64us

FS_TIME Based on TACQ and Touch Mode:

When touch is in dual and pressure measurement mode, TACQ is , the FS_TIME must be no less than 6*(TACQ + Conversion Time)

FS_TIME >= M*(TACQ + Conversion Time)

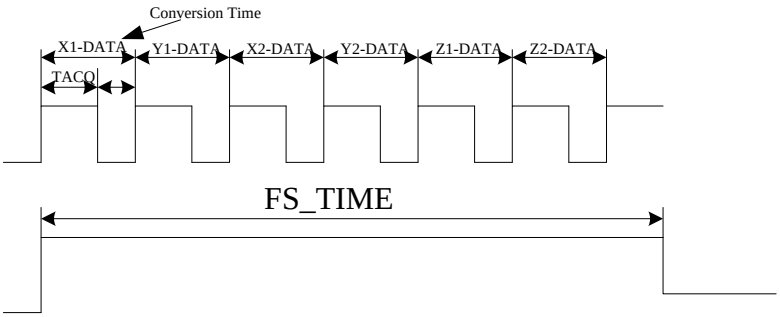


Figure 24-3.Dual Touch And Pressure Measurement

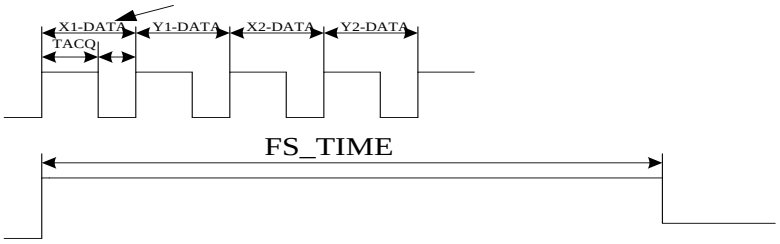


Figure24-4. Dual Touch No Pressure Measurement

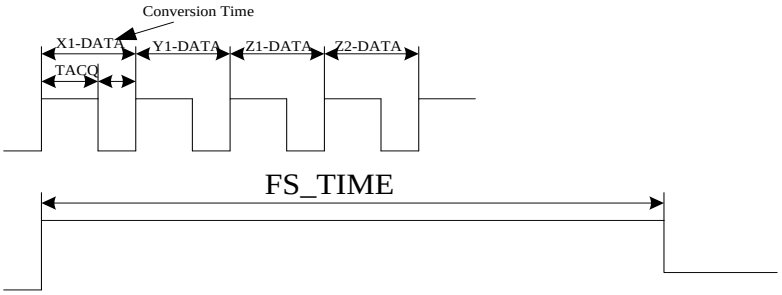


Figure24-5. Single Touch and Pressure Measurement

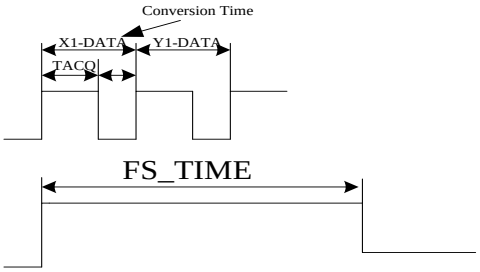


Figure24-6. Single Touch No Pressure Measurement Mode

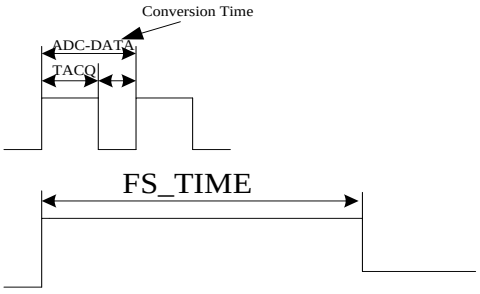


Figure24-7. General ADC Mode

24.4. Principle of Operation

24.4.1. The Basic Principle

The controller is a typical type of successive approximation ADC (SAR ADC), contains a sample/hold, analog-to-digital conversion, serial data output functions. The analog inputs (X+, X-, Y+, Y-) via control register enter the ADC, ADC can be configured as single-ended or differential mode. Selecting Aux ADC or temperature should be configured for single-ended mode; as a touch screen application, it should be configured as a differential mode, which can effectively eliminate the parasitic resistance of the driver switch and external interference caused by measurement error and impact conversion accuracy

24.4.2. Single-ended Mode

When the TP Control Register 0 Bit12(ADC Mode Select) is high, the controller is in the measurement mode of AUX, Temp, the internal ADC reference voltage source is the single-ended mode, using the AVCC reference source as the ADC reference voltage, application of the principle of single-ended mode shown in Figure 24-8.

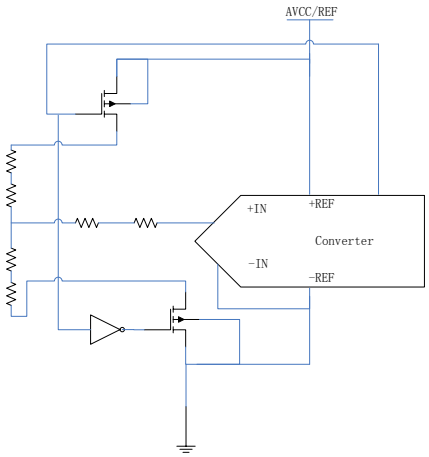


Figure 24-8. Simplified Diagram of Single-Ended Reference

24.4.3. Differential Mode

When the TP Control Register 0 Bit12(ADC Mode Select) is low, the controller is in the measurement mode of X,Y,Z, the internal ADC reference voltage source is the differential mode, shown in Figure 24-9. The advantage of differential mode: +REF and –REF input directly to the Y+, Y-, which can eliminate measurement error because of the switch on-resistance. The disadvantage is that: both the ample or conversion process, the driver needs to be on, relative to single-ended mode, the power consumption increases.

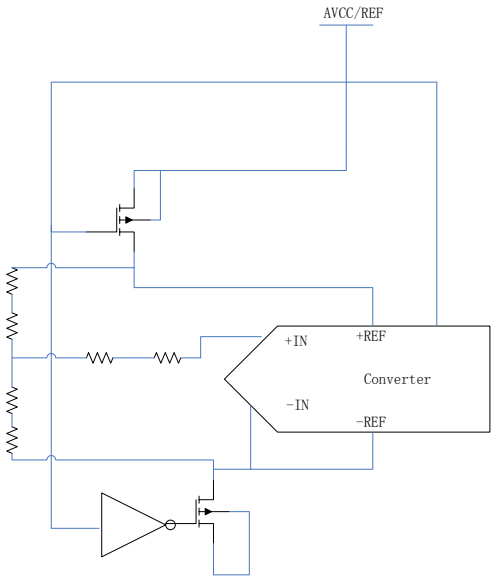


Figure24-9. Simplified Diagram of Differential Reference

24.4.4. Single Touch Detection

The principle of operation is illustrated below, For an X co-ordinate measurement, the X+ pin is internally switched to AVCC and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the Y+, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. Y co-ordinate measurements are similar to X co-ordinate measurements, with the X and Y plates interchanged. In Single Touch mode, only need to test X+, Y+ signal.

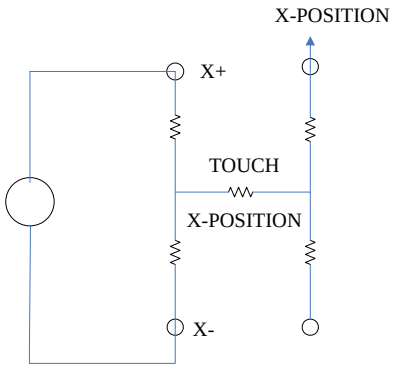


Figure24-10. Single Touch X-Position Measurement

24.4.5. Dual Touch Detection

The principle of operation is illustrated below, For an X co-ordinate measurement, the X+ pin is internally switched to AVCC and X- to GND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the Y+ and Y-, which carry no current (hence there is no voltage drop in R_Y+ or R_Y-). Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement. the controller will need to test X+,X-,Y+,Y- , and record $\Delta X=|X+ - X-|$, $\Delta Y= | Y+ - Y-|$, if ΔX or ΔY great than threshold, as a dual touch, thus as a single touch.

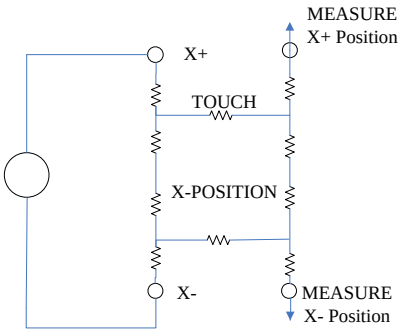


Figure24-11. Dual Touch X-Position Measurements

24.4.6. Touch-Pressure Measurement

The pressure applied to the touch screen by a pen or finger to filter unavailable can also be also be measurement with the controller using some simple calculations. The contact resistance between the X and Y plates is measured, providing a good indication of the size of the depressed area and, therefore, the applied pressure. The area of the spot that is touched is proportional to the size of the object touching it. The size of this resistance (R_{touch}) can be calculated using two different methods.

First Method:

The first method requires the user to know the total resistance of the X-plate tablet (RX). Three touch screen conversions are required: measurement of the X position, XPOSITION (Y+ input); measurement of the X+ input with the excitation voltage applied to Y+ and X− (Z1 measurement); and measurement of the Y− input with the excitation voltage applied to Y+ and X− (Z2 measurement). These three measurements are illustrated in Figure 24-12. The controller have two special ADC channel settings that configure the X and Y switches for the Z1 and Z2 measurements and store the results in the Z1 and Z2 result registers. The touch resistance (RTOUCH) can then be calculated using the following equation:

$$R_{TOUCH} = (R_{XPLATE}) \times (X_{POSITION} /4096) \times [(Z2/Z1) - 1] \quad (1)$$

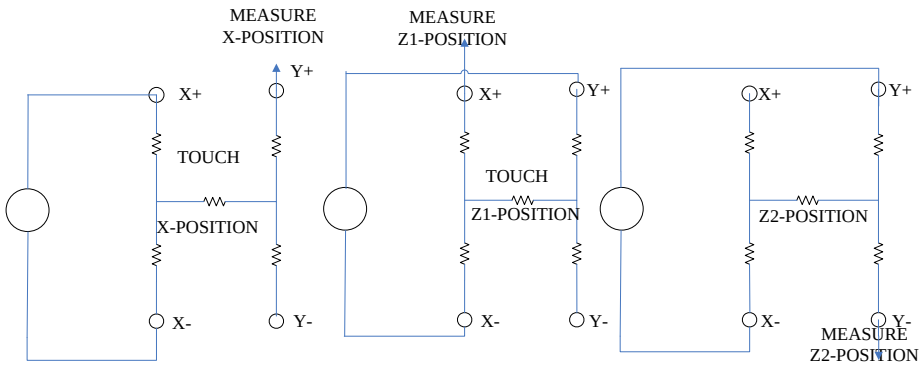


Figure24-12. Pressure Measurement Block Diagram

Second Method:

The second method requires the user to know the resistance of the X-plate and Y-plate tablets. Three touch screen conversions are required: a measurement of the X position ($X_{POSITION}$), the Y position ($Y_{POSITION}$), and the Z1 position. The following equation also calculates the touch resistance (R_{TOUCH}):

$$R_{TOUCH} = R_{XPLATE} \times (X_{POSITION}/4096) \times [(4096/Z1) - 1] - R_{YPLATE} \times [1 - (Y_{POSITION}/4096)] \quad (2)$$

24.4.7. Pen Down Detection, with Programmable Sensitivity

Pen down detection is used as an interrupt to the host. R_{IRQ} is an internal pull-up resistor with a programmable value of 6~96 kΩ (default 48kΩ). The PENIRQ output is pulled high by an internal pull-up. the Y– driver is on and connected to GND, and the PENIRQ output is connected to the X+ input. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the PENIRQ output goes low because of the current path through the panel to GND, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-position, the X+ input is disconnected from the PENIRQ pull-down transistor to eliminate any pull-up resistor leakage current from flowing through the touch screen, thus causing no errors.

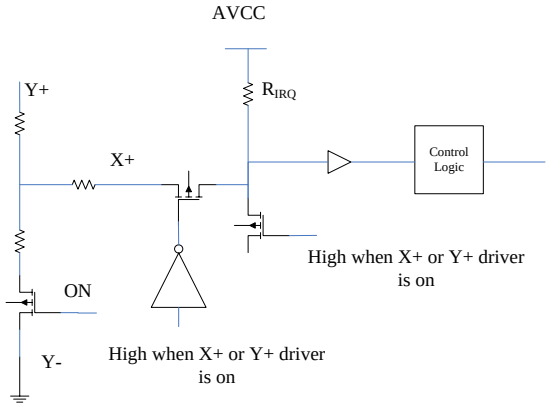


Figure 24-13. Example of Pen touch Interrupt via Pen Down IRQ

24.4.8. Median and Averaging Filter

As explained in the Touch Screen Principles section, touch screens are composed of two resistive layers, normally placed over an LCD screen. Because these layers are in close proximity to the LCD screen, noise can be coupled from the screen onto these resistive layers, causing errors in the touch screen positional measurements. The controller contain a filtering block to process the data and discard the spurious noise before sending the information to the host. The purpose of this block is not only the suppression of noise; the on-chip filtering also greatly reduces the host processing loading. The processing function consists of two filters that are applied to the converted results: the median filter and the averaging filter. The median filter suppresses the isolated out-of-range noise and sets the number of measurements to be taken. These measurements are arranged in a temporary array, where the first value is the smallest measurement and the last value is the largest measurement. Bit1 and Bit0 in Control Register 3(MED1,MED0)set the window of the median filter and, therefore, the number of measurements taken.

Table24-1. Median Filter Size

MED1	MED0	Median Filter Size
0	0	4
0	1	5
1	0	8
1	1	16

The averaging filter size determines the number of values to average. Bit5 and Bit4 in Control Register 3 (AVG1, AVG0) set the average to 2, 3, 4, or 8 samples. Only the final averaged result is written into the result FIFO register.

Table24-2. Averaging Filter Size

AVG1	AVG0	Averaging Filter Size
0	0	2
0	1	3
1	0	4
1	1	8

When Bit4 of Control Register 3 is set 0, and Median Averaging Filter mode is disabled, only one measurement is transferred to the register map. The number specified with the MED1 and MED0 settings must be greater than or equal to the number specified with the AVG1 and AVG0 settings. If both settings specify the same number, the median filter is switched off.

Table24-3. Median Averaging Filters (MAVF)

Setting	Function
M = A	Median filter is disabled; output is the average of A converted results
M > A	Output is the average of the middle A values from the array of M measurements
M < A	Not possible because the median filter size is always larger than the averaging window size

Example In this example, MED1, MED0 = 11 and AVG1, AVG0 = 10; the median filter has a window size of 16. This means that 16 measurements are taken and arranged in descending order in a temporary array. The averaging window size in this example is 8. The output is the average of the middle eight values of the 16 measurements taken with the median filter.

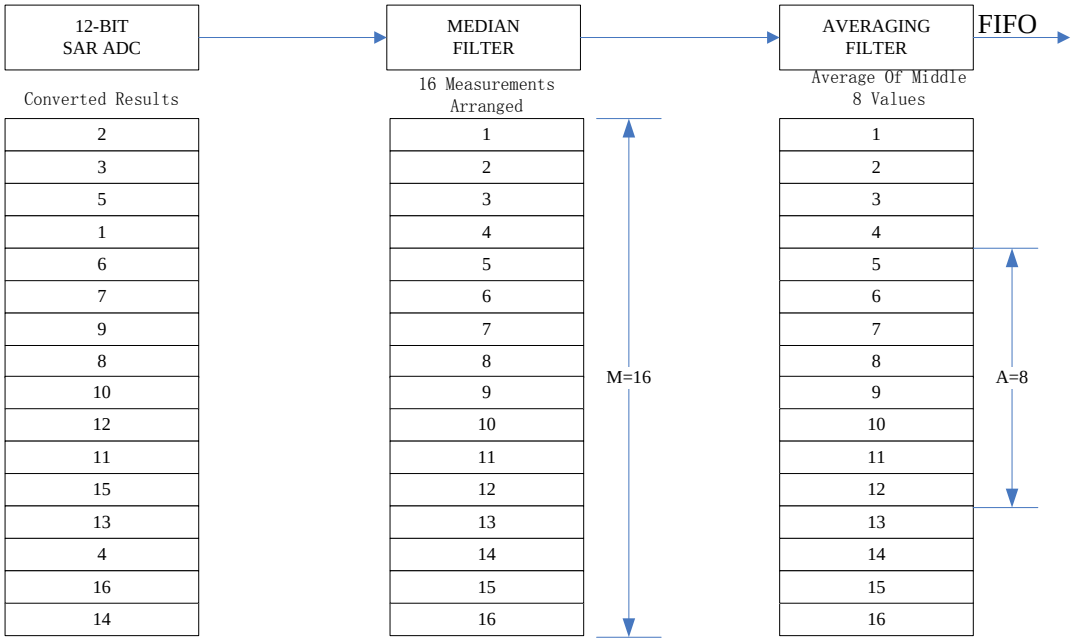


Figure 24-14. Median and Averaging Filter Example

24.5. TP Register List

Module Name	Base Address
TP	0x01C25000

Register Name	Offset	Description
TP_CTRL0	0x00	TP Control Register0
TP_CTRL1	0x04	TP Control Register1
TP_CTRL2	0x08	TP Pressure Measurement and touch sensitive Control Register
TP_CTRL3	0x0c	Median filter Controller Register
TP_INT_FIFOC	0x10	TP Interrupt FIFO Control Register
TP_INT_FIFOS	0x14	TP Interrupt FIFO Status Register
TP_CDAT	0x1C	TP Common Data Register
TP_DATA	0x24	TP Data Register
TP_IO_CONFIG	0x28	TP PORT IO Configure Register
TP_PORT_DATA	0x2C	TP Port Data Register

24.6. TP Register Description

24.6.1. TP Control Register 0(Default: 0x0F800000)

Offset: 0x00			Register Name: TP_CTRL
Bit	Read/Write	Default /Hex	Description
31:24	R/W	0xF	ADC_FIRST_DLY. ADC First Convert Delay setting Based on ADC First Convert Delay Mode select
23	R/W	0x1	ADC_FIRST_DLY_MODE. ADC First Convert Delay Mode Select 0: CLK_IN/16 1: CLK_IN/16*256
22	R/W	0x0	ADC_CLK_SELECT. ADC Clock Source Select: 0: HOSC(24MHZ) 1: Audio PLL
21:20	R/W	0x0	ADC_CLK_DIVIDER. ADC Clock Divider(CLK_IN) 00: CLK/2 01: CLK/3 10: CLK/6 11: CLK/1 In TP mode, these two bits must set 1x
19:16	R/W	0x0	FS_DIV. ADC Sample Frequency Divider 0000: CLK_IN/2(20-n) 0001: CLK_IN/2(20-n) 0010: CLK_IN/2(20-n) .... 1111: CLK_IN/32
15:0	R/W	0x0	T_ACQ. Touch panel ADC acquire time CLK_IN/(16*N)

24.6.2. TP control Register 1(Default: 0x00000008)

Offset: 0x04			Register Name: TP_CTRL1
Bit	Read/Write	Default /Hex	Description
31:20	/	/	/
19:12	R/W	0x0	STYLUS_UP_DEBOUNCE. Stylus Up De-bounce Time setting 0x00: 0 .... 0xff: 2N*(CLK_IN/16*256)
11:10	/	/	/
9	R/W	0x0	STYLUS_UP_DEBOUCE_EN. Stylus Up De-bounce Function Select 0: Disable 1: Enable
8:7	/	/	/
6	R/W	0x0	TOUCH_PAN_CALI_EN. Touch Panel Calibration 1: start Calibration, it is clear to 0 after calibration
5	R/W	0x0	TP_DUAL_EN. Touch Panel Double Point Enable 0: Disable 1: Enable
4	R/W	0x0	TP_MODE_EN. Tp Mode Function Enable 0: Disable 1: Enable
3	R/W	0x1	TP_ADC_SELECT. Touch Panel and ADC Select 0: TP 1: ADC
2:0	R/W	0x0	ADC_CHAN_SELECT. Analog input channel Select In Normal mode: 000: X1 channel 001: X2 Channel 010: Y1 Channel 011: Y2 Channel 1xx : 4-channel robin-round FIFO Access Mode,based on this setting. Selecting one channel, FIFO will access that channel data; Selecting four channels FIFO will access each channel data in successive turn, first is X1 data.

24.6.3. TP Control Register 2(Default: 0x80000FFF)

Offset: 0x08			Register Name: TP_CNT2
Bit	Read/Write	Default/Hex	Description
31:28	R/W	0x8	TP_SENSITIVE_ADJUST. Internal Pull-up Resistor Control 0000 least sensitive 0011 …… 1111 most sensitive Note: Used to adjust sensitivity of pen down detection

27:26	R/W	0x0	TP_MODE_SELECT. TP Mode Select 00: FIFO store X,Y data with Z-filter 01: FIFO store X,Y, Δ X, Δ Y data with Z-filter 10: FIFO store X,Y, X2,Y2 data with Z-filter 11: Debug Mode, FIFO store X1,Y1, X2,Y2,Z1,Z2 data
25	/	/	/
24	R/W	0x0	PRE_MEA_EN. TP Pressure Measurement Enable Control 0: Disable 1: Enable
23:0	R/W	0xFFF	PRE_MEA_THRE_CNT. TP Pressure Measurement threshold Control Notes: 0x000000: least sensitive 0xFFFFFF: most sensitive Note: used to adjust sensitivity of touch

24.6.4. Median Filter Control Register(Default: 0x00000001)

Offset: 0x0c			Register Name: TP_CTRL3
Bit	Read/Write	Default/Hex	Description
31:3	/	/	/
2	R/W	0x0	FILTER_EN. Filter Enable 0: Disable 1: Enable
1:0	R/W	0x1	FILTER_TYPE. Filter Type 00: 4/2 01: 5/3 10: 8/4 11: 16/8

24.6.5. TP Interrupt& FIFO Control Register(Default: 0x00000F00)

Offset: 0x10			Register Name: TP_INT
Bit	Read/Write	Default/Hex	Description
31:19	/	/	
18	R/W	0x0	/
17	R/W	0x0	TP_OVERRUN_IRQ_EN. TP FIFO Over Run IRQ Enable 0: Disable 1: Enable
16	R/W	0x0	TP_DATA_IRQ_EN. TP FIFO Data Available IRQ Enable 0: Disable 1: Enable
15:14	/	/	/
13	R/W	0x0	TP_DATA_XY_CHANGE. TP FIFO X,Y Data interchange Function Select 0: Disable 1: Enable
12:8	R/W	0xF	TP_FIFO_TRIG_LEVEL. TP FIFO Data Available Trigger Level

			Interrupt and DMA request trigger level for TP or Auxiliary ADC Trigger Level = TXTL + 1
7	R/W	0x0	TP_DATA_DRQ_EN. TP FIFO Data Available DRQ Enable 0: Disable 1: Enable
6:5	/	/	/
4	R/W	0x0	TP_FIFO_FLUSH. TP FIFO Flush Write '1' to flush TX FIFO, self clear to '0'
3:2	/	/	/
1	R/W	0x0	TP_UP_IRQ_EN. Touch Panel Last Touch (Stylus Up) IRQ Enable 0: Disable 1: Enable
0	R/W	0x0	TP_DOWN_IRQ_EN. Touch Panel First Touch (Stylus Down) IRQ Enable 0: Disable 1: Enable

24.6.6. TP Interrupt& FIFO Status Register(Default: 0x00000000)

Offset: 0x14			Register Name: TP_FIFOCS
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18	R/W	0x0	/
17	R/W	0x0	FIFO_OVERRUN_PENDING. TP FIFO Over Run IRQ pending 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
16	R/W	0x0	FIFO_DATA_PENDING. TP FIFO Data Available pending Bit 0: NO Pending IRQ 1: FIFO Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails
15:13	/	/	/
12:8	R	0x0	RXA_CNT. TP FIFO available Sample Word Counter
7:3	/	/	/
2	R	0x0	TP_IDLE_FLG. Touch Panel Idle Flag 0: idle 1: not idle
1	R/W	0x0	TP_UP_PENDING. Touch Panel Last Touch (Stylus Up) IRQ Pending bit 0: No IRQ 1: IRQ Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.
0	R/W	0x0	TP_DOWN_PENDING. Touch Panel First Touch (Stylus Down) IRQ Pending bit 0: No IRQ 1: IRQ Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.

24.6.7. Common Data Register(Default: 0x00000000)

Offset: 0x1c			Register Name: TP_CDAT
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0x0	TP_CDAT. TP Common Data

24.6.8. TP Data Register(Default: 0x00000000)

Offset: 0x24			Register Name: TP_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R	0x0	TP_DATA Touch Panel X,Y data or Auxiliary analog input data

24.6.9. TP Port IO Configure Register(Default: 0x00002222)

Offset: 0x28			Register Name: TP_IO_CONFIG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:12	R/W	0x2	TY_N_SELECT TY_N Port Function Select: 000:Input 001:Output 010: TP_YN 011:/ 100: / 101:/ 110: / 111:/
11	/	/	/
10:8	R/W	0x2	TY_P_SELECT TY_P Port Function Select: 000:Input 001:Output 010: TP_YP 011:/ 100: / 101:/ 110: / 111:/
7	/	/	/
6:4	R/W	0x2	TX_N_SELECT TX_P Port Function Select: 000:Input 001:Output 010: TP_XP 011:/ 100: / 101:/ 110: / 111:/
3	/	/	/
2:0	R/W	0x2	TX_P_SELECT TX_P Port Function Select: 000:Input 001:Output 010: TP_XP 011:/ 100: / 101:/ 110: / 111:/

24.6.10. TP Port Data Register(Default: 0x00000000)

Offset: 0x2c			Register Name: TP_PORT_DATA
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/

3:0	R/W	0x0	TP_PORT_DATA TP Port Data Value,TP_XP,TP_XN,TP_YP,TP_YN

Chapter 25 CSI

25.1. Overview

The CMOS Sensor Interface (CSI) features:

- 8-bit input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Support Received data double buffer
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or MB Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software
- Luminance statistical value

25.2. CSI Block Diagram

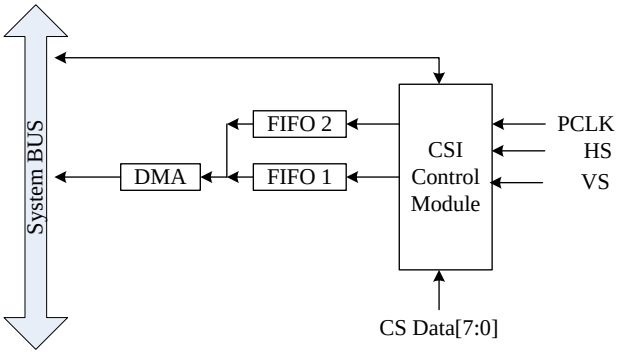


Figure 25-1. CSI Block Diagram

25.3. CSI Register List

Module Name	Base Address
CSI	0x01C00900

Register Name	Offset	Description
CSI_EN_REG	0x0000	CSI Enable Register
CSI_CFG_REG	0x0004	CSI Configuration Register
CSI_CPT_CTRL_REG	0x0008	CSI Capture Control Register
CSI_FIFO0_BUF_A_ADDR_REG	0x0010	CSI FIFO0 Buffer A Register
CSI_FIFO0_ BUF_B_ADDR_REG	0x0014	CSI FIFO0 Buffer B Register
CSI_FIFO1_ BUF_A_ADDR_REG	0x0018	CSI FIFO1 Buffer A Register
CSI_FIFO1_ BUF_B_ADDR_REG	0x001C	CSI FIFO1 Buffer B Register
CSI_BUF_CTRL_REG	0x0028	CSI Buffer Contrl Register
CSI_STA_REG	0x002C	CSI Status Register
CSI_INT_EN_REG	0x0030	CSI Interrupt Enable Register
CSI_INT_STA_REG	0x0034	CSI Interrupt Status Register
CSI_WIN_CTRL_W_REG	0x0040	CSI Window Width Control Register

CSI_WIN_CTRL_H_REG	0x0044	CSI Window Height Control Register
CSI_BUF_LEN_REG	0x0048	CSI Buffer Length Register

25.4. CSI Register Description

25.4.1. CSI Enable Register(Default: 0x00000000)

Offset: 0X0000			Name: CSI_EN_REG
Bit	Read/Write	Default/Hex	Description
31:01	/	/	Reserved
00	R/W	0	EN CSI Enable 0: Reset and disable 1: Enable

25.4.2. CSI Configuration Register(Default: 0x00000200)

Offset Address: 0X0004			Register Name: CSI_CFG_REG
Bit	Read/Write	Default/Hex	Description
31:23	/	/	Reserved
22:20	R/W	0	IN_FMT Input data format 000: RAW stream 010: CCIR656 011: YUV422 others: reserved
19:16	R/W	0	OUT_FMT Output data format When the input format is set RAW stream 0000: pass-through When the input format is set CCIR656 interface 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1111: interlaced interleaved YCbCr422. In this mode, capturing interlaced input and output the interlaced fields from individual ports. Field 1 data will be written to FIFO0 output buffer and field 2 data will be written to FIFO1 output buffer. 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 When the input format is set YUV422 0000: planar YUV 422 0001: planar YUV 420 0100: planar YUV 422 UV combined 0101: planar YUV 420 UV combined 1000: MB YUV 422 1001: MB YUV 420

15:12	/	/	Reserved
11:10	R/W	0	FIELD_SEL Field selection. Applies to CCIR656 interface only. 00: start capturing with field odd. 01: start capturing with field even. 10: start capturing with either field. 11: reserved
09:08	R/W	2	DATA_SEQ Input data sequence, only valid for YUV422 mode. 00: YUYV 01: YVYU 10: UYVY 11: VYUY
07:03	/	/	Reserved
02	R/W	0	VSYNC_POL Vref polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
01	R/W	0	HSYNC_POL Href polarity 0: negative 1: positive This register is not applied to CCIR656 interface.
00	R/W	0	PCLK_POL Data clock type 0: active in falling edge 1: active in rising edge

25.4.3. CSI Capture Control Register(Default: 0x00000000)

Offset Address: 0X0008			Register Name: CSI_CPT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:02	/	/	Reserved
01	R/W	0	VIDEO_CAP_CTRL Video capture control: Capture the video image data stream. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
00	W	0	STILL_CAP_CTRL Still capture control: Capture a single still image frame. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self cleared and always reads as a 0.

25.4.4. CSI FIFO0 Buffer A Register(Default: 0x00000000)

Offset Address: 0X0010			Register Name: CSI_FIFO0_BUF_A_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	FIFO0_BUF_A

			FIFO0 output buffer-A address

25.4.5. CSI FIFO0 Buffer B Register(Default: 0x00000000)

Offset Address: 0X0014			Register Name: CSI_FIFO0_BUF_B_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	FIFO0_BUF_B FIFO0 output buffer-B address

25.4.6. CSI FIFO1 Buffer A Register(Default: 0x00000000)

Offset Address: 0X0018			Register Name: CSI_FIFO1_BUF_A_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	FIFO1_BUF_A FIFO1 output buffer-A address

25.4.7. CSI FIFO1 Buffer B Register(Default: 0x00000000)

Offset Address: 0X001C			Register Name: CSI_FIFO1_BUF_B_ADDR_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	FIFO1_BUF_B FIFO1 output buffer-B address

25.4.8. CSI Buffer Control Register(Default: 0x00000000)

Offset Address: 0X0028			Register Name: CSI_BUF_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:02	/	/	Reserved
01	R	0	DBS output buffer selected status 0: Selected output buffer-A 1: Selected output buffer-B
00	R/W	0	DBE Double buffer mode enable 0: disable 1: enable If the double buffer mode is disabled, the buffer-A will be always selected by CSI module.

25.4.9. CSI Status Register(Default: 0x00000000)

Offset Address: 0X002C			Register Name: CSI_STA_REG
Bit	Read/Write	Default/Hex	Description
31:08	R	0	LUM_STAT_VALUE luminance statistical value When frame done interrupt flag come, value is ready and will last until next frame done. For raw data, value = (G>>1+R+G)>>8 For yuv422, value = Y>>8
07:02	/	/	Reserved
01	R	0	VIDEO_CAP_ON Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture.

			When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	STILL_CPT_ON Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It is self-cleared after the last pixel of the first frame is captured. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, and the other frame end means filed end.

25.4.10. CSI Interrupt Enable Register(Default: 0x00000000)

Offset Address: 0X0030			Register Name: CSI_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:08	/	/	Reserved
07	R/W	0	VSYNC_FLAG vsync flag The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq comes, change the buffer address could only affect next frame
06	R/W	0	HB_OF Hblank FIFO overflow The bit is set when 3 FIFOs still overflow after the hblank.
05	R/W	0	PRT_ERR Protection error Indicates a protection error has been detected. Applies only when the 656 protocol is selected.
04	/	/	Reserved
03	R/W	0	FIFO0_OF FIFO1 overflow The bit is set when the FIFO 1 overflows.
02	R/W	0	FIFO0 overflow The bit is set when the FIFO 0 overflows.
01	R/W	0	FRM_DONE Frame done Indicates the CSI finishes capturing an image frame. Applied to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.
00	R/W	0	CPT_DONE Capture done Indicates the CSI has completed capturing the image data. For still capture, the bit is set when one frame data has been written to buffer. For video capture, the bit is set when the last frame has been written to buffer after video capture is disabled. For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, and the other frame end means field end.

25.4.11. CSI Interrupt Status Register(Default: 0x00000000)

Offset Address: 0X0034			Register Name: CSI_INT_STA_REG
Bit	Read/Write	Default/Hex	Description
31:08	/	/	Reserved

07	R/W	0	VSYNC_FLAG vsync flag
06	R/W	0	HB_OF Hblank FIFO overflow
05	R/W	0	PRT_ERR Protection error
04	/	/	Reserved
03	R/W	0	FIFO1 OF FIFO1 overflow
02	R/W	0	FIFO0_OF FIFO0 overflow
01	R/W	0	FRM_DONE Frame done
00	R/W	0	CPT_DONE Capture done

25.4.12. CSI Window Width Control Register(Default: 0x05000000)

Offset Address: 0X0040			Register Name: CSI_WIN_CTRL_W_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	Reserved
28:16	R/W	500	ACTIVE_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	Reserved
12:00	R/W	0	ACTIVE_START Horizontal pixel clock start. Pixel data is valid from this clock.

25.4.13. CSI Window Height Control Register(Default: 0x01E00000)

Offset Address: 0X0044			Register Name: CSI_WIN_CTRL_H_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	Reserved
28:16	R/W	0x1E0	ACTIVE_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	Reserved
12:00	R/W	0	ACTIVE_START Vertical line start. data is valid from this line.

25.4.14. CSI Buffer Length Register(Default: 0x00000280)

Offset: 0X0048			Register Name: CSI_BUF_LEN_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	Reserved
12:00	R/W	0x280	BUFF_LEN Buffer Length Buffer length of a line. Unit is byte.

25.5. CCIR656 Format

25.5.1. Header Data Bit Definition

Data Bit	First Word(0xFF)	Second Word (0x00)	Third Word(0x00)	Fourth Word
CS D[7] (MSB)	1	0	0	1

CS D[6]	1	0	0	F
CS D[5]	1	0	0	V
CS D[4]	1	0	0	H
CS D[3]	1	0	0	P3
CS D[2]	1	0	0	P2
CS D[1]	1	0	0	P1
CS D[0]	1	0	0	P0

25.5.2. CCIR656 Header Decode

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

25.6. CSI Timing Diagram

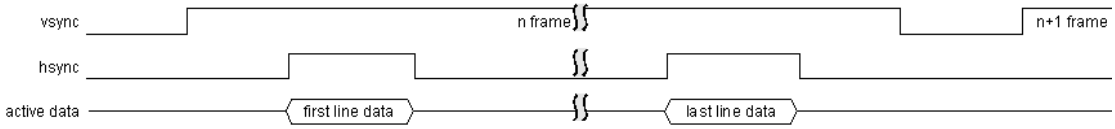


Figure 25-2. Vref= Positive; Href= Positive

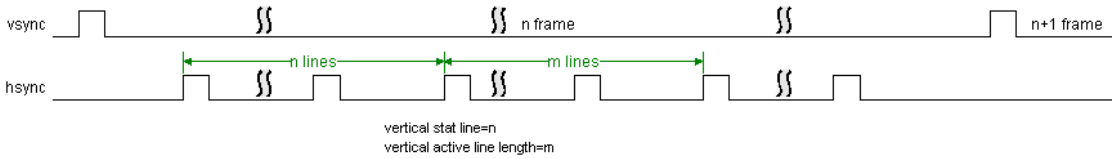


Figure 25-3. Vertical Size Setting

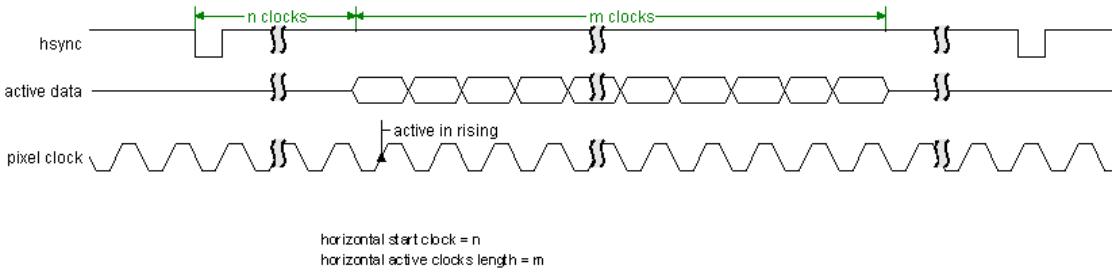


Figure 25-4. Horizontal Size Setting and Pixel Clock Timing (Href= positive)

Chapter 26 Display Engine Front End (DEFE)

26.1. Overview

The Display Engine Front End (DEFE) performs image capture/driver, video/graphic scale, format conversion and color space conversion. It is composed of DMA controller, input controller, scaler, color space conversion and output controller as show in figure 26-1.

The DEFE features:

- Output scan type: interlace/progressive
- Input format: YUV444/YUV422/YUV420/YUV411/RGB
- Direct display output format: RGB
- Write back output format: RGB/YUV444/YUV420/YUV422/YUV411
- 3 channel scaling pipelines for scaling up/down
- Programmable source image size from 8x4 to 8192x8192 resolution
- Programmable destination image size from 8x4 to 8192x8192 resolution
- 4 tap scale filter in horizontal and vertical direction
- 32 Programmable coefficients for each tap
- Color space conversion between YUV and RGB
- Support direct display and write back to memory

26.2. DEFE Block Diagram

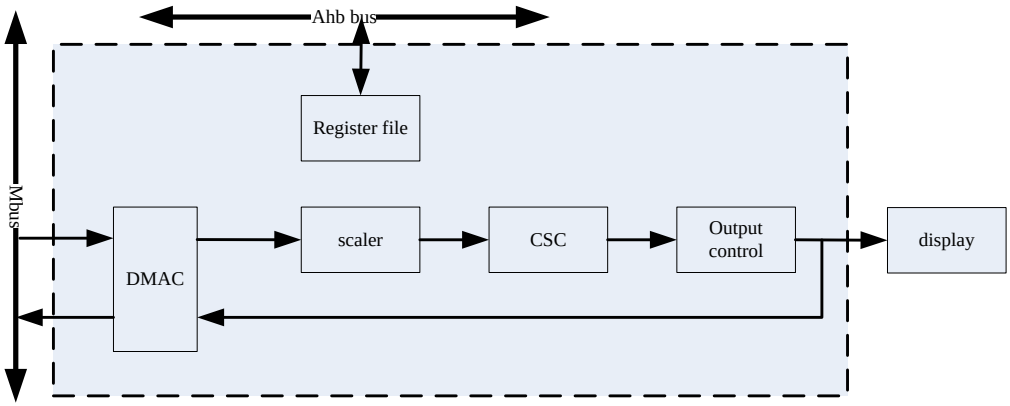


Figure 26-1. DEFE Block Diagram

26.3. DEFE Description

DEFE supports scaling or resizing of planar or interleaved video component data. Resizing or scaling the image means generating a new image that is larger or smaller than the original. The new image will have a larger or smaller number of pixels in the horizontal and/or vertical directions than the original image. Filtering provides image enhancement, and scaler provides high quality, 4-tap in horizontal and 4-tap in vertical filtering of YUV or RGB data.

26.3.1. Re-Sampling

Up-sampling is the process of inserting new data samples between original data samples to increase the sampling rate.

Down-sampling is the process of reducing the sampling rate by removing or throwing away original data samples.

In order to generate the output pixels, one first needs to relate the output grid to the input grid. Scaling is a pixel transformation in which an array of output pixels is generated from an array of input pixels. The value of each pixel on the output pixel grid is calculated from the values of its adjacent pixels on the input grid. To find these adjacent pixels, the output grid needs to be overlaid on the input grid and the starting pixels, X0Y0, of the two grids are alignd. To identify the adjacent input pixels for a given output pixel, the output pixel X (pixel number along the output line) and Y (pixel line number within window) should be divided by their corresponding scaling factors:

Xout = Xin / (horizontal scaling factor)

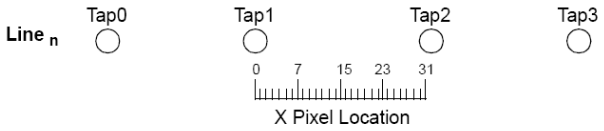
where: horizontal scaling factor = input length / output length

Yout = Yin / (vertical scaling factor)

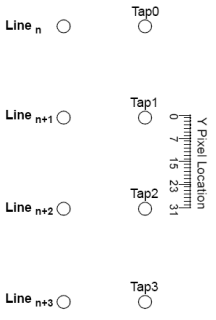
where: vertical scaling factor = input height / output height

Note that the resulting Xin and Yin values will be real numbers because the output pixels will usually fall between the input pixels. The fractional portion indicates the fractional distance to the next pixel. To calculate the output pixel value, you use the value for the nearest pixel to the left and above and combine it with the value of the other adjacent pixel(s). For example, horizontal interpolation uses the starting pixel to the left interpolated with the next pixel to the right, with the fractional value used to determine the weighting for the interpolation.

26.3.2. Quantizing



Horizontal quantizing



Vertical quantizing

The relation between each output pixel location the input pixel grid is:

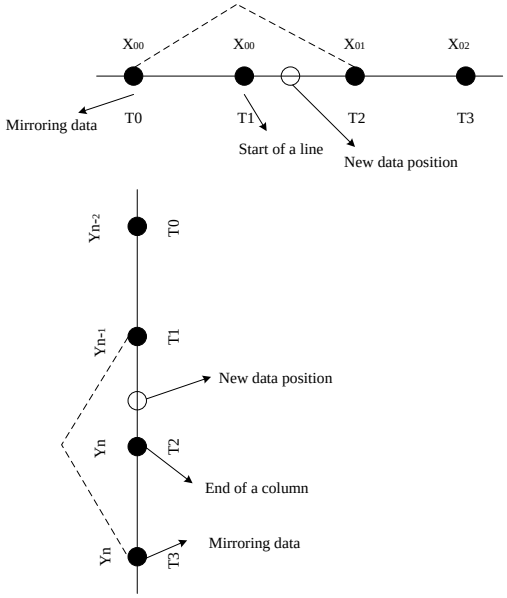
X location of output pixel = X0 of input line + output pixel number * X Scale Factor

Y location of output pixel = Y0 of input window + output line number * Y scale factor

The X and Y locations may not be integer values, which depend on the scale factor. The resulting X and Y pixel locations can be separated into an integer and a fractional part. The integer part of the X and Y location selects the pixel and line number closest to the output pixel, respectively. The fractional part gives the fractional distance of the output pixel to the next X and Y input pixel values. These fractional parts are the α and β values shown in scaling algorithm diagram.

To perform scaling, the X and Y locations of the output pixel relating to the input pixel grid must be generated. This includes both the integer part to locate the adjacent pixels and the fractional part to choose the filter coefficients which generate the output value from the adjacent pixels. This could be done by generating the output pixel X and Y numbers and dividing each by its associated scale factor.

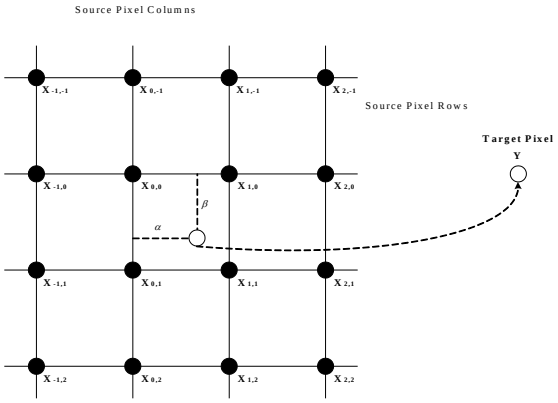
A line may start and/or end at the edge of the input image. In this case, you should use mirroring data shown in follow figure:



The scaler uses a 16-bit integer and a16-bit fractional value for the X and Y increment values. This allows a fractional value resolution of 1/64K. Only the most significant 5 bits of the fractional value are used by the filter coefficient RAMs.

26.3.3. Scaling/Filter

New pixels are generated by interpolation or filtering of the original pixels. Interpolation is the weighted average of the input pixels adjacent to the output pixel. Filtering extends interpolation to include input pixels beyond the input pair adjacent to the output pixel. The number of pixels used to generate the output defines the filter type. Interpolation is a 2-tap filter (A tap is equivalent to an original un-scaled pixel of data). A 4-tap filter would use the two pixels to the left and the two pixels to the right of the output pixel. Following is the scaling algorithm.



$$Y_{i,j} = \sum_{m=-1}^{2} \sum_{n=-1}^{2} X_{i+m,j+n} h_c(n-\beta) h_c(\alpha - m)$$

26.3.4. Input Data Channel

DEFE supports planar or interleaved video component data inputting via 3 input channels: channel0, channel1, and channel2. In planar mode, if the U, V data are not combined, channe0, 1, 2 refer to the Y, U, V data channel respectively, and if the U, V data are combined, the channel0 refers to the Y channel, and the channel 1 refers to the U, V combined channel, and the channel2 will be inactive. In interleaved mode, the channel0 refers to UYVY (or VYUY, YUYV, or YVYU depending on the configuration), the channel1 and channel2 will be inactive.

Note: Interleaved YUV data, only YUV422 and YUV444 format is valid.

26.3.5. CSC (Color Space Conversion) Description

YUV / RGB conversion is used to generate an RGB version data of the image for display or RGB / YUV version data for write back to memory.

Conversion algorithm formula:

R =

(R Y component coefficient * Y) +

(R U component coefficient * U) +

(R V component coefficient * V) +

R constant

G =

(G Y component coefficient * Y) +

(G U component coefficient * U) +

Y =

(Y R component coefficient * R) +

(Y G component coefficient * G) +

(Y B component coefficient * B) +

Y constant

U =

(U R component coefficient * R) +

(U G component coefficient * G) +

(G V component coefficient * V) +

G constant

B =

(B Y component coefficient * Y) +

(B U component coefficient * U) +

(B V component coefficient * V) +

B constant

(U B component coefficient * B) +

U constant

V =

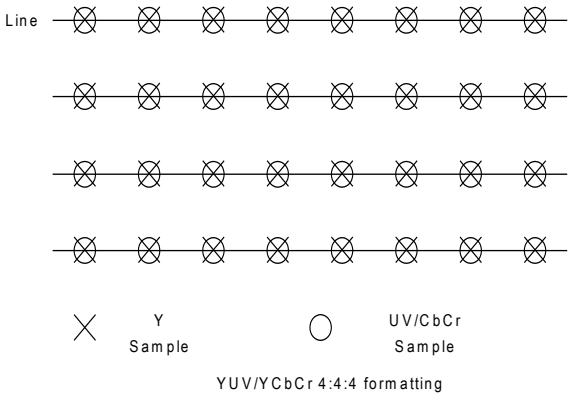
(V R component coefficient * R) +

(V G component coefficient * G) +

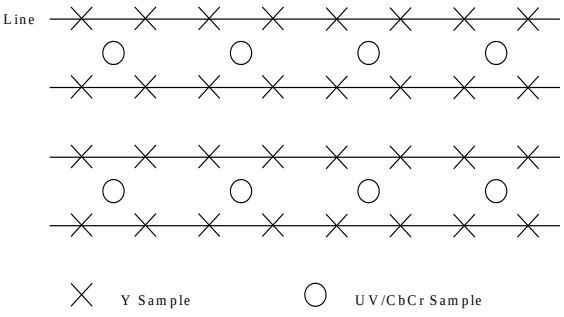
(V B component coefficient * B) +

V constant

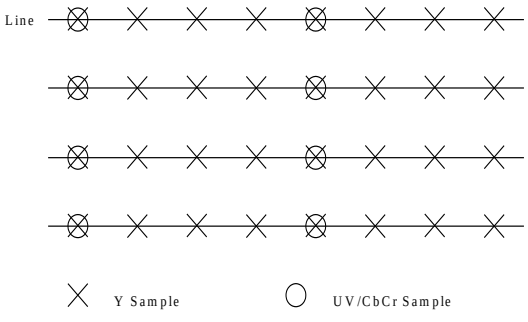
26.3.6. DEFE Source Input Formats



YUV/YCbCr 4:4:4 formatting



YCbCr 4:2:0 formatting



YCbCr 4:1:1 formatting

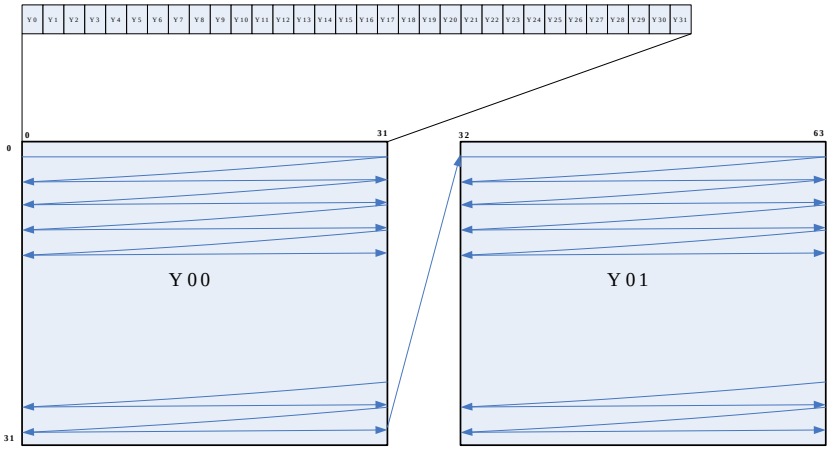
26.3.7. Image Data Memory Mapping

The DEFE not only supports the sequence non-tile-based format input data, but also the tile-based format input data. The tile-based format data is valid for YUV422, YUV420 and YUV411 when input data mode is planar or UV combined mode. In different conditions, the tile-based format memory mapping can refer to the following:

Tile-Based UV Combined Mode

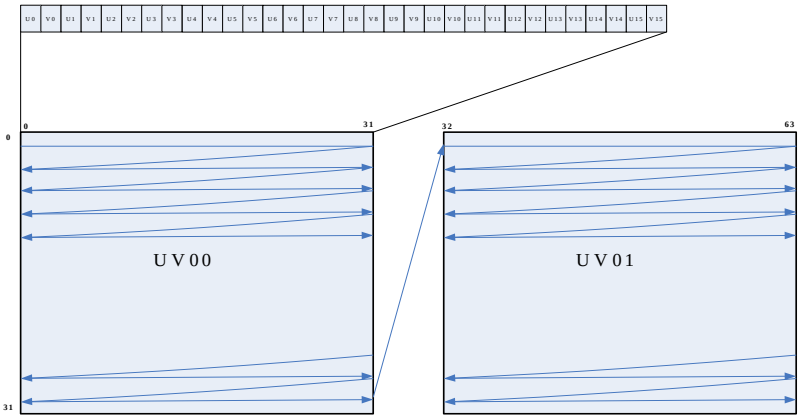
Y component mapping:

The mapping of Y component is the same in YUV422, YUV420 and YUV411.

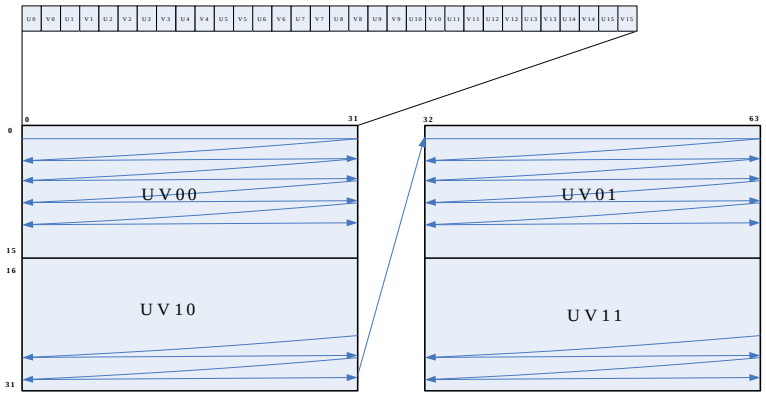


UV component mapping:

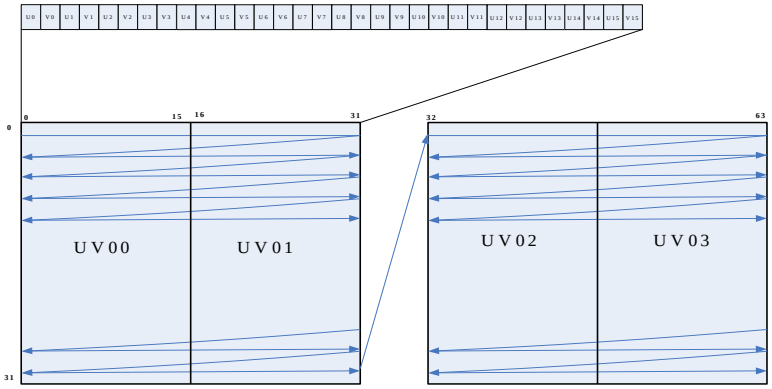
YUV422:



YUV420:



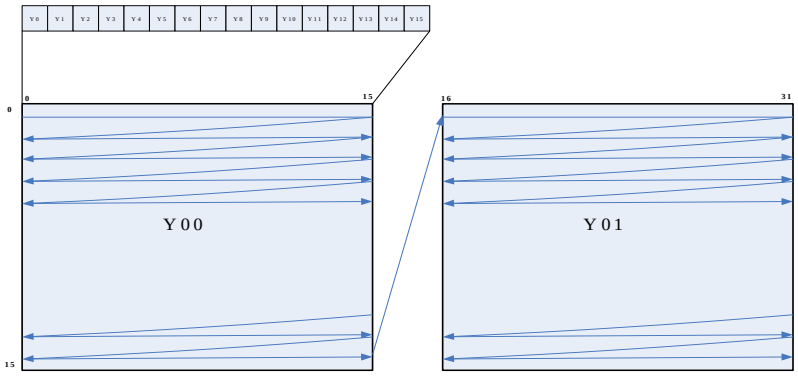
YUV411:



Tile-Based Planar Mode:

Y component:

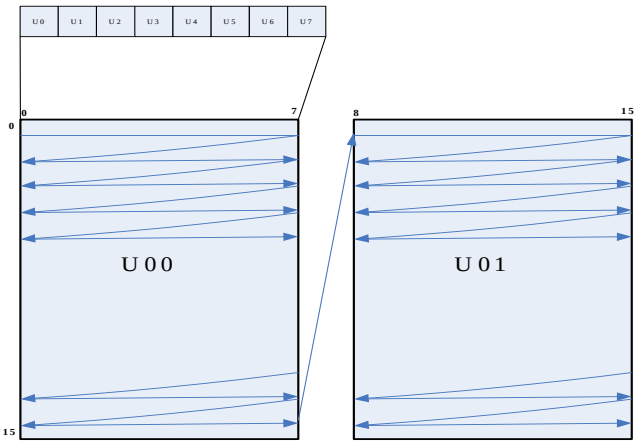
The mapping of Y component is the same in YUV422, YUV420 and YUV411.



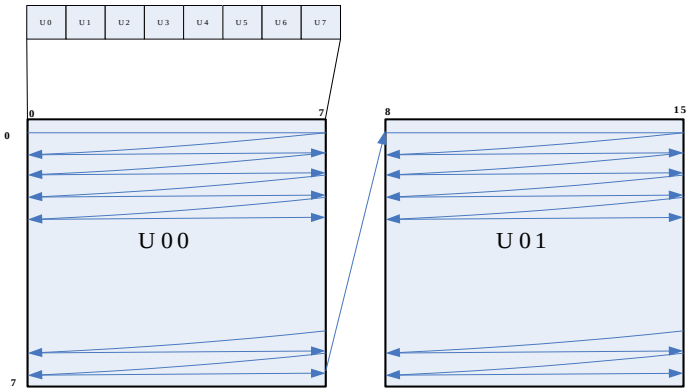
U or V component:

The mapping of V component is the same as U component.

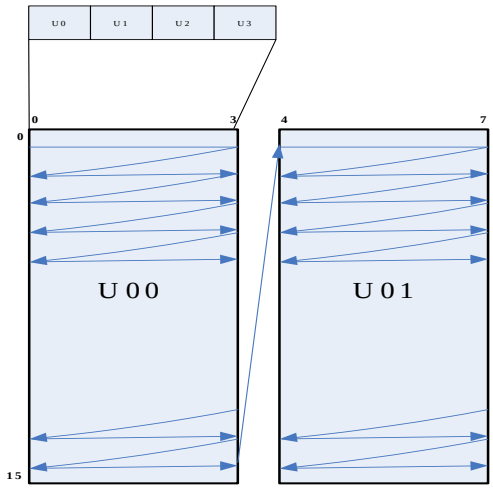
YUV422:



YUV420:



YUV411:



26.4. DEFE Register List

Module Name	Base Address
DEFE0	0x01E00000

Register Name	Offset	Description
DEFE_EN_REG	0x0000	DEFE Module Enable Register
DEFE_FRM_CTRL_REG	0x0004	DEFE Frame Process Control Register
DEFE_BYPASS_REG	0x0008	DEFE CSC By-Pass Register
DEFE_AGTH_SEL_REG	0x000C	DEFE Algorithm Selection Register
DEFE_LINT_CTRL_REG	0x0010	DEFE Line Interrupt Control Register
DEFE_BUF_ADDR0_REG	0x0020	DEFE Input Channel 0 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0024	DEFE Input Channel 1 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0028	DEFE Input Channel 2 Buffer Address Register
DEFE_FIELD_CTRL_REG	0x002C	DEFE Field Sequence Register
DEFE_TB_OFF0_REG	0x0030	DEFE Channel 0 Tile-Based Offset Register
DEFE_TB_OFF1_REG	0x0034	DEFE Channel 1 Tile-Based Offset Register
DEFE_TB_OFF2_REG	0x0038	DEFE Channel 2 Tile-Based Offset Register
DEFE_LINESTRD0_REG	0x0040	DEFE Channel 0 Line Stride Register
DEFE_LINESTRD1_REG	0x0044	DEFE Channel 1 Line Stride Register
DEFE_LINESTRD2_REG	0x0048	DEFE Channel 2 Line Stride Register
DEFE_INPUT_FMT_REG	0x004C	DEFE Input Format Register
DEFE_WB_ADDR0_REG	0x0050	DEFE Channel 3 Write Back Address Register
DEFE_OUTPUT_FMT_REG	0x005C	DEFE Output Format Register
DEFE_INT_EN_REG	0x0060	DEFE Interrupt Enable Register
DEFE_INT_STATUS_REG	0x0064	DEFE Interrupt Status Register
DEFE_STATUS_REG	0x0068	DEFE Status Register
DEFE_CSC_COEF00_REG	0x0070	DEFE CSC Coefficient 00 Register
DEFE_CSC_COEF01_REG	0x0074	DEFE CSC Coefficient 01 Register
DEFE_CSC_COEF02_REG	0x0078	DEFE CSC Coefficient 02 Register
DEFE_CSC_COEF03_REG	0x007C	DEFE CSC Coefficient 03 Register
DEFE_CSC_COEF10_REG	0x0080	DEFE CSC Coefficient 10 Register
DEFE_CSC_COEF11_REG	0x0084	DEFE CSC Coefficient 11 Register
DEFE_CSC_COEF12_REG	0x0088	DEFE CSC Coefficient 12 Register
DEFE_CSC_COEF13_REG	0x008C	DEFE CSC Coefficient 13 Register
DEFE_CSC_COEF20_REG	0x0090	DEFE CSC Coefficient 20 Register
DEFE_CSC_COEF21_REG	0x0094	DEFE CSC Coefficient 21 Register
DEFE_CSC_COEF22_REG	0x0098	DEFE CSC Coefficient 22 Register
DEFE_CSC_COEF23_REG	0x009C	DEFE CSC Coefficient 23 Register
DEFE_WB_LINESTRD_EN_REG	0x00D0	DEFE Write Back Line Stride Enable Register
DEFE_WB_ LINESTRD0_REG	0x00D4	DEFE Write Back Channel 3 Line Stride Register
DEFE_CH0_INSIZE_REG	0x0100	DEFE Channel 0 Input Size Register
DEFE_CH0_OUTSIZE_REG	0x0104	DEFE Channel 0 Output Size Register
DEFE_CH0_HORZFACT_REG	0x0108	DEFE Channel 0 Horizontal Factor Register
DEFE_CH0_VERTFACT_REG	0x010C	DEFE Channel 0 Vertical factor Register
DEFE_CH0_HORZPHASE_REG	0x0110	DEFE Channel 0 Horizontal Initial Phase Register
DEFE_CH0_VERTPHASE0_REG	0x0114	DEFE Channel 0 Vertical Initial Phase 0 Register
DEFE_CH0_VERTPHASE1_REG	0x0118	DEFE Channel 0 Vertical Initial Phase 1 Register
DEFE_CH1_INSIZE_REG	0x0200	DEFE Channel 1 Input Size Register
DEFE_CH1_OUTSIZE_REG	0x0204	DEFE Channel 1 Output Size Register
DEFE_CH1_HORZFACT_REG	0x0208	DEFE Channel 1 Horizontal Factor Register
DEFE_CH1_VERTFACT_REG	0x020C	DEFE Channel 1 Vertical factor Register
DEFE_CH1_HORZPHASE_REG	0x0210	DEFE Channel 1 Horizontal Initial Phase Register
DEFE_CH1_VERTPHASE0_REG	0x0214	DEFE Channel 1 Vertical Initial Phase 0 Register

DEFE_CH1_VERTPHASE1_REG	0x0218	DEFE Channel 1 Vertical Initial Phase 1 Register
DEFE_CH0_HORZCOEF_REGN	0x0400+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register N=0:31
DEFE_CH0_VERTCOEF_REGN	0x0500+N*4	DEFE Channel 0 Vertical Filter Coefficient Register N=0:31
DEFE_CH1_HORZCOEF_REGN	0x0600+N*4	DEFE Channel 1 Horizontal Filter Coefficient Register N=0:31
DEFE_CH1_VERTCOEF_REGN	0x0700+N*4	DEFE Channel 1 Vertical Filter Coefficient Register N=0:31

Note: Registers 0x0008~0x0218 except status registers are double buffered. when a new frame process starts and the buffered register configuration ready bit in frame process control register is set, the value of corresponding internal configuration register will be refreshed by this register, and programmers always can't read the value of corresponding internal register.

26.5. DEFE Register Description

26.5.1. DEFE_EN_REG(Default: 0x00000000)

Offset: 0x0			Register Name: DEFE_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EN DEFE enable 0: Disable 1: Enable When DEFE enable bit is disabled, the clock of DEFE module will be disabled. If this bit transits from 0 to 1, the frame process control register and the interrupt enable register will be initialized to default value, and the state machine of the module is reset.

26.5.2. DEFE_FRM_CTRL_REG(Default: 0x00000000)

Offset: 0x4			Register Name: DEFE_FRM_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	R/W	0	COEF_ACCESS_CTRL Fir coef ram access control 0: CPU doesn't access fir coef ram 1: CPU will access fir coef ram This bit will be set to 1 before CPU accesses fir coef ram
22:17	/	/	/
16	R/W	0x0	FRM_START Frame start & reset control 0: reset 1: start If the bit is written to zero, the whole state machine and data paths of DEFE module will be reset. When the bit is written to 1, DEFE will start a new frame process.
15:12	/	/	/
11	R/W	0x0	OUT_CTRL DEFE output control 0: enable DEFE output to DEBE 1: disable DEFE output to DEBE If DEFE write back function is enabled, DEFE output to DEBE isn't recommended.
10:3	/	/	/
2	R/W	0x0	WB_EN

			Write back enable 0: Disable 1: Enable If output to DEBE is enabled, the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be self-cleared when writing-back frame process starts.
1	/	/	/
0	R/W	0x0	REG_RDY_EN Register ready enable 0: not ready 1: registers configuration ready Just as filter coefficients configuration, in order to ensure the display to be correct, the correlative display configuration registers are buffered too, and programmers also can change the value of correlative registers in any time. When the registers setting is finished, the programmer should set the bit if the new configuration is needed in next scaling frame. When the new frame starts, the bit will also be self-cleared.

26.5.3. DEFE_BYPASS_REG(Default: 0x00000000)

Offset: 0x8			Register Name: DEFE_BYPASS_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0x0	CSC_BYPASS_EN CSC by-pass enable 0: CSC enable 1: CSC will be by-passed Actually, in order to ensure the module working to be correct, this bit only can be set when input data format is the same as output data format (both YUV or both RGB)
0	/	/	/

26.5.4. DEFE_AGTH_SEL_REG(Default: 0x00000000)

Offset: 0xC			Register Name: DEFE_AGTH_SEL_REG
Bit	Read/Write	Default/Hex	Description
31:9	/	/	/
8	R/W	0x0	LINEBUF_AGTH DEFE line buffer algorithm select 0: horizontal filtered result 1: original data
7:0	/	/	/

26.5.5. DEFE_LINT_CTRL_REG(Default: 0x00000000)

Offset: 0x10			Register Name: DEFE_LINT_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R	0x0	CURRENT_LINE
15	R/W	0x0	FIELD_SEL Field select 0: each field 1: end field(field counter in reg0x2c)
14:13	/	/	/

12:0	R/W	0x0	TRIG_LINE Trigger line number of line interrupt

26.5.6. DEFE_BUF_ADDR0_REG(Default: 0x00000000)

Offset: 0x20			Register Name: DEFE_BUF_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generate output frame. In non-tile-based type: The address is the start address of the first line.

26.5.7. DEFE_BUF_ADDR1_REG(Default: 0x00000000)

Offset: 0x24			Register Name: DEFE_BUF_ADDR1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generate output frame. In non-tile-based type: The address is the start address of the first line.

26.5.8. DEFE_BUF_ADDR2_REG(Default: 0x00000000)

Offset: 0x28			Register Name: DEFE_BUF_ADDR2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	BUF_ADDR DEFE frame buffer address In tile-based type: The address is the start address of the line in the first tile used to generate output frame. In non-tile-based type: The address is the start address of the first line.

26.5.9. DEFE_FIELD_CTRL_REG(Default: 0x00000000)

Offset: 0x2C			Register Name: DEFE_FIELD_CTRL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	0x0	FIELD_LOOP_MOD Field loop mode 0：the last field； 1：the full frame
11	/	/	/
10:8	R/W	0x0	VALID_FIELD_CNT Valid field counter bit the valid value = this value + 1；
7:0	R/W	0x0	FIELD_CNT Field counter each bit specify a field to display，0：top field，1：bottom field

26.5.10. DEFE_TB_OFF0_REG(Default: 0x00000000)

Offset: 0x30			Register Name: DEFE_TB_OFF0_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

26.5.11. DEFE_TB_OFF1_REG(Default: 0x00000000)

Offset: 0x34			Register Name: DEFE_TB_OFF1_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

26.5.12. DEFE_TB_OFF2_REG(Default: 0x00000000)

Offset: 0x38			Register Name: DEFE_TB_OFF2_REG
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:16	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:13	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

26.5.13. DEFE_LINESTRD0_REG(Default: 0x00000000)

Offset: 0x40			Register Name: DEFE_LINESTRD0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LINE_STRIDE In tile-based type The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) In non-tile-based type The stride length is the distance from the start of one line to the start of the next line.

26.5.14. DEFE_LINESTRD1_REG(Default: 0x00000000)

Offset: 0x44			Register Name: DEFE_LINESTRD1_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LINE_STRIDE In tile-based type The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) In non- tile-based type The stride length is the distance from the start of one line to the start of the next line.

26.5.15. DEFE_LINESTRD2_REG(Default: 0x00000000)

Offset: 0x48			Register Name: DEFE_LINESTRD2_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LINE_STRIDE In tile-based type The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) In non- tile-based type The stride length is the distance from the start of one line to the start of the next line.

26.5.16. DEFE_INPUT_FMT_REG(Default: 0x00000000)

Offset: 0x4C			Register Name: DEFE_INPUT_FMT_REG
Bit	Read/Write	Default/Hex	Description
31:17	/	/	/
16	R/W	0x0	BYTE_SEQ Input data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word)
15:13	/	/	/
12	R/W	0x0	SCAN_MOD Scanning Mode selection 0: non-interlace 1: interlace
11	/	/	/
10:8	R/W	0x0	DATA_MOD Input data mode selection 000: non-tile-based planar data 001: interleaved data 010: non- tile-based UV combined data 100: tile-based planar data 110: tile-based UV combined data other: reserved
7	/	/	/
6:4	R/W	0x0	DATA_FMT Input component data format In non-tile-based planar data mode: 000: YUV 4:4:4 001: YUV 4:2:2 010: YUV 4:2:0

			011: YUV 4:1:1 100: CSI RGB data 101: RGB888 Other: Reserved In interleaved data mode: 000: YUV 4:4:4 001: YUV 4:2:2 101: ARGB8888 Other: reserved In non-tile-based UV combined data mode: 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved In tile-based planar data mode: 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: Reserved In tile-based UV combined data mode: 001: YUV 4:2:2 010: YUV 4:2:0 011: YUV 4:1:1 Other: reserved
3:2	/	/	/
1:0	R/W	0x0	DATA_PS Pixel sequence In interleaved YUV422 data mode: 00: Y1V0Y0U0 01: V0Y1U0Y0 10: Y1U0Y0V0 11: U0Y1V0Y0 In interleaved YUV444 data mode: 00: VUYA 01: AYUV Other: reserved In UV combined data mode: (UV component) 00: V1U1V0U0 01: U1V1U0V0 Other: reserved In interleaved ARGB8888 data mode: 00: BGRA 01: ARGB Other: reserved

26.5.17. DEFE_WB_ADDR0_REG(Default: 0x00000000)

Offset: 0x50			Register Name: DEFE_WB_ADDR0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	WB_ADDR Write-back address setting for scaled data.

26.5.18. DEFE_OUTPUT_FMT_REG(Default: 0x00000000)

Offset: 0x5C			Register Name: DEFE_OUTPUT_FMT_REG
Bit	Read/Write	Default/Hex	Description

31:18	/	/	/
17:16	R/W	0	WB_Ch_Sel Write back channel select(chsel) 0/1: Ch3 2: Ch4 3: Ch5 Other: reserved
15:9	/	/	/
8	R/W	0x0	BYTE_SEQ Output data byte sequence selection 0: P3P2P1P0(word) 1: P0P1P2P3(word) For ARGB, when this bit is 0, the byte sequence is BGRA, and when this bit is 1, the byte sequence is ARGB;
7:5	/	/	/
4	R/W	0x0	SCAN_MOD Output interlace enable 0: disable 1: enable When output interlace enable, scaler selects YUV initial phase according to LCD field signal
3	/	/	/
2:0	R/W	0x0	DATA_FMT Data format 000: planar RGB888 conversion data format 001: interleaved BGRA8888 conversion data format(A component always be pad 0xff) 010: interleaved ARGB8888 conversion data format(A component always be pad 0xff) 100: planar YUV 444 101: planar YUV 420(only support YUV input and not interleaved mode) 110: planar YUV 422(only support YUV input) 111: planar YUV 411(only support YUV input) Other: reserved

26.5.19. DEFE_INT_EN_REG(Default: 0x00000000)

Offset: 0x60			Register Name: DEFE_INT_EN_REG
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	REG_LOAD_EN Register ready load interrupt enable
9	R/W	0x0	LINE_EN Line interrupt enable
8	/	/	/
7	R/W	0x0	WB_EN Write-back end interrupt enable 0: Disable 1: Enable
6:0	/	/	/

26.5.20. DEFE_INT_STATUS_REG(Default: 0x00000000)

Offset: 0x64	Register Name: DEFE_INT_STATUS_REG

Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0x0	REG_LOAD_STATUS Register ready load interrupt status
9	R/W	0x0	LINE_STATUS Line interrupt status
8	/	/	/
7	R/W	0x0	WB_STATUS Write-back end interrupt status
6:0	/	/	/

26.5.21. DEFE_STATUS_REG

Offset: 0x68			Register Name: DEFE_STATUS_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R	0x0	LINE_ON_SYNC Line number(when sync reached)
15	R/W	0x0	WB_ERR_SYNC Sync reach flag when capture in process
14	R/W	0x0	WB_ERR_LOSEDATA Lose data flag when capture in process
13	/	/	/
12	R	0x0	WB_ERR_STATUS write-back error status 0: valid write back 1: un-valid write back This bit is cleared through writing 0 to reset/start bit in frame control register
11	R	0x0	COEF_ACCESS_STATUS Fir coef access status 0: scaler module can access fir coef RAM 1: CPU can access fir coef ram This bit must be 1 before CPU accesses fir coef RAM. When this bit is 1, scaler module will fetch 0x00004000 from RAM.
10:6	/	/	/
5	R	0x0	LCD_FIELD LCD field status 0: top field 1: bottom field
4	R	0x0	DRAM_STATUS Access dram status 0: idle 1: busy This flag indicates whether DEFE is accessing dram
3	/	/	/
2	R	0x0	CFG_PENDING Register configuration pending 0: no pending 1: configuration pending This bit indicates the registers for the next frame has been configured. This bit will be set when configuration ready bit is set and this bit will be cleared when a new frame process begins.
1	R	0x0	WB_STATUS Write-back process status 0: write-back end or write-back disable

			1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process ends.
0	R	0x0	FRM_BUSY Frame busy. This flag indicates that the frame is being processed. The bit will be set when frame process reset & start is set, and be cleared when frame process is reset or disabled.

26.5.22. DEFE_CSC_COEF00_REG(Default: 0x00000000)

Offset: 0x70			Register Name: DEFE_CSC_COEF00_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

26.5.23. DEFE_CSC_COEF01_REG(Default: 0x00000000)

Offset: 0x74			Register Name: DEFE_CSC_COEF01_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

26.5.24. DEFE_CSC_COEF02_REG(Default: 0x00000000)

Offset: 0x78			Register Name: DEFE_CSC_COEF02_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient*2^{10}

26.5.25. DEFE_CSC_COEF03_REG(Default: 0x00000000)

Offset: 0x7C			Register Name: DEFE_CSC_COEF03_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0x0	CONT the Y/G constant the value equals to coefficient*2^{4}

26.5.26. DEFE_CSC_COEF10_REG(Default: 0x00000000)

Offset: 0x80			Register Name: DEFE_CSC_COEF10_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

26.5.27. DEFE_CSC_COEF11_REG(Default: 0x00000000)

Offset: 0x84			Register Name: DEFE_CSC_COEF11_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

26.5.28. DEFE_CSC_COEF12_REG(Default: 0x00000000)

Offset: 0x88			Register Name: DEFE_CSC_COEF12_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient*2^{10}

26.5.29. DEFE_CSC_COEF13_REG(Default: 0x00000000)

Offset: 0x8C			Register Name: DEFE_CSC_COEF13_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x0	CONT the U/R constant the value equals to coefficient*2^{4}

26.5.30. DEFE_CSC_COEF20_REG(Default: 0x00000000)

Offset: 0x90			Register Name: DEFE_CSC_COEF20_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

26.5.31. DEFE_CSC_COEF21_REG(Default: 0x00000000)

Offset: 0x94			Register Name: DEFE_CSC_COEF21_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

26.5.32. DEFE_CSC_COEF22_REG(Default: 0x00000000)

Offset: 0x98			Register Name: DEFE_CSC_COEF22_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient*2^{10}

26.5.33. DEFE_CSC_COEF23_REG(Default: 0x00000000)

Offset: 0x9C			Register Name: DEFE_CSC_COEF23_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x0	CONT the V/B constant the value equals to coefficient*2^4

26.5.34. DEFE_WB_LINESTRD_EN_REG(Default: 0x00000000)

Offset: 0xD0			Register Name: DEFE_WB_LINESTRD_EN_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	0x0	EN Write back line-stride enable 0: disable 1: enable

26.5.35. DEFE_WB_LINESTRD0_REG(Default: 0x00000000)

Offset: 0xD4			Register Name: DEFE_WB_LINESTRD0_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0x0	LINE_STRD Ch3 write back line-stride

26.5.36. DEFE_CH0_INSIZE_REG(Default: 0x00000000)

Offset: 0x100			Register Name: DEFE_CH0_INSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image Y/G component height Input image height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image Y/G component width The image width = The value of these bits add 1 When line buffer result selection is original data, the maximum width is 2048.

26.5.37. DEFE_CH0_OUTSIZE_REG(Default: 0x00000000)

Offset: 0x104			Register Name: DEFE_CH0_OUTSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer Y/G component height The output layer height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output layer Y/G component width The output layer width = The value of these bits add 1

			When line buffer result selection is horizontal filtered result, the maximum width is 2048

26.5.38. DEFE_CH0_HORZFACT_REG(Default: 0x00000000)

Offset: 0x108			Register Name: DEFE_CH0_HORZFACT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

26.5.39. DEFE_CH0_VERTFACT_REG(Default: 0x00000000)

Offset: 0x10C			Register Name: DEFE_CH0_VERTFACT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

26.5.40. DEFE_CH0_HORZPHASE_REG(Default: 0x00000000)

Offset: 0x110			Register Name: DEFE_CH0_HORZPHASE_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

26.5.41. DEFE_CH0_VERTPHASE0_REG(Default: 0x00000000)

Offset: 0x114			Register Name: DEFE_CH0_VERTPHASE0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in vertical for top field (complement) This value equals to initial phase * 2^{16}

26.5.42. DEFE_CH0_VERTPHASE1_REG(Default: 0x00000000)

Offset: 0x118			Register Name: DEFE_CH0_VERTPHASE1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE Y/G component initial phase in vertical for bottom field (complement) This value equals to initial phase * 2^{16}

26.5.43. DEFE_CH1_INSIZE_REG(Default: 0x00000000)

Offset: 0x200			Register Name: DEFE_CH1_INSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	IN_HEIGHT Input image U/R component height Input image height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image U/R component width The image width = The value of these bits add 1 When line buffer result selection is original data, the maximum width is 2048

26.5.44. DEFE_CH1_OUTSIZE_REG(Default: 0x00000000)

Offset: 0x204			Register Name: DEFE_CH1_OUTSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:29	/	/	/
28:16	R/W	0x0	OUT_HEIGHT Output layer U/R component height The output layer height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	0x0	OUT_WIDTH Output layer U/R component width The output layer width = The value of these bits add 1 When line buffer result selection is horizontal filtered result, the maximum width is 2048

26.5.45. DEFE_CH1_HORZFACT_REG(Default: 0x00000000)

Offset: 0x208			Register Name: DEFE_CH1_HORZFACT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width

26.5.46. DEFE_CH1_VERTFACT_REG(Default: 0x00000000)

Offset: 0x20C			Register Name: DEFE_CH1_VERTFACT_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

26.5.47. DEFE_CH1_HORZPHASE_REG(Default: 0x00000000)

Offset: 0x210			Register Name: DEFE_CH1_HORZPHASE_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

26.5.48. DEFE_CH1_VERTPHASE0_REG(Default: 0x00000000)

Offset: 0x214			Register Name: DEFE_CH1_VERTPHASE0_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in vertical for top field (complement) This value equals to initial phase * 2^{16}

26.5.49. DEFE_CH1_VERTPHASE1_REG(Default: 0x00000000)

Offset: 0x218			Register Name: DEFE_CH1_VERTPHASE1_REG
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in vertical for bottom field (complement) This value equals to initial phase * 2^{16}

26.5.50. DEFE_CH0_HORZCOEF0_REGN (N=0:31) (Default: 0x00000000)

Offset: 0x400+N*4			Register Name: DEFE_CH0_HORZCOEF0_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

26.5.51. DEFE_CH0_VERTCOEF_REGN (N=0:31) (Default: 0x00000000)

Offset: 0x500+N*4			Register Name: DEFE_CH0_VERTCOEF_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1

			Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

26.5.52. DEFE_CH1_HORZCOEF0_REGN (N=0:31) (Default: 0x00000000)

Offset: 0x600+N*4			Register Name: DEFE_CH1_HORZCOEF0_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient*2^6

26.5.53. DEFE_CH1_VERTCOEF_REGN (N=0:31) (Default: 0x00000000)

Offset: 0x700+N*4			Register Name: DEFE_CH1_VERTCOEF_REGN
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient*2^6
23:16	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient*2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient*2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient*2^6

Chapter 27 Display Engine Back End (DEBE)

27.1. Overview

The Display Engine Back End (DEBE) features:

- 4 moveable & size-adjustable layers
- Layer size up to 8192*8192 pixels
- Support Alpha blending
- Support color key
- Support write back function
- Support 1/2/4/8 bpp mono / palette
- Support 16/24/32 bpp color (external frame buffer)
  - 5/6/5
  - 1/5/5/5
  - 0/8/8/8
  - 8/8/8
  - 8/8/8/8
  - 4/4/4/4
- Support on-chip SRAM
  - 256 entry 32-bpp palette
  - 1/2/4/8 bpp internal frame buffer
  - support Gamma correction
- Support hardware cursor
  - 32x32 @8-bpp
  - 64x64 @2-bpp
  - 64x32 @4-bpp
  - 32x64 @4-bpp
- Support YUV input channel
- Output color correction

27.2. DEBE Block Diagram

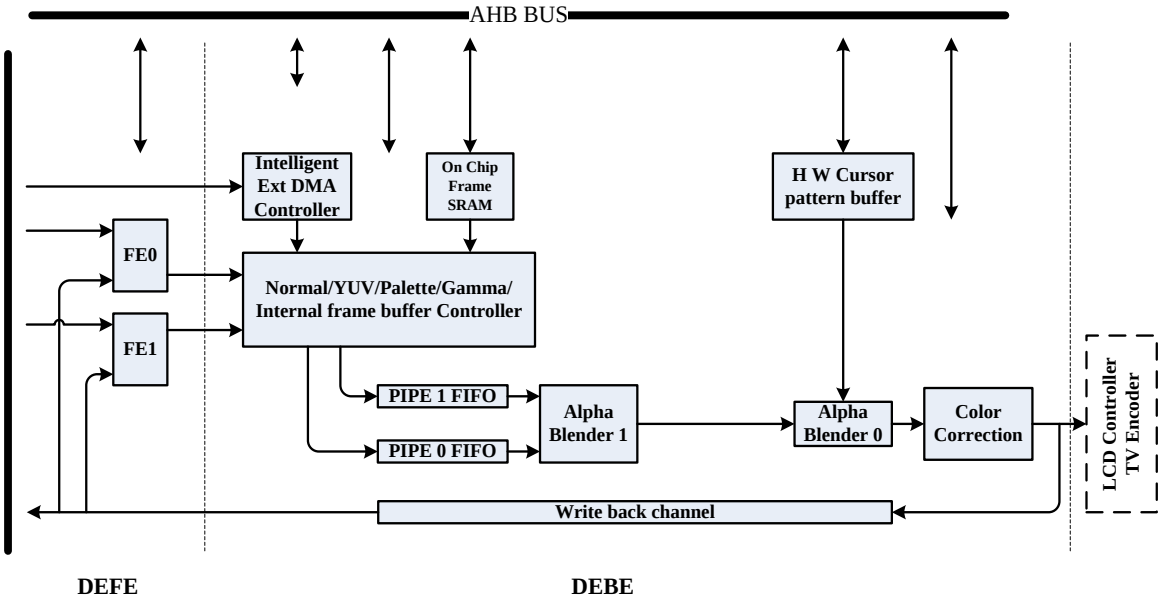


Figure 27-1. Display Engine Block Diagram

27.3. DEBE Description

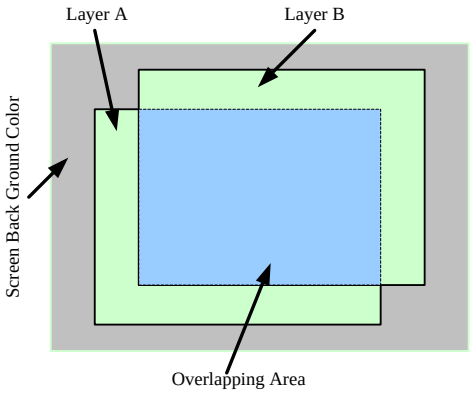
27.3.1. Alpha Blending

Alpha blending is a convex combination of two colors allowing for transparency effects in computer graphics. The value of alpha in the color code ranges from 0.0 to 1.0, where 0.0 represents a fully transparent color, and 1.0 represents a fully opaque color.

In the display engine:

If setting the alpha register value (ARV) = 0B xxxxxxxx (8 bit value)

Then the alpha value (AV) = ARV/256



In the above diagram, layer A and layer B are not in same channel.

The alpha value of layer A : AV_a

The alpha value of layer A : AV_b

The RGB value of layer A : R_a, G_a, B_a

The RGB value of layer B : R_b, G_b, B_b

The RGB value of Background color : R_bg, G_bg, B_b

In the only layer A area:

R = R_a * AV_a + R_bg * (1-AV_a)

G = G_a * AV_a + G_bg * (1-AV_a)

B = B_a * AV_a + B_bg * (1-AV_a)

In the only layer B area:

R = R_b * AV_b + R_bg * (1-AV_b)

G = G_b * AV_b + G_bg * (1-AV_b)

B = B_b * AV_b + B_bg * (1-AV_b)

In the overlapping area:

If the priority of layer A is higher than layer B

R = R_a * AV_a + (R_b * AV_b +R_bg * (1-AV_b)) * (1-AV_a)

G = G_a * AV_a + (G_b * AV_b +G_bg * (1-AV_b)) * (1-AV_a)

B = B_a * AV_a + (B_b * AV_b +B_bg * (1-AV_b)) * (1-AV_a)

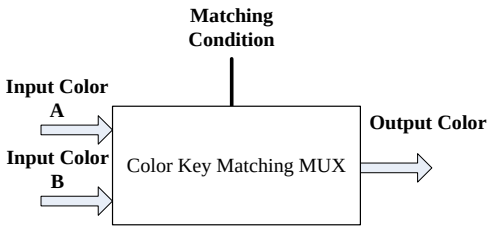
If the priority of layer A is lower than layer B

R = (R_a * AV_a +R_bg * (1-AV_a)) * (1-AV_b) + R_b * AV_b

G = (G_a * AV_a +G_bg * (1-AV_a)) * (1-AV_b) + G_b * AV_b

B = (B_a * AV_a +B_bg * (1-AV_a)) * (1-AV_b) + B_b * AV_b

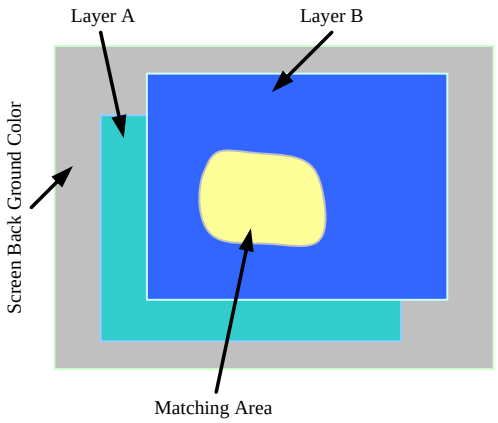
27.3.2. Color Key



Color Key Theory Block

In display engine, the process of color key will be done in Alpha Blender1 block. Only 2 channels can process color key at the same coordinate of screen. If both channels are set into color key mode, the higher priority channel will match another channel.

See the following diagram



The alpha value of layer A : AV_a

The alpha value of layer A : AV_b

The RGB value of layer A : R_a, G_a, B_a

The RGB value of layer B : R_b, G_b, B_b

The RGB value of Background color : R_bg, G_bg, B_bg

In none matching area:

As same as normal alpha blending process

In matching area:

If priority of layer A > priority of layer B

Layer A color key setting status: True

Layer B color key setting status: True or false

Color key selection: Layer A match layer B

R = R_a * AV_a + R_bg * (1-AV_a)

G = G_a * AV_a + G_bg * (1-AV_a)

B = B_a * AV_a + B_bg * (1-AV_a)

If priority of layer A > priority of layer B

Layer A color key setting status: False

Layer B color key setting status: True

Color key selection: Layer B match layer A

R = R_b * AV_b + R_bg * (1-AV_b)

G = G_b * AV_b + G_bg * (1-AV_b)

B = B_b * AV_b + B_bg * (1-AV_b)

27.3.3. PIPE

There are 2 normal pipes in the engine, pipe 0 and pipe1.

In normal mode, the dedicated layer will get the data from system DRAM direct or DEFE by setting dedicated **Layer video channel selection** bit in **DE-layer Attribute control register**. In other work modes, the layer data source also comes from internal frame buffer.

In the same pipe, the highest layer pixel data can pass.

27.4. DEBE Register list

Module name	Base address
DEBE	0x01e60000

Register name	Offset	Description
DEBE_MODCTL_REG	0x800	DEBE mode control register
DEBE_BACKCOLOR_REG	0x804	DE-back color control register
DEBE_DISSIZE_REG	0x808	DE-back display size setting register
DEBE_LAYSIZE_REG	0x810 – 0x81C	DE-layer size register
DEBE_LAYCOOR_REG	0x820 – 0x82C	DE-layer coordinate control register
DEBE_LAYLINEWIDTH_REG	0x840 – 0x84C	DE-layer frame buffer line width register
DEBE_LAYFB_L32ADD_REG	0x850 – 0x85C	DE-layer frame buffer low 32 bit address register
DEBE_LAYFB_H4ADD_REG	0x860	DE-layer frame buffer high 4 bit address register
DEBE_REGBUFFCTL_REG	0x870	DE-Register buffer control register
DEBE_CKMAX_REG	0x880	DE-color key MAX register
DEBE_CKMIN_REG	0x884	DE-color key MIN register
DEBE_CKCFG_REG	0x888	DE-color key configuration register
DEBE_ATTCTL_REG0	0x890 – 0x89C	DE-layer attribute control register0
DEBE_ATTCTL_REG1	0x8A0 – 0x8AC	DE-layer attribute control register1
DEBE_HWCCTL_REG	0x8D8	DE-HWC coordinate control register

DEBE_HWCFBCTL_REG	0x8E0	DE-HWC frame buffer format register
DEBE_WBCTL_REG	0x8F0	DEBE write back control register
DEBE_WBADD_REG	0x8F4	DEBE write back address register
DEBE_WBLINEWIDTH_REG	0x8F8	DEBE write back buffer line width register
DEBE_IYUVCTL_REG	0x920	DEBE input YUV channel control register
DEBE_IYUVADD_REG	0x930 – 0x938	DEBE YUV channel frame buffer address register
DEBE_IYUVLINEWIDTH_REG	0x940 – 0x948	DEBE YUV channel buffer line width register
DEBE_YGCOEF_REG	0x950 – 0x958	DEBE Y/G coefficient register
DEBE_YGCONS_REG	0x95C	DEBE Y/G constant register
DEBE_URCOEF_REG	0x960 – 0x968	DEBE U/R coefficient register
DEBE_URCONS_REG	0x96C	DEBE U/R constant register
DEBE_VBCOEF_REG	0x970 – 0x978	DEBE V/B coefficient register
DEBE_VBCONS_REG	0x97C	DEBE V/B constant register
DEBE_OCCTL_REG	0x9C0	DEBE output color control register
DEBE_OCRCOEF_REG	0x9D0-0x9D8	DEBE output color R coefficient register
DEBE_OCRCONS_REG	0x9DC	DEBE output color R constant register
DEBE_OCGCOEF_REG	0x9E0-0x9E8	DEBE output color G coefficient register
DEBE_OCGCONS_REG	0x9EC	DEBE output color G constant register
DEBE_OCBCOEF_REG	0x9F0-0x9F8	DEBE output color B coefficient register
DEBE_OCBCONS_REG	0x9FC	DEBE output color B constant register
/	Memories	/
/	0x4400-0x47FF	Gamma table
	0x4800-0x4BFF	DE-HWC pattern memory block
	0x4C00-0x4FFF	DE-HWC color palette table
	0x5000-0x53FF	Pipe0 palette table
	0x5400-0x57FF	Pipe1 palette table

27.5. DEBE Register Description

27.5.1. DEBE Mode Control Register (Default: 0x00000000)

Offset: 0x800			Register Name: DEBE_MODCTL_REG
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29	R/W	0	LINE_SEL Start top/bottom line selection in interlace mode
28	R/W	0	ITLMOD_EN Interlace mode enable 0:disable 1:enable
27:17	/	/	/
16	R/W	0	HWC_EN Hardware cursor enabled/disabled control 0: Disabled 1: Enabled Hardware cursor has the highest priority, in the alpha blender0, the alpha value of cursor will be selected
15:12	/	/	/
11	R/W	0	LAY3_EN Layer3 Enable/Disable 0: Disabled 1: Enabled
10	R/W	0	LAY2_EN Layer2 Enable/Disable

			0: Disabled 1: Enabled
9	R/W	0	LAY1_EN Layer1 Enable/Disable 0: Disabled 1: Enabled
8	R/W	0	LAY0_EN Layer0 Enable/Disable 0: Disabled 1: Enabled
7:2	/	/	/
1	R/W	0	START_CTL Normal output channel Start & Reset control 0: reset 1: start
0	R/W	0	DEBE_EN DEBE enable/disable 0: disable 1: enable

27.5.2. DE-Back Color Control Register

Offset: 0x804			Register Name: DEBE_BACKCOLOR_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	UDF	BK_RED Red Red screen background color value
15:8	R/W	UDF	BK_GREEN Green Green screen background color value
7:0	R/W	UDF	BK_BLUE Blue Blue screen background color value

27.5.3. DE-Back Display Size Setting Register

Offset: 0x808			Register Name: DEBE_DISSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	UDF	DIS_HEIGHT Display height The real display height = The value of these bits add 1
15:0	R/W	UDF	DIS_WIDTH Display width The real display width = The value of these bits add 1

27.5.4. DE-Layer Size Register

Offset: Layer 0: 0x810 Layer 1: 0x814 Layer 2: 0x818 Layer 3: 0x81C			Register Name: DEBE_LAYSIZE_REG
Bit	Read/Write	Default/Hex	Description

31:29	/	/	/
28:16	R/W	UDF	LAY_HEIGHT Layer Height The Layer Height = The value of these bits add 1
15:13	/	/	/
12:0	R/W	UDF	LAY_WIDTH Layer Width The Layer Width = The value of these bits add 1

27.5.5. DE-Layer Coordinate Control Register

Offset: Layer 0: 0x820 Layer 1: 0x824 Layer 2: 0x828 Layer 3: 0x82C			Register Name: DEBE_LAYCOOR_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	UDF	LAY_YCOOR Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represents the two's complement
15:0	R/W	UDF	LAY_XCOOR X coordinate X is left-top x coordinate of the layer on screen in pixels The X represents the two's complement

Setting the layer0-layer3 the coordinate (left-top) on screen control information

27.5.6. DE-Layer Frame Buffer Line Width Register

Offset: Layer 0: 0x840 Layer 1: 0x844 Layer 2: 0x848 Layer 3: 0x84C			Register Name: DEBE_LAYLINEWIDTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	LAY_LINEWIDTH Layer frame buffer line width in bits

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

27.5.7. DE-Layer Frame Buffer Low 32 Bit Address Register

Offset: Layer 0: 0x850 Layer 1: 0x854 Layer 2: 0x858 Layer 3: 0x85C			Register Name: DEBE_LAYFB_L32ADD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	LAYFB_L32ADD Buffer start Address Layer Frame start Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

27.5.8. DE-Layer Frame Buffer High 4 Bit Address Register

Offset: 0x860			Register Name: DEBE_LAYFB_H4ADD_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	UDF	LAY3FB_H4ADD Layer3 Layer Frame Buffer Address in bit
23:20	/	/	/
19:16	R/W	UDF	LAY2FB_H4ADD Layer2 Layer Frame Buffer Address in bit
15:12	/	/	/
11:8	R/W	UDF	LAY1FB_H4ADD Layer1 Layer Frame Buffer Address in bit
7:4	/	/	/
3:0	R/W	UDF	LAY0FB_H4ADD Layer0 Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

27.5.9. DE-Register Buffer Control Register (Default: 0x00000000)

Offset: 0x870			Register Name: DEBE_REGBUFFCTL_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0X00	REGAUTOLOAD_DIS Module registers loading auto mode disable control 0: registers auto loading mode 1: disable registers auto loading mode, the registers will be loaded by writing 1 to bit0 of this register
0	R/W	0X00	REGLOADCTL Register load control When the Module registers loading auto mode disable control bit is set, the registers will be loaded by writing 1 to the bit, and the bit will be self cleared after the registers is loaded.

27.5.10. DE-Color Key MAX Register

Offset: 0x880			Register Name: DEBE_CKMAX_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	UDF	CKMAX_R Red Red color key max
15:8	R/W	UDF	CKMAX_G Green Green color key max
7:0	R/W	UDF	CKMAX_B Blue Blue color key max

27.5.11. DE-Color Key MIN Register

Offset: 0x884			Register Name: DEBE_CKMIN_REG
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	UDF	CKMIN_R Red Red color key min
15:8	R/W	UDF	CKMIN_G Green Green color key min
7:0	R/W	UDF	CKMIN_B Blue Blue color key min

27.5.12. DE-Color Key Configuration Register

Offset: 0x888			Register Name: DEBE_CKCFG_REG
Bit	Read/Write	Default/Hex	Description
31:06	/	/	/
5:4	R/W	UDF	CKR_MATCH Red Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
3:2	R/W	UDF	CKG_MATCH Green Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
1:0	R/W	UDF	CKB_MATCH Blue Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)

27.5.13. DE-Layer Attribute Control Register0

Offset: Layer0: 0x890 Layer1: 0x894 Layer2: 0x898 Layer3: 0x89C			Register Name: DEBE_ATTCTL_REG0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	LAY_GLBALPHA Alpha value Alpha value is used for this layer
23:22	R/W	UDF	LAY_WORKMOD Layer working mode selection 00: normal mode (Non-Index mode)

			01: palette mode (Index mode) 10: internal frame buffer mode 11: gamma correction Except the normal mode, if the other working mode is selected, the on chip SRAM will be enabled.
21:20	R/W	UDF	PREMUL 0: normal input layer 1: pre-multiply input layer Other: reserved
19:18	R/W	UDF	CKEN Color key Mode 00: disabled color key 01: The layer color key matches another channel pixel data in Alpha Blender1. 1x: Reserved Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:16	/	/	/
15	R/W	UDF	LAY_PIPESEL Pipe Select 0: select Pipe 0 1: select Pipe 1
14:12	/	/	/
11:10	R/W	UDF	LAY_PRISEL Priority The rule is: 11>10>01>00 When more than 2 layers are enabled, the priority value of each layer must be different, so designers must keep the condition. If more than 1 layers select the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1. If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.
9:3	/	/	/
2	R/W	UDF	LAY_YUVEN YUV channel selection 0: disable 1: enable Setting 2 or more layers YUV channel mode is illegal, so programmers should confirm it.
1	R/W	UDF	LAY_VDOEN Layer video channel selection enable control 0: disable 1: enable Normally, one layer can not be set both video channel and YUV channel mode. If both 2 mode are set, the layer will work in video channel mode, and YUV channel mode will be ignored, so programmers should confirm it. Setting 2 or more layers video channel mode is illegal, and programmers should confirm it.
0	R/W	UDF	LAY_GLBALPHAEN

			Alpha Enable 0: Disabled the alpha value of this register 1: Enabled the alpha value of this register for the layer

27.5.14. DE-Layer Attribute Control Register1

Offset: Layer0: 0x8A0 Layer1: 0x8A4 Layer2: 0x8A8 Layer3: 0x8AC			Register Name: DEBE_ATTCTL_REG1
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15:14	R/W	UDF	LAY_HSCAFCT Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode SH Height scale factor 00: no scaling 01: *2 10: *4 11: Reserved
13:12	R/W	UDF	LAY_WSCAFCT Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode SW Width scale factor 00: no scaling 01: *2 10: *4 11: Reserved
11:8	R/W	UDF	LAY_FBFMT Frame buffer format Normal mode data format 0000: mono 1-bpp 0001: mono 2-bpp 0010: mono 4-bpp 0011: mono 8-bpp 0100: color 16-bpp (R:6/G:5/B:5) 0101: color 16-bpp (R:5/G:6/B:5) 0110: color 16-bpp (R:5/G:5/B:6) 0111: color 16-bpp (Alpha:1/R:5/G:5/B:5) 1000: color 16-bpp (R:5/G:5/B:5/Alpha:1) 1001: color 24-bpp (Padding:8/R:8/G:8/B:8) 1010: color 32-bpp (Alpha:8/R:8/G:8/B:8) 1011: color 24-bpp (R:8/G:8/B:8) 1100: color 16-bpp (Alpha:4/R:4/G:4/B:4) 1101: color 16-bpp (R:4/G:4/B:4/Alpha:4) Other: Reserved Palette Mode data format In palette mode, the data of external frame buffer is regarded as pattern. 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp

			0011: 8-bpp other: Reserved Internal Frame buffer mode data format 0000: 1-bpp 0001: 2-bpp 0010: 4-bpp 0011: 8-bpp Other: Reserved
7:3	/	/	/
2	R/W	UDF	LAY_BRSWAPEN B R channel swap 0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
1:0	R/W	UDF	LAY_FBPS PS Pixels Sequence See the follow table “Pixels Sequence”

27.5.15. Pixels Sequence Table

DE-layer attribute control register1 [11:08] = FBF (frame buffer format)

DE-layer attribute control register1 [01:00] = PS (pixels sequence)

Mono or Internal Frame Buffer 1-Bpp Or Palette 1-Bpp Mode : FBF = 0000

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P24	P25	P26	P27	P28	P29	P30	P31	P16	P17	P18	P19	P20	P21	P22	P23
P08	P09	P10	P11	P12	P13	P14	P15	P00	P01	P02	P03	P04	P05	P06	P07
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P07	P06	P05	P04	P03	P02	P01	P00	P15	P14	P13	P12	P11	P10	P09	P08
P23	P22	P21	P20	P19	P18	P17	P16	P31	P30	P29	P28	P27	P26	P25	P24

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P00	P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15
P16	P17	P18	P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Mono or Internal Frame Buffer 2-Bpp Or Palette 2-Bpp Mode : FBF = 0001

PS=00

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P15	P14	P13	P12	P11	P10	P09	P08
P07	P06	P05	P04	P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P12	P13	P14	P15	P08	P09	P10	P11
P04	P05	P06	P07	P00	P01	P02	P03

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P03	P02	P01	P00	P07	P06	P05	P04
P11	P10	P09	P08	P15	P14	P13	P12

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

PS=11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P00		P01		P02		P03		P04		P05		P06		P07	
P08		P09		P10		P11		P12		P13		P14		P15	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Mono 4-bpp or palette 4-bpp mode : FBF = 0010

PS=00

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P07		P06		P05		P04	
P03		P02		P01		P00	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P06		P07		P04		P05	
P02		P03		P00		P01	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P01		P00		P03		P02	
P05		P04		P07		P06	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=11

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P00		P01		P02		P03	
P04		P05		P06		P07	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Mono 8-bpp mode or palette 8-bpp mode : FBF = 0011

PS=00/11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P3								P2							
P1								P0							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01/10

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0								P1							
P2								P3							
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Color 16-bpp mode : FBF = 0100 or 0101 or 0110 or 0111 or 1000

PS=00

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P1															
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
P1															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=10/11

Invalid

Color 24-bpp or 32-bpp mode : FBF = 1001 or 1010

PS=00/01

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The bytes sequence is ARGB

PS=10/11

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

The bytes sequence is BGRA

27.5.16. DE-HWC Coordinate Control Register

Offset: 0x8D8			Register Name: DEBE_HWCCTL_REG
Bit	Read/Write	Default/Hex	Description
31:16	R/W	UDF	HWC_YCOOR Hardware cursor Y coordinate
15:0	R/W	UDF	HWC_XCOOR Hardware cursor X coordinate

27.5.17. DE-HWC Frame Buffer Format Register

Offset: 0x8E0			Register Name: DEBE_HWCFBCTL_REG
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	HWC_YCOOROFF Y coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in Y coordinate
23:16	R/W	UDF	HWC_XCOOROFF X coordinate offset The hardware cursor is 32*32 2-bpp pattern, this value represent the start position of the cursor in X coordinate
15:6	/	/	/
5:4	R/W	UDF	HWC_YSIZE Y size control 00: 32pixels per line 01: 64pixels per line Other: reserved
3:2	R/W	UDF	HWC_XSIZE X size control 00: 32pixels per row

			01: 64pixels per row Other: reserved
1:0	R/W	UDF	HWC_FBFMT Pixels format control 00: 1bpp 01: 2bpp 10: 4bpp 11: 8bpp

27.5.18. DEBE Write Back Control Register

Offset: 0x8F0			Register Name: DEBE_WBCTL_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12	R/W	UDF	WB_FMT Write back data format setting 0:ARGB (little endian system) 1:BGRA (little endian system)
11:10	/	/	/
9	R/W	UDF	WB_EFLAG Error flag 0:/ 1: write back error
8	R/W	UDF	WB_STATUS Write-back process status 0: write-back end or write-back disable 1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process ends.
7:2	/	/	/
1	R/W	UDF	WB_WOC Write back only control 0: disable the write back only control, the normal channel data of back end will transfer to LCD/TV controller too. 1: enable the write back only function, and the all output data will bypass the LCD/TV controller.
0	R/W	UDF	WB_EN Write back enable 0: Disable 1: Enable If normal channel of back-end is selected by LCD/TV controller (write back only function is disabled), the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be cleared when the new writing-back frame starts to process.

27.5.19. DEBE Write Back Address Register

Offset: 0x8F4			Register Name: DEBE_WBADD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	WB_ADD The start address of write back data in WORD

27.5.20. DEBE Write Back Buffer Line Width Register

Offset: 0x8F8			Register Name: DEBE_WBLINEWIDTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	WB_LINEWIDTH Write back image buffer line width in bits

27.5.21. DEBE Input YUV Channel Control Register

Offset: 0x920			Register Name: DEBE_IYUVCTL_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:12	R/W	UDF	IYUV_FBFMT Input data format 000: planar YUV 411 001: planar YUV 422 010: planar YUV 444 011: interleaved YUV 422 100: interleaved YUV 444 Other: illegal
11:10	/	/	/
9:8	R/W	UDF	IYUV_FBPS Pixel sequence In planar data format mode: 00: Y3Y2Y1Y0 01: Y0Y1Y2Y3 (the other 2 components are same) Other: illegal In interleaved YUV 422 data format mode: 00: UYVY 01: YUYV 10: VYUY 11: YVYU In interleaved YUV 444 data format mode: 00: AYUV 01: VUYA Other: illegal
7:5	/	/	/
4	R/W	UDF	IYUV_LINNEREN 0: liner 1:
3:1	/	/	/
0	R/W	UDF	IYUV_EN YUV channel enable control 0: disable 1: enable

Source Data Input Data Ports:

Input buffer channel	Planar YUV	Interleaved YUV
Channel0	Y	YUV
Channel1	U	-

Channel2	V	-

27.5.22. DEBE YUV Channel Frame Buffer Address Register

Offset: Channel 0 : 0x930 Channel 1 : 0x934 Channel 2 : 0x938			Register Name: DEBE_IYUVADD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	IYUV_ADD Buffer Address Frame buffer address in BYTE

27.5.23. DEBE YUV Channel Buffer Line Width Register

Offset: Channel 0 : 0x940 Channel 1 : 0x944 Channel 2 : 0x948			Register Name: DEBE_IYUVLINEWIDTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	UDF	IYUV_LINEWIDTH Line width The width is the distance from the start of one line to the start of the next line. Description in bits

YUV to RGB conversion algorithm formula:

R =
(R Y component coefficient * Y) +
(R U component coefficient * U) +
(R V component coefficient * V) +
R constant

G =
(G Y component coefficient * Y) +
(G U component coefficient * U) +
(G V component coefficient * V) +
G constant

B =
(B Y component coefficient * Y) +
(B U component coefficient * U) +
(B V component coefficient * V) +
B constant

27.5.24. DEBE Y/G Coefficient Register

Offset: G/Y component: 0x950 R/U component: 0x954 B/V component: 0x958			Register Name: DEBE_YGCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/

12:0	R/W	UDF	IYUV_YGCOEF the Y/G coefficient the value equals to coefficient*2^{10}

27.5.25. DEBE Y/G Constant Register

Offset: 0x95C			Register Name: DEBE_YGCONS_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	IYUV_YGCONS the Y/G constant the value equals to coefficient*2^{4}

27.5.26. DEBE U/R Coefficient Register

Offset: G/Y component: 0x960 R/U component: 0x964 B/V component: 0x968			Register Name: DEBE_URCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	UDF	IYUV_URCOEF the U/R coefficient the value equals to coefficient*2^{10}

27.5.27. DEBE U/R Constant Register

Offset: 0x96C			Register Name: DEBE_URCONS_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	IYUV_URCONS the U/R constant the value equals to coefficient*2^{4}

27.5.28. DEBE V/B Coefficient Register

Offset: G/Y component: 0x970 R/U component: 0x974 B/V component: 0x978			Register Name: DEBE_VBCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	UDF	IYUV_VBCOEF the V/B coefficient the value equals to coefficient*2^{10}

27.5.29. DEBE V/B Constant Register

Offset: 0x97C			Register Name: DEBE_VBCONS_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	IYUV_VBCONS the V/B constant

			the value equals to coefficient*2^4

27.5.30. DEBE Output Color Control Register

Offset: 0x9C0			Register Name: DEBE_OCCTL_REG
Bit	Read/Write	Default/Hex	Description
31:1	/	/	/
0	R/W	UDF	OC_EN Color control module enable control 0: disable 1: enable

Color correction conversion algorithm formula:

R =
(R R component coefficient * R) +
(R G component coefficient * G) +
(R B component coefficient * B) +
R constant

G =
(G R component coefficient * R) +
(G G component coefficient * G) +
(G B component coefficient * B) +
G constant

B =
(B R component coefficient * R) +
(B G component coefficient * G) +
(B B component coefficient * B) +
B constant

27.5.31. DEBE Output Color R Coefficient Register

Offset: R component: 0x9D0 G component: 0x9D4 B component: 0x9D8			Register Name: DEBE_OCRCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	OC_RCOEF the R coefficient the value equals to coefficient*2^{10}

27.5.32. DEBE Output Color R Constant Register

Offset: 0x9DC			Register Name: DEBE_OCRCONS_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	UDF	OC_RCONS the R constant the value equals to coefficient*2^4

27.5.33. DEBE Output Color G Coefficient Register

Offset: R component: 0x9E0 G component: 0x9E4 B component: 0x9E8			Register Name: DEBE_OCGCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	OC_GCOEF the G coefficient the value equals to coefficient*2^{10}

27.5.34. DEBE Output Color G Constant Register

Offset: 0x9EC			Register Name: DEBE_OCGCONS_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	UDF	OC_GCONS the G constant the value equals to coefficient*2^{4}

27.5.35. DEBE Output Color B Coefficient Register

Offset: G/Y component: 0x9F0 R/U component: 0x9F4 B/V component: 0x9F8			Register Name: DEBE_OCBCOEF_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	UDF	OC_BCOEF the B coefficient the value equals to coefficient*2^{10}

27.5.36. DEBE Output Color B Constant Register

Offset: 0x9FC			Register Name: DEBE_OCBCONS_REG
Bit	Read/Write	Default/Hex	Description
31:15	/	/	/
14:0	R/W	UDF	OC_BCONS the B constant the value equals to coefficient*2^{4}

27.5.37. DE-HWC Pattern Memory Block

Function:

1bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

2bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P15	P14	P13	P12	P11	P10	P09	P08
P07	P06	P05	P04	P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

4bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P07	P06	P05	P04
P03	P02	P01	P00

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

8bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P3	P2
P1	P0

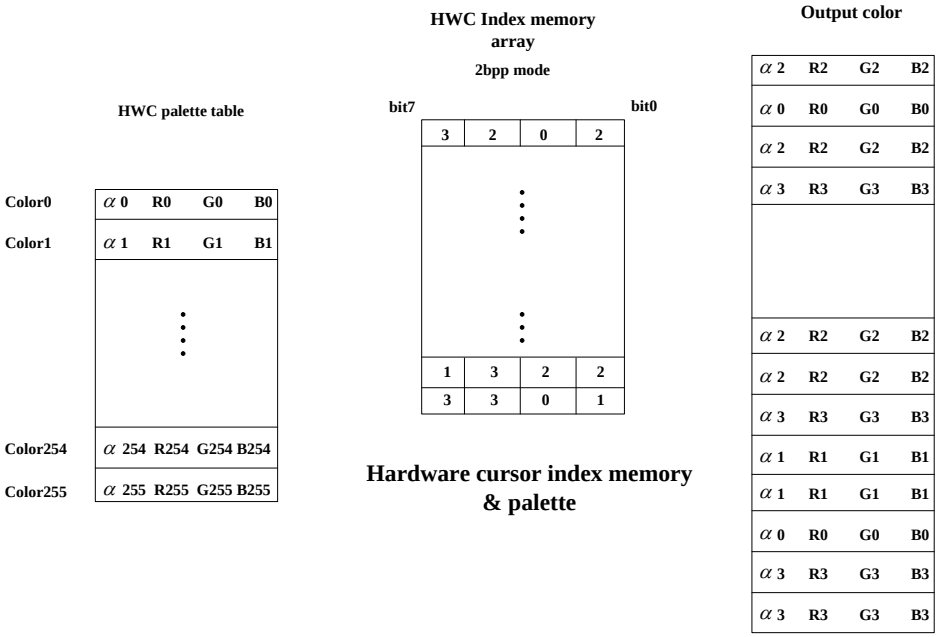
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Offset: 0x4800-0x4BFF			DE-HW cursor pattern memory block
Bit	Read/Write	Default/Hex	Description
31:00	R/W	UDF	Hardware cursor pixel pattern Specify the color displayed for each of the hardware cursor pixels.

27.5.38. DE-HWC Palette Table

Offset: 0x4C00-0x4FFF			DE-HW palette table
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:08	R/W	UDF	Green value
07:00	R/W	UDF	Blue value

The following figure (only with 2bpp mode) shows the RAM array used for hardware cursor palette lookup and the corresponding colors output.



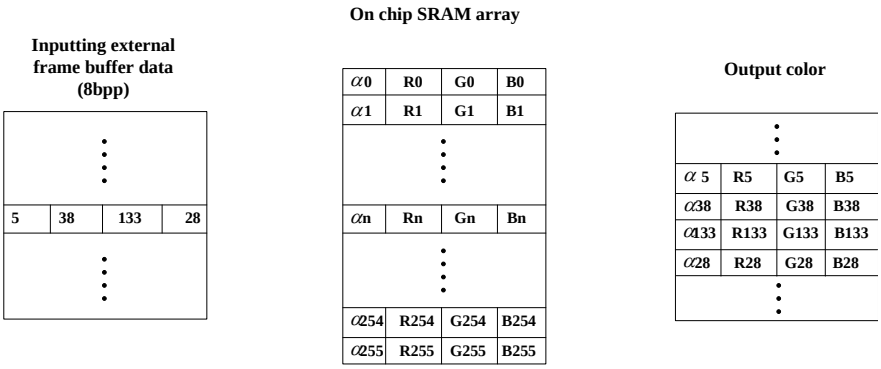
Hardware cursor index memory & palette

27.5.39. Palette Mode

Offset: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			Pipe palette color table SRAM block
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:08	R/W	UDF	Green value
07:00	R/W	UDF	Blue value

In this mode, RAM array is used for palette lookup table; each pixel in the layer frame buffer is treated as an index into the RAM array to select the actual color.

The following figure shows the RAM array used for palette lookup and the corresponding colors output.



27.5.40. Internal Frame Buffer Mode

In internal frame buffer mode, the RAM array is used as an on-chip frame buffer; each pixel in the RAM array is used to select one of the palette 32-bit colors.

1bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P31	P30	P29	P28	P27	P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P01	P00
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

2bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P15	P14	P13	P12	P11	P10	P09	P08
P07	P06	P05	P04	P03	P02	P01	P00
15 14	13 12	11 10	09 08	07 06	05 04	03 02	01 00

4bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P07	P06	P05	P04
P03	P02	P01	P00
15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00

8bpp:

Bit

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

P3	P2
P1	P0
15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00

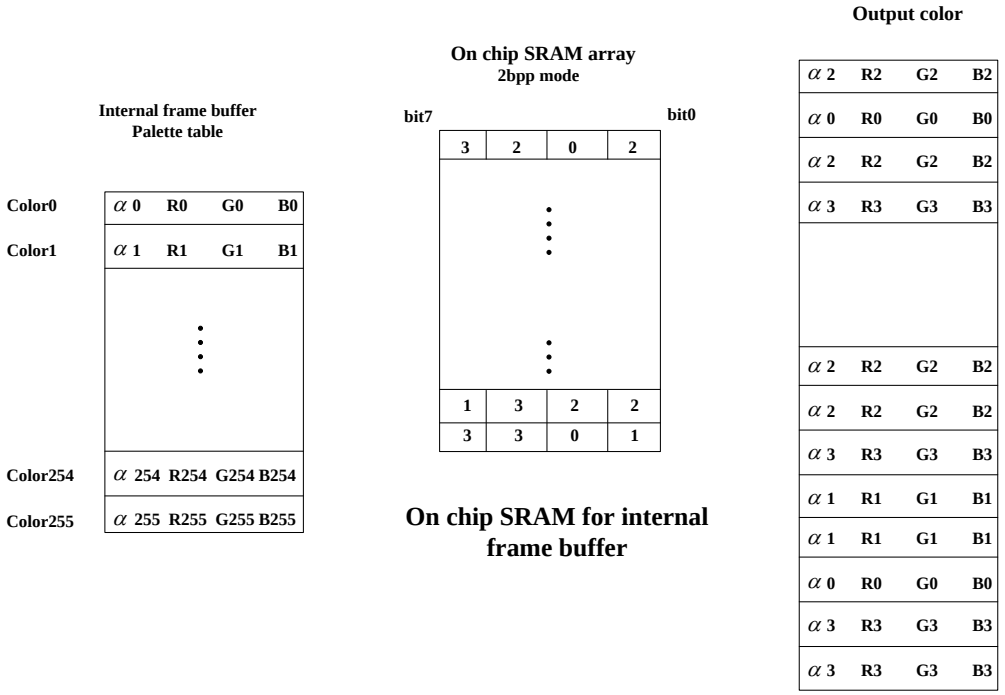
Offset: 0x4000-0x57FF			DE-on chip SRAM block
Bit	Read/Write	Default/Hex	Description
31:00	R/W	UDF	Internal frame buffer pixel pattern Specify the color displayed for each of the internal frame buffer pixels.

27.5.41. Internal Frame Buffer Mode Palette Table

Address: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			Pipe palette table
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha value

23:16	R/W	UDF	Red value
15:08	R/W	UDF	Green value
07:00	R/W	UDF	Blue value

The following figure shows the RAM array used for internal frame buffer mode and the corresponding colors output.



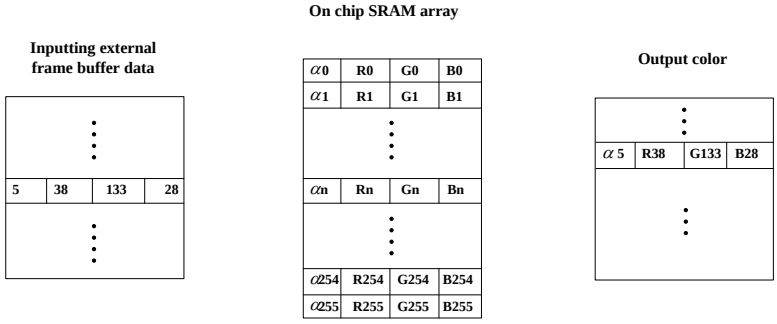
27.5.42. Gamma Correction Mode

Offset: 0x4400-0x47FF			DE-on chip SRAM block
Bit	Read/Write	Default/Hex	Description
31:24	R/W	UDF	Alpha channel intensity
23:16	R/W	UDF	Red channel intensity
15:08	R/W	UDF	Green channel intensity
07:00	R/W	UDF	Blue channel intensity

In gamma correction mode, the RAM array is used for gamma correction; each pixel's alpha, red, green, and blue color component is treated as an index into the SRAM array. The corresponding

Alpha, red, green, or blue channel intensity value at that index is used in the actual color.

The following figure shows the RAM array used for gamma correction and the corresponding colors output.



On chip SRAM for gamma correction

27.6. Display Engine Memory Mapping

Base Address:
BE0: 0x01e60000

Offset:	
0x0000 0x07FF	**Reserved**
0x0800 0x0DFF	**Registers**
0x0E00 0x3FFF	**Reserved**
0x4000 0x43FF	**Reserved**
0x4400 0x47FF	**Gamma Table**
0x4800 0x4BFF	**HWC Memory Block**
0x4C00 0x4FFF	**HWC Palette Table**
0x5000 0x53FF	**PIPE0 Palette Table**
0x5400 0x57FF	**PIPE1 Palette Table**
0x5800 0xFFFF	**Reserved**

Chapter 28 TCON

28.1. TCON Block Diagram

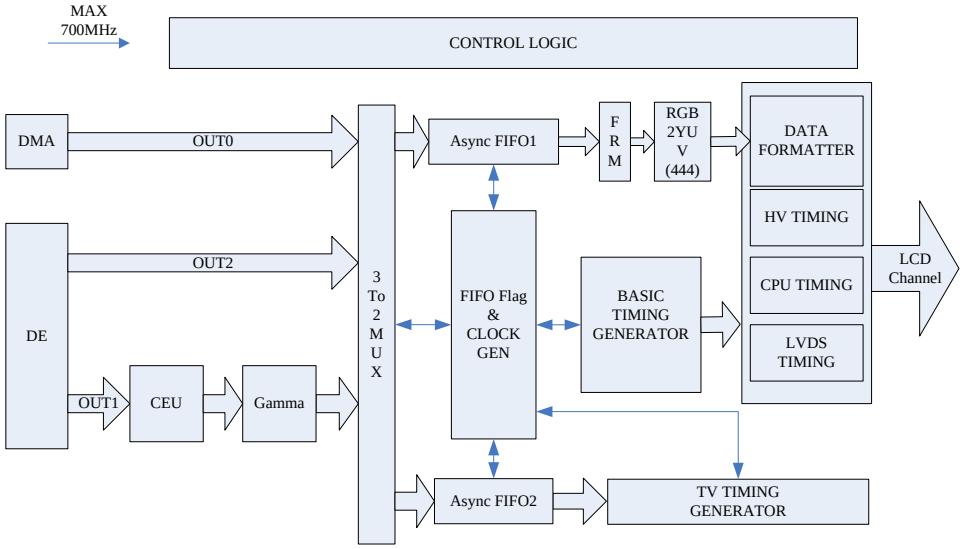


Figure 28-1. LCD/TV Timing Controller Block Diagram

28.2. TCON Register List

Module Name	Base Address
TCON	0x01C0C000

Register Name	Offset	Description
TCON_GCTL_REG	0x0000	TCON Global Control Register
TCON_GINT0_REG	0x0004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x0008	TCON Global Interrupt Register1
TCON0_FRM_CTL_REG	0x0010	TCON FRM Control Register
TCON0_FRM_SEED0_REG	0x0014	TCON FRM Seed Register0
TCON0_FRM_SEED1_REG	0x0018	TCON FRM Seed Register1
TCON0_FRM_SEED2_REG	0x001C	TCON FRM Seed Register2
TCON0_FRM_SEED3_REG	0x0020	TCON FRM Seed Register3
TCON0_FRM_SEED4_REG	0x0024	TCON FRM Seed Register4
TCON0_FRM_SEED5_REG	0x0028	TCON FRM Seed Register5
TCON0_FRM_TAB0_REG	0x002C	TCON FRM Table Register0
TCON0_FRM_TAB1_REG	0x0030	TCON FRM Table Register1
TCON0_FRM_TAB2_REG	0x0034	TCON FRM Table Register2
TCON0_FRM_TAB3_REG	0x0038	TCON FRM Table Register3
TCON0_CTL_REG	0x0040	TCON0 Control Register
TCON0_DCLK_REG	0x0044	TCON0 Data Clock Register

TCON0_BASIC0_REG	0x0048	TCON0 Basic Timing Register0
TCON0_BASIC1_REG	0x004C	TCON0 Basic Timing Register1
TCON0_BASIC2_REG	0x0050	TCON0 Basic Timing Register2
TCON0_BASIC3_REG	0x0054	TCON0 Basic Timing Register3
TCON0_HV_IF_REG	0x0058	TCON0 Hv Panel Interface Register
TCON0_CPU_IF_REG	0x0060	TCON0 CPU Panel Interface Register
TCON0_CPU_WR_REG	0x0064	TCON0 CPU Panel Write Data Register
TCON0_CPU_RD0_REG	0x0068	TCON0 CPU Panel Read Data Register0
TCON0_CPU_RD1_REG	0x006C	TCON0 CPU Panel Read Data Register1
TCON0_IO_POL_REG	0x0088	TCON0 IO Polarity Register
TCON0_IO_TRI_REG	0x008C	TCON0 IO Control Register
TCON1_CTL_REG	0x0090	TCON1 Control Register
TCON1_BASIC0_REG	0x0094	TCON1 Basic Timing Register0
TCON1_BASIC1_REG	0x0098	TCON1 Basic Timing Register1
TCON1_BASIC2_REG	0x009C	TCON1 Basic Timing Register2
TCON1_BASIC3_REG	0x00A0	TCON1 Basic Timing Register3
TCON1_BASIC4_REG	0x00A4	TCON1 Basic Timing Register4
TCON1_BASIC5_REG	0x00A8	TCON1 Basic Timing Register5
TCON1_IO_POL_REG	0x00F0	TCON1 IO Polarity Register
TCON1_IO_TRI_REG	0x00F4	TCON1 IO Control Register
TCON_CEU_CTL_REG	0x0100	TCON CEU Control Register
TCON_CEU_COEF0_REG	0x0110	TCON CEU Coefficient Register0
TCON_CEU_COEF1_REG	0x0114	TCON CEU Coefficient Register1
TCON_CEU_COEF2_REG	0x0118	TCON CEU Coefficient Register2
TCON_CEU_COEF3_REG	0x011C	TCON CEU Coefficient Register3
TCON_CEU_COEF4_REG	0x0120	TCON CEU Coefficient Register4
TCON_CEU_COEF5_REG	0x0124	TCON CEU Coefficient Register5
TCON_CEU_COEF6_REG	0x0128	TCON CEU Coefficient Register6
TCON_CEU_COEF7_REG	0x012C	TCON CEU Coefficient Register7
TCON_CEU_COEF8_REG	0x0130	TCON CEU Coefficient Register8
TCON_CEU_COEF9_REG	0x0134	TCON CEU Coefficient Register9
TCON_CEU_COEF10_REG	0x0138	TCON CEU Coefficient Register10
TCON_CEU_COEF11_REG	0x013C	TCON CEU Coefficient Register11
TCON_CEU_COEF12_REG	0x0140	TCON CEU Coefficient Register12
TCON_CEU_COEF13_REG	0x0144	TCON CEU Coefficient Register13
TCON_CEU_COEF14_REG	0x0148	TCON CEU Coefficient Register14
TCON1_ FILL_CTL_REG	0x0300	TCON1 Fill Data Control Register
TCON1_ FILL_BEGIN0_REG	0x0304	TCON1 Fill Data Begin Register0
TCON1_ FILL_END0_REG	0x0308	TCON1 Fill Data End Register0
TCON1_ FILL_DATA0_REG	0x030C	TCON1 Fill Data Value Register0
TCON1_ FILL_BEGIN1_REG	0x0310	TCON1 Fill Data Begin Register1
TCON1_ FILL_END1_REG	0x0314	TCON1 Fill Data End Register1
TCON1_ FILL_DATA1_REG	0x0318	TCON1 Fill Data Value Register1
TCON1_ FILL_BEGIN2_REG	0x031C	TCON1 Fill Data Begin Register2
TCON1_ FILL_END2_REG	0x0320	TCON1 Fill Data End Register2
TCON1_ FILL_DATA2_REG	0x0324	TCON1 Fill Data Value Register2
TCON1_GAMMA_TABLE_REG	0x400-0x7FF	TCON1 Gama Table Register

28.3. TCON Register Description

28.3.1. TCON_GCTL_REG(Default: 0x00000000)

Offset: 0x000			Register Name: TCON global control register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON_En 0: disable 1: enable When it's disabled, the module will be reset to idle state.
30	R/W	0	TCON_Gamma_En 0: disable 1: enable
29:1	/	/	/
0	R/W	0	IO_Map_Sel 0: TCON0 1: TCON1 Note: This bit determines which IO_INV/IO_TRI is valid

28.3.2. TCON_GINT0_REG(Default: 0x00000000)

Offset: 0x004			Register Name: TCON global interrupt register0
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON0_Vb_Int_En 0: disable 1: enable
30	R/W	0	TCON1_Vb_Int_En 0: disable 1: enable
29	R/W	0	TCON0_Line_Int_En 0: disable 1: enable
28	R/W	0	TCON1_Line_Int_En 0: disable 1: enable
27:16	/	/	/
15	R/W	0	TCON0_Vb_Int_Flag Asserted during vertical no-display period every frame. Write 0 to clear it.
14	R/W	0	TCON1_Vb_Int_Flag Asserted during vertical no-display period every frame. Write 0 to clear it.
13	R/W	0	TCON0_Line_Int_Flag trigger when SY0 matches the current TCON0 scan line Write 0 to clear it.
12	R/W	0	TCON1_Line_Int_Flag trigger when SY1 matches the current TCON1 scan line Write 0 to clear it.
11:0	/	/	/

28.3.3. TCON_GINT1_REG(Default: 0x00000000)

Offset: 0x008			Register Name: TCON global interrupt register1
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	TCON0_Line_Int_Num scan line for TCON0 line trigger(including inactive lines)

			Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 is disabled.
15:11	/	/	/
10:0	R/W	0	TCON1_Line_Int_Num scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 is disabled.

28.3.4. TCON0_FRM_CTL_REG(Default: 0x00000000)

Offset: 0x010			Register Name: TCON FRM control register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON0_Frm_En 0:disable 1:enable
30:12	/	/	/
6	R/W	0	TCON0_Frm_Mode_R 0: 6bit frm output 1: 5bit frm output
5	R/W	0	TCON0_Frm_Mode_G 0: 6bit frm output 1: 5bit frm output
4	R/W	0	TCON0_Frm_Mode_B 0: 6bit frm output 1: 5bit frm output
1:0	R/W	0	TCON0_Frm_Test 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM 11: half 8bit, half 5/6bit

28.3.5. TCON0_FRM_PIXEL_SEED_REG(Default: 0x00000000)

Offset: 0x014-0x01C			Register Name: TCON FRM pixel seed register
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24:0	R/W	0	Pixel_Seed_Value Note: avoid set it to 0

28.3.6. TCON0_FRM_LINE_SEED_REG(Default: 0x00000000)

Offset: 0x020-0x028			Register Name: TCON FRM line seed register
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
12:0	R/W	0	Line_Seed_Value Note: avoid set it to 0

28.3.7. TCON0_FRM_TAB_REG(Default: 0x00000000)

Offset: 0x02C-0x038			Register Name: TCON FRM table register
Bit	Read/Write	Default/Hex	Description
127:0	R/W	0	Frm_Table_Value

28.3.8. TCON0_CTL_REG(Default: 0x00000000)

Offset: 0x040			Register Name: TCON0 control register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON0_En 0: disable 1: enable Note: It executes at the beginning of the first blank line of TCON0 timing.
30:26	/	/	/
25:24	R/W	0	TCON0_IF 00: HV(Sync+DE) 01: 8080 I/F 10: TTL I/F 11: reserved
23	R/W	0	TCON0_RG_Swap 0: default 1: swap RED and BLUE data at FIFO1
22	R/W	0	TCON0_Test_Value 0:all 0s 1:all 1s
21	R/W	0	TCON0_FIFO1_Rst Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must be more than 1 DCLK
20	R/W	0	TCON0_Interlace_En 0:disable 1:enable NOTE: this flag is valid only when TCON0_EN == 1
19:9	/	/	/
8:4	R/W	0	TCON0_State_Delay STA delay NOTE: valid only when TCON0_EN == 1
3:2	/	/	/
1:0	R/W	0	TCON0_SRC_SEL: 00: DE CH1(FIFO1 enable) 01: DE CH2(FIFO1 enable) 10: DMA 565 input(FIFO1 enable) 11: Test intput(FIFO1 disable) Note: These bits are sampled only at the beginning of the first blank line of TCON0 timing. Generally, when input source changes, it will change at the beginning of the first blank line of TCON0 timing. When FIFO1 and FIFO2 select the same source and FIFO2 is enabled, it executes at the beginning of the first blank line of TV timing. Also, TCON0 timing generator will reset to the beginning of the first blank line.

28.3.9. TCON0_DCLK REG(Default: 0x00000000)

Offset: 0x044			Register Name: TCON0 data clock register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON0_Dclk_En
30:6	/	/	/
6:0	R/W	0	TCON0_Dclk_Div Tdclk = Tsclk * DCLKDIV Note: 1.if dclk1&dclk2 used， DCLKDIV >=6

			2.if dclk only， DCLKDIV >=4

28.3.10. TCON0_BASIC0_REG(Default: 0x00000000)

Offset: 0x048			Register Name: TCON0 basic timing register0
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
26:16	R/W	0	TCON0_X Panel width is X+1
15:11	/	/	/
10:0	R/W	0	TCON0_Y Panel height is Y+1

28.3.11. TCON0_BASIC1_REG(Default: 0x00000000)

Offset: 0x04C			Register Name: TCON0 basic timing register1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	HT Thcycle = (HT+1) * Tdclk Note:1) parallel :HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:10	/	/	/

28.3.12. TCON0_BASIC2_REG(Default: 0x00000000)

Offset: 0x050			Register Name: TCON0 basic timing register2
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
27:16	R/W	0	VT TVT = (VT)/2 * Thsync Note: VT/2 >= (VBP+1) + (Y+1) +2
15:10	/	/	/
9:0	R/W	0	VBP Tvbp = (VBP +1) * Thsync

28.3.13. TCON0_BASIC3_REG(Default: 0x00000000)

Offset: 0x054			Register Name: TCON0 basic timing register3
Bit	Read/Write	Default/Hex	Description
31:22	/	/	/
25:16	R/W	0	HSPW Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	VSPW Tvspw = (VSPW+1) * Thsync Note: VT/2 > (VSPW+1)

28.3.14. TCON0_HV_IF_REG(Default: 0x00000000)

Offset: 0x058			Register Name: TCON0 hv panel interface register
Bit	Read/Write	Default/Hex	Description

31	R/W	0	HV_Mode 0: 24bit parallel mode 1: 8bit serial mode
30	R/W	0	Serial_Mode 0: 8bit/3cycle RGB serial mode(RGB888) 1: 8bit/2cycle YUV serial mode(CCIR656)
29:28	/	/	/
27:26	R/W	0	RGB888_SM0 Serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
25:24	R/W	0	RGB888_SM1 Serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8…) 00: R→G→B 01: B→R→G 10: G→B→R 11: R→G→B
23:22	R/W	0	YUV_SM serial YUV mode Output sequence 2-pixel-pair of every scan line 00: YUYV 01: YVYU 10: UYVY 11: VYUY
21:20	R/W	0	YUV EAV/SAV F line delay 0:F toggle right after active video line 1:delay 2 line(CCIR NTSC) 2:delay 3 line(CCIR PAL) 3:reserved
19：0	/	/	/

28.3.15. TCON0_CPU_IF_REG(Default: 0x00000000)

Offset: 0x060			Register Name: TCON0 cpu panel interface register
Bit	Read/Write	Default/Hex	Description
31:29	R/W	0	CPU_MOD 000: 18bit/256K mode 001: 16bit mode0 010: 16bit mode1 011: 16bit mode2 100: 16bit mode3 101: 9bit mode 110: 8bit 256K mode 111: 8bit 65K mode
28	R/W	0	AUTO auto Transfer Mode: If it's 1, all valid data during this frame is written to panel. Note: This bit is sampled by Vsync
27	R/W	0	FLUSH direct transfer mode: If it's enabled, FIFO1 is irrelevant to the HV timing, and pixels data keeps being transferred unless the input FIFO is empty.

			Data output rate control by DCLK.
26	R/W	0	DA pin A1 value in 8080 mode auto/flash states
25	R/W	0	CA pin A1 value in 8080 mode WR/RD execute
24	R/W	0	VSYNC_Cs_Sel 0:CS 1:VSYNC
23	R	0	Wr_Flag 0:write operation ends 1:write operation is pending
22	R	0	Rd_Flag 0:read operation ends 1:read operation is pending
21:0	/	/	/

28.3.16. TCON0_CPU_WR_REG(Default: 0x00000000)

Offset: 0x064			Register Name: TCON0 cpu panel write data register
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/
23:0	W	0	Data_Wr data write on 8080 bus, launch a write operation on 8080 bus

28.3.17. TCON0_CPU_RD0_REG(Default: 0x00000000)

Offset: 0x068			Register Name: TCON0 cpu panel read data register0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	/	Data_Rd0 data read on 8080 bus, launch a new read operation on 8080 bus

28.3.18. TCON0_CPU_RD1_REG(Default: 0x00000000)

Offset: 0x06C			Register Name: TCON0 cpu panel read data register1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R	/	Data_Rd1 data read on 8080 bus, without a new read operation on 8080 bus

28.3.19. TCON0_IO_POL_REG(Default: 0x00000000)

Offset: 0x088			Register Name: TCON0 IO polarity register
Bit	Read/Write	Default/Hex	Description
31:30	/	/	/
29:28	R/W	0	DCLK_Sel 00: used DCLK0(normal phase offset) 01: used DCLK1(1/3 phase offset) 10: used DCLK2(2/3 phase offset) 11: reserved
27	R/W	0	IO3_Inv 0: not invert 1: invert
26	R/W	0	IO2_ Inv 0: not invert

			1: invert
25	R/W	0	IO1_Inv 0: not invert 1: invert
24	R/W	0	IO0_Inv 0: not invert 1: invert
23:0	R/W	0	Data_Inv TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

28.3.20. TCON0_IO_TRI_REG(Default: 0x0FFFFFFF)

Offset: 0x08C			Register Name: TCON0 IO control register
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	1	IO3_Output_Tri_En 1: disable 0: enable
26	R/W	1	IO2_Output_Tri_En 1: disable 0: enable
25	R/W	1	IO1_Output_Tri_En 1: disable 0: enable
24	R/W	1	IO0_Output_Tri_En 1: disable 0: enable
23:0	R/W	0xFFFFFF	Data_Output_Tri_En TCON0 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

28.3.21. TCON1_CTL_REG(Default: 0x00000000)

Offset: 0x090			Register Name: TCON1 control register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON1_En 0: disable 1: enable
30:21	/	/	/
20	R/W	0	Interlace_En 0:disable 1:enable
19:9	/	/	/
8:4	R/W	0	Start_Delay This is for DE1 and DE2

28.3.22. TCON1_BASIC0_REG(Default: 0x00000000)

Offset: 0x094			Register Name: TCON1 basic timing register0
Bit	Read/Write	Default/Hex	Description

31:27	/	/	/
27:16	R/W	0	TCON1_XI source width is X+1
15:12	/	/	/
11:0	R/W	0	TCON1_YI source height is Y+1

28.3.23. TCON1_BASIC1_REG(Default: 0x00000000)

Offset: 0x098			Register Name: TCON1 basic timing register1
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
27:16	R/W	0	LS_XO width is LS_XO+1
15:12	/	/	/
11:0	R/W	0	LS_YO width is LS_YO+1 Note: this version LS_YO = TCON1_YI

28.3.24. TCON1_BASIC2_REG(Default: 0x00000000)

Offset: 0x09C			Register Name: TCON1 basic timing register2
Bit	Read/Write	Default/Hex	Description
31:27	/	/	/
27:16	R/W	0	TCON1_XO width is TCON1_XO+1
15:12	/	/	/
11:0	R/W	0	TCON1_YO height is TCON1_YO+1

28.3.25. TCON1_BASIC3_REG(Default: 0x00000000)

Offset: 0x0A0			Register Name: TCON1 basic timing register3
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
28:16	R/W	0	HT horizontal total time Thcycle = (HT+1) * Thdclk
15:12	/	/	/
11:0	R/W	0	HBP horizontal back porch Thbp = (HBP +1) * Thdclk

28.3.26. TCON1_BASIC4_REG(Default: 0x00000000)

Offset: 0x0A4			Register Name: TCON1 basic timing register4
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
28:16	R/W	0	VT horizontal total time (in HD line) Tvt = VT/2 * Th
15:12	/	/	/
11:0	R/W	0	VBP horizontal back porch (in HD line)

			Tvbp = (VBP +1) * Th

28.3.27. TCON1_BASIC5_REG(Default: 0x00000000)

Offset: 0x0A8			Register Name: TCON1 basic timing register5
Bit	Read/Write	Default/Hex	Description
31:26	/	/	/
25:16	R/W	0	HSPW horizontal Sync Pulse Width (in dclk) Thspw = (HSPW+1) * Tdclk Note: HT> (HSPW+1)
15:10	/	/	/
9:0	R/W	0	VSPW vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Th Note: VT/2 > (VSPW+1)

28.3.28. TCON1_IO_POL_REG(Default: 0x00000000)

Offset: 0x0F0			Register Name: TCON1 IO polarity register
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	0	IO3_Inv 0: not invert 1: invert
26	R/W	0	IO2 Inv 0: not invert 1: invert
25	R/W	0	IO1_Inv 0: not invert 1: invert
24	R/W	0	IO0_Inv 0: not invert 1: invert
23:0	R/W	0	Data_Inv:TCON1 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

28.3.29. TCON1_IO_TRI_REG(Default: 0x0FFFFFFF)

Offset: 0x0F4			Register Name: TCON1 IO control register
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27	R/W	1	IO3_Output_Tri_En 1: disable 0: enable
26	R/W	1	IO2_Output_Tri_En 1: disable 0: enable
25	R/W	1	IO1_Output_Tri_En 1: disable 0: enable
24	R/W	1	IO0_Output_Tri_En 1: disable

			0: enable
27:0	R/W	0xFFFFFF	Data_Output_Tri_En TCON1 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

28.3.30. TCON_CEU_CTL_REG(Default: 0x00000000)

Offset: 0x100			Register Name: TCON CEU control register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	CEU_en 0: bypass 1: enable
30:0	/	/	/

28.3.31. TCON_CEU_MUL_COEF_REG(Default: 0x00000000)

Offset: 0x110-118, 0x120-0x128, 0x130-0x138			Register Name: TCON CEU multiplier coefficient register
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:0	R/W	0	CEU_Coef_Mul_Value signed 13bit value, range of (-16,16)

28.3.32. TCON_CEU_ADD_COEF_REG(Default: 0x00000000)

Offset: x11C,0x12C,0x13C			Register Name: TCON CEU add coefficient register
Bit	Read/Write	Default/Hex	Description
31:19	/	/	/
18:0	R/W	0	CEU_Coef_Add_Value signed 19bit value, range of (-16384, 16384)

28.3.33. TCON_CEU_RANGE_COEF_REG(Default: 0x00000000)

Offset: 0x140,0x144,0x148			Register Name: TCON CEU range coefficient register
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	CEU_Coef _Range_Min unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0	CEU Coef _Range_Max unsigned 8bit value, range of [0,255]

28.3.34. TCON1_FILL_CTL_REG(Default: 0x00000000)

Offset: 0x300			Register Name: TCON1 fill data control register
Bit	Read/Write	Default/Hex	Description
31	R/W	0	TCON1_Fill_En: 0: bypass 1: enable
30:0	/	/	/

28.3.35. TCON1_FILL_BEGIN_REG(Default: 0x00000000)

Offset: 0x304,0x310,0x31C			Register Name: TCON1 fill data begin register
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	Fill_Begin

28.3.36. TCON1_FILL_END_REG(Default: 0x00000000)

Offset: 0x308,0x314,0x320			Register Name: TCON1 fill data end register
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	Fill_End

28.3.37. TCON1_FILL_DATA_REG(Default: 0x00000000)

Offset: 0x30C,0x318,0x324			Register Name: TCON1 fill data value register
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:0	R/W	0	Fill_Value

Chapter 29 IEP

29.1. Overview

The Image Enhancement Processor (IEP) is capable of adjusting the dynamic range of pictures according to statistics.

29.2. IEP Register Description

29.2.1. General Control Register(Default: 0x00000000)

Offset: 0X0000			Register Name: IMGEHC_GNECTL_REG
Bit	Read/Write	Default/Hex	Description
31	R/W	0	BIST_EN BIST enable 0: disable 1: enable
30:10	/	/	/
09:08	R/W	0	MOD Work mode selection. If bit 0 of the register is set ZERO, the following setting will be ignored. 00: Output FIFO mode 01: De-flicker mode 10: DRC mode 11: Reserved
07:01	/	/	/
00	R/W	0	EN 0: disabled the module, and the whole module will be by passed 1: enable

29.2.2. DRC Size Setting Register(Default: 0x00000000)

Offset: 0X0004			Register Name: IMGEHC_DRCSIZE_REG
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	DRC_HEIGHT Display height The real display height = The value of these bits + 1.
15:12	/	/	/
11:00	R/W	0	DRC_WIDTH Display width The real display width = The value of these bits + 1.

29.2.3. DRC Control Register(Default: 0x00000000)

Offset: 0X0010			Register Name: IMGEHC_DRCCTL_REG
Bit	Read/Write	Default/Hex	Description
31:09	/	/	/
08	R/W	0	DRC_WIN_EN Output window function enable 0: disable

			1: enable
07:02	/	/	/
01	R/W	0	DRC_DBRDY_CTL Only valid when DRC_DB_EN bit is set. If the bit is set, when the SYNC signal is coming, the all double buffered DRC registers will be loaded, and the loading is done, the bit will be cleared automatically
00	R/W	0	DRC_DB_EN DRC double buffer function enable control 0: disable 1: enable

(LGC = Luminance Gain Coefficient)

29.2.4. DRC External LGC Start Address Register(Default: 0x00000000)

Offset: 0X0014			Register Name: IMGEHC_DRCLGC_STAADD_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	DRC_LGC_STAADD Start address in byte

Double buffered register of DRC, double buffer function is controlled by DRC_DB_EN and DRC_DBRDY_CTL bits.

29.2.5. DRC Setting Register(Default: 0x00008000)

Offset: 0X0018			Register Name: IMGEHC_DRC_SET_REG
Bit	Read/Write	Default/Hex	Description
31:25	/	/	/
24	R/W	0	DRC_GAIN_AUTOLOAD_DIS Only valid when the module is enabled and MOD is DRC mode, or the bit is ignored. If the auto load function is enabled, the DRC luminance gain coefficient will be auto loaded from the external appointed memory address when the SYNC signal (LCD SYNC signal) is coming, otherwise ignore the auto load function. About the calculating way of the external appointed memory address, refer to the DRC external LGC start address register. 0: Enable the auto load function 1: Disable the auto load function
23:16	/	/	/
15:08	R/W	0x80	DRC_LGC_ABSLUMPERVAL Abs luminance percent value
07:02	/	/	/
01	R/W	0x00	DRC_ADJUST_EN 0: disable 1: enable
00	R/W	0x00	DRC_LGC_ABSLUMSHF Abs luminance shift bits 0: shift 8bits 1: shift 9bits

Note: Double buffered register of DRC, double buffer function is controlled by DRC_DB_EN and DRC_DBRDY_CTL bits.

29.2.6. DRC Window Position Register0(Default: 0x00000000)

Offset: 0X001C	Register Name: IMGEHC_DRC_WP_REG0

Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	DRC_WIN_TOP Window Top position Top position is the left-top y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0	DRC_WIN_LEFT Window Left position Left position is left-top x coordinate of display window in pixels

29.2.7. DRC Window Position Register1(Default: 0x00000000)

Offset: 0X0020			Register Name: IMGEHC_DRC_WP_REG1
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:16	R/W	0	DRC_WIN_BOT Window Bottom position Bottom position is the right-bottom y coordinate of display window in pixels
15:12	/	/	/
11:00	R/W	0	DRC_WIN_RIGHT Window Right position Right position is the right-bottom x coordinate of display window in pixels

29.2.8. DRC Write Back Control Register(Default: 0x00000000)

Offset: 0X0024			Register Name: IMGEHC_WBCTL_REG0
Bit	Read/Write	Default/Hex	Description
31	R/W	0x0	WB_STATUS Write back process status 0: write back end or write back disable 1: write back in process
30:25	/	/	/
24	R/W	0x0	WB_FIELD Write back field setting for de-flicker 0: top field 1: bottom field
23:17	/	/	/
16	R/W	0x0	WB_FMT Write back data format setting 0: ARGB 1: BGRA
15:09	/	/	/
08	R/W	0x0	WB_WOC Write back only control 0: disable the write back only control, the data will transfer to LCD controller too. 1: enable the write back only control, the data won't transfer to LCD controller.
07:02	/	/	/
00	R/W	0x0	WB_EN Write back enable 0: disable 1: enable

			The bit will be cleared when write back ends.

29.2.9. DRC Write Back Address Register(Default: 0x00000000)

Offset: 0X0028			Register Name: IMGEHC_WBADD_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	WB_ADD The start address of write back data in BYTE

29.2.10. DRC Write Back Buffer Line Width Register(Default: 0x00000000)

Offset: 0X002c			Register Name: IMGEHC_WBLINEWIDTH_REG
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	WB_LINEWIDTH Write back image buffer line width in BYTE

29.2.11. Luminance Histogram Control Register(Default: 0x00000000)

Offset: 0X0030			Register Name: IMGEHC_LHC_REG
Bit	Read/Write	Default/Hex	Description
31:2	/	/	/
1	R/W	0	LH_MOD 0: Current frame case 1: Average case
0	R/W	0	LH_REC_CLR If the bit is set, all of the luminance statistics recording registers will be cleared, and the bit will self-clear when the recording registers is cleared.

29.2.12. Luminance Histogram Threshold Setting Register 0(Default: 0x80604020)

Offset: 0X0034			Register Name: IMGEHC_LHT_REG0
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0x80	LH_THRES_VAL4 Step4 threshold value
23:16	R/W	0x60	LH_THRES_VAL3 Step3 threshold value
15:08	R/W	0x40	LH_THRES_VAL2 Step2 threshold value
07:00	R/W	0x20	LH_THRES_VAL1 Step1 threshold value

29.2.13. Luminance Histogram Threshold Setting Register 1(Default: 0x00E0C0A0)

Offset: 0X0038			Register Name: IMGEHC_LHT_REG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0xe0	LH_THRES_VAL7 Step7 threshold value
15:08	R/W	0xc0	LH_THRES_VAL6 Step6 threshold value
07:00	R/W	0xa0	LH_THRES_VAL5 Step5 threshold value

When set IMGEHC_LHT_REG0 and IMGEHC_LHT_REG1, make sure that THRES_VAL1<THRES_VAL2<…<THRES_VAL7.

29.2.14. Luminance Histogram Statistics Lum Recording Register(Default: 0x00000000)

Offset: 0X0040 ~ 0X005C			Register Name: IMGEHC_LHSLUM_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	LH_LUM_DATA Luminance statistics data

29.2.15. Luminance Histogram Statistics Counter Recording Register(Default: 0x00000000)

Offset: 0X0060 ~ 0X007C			Register Name: IMGEHC_LHSCNT_REG
Bit	Read/Write	Default/Hex	Description
31:00	R/W	0	LH_CNT_DATA Luminance statistics data

YUV to RGB conversion algorithm formula:

R =
(R Y component coefficient * Y) +
(R U component coefficient * U) +
(R V component coefficient * V) +
R constant
G =
(G Y component coefficient * Y) +
(G U component coefficient * U) +
(G V component coefficient * V) +
G constant
B =
(B Y component coefficient * Y) +
(B U component coefficient * U) +
(B V component coefficient * V) +
B constant

29.2.16. CSC Y/G Coefficient Register

Offset: G/Y component: 0X00C0 R/U component: 0X00C4 B/V component: 0X00C8			Register Name: IMGEHC_CSCYGCOFF_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:00	R/W	0x4a7 0x1e6f 0x1cbf	CSC_YG_COFF the Y/G coefficient the value equals to coefficient*2^{10}

29.2.17. CSC Y/G Constant Register(Default: 0x00000877)

Offset: 0X00CC			Register Name: IMGEHC_CSCYGCON_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x877	CSC_YG_CON

			the Y/G constant the value equals to coefficient*2^4

29.2.18. CSC U/R Coefficient Register

Offset: G/Y component: 0X00D0 R/U component: 0X00D4 B/V component: 0X00D8			Register Name: IMGEHC_CSCURCOFF_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:00	R/W	0x4a7 0x00 0x662	CSC_UR_COFF the U/R coefficient the value equals to coefficient*2^{10}

29.2.19. CSC U/R Constant Register(Default: 0x00003211)

Offset: 0X00DC			Register Name: IMGEHC_CSCURCON_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x3211	CSC_UR_CON the U/R constant the value equals to coefficient*2^4

29.2.20. CSC V/B Coefficient Register

Offset: G/Y component: 0X00E0 R/U component: 0X00E4 B/V component: 0X00E8			Register Name: IMGEHC_CSCVBCOFF_REG
Bit	Read/Write	Default/Hex	Description
31:13	/	/	/
12:00	R/W	0x4a7 0x812 0x00	CSC_VB_COFF the V/B coefficient the value equals to coefficient*210

29.2.21. CSC V/B Constant Register(Default: 0x00002EB1)

Offset: 0X00EC			Register Name: IMGEHC_CSCVBCON_REG
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:00	R/W	0x2eb1	CSC_VB_CON the V/B constant the value equals to coefficient*2^4

29.2.22. DRC Spatial Coefficient(Default: 0x00000000)

Offset: 0X00F0 ~ 0X00F8			Register Name: IMGEHC_DRCSPACOFF
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23:16	R/W	0	8 bits unsigned spatial coefficient data
15:08	R/W	0	8 bits unsigned spatial coefficient data
07:00	R/W	0	8 bits unsigned spatial coefficient data

29.2.23. DRC Intensity Coefficient(Default: 0x00000000)

Offset: 0X0100 ~ 0X01FC			Register Name: IMGEHC_DRCINTCOFF
Bit	Read/Write	Default/Hex	Description
31:24	R/W	0	8 bits unsigned intensity coefficient data
23:16	R/W	0	8 bits unsigned intensity coefficient data
15:08	R/W	0	8 bits unsigned intensity coefficient data
07:00	R/W	0	8 bits unsigned intensity coefficient data

29.2.24. DRC Luminance Gain Coefficient(Default: 0x00000000)

Offset: 0X0200 ~ 0X03FC			Register Name: IMGEHC_DRCLGCOFF
Bit	Read/Write	Default/Hex	Description
31:16	R/W	0	16bits luminance gain coefficient, unsigned data The high 5 bits is the integer part The low 11 bits is the decimal part
15:00	R/W	0	16bits luminance gain coefficient, unsigned data The high 5 bits is the integer part The low 11 bits is the decimal part

Chapter 30 Crypto Engine

30.1. Overview

The Crypto Engine is one encrypt/ decrypt function accelerator suitable for a variety of applications. It supports both encryption and decryption and several modes. Besides, both CPU mode and DMA method are supported for different applications.

It features:

- Support AES, DES, 3DES, SHA-1, MD5
- Support ECB, CBC modes for AES/DES/3DES
- 128-bits, 192-bits and 256-bits key size for AES
- 160-bits hardware PRNG with 192-bits seed
- Support 32-words RX FIFO and 32-words TX FIFO for high speed application
- Support CPU mode and DMA mode

30.2. Crypto Engine Block Diagram

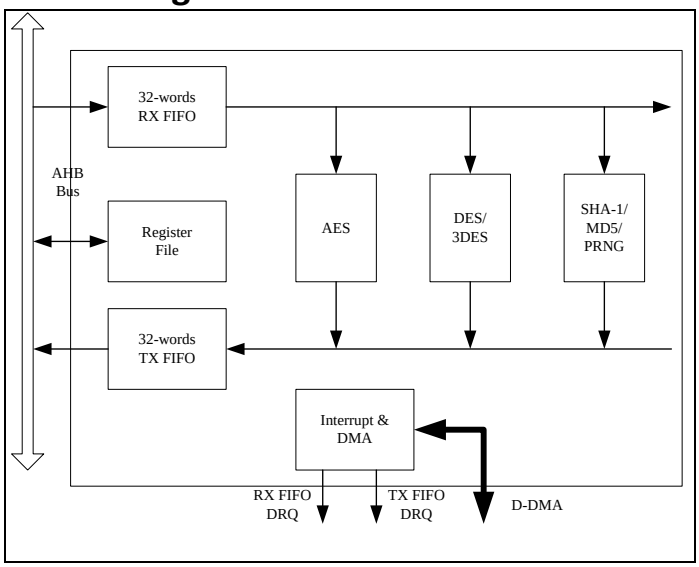


Figure30-1. Crypto Engine Block Diagram

30.3. Crypto Engine Register List

Module Name	Base Address
Crypto Engine	0x01C15000

Register Name	Offset	Description
CE_CTL	0x00	Control Register
CE_KEY0	0x04	Input Key 0/ PRNG Seed 0
CE_KEY1	0x08	Input Key 1/ PRNG Seed 1
…	…	…
CE_KEY7	0x20	Input Key 7

CE_IV0	0x24	Initialization Vector 0
CE_IV1	0x28	Initialization Vector 1
…	…	…
CE_IV7	0x40	Initialization Vector 7
CE_FCSR	0x44	FIFO Control/ Status Register
CE_ICSR	0x48	Interrupt Control/ Status Register
CE_MD0	0x4C	SHA1/MD5 Message Digest 0/PRNG Data0
CE_MD1	0x50	SHA1/MD5 Message Digest 1/PRNG Data1
CE_MD2	0x54	SHA1/MD5 Message Digest 2/PRNG Data2
CE_MD3	0x58	SHA1/MD5 Message Digest 3/PRNG Data3
CE_MD4	0x5C	SHA1/MD5 Message Digest 4/PRNG Data4
CE_RXFIFO	0x200	RX FIFO input port
CE_TXFIFO	0x204	TX FIFO output port

30.4. Crypto Engine Register Description

30.4.1. Crypto Engine Control Register(Default: 0x00000000)

Offset: 0x00			Register Name: CE_CTL
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:24	R/W	0	AES/DES/3DES key select 0: Select input CE_KEYx (Normal Mode) 1: Select SID_RKEYx from Security ID 2: Reserved 3-10: Select internal Key n (n from 0 to 7) Others: Reserved
18:16	R	x	Reserved
15	R/W	0	PRNG generator mode 0: One-shot mode 1: Continue mode
14	R/W	0	IV Steady of SHA-1/MD5 constants 0: Constants 1: Arbitrary IV Notes: It is only used for SHA-1/MD5 engine. If the number of IV word is beyond of 4, Counter 0 register is used for IV4.
13:12	R/W	0	CE Operation Mode 00: Electronic Code Book (ECB) mode 01: Cipher Block Chaining (CBC) mode 10/11: Reserved
11:10	/	/	/
9:8	R/W	0	Key Size for AES 00: 128-bits 01: 192-bits 10: 256-bits 11: Reserved
7	R/W	0	CE Operation Direction 0: Encryption 1: Decryption
6:4	R/W	0	CE Method 000: AES 001: DES 010: Triple DES (3DES) 011: SHA-1 100: MD5

			101: PRNG Others: Reserved
3	/	/	/
2	R/W	0	SHA-1/MD5 Data End bit Write '1' to tell SHA-1/MD5 engine that the text data ends. If there is some data in FIFO, the engine will fetch these data and process them. After finishing message digest, this bit is cleared to '0' by hardware and message digest can be read out from digest registers. Notes: It is only used for SHA-1/MD5 engine.
1	R/W	0	PRNG start bit In PRNG one-shot mode, write '1' to start PRNG. After generating one group random data (5 words), this bit is cleared to '0' by hardware.
0	R/W	0	CE Enable A disable on this bit overrides any other block and flushes all FIFOs. 0: Disable 1: Enable

30.4.2. Crypto Engine Key[n] Register(Default: 0x00000000)

Offset: 0x04 +4*n			Register Name: CE_KEY[n]
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	Key[n] Input Value (n= 0~7)/ PRNG Seed[n] (n= 0~5)

30.4.3. Crypto Engine IV[n] Register(Default: 0x00000000)

Offset: 0x24 +8*n			Register Name: CE_IV[n]
Bit	Read/Write	Default/Hex	Description
31:0	R/W	0	Initialization Vector (IV[n]) Input Value (n= 0~7)

30.4.4. Crypto Engine FIFO Control/ Status Register(Default: 0x60000F0F)

Offset: 0x44			Register Name: CE_FCSR
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30	R	0x1	RX FIFO Empty 0: No room for new word in RX FIFO 1: More than one room for new word in RX FIFO (>= 1 word)
29:24	R	0x20	RX FIFO Empty Space Word Counter
23	/	/	/
22	R	0	TX FIFO Data Available Flag 0: No available data in TX FIFO 1: More than one data in TX FIFO (>= 1 word)
21:16	R	0	TX FIFO Available Word Counter
15:13	/	/	/
12:8	R/W	0xF	RX FIFO Empty Trigger Level Interrupt and DMA request trigger level for RXFIFO normal condition Trigger Level = RXTL + 1 Notes: RX FIFO is used for input the data.
7:5	/	/	/
4:0	R/W	0xF	TX FIFO Trigger Level Interrupt and DMA request trigger level for TXFIFO normal condition Trigger Level = TXTL + 1

			Notes: TX FIFO is used to output the result data.

30.4.5. Crypto Engine Interrupt Control/ Status Register(Default: 0x00000000)

Offset: 0x48			Register Name: CE_ICSR
Bit	Read/Write	Default/Hex	Description
31:11	/	/	/
10	R/W	0	RX FIFO Empty Pending bit 0: No pending 1: RX FIFO Empty pending Notes: Write '1' to clear or automatically clear if interrupt condition fails.
9	/	/	/
8	R/W	0	TX FIFO Data Available Pending bit 0: No TX FIFO pending 1: TX FIFO pending Notes: Write '1' to clear or automatically clear if interrupt condition fails.
7:5	/	/	/
4	R/W	0	DRQ Enable 0: Disable DRQ (CPU polling mode) 1: Enable DRQ (DMA mode)
3	/	/	/
2	R/W	0	RX FIFO Empty Interrupt Enable 0: Disable 1: Enable Notes: If it is set to '1', when the number of empty room is no smaller than (>=) the preset threshold, the interrupt is triggered and the correspond flag is set.
1	/	/	/
0	R/W	0	TX FIFO Data Available Interrupt Enable 0: Disable 1: Enable Notes: If it is set to '1', when available data number is no smaller than (>=) the preset threshold, the interrupt is triggered and the correspond flag is set.

30.4.6. Crypto Engine Message Digest[n] Register(Default: 0x00000000)

Offset: 0x4C +4*n			Register Name: CE_MD[n]
Bit	Read/Write	Default/Hex	Description
31:0	R	0	SHA1/ MD5 Message digest MD[n] for SHA1/MD5 (n= 0~4)

30.4.7. Crypto Engine RX FIFO Register(Default: 0x00000000)

Offset: 0x200			Register Name: CE_RX
Bit	Read/Write	Default/Hex	Description
31:0	W	0	32-bits RX FIFO for Input

30.4.8. Crypto Engine TX FIFO Register(Default: 0x00000000)

Offset: 0x204			Register Name: CE_TX
Bit	Read/Write	Default/Hex	Description

31:0	R	0	32-bits TX FIFO for Output

30.5. Crypto Engine Clock Requirement

Clock Name	Description	Requirement
ahb_clk	AHB bus clock	>=24MHz
ce_clk	CE serial clock	<= 150MHz

30.6. Crypto Engine Programming Guide

For SHA1,It should be noted the sequence of the message digest.

Let the message,24-bit ASCII string “abc”,the resulting 160-bit message digest for Fips180-2 is :

a9993e36 4706816a ba3e2571 7850c26c 9cd0d89d

For SHA1 of the Allwinner:

Let the message,24-bit ASCII string “abc”,the read message digest result from CE_MD[n](n=0~4) register,in Hex:

CE_MD[0] = a9993e36

CE_MD[1] = 4706816a

CE_MD[2] = ba3e2571

CE_MD[3] = 7850c26c

CE_MD[4] = 9cd0d89d

It is worth nothing that SHA1 is a big-endian algorithm, the most significant bit is stored in the left-most bit position. But the default access mode of ARM is litter-endian ,so every word of CE_MD[n](n=0~4) register need convert the byte sequence by the software.

Chapter 31 Security ID

31.1. Overview

There is one on chip 128-bit EFUS for security application. It can also be used as root key or for other purposes.

It features:

- 128-bit electrical fuses for root key

31.2. Security ID Register List

Module Name	Base Address
SID	0x01c23800

Register Name	Offset	Description
SID_RKEY0	0x00	Root Key[31:0]
SID_RKEY1	0x04	Root Key[63:32]
SID_RKEY2	0x08	Root Key[95:64]
SID_RKEY3	0x0c	Root Key[127:96]

31.3. Security ID Register Description

31.3.1. SID Root Key 0 Register

Offset: 0x00			Register Name: SID_RKEY0
Bit	Read/Write	Default/Hex	Description
31:0	R	x	Securiy root key[31:0]

31.3.2. SID Root Key 1 Register

Offset: 0x04			Register Name: SID_RKEY1
Bit	Read/Write	Default/Hex	Description
31:0	R	x	Security root key[63:32]

31.3.3. SID Root Key 2 Register

Offset: 0x08			Register Name: SID_RKEY2
Bit	Read/Write	Default/Hex	Description
31:0	R	x	Security root key[95:64]

31.3.4. SID Root Key 3 Register

Offset: 0x0c			Register Name: SID_RKEY3
Bit	Read/Write	Default/Hex	Description
31:0	R	x	Security root key[127:96]

31.3.5. SID Program Control Register(Default: 0x00000000)

Offset: 0x44			Register Name: SID_PCTL
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
7:4	R/W	0	Program index The index value of 32-bits electrical fuses hardware macrocell
3:1	/	/	/
0	R/W	0	Software program start Write ‘1’ to start software program and automatically clear to ‘0’ after program.

Chapter 32 Port Controller

32.1. Overview

The chip has 6 ports for multi-functional input/out pins. They are:

- Port B(PB): 10input/output port
- Port C(PC): 17 input/output port
- Port D(PD): 22 input/output port
- Port E(PE): 12 input/output port
- Port F(PF): 6 input/output port
- Port G(PG): 9 input/output port

These ports can be easily configured by software for various system configurations.

32.2. Port Configuration Table

PIO Name	Multiplex Function Select						
	M0	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
PB0	Input	Output	TWI0_SCK				
PB1	Input	Output	TWI0_SDA				
PB2	Input	Output	PWM				EINT16
PB3	Input	Output	IR_TX				EINT17
PB4	Input	Output	IR_RX				EINT18
PB10	Input	Output	SPI2_CS1				EINT24
PB15	Input	Output	TWI1_SCK				
PB16	Input	Output	TWI1_SDA				
PB17	Input	Output	TWI2_SCK				
PB18	Input	Output	TWI2_SDA				
PC0	Input	Output	NWE	SPI0_MOSI			
PC1	Input	Output	NALE	SPI0_MISO			
PC2	Input	Output	NCLE	SPI0_CLK			
PC3	Input	Output	NCE1	SPI0_CS0			
PC4	Input	Output	NCE0				
PC5	Input	Output	NRE				
PC6	Input	Output	NRB0	SDC2_CMD			
PC7	Input	Output	NRB1	SDC2_CLK			
PC8	Input	Output	NDQ0	SDC2_D0			
PC9	Input	Output	NDQ1	SDC2_D1			
PC10	Input	Output	NDQ2	SDC2_D2			
PC11	Input	Output	NDQ3	SDC2_D3			
PC12	Input	Output	NDQ4	SDC2_D4			
PC13	Input	Output	NDQ5	SDC2_D5			
PC14	Input	Output	NDQ6	SDC2_D6			
PC15	Input	Output	NDQ7	SDC2_D7			
PC19	Input	Output	NDQS				
PD2	Input	Output	LCD_D2	UART2_TX			
PD3	Input	Output	LCD_D3	UART2_RX			

PD4	Input	Output	LCD_D4	UART2_CTS			
PD5	Input	Output	LCD_D5	UART2_RTS			
PD6	Input	Output	LCD_D6	ECRS			
PD7	Input	Output	LCD_D7	ECOL			
PD10	Input	Output	LCD_D10	ERXD0			
PD11	Input	Output	LCD_D11	ERXD1			
PD12	Input	Output	LCD_D12	ERXD2			
PD13	Input	Output	LCD_D13	ERXD3			
PD14	Input	Output	LCD_D14	ERXCK			
PD15	Input	Output	LCD_D15	ERXERR			
PD18	Input	Output	LCD_D18	ERXDV			
PD19	Input	Output	LCD_D19	ETXD0			
PD20	Input	Output	LCD_D20	ETXD1			
PD21	Input	Output	LCD_D21	ETXD2			
PD22	Input	Output	LCD_D22	ETXD3			
PD23	Input	Output	LCD_D23	ETXEN			
PD24	Input	Output	LCD_CLK	ETXCK			
PD25	Input	Output	LCD_DE	ETXERR			
PD26	Input	Output	LCD_HSYNC	EMDC			
PD27	Input	Output	LCD_VSYNC	EMDIO			
PE0	Input		TS_CLK	CSI_PCLK	SPI2_CS0		EINT14
PE1	Input		TS_ERR	CSI_MCLK	SPI2_CLK		EINT15
PE2	Input		TS_SYNC	CSI_HSYNC	SPI2_MOSI		
PE3	Input	Output	TS_DVLD	CSI_VSYNC	SPI2_MISO		
PE4	Input	Output	TS_D0	CSI_D0	SDC2_D0		
PE5	Input	Output	TS_D1	CSI_D1	SDC2_D1		
PE6	Input	Output	TS_D2	CSI_D2	SDC2_D2		
PE7	Input	Output	TS_D3	CSI_D3	SDC2_D3		
PE8	Input	Output	TS_D4	CSI_D4	SDC2_CMD		
PE9	Input	Output	TS_D5	CSI_D5	SDC2_CLK		
PE10	Input	Output	TS_D6	CSI_D6	UART1_TX		
PE11	Input	Output	TS_D7	CSI_D7	UART1_RX		
PF0	Input	Output	SDC0_D1		JTAG_MS1		
PF1	Input	Output	SDC0_D0		JTAG_DI1		
PF2	Input	Output	SDC0_CLK		UART0_TX		
PF3	Input	Output	SDC0_CMD		JTAG_DO1		
PF4	Input	Output	SDC0_D3		UART0_RX		
PF5	Input	Output	SDC0_D2		JTAG_CK1		
PG0	Input		GPS_CLK				EINT0
PG1	Input		GPS_SIG				EINT1
PG2	Input		GPS_MAG				EINT2
PG3	Input	Output			UART1_TX		EINT3
PG4	Input	Output			UART1_RX		EINT4
PG9	Input	Output	SPI1_CS0	UART3_TX			EINT9
PG10	Input	Output	SPI1_CLK	UART3_RX			EINT10
PG11	Input	Output	SPI1_MOSI	UART3_CTS			EINT11
PG12	Input	Output	SPI1_MISO	UART3_RTS			EINT12

32.3. Port Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 6)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 6)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 6)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 6)
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 6)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 6)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 6)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 6)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 6)
PIO_INT_CFG0	0x200	PIO Interrrupt Configure Register 0
PIO_INT_CFG1	0x204	PIO Interrrupt Configure Register 1
PIO_INT_CFG2	0x208	PIO Interrrupt Configure Register 2
PIO_INT_CFG3	0x20C	PIO Interrrupt Configure Register 3
PIO_INT_CTL	0x210	PIO Interrupt Control Register
PIO_INT_STA	0x214	PIO Interrupt Status Register
PIO_INT_DEB	0x218	PIO Interrupt Debounce Register

32.4. Port Register Description

32.4.1. PB Configure Register 0(Default: 0x00000000)

Offset: 0x24			Register Name: PB_CFG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0	/
27	/	/	/
26:24	R/W	0	/
23	/	/	/
22:20	R/W	0	/
19	/	/	/
18:16	R/W	0	PB4 Select 000: Input 001: Output 010: IR_RX 011: / 100: / 101: / 110: EINT18 111: /
15	/	/	/
14:12	R/W	0	PB3 Select 000: Input 001: Output 010: IR_TX 011: / 100: / 101: / 110: EINT17 111: /
11	/	/	/
10:8	R/W	0	PB2 Select 000: Input 001: Output 010: PWM 011: / 100: / 101: / 110: EINT16 111: /
7	/	/	/
6:4	R/W	0	PB1 Select 000: Input 001: Output

			010: TWI0_SDA 100: / 110: /	011: / 101: / 111: /
3	/	/	/	
2:0	R/W	0	PB0 Select 000: Input 010: TWI0_SCK 100: / 110: /	001: Output 011: / 101: / 111: /

32.4.2. PB Configure Register 1(Default: 0x00000000)

Offset: 0x28			Register Name: PB_CFG1	
Bit	Read/Write	Default/Hex	Description	
31	/	/	/	
30:28	R/W	0	PB15 Select 000: Input 010: TWI1_SCK 100: / 110: /	001: Output 011: / 101: / 111: /
27:11	/	/	/	
10:8	R/W	0	PB10 Select 000: Input 010: SPI2_CS1 100: / 110: EINT24	001: Output 011: / 101: / 111: /
7:0	/	/	/	

32.4.3. PB Configure Register 2(Default: 0x00000000)

Offset: 0x2C			Register Name: PB_CFG2	
Bit	Read/Write	Default/Hex	Description	
31:11	/	/	/	
10:8	R/W	0	PB18 Select 000: Input 010: TWI2_SDA 100: / 110: /	001: Output 011: / 101: / 111: /
7	/	/	/	
6:4	R/W	0	PB17 Select 000: Input 010: TWI2_SCK 100: / 110: /	001: Output 011: / 101: / 111: /
3	/	/	/	
2:0	R/W	0	PB16 Select 000: Input 010: TWI1_SDA 100: / 110: /	001: Output 011: / 101: / 111: /

32.4.4. PB Configure Register 3(Default: 0x00000000)

Offset: 0x30			Register Name: PB_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.5. PB Data Register(Default: 0x00000000)

Offset: 0x34			Register Name: PB_DAT
Bit	Read/Write	Default/Hex	Description
31:21	/	/	/
20:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

32.4.6. PB Multi-Driving Register 0(Default: 0x55555555)

Offset: 0x38			Register Name: PB_DRV0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PB[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.7. PB Multi-Driving Register 1(Default: 0x00000155)

Offset: 0x3C			Register Name: PB_DRV1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
[2i+1:2i] (i=0~4)	R/W	0x1	PB[n] Multi-Driving Select (n = 16~20) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.8. PB Pull Register 0(Default: 0x00000000)

Offset: 0x40			Register Name: PB_PULL0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PB[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.9. PB Pull Register 1(Default: 0x00000000)

Offset: 0x44			Register Name: PB_PULL1
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
[2i+1:2i] (i=0~4)	R/W	0x0	PB[n] Pull-up/down Select (n = 16~20) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

32.4.10. PC Configure Register 0(Default: 0x00000000)

Offset: 0x48			Register Name: PC_CFG0	
Bit	Read/Write	Default/Hex	Description	
31	/	/	/	
30:28	R/W	0	PC7 Select 000: Input 010: NRB1 100: / 110: /	 001: Output 011: SDC2_CLK 101: / 111: /
27	/	/	/	
26:24	R/W	0	PC6 Select 000: Input 010: NRB0 100: / 110: /	 001: Output 011: SDC2_CMD 101: / 111: /
23	/	/	/	
22:20	R/W	0	PC5 Select 000: Input 010: NRE 100: / 110: /	 001: Output 011: / 101: / 111: /
19	/	/	/	
18:16	R/W	0	PC4 Select 000: Input 010: NCE0 100: / 110: /	 001: Output 011: / 101: / 111: /
15	/	/	/	
14:12	R/W	0	PC3 Select 000: Input 010: NCE1 100: / 110: /	 001: Output 011: SPI0_CS0 101: / 111: /
11	/	/	/	
10:8	R/W	0	PC2 Select 000: Input 010: NCLE 100: / 110: /	 001: Output 011: SPI0_CLK 101: / 111: /
7	/	/	/	
6:4	R/W	0	PC1 Select 000: Input 010: NALE 100: / 110: /	 001: Output 011: SPI0_MISO 101: / 111: /
3	/	/	/	
2:0	R/W	0	PC0 Select 000: Input 010: NWE 100: / 110: /	 001: Output 011: SPI0_MOSI 101: / 111: /

32.4.11. PC Configure Register 1(Default: 0x00000000)

Offset: 0x4C			Register Name: PC_CFG1	
Bit	Read/Write	Default/Hex	Description	
31	/	/	/	
30:28	R/W	0	PC15 Select 000: Input 010: NDQ7 100: / 110: /	 001: Output 011: SDC2_D7 101: / 111: /
27	/	/	/	
26:24	R/W	0	PC14 Select 000: Input 010: NDQ6 100: / 110: /	 001: Output 011: SDC2_D6 101: / 111: /
23	/	/	/	
22:20	R/W	0	PC13 Select 000: Input 010: NDQ5 100: / 110: /	 001: Output 011: SDC2_D5 101: / 111: /
19	/	/	/	
18:16	R/W	0	PC12 Select 000: Input 010: NDQ4 100: / 110: /	 001: Output 011: SDC2_D4 101: / 111: /
15	/	/	/	
14:12	R/W	0	PC11 Select 000: Input 010: NDQ3 100: / 110: /	 001: Output 011: SDC2_D3 101: / 111: /
11	/	/	/	
10:8	R/W	0	PC10 Select 000: Input 010: NDQ2 100: / 110: /	 001: Output 011: SDC2_D2 101: / 111: /
7	/	/	/	
6:4	R/W	0	PC9 Select 000: Input 010: NDQ1 100: / 110: /	 001: Output 011: SDC2_D1 101: / 111: /
3	/	/	/	
2:0	R/W	0	PC8 Select 000: Input 010: NDQ0 100: / 110: /	 001: Output 011: SDC2_D0 101: / 111: /

32.4.12. PC Configure Register 2(Default: 0x00000000)

Offset: 0x50			Register Name: PC_CFG2
Bit	Read/Write	Default/Hex	Description
31:16	/	/	/
15	/	/	/
14:12	R/W	0	PC19 Select 000: Input 001: Output 010: NDQS 011: / 100: / 101: / 110: / 111: /
11:0	/	/	/

32.4.13. PC Configure Register 3(Default: 0x00000000)

Offset: 0x54			Register Name: PC_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.14. PC Data Register(Default: 0x00000000)

Offset: 0x58			Register Name: PC_DAT
Bit	Read/Write	Default/Hex	Description
31:20	/	/	/
19:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

32.4.15. PC Multi-Driving Register 0(Default: 0x55555555)

Offset: 0x5C			Register Name: PC_DRV0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PC[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.16. PC Multi-Driving Register 1(Default: 0x00000055)

Offset: 0x60			Register Name: PC_DRV1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
[2i+1:2i] (i=0~3)	R/W	0x1	PC[n] Multi-Driving Select (n = 16~19) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.17. PC Pull Register 0(Default: 0x00005140)

Offset: 0x64			Register Name: PC_PULL0
Bit	Read/Write	Default/Hex	Description

[2i+1:2i] (i=0~15)	R/W	0x0000_5140	PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.18. PC Pull Register 1(Default: 0x00000016)

Offset: 0x68			Register Name: PC_PULL1
Bit	Read/Write	Default/Hex	Description
31:8	/	/	/
[2i+1:2i] (i=0~3)	R/W	0x16	PC[n] Pull-up/down Select (n = 16~19) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.19. PD Configure Register 0(Default: 0x00000000)

Offset: 0x6C			Register Name: PD_CFG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0	PD7 Select 000: Input 001: Output 010: LCD_D7 011: ECOL 100: / 101: / 110: / 111: /
27	/	/	/
26:24	R/W	0	PD6 Select 000: Input 001: Output 010: LCD_D6 011: ECRS 100: / 101: / 110: / 111: /
23	/	/	/
22:20	R/W	0	PD5 Select 000: Input 001: Output 010: LCD_D5 011: UART2_RTS 100: / 101: / 110: / 111: /
19	/	/	/
18:16	R/W	0	PD4 Select 000: Input 001: Output 010: LCD_D4 011: UART2_CTS 100: / 101: / 110: / 111: /
15	/	/	/
14:12	R/W	0	PD3 Select 000: Input 001: Output 010: LCD_D3 011: UART2_RX 100: / 101: / 110: / 111: /
11	/	/	/
10:8	R/W	0	PD2 Select 000: Input 001: Output 010: LCD_D2 011: UART2_TX 100: / 101: / 110: / 111: /

7	/	/	/
6:4	R/W	0	/
3	/	/	/
2:0	R/W	0	/

32.4.20. PD Configure Register 1(Default: 0x00000000)

Offset: 0x70			Register Name: PD_CFG1
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0	PD15 Select 000: Input 001: Output 010: LCD_D15 011: ERXERR 100: / 101: / 110: / 111: /
27	/	/	/
26:24	R/W	0	PD14 Select 000: Input 001: Output 010: LCD_D14 011: ERXCK 100: / 101: / 110: / 111: /
23	/	/	/
22:20	R/W	0	PD13 Select 000: Input 001: Output 010: LCD_D13 011: ERXD3 100: / 101: / 110: / 111: /
19	/	/	/
18:16	R/W	0	PD12 Select 000: Input 001: Output 010: LCD_D12 011: ERXD2 100: / 101: / 110: / 111: /
15	/	/	/
14:12	R/W	0	PD11 Select 000: Input 001: Output 010: LCD_D11 011: ERXD1 100: / 101: / 110: / 111: /
11	/	/	/
10:8	R/W	0	PD10 Select 000: Input 001: Output 010: LCD_D10 011: ERXD0 100: / 101: / 110: / 111: /
7	/	/	/
6:4	R/W	0	/
3	/	/	/
2:0	R/W	0	/

32.4.21. PD Configure Register 2(Default: 0x00000000)

Offset: 0x74			Register Name: PD_CFG2	
Bit	Read/Write	Default/Hex	Description	
31	/	/	/	
30:28	R/W	0	PD23 Select 000: Input 010: LCD_D23 100: / 110: /	 001: Output 011: ETXEN 101: / 111: /
27	/	/	/	
26:24	R/W	0	PD22 Select 000: Input 010: LCD_D22 100: / 110: /	 001: Output 011: ETXD3 101: / 111: /
23	/	/	/	
22:20	R/W	0	PD21 Select 000: Input 010: LCD_D21 100: / 110: /	 001: Output 011: ETXD2 101: / 111: /
19	/	/	/	
18:16	R/W	0	PD20 Select 000: Input 010: LCD_D20 100: / 110: /	 001: Output 011: ETXD1 101: / 111: /
15	/	/	/	
14:12	R/W	0	PD19 Select 000: Input 010: LCD_D19 100: / 110: /	 001: Output 011: ETXD0 101: / 111: /
11	/	/	/	
10:8	R/W	0	PD18 Select 000: Input 010: LCD_D18 100: / 110: /	 001: Output 011: ERXDV 101: / 111: /
7	/	/	/	
6:4	R/W	0	/	
3	/	/	/	
2:0	R/W	0	/	

32.4.22. PD Configure Register 3(Default: 0x00000000)

Offset: 0x78			Register Name: PD_CFG3	
Bit	Read/Write	Default/Hex	Description	
31:16	/	/	/	
15	/	/	/	
14:12	R/W	0	PD27 Select 000: Input	 001: Output

			010: LCD_VSYNC 100: / 110: /	011: EMDIO 101: / 111: /
11	/	/	/	
10:8	R/W	0	PD26 Select 000: Input 010: LCD_HSYNC 100: / 110: /	001: Output 011: EMDC 101: / 111: /
7	/	/	/	
6:4	R/W	0	PD25 Select 000: Input 010: LCD_DE 100: / 110: /	001: Output 011: ETXERR 101: / 111: /
3	/	/	/	
2:0	R/W	0	PD24 Select 000: Input 010: LCD_CLK 100: / 110: /	001: Output 011: ETXCK 101: / 111: /

32.4.23. PD Data Register(Default: 0x00000000)

Offset: 0x7C			Register Name: PD_DAT
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
27:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

32.4.24. PD Multi-Driving Register 0(Default: 0x55555555)

Offset: 0x80			Register Name: PD_DRV0
Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.25. PD Multi-Driving Register 1(Default: 0x00555555)

Offset: 0x84			Register Name: PD_DRV1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PD[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.26. PD Pull Register 0(Default: 0x00000000)

Offset: 0x88	Register Name: PD_PULL0

Bit	Read/Write	Default/Hex	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.27. PD Pull Register 1(Default: 0x00000000)

Offset: 0x8C			Register Name: PD_PULL1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PD[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable 10: Pull-down 11: Reserved

32.4.28. PE Configure Register 0(Default: 0x00000000)

Offset: 0x90			Register Name: PE_CFG0
Bit	Read/Write	Default/Hex	Description
31	/	/	/
30:28	R/W	0	PE7 Select 000: Input 001: Output 010: TS_D3 011: CSI_D3 100: SDC2_D3 101: / 110: / 111: /
27	/	/	/
26:24	R/W	0	PE6 Select 000: Input 001: Output 010: TS_D2 011: CSI_D2 100: SDC2_D2 101: / 110: / 111: /
23	/	/	/
22:20	R/W	0	PE5 Select 000: Input 001: Output 010: TS_D1 011: CSI_D1 100: SDC2_D1 101: / 110: / 111: /
19	/	/	/
18:16	R/W	0	PE4 Select 000: Input 001: Output 010: TS_D0 011: CSI_D0 100: SDC2_D0 101: / 110: / 111: /
15	/	/	/
14:12	R/W	0	PE3 Select 000: Input 001:Output 010: TS_DVLD 011: CSI_VSYNC 100: SPI2_MISO 101: / 110: / 111: /
11	/	/	/
10:8	R/W	0	PE2 Select 000: Input 001: Reserved 010: TS_SYNC 011:CSI_HSYNC 100: SPI2_MOSI 101: /

			110: /	111: /
7	/	/	/	
6:4	R/W	0	PE1 Select 000: Input 010: TS_ERR 100: SPI2_CLK 110: EINT15	001: Reserved 011: CSI_MCLK 101: / 111: /
3	/	/	/	
2:0	R/W	0	PE0 Select 000: Input 010: TS_CLK 100: SPI2_CS0 110: EINT14	001: Reserved 011: CSI_PCLK 101: / 111: /

32.4.29. PE Configure Register 1(Default: 0x00000000)

Offset: 0x94			Register Name: PE_CFG1	
Bit	Read/Write	Default/Hex	Description	
31:16	/	/	/	
15	/	/	/	
14:12	R/W	0	PE11 Select 000: Input 010: TS_D7 100: UART1_RX 110: /	001: Output 011: CSI_D7 101: / 111: /
11	/	/	/	
10:8	R/W	0	PE10 Select 000: Input 010: TS_D6 100: UART1_TX 110: /	001: Output 011: CSI_D6 101: / 111: /
7	/	/	/	
6:4	R/W	0	PE9 Select 000: Input 010: TS_D5 100: SDC2_CLK 110: /	001: Output 011: CSI_D5 101: / 111: /
3	/	/	/	
2:0	R/W	0	PE8 Select 000: Input 010: TS_D4 100: SDC2_CMD 110: /	001: Output 011: CSI_D4 101: / 111: /

32.4.30. PE Configure Register 2(Default: 0x00000000)

Offset: 0x98			Register Name: PE_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.31. PE Configure Register 3(Default: 0x00000000)

Offset: 0x9C			Register Name: PE_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.32. PE Data Register(Default: 0x00000000)

Offset: 0xA0			Register Name: PE_DAT
Bit	Read/Write	Default/Hex	Description
31:12	/	/	/
11:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

32.4.33. PE Multi-Driving Register 0(Default: 0x00555555)

Offset: 0xA4			Register Name: PE_DRV0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PE[n] Multi-Driving Select (n = 0~11) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.34. PE Multi-Driving Register 1(Default: 0x00000000)

Offset: 0xA8			Register Name: PE_DRV1
Bit	Read/Write	Default	Description
31:0	/	/	/

32.4.35. PE Pull Register 0(Default: 0x00000000)

Offset: 0xAC			Register Name: PE_PULL0
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PE[n] Pull-up/down Select (n = 0~11) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.36. PE Pull Register 1(Default: 0x00000000)

Offset: 0xB0			Register Name: PE_PULL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.37. PF Configure Register 0(Default: 0x00404044)

Offset: 0xB4			Register Name: PF_CFG0
Bit	Read/Write	Default/Hex	Description

31:24	/	/	/
23	/	/	/
22:20	R/W	0x4	PF5 Select 000: Input 001: Output 010: SDC0_D2 011: / 100: JTAG_CK1 101: / 110: / 111: /
19	/	/	/
18:16	R/W	0x0	PF4 Select 000: Input 001: Output 010: SDC0_D3 011: / 100: UART0_RX 101: / 110: / 111: /
15	/	/	/
14:12	R/W	0x4	PF3 Select 000: Input 001: Output 010: SDC0_CMD 011: / 100: JTAG_DO1 101: / 110: / 111: /
11	/	/	/
10:8	R/W	0	PF2 Select 000: Input 001: Output 010: SDC0_CLK 011: / 100: UART0_TX 101: / 110: / 111: /
7	/	/	/
6:4	R/W	0x4	PF1 Select 000: Input 001: Output 010: SDC0_D0 011: / 100: JTAG_DI1 101: / 110: / 111: /
3	/	/	/
2:0	R/W	0x4	PF0 Select 000: Input 001: Output 010: SDC0_D1 011: / 100: JTAG_MS1 101: / 110: / 111: /

32.4.38. PF Configure Register 1(Default: 0x00000000)

Offset: 0xB8			Register Name: PF_CFG1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.39. PF Configure Register 2(Default: 0x00000000)

Offset: 0xBC			Register Name: PF_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.40. PF Configure Register 3(Default: 0x00000000)

Offset: 0xC0			Register Name: PF_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.41. PF Data Register(Default: 0x00000000)

Offset: 0xC4			Register Name: PF_DAT
Bit	Read/Write	Default/Hex	Description
31:6	/	/	/
5:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

32.4.42. PF Multi-Driving Register 0(Default: 0x00000155)

Offset: 0xC8			Register Name: PF_DRV0
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x1	PF[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.43. PF Multi-Driving Register 1(Default: 0x00000000)

Offset: 0xCC			Register Name: PF_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.44. PF Pull Register 0(Default: 0x00000000)

Offset: 0xD0			Register Name: PF_PULL0
Bit	Read/Write	Default/Hex	Description
31:10	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PF[n] Pull-up/down Select (n = 0~5) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.45. PF Pull Register 1(Default: 0x00000000)

Offset: 0xD4			Register Name: PF_PULL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.46. PG Configure Register 0(Default: 0x00000000)

Offset: 0xD8			Register Name: PG_CFG0
Bit	Read/Write	Default/Hex	Description

31	/	/	/
30:28	R/W	0	/
27	/	/	/
26:24	R/W	0	/
23	/	/	/
22:20	R/W	0	/
19	/	/	/
18:16	R/W	0	PG4 Select 000: Input 001: Output 010: / 011: / 100: UART1_RX 101: / 110: EINT4 111: /
15	/	/	/
14:12	R/W	0	PG3 Select 000: Input 001: Output 010: / 011: / 100: UART1_TX 101: / 110: EINT3 111: /
11	/	/	/
10:8	R/W	0	PG2 Select 000: Input 001: Reserved 010: GPS_MAG 011: / 100: / 101: / 110: EINT2 111: /
7	/	/	/
6:4	R/W	0	PG1 Select 000: Input 001: Reserved 010: GPS_SIGN 011: / 100: / 101: / 110: EINT1 111: /
3	/	/	/
2:0	R/W	0	PG0 Select 000: Input 001: Reserved 010: GPS_CLK 011: / 100: / 101: / 110: EINT0 111: /

32.4.47. PG Configure Register 1(Default: 0x00000000)

Offset: 0xDC			Register Name: PG_CFG1
Bit	Read/Write	Default/Hex	Description
31:24	/	/	/
23	/	/	/
22:20	R/W	0	/
19	/	/	/
18:16	R/W	0	PG12 Select 000: Input 001: Output 010: SPI1_MISO 011: UART3_RTS 100: / 101: / 110: EINT12 111: /
15	/	/	/

14:12	R/W	0	PG11 Select 000: Input 001: Output 010: SPI1_MOSI 011: UART3_CTS 100: / 101: / 110: EINT11 111: /
11	/	/	/
10:8	R/W	0	PG10 Select 000: Input 001: Output 010: SPI1_CLK 011: UART3_RX 100: / 101: / 110: EINT10 111: /
7	/	/	/
6:4	R/W	0	PG9 Select 000: Input 001: Output 010: SPI1_CS0 011: UART3_TX 100: / 101: / 110: EINT9 111: /
3	/	/	/
2:0	R/W	0	/

32.4.48. PG Configure Register 2(Default: 0x00000000)

Offset: 0xE0			Register Name: PG_CFG2
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.49. PG Configure Register 3(Default: 0x00000000)

Offset: 0xE4			Register Name: PG_CFG3
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.50. PG Data Register(Default: 0x00000000)

Offset: 0xE8			Register Name: PG_DAT
Bit	Read/Write	Default/Hex	Description
31:14	/	/	/
13:0	R/W	0	If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

32.4.51. PG Multi-Driving Register 0(Default: 0x05555555)

Offset: 0xEC			Register Name: PG_DRV0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x1	PG[n] Multi-Driving Select (n = 0~13) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

32.4.52. PG Multi-Driving Register 1(Default: 0x00000000)

Offset: 0xF0			Register Name: PG_DRV1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.53. PG Pull Register 0(Default: 0x00000000)

Offset: 0xF4			Register Name: PG_PULL0
Bit	Read/Write	Default/Hex	Description
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x0	PG[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

32.4.54. PG Pull Register 1(Default: 0x00000000)

Offset: 0xF8			Register Name: PG_PULL1
Bit	Read/Write	Default/Hex	Description
31:0	/	/	/

32.4.55. PIO Interrupt Configure Register 0(Default: 0x00000000)

Offset: 0x200			Register Name: PIO_INT_CFG0
Bit	Read/Write	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

32.4.56. PIO Interrupt Configure Register 1(Default: 0x00000000)

Offset: 0x204			Register Name: PIO_INT_CFG1
Bit	Read/Write	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	External INTn Mode (n = 8~15) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

32.4.57. PIO Interrupt Configure Register 2(Default: 0x00000000)

Offset: 0x208			Register Name: PIO_INT_CFG2
Bit	Read/Write	Default/Hex	Description
[4i+3:4i]	R/W	0	External INTn Mode (n = 16~23)

(i=0~7)			0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

32.4.58. PIO Interrupt Configure Register 3(Default: 0x00000000)

Offset: 0x20C			Register Name: PIO_INT_CFG3
Bit	Read/Write	Default/Hex	Description
[4i+3:4i] (i=0~7)	R/W	0	External INTn Mode (n = 24~31) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

32.4.59. PIO Interrupt Control Register(Default: 0x00000000)

Offset: 0x210			Register Name: PIO_INT_CTL
Bit	Read/Write	Default/Hex	Description
[n] (n=0~31)	R/W	0	External INTn Enable (n = 0~31) 0: Disable 1: Enable

32.4.60. PIO Interrupt Status Register(Default: 0x00000000)

Offset: 0x214			Register Name: PIO_INT_STATUS
Bit	Read/Write	Default/Hex	Description
[n] (n=0~31)	R/W	0	External INTn Pending Bit (n = 0~31) 0: No IRQ pending 1: IRQ pending Write '1' to clear it.

32.4.61. PIO Interrupt Debounce Register(Default: 0x00000000)

Offset: 0x218			Register Name: PIO_INT_DEB
Bit	Read/Write	Default/Hex	Description
31:7	/	/	/
6:4	R/W	0	Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/
0	R/W	0	PIO Interrupt Clock Select 0: 32KHz 1: 24MHz